AMPLIFIER REFERENCE MANUAL

OPERATIONAL AMPLIFIERS •

INSTRUMENTATION AMPLIFIERS •

ISOLATION AMPLIFIERS • BUFFER AMPLIFIERS •

COMPARATORS • ASICs

ANALOG DEVICES

How to Find Product Data in This Reference Manual

THIS VOLUME

Contains Data Sheets, Selection Guides and a wealth of background information on op amps, in amps, comparators and isolation amps.

It is one member of a five-volume set of reference manuals describing and specifying Amplifier, Special Linear, Converter and Audio/Video products from Analog Devices, Inc., in IC, hybrid and assembled form for measurement, control and real-world signal processing.

IF YOU KNOW THE MODEL NUMBER

Turn to the product index at the back of the book and look up the model number. You will find the Volume-Section-Page location of any data sheet in this volume or its companion manual, the *Special Linear Reference Manual*. You will find additional references for all other Analog Devices product categories currently available.

If you're looking for a form-and-function-compatible version of a product originally brought to market by some other manufacturer (second source), you may find it by adding our "AD" prefix and looking it up in the index. Or call our nearest sales office.

IF YOU DON'T KNOW THE MODEL NUMBER

Find your functional group in the list on the opposite page. Turn directly to the appropriate Section. You will find a functional Selection Tree and Selection Guide at the beginning of the Section. The Selection Tree and Selection Guide (and the accompanying "Orientation") and will help you find the products that are the closest to satisfying your need. Use them to compare all products in the category by salient criteria. A comprehensive Table of Contents is provided for your convenience on pages 1–5 through 1–9.

IF YOU CAN'T FIND IT HERE . . . ASK!

If it's not an amplifier product, it's probably in one of the four companion volumes, the *Special Linear Reference Manual*, the *Audio/Video Reference Manual*, or the *Data Converter Reference Manual (Volume I* or *II)*. If you don't already own these volumes, you can have them FREE by getting in touch with Analog Devices or the nearest sales office, or phoning 1-800-262-5643.

See the Worldwide Sales Directory on pages 9–12 and 9–13 at the back of this volume for our sales office phone numbers.

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Power Supplies

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Introduction

Analog Devices, a *Fortune* 500 Industrials company, designs, manufactures and sells worldwide sophisticated electronic components and subsystems for use in real-world signal processing. More than six hundred standard products are produced in manufacturing facilities located throughout the world. These facilities encompass all relevant technologies, including several embodiments of CMOS, BiMOS, bipolar and hybrid integrated circuits, each optimized for specific attributes—and assembled products in the form of potted modules, printed-circuit boards and instrument packages.

State-of-the-art technologies (including surface micromachining) have been utilized (and in many cases invented) to provide timely, reliable, easy-to-use advanced designs at realistic prices. Our popular IC products are available in both conventional and surface-mount packages (SOIC, LCC, PLCC), and many of our assembled products employ surface-mount technology to reduce manufacturing costs and overall size. A quarter-century of successful applications experience and continuing vertical integration insure that these products are oriented to user needs. The ongoing application of today's state-of-the-art and the invention of tomorrow's state-of-the-art processes strengthen the leadership position of Analog Devices in standard data-acquisition and signal-processing products and make us a strong contender in high performance mixed-signal ASICs.

MAJOR PROGRESS

Since publication of the selection guides in the *1990/91 Linear Products Databook*, Analog Devices has introduced more than 120 significant new products; they run the gamut from brand new product and market categories and technologies to standard products (with improvements in price, performance, or design) to augmented second-source products. In addition to these new products, we now include the products of Precision Monolithics, Inc., which was acquired by Analog Devices in 1990. The combined company is the world's largest manufacturer of high performance op amps and second in standard linear ICs. The new amplifier products are all classified and summarized here, along with existing devices that are appropriate and desirable for use in new designs. More than 100 standard op amp families are included here.

Examples of the variety, performance, and innovation content of outstanding new amplifier ICs to be found in this volume include:

- **AD797** low noise and distortion (<1 nV/$\sqrt{\text{Hz}}$, 3 ppm), 75 MHz GBWP operational amplifier (op amp)
- **AD811** high performance (0.01%, 0.01° differential gain and phase) video op amp
- **AD206** high-performance (100 kHz bandwidth, low nonlinearity and distortion) internally powered isolation amplifier
- **OP-497** high precision (50 μV max V_{OS}, 0.5 μV/°C drift, 450 pA up to 125°C I_b), low power (625 μA/channel) *quadruple* op amp
- **AD620** low cost, high accuracy (50 μV V_{OS}, 0.6 μV/°C drift, 1 nA I_b) instrumentation amplifier (in amp)
- **OP-282/OP-482** low dissipation (250 μA/channel) 4 MHz, 1.6 μs (0.01%) settling time, low cost dual/quad J-FET op amp
- **OP-275** dual low distortion, low power audio op amp
- **OP-295** dual single-supply (+3 to 36 V) op amp with rail-to-rail output range

Many more could have been added to this list.

AMPLIFIER REFERENCE MANUAL

This volume provides comprehensive technical data on Analog Devices amplifier products, principally operational amplifiers, instrumentation amplifiers, isolation amplifiers, and comparators. It is a companion to the *Special Linear Reference Manual*, which includes data on other analog signal-processing products, such as multiplier/dividers, rms-to-dc converters, sensors and signal conditioners, and devices oriented to the computer, mass-storage, automotive, process control, and ATE markets. Both are members of the series of Analog Devices *Reference Manuals*, which includes the *Audio/Video Reference Manual*, and the two-volume *Data-Converter Reference Manual*.

In the more than 1,000 pages of this volume you will find:

- comprehensive data sheets and package information on >150 significant product families
- orientation material and selection guides/trees for finding products rapidly
- a representative list of available Analog Devices technical publications on real-world analog and digital signal processing
- our Worldwide Sales Directory
- the complete Product Index to all amplifier and special linear products listed in these two volumes, data conversion products listed in the *Data Converter Reference Manual* (Volumes I and II), products with audio and video signal processing applications listed in the *Audio/Video Reference Manual*, and DSP products for which data sheets are available.

The product data in this book are intended primarily for the majority of users who are concerned with new designs. For this reason, existing and available products that offer little if any unique advantage over newer products in future designs are listed in the Index, and data sheets may be available separately —but they are not published in this book.

TECHNICAL SUPPORT

Our extensive technical literature discusses the technology and applications of products for real-world signal processing. Besides tutorial material and comprehensive data sheets, including a large number in our Reference Manuals, we offer Application Notes, Application Guides, Technical Handbooks (at reasonable prices), and several free serial publications; for example, *Analog Productlog* provides brief information on new products being introduced, and *Analog Dialogue*, our technical magazine, provides in-depth discussions of new developments in analog and digital circuit technology as applied to data acquisition, signal processing, control, and test. *DSPatch*™ is a quarterly newsletter that brings its readers up-to-date applications information on our DSP products and the general field of digital signal processing. We maintain a mailing list of engineers, scientists, and technicians with a serious interest in our products. In addition to these Reference Manual catalogs—and general short-form selection guides—we also publish several short-form catalogs on specific product families. You will find typical publications described on pages 9–8 to 9–11 at the back of the book.

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SALES AND SERVICE

Backing up our design and manufacturing capabilities and our extensive array of publications, is a network of distributors, plus sales offices and representatives throughout the United States and most of the world, staffed by experienced sales and applications engineers. Our Worldwide Sales Directory, as of the publication date, appears on pages 9–12 and 9–13 at the back of the book.

RELIABILITY

The manufacture of reliable products is a key objective at Analog Devices. The primary focus is a companywide Total Quality Management (TQM) Program. In addition, we maintain facilities that have been qualified under such standards as MIL-M-38510 (Class B and Class S) for ICs in the U.S., MIL-STD-1772 for hybrids, and ISO9000 (required by many European customers). Many of our products—both proprietary and second-source—have qualified for JAN part numbers; others are in the process. A larger number of products—including many of the newer ones just starting the JAN qualification process—are specifically characterized on Standard Military Drawings (SMDs). Most of our ICs are available in versions that comply with MIL-STD-883C Class B, and many also comply with Class S. We publish a *Military Products Databook* for designers who specify ICs and hybrids for military contracts. The 1990 issue consists of two volumes with data on 343 product families; the 120 entries in the second of those volumes describe qualified products manufactured by our PMI Division. A newsletter, *Analog Briefings*®, provides current information about the status of reliability at ADI.

Our PLUS program makes available standard devices (commercial and industrial grades, plastic or ceramic packaging) for *any* user with demanding application environments, at a small premium. Subjected to stringent screening, similar to MIL-STD-883 test methods, these devices are suffixed "/+" and are available from stock.

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PRODUCTS NOT FOUND IN THE SELECTION GUIDES

For maximum usefulness to designers of new equipment, we have limited the contents of selection guides to standard products most likely to be used for the design of new circuits and systems. If the model number of a product you are interested in is not in the Index, turn to page 9–4 at the back of this volume where you will find a list of older products for which data sheets are available upon request. On page 9–5 you will find a guide to substitutions (where possible) for products no longer available.

ICs embodying combinations of functions that you need but cannot find among our standard offerings may be available to meet your specific requirements as custom designs. Consult the section in this book on Application Specific ICs—and/or get in touch with Analog Devices.

PRICES

Accurate, up-to-date prices are an important consideration in making a choice among the many available product families. Since prices are subject to change, current price lists and/or quotations are available upon request from our sales offices and distributors.

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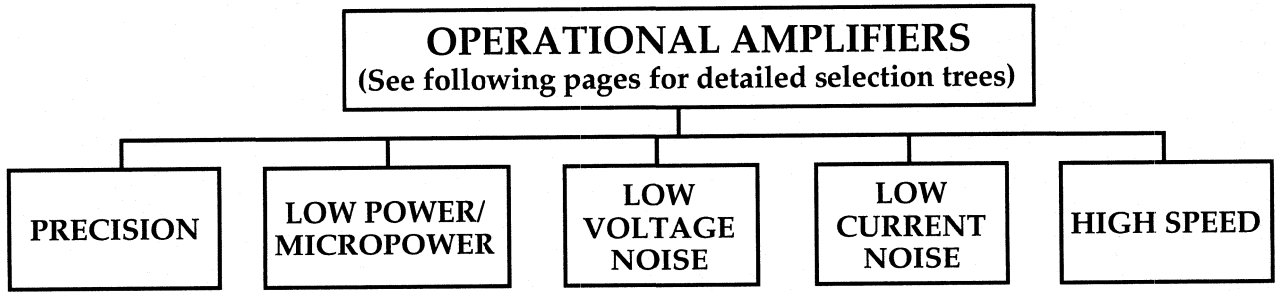
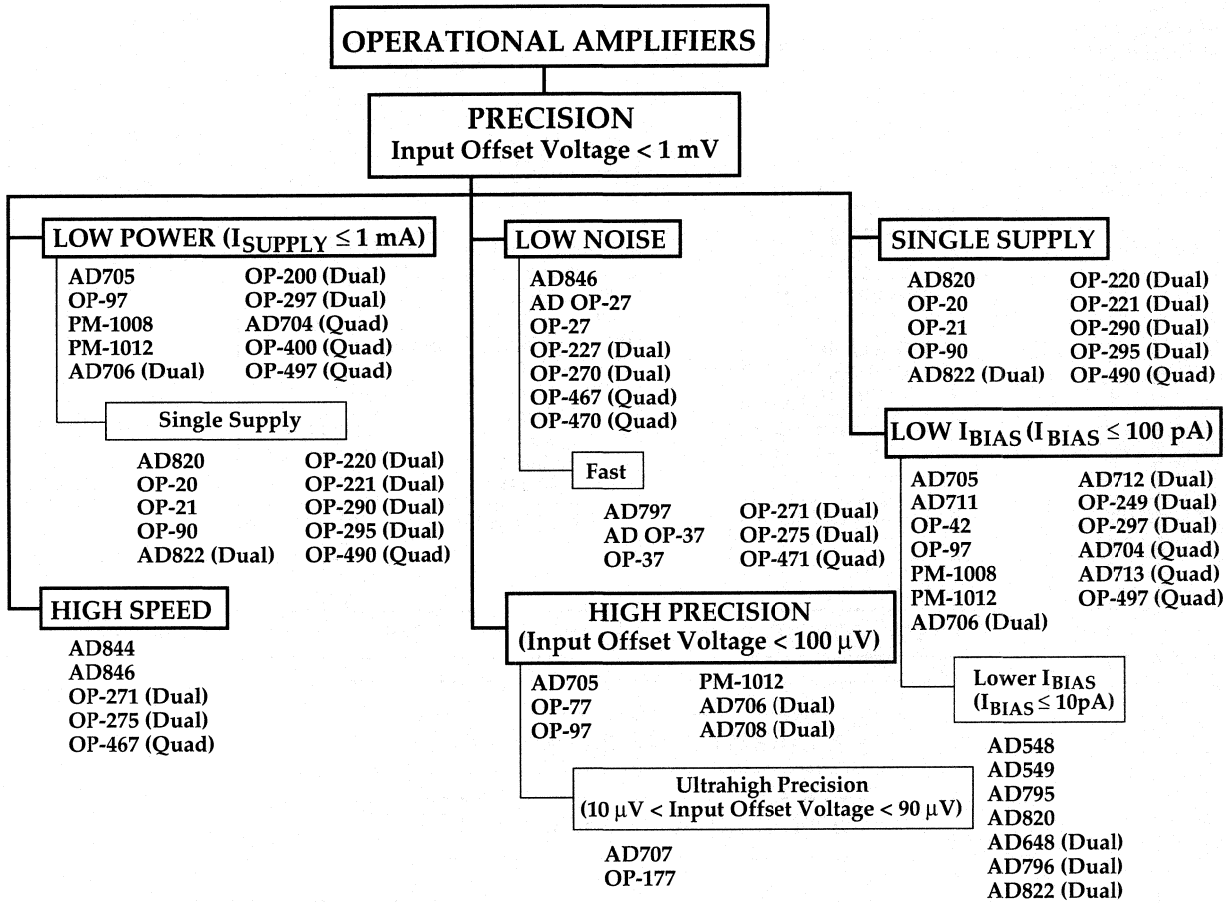
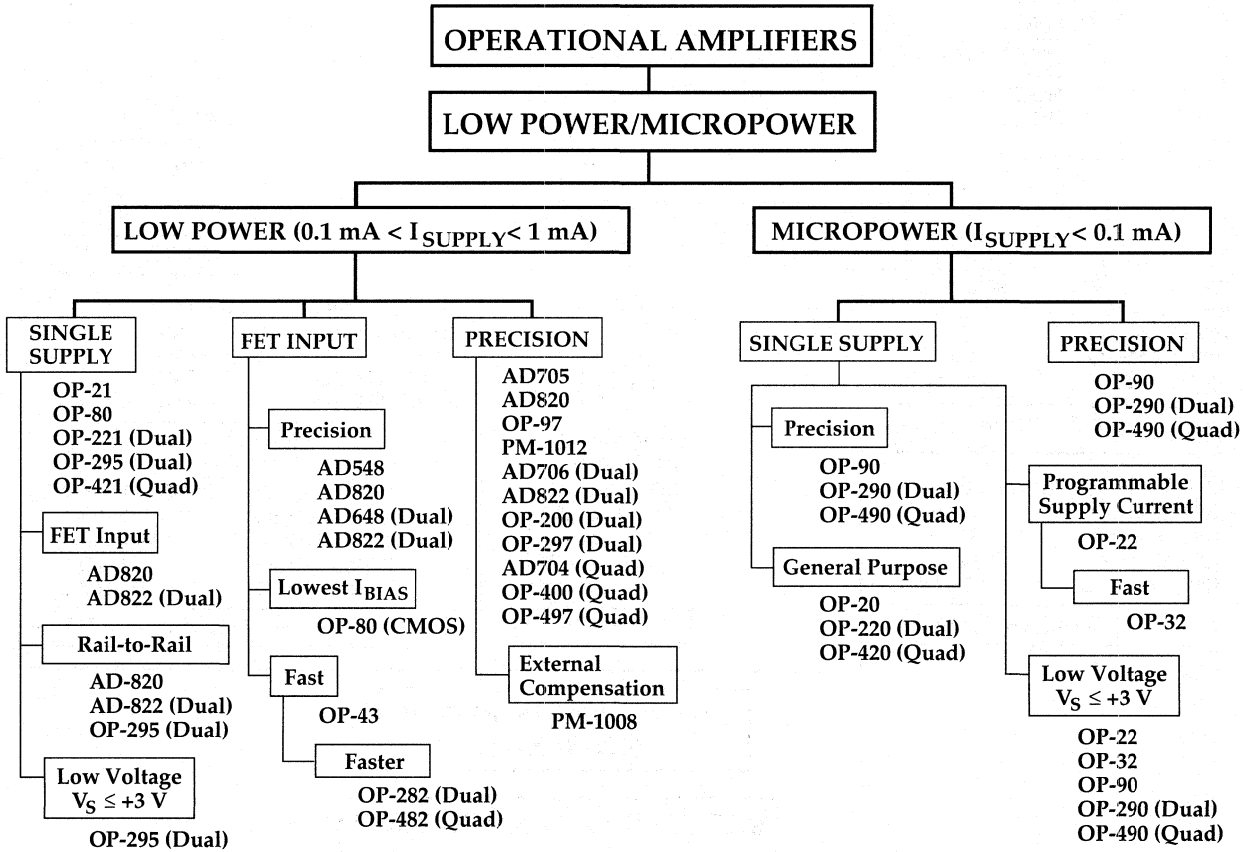
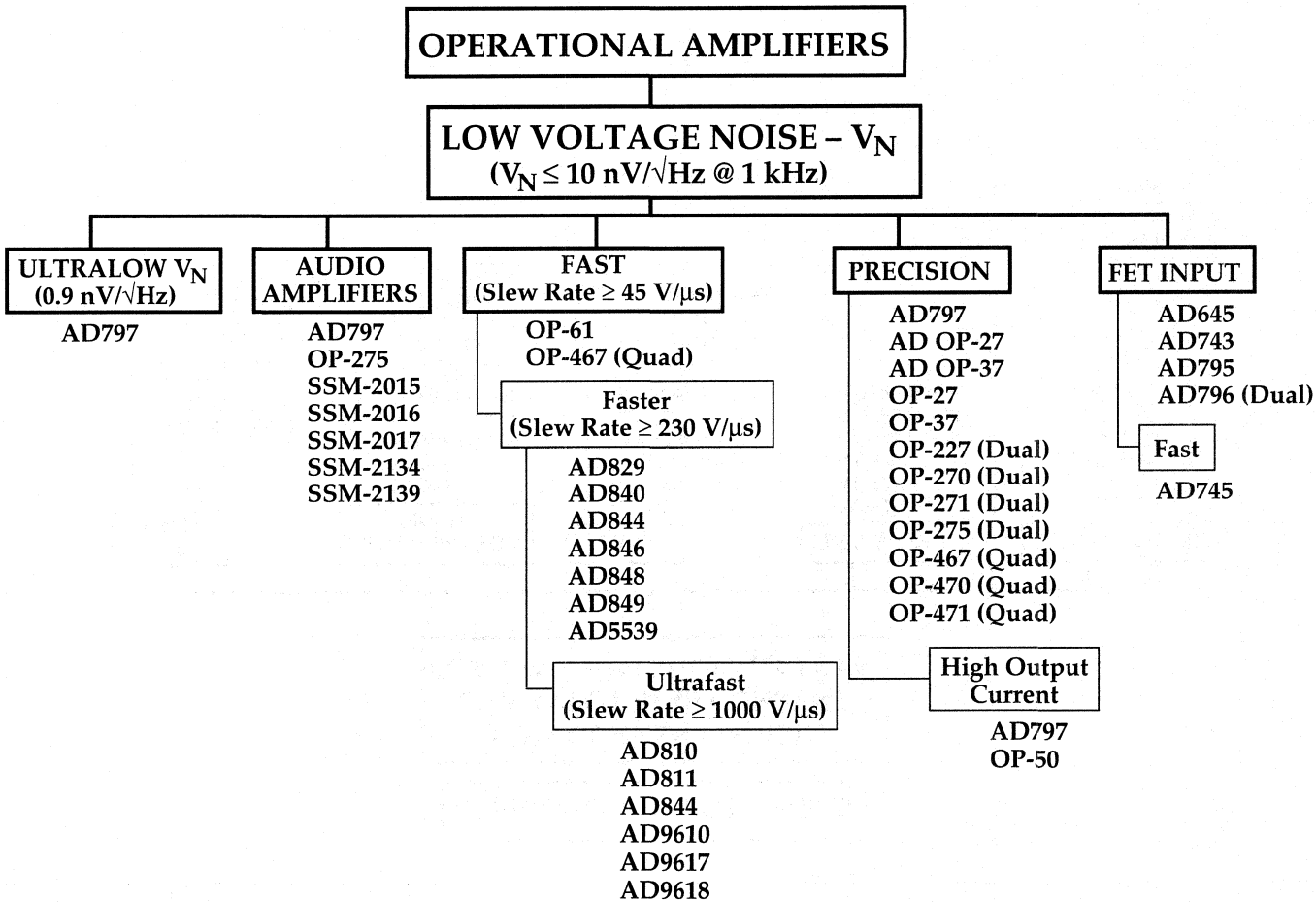
Selection Trees
Operational Amplifiers



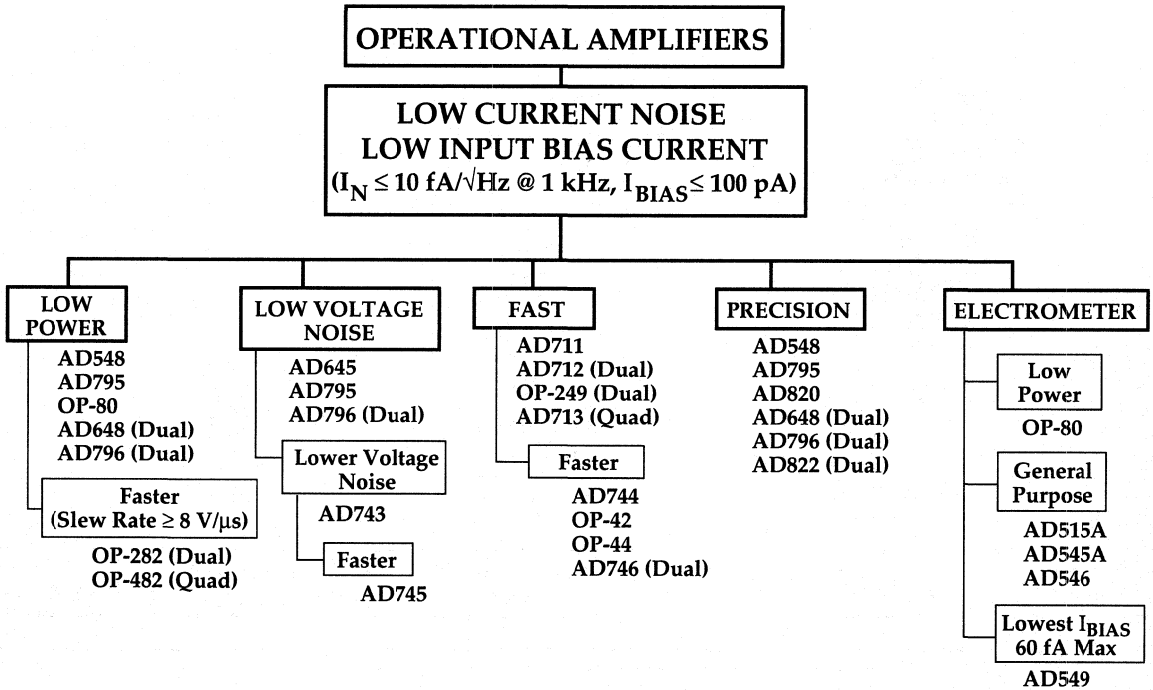

OPERATIONAL AMPLIFIERS
PRECISION
Input Offset Voltage < 1 mV
LOW POWER ($I_{SUPPLY} \leq 1$ mA)
AD705
OP-97
PM-1008
PM-1012
AD706 (Dual)
OP-200 (Dual)
OP-297 (Dual)
AD704 (Quad)
OP-400 (Quad)
OP-497 (Quad)
Single Supply
AD820
OP-20
OP-21
OP-90
AD822 (Dual)
OP-220 (Dual)
OP-221 (Dual)
OP-290 (Dual)
OP-295 (Dual)
OP-490 (Quad)
HIGH SPEED
AD844
AD846
OP-271 (Dual)
OP-275 (Dual)
OP-467 (Quad)
LOW NOISE
AD846
AD OP-27
OP-27
OP-227 (Dual)
OP-270 (Dual)
OP-467 (Quad)
OP-470 (Quad)
Fast
AD797
AD OP-37
OP-37
OP-271 (Dual)
OP-275 (Dual)
OP-471 (Quad)
HIGH PRECISION
(Input Offset Voltage < 100 μV)
AD705
OP-77
OP-97
PM-1012
AD706 (Dual)
AD708 (Dual)
Ultrahigh Precision
(10 μV < Input Offset Voltage < 90 μV)
AD707
OP-177
SINGLE SUPPLY
AD820
OP-20
OP-21
OP-90
AD822 (Dual)
OP-220 (Dual)
OP-221 (Dual)
OP-290 (Dual)
OP-295 (Dual)
OP-490 (Quad)
LOW I_{BIAS} ($I_{BIAS} \leq 100$ pA)
AD705
AD711
OP-42
OP-97
PM-1008
PM-1012
AD706 (Dual)
AD712 (Dual)
OP-249 (Dual)
OP-297 (Dual)
AD704 (Quad)
AD713 (Quad)
OP-497 (Quad)
Lower I_{BIAS}
($I_{BIAS} \leq 10$pA)
AD548
AD549
AD795
AD820
AD648 (Dual)
AD796 (Dual)
AD822 (Dual)

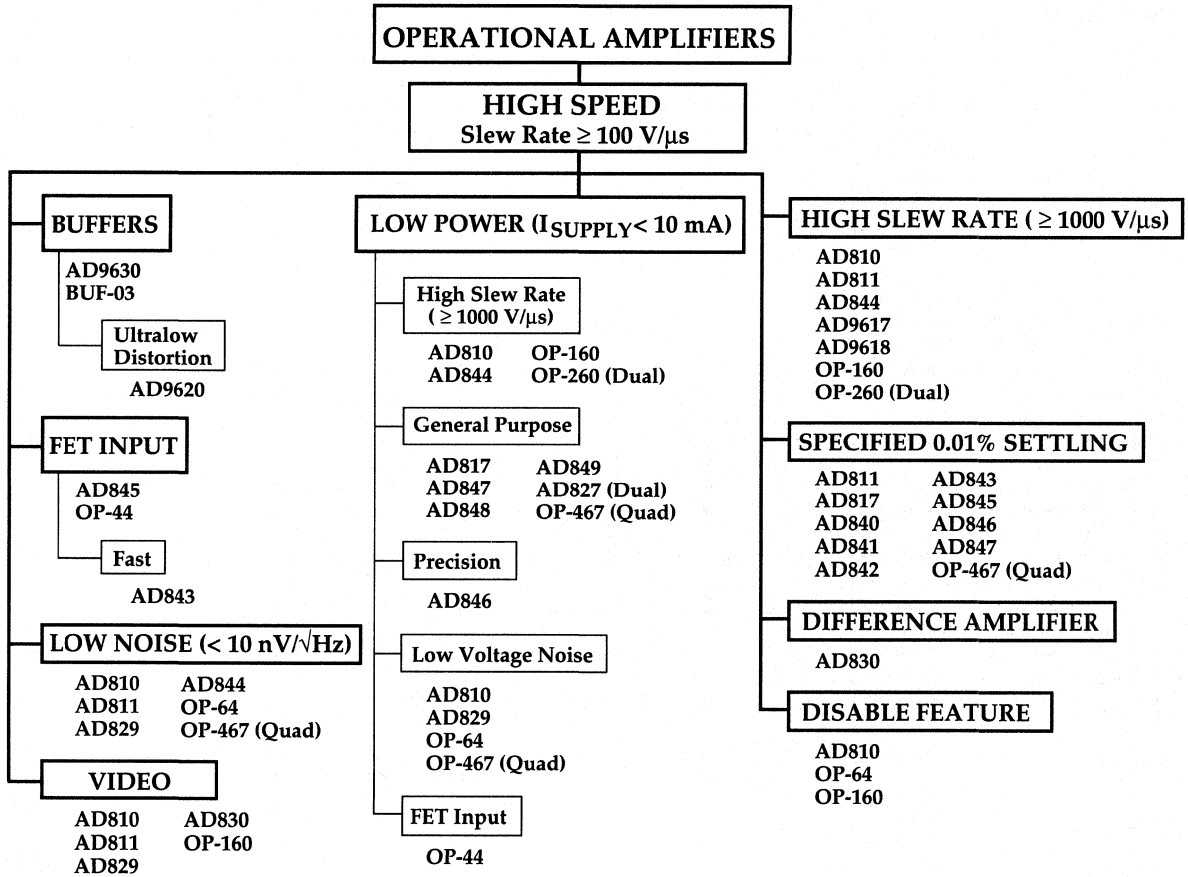
Selection Trees
Operational Amplifiers




OPERATIONAL AMPLIFIERS
LOW VOLTAGE NOISE – V_N
($V_N \leq 10$ nV/√Hz @ 1 kHz)
ULTRALOW V_N
(0.9 nV/√Hz)
AD797
AUDIO AMPLIFIERS
AD797
OP-275
SSM-2015
SSM-2016
SSM-2017
SSM-2134
SSM-2139
FAST
(Slew Rate ≥ 45 V/µs)
OP-61
OP-467 (Quad)
Faster
(Slew Rate ≥ 230 V/µs)
AD829
AD840
AD844
AD846
AD848
AD849
AD5539
Ultrafast
(Slew Rate ≥ 1000 V/µs)
AD810
AD811
AD844
AD9610
AD9617
AD9618
PRECISION
AD797
AD OP-27
AD OP-37
OP-27
OP-37
OP-227 (Dual)
OP-270 (Dual)
OP-271 (Dual)
OP-275 (Dual)
OP-467 (Quad)
OP-470 (Quad)
OP-471 (Quad)
High Output Current
AD797
OP-50
FET INPUT
AD645
AD743
AD795
AD796 (Dual)
Fast
AD745

Selection Trees
Operational Amplifiers




OPERATIONAL AMPLIFIERS
HIGH SPEED
Slew Rate ≥ 100 V/μs
BUFFERS
AD9630
BUF-03
Ultralow Distortion
AD9620
FET INPUT
AD845
OP-44
Fast
AD843
LOW NOISE (< 10 nV/√Hz)
AD810 AD844
AD811 OP-64
AD829 OP-467 (Quad)
VIDEO
AD810 AD830
AD811 OP-160
AD829
LOW POWER (ISUPPLY< 10 mA)
High Slew Rate (≥ 1000 V/μs)
AD810 OP-160
AD844 OP-260 (Dual)
General Purpose
AD817 AD849
AD847 AD827 (Dual)
AD848 OP-467 (Quad)
Precision
AD846
Low Voltage Noise
AD810
AD829
OP-64
OP-467 (Quad)
FET Input
OP-44
HIGH SLEW RATE (≥ 1000 V/μs)
AD810
AD811
AD844
AD9617
AD9618
OP-160
OP-260 (Dual)
SPECIFIED 0.01% SETTLING
AD811 AD843
AD817 AD845
AD840 AD846
AD841 AD847
AD842 OP-467 (Quad)
DIFFERENCE AMPLIFIER
AD830
DISABLE FEATURE
AD810
OP-64
OP-160

Selection Guides
Operational Amplifiers

High Speed Amplifiers

Model	SR V/μs typ	GBW MHz typ	Settling Time ns to % typ	A_{CL} min V/V	V_{OS} mV typ	I_{OUT} mA min	Supply Current mA typ	Package Options[1]	Temp Range[2]	Page[3]	Comments
AD9610	3500	100	18–0.1	1	0.3	50	21	7	I, M	2-431	Wide Bandwidth, Fast Settling
***AD811**	**2500**	**1000**	**65–0.01**	**1**	**0.5**	**100 typ**	**16.5**	**2, 3, 4, 6**	**I, M**	**2-281**	**High Speed Video Amp, 0.12%/0.01° Differential Gain/Phase Error, 0.1 dB Flatness at 35 MHz**
AD844	**2000**	**900**	**100–0.1**	**1**	**0.05**	**20**	**6.5**	**2, 3, 6**	**I, M**	**2-363**	**Constant 10 ns Rise Time for Any Pulse Input, Current Feedback**
AD9618	1800	8000	10–0.1	−1	0.2	60	31	2, 3, 6, 12	C, I, M	2-447	Low Distortion, Wideband, IMD ≤ −70 dBc at 20 MHz
AD9617	1600	570	10–0.1	1	0.4	60	34	2, 3, 6, 12	C, I, M	2-439	Low Distortion, Wide Bandwidth, IMD ≤ −70 dBc at 20 MHz
OP-160	**1300**	**90**	**75–0.1**	**1**	**2**	**35**	**6.5**	**2, 3, 6**	**I, M**	**2-765**	**High Speed, Current Feedback**
***AD810**	**1000**	**500**	**50–0.1**	**1**	**0.5**	**65**	**8/2.5**	**2, 3, 6**	**I, M**	**2-277**	**Video Amp with Disable Feature**
OP-260	**1000**	**90**	**250–0.1**	**1**	**1**	**20**	**9**	**2, 3, 4, 6, 7**	**I, M**	**2-873**	**Dual Current Feedback**
AD5539	**600**	**1400**	**12–1**	**5**	**2**	**15**	**14**	**2, 3**	**C, M**	**2-415**	**Improved Replacement for SE/NE5539**
***AD830**	**530**	**60**	**25–0.1**	**1**	**1**	**30**	**13.6**	**2, 3, 6**	**C, I, M**	**2-321**	**Video Difference Amplifier**
AD846	**450**	**450**	**110–0.01**	**1**	**0.025**	**20 typ**	**5**	**2, 3**	**I, M**	**2-383**	**High Speed, Precision, Current Feedback**
AD840	**400**	**400**	**100–0.01**	**10**	**0.1**	**50**	**10.5**	**2, 3, 4**	**C, M**	**2-327**	**Wide Bandwidth Precision, Fast Settling, $A_{VCL} \geq 10$**
AD842	**375**	**80**	**100–0.01**	**2**	**0.3**	**100**	**13**	**2, 3, 4, 7**	**C, M**	**2-343**	**Fast Settling, High Current Output, Cable Driver, $A_{VCL} \geq 2$**
AD380	330	40	250–0.01	20	2.0	50	12	7	C, M	2-31	Wide Band, Fast Settling, FET Input Op Amp
***AD817**	**300**	**50**	**65–0.1**	**1**	**0.5**	**30**	**6.0**	**2, 3, 6**	**I**	**2-295**	**Low Power, General Purpose**
AD849	**300**	**725**	**80–0.1**	**25**	**0.3**	**20 typ**	**5.1**	**2, 3, 6**	**C, I, M**	**2-407**	**High Speed, Low Power Preamp, Drives Capacitive Loads**
AD848	**300**	**175**	**100–0.1**	**5**	**0.2**	**20 typ**	**5.1**	**2, 3, 6**	**C, I, M**	**2-407**	**High Speed, Low Power, Drives Capacitive Loads**
AD827	**300**	**50**	**120–0.1**	**1**	**0.5**	**20 typ**	**10.5**	**2, 3, 6**	**C, I, M**	**2-301**	**Dual AD847**
AD847	**300**	**50**	**120–0.01**	**1**	**0.5**	**20 typ**	**5.3**	**2, 3, 6**	**C, I, M**	**2-395**	**High Speed, Low Power, Drives Capacitive Loads**
AD841	**300**	**40[4]**	**110–0.01**	**1**	**0.5**	**50**	**11**	**2, 3, 4, 7**	**C, M**	**2-335**	**High Speed, Precision, Drives Capacitive Loads**
AD843	**250**	**34[4]**	**135–0.01**	**1**	**0.5**	**50**	**12**	**2, 3, 4, 6, 7**	**C, I, M**	**2-351**	**FET Input, Fast Settling, High Speed**
AD829	**230**	**750**	**65–0.1**	**1**	**0.2**	**20 typ**	**5.3**	**2, 3, 6**	**C, I, M**	**2-309**	**High Speed, Low Noise, Video Amp**
OP-61	**200**	**45**	**300–0.01**	**10**	**0.1–0.2**	**22**	**6.1**	**2, 3, 4, 6**	**I, M**	**2-683**	**Wide Bandwidth, Ultralow Noise**
***OP-467**	**170**	**30**	**170–0.01**	**1**	**0.5**	**10**	**8**	**2, 3, 5, 6**	**I, M**	**2-999**	**Quad High Speed**
OP-64	**170**	**80**	**100–0.1**	**5**	**0.4–1.2**	**50**	**6.2**	**2, 3, 4, 6, 7**	**I, M**	**2-701**	**Wide Bandwidth, High Output Current**
AD509	120	20	200–0.1	1	4	—	4	7	C, M	2-41	General Purpose
AD845	**100**	**16[4]**	**350–0.01**	**1**	**0.1**	**25 typ**	**10**	**2, 3, 6**	**C, I, M**	**2-375**	**FET Input, Fast Settling, High Speed**

Model	SR V/μs typ	GBW MHz typ	Settling Time ns to % typ	A_{CL} min V/V	V_{OS} mV typ	I_{OUT} mA min	Supply Current mA typ	Package Options[1]	Temp Range[2]	Page[3]	Comments
AD744	75	13	500–0.01	2	0.1	—	3.5	2, 3, 6, 7	C, I, M	2-229	**FET Input, Fast Settling, High Speed, Custom Compensation**
AD746	75	13	500–0.01	2	0.25	—	7	2, 3, 6	C, I, M	2-253	**Dual AD744**
OP-17	60	30	600–0.1	1	0.2–0.5	5.5	4.6	2, 3, 6, 7	C, I, M	2-571	Precision, Low Power
OP-42	58	10	800–0.01	1	0.3–1.5	20	5.1	2, 3, 4, 6, 7	I, M	2-657	**Precision, Fast Settling**
SSM-2131	50	10	900–0.01	1	1.5	20	5.1	2, 6	I	AV	Ultralow Distortion, Low Cost
PM-157A	45	20	4000–0.01	1	1	5	5	3, 7	C, M	D	Improved Industry Standard
AD507	35	100	900–0.1	≥10	1.5	22	3	7	C, M	2-37	General Purpose
SSM-2139	30	11	—	3	0.02	20	4	2, 6	I	AV	Dual, Low Noise
OP-16	25	8	900–0.1	1	0.2–0.5	5.5	4.6	2, 3, 6, 7	C, I, M	2-571	Precision, Low Power
***OP-275**	22	9	—	1	0.4	30	4	2, 6	I	2-919	**Dual Audio Amp**
OP-249	22	4.7	900–0.01	1	0.2–0.4	20	5.6	2, 3, 4, 6, 7	I, M	2-855	**Dual Precision, Low Power, Low Distortion**
AD711	20	4	1000–0.01	1	0.3	25 typ	2.5	2, 3, 6, 7	C, I, M	2-177	**Precision BiFET**
AD712	20	4	1000–0.01	1	0.3	25 typ	5	2, 3, 6, 7	C, I, M	2-189	**Dual AD711**
AD713	20	4	1000–0.01	1	0.3	25 typ	10	2, 3, 6	C, I, M	2-201	**Quad AD711**
***AD797**	18	100	—	1	0.025	30	7.5	2, 3, 6	I, M	2-271	**Ultralow Noise, Low Distortion**
OP-215	18	5.7	900–0.1	1	0.2–2	5.5	6	2, 3, 4, 6, 7	C, I, M	2-819	**Dual Precision**
OP-01	18	2.5	700–0.1	1	0.3–2	6	1.6	2, 3, 7	C, M	2-497	Inverting, High Speed
OP-15	13	6	1200–0.1	1	0.2–0.5	5.5	2.7	2, 3, 6, 7	C, I, M	2-571	**Precision, Low Power**
***AD745**	12.5	20	5000–0.01	5	0.1–0.25	20	8	2, 3, 6	C, I, M	2-241	**Low Noise, High Speed, BiFET Op Amp**
PM-156A	12	4.5	4000–0.01	1	1	5	5	3, 4, 7	C, M	2-1065	Improved Industry Standard
***OP-282**	9.0	4	1500–0.01	1	1	10	0.5	2, 3, 6	I	2-927	**Dual High Speed, Low Power**
***OP-482**	9.0	4	1500–0.01	1	2	10	1.0	2, 3, 5, 6	I	2-927	**Quad High Speed, Low Power**
OP-50	3.0	25	—	≥5	0.01	95	2.6	2, 3	I, M	2-671	High Output Current

[1]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack, 11 = Single-in-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92; 17 = Plastic Pin Grid Array.

[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.

[3]AV = *Audio/Video Reference Manual*; D = data sheet available.

[4]−3 dB BW

Boldface Type: Product recommended for new design.

*New product.

Selection Guides
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Precision Amplifiers

Model	V_{OS} μV max	V_{OS} TC μV/°C max	Noise μV p-p 0.1–10 Hz typ	GBW MHz typ	Slew Rate V/μs typ	I_B nA max	CMRR dB f = 1 kHz typ	Package Options[1]	Temp Range[2]	Page	Comments
OP-177	**10–60**	**0.1–1.2**	**0.35**	**0.6**	**0.3**	**1.5–2.8**	**110**	**2, 3, 6**	**I, M**	**2-791**	**Highest Precision**
AD707	**15–90**	**0.1–1.0**	**0.23**	**0.9**	**0.3**	**1.0–2.5**	**100**	**2, 3, 6, 7**	**C, I, M**	**2-161**	**High Precision**
OP-77	**25–100**	**0.3–1.2**	**0.35**	**0.6**	**0.3**	**2–2.8**	**105**	**2, 3, 4, 6, 7**	**C, I, M**	**2-715**	**Next Generation OP-07**
OP-50	25–100	0.3–1	0.12	25	3	5–10	85	3	I, M	2-671	Low Noise, High Output Current $A_{VCL} \geq 5$
AD705	**25–90**	**0.6–1.2**	**0.5**	**0.8**	**0.15**	**0.1–0.15**	**110**	**2, 3, 6**	**C, I, M**	**2-145**	**Low I_B Precision Bipolar**
OP-97	**25–75**	**0.6–2**	**0.5**	**0.9**	**0.2**	**0.1–0.15**	**100**	**2, 3, 4, 6, 7**	**I, M**	**2-751**	**Low Power OP-07**
OP-27	**25–100**	**0.6–1.8**	**0.08**	**8**	**2.8**	**40–80**	**125**	**2, 3, 4, 6, 7**	**C, I, M**	**2-609**	**Low Noise, Precision**
AD OP-27	**25–100**	**0.6–1.8**	**0.08**	**8**	**2.8**	**40–80**	**123**	**2, 3, 7**	**C, I, M**	**2-473**	**Ultralow Noise**
OP-37	**25–100**	**0.6–1.8**	**0.08**	**63**	**17**	**40–80**	**125**	**2, 3, 4, 6, 7**	**C, I, M**	**2-633**	**Fast, Low Noise, Precision $A_{VCL} \geq 5$**
AD OP-37	**25–100**	**0.6–1.8**	**0.08**	**63 (GBP)**	**17**	**40–80**	**123**	**2, 3, 7**	**I, M**	**2-481**	**Combines Precision and Speed**
AD OP-07	**25–150**	**0.6–2.5**	**0.35**	**0.6**	**0.17**	**2–12**	**95**	**2, 3, 6, 7**	**I, M**	**2-467**	**Improved Industry Standard**
OP-07	**25–150**	**0.6–2.5**	**0.35**	**0.6**	**0.3**	**2–12**	**98**	**2, 3, 4, 6, 7**	**C, I, M**	**2-537**	**Low Offset Voltage**
AD846	**25–200**	**0.8–5.0**	**—**	**75–450**	**450**	**250**	**—**	**2, 3**	**I, M**	**2-383**	**High Precision, High Speed**
AD708	**30–100**	**0.3–1.0**	**0.23**	**0.9**	**0.3**	**1.0–2.5**	**100**	**2, 3, 7**	**C, I, M**	**2-169**	**Dual AD707**
PM-1012	35–50	1.5	0.5	0.5	0.2	0.1–0.15	100	2, 3, 6, 7	C, I, M	2-1071	Low Power, Low I_B
***AD797**	**40–100**	**0.8–1.5**	**0.05**	**100**	**18**	**50–1000 (typ)**	**130**	**2, 3, 6**	**I, M**	**2-271**	**Ultralow Noise, Low Distortion Amp**
AD706	**50–100**	**0.5–1.0**	**0.5**	**0.8**	**0.15**	**0.11–0.20**	**110**	**2, 3, 6**	**C, I**	**2-153**	**Dual AD705**
AD517	50–100	1.3–3	2	0.25	0.1	0.25–2	94	7	C, M	2-51	General Purpose, Low Offset
***OP-497**	**50–150**	**0.5–1.5**	**0.3**	**0.5**	**0.15**	**0.1–0.2**	**130**	**2, 3, 4, 6**	**I, M**	**2-1049**	**Quad Precision, Low I_B**
***OP-297**	**50–200**	**0.6–2**	**0.3**	**0.5**	**0.15**	**0.1–0.2**	**105**	**2, 3, 6**	**I, M**	**2-959**	**Dual Precision, Low Power, Low I_B**
AD704	**75–150**	**1.0–1.5**	**0.5**	**0.8**	**0.1**	**0.15–0.27**	**110**	**2, 3, 6**	**C, I, M**	**2-137**	**Quad AD705**
OP-200	**75–200**	**0.5–2**	**0.5**	**0.5**	**0.15**	**2–5**	**110**	**2, 3, 4, 6**	**I, M**	**2-803**	**Dual Monolithic, Precision**
OP-270	**75–250**	**1–3**	**0.08**	**5**	**2.4**	**20–60**	**115**	**2, 3, 4, 6**	**I, M**	**2-893**	**Dual Monolithic, Low Power**
OP-227	80–180	1–1.8	0.08	8	2.8	40–80	125	3	I, M	2-843	Dual Matched, Low Noise
OP-207	100–200	1.3–1.8	0.35	0.6	0.2	3–7	98	3	C, M	2-813	Dual Matched, Precision
OP-21	100–500	1–5	—	0.6	0.25	100–150	60	2, 3, 6, 7	I, M	2-591	Low Power, Single Supply
AD844	**150–300**	**5**	**—**	**900**	**2000**	**250**	**—**	**2, 3, 6**	**I, M**	**2-363**	**Precision, High Speed**
OP-400	**150–300**	**1.2–2.5**	**0.5**	**0.5**	**0.15**	**3–7**	**110**	**2, 3, 4, 6**	**C, I, M**	**2-975**	**Quad, Monolithic, Precision**
OP-90	150–450	2–5	3	—	—	15–25	80	2, 3, 4, 6	I, M	2-739	Micropower, Low Voltage, Single Supply
OP-221	**150–500**	**1.5–3**	**—**	**0.6**	**0.3**	**80–120**	**60**	**2, 3, 6, 7**	**C, I, M**	**2-835**	**Dual Low Power, Single Supply**
OP-220	**150–750**	**1.5–3**	**—**	**0.2**	**0.05**	**20–30**	**30**	**2, 3, 6, 7**	**C, I, M**	**2-827**	**Dual Micropower, Single Supply**

Precision Amplifiers

Model	V_{OS} μV max	V_{OS} TC μV/°C max	Noise μV p-p 0.1–10 Hz typ	GBW MHz typ	Slew Rate V/μs typ	I_B nA max	CMRR dB f = 1 kHz typ	Package Options[1]	Temp Range[2]	Page	Comments
OP-12	150–1400	0.5–1.5	0.9	0.8	0.12	2–6.5	—	3, 7	C, M	2-567	Internally Compensated
OP-05	150–1600	0.9–4.5	0.38	0.8	0.3	2.9	—	2, 3, 7	C, M	2-519	Instrumentation Amplifier
OP-271	**200–400**	**2–5**	**—**	**5**	**8.5**	**20–60**	**125**	**2, 3, 4, 6**	**I, M**	**2-909**	**Dual, Fast, Low Noise**
OP-290	**200–500**	**3–5**	**3**	**0.02**	**—**	**15–25**	**100**	**2, 3, 4, 6**	**I, M**	**2-943**	**Dual Micropower, Low Voltage Single Supply**
***OP-467**	**200–1000**	**3.5**	**6**	**30**	**170**	**—**	**80**	**2, 3, 5, 6**	**C, I, M**	**2-999**	**Quad High Speed**
OP-06	200–1300	0.8–1.4	—	—	—	70–110	—	3, 7	C, M	2-529	Instrumentation Amplifier
***AD795**	**250–500**	1–10	1	2	1	0.001–0.004	110	2, 6, 7	C, I, M	2-261	Low Power, Low Noise FET
AD547	250–1000	1–5	2	1	3	0.025–0.05	60	7	C, M	2-57	Low Drift BiFET
AD647	250–1000	2.5–10	4	1	3	0.035	60	4, 7	C, M	2-121	Dual AD547
OP-20	250–1000	1.5–7	—	0.1	0.05	25–40	30	2, 3, 6, 7	C, I, M	2-585	Micropower, Single Supply
***AD820**	**250–1000**	**5–10**	**2**	**2**	**3.75**	**0.02–0.03**	**100**	**2, 3, 6**	**C, I, M**	**2-299**	**Single Supply, Rail to Rail, FET Input**
***AD822**	**250–1000**	**5–10**	**2**	**2**	**3.75**	**0.02–0.03**	**100**	**2, 3, 6**	**C, I, M**	**2-299**	**FET Dual AD820**
AD711	**250–2000**	**3–20**	**2**	**4**	**20**	**0.025–0.050**	**94**	**—**	**C, I, M**	**2-177**	**Precision, High Speed**
AD548	**250–2000**	**2–20**	**2**	**1**	**1.8**	**0.01–0.02**	**83**	**2, 3, 6, 7**	**C, I, M**	**2-81**	**Low Power BiFET**
OP-41	250–2000	5–10	—	0.5	1.3	0.005–0.02	100	2, 6, 7	C, I, M	2-645	Low I_B
***AD796**	**300–500**	**3–12**	**1**	**2**	**1**	**0.002–0.004**	**110**	**2, 6, 7**	**C, I, M**	**2-267**	**Dual AD795**
OP-22	300–1000	1.5–3	—	0.25	0.08	5–10	60	2, 3, 6, 7	C, I, M	2-597	Micropower, Programmable
OP-32	300–1000	1.5–3	—	4.5	1.5	5–10	90	2, 3	C, I, M	2-621	Micropower, Fast, Programmable
AD648	**300–2000**	**3–20**	**2**	**1**	**1.8**	**0.01–0.02**	**83**	**2, 3, 6, 7**	**C, I, M**	**2-127**	**Dual AD548**
AD712	**300–3000**	**5–20**	**2**	**4**	**20**	**0.05–0.075**	**94**	**—**	**C, I, M**	**2-189**	**Dual AD711**
OP-470	**400–1000**	**2–4**	**0.08**	**6**	**2**	**25–60**	**110**	**2, 3, 4, 6**	**C, I, M**	**2-1005**	**Quad, Low Noise**
AD713	**500–1500**	**15–20**	**2**	**4**	**20**	**0.075–0.150**	**94**	**—**	**C, I, M**	**2-201**	**Dual AD711**
AD741	500–6000	5–20	—	1	0.5	50–500	100	2, 7	C, M	2-213	General Purpose
OP-471	**800–1800**	**4–7**	**0.25**	**6.5**	**8**	**25–60**	**108**	**2, 3, 4, 6**	**C, I, M**	**2-1021**	**Quad, Fast, Low Noise**

[1]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack, 11 = Single-in-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92; 17 = Plastic Pin Grid Array.
[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.
Boldface Type: Product recommended for new design.
*New product.

Selection Guides
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Single Supply Amplifiers

Model	ISY max mA	V_{OS} max mV	Supply Voltage Range V	GBW typ MHz	SR typ V/µs	Package Options[1]	Temp Range[2]	Page	Comments
OP-22	0.0002–0.4	0.3–1	+3 to +30	0.25	0.08	2, 3, 6, 7	I, M	2-597	Programmable
OP-32	0.0005–2	0.3–1	+3 to +30	4.5	1.5	2, 3	I, M	2-621	Fast, Programmable A_{VCL} = 10
OP-90	0.02	0.15–0.45	+1.6 to +36	0.02	—	2, 3, 4, 6	I, M	2-739	Micropower, Low Voltage
OP-290	**0.04**	**0.2–0.5**	**+1.6 to +36**	**0.02**	**—**	**2, 3, 4, 6**	**I, M**	**2-943**	**Dual Micropower, Low Voltage**
OP-20	0.08	0.25–1	+5 to +30	0.1	0.05	2, 3, 4, 6	I, M	2-585	Micropower, Low Cost
OP-490	**0.08**	**0.5–1**	**+1.6 to +36**	**0.02**	**—**	**2, 3, 4, 6**	**I, M**	**2-1037**	**Quad Micropower, Low Voltage**
OP-220	**0.17**	**0.15–0.75**	**+5 to +30**	**0.2**	**0.05**	**2, 3, 6, 7**	**I, M**	**2-827**	**Dual Micropower, Low Cost**
***OP-295**	**0.200**	**0.25–1.0**	**+2.4 to +36**	**0.08**	**0.02**	**2, 3, 6**	**I, M**	**2-953**	**Rail to Rail Dual**
OP-80	**0.325**	**1.5**	**+5 to +16**	**0.3**	**0.4**	**2, 6, 7**	**I, M**	**2-727**	**Low I_B, CMOS**
OP-420	0.36	2.5–6	+5 to +30	0.15	0.05	2, 3, 4, 6	I, M	2-987	Quad Micropower, Low Cost
OP-21	0.3–0.4	0.1–0.5	+5 to +30	0.6	0.25	2, 3, 6, 7	I, M	2-591	Low Cost, Low Power
***OP-495**	**0.4**	**0.2–0.5**	**+3 to +36**	**0.08**	**0.02**	**2, 3, 6**	**I, M**	**2-953**	**Quad Rail to Rail**
***AD820**	**0.660**	**0.25–1**	**+4 to +36**	**2**	**3.75**	**2, 3, 6**	**C, I, M**	**2-299**	**Fast FET Input Rail to Rail**
OP-221	**0.8**	**0.15–0.5**	**+5 to +30**	**0.6**	**0.3**	**2, 3, 6, 7**	**I, M**	**2-835**	**Dual Low Cost, Low Power**
***AD822**	**1.3**	**0.25–1**	**+4 to +36**	**2**	**3.75**	**2, 3, 6**	**C, I, M**	**2-299**	**Dual AD820**
OP-421	1.8	2.5–6	+5 to +30	1.9	0.5	2, 3, 6	I, M	2-993	**Quad Low Cost, Low Power**
***OP-113/213/413**	**4**	**0.150**	**+5 to +30**	**3**	**1**	**2, 3, 4, 5, 6**	**I, M**	**2-761**	**Low Noise, Low Drift Op Amp**

Low Voltage Noise Amplifiers

Model	Voltage Noise e_n typ 1 kHz $nV/\sqrt{Hz}$	Voltage Noise e_n typ 10 kHz $nV/\sqrt{Hz}$	Current Noise $I_n \pm I_{n-}$ typ 1 kHz $pA/\sqrt{Hz}$	I_B typ nA	V_{OS} mV typ	GBW MHz typ	SR V/µs typ	Settling Time ns to % typ	A_{CL} min V/V	Package Options[1]	Temp Range[2]	Page[3]	Comments
SSM-2016	0.8	—	—	900	0.5	1	10	—	1	2	C	4-185	Ultralow Noise Differential Audio Preamplifier
***AD797**	**0.9**	**0.9**	**2**	**500**	**0.025**	**100**	**18**	**—**	**1**	**2, 3, 6**	**I, M**	**2-271**	**Ultralow Noise, Low Distortion**
SSM-2017	0.95	—	—	600	0.1	4	17	—	1	2, 3, 6	I	4-193	Self-Contained Audio Preamplifier
AD9610	1.6	0.7	32/32	5000	0.3	100	3500	1–0.1	1	2	I, M	2-431	Wide Bandwidth, Fast Settling
AD829	**1.7**	**—**	**1.5**	**3300**	**0.2**	**750**	**230**	**65–0.1**	**1**	**2, 3, 6**	**C, I, M**	**2-309**	**High Speed, Low Noise, Video Amp**
***AD811**	**1.9**	**1.9**	**1.5/20**	**2000**	**0.5**	**1000**	**2500**	**65–0.01**	**1**	**2, 3, 4, 6**	**I, M**	**2-281**	**High Performance Video Op Amp**
AD9617	2.0	1.3	32/32	12000	0.5	570	1400	10–0.1	±1	2, 3, 6, 12	C, I, M	2-439	Low Distortion, Wide Bandwidth
AD9618	2.0	1.3	32/32	10000	0.5	8000	1800	9–0.1	+5, −1	2, 3, 6, 12	C, I, M	2-447	Low Distortion, Wide Bandwidth
AD844	**2**	**—**	**12/10**	**200**	**0.05**	**900**	**2000**	**100–0.1**	**1**	**2, 3, 6**	**I, M**	**2-363**	**Current Feedback Amplifier**
AD846	**2**	**—**	**6/20**	**100**	**0.025**	**450**	**450**	**110–0.01**	**1**	**2, 3**	**I, M**	**2-383**	**Current Feedback, Precision**
***AD810**	**2.5**	**2.5**	**1.5/20**	**2000**	**0.5**	**500**	**1000**	**50–0.1**	**1**	**2, 3, 6**	**I, M**	**2-277**	**Video Op Amp with Disable**
AD849	**3**	**—**	**—**	**3300**	**0.3**	**725**	**300**	**80–0.1**	**25**	**2, 3, 6**	**C, I, M**	**2-407**	**High Speed, Low Power**
OP-27	**3.0**	**3.5**	**0.4**	**10**	**0.01**	**8**	**2.8**	**—**	**1**	**2, 3, 4, 6, 7**	**C, I, M**	**2-609**	**Low Noise, Precision**
AD OP-27	**3**	**3.5**	**0.4**	**10**	**0.01**	**8**	**2.8**	**—**	**1**	**2, 3, 7**	**I, M**	**2-473**	**Low Noise, Precision**
OP-227	3	3.5	0.4	10	0.02	8	2.8	—	1	3	C, I, M	2-843	Dual Matched Precision
OP-37	**3**	**3.5**	**0.4**	**10**	**0.01**	**63**	**17**	**—**	**1**	**2, 3, 4, 6, 7**	**C, I, M**	**2-633**	**Fast, Precision $A_{VCL} \geq 5$**
AD OP-37	**3**	**3.5**	**0.4**	**10**	**0.01**	**63**	**17**	**—**	**5**	**2, 3, 7**	**I, M**	**2-481**	**Low Noise, Precision**
***AD745**	**3.2**	**2.9**	**0.007**	**0.150**	**0.1**	**20**	**12.5**	**5000–0.01**	**5**	**2, 3, 6**	**C, I, M**	**2-241**	**Ultralow Noise, High Speed, BiFET Op Amp**
AD743	**3.2**	**2.9**	**0.007**	**0.15**	**0.1**	**4.5**	**2.8**	**—**	**1**	**2, 3, 6**	**C, I, M**	**2-217**	**Ultralow Noise FET Input**
OP-270	**3.2**	**3.6**	**0.6**	**5**	**0.01**	**5**	**2.4**	**—**	**1**	**2, 3, 4, 6**	**I, M**	**2-893**	**Dual Monolithic**
SSM-2139	3.2	3.2	0.6	5	0.02	30	11	—	3	2, 6	I	AV	Dual Audio
SSM-2134	3.5	3.5	0.6	350	0.3	10	13	—	3	2	I	AV	Improved Replacement for "5534A"
OP-470	**3.2**	**3.8**	**0.4**	**6**	**0.1**	**6**	**2**	**—**	**1**	**2, 3, 4, 6**	**I, M**	**2-1005**	**Quad Monolithic, Low Noise**
AD5539	**4**	**—**	**—**	**6000**	**2**	**1400**	**600**	**12–1**	**5**	**2, 3**	**C, M**	**2-415**	**Improved Replacement for SE/NE5539**
AD840	**4**	**—**	**—**	**3500**	**0.1**	**400**	**400**	**100–0.01**	**10**	**2, 3, 4**	**C, M**	**2-327**	**Wide Bandwidth, Precision**
OP-50	4.5	5.5	0.23	1	0.01	25	3	—	5	3	I, M	2-671	High Output Current
***OP-176**	**6**	**—**	**1.5**	**100**	**0.5**	**8**	**22**	**—**	**1**	**2, 6**	**I**	**2-789**	**Bipolar/JFET Audio Preamplifer**
***OP-467**	**6**	**5.5**	**—**	**100**	**1**	**30**	**170**	**170**	**1**	**2, 3, 5, 6**	**C, I, M**	**2-919**	**Quad, High Speed**
***OP-275**	**6**	**6**	**—**	**—**	**1**	**9**	**22**	**—**	**1**	**2, 6**	**I, M**	**2-999**	**Dual Audio Amp**
AD848	**5**	**—**	**—**	**3300**	**0.2**	**175**	**300**	**100–0.1**	**5**	**2, 3, 6**	**C, I, M**	**2-407**	**High Speed, Low Power**
OP-471	**6.5**	**9**	**0.4**	**7**	**0.25**	**6.5**	**8**	**—**	**1**	**2, 3, 4, 6**	**I, M**	**2-1021**	**Quad Monolithic, Fast**
***AD795**	**7**	**8**	**0.0006**	**0.001**	**0.05**	**2**	**1**	**8000–0.01**	**1**	**2, 6, 7**	**C, I, M**	**2-261**	**Low Power, Low Noise Photo Diode Preamp**
***AD796**	**7**	**8**	**0.0007**	**0.001**	**0.05**	**2**	**1**	**1200–0.01**	**1**	**2, 6, 7**	**C, I, M**	**2-267**	**Dual AD795**
OP-271	**7.6**	**16**	**0.6**	**4**	**0.075**	**5**	**8.5**	**—**	**1**	**2, 3, 4, 6**	**I, M**	**2-909**	**Dual Monolithic, Fast**
OP-61	**3.4**	**16**	**1.7**	**130**	**0.1–0.2**	**200**	**45**	**300–0.01**	**10**	**2, 3, 4, 6**	**I, M**	**2-683**	**Wide Bandwidth**
AD645	**9**	**8**	**0.0006**	**0.0007**	**0.1**	**2**	**2**	**—**	**1**	**2, 7**	**C, I, M**	**2-113**	**FET Input, Low I_B**

[1]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack, 11 = Single-in-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92; 17 = Plastic Pin Grid Array.

[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.

[3]AV = *Audio/Video Reference Manual.*

Boldface Type: Product recommended for new design.

*New product.

Selection Guides
Operational Amplifiers

Low Power/Micropower Amplifiers

Model	ISY max mA	V_{OS} max mV	I_B max nA	GBW typ MHz	SR typ V/μs	Package Option[1]	Temp Range[2]	Page	Comments
OP-22	0.0002–0.4	0.3–1	5–10	0.25	0.08	2, 3, 6, 7	I, M	2-597	Programmable, Single Supply
OP-32	0.0005–2	0.3–1	5–10	4.5	1.5	2, 3	I, M	2-621	Fast, Programmable $A_{VCL} \geq 10$, Single Supply
OP-90	0.02	0.15–0.45	15–25	0.02	—	2, 3, 4, 6	I, M	2-739	Micropower, Low Voltage Single Supply
OP-290	**0.04**	**0.2–0.5**	**15–25**	**0.02**	**—**	**2, 3, 4, 6**	**I, M**	**2-943**	**Dual, Micropower, Low Voltage, Single Supply**
OP-20	0.08	0.25–1	25–40	0.1	0.05	2, 3, 4, 6	I, M	2-585	Micropower, Single Supply, Low Cost
OP-490	**0.08**	**0.5–1**	**15–25**	**0.02**	**—**	**2, 3, 4, 6**	**I, M**	**2-1037**	**Quad, Micropower, Low Voltage, Single Supply**
OP-220	**0.17**	**0.15–0.75**	**20–30**	**0.2**	**0.05**	**2, 3, 6, 7**	**I, M**	**2-827**	**Dual, Low Cost, Micropower, Single Supply**
AD548	**0.2**	**0.25–0.2**	**0.01–0.02**	**1.0**	**1.8**	**2, 3, 7**	**C, I, M**	**2-81**	**Precision Low Power BiFET Op Amp**
***OP-295**	**0.3**	**0.2–0.5**	**15**	**0.085**	**0.04**	**2, 6**	**I, M**	**2-953**	**Dual Rail to Rail**
OP-80	**0.325**	**1.5**	**0.00025–0.001**	**0.3**	**0.4**	**2, 6, 7**	**I, M**	**2-727**	**Low I_B, CMOS**
OP-420	0.36	2.5–6	20–40	0.15	0.05	2, 3, 4, 6	I, M	2-987	Quad, Low Cost, Micropower, Single Supply
OP-21	0.3–0.4	0.1–0.5	100–150	0.6	0.25	2, 3, 6, 7	I, M	2-591	Low Cost, Low Power, Single Supply
***OP-282**	**0.5**	**2.0**	**0.1**	**4**	**9**	**2, 3, 6**	**I**	**2-927**	**Dual, High Speed, Low Power**
AD648	**0.4**	**0.4–2.0**	**0.005–.01**	**1.0**	**1.8**	**2, 3, 7**	**C, I, M**	**2-127**	**Dual, Precision Low Power BiFET Op Amp**
PM-108/208/308	0.4	0.5–10	2–10	—	—	2, 3, 4, 6, 7	C, I, M	2-1061	Low Input Bias Current
OP-97	**0.6**	**0.025–0.075**	**0.1–0.15**	**0.9**	**0.2**	**2, 3, 4, 6, 7**	**I, M**	**2-751**	**Precision, Low I_B**
AD705	**0.6**	**0.025–0.09**	**0.1–0.15**	**0.8**	**0.15**	**2, 3, 6**	**C, I, M**	**2-145**	**Picoampere Input Current Bipolar Op Amp**
PM-1012	0.6	0.035–0.05	0.1–0.15	0.5	0.2	2, 3, 6, 7	C, I, M	2-1071	Precision, Low I_B
***AD820**	**0.66**	**0.25–1**	**0.02–0.03**	**2**	**3.75**	**2, 3, 6**	**C, I, M**	**2-299**	**Fast, Single Supply, Rail to Rail FET Input**
OP-221	**0.8**	**0.15–0.5**	**80–120**	**0.6**	**0.3**	**2, 3, 6, 7**	**I, M**	**2-835**	**Dual, Low Cost, Low Power, Single Supply**
OP-41	1	0.25–2	0.005–0.02	0.5	1.3	2, 6, 7	I, M	2-645	Low Power, Low I_B
***OP-482**	**1.0**	**3.0**	**0.1**	**4**	**9**	**2, 3, 5, 6**	**I**	**2-927**	**Quad, High Speed, Low Power**
AD706	**1.2**	**0.05–0.1**	**0.11–0.2**	**0.8**	**0.15**	**2, 3, 6**	**C, I, M**	**2-153**	**Dual, Picoampere Input Current Bipolar Op Amp**
***OP-297**	**1.25**	**0.05–0.2**	**0.1–0.2**	**0.5**	**0.15**	**2, 3, 4, 6**	**I, M**	**2-959**	**Dual, Precision, Low I_B**
***AD822**	**1.3**	**0.25–1**	**0.02–0.03**	**2**	**3.75**	**2, 3, 6**	**C, I, M**	**2-299**	**Dual AD820**
OP-200	**1.45**	**0.075–0.2**	**2–5**	**0.5**	**0.15**	**2, 3, 4, 6**	**I, M**	**2-803**	**Dual, Precision**
OP-421	1.8	2.5–6	50–150	1.9	0.5	2, 3, 6	I, M	2-993	Quad, Low Cost, Low Power, Single Supply
AD704	**2.4**	**0.075–0.150**	**0.15–0.17**	**1.0**	**0.15**	**2, 3, 6**	**C, I, M**	**2-137**	**Quad, Picoampere Input Current Bipolar Op Amp**
OP-02	2.4	0.5–5	30–100	1.3	0.5	2, 3, 7	C, M	2-503	Improved 741
OP-400	**2.9**	**0.15–0.3**	**3–7**	**0.5**	**0.15**	**2, 3, 4, 6**	**C, I, M**	**2-975**	**Quad, Precision**

Low Current Noise, Low Input Bias Current Amplifiers

Model	I_B pA max	I_N f=1 kHz FA/$\sqrt{Hz}$	Input Impedance Differential Ω‖pF typ	Input Impedance Common Mode Ω‖pF typ	CMRR dB f=1 kHz typ	V_{OS} mV max	V_{OS} TC µV/°C max	BW MHz typ[3]	Package Options[1]	Temp Range[2]	Page	Comments
AD549	**0.06–0.25**	**0.11**	**10^{13}‖1**	**10^{15}‖0.8**	**62**	**0.25–1**	**5–20**	**1**	**7**	**C, M**	**2-89**	**Monolithic, Lowest I_B**
AD515A	0.075–0.3	—	10^{13}‖1.6	10^{15}‖0.8	62	1–3	15–50	1	7	C	2-45	Lower Cost AD515 Replacement
OP-80	**0.25–1**	**—**	**—**		**90**	**1.5**	**—**	**0.3**	**2, 6, 7**	**I, M**	**2-727**	**Low Cost CMOS**
AD546	**0.5–1**	**0.4**	**10^{13}‖1**	**10^{15}‖0.8**	**62**	**1–2**	**20**	**1**	**2**	**C**	**2-69**	**Precision Low Cost Electrometer**
AD545A	1–2	—	10^{13}‖1.6	10^{15}‖0.8	62	0.25–1	3–25	1	7	C	2-65	Lower Cost AD545 Replacement
***AD795**	**1–4**	**0.6**	**10^{12}‖1**	**10^{14}‖2.2**	**110**	**0.25–0.5**	**1–10**	**2**	**2, 6, 7**	**C, I, M**	**2-261**	**Low Power, Low Noise, Photodiode Preamp**
AD645	**1.5–3**	**0.6**	**10^{13}‖1**	**10^{14}‖3**	**94**	**0.25–0.5**	**1–5**	**2**	**2, 7**	**C, I, M**	**2-113**	**Low Noise, Precision BiFET**
***AD796**	**2.5–4**	**0.7**	**10^{12}‖1**	**10^{14}‖2.2**	**110**	**0.3–0.5**	**3–10**	**2**	**2, 6, 7**	**C, I, M**	**2-267**	**Dual AD795**
OP-41	5–20	—	—		98	0.25–2	5–10	0.5	2, 6, 7	C, I, M	2-645	High Stability JFET
AD548	**10–20**	**1.8**	**10^{12}‖3**	**3×10^{12}‖3**	**84**	**0.25–2**	**2–20**	**1**	**2, 3, 6, 7**	**C, I, M**	**2-81**	**Low Power, Low Cost**
AD648	**10–20**	**1.8**	**10^{12}‖3**	**3^{12}‖3**	**84**	**0.3–2**	**3–20**	**1**	**2, 3, 6, 7**	**C, I, M**	**2-127**	**Dual AD548**
***AD820**	**20–30**	**1.8**	**—**	**—**	**100**	**0.25–1**	**5–10**	**2**	**2, 3, 6**	**C, I, M**	**2-299**	**Single Supply, Fast, Rail to Rail**
***AD822**	**20–30**	**1.8**	**—**	**—**	**100**	**0.25–1**	**5–10**	**2**	**2, 3, 6**	**C, I, M**	**2-299**	**Dual AD820**
AD542	25–50	—	—	—	80	0.5–2	5–20	1	7	C, M	2-57	Precision
AD544	25–50	—	—	—	80	0.5–2	5–20	2	7	C, M	2-57	Precision, Low Distortion
AD547	25–50	—	10^{12}‖6	10^{12}‖3	60	0.25–1	1–5	1	7	C, M	2-57	Low Drift
AD711	**25–50**	**10**	**3×10^{12}‖5.5**	**3×10^{12}‖5.5**	**62**	**0.25–2**	**3–20**	**4**	**2, 3, 6, 7**	**C, I, M**	**2-177**	**Low Cost BiFET, Excellent AC and DC Performance**
AD642	35–75	—	10^{12}‖6	10^{12}‖6	90	0.5–2	—	1	7	C, M	2-101	Dual Precision
AD647	35–75	—	10^{12}‖6	10^{12}‖6	90	0.5–1	2.5–10	1	4, 7	C, M	2-121	Dual AD547
PM-155A	50	10	—		90	2	5	2.5	3, 7	C, M	2-1065	Improved Industry Standard
PM-156A	50	10	—		90	2	5	4.5	3, 7	C, M	2-1065	Improved Industry Standard
PM-157A	50	10	—		90	2	5	20	3, 7	C, M	2-1065	Improved Industry Standard
AD712	**50–75**	**10**	**3^{12}‖5.5**	**3^{12}‖5.5**	**94**	**0.3–3**	**5–20**	**4**	**2, 3, 6, 7**	**C, I, M**	**2-189**	**Dual AD711**
OP-15	**50–200**	**10**	**—**		**90**	**0.5–3**	**5–15**	**6**	**2, 3, 6, 7**	**C, I, M**	**2-571**	**Precision BiFET**
OP-16	50–200	10	—		90	0.5–3	5–15	8	2, 3, 6, 7	C, I, M	2-571	Precision BiFET
OP-17	50–200	10	—		90	0.5–3	5–15	30	2, 3, 6, 7	C, I, M	2-571	Fast, Precision BiFET

[1]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack, 11 = Single-in-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92; 17 = Plastic Pin Grid Array.
[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.
[3]Unity gain small signal bandwidth.
Boldface Type: Product recommended for new design.
*New product.

Selection Guides
Operational Amplifiers

Dual Operational Amplifiers

Model	V_{OS} mV max	V_{OS} TC µV/°C max	I_B nA max	BW MHz typ[1]	Slew Rate V/µs typ	Settling Time to 0.01% µs typ	Package Options[2]	Temp Range[3]	Page[4]	Comments
AD708	**0.03–0.1**	**0.3–1.0**	**1–2.5**	**0.9**	**0.3**		**2, 3, 7**	**C, I, M**	**2-169**	**Highest DC Precision; Excellent Matching Between Amps, Dual AD707**
AD706	**0.05–0.10**	**0.6–1.5**	**0.11–0.200**	**0.8**	**0.15**	**—**	**2, 3, 6**	**C, I**	**2-153**	**Dual AD705, Low I_B Precision Bipolar**
***OP-297**	**0.05–0.2**	**0.6–2**	**0.1–0.2**	**0.5**	**0.15**	**—**	**2, 3, 6**	**I, M**	**2-959**	**Precision, Low Power, Low I_B**
OP-200	**0.075–0.2**	**0.5–2**	**2–5**	**0.5**	**0.15**	**—**	**2, 3, 4, 6**	**I, M**	**2-803**	**Dual Monolithic, Precision**
OP-270	**0.075–0.25**	**1–3**	**20–60**	**5**	**2.4**	**—**	**2, 3, 4, 6**	**I, M**	**2-893**	**Dual Monolithic, Low Noise**
OP-227	0.08–0.18	1–1.8	40–80	8	2.8	—	3	I, M	2-843	Dual Matched, Low Noise
OP-207	0.1–0.2	1.3–1.8	3–7	0.6	0.2	—	3	C, M	2-813	Dual Matched, Precision
OP-221	**0.15–0.5**	**1.5–3**	**80–120**	**0.6**	**0.3**	**—**	**2, 3, 6, 7**	**C, I, M**	**2-835**	**Low Power, Single Supply**
OP-220	**0.15–0.75**	**1.5–3**	**20–30**	**0.2**	**0.05**	**—**	**2, 3, 6, 7**	**C, I, M**	**2-827**	**Micropower, Single Supply**
OP-271	**0.2–0.4**	**2–5**	**20–60**	**5**	**8.5**	**—**	**2, 3, 4, 6**	**I, M**	**2-909**	**Dual Monolithic, Fast, Low Noise**
OP-290	**0.2–0.5**	**3–5**	**15–25**	**0.02**	**—**	**—**	**2, 3, 4, 6**	**I, M**	**2-943**	**Micropower, Low Voltage Single Supply**
***OP-295**	**0.2–0.5**	**<10**	**15**	**0.085**	**0.04**	**—**	**2, 6**	**I, M**	**2-953**	**Rail to Rail**
***OP-285**	**0.25**	**—**	**150**	**8**	**20**	**—**	**2, 3, 6**		**2-939**	**Dual High Performance, Low Power**
AD647	0.25–1	2.5–10	0.035–0.075	1	3	—	4, 7	C, M	2-121	Dual AD547
***AD822**	**0.25–1**	**5–10**	**0.02–0.03**	**2**	**3.75**	**—**	**2, 3, 6**	**C, I, M**	**2-299**	**Single Supply, Rail to Rail, Fast FET Input**
AD746	**0.5–1**	**10–20**	**0.15**	**13**	**75**	**0.5**	**2, 3, 6**	**C, I, M**	**2-253**	**Precision, Fast Settling, Dual AD744**
***AD796**	**0.3–0.5**	**3–12**	**0.002–0.004**	**2**	**1**	**12–0.01**	**2, 6, 7**	**C, I, M**	**2-267**	**Low Power, Low Cost, Photodiode Preamp**
AD648	**0.3–2**	**3–20**	**0.01–0.02**	**1**	**1.8**	**8**	**2, 3, 6, 7**	**C, I, M**	**2-127**	**Low Power, BiFET, Dual AD548**
AD712	**0.3–3**	**5–20**	**0.05–0.075**	**4**	**20**	**1**	**2, 3, 6, 7**	**C, I, M**	**2-189**	**Excellent AC and DC Performance, Dual AD711**
OP-10	0.5	2–4.5	3–7	0.6	0.17	—	3	C, M	2-555	Dual Matched, Precision
SSM-2139	0.5	2.5	80	30	11	—	2, 6	I	AV	Audio, Low Noise
OP-249	**0.5–0.7**	**5–6**	**0.05–0.075**	**4.7**	**22**	**0.9–0.01**	**2, 3, 4, 6, 7**	**I, M**	**2-855**	**Fast, Low Distortion**
AD642	0.5–2	1–3.5	0.035–0.075	1	3	—	7	C, M	2-101	Dual AD542
AD644	0.5–2	—	0.035–0.075	2	13	—	7	C, M	2-107	Dual AD544
OP-04	0.75–5	8–20	50–100	1.3	0.5	—	3, 7	I, M	2-511	Improved "747"
OP-14	0.75–5	8–20	50–100	1.3	0.5	—	2, 3, 6, 7	I, M	2-511	General Purpose, Low Cost
OP-15	**0.75–5**	**8–20**	**50–100**	**1.3**	**0.5**	**—**	**2, 3, 6, 7**	**I, M**	**2-571**	**Improved "1458" Dual**
***OP-275**	**1**	**—**	**350**	**9**	**22**	**—**	**2, 6**		**2-919**	**Dual Audio Amp**
OP-215	**1–4**	**10**	**0.1–0.3**	**5.7**	**18**	**0.9–0.1**	**2, 3, 4, 6, 7**	**C, I, M**	**2-819**	**High Speed, Precision**
***OP-282**	**2.0**	**10**	**0.1**	**4.0**	**9**	**1.5**	**2, 3, 6**	**I**	**2-927**	**Dual High Speed, Low Power**
AD827	**4.0**	**15**	**7000**	**50**	**300**	**0.120–0.1**	**2, 3, 6**	**C, I, M**	**2-301**	**Dual AD847, High Speed, Low Power**
OP-260	**3.5–7**	**10**	**1000–15000**	**90**	**1000**	**0.25–0.1**	**2, 3, 4, 6, 7**	**I, M**	**2-873**	**Dual High Speed, Current Feedback**

Quad Operational Amplifiers

Model	V_{OS} mV max	V_{OS} TC µV/°C max	I_B nA max	BW MHz typ[1]	Slew Rate V/µs typ	Settling Time to 0.01% µs typ	Package Options[2]	Temp Ranges[3]	Page	Comments
AD704	0.075–0.10	1.0–1.5	150–270	0.8	0.10	—	2, 3, 6	C, I, M	2-137	Quad AD705, Low I_B Precision Bipolar
***OP-497**	**0.05–0.15**	**0.5–1.5**	**150–200**	**0.5**	**0.15**	**—**	**2, 3, 4, 6**	**I, M**	**2-1049**	**Low Power, Low I_B Precision Bipolar**
OP-400	**0.15–0.3**	1.2–2.5	**3–7**	**0.5**	**0.15**	**—**	**2, 3, 4, 6**	**C, I, M**	**2-975**	**Quad Monolithic, Precision**
***OP-495**	**0.2–0.5**	**<10**	**15**	**0.085**	**0.04**	**—**	**2, 3, 6**	**I, M**	**2-953**	**Rail to Rail**
OP-470	**0.4–1**	**2–4**	**25–60**	**6**	**2**	**—**	**2, 3, 4, 6**	**C, I, M**	**2-1005**	**Quad Monolithic, Low Noise**
***OP-467**	0.5	3.5	**100**	**30**	**170**	**170**	**2, 3, 5, 6**		**2-999**	**30 MHz, Low Power**
OP-490	**0.5–1**	5	**15–25**	**0.02**	**—**	**—**	**2, 3, 4, 6**	**I, M**	**2-1037**	**Micropower, Low Voltage, Single Supply**
AD713	**0.5–1.5**	**15**	**35–100**	**4**	**20**	**1**	**2, 3, 6**	**C, I, M**	**2-201**	Superior AC and DC Performance, Quad AD711
OP-09	0.5–5	10–15	300–500	3	1	—	3	C, M	2-547	Improved "4136"
OP-11	**0.5–5**	**10–15**	**300–500**	**3**	**1**	**—**	**2, 3, 4, 6**	**C, I, M**	**2-547**	**Improved Quad "741"**
OP-471	**0.8–1.8**	**4–7**	**25–60**	**6.5**	**8**	**—**	**2, 3, 4, 6**	**C, I, M**	**2-1021**	**Monolithic, Fast, Low Noise**
***OP-482**	**3.0**	**10**	**0.1**	**4.0**	**9**	**1.5**	**2, 3, 5, 6**	**I**	**2-927**	**High Speed, Low Power**
OP-421	2.5–6	10–15	50–150	1.9	0.5	—	2, 3, 6	I, M	2-993	Low Power, Low Cost, Single Supply
OP-420	2.5–6	10–25	20–40	0.15	0.05	—	2, 3, 4, 6	I, M	2-987	Micropower, Low Cost, Single Supply

Unity Gain Buffers

Model	−3 dB BW MHz typ	SR V/µs min	Settling Time to 0.02% ns typ	Rise Time 1V Step ns typ	I_{OUT} mA min	V_{OS} mV typ	I_{SS} mA max	Package Options[2]	Temp Range[3]	Page	Comments
AD9630	**750**	**1800**	**8**	**0.9**	**50**	**3**	**26**	**2, 3, 6**	**I, M**	**2-461**	**High Performance, Wide-Band Buffer**
***AD9620**	**600**	**2200**	**8**	**0.8**	**40**	**2**	**48**	**1**	**I, M**	**2-455**	**High Performance, Low Harmonic Distortion Buffer**
BUF-03	50	220	100 (0.1%)	7 (1/2 V)	70	10	25	7	C, M	2-489	High Speed Voltage Follower/Buffer

[1]Unity gain small signal bandwidth.
[2]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack, 11 = Single-in-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92; 17 = Plastic Pin Grid Array.
[3]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.
[4]AV = *Audio/Video Reference Manual.*
Boldface Type: Product recommended for new design.
*New product.

Orientation
Operational Amplifiers

The amplifiers listed in this volume are intended to provide cost-effective solutions to the bulk of op amp requirements in precision measurement and control, as well as to more general requirements within electronic circuits. The technical data included here* covers properties of approximately 100 different op amp families, comprising several hundred distinct types. Some amplifiers are general purpose; others provide near optimum performance for specific classes of application.

The amplifiers differ in a variety of ways, for example, circuit technology, circuit architecture, package type and contents, input properties, output properties, operating temperature range and in terms of the many performance specifications. Most devices are monolithic ICs, including precision and high speed single, dual and quad devices, while some also are hybrid ICs.

The amplifiers catalogued in this volume are available in a broad choice of packaging styles, temperature ranges, and performance grades. If your application calls for versions of these products that have been processed in accordance with MIL-STD-883, a wealth of relevant information can be found in the latest edition of the *Military Products Databook*, available free upon request from Analog Devices.

BACKGROUND

The operational amplifier is today the most widely used analog subassembly. It is safe to say that its *basic* properties and applications are sufficiently understood by most circuit designers and builders. However, the basis for choice, the subtleties of using op amps in circuits for best results (especially in precision measurement and control) and the varieties of possible applications are less clearly understood by op amp users, in varying degrees.

In these few pages, we shall address the question of making a proper choice of op amp type for an application, in relation to the extensive array of device properties presented in the data sheets that follow.

For those users requiring basic tutorial material and detailed information on getting the most out of op amps, at the end of this orientation section we have provided a bibliography that should make available up to 99% of information needed now and then, with "fanout" to the vast body of literature that—with some redundancy—will provide the remainder. Analog Devices' op amp data sheets are an excellent source of pertinent information.

SELECTION PRINCIPLES

In selecting the right device for a specific application, you should have clearly in mind your design objectives and a firm understanding of what the published specifications mean. Beyond this, you should detail the significant variables that are pertinent to your application. The purpose of this section is to put these many decision factors into perspective to help you make the most meaningful buying decisions.

*In addition to the listed products recommended for new designs, a number of older products are still available (see page 9–4); data sheets are available on request.

To make a proper choice of an operational amplifier for any given set of requirements, the designer must have:

1. *A complete definition of the design objectives.*
   Signal levels, closed-loop gain, accuracy desired, bandwidth requirements, circuit impedance, environmental conditions and other factors must be well defined before selection can be effectively undertaken.
2. *A firm understanding of what the manufacturer means by the numbers published for the parameters.*
   Two manufacturers may have comparable published specifications, but they may result from the use of differing measurement techniques. This creates a pitfall in op amp selection. To avoid these difficulties, the designer must know what the published specifications mean as well as how the parameters are measured, and then must be able to translate the published specifications into terms meaningful to the design requirements.

There are three fundamental aspects to the rational selection of an operational amplifier for a given application: (1) establishing the circuit architecture, (2) defining the performance levels and (3) choosing the amplifier(s).

1. To obtain a circuit building block to implement a defined functional job, the principal choices are either to purchase a committed functional device, or to design a circuit employing op amps to perform the function. For example, to obtain a difference between two voltages, one may either purchase an instrumentation or isolation amplifier or design a suitable subtraction circuit using op amps. If a committed functional building block with appropriate specs and price is not available, the circuit designer must start by developing schematic diagrams of circuits that will perform the function simply using "ideal" operational amplifiers. Most commonly used circuits can be found in textbooks, "cookbooks" and linear circuit books as well as in application notes and data sheets.
2. Recognizing that the choice of an op amp depends upon both the overall circuit requirements and the characteristics of available devices, the design should interpret the desired overall performance in terms of the parameters of op amps, and establish acceptable ranges of the various parameters and their variation with time, temperature, supply voltage, etc. Examples of key parameters are input offset voltage, input bias and offset currents, and the high frequency performance and transient behavior of the op amp block (and its effect on the closed-loop circuit), for both large and small signals. It will be helpful to develop an application checklist which includes such considerations as the character of the input signals and their impedance, the output load, the desired accuracy—static and dynamic—the available power supplies, and other environmental conditions.
3. The designer must then relate acceptable performance of the op amp building block to the specifications and prices of available devices from preferred suppliers, bearing in mind a firm understanding of the way in which manufacturers define their specifications, and how definitions can differ in misleading ways. A set of definitions used by Analog Devices follows this discussion.

APPLICATION CHECKLIST

By way of an application checklist, the designer will need to account for the following:

Character of the application: The character of the application (inverter, follower, differential amplifier, etc.) will often influence the choice of amplifier. For example, an adjustable-gain wideband application may call for a transimpedance op amp to keep bandwidth independent of gain setting.

Accurate description of the input signal: It is extremely important that the input signal be thoroughly characterized. Is the input a voltage source or current source? Range of amplitude? Source impedance? Time/frequency characteristics?

Environmental conditions? What is the maximum range of temperature, time and supply voltage over which the circuits must operate (to the required accuracy) without readjustment?

Accuracy desired: The accuracy requirement determines the extent to which the foregoing considerations are critical, and ultimately points the way to a device (or series of devices) which are acceptable. Accuracy of course, must be defined in terms meaningful to the application with regard to bandwidth, dc offset and other parameters.

SELECTION PROCESS

In general, the objective of amplifier selection should be to choose the least expensive device which will meet the physical, electrical and environmental requirements imposed by the application. This suggests that a "General Purpose" amplifier will be the best choice in all applications where the desired performance requirements can be met. Where this is not possible, it is generally because of limitations encountered in two areas—bandwidth requirements and/or offset and drift parameters.

To make it easier to relate bandwidth requirements with the drift and offset characteristics, a capsule view of bandwidth considerations precedes the dc discussion below. The reader is then returned to an expanded discussion of gain bandwidth considerations.

Gain Bandwidth Considerations, a Capsule View

Although all selection criteria must be met simultaneously, determination of the bandwidth requirements is a logical starting point because:

1. If dc information is not of interest, a suitable blocking capacitor can be connected at the amplifier input and/or output and all of the "drift" specifications may usually be ignored, and,
2. Where high frequency (>10 MHz) characteristics are of primary importance, the choice will be limited to those amplifiers designated "Wide Bandwidth/Fast Settling."

Where dc information is required and where frequency requirements are relatively modest (full power response below 100 kHz, unity gain bandwidth of less than 1.5 MHz) other criteria will probably influence the final choice. It is important, however, to choose an amplifier with which an adequate value of loop gain is assured (at the maximum frequency of interest) to obtain the desired accuracy. Loop gain is the excess of open-loop gain over closed-loop gain, and is responsible for the diminishing error due to fluctuations in the open-loop gain due to time, temperature, etc. For example, if the design closed-loop gain is 1,000, the open-loop gain must be at least 100,000 to yield an error of no more than 1%, and 1,000,000 to yield an error no greater than 0.1%. Where undistorted response is required, the specifications for full linear response and slewing rate should be chosen such that they are not exceeded at the highest frequency of operation.

Distinctions Within the Overall Class of Operational Amplifiers

The conventional or classical operational amplifier is a *voltage-in/voltage-out* device, and may also be called a "voltage input" amplifier. It is called a voltage input amplifier because it amplifies small differences of two voltages between the respective input terminals (V_i), and it delivers an output in terms of voltage, V_o. The gain rating of this type of amplifier is given in terms of V/V or V/μV (or $-V_o/-V_i$).

Both amplifier inputs are voltage driven, and essentially do not load the signal and feedback sources. This type of amplifier has a constant gain bandwidth product, therefore increases in closed- loop gain necessarily result in reductions in closed-loop bandwidth. In this discussion, the term "V/V amplifier" is intended to mean this classical type of op amp, a differential input/voltage sensitive device.

However, for wide bandwidth applications, it is often useful to consider applying an amplifier class using *current feedback*, or, called alternately, a *transimpedance* amplifier. This type of amplifier is characterized for gain by the *transresistance* ($-V_o/-I_i$), where the input current I_i is an error current flowing into the amplifier's inverting input. The inverting input of a transimpedance amplifier has a characteristically *low* (ideally zero) input impedance. This input is considered to be current driven (as opposed to voltage driven) in the design of circuits using this amplifier. The low impedance at this input minimizes the gain-error voltage developed by the input current.

As a class of amplifier, transimpedance types tend to be characterized by high slewing rates and high closed-loop bandwidths. In contrast to the mentioned constant gain bandwidth of V/V or voltage input amplifiers, the closed-loop bandwidth of a current feedback amplifier is essentially independent of closed-loop gain —as long as the feedback resistance is kept constant when the gain is adjusted. This feature often makes them the choice amplifier type, where bandwidth considerations are paramount.

Note: A caveat which applies to transimpedance amplifiers is the fact that they have nonsymmetric input impedances. As mentioned, the inverting input impedance is low, but the non-inverting input is voltage driven, and functions generally like the noninverting input of a voltage input amplifier.

Offset and Drift Considerations

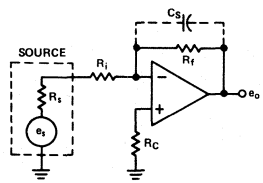
In the majority of op amp applications, final selection is determined by the dc offset and drift characteristics. To undertake amplifier selection in these cases, it is necessary to translate the requirements listed above as follows. (It is assumed that bandwidth requirements and temperature range have been established at this point.)

1. *What input impedance must the circuit present to the signal source?* This depends primarily on the source impedance, R_s and the amount of loading error which is acceptable. Most amplifier circuits are designed around the inverting and noninverting circuits of Figure 1. The choice is often made between the

two to accommodate impedance requirement(s). Input impedance for the inverting circuit is approximately equal to the summing impedance, R_i, and the upper limit on the magnitude of R_i is determined by the allowable drift error because of bias currents as discussed below. The noninverting circuit offers inherently higher input impedance than the inverting circuit (due to "bootstrapping" feedback), and in this case input impedance is approximately equal to the amplifier common-mode impedance, R_{cm}.

2. *How much drift error can be tolerated?*
The question is related to the input signal level, e_s, and the required input signal of one volt with an accuracy of 0.1%, the offset drift error, V_d, must be one millivolt or less. (This assumes that other sources of error such as input loading, noise and gain error have already been allowed for.) By the same reasoning, the allowable drift error for a 1 volt signal and 0.01% accuracy would be 100 μV.

When this has been defined, the allowable limits of offset voltage (e_{os}), bias current (i_b) and difference current can be calculated by the equations of Figure 1.



$$e_o = -\frac{R_f}{R_i}\left[e_s + e_{os}\left(\frac{R_f + R_i}{R_f}\right) + I_b R_i\right]$$

Signal | Input Drift Error = V_d

For $R_C = 0$ and $R_s \ll R_i$

$$e_o = -\frac{R_f}{R_i}\left[e_s + e_{os}\frac{R_f + R_i}{R_f} + i_d R_i\right]$$

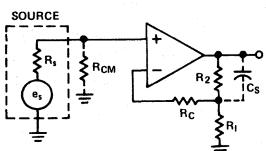
Signal | Input Drift Error = V_d

For $R_C = R_i R_f/(R_i + R_f)$ and $R_s \ll R_i$

Input Impedance $R_{IN} \approx R_i$

% Drift Error = $\frac{100V_d}{e_s}$

Figure 1a. Inverting Configuration



$$e_o = \frac{R_2 + R_i}{R_i}\left[e_s + e_{os} + i_b R_s\right] \text{ for } R_C = 0$$

Signal | Drift Error = V_d

$$e_o = \frac{R_2 + R_i}{R_i}\left[e_s + e_{os} + i_d R_s\right] \text{ for } R_C = R_s - \frac{R_i R_2}{R_i + R_2}$$

Signal | Drift Error = V_d

Input Impedance $R_{IN} \approx R_{CM}$

% Drift Error = $\frac{100V_d}{e_s}$

Figure 1b. Noninverting Configuration

For example, in the case of the inverting circuit, an offset error voltage, i_bR_i, is generated by the bias current flowing through the summing impedance. This error increases for increasing R_i. Since R_i also sets the input impedance, there is a conflict between high input impedance and low offset errors. Likewise, for a given offset error, higher values for R_i can be used with an amplifier which has lower bias current.

Where it will otherwise function properly, the noninverting circuit generally makes a better choice for high input impedance circuits. Also, for the same source and input impedance requirement, a given amplifier will generate lower offset errors for the noninverting circuit than for the inverting circuit. This is so because the bias current flows only through R_s for the noninverter and this will always be less than the input impedance, R_i, of the inverter. Input impedance of the noninverter (approximately R_{cm}) is typically 10^7 ohms even for the least expensive bipolar amplifiers and up to 10^{11} ohms for FET types.

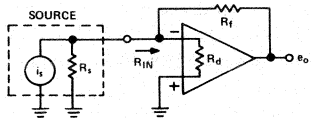
Unfortunately, however, the noninverting configuration cannot always be used since it is not convenient to use for many circuit functions such as integration or summation. A further limitation occurs in high accuracy applications where common-mode errors may rule out this circuit configuration. Transimpedance amplifiers in the noninverting configuration have high dynamic input impedance, but they must be driven from a source that can furnish the input current. This rules out the possibility of unloading some high impedance sources but still permits a single amplifier to be used for noninverting gains (as always, it is helpful to consult the data sheet).

Note: In both figures, there is shown an optional bias compensation resistance, R_c. The use of R_c will minimize offset voltage errors due to bias current for many conventional amplifiers, by making the error proportional to the offset current (a reduction of 10 or more times). However, this will only be true for amplifiers which do not already use internal bias current compensation, such as for example the AD847. An example where it does not apply is with OP-07 family types, such as the OP-177 or AD707, which are internally bias current compensated. Also, it does not apply at all to transimpedance amplifiers, as the two bias currents of these amplifiers are unrelated and cannot be compensated. In case of doubt, study the data sheet −bias and offset current specs nominally equal (±) imply use of internal bias current compensation.

Initial offsets can usually be zeroed at room temperature so that only the maximum temperature excursion (−T) from +25°C need to be considered. For example, over the range of −25°C to +85°C, the maximum temperature excursion (−T) from +25°C would be 60°C. As a practical matter, offset errors due to supply voltage and time drift can generally be neglected since errors due to temperature drift are usually much greater.

Current Amplifier Considerations

Before leaving the subject of offset errors, we shall discuss briefly the current amplifier configuration which is shown in Figure 2a. The obvious approach to measuring current is to develop a voltage drop across a load resistor, R_f, and to measure this potential with a high impedance amplifier as shown in Figure 2b.



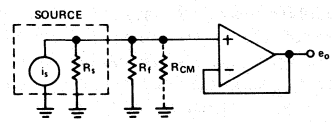
$$e_o = -R_f \left[i_s + e_{os} \left(\frac{R_f + R_s}{R_s R_f} \right) + i_b \right]$$

Signal — Drift error = Iε

$$\text{Input Impedance } R_{IN} = \left(\frac{R_f R_d}{R_f + R_d} \right) \left(\frac{1}{1 + A\beta} \right)$$

$$\text{where } 1/\beta = 1 + \frac{R_f (R_s + R_d)}{R_s R_d} \qquad \% \text{ Drift Error} = \frac{100\, I\epsilon}{i_s}$$

Figure 2a. Current Amplifier



$$e_o = R_f i_s + e_{os} + i_b R_f \text{ for } R_s > R_f$$

Signal — Drift Error = V_d

$$\text{Input Impedance } R_{IN} \approx R_f$$

$$\% \text{ Drift Error} = \frac{100 V_c}{R_f i_s}$$

Figure 2b. Voltage Amplifier with Sampling Resistor

This approach has several disadvantages as compared to the circuit of Figure 2a. First, the noninverting amplifier introduces common-mode errors which do not occur for Figure 2a. Second, an ideal current meter would have zero impedance whereas R_f in Figure 2b may become very large, since this resistor determines the sensitivity of the measurement. Third, the changes of input impedance, R_{cm}, for the noninverting amplifier with temperature will cause variable loading on R_f and hence a change in sensitivity.

The current amplifier of Figure 2a circumvents all of these difficulties and approaches an ideal current meter; that is, there is essentially no voltage drop across the measuring circuit, since with enough open-loop gain, A, the input impedance R_{IN} becomes very small.

In selecting a current amplifier, the most important consideration is current noise, and bias current drift. Measuring accuracy is largely the ratio of current noise and drift to signal current, i_s. To obtain the drift of error current I_e referred to the input, use the following expression.

$$-I_e = \left[\frac{\Delta e_{os}}{\Delta T} \left(\frac{R_f + R_s}{R_f R_s} \right) + \frac{\Delta i_B}{\Delta T} \right] \Delta T$$

Now, to make a proper selection you must pick an amplifier with an error current, I_e, over the operating temperature which is small compared to the signal current, i_s. Do not overlook current noise which may be more important than current drift in many applications. Likely candidates here might be from FET input families such as the AD645, OP-41, etc., or bias current compensated Super-β input types, such as the OP-97/297/497 or the AD705/706/704 units.

Gain Bandwidth Considerations, Expanded Discussion

From the previous discussion, it is apparent that most general purpose operational amplifiers will usually give adequate performance for dc and audio-frequency-range applications. However, amplifiers having unity-gain bandwidth above 5 MHz, full power response above 100 kHz and slewing rate above 6 V/μs, in general require more specialized design techniques. Amplifiers with wideband, fast response characteristics have been listed in the Wide Bandwidth group to simplify the selection for higher frequency applications.

One factor often overlooked is that stray capacitance and impedance levels of the external feedback circuit can be the major limitation in high frequency applications. For example, in Figure 1a, if R_f were one megohm, and stray capacitance, C_s, were one picofarad, then the closed-loop bandwidth would be limited to 160 kHz ($1/(2\pi R_F C_S)$), regardless of how fast the amplifier may be. Moreover, output slewing rate will be limited by how fast C_s can be charged, which in turn is related to signal level, e_s, and input impedance R_i, by $de_o/dt = -e_s/R_iC_s$. For these reasons it is usually not possible to obtain both fast response and high input impedance for an inverting circuit since both R_i and R_f must be large to obtain high input impedance.

Another advantage of the noninverting circuit (Figure 1b) is that the feedback network is potentiometric, and is thus relatively independent of the absolute values for R_1 and R_2. Therefore, a low impedance can be used for R_2 so that stray capacitance of C_s will not limit the circuit's bandwidth. In this case the minimum value for R_2 is constrained only by the output current rating of the amplifier. Again the trade-off between the frequency response and input impedance of the inverting and noninverting circuits must be evaluated in light of the common-mode rejection error (with frequency) introduced by the noninverter.

For greater emphasis, wideband applications can be separated into categories—steady state and transient. Since the amplifier requirements for the two are somewhat different, these categories will be discussed separately.

STEADY STATE APPLICATIONS

Steady state applications involve amplifying or otherwise manipulating *continuous* sinusoidal, complex or random waveforms. In these applications the significant issues in choosing an amplifier are as follows:

1. *Is dc coupling required?*
   If dc information is not of consequence, then offset drift errors are not usually important and a capacitor can be used if necessary to block the output dc offset. Your only concern here is that dc offset at the output does not become so large, as might be the case with a high gain stage, that the output is saturated or the dynamic swing for ac signals is limited. One way to circumvent the latter problem is to use feedback to limit the gain at dc as shown in Figure 3. The gain of this kind of circuit can be small at dc but large at high frequencies.

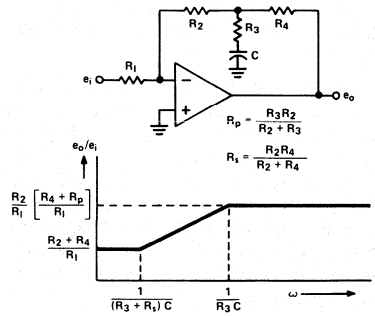


Figure 3. DC Feedback Minimizes Output Offset for AC Applications

2. *What closed-loop gain and bandwidth are required?*
Closed-loop gain, G, is dictated by the application. For V/V amplifiers, to a first approximation the intersection of the open- and closed-loop gain curves in Figure 4 gives the closed- loop bandwidth, F_{c1} (−3 dB). For high gain, wide-band requirements, it may be necessary, or more economical, to use two amplifiers in cascade, each operating at lower gain. When using transimpedance amplifiers, f_{c1} changes little over a wide range of gain as set by the choice of R_g, with R_f (the feedback resistor) held constant.

3. *What loop gain is required or alternatively what gain stability, output impedance and/or linearity are necessary?*
The available loop gain at a particular frequency or over a range of frequencies is very often more important than closed-loop bandwidth in selecting an amplifier. Loop gain, as illustrated in Figure 4, is defined as the difference, in dB, or as the ratio, arithmetically, of the open- to closed-loop gain (Aβ = A/G). You will find in most of the equations defining the closed-loop characteristic of a feedback (V/V) amplifier that the loop gain (Aβ) is the determining factor in performance. Some of the more notable examples of this point are as follows:

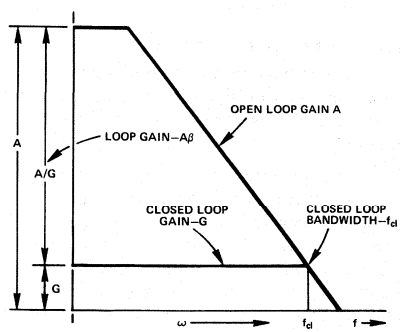


Figure 4. Closed-Loop Bandwidth and Loop Gain

a. Closed-loop gain stability = −G/G
$-G/G = (-A/A)\,[1/(1 + A\beta)]$,
where −A/A is the open-loop gain stability, usually about 1%/°C.

b. Closed-loop output impedance = $Z_{ocl} = Z_o/(1 + A\beta)$, where Z_o is the open-loop output impedance (can vary from 10 Ω to above 1 kΩ, dependent upon the specific type).

c. Closed-loop nonlinearity = $L_{cl} = L_{ol}/(1 + A\beta)$, where L_{ol} is the open-loop linearity error, usually less than 5%.

A loop gain of 100 dB, or 40 dB, is adequate for most applications, and this is readily achievable at dc and low frequencies. But note that loop gain decreases with increasing frequency which makes it difficult to obtain large loop gains at high frequencies. For this reason it may be necessary to use a 10 MHz unity gain amplifier in order to obtain adequate feedback over a 10 kHz bandwidth.

4. *What full power response and/or slew rate are required?*
You should examine your expected output waveform and select an amplifier whose SR (with the expected capacitive loading), exceeds the maximum rate of change of an ideally scaled output signal. For a sinusoidal waveform with a peak voltage output equal to the rated amplifier output (e_p), the signal frequency should not exceed f_p, the rated full power response of the amplifier.

$$f_p = SR/(2\,\pi\,e_p)$$

As a useful rule of thumb, a amplifier SR of 1 V/μs will support an f_p of 16 kHz at a 10 V (peak) output level. As the output signal voltage is reduced below the rated output voltage, the usable maximum frequency is be extended proportionately. Note: If you do not observe these restrictions, you will get distortion and unexpected dc offset at the amplifier output.

For some monolithic amplifier designs intended for high-gain and wide-bandwidth applications, their frequency response is not a simple 6 dB roll-off; the response may be shaped with external RC components for improved performance at lower closed-loop gains. Using feedforward or phase lag compensation networks, gain-bandwidth product and/or full power response may be shaped to meet varying design requirements. Most internally compensated V/V op amps offer a stable 6dB per octave roll-off with specified unity gain-bandwidth and slew rate thereby limiting maximum speed and response to those published specifications.

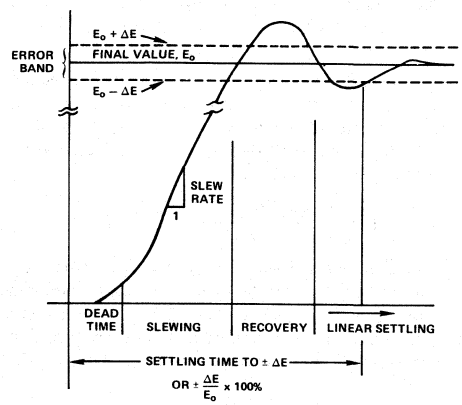


Figure 5. Typical Settling Time Characteristics

TRANSIENT APPLICATIONS

In applications such as A/D and D/A converters and pulse amplifiers, the transient response of the wideband amplifier is generally more important than the gain bandwidth characteristic described above. Slewing rate, overload recovery and settling time are the specifications which determine the transient response.

When applying the high frequency amplifier, it is important to understand how amplifier performance is affected by component selection as well as impedance levels used around the amplifier.

Settling Time

Settling time is defined as the time elapsed from the application of a perfect step input to the time when the amplifier output has entered and remained within a specified error band symmetrical about the final value (Figure 5). Settling time, therefore, includes the time required for the amplifier to slew from the initial value, recover from slew rate limited overload, and settle into a given error band ($E_o \pm -E$) within the linear range.

The time and frequency response of a linear, bilateral network or amplifier are related by well known mathematics. For example the step response for a well behaved, ideally linear, 6 dB/octave amplifier with a closed-loop bandwidth of ω_{CL} is shown in Figure 6.

However, since settling time is determined by a combination of amplifier characteristics (both linear and nonlinear) and because it is a closed-loop parameter, it cannot be readily predicted from the open-loop specifications such as slew rate, small signal bandwidth, etc.

Analog Devices specifies settling time for the condition of unity gain, relatively low impedance levels and no capacitive loading (unless otherwise indicated). A full-scale step input is used to determine settling time and the step is generally unipolar—i.e., from zero to plus or minus full scale. The settling time indicated is generally the longest time resulting from a step of either polarity and is given as a percentage of the full-scope step transition.

Settling time is a nonlinear function. It varies with the input signal level and it is greatly affected by impedances external to the amplifier.

ERRORS DUE TO NOISE

A major criterion in the selection of an amplifier for low level signals is the amplifier input noise, since this is usually the limiting factor on system resolution. In the general case, amplifier noise can be characterized by a voltage source in series with the summing junction and a current source in parallel with the summing junction. Whenever high source impedance is encountered, current noise flowing through the source impedance will appear as an additional voltage noise, combining with the amplifier voltage noise. The sum of these noise sources will then be amplified along with the desired signal. For this reason, selection of a particular amplifier must consider both the amplifier noise performance as well as the source impedance.

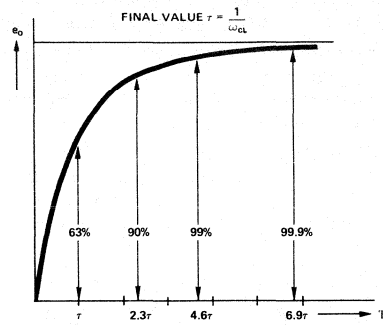


Figure 6. Step Response for Linear 6 dB/Octave Amplifier

Consideration must also be given to noise sources other than the amplifier whenever determining total system noise. RF and digital noise may be fed into an amplifier through any connecting wire, including power supply and output leads. Adequate shielding and low-pass filters on all incoming leads will greatly reduce noise pickup.

Thermal noise is generated in any conductor or resistor as a result of thermal agitation of the electrons. This noise voltage source, sometimes referred to as "Johnson Noise," is generated in the resistive component (R) of any impedance, and has a value:

$$e_n = \sqrt{4kTBR}$$

where, e_n = the rms value of the noise voltage
k = Boltzman's Constant (1.38×10^{23} joules/K)
T = absolute temperature of the resistance, K
B = the bandwidth in which the noise is measured

Since noise is related to the bandwidth over which the measurement is made, no noise specification is meaningful unless the bandwidth for the specification is given. Although the thermal noise equation may appear unwieldy, for most practical noise calculations all that is required to enable rapid approximations is to apply a few simple rules of thumb.

Rules of Thumb

1. Remember that a 100 kΩ resistor generates 40 nV rms in a 1 Hz bandwidth. The noise voltages generated by other resistance values for other bandwidths can be calculated by remembering that the noise is proportional to the square root of the resistance (R) and the bandwidth (BW) as:

$$e_n\ (rms) = (40\ nV/\sqrt{Hz})\left(\sqrt{\frac{R}{100\ k\Omega}\ (BW)}\right)$$

2. To convert the rms noise to a p–p value, a conversion factor is applied. The factor is 6.6 μV (p–p)/μV(rms), for a criterion of less than 0.1% probability of noise peaks exceeding calculated limits.

3. The total rms noise contribution due to several noise sources is determined by the square root of the sum of the squares:

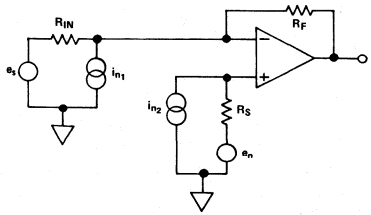
$$e_t = \sqrt{e_a^2 + e_b^2 + e_c^2 + \ldots e_n^2}$$

If any single noise source of this expression is less than a third of another, it may be neglected with a resulting error of less than 5%.

4. Some basic ways to reduce system noise are to restrict bandwidth to a minimum usable range and to use the lowest impedances possible.

DESIGN EXAMPLE

Figure 7a illustrates a typical circuit with noise calculations shown for each noise source. The total of the noise sources is obtained by adding each of the individual sources in a rms fashion.

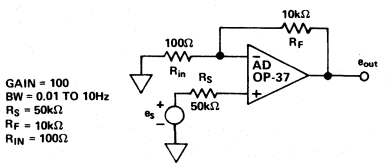


COMPONENT	CAUSE	OUTPUT CONTRIBUTION
R_{IN}	Johnson Noise	$\sqrt{4kTBR_{IN}}\ (R_F/R_{IN})$
R_S	Johnson Noise	$\sqrt{4kTBR_S}\ (R_F/R_{IN}+1)$
R_F	Johnson Noise	$\sqrt{4kTBR_F}$
i_{n_1}	Amp. Current Noise	$i_{n_1} R_F$
i_{n_2}	Amp. Current Noise	$(i_{n_2} R_S)\ (R_F/R_{IN}+1)$
e_n	Amp. Voltage Noise	$e_n\ (R_F/R_{IN}+1)$

$$\text{TOTAL NOISE} = \sqrt{(e_{R_{IN}}\ G)^2 + [e_{R_S}\ (G+1)]^2 + e^2_{R_F} + [(i_{n_1} R_F)^2] + [(i_{n_2} R_S)\ (G+1)]^2 + [e_n\ (G+1)]^2}$$

Figure 7a. Noise Components

Figure 7b illustrates how the Rules of Thumb may be applied in a practical case to approximate the total output noise. In this example, a low noise type amplifier (OP-37) is being used with a 50 kΩ source impedance. The two major noise sources, in addition to the OP-37's input voltage noise of 0.18 μV p–p, are the Johnson noise (59 μV p–p) and current noise (83 pA p–p).



1) RESISTOR NOISE: $R_F \rightarrow 13nV/\sqrt{Hz}$
$R_{IN} \rightarrow (1.3nV/\sqrt{Hz}$
$R_S \rightarrow (28nV/\sqrt{Hz})\ 101 = 2.8\mu V/\sqrt{Hz}$
TOTAL RESISTOR NOISE IN 10Hz BW =
$(2.8\mu V/\sqrt{Hz})\ (\sqrt{10Hz})\ 6.6\mu V\ p\text{-}p/\mu V\ rms = 59\mu V\ p\text{-}p$

2) AMPLIFIER CURRENT NOISE: $(83pA\ p\text{-}p)\ (50k)\ (101) = 422\mu V\ (R_S)$
$(83pA\ p\text{-}p)\ (10k) = 0.8\mu V\ (R_F)$

3) AMPLIFIER VOLTAGE NOISE: $(0.18V\ p\text{-}p)\ (101) = 18.2\mu V\ p\text{-}p$

TOTAL OUTPUT NOISE = $\sqrt{(422)^2 + (59)^2 + (18.2)^2 + (0.18)^2} = 426\mu V\ p\text{-}p$

Figure 7b. Design Example

This noise discussion should be taken in a context of generality, not one which implies that an OP-37 amplifier example is universally useful for lowest noise. Many lower voltage noise devices exist, for instance the AD829 and AD797 amplifiers, and several instrumentation amplifiers/preamps; SSM-2015/2016, and the SSM-2017. Lower current noise devices also exist in the form of many different FET input types, the AD645, OP-42, OP-80, and AD711/712/713 families, and the unusual combination of both low voltage and low current noise in the AD743/745.

As a rule, transimpedance amplifiers will be application dependent in terms of their specification impact on noise. In general they tend to have low voltage noise, but relatively high current noise. The net contribution to noise for a given stage will be dominated by one or the other, dependent upon the working gain and relative impedances.

HOW THE OPERATIONAL AMPLIFIERS ARE CLASSIFIED

To assist the designer in distinguishing among the many types available from Analog Devices, we have provided a Selection Guide in which amplifiers are grouped in terms of common properties which have been optimized in order to satisfy the needs of specific classes of applications. Once the choice has been narrowed to the manageable number of types in any group, distinctions can be drawn in terms of other requirements or considerations.

Temperature Range and Nomenclature

Op amp devices currently available from Analog Devices fall into two broad catalog categories, dependent upon whether the design originated with Analog Devices or with the PMI division. The former parts are generally denoted by an "AD" prefix, while the latter are generally denoted by an "OP" prefix.

The part numbering sequences of both catalog families are briefly summarized below, in terms of "AD original" and "PMI original" numberings. In both cases the suffixes permit identification of the temperature and performance range for which a device is intended.

AD Original Part Numbers (AD PREFIX)

The most popular is the "C" (commercial) range, covering temperatures from 0°C to +70°C. This range is designated by suffixes such as J, K, L, M, in order of increasingly tighter specs (e.g., AD549L). Also popular is the "M" (military) range, −55°C to +125°C, designated by S, T, U, (e.g., AD846S). Note, however, that not all part families will have types with performance specified in this range. There are also types designed for operation in the "I" (industrial) range, −40°C to +85°C, designated by A, B, C (e.g., AD707A, AD707B AD707C). (Note: Some older products with similar suffixes are rated for −25°C to +85°C.)

PMI Original Part Numbers (OP PREFIX)

The most popular is the "COM" (commercial) range, covering temperatures from 0°C to +70°C. It is designated by a suffix such as F, E, in order of increasingly tighter specs (e.g., OP-27F, OP-27E). The "MIL" (military) range, −55°C to +125°C, is designated by C, B, A, (e.g., OP-27C, OP-27B, OP-27A); but again note that not all families will have types with performance specified in this range. The "IND" (industrial) range is −25°C to +85°C, also designated by grades F and E. There is also an "XIND" (extended industrial) range, which is −40°C to +85°C, designated by grade G.

For both catalog categories, it is worth noting that wider temperature range types will generally meet the same or better specs in a more narrow range.

A few amplifier types are second sources for products originally introduced by other manufacturers. In those instances, a more generic nomenclature is used (AD741C or PM-741C), or, it may be further enlarged upon, if superior selections or family relations of the basic generic design are offered (e.g., AD741L, upgrade of 741; OP-02XX, family upgrade of PM-741 family).

SELECTION GUIDES

Seven Selection Guides classify operational amplifiers within these categories:

Low Voltage Noise Amplifiers
High Speed Amplifiers
Precision Amplifiers
Low Power/Micropower Amplifiers
Low Current Noise, Low I_B Amplifiers
Dual Operational Amplifiers
Quad Operational Amplifiers

The choice of category depends on which class of specification is most critical. Within these categories, the selection guide provide comparisons of salient specifications.

These selection areas are somewhat broad; they include various criteria, not all of which are central to the application. For example, if one is seeking a high-input-impedance amplifier for an ac application, voltage offset and drift may be far less critical than bias current, and both of these may be unimportant compared to bandwidth.

With the hope that it will be found useful, the following interpretive list identifies the best device choices in a variety of categories:

(At the extremes of performance are the fastest op amps and the highest precision op amps)

The *fastest* op amps include those having

- The highest *slewing rates*,—the hybrid AD9610 (3,500 V/μs), and the monolithic AD811 (2,500 V/μs), the AD9618 (1,800 V/μs), and the OP-160 (1300 V/μs).
- The lowest *settling time*—the monolithic CB (complementary bipolar) AD840/841/842/846 (110 ns to ±0.01%), the hybrid AD9610 (20 ns to ±0.1%) and the AD9618 (9 ns to ±0.1%).
- The highest *gain-bandwidth*—the AD5539 (1,400 MHz) and the CB AD844 (900 MHz), AD849 (725 MHz) and AD840 (400 MHz).

  High speed op amps are characterized by high slewing rates, fast settling time and wide bandwidth. Fast settling time is especially important in applications with rapidly changing or switched analog data in buffers, D/A converters, and multiplexer circuits; wide small-signal bandwidth is important in preamplification and in handling low-level wideband ac signals; high slewing rate is associated with fast settling time and is also important in handling ac signals having large magnitudes with distortion since the large-signal bandwidth is closely related to the slewing rate.

  ICs using the proprietary Analog Devices CB (complementary bipolar) process contain wideband PNP and NPN transistors that have similar characteristics—without the use of dielectric isolation. Since poor frequency response of lateral PNPs is the source of the bandwidth limitation in conventional linear bipolar processes, CB devices can have much faster response.

The *highest precision* monolithic op amp families include those having

- The grades with the lowest *untrimmed offset voltage*—the OP-177 (10 μV) and AD707 (15 μV).
- The lowest *bias current*—the revolutionary electrometer op amp using top-gate-FET inputs, the AD549 (60 femtoamperes).
- The *lowest drift*—the AD707 and OP-177 (100 nV/°C).
- The highest *open-loop gain* (hence highest accuracy as an integrator and high-gain amplifier)—the AD707 (13×10^6 V/V) and OP-177 (12×10^6 V/V).
- The highest *common-mode rejection*—the AD707 and OP-177 (130 dB).

Precision op amps (in this list) include those emphasizing

- *Low bias current and high input impedance.* These types use the inherently high input impedance and low leakage current of junction field-effect transistors (FETs) to deal with configurations that measure low currents or involve high resistance values. Applications range from general purpose high-impedance circuitry to integrators, current-to-voltage converters, and log-function generation, to measurements with high-impedance transducers such as photomultipliers, flame detectors, pH cells and radiation detectors.
- *High accuracy* through low offset and drift voltage, low voltage noise, high open-loop gain, and high common-mode rejection (CMR). Such types are used for high-accuracy instrumentation, low-level transducer circuitry, precision voltage comparison, and impedance buffering.

  All FET-input op amps from Analog Devices are conservatively manufactured to meet their published bias-current specifications *after full warmup* (some manufacturers specify *initial* current, which is lower than warmedup bias current). Our published max bias current specification applies to *either* input (some manufacturers call "bias current" the average of the two input currents).

For applications needing high, but not extreme, performance or *where high speed and high precision must be combined*, there are a number of device families to be considered.

- The complementary-bipolar AD844 family *combines low offset* voltage (200 μV) with high slewing rate (2000 V/μs).
- The AD744 BiFET family *combines low input bias current* (50 pA) with low settling time (500 ns to ±0.01%).
- The OP-37 family *combines low drift* (600 nV°C) *with wide gain bandwidth* (63 MHz) (families available as both AD and PMI original designs).
- The hybrid AD381/382 combine 50 pA bias current with 0.75 μs settling time (to ±0.1%) and 50 mA output-current range.

Fast amplifiers, which often boast output current ranges of 50 mA or 100 mA, include families with

- *High slewing rate*—the CB monolithic AD811 (2500 V/μs) and AD840/841/842 (400/300/375 V/μs), and the hybrid, AD380 (330 V/μs), and AD9517/9618 (1,400 V/μs).

- *Low settling time*—the monolithic AD847/848/849 (65 ns to ±0.1%) and hybrid HOS-050 (80 ns to ±0.1%, 200 ns to ±0.01%), the AD845 and AD744 families (300 ns and 500 ns to ±0.01%), and the AD9617 (10 ns to ±0.1%) and AD9618 (9 ns to ±0.1%).
- *Wide gain-bandwidth*—the monolithic AD848 (250 MHz) and the hybrid AD9611 (280 MHz) and HOS-050/060 (100 MHz).

High precision monolithic amplifier families start with lower grades of the highest-precision families; beyond this, they include:

- *Low-drift* OP-07/27/37 families (600 nV/°C) (families available as both AD and PMI original designs).
- *High-gain* OP-07 (3×10^6) and OP-27/37 (1×10^6) (family available as both AD and PMI original designs).
- *Low offset and low bias current* OP-97/297/497 and AD704/705/706.
- Wide selection of low bias-current FET-input op amps— the AD645 (2 pA), OP-41 (3.5 pA), AD548 (10 pA), and the AD711 (25 pA).

Many applications require very low power consumption or operation from a single voltage supply.

- *Lowest power consumption* OP-90/290/490 (20 μA per channel and 1.6 V_S).
- *High speed/power ratio* OP-282/482 (9 V/μs @ 250 μA per channel).
- *Single supply and low bias current* OP-80 and AD820/822.

Many of these devices are duplicated in a single package; for example:

- The AD712 is a dual AD711; the AD713 is a quad AD711.
- The OP-297 is a dual OP-97; the OP-497 is a quad OP-97.
- The AD746 is a dual AD744.
- The AD648 is a dual AD548.
- The OP-282 is a dual; the OP482 is a quad.
- The OP-290 is a dual OP-90; the OP-490 is a quad OP-90.
- The AD708 is a dual AD707.

Also included in this section are *buffers*, wideband amplifiers having slightly less than unity gain, low output impedance and high output-current availability (50 mA). Although they can stand alone, a more frequent use is inside-the-loop as a "booster" amplifier to magnify the output power capability of any op amp or reduce the dynamic output impedance without losing precision.

An example is the BUF-03, a low offset, low bias current FET input buffer which slews at 220 V/μs and can deliver ±70 mA of output, operating on supplies of ±15 V. Another example is the AD9630 which operates on ±5 V supplies and can follow slewing rates of up to 1,800 V/μs with a full-power frequency of 125 MHz and deliver voltages up to ±3 V and currents up to ±50 mA.

DEFINITIONS OF SPECIFICATIONS

Absolute Maximum Differential Voltage

Under most operating conditions, feedback maintains the error voltage between inputs to nearly zero volts. However, under overload conditions or between applications, such as voltage comparators, the voltage between the inputs can be large. This specification defines the maximum voltage which can be applied between inputs without causing permanent damage to the amplifier.

Common-Mode Rejection

An ideal operational amplifier responds only to the difference voltage between inputs (e^+–e^-) and produces no output for a *common-mode voltage*, that is, when both inputs are at the same potential. However, due to slightly different gains between the plus and minus inputs, or variations in offset voltage as a function of common-mode level, common-mode input voltages are not eliminated at the output. If the output error voltage, due to a known magnitude of common-mode voltage, is referred to the input (dividing by the closed-loop gain), it reflects the equivalent *common-mode error* voltage (CME) between the inputs. Common-mode rejection ratio (CMRR) is defined as the ratio of common-mode voltage to the resulting common-mode error voltage. Common-mode rejection is usually expressed logarithmically: CMR (in dB) = 20 $\log_{10}$ (CMRR).

The precise specification of CMR is complicated by the fact that the common-mode voltage error can be a highly nonlinear function of common-mode voltage and also varies with temperature. As a consequence, CMR data published by Analog Devices are average figures, assuming an endpoint measurement over the common-mode range specified. The incremental CMR about small values of common-mode voltage may be greater than the average CMR specified but decrease and become less in the neighborhood of large CMV. Published CMR specifications for op amps pertain to low-frequency voltages, unless specified otherwise: CMR decreases with frequency.

Common-Mode Voltage, Maximum

For differential-input amplifiers, the voltage at both inputs can swing about ground (power-supply common) level. *Common-mode voltage* is defined as any voltage (above or below ground) that could be observed at both inputs. The maximum common-mode voltage is defined as that voltage which will produce less than a specified value of common-mode error. This establishes the maximum input voltage for the voltage-follower connections.

Note that for amplifiers which must operate from a single power supply, the operating common mode range usually must include the negative rail, or ground.

Drift vs. Supply

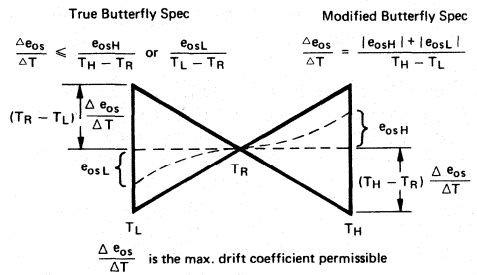
Offset voltage, bias current and difference current vary as supply voltage is varied. Usually, dc errors due to this effect are negligible compared to drift with temperature. No inference may be drawn from this low-frequency specification concerning the effects of rapid variation of voltage at the supply terminals.

Drift vs. Temperature

Offset voltage, bias current and different current all change, or "drift" from their initial values with temperature. This is by far the most important source of error in most precision applications. The temperature coefficients (tempcos) of those parameters are all defined as the average slope over a specified temperature range. Drift can be a nonlinear function of temperature (though it is often quite linear over limited temperature range); the slopes generally are greater at the extremes of temperature than around normal ambient (+25°C), which generally

means that for small temperature excursions in the vicinity of +25°C, the specification is conservative.

Analog Devices precision operational amplifiers are specified by three- (or more) point measurements, at 25°C and at the high and low extremes of the range (T_H, T_L), with the amplifier adjusted to zero at room temperature. The sum of the magnitudes of the drift in the two ranges must be less than the specified drift rate (μV/°C or nA/°C) multiplied by the total temperature range (modified "butterfly"), or, in some cases, the magnitude of the drifts in both ranges must be less than the specified drift rate multiplied by the respective temperature ranges ("true butterfly").



The lowest-cost second-source IC amplifiers are specified only in terms of the maximum value of the parameter (e.g., offset voltage) over temperature in the specified range.

Drift vs. Time

Offset voltage, bias current and difference current change with time as components age. It is important to realize that drift with time is random and rarely—if ever—accumulates linearly for healthy devices. For example, voltage drift might be quoted at 15 μV/month, whereas cumulative drift might not exceed 50 μV in a year. A convenient rule of thumb for extrapolation is to divide the drift for a stated interval by the square root of its ratio to any other interval of interest.

Full-Power Response

The large-signal and small-signal response characteristics of operational amplifiers differ substantially. An amplifier's output will not respond to large signal changes as fast as the small-signal bandwidth characteristics would predict, primarily because of slew-rate limiting in the output stages. Full-power response is specified in two ways: full linear response and full peak response. Full linear response is specified in terms of the maximum frequency, at unity closed-loop gain, for which a sinusoidal input signal will produce full output at rated loads without exceeding a predetermined distortion level. There is no industrywide accepted value for the distortion level which determines the full-linear-response limitation, but unless otherwise noted, we use 3% as a maximum acceptable limit.

In many applications, the distortion caused by exceeding the full linear response can be comfortably ignored, but a more serious effect (often overlooked) is an effect equivalent to dc offset voltage than can be generated when full linear response is exceeded, due to rectification of the asymmetrical feedback waveform or overloading of the input stage by large distortion signals at the summing junction.

Another frequency response that is often of interest is the maximum frequency at which full output swing may be obtained, irrespective of distortion. This is termed "full peak response" and can often be found in a plot of output voltage swing vs. frequency.

Initial Bias Current

Bias current is defined as the current required at either input from an infinite source impedance to drive the output to zero (assuming zero common-mode voltage). For differential amplifiers, bias current is present at both the negative and the positive input. All Analog Devices specifications pertain to the *larger* of the two, *not the average*.

Analog Devices specifies initial bias current, I_b, as the bias current at either input, specified +25°C ambient with the input junctions at *normal operating temperature*. (Some manufacturers specify initial bias current at power turn-on. Such specifications may be misleading. For example, in FET-input amplifiers, bias current is doubled for each 10°C increase; since junction temperatures may warm up to 20°C or more above ambient, the "initial bias current" specs used by some manufacturers may be met only during a brief interval after the power is burned on, and I_b may be quadrupled under ordinary operation conditions.)

Initial Difference Current

Difference current is defined as the difference between the bias currents at the two inputs. Uncompensated input circuitry of differential amplifiers is generally symmetrical, so that bias currents at both inputs tend to be equal and tend to track with changes in temperature and supply voltage. Therefore, difference current is often about 0.1 times the bias current at either input, assuming the initial bias current has not been compensated internally at the input terminals. For amplifiers in which bias currents track, it is often possible to reduce voltage errors due to bias current and its variations by the use of equal impedance loads at both inputs.

Input Impedance

Differential input impedance of voltage-input op amps is defined as the impedance between the two input terminals at +25°C, assuming that the error voltage is nulled or very near zero volts. To a first approximation, dynamic impedance can be represented by a capacitor in parallel with a resistor.

Common-mode impedance, expressed as a resistance in parallel with a capacitance, is defined as the impedance between each input and power-supply common, specified at +25°C. For most circuits, common-mode impedance on the negative input has little significance, except for the capacitance which it adds at the summing junction (one exception is electrometer circuitry). However, common-mode impedance on the plus input sets the upper limit on closed-loop input impedance for the noninverting configuration. Common-mode impedance is a nonlinear function of both temperature and common-mode voltage. For FET-input amplifiers, common-mode resistance is reduced by a factor of two for each 10°C of temperature rise. As a function of common-mode voltage, the resistive component is defined as the average resistance for a common-mode change from zero to the maximum common-mode voltage. Incremental resistance may be less than the specified average value, especially at full-scale for some FET-input amplifiers.

Input Offset Voltage
Offset voltage is defined as the voltage required at the input from zero source impedance to drive the output to zero; its magnitude is measured by closing the loop (using low values of resistance) to establish a large fixed gain, measuring the amplified error at the output and dividing the measured value by the gain.

The initial offset voltage is specified at +25°C and rated supply voltage. In most amplifiers, provisions are made to adjust initial offset to zero with an internal trim potentiometer.

Input Noise
Input voltage- and current-noise characteristics can be specified and analyzed in much the same way as offset-voltage and bias-current characteristics. In fact, long-term drift can be considered as noise which occurs at very low frequencies. When evaluating noise performance, bandwidth or period must be considered. Also rms noise from different sources is summed by root-sum-of-squares, rather than linear, addition. Depending on the amplifier design, noise may have differing characteristics as a function of frequency, being dominated by "1/f noise," resistor noise or junction noise, at various frequencies.

For this reason, several noise specifications are given. Low-frequency noise in the band 0.01 Hz to 1 Hz (or 0.1 Hz to 10 Hz) is specified as peak-to-peak, with a 3.3Â uncertainty, signifying that 99.9% of the observed peak to peak excursions will fall within the specified limits. Wideband noise is specified as rms. For some amplifiers types, spectral-density plots or "spot noise," at specific frequencies, in $nV/\sqrt{Hz}$ or $pA/\sqrt{Hz}$, are provided.

Open-Loop Gain
Open-loop gain is defined as the ratio of a change of output voltage to the voltage applied between the amplifier inputs to produce the change. Gain is specified at dc. In many applications, the frequency dependence of gain is important; for this reason, the typical open-loop gain as a function of frequency is also published for each amplifier type. See also *unity gain small signal response*.

For *transimpedance amplifiers*, since the input is a current and the output is a voltage, the "gain" is expressed in ohms ($R_T = -V_o/-I_i$). Because small changes in current cause large voltage changes, the transimpedance can be quite large—e.g., 100 MΩ for the AD846. As long as the amplifiers' internal input impedance is very low, errors in closed-loop circuitry depend principally on the ratio, R_F/R_T, relative to unity—where R_F is the feedback resistance and R_T is the transimpedance. It will be recalled that, in V/V op amps, the increase in error depends mainly on $R_F/(AR_I)$, where A is the open-loop gain and R_I is the resistance of the external input resistor. The significant difference is that, as gain or transresistance decreases with increasing frequency, the error in transimpedance-amplifier circuits is independent of R_I, hence closed-loop gain can be increased by reducing R_I without substantially affecting bandwidth.

Overload Recovery
Overload recovery is defined at the time required for the output voltage to recover to the rated output voltage from a saturated condition caused by a 50% overdrive. Published specifications apply for low impedances and contain the assumption that overload recovery is not degraded by stray capacitance in the feedback network.

Rated Output
Rated output voltage is the minimum peak output voltage which can be obtained at rated current or a specified value of resistive load before clipping or out-of-spec nonlinearity occurs. Rated output *current* is the minimum guaranteed value of current supplied at the rated output voltage (or other specified voltage). Load impedances less than the specified (or implied) value can be used, but the maximum output voltage will decrease, distortion may increase, and the open-loop gain will be reduced. (All models are short-circuit protected to ground, and many are safe against shorts to the supplies.)

Settling Time
Settling time is defined as the time elapsed from the application of a perfect step input to the time when the amplifier output has entered and remained within a specified error band symmetrical about the final value. Settling time, therefore, includes the time required: for the signal to propagate through the amplifier, for the amplifier to slew from the initial value, recover from slew-rate limited overload (if it occurs) and settle to a given error in the linear range. It may also include a "long-tail" due to the time required to reach thermal equilibrium, or the settling time of compensation circuits. Settling time is usually specified for the condition of unity gain, relatively low impedance levels, and no (or a specified value of) capacitive loading, and any specified compensation. A full-scale unipolar step input is used, and both polarities are tested.

Although settling time can generally be grossly inferred from the other amplifier specifications (an amplifier that has extra-wide small signal bandwidth, extra-fast slewing and excellent full-power response may reasonably—but not always—be expected to have fast settling), the settling time cannot usually be rationally predicted from the other dynamic specifications.

Slewing Rate
The slewing rate of an amplifier, usually in volts per microsecond (V/μs), defines the maximum rate of change of output voltage for a large input step change.

Unity-Gain Small-Signal Response
Unity-gain small-signal response is the frequency at which the open-loop gain (or its projection on a Bode plot) falls to 1 V/V, or 0 dB under a specified compensation condition. For amplifiers having 6 dB-per-octave rolloff, this frequency is also called *unity-gain bandwidth*; for such amplifiers, the gain bandwidth product is essentially constant. "Small signal" indicates that, in general, it is not possible to obtain large output voltage swing at high frequencies because of the distortion due to slew rate limiting or signal rectification.

For amplifiers with symmetrical response for signals applied to either input, the dynamic behavior will be consistent for both inverting and noninverting configurations. However, if feed-forward compensation is used, fast response will be available only on the negative input, restricting fast applications of the device to the inverting mode.

ANALOG DEVICES

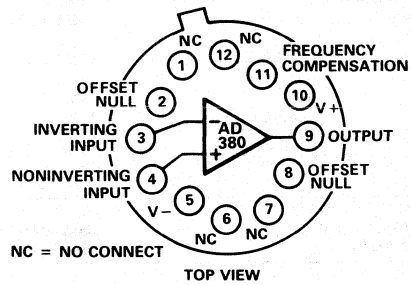
Wideband, Fast-Settling FET-Input Op Amp

AD380

FEATURES

High Output Current: 50mA @ ±10V
Fast Settling to 0.1%: 130ns
High Slew Rate: 330V/μs
High Gain-Bandwidth Product: 300MHz
High Unity Gain Bandwidth: 40MHz
Low Offset Voltage (1mV for AD380K, L, S)

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD380 is a hybrid operational amplifier that combines the low input bias current advantages of a FET input stage with the high slew rate and line driving capability of a fast, high power output amplifier.

The AD380 has a slew rate of 330V/μs and will output ±10V at ±50mA. A single external compensation capacitor allows the user to optimize the bandwidth, slew rate, or settling time for the given application.

A true differential input ensures equally superior performance in all system designs whether they are inverting, noninverting, or differential.

The AD380 is especially designed for use in applications, such as fast A/D, D/A and sampling circuits, that require fast and smooth settling and FET input parameters.

The AD380 is offered in three commercial versions, J, K and L specified from 0 to +70°C and one extended temperature version, the S, specified from −55°C to +125°C. All grades are packaged in hermetically sealed TO-8 style cans.

PRODUCT HIGHLIGHTS

1. The AD380's high output current (50mA @ ±10V) makes it suitable for driving terminated 200Ω twisted pairs.
2. The fast settling output (250ns to 0.01%) makes the AD380 an ideal choice for video A/D and D/A converters and sample and hold applications.
3. The settling wave forms are not only fast but are also very smooth. The absence of large overshoot and oscillations makes the AD380 a very predictable and dependable system element.
4. The high gain-bandwidth product (300MHz) ensures low distortion in high frequency applications.
5. Quick, symmetrical overdrive recovery time (250ns) is assured by an internal antisaturation diode. This is useful in applications where large transient signals may occur.
6. The precision input (1mV offset, max), along with fast settling and high current output make the AD380 an excellent choice for:
   - ATE pin drivers
   - precision coax buffers
   - signal conditioning on pulse waveforms
   - high resolution graphics displays.

AD380—SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

MODEL	AD380JH	AD380KH	AD380LH	AD380SH
OPEN LOOP GAIN				
V_{OUT} = ±10V, no load	40,000 min	*	*	*
V_{OUT} = ±10V, $R_L \geq 200\Omega$	25,000 min	*	*	*
OUTPUT CHARACTERISTICS				
Voltage @ R_L = 200Ω, T_A = min to max	±12V (±10V min)	*	*	*
Output Impedance (Open Loop)	100Ω	*	*	*
Short Circuit Current	100mA	*	*	*
DYNAMIC RESPONSE				
Unity Gain, Small Signal	40MHz	*	*	*
Gain-Bandwidth Product, f = 100kHz, C_C = 1pF	300MHz (200MHz min)	*	*	*
Full Power Response	6MHz	*	*	*
Slew Rate, C_C = 1pF, 20V Swing	330V/μs (200V/μs min)	*	*	*
Settling Time: 10V Step to 1%	90ns	*	*	*
10V Step to 0.1%	130ns	*	*	*
10V Step to 0.01%	250ns	250ns (400ns max)	**	**
INPUT OFFSET VOLTAGE	2.0mV max	1.0mV max	**	**
vs. Temperature[1], T_A = min to max	50μV/°C max	20μV/°C max	10μV/°C max	50μV/°C max
vs. Supply	1mV/V max	*	*	*
INPUT BIAS CURRENT				
Either Input, Initial[2]	10pA (100pA max)	*	*	*
Input Offset Current	5pA	*	*	*
INPUT IMPEDANCE				
Differential	$10^{11}\Omega \| 6pF$	*	*	*
Common Mode	$10^{11}\Omega \| 6pF$	*	*	*
INPUT VOLTAGE RANGE				
Differential[3]	±20V	*	*	*
Common Mode	±12V (±10V min)	*	*	*
Common Mode Rejection, V_{IN} = ±10V	60dB min	*	*	*
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	±(6 to 20)V	*	*	*
Quiescent Current	12mA (15mA max)	*	*	*
VOLTAGE NOISE				
0.1Hz to 100Hz	3.3μV p-p (0.5μV rms)	*	*	*
100Hz to 10kHz	6.6μV p-p (1μV rms)	*	*	*
10kHz to 1MHz	40μV p-p (6μV rms)	*	*	*
TEMPERATURE RANGE				
Operating, Rated Performance	0 to +70°C	*	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*	*
Thermal Resistance θ_{JA}	100°C/W	*	*	*
θ_{JC}	70°C/W	*	*	*
PACKAGE OPTION[4]				
TO-8 Style	H12-A	*	*	*

NOTES
[1]Input Offset Voltage Drift is specified with the offset voltage unnulled. Nulling will induce an additional 3μV/°C/mV of offset nulled.
[2]Bias Current specifications are guaranteed maximum at either input at T_{CASE} = +25°C. For higher temperatures see Figure 16.
[3]Defined as the maximum safe voltage between inputs such that neither exceeds ±10V from ground.
[4]For outline information see Package Information section

*Specifications same as AD380JH.
**Specifications same as AD380KH.
Specifications subject to change without notice.

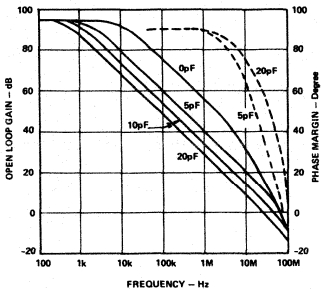


Figure 1. Open Loop Frequency Response

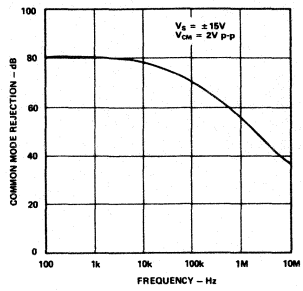


Figure 2. CMRR vs. Frequency

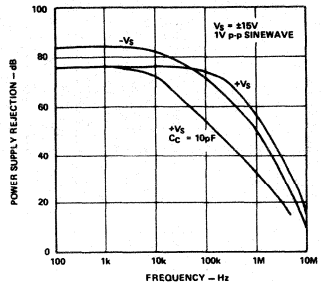


Figure 3. PSRR vs. Frequency

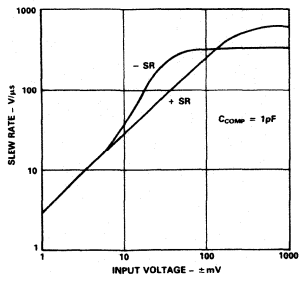


Figure 4. Slew Rate vs. Differential Input Voltage

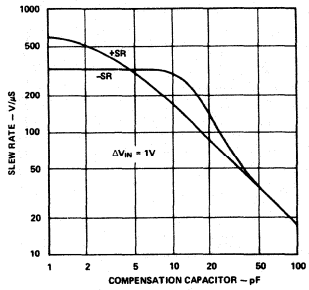


Figure 5. Slew Rate vs. Compensation Capacitor

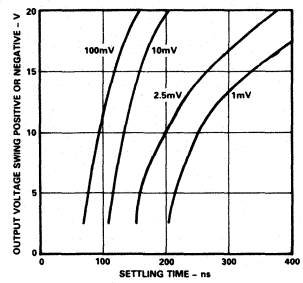


Figure 6. Output Settling Time vs. Output Voltage Swing and Error

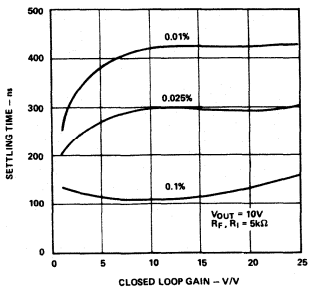


Figure 7. Settling Time vs. Closed Loop Gain

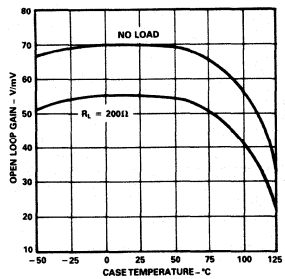


Figure 8. Gain vs. Temperature

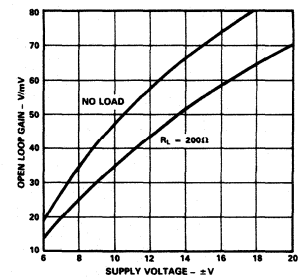


Figure 9. Gain vs. Supply Voltage

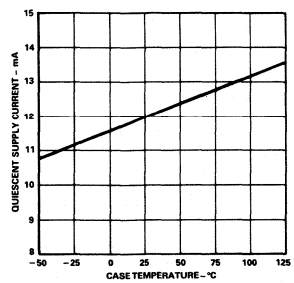


Figure 10. Supply Current vs. Temperature

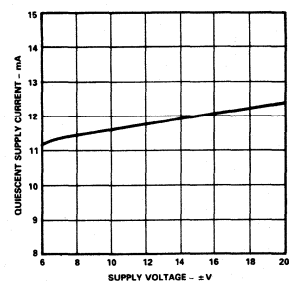


Figure 11. Supply Current vs. Supply Voltage

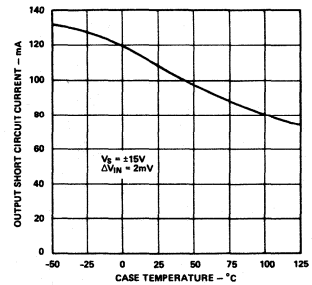


Figure 12. I_{SC} vs. Temperature

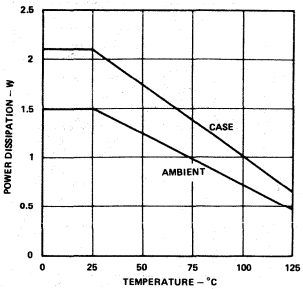


Figure 13. Power Dissipation vs. Temperature

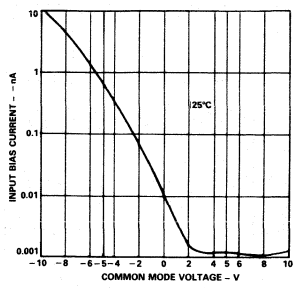


Figure 14. Input Bias Current vs. Common Mode Voltage

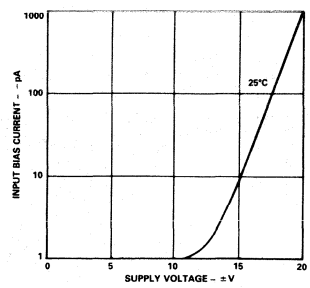


Figure 15. Input Bias Current vs. Supply Voltage

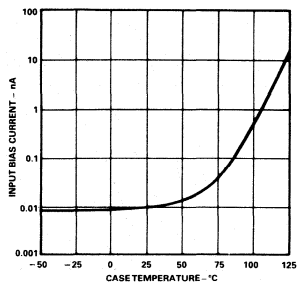


Figure 16. Input Bias Current vs. Temperature

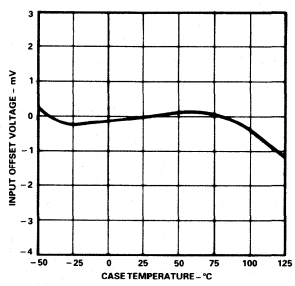


Figure 17. Offset Voltage vs. Temperature

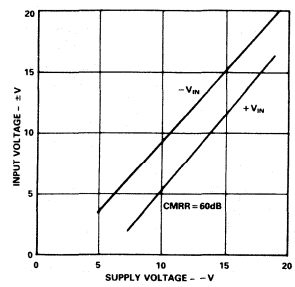


Figure 18. Input Voltage Range vs. Supply Voltage

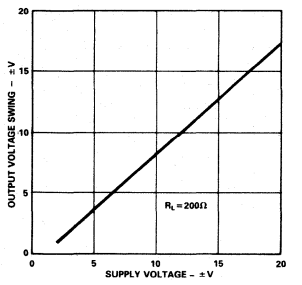


Figure 19. Output Voltage Swing vs. Supply Voltage

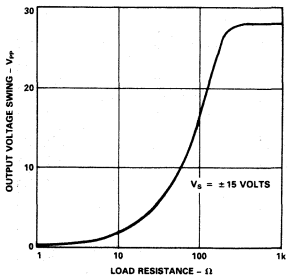


Figure 20. Output Voltage Swing vs. Load Resistance

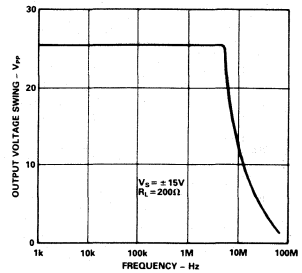


Figure 21. Large Signal Frequency Response

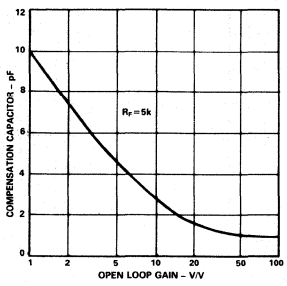


Figure 22. Recommended Compensation Capacitor vs. Closed Loop Gain

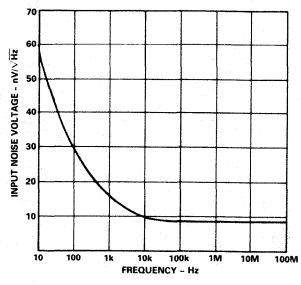


Figure 23. Input Noise Voltage Spectral Density

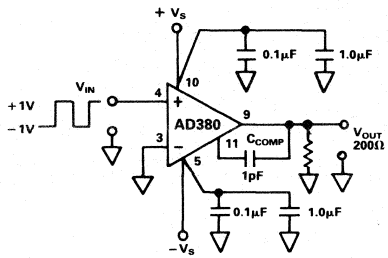


Figure 24a. Overdrive Recovery Test Circuit

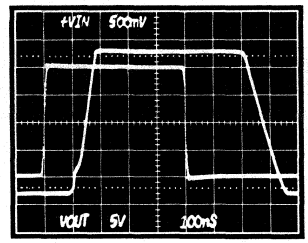


Figure 24b. Overdrive Recovery Response (Symmetrial 20ns Version Available)

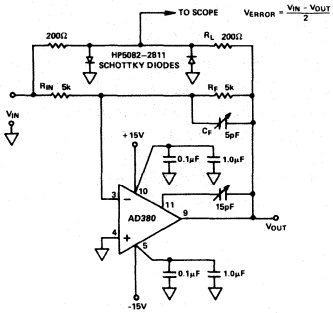


Figure 25a. Unity Gain Inverter Settling Time Test Circuit

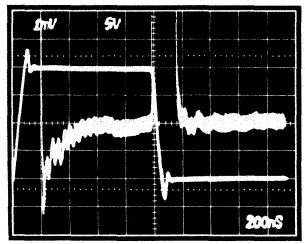


Figure 25b. Unity Gain Inverter Large Signal Response

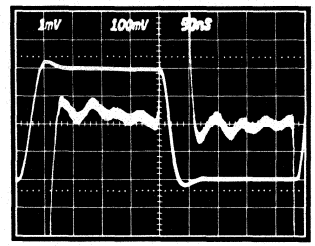


Figure 25c. Unity Gain Inverter Small Signal Response

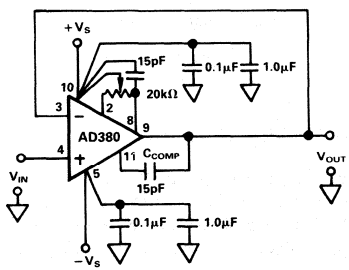


Figure 26a. Unity Gain Buffer Circuit

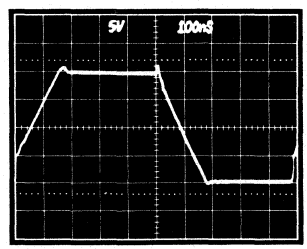


Figure 26b. Unity Gain Buffer Large Signal Response

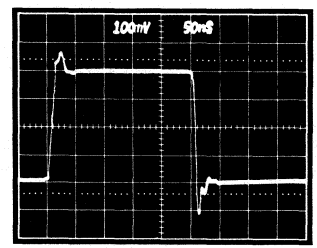


Figure 26c. Unity Gain Small Signal Response

APPLICATIONS INFORMATION

Compensation Capacitor

For low gain applications a 5pF to 27pF capacitor between the frequency compensation input (pin 11) and the output (pin 9) will reduce the risk of oscillation by adding phase margin. A compensation capacitor is especially needed when driving capacitive loads. For gains greater than 30 a 1pF compensation capacitor is recommended; see Figure 22.

For unity gain buffer applications it may be necessary to add a small (10pF to 20pF) capacitor between pins 8 and 10 for improved phase margin; see Figure 26a.

Offset Null

If the initial offset voltage is not low enough for the user's application offset nulling is required. To null the offset tie a 20kΩ potentiometer between the offset null pins (pins 2 and 8). The wiper of the potentiometer is tied to the positive supply. With the analog input signal to the circuit grounded, adjust the potentiometer for zero output.

To minimize the effects of offset voltage drift as a function of temperature, null the offset at the midpoint of the operating temperature range. For example, if the operating environment is 0°C to 70°C do the offset nulling at 35°C. This will insure a maximum offset voltage drift of 35 times the V_{OS} drift specification at either temperature extreme.

Typical Circuits

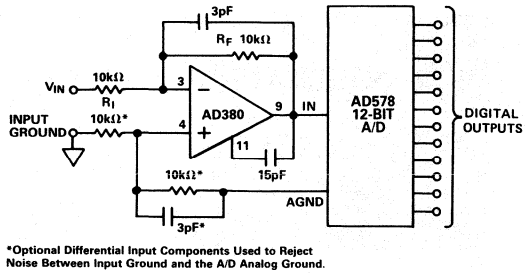


Figure 27. Fast-Settling Buffer

Its quick recovery from load variations makes the AD380 an excellent buffer for fast successive approximation A/D converters; see Figure 27.

Many high speed A/D converters require a wideband buffer that can hold a constant output voltage under dynamically-changing load conditions that fluctuate at the bit decision rate.

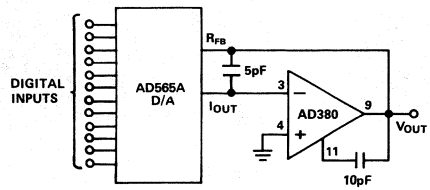


Figure 28. 12-Bit Voltage Output DAC Circuit Settles to 1/2LSB in 300ns

The AD565A 12-bit digital to analog converter with an AD380 output amplifier will give a voltage output that typically settles to within 1/2LSB in less than 300ns. Total settling time is the root mean square of the DAC current output settling time and the output amplifier settling time.

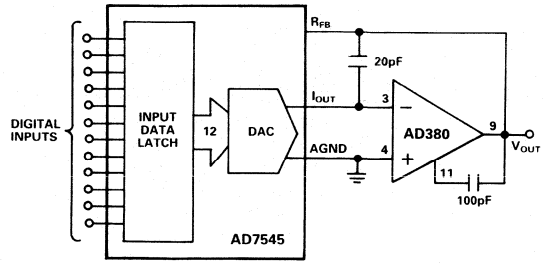


Figure 29. CMOS DAC Output Amplifier

CMOS DAC output amplifiers require low offset voltage op amps. The output impedance of CMOS DACs varies with input code. This can cause a code dependent error term at the output that approaches the op amps' offset voltage. If the DAC has a differential nonlinearity of 1/2LSB, it will require an output amplifier with less than 1/2LSB offset error to remain monotonic. An LSB for a 12-bit DAC such as the AD7545 is 2.44mV (10 volts full scale/4096). Thus, the AD380KH, with only 1mV offset maximum, will contribute less than 1/2LSB to differential linearity error.

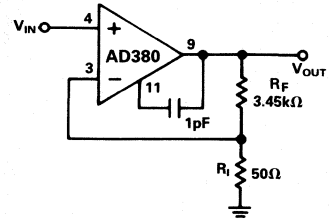


Figure 30. Video Amplifier

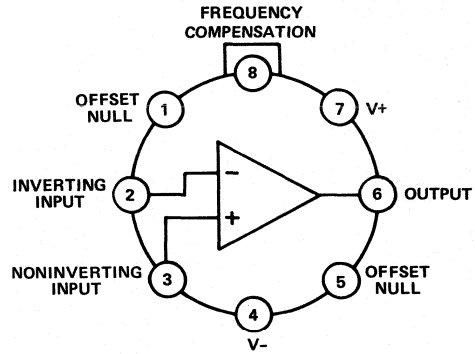
The high output current capability of the AD380 makes it suitable for video speed driver applications. In the circuit above the closed loop gain of 70 (37dB) is available over a bandwidth of 5MHz. Note that a 1pF compensation capacitor is required in this high gain application.

IC, Wideband, Fast Slewing, General Purpose Operational Amplifier

AD507

FEATURES
Gain Bandwidth: 100MHz
Slew Rate: 20V/μs min
I_B: 15nA max (AD507K)
V_{os}: 3mV max (AD507K)
V_{os} Drift: 15μV/°C max (AD507K)
High Capacitive Drive

CONNECTION DIAGRAM



PRODUCT DESCRIPTION

The Analog Devices AD507J, K and S are low cost monolithic operational amplifiers that are designed for general purpose applications where high gain bandwidth and high speed are significant requirements. The devices also provide excellent dc performance with low input offset voltage, low offset voltage drift and low bias current. The AD507 is a low cost, high performance alternative to a wide variety of modular and IC op amps; a brief review of the specifications confirms its outstanding price/performance characteristics.

The AD507 is recommended for use where low cost and all around performance, especially at high frequencies, are needed. It is particularly well suited as a fast, high impedance comparator, integrator or wideband amplifier and in sample/hold circuits. It is unconditionally stable for all closed loop gains above 10 without external compensation; the frequency compensation terminal is used for stability at lower closed loop gains. The circuit is short circuit protected and offset voltage nullable. The AD507J and K are specified over the 0 to +70°C temperature range, the AD507S over the extended temperature range, -55°C to +125°C. All devices are packaged in the hermetic TO-99 metal can.

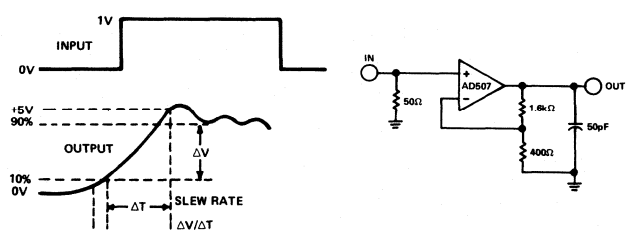
PRODUCT HIGHLIGHTS

1. Excellent dc and ac performance combined with low cost.
2. The AD507 will drive several hundred pF of output capacitance without oscillation.
3. All guaranteed dc parameters, including offset voltage drift, are 100% tested.
4. To insure compliance with gain bandwidth and slew rate specifications, all devices are tested for ac performance characteristics.

AD507—SPECIFICATIONS (typical @ +25°C and ±15V dc, unless otherwise specified)

PARAMETER	AD507J	AD507K	AD507S
OPEN LOOP GAIN			
R_L = 2kΩ, C_L = 50pF	80,000 min (150,000 typ)	100,000 min (150,000 typ)	100,000 min (150,000 typ)
@ T_{min} to T_{max}	70,000 min	85,000 min	70,000 min
OUTPUT CHARACTERISTICS			
Voltage @ R_L = 2kΩ, C_L = 50pF, T_{min} to T_{max}	±10V min (±12V typ)	*	±10V min (±12V typ)
Current @ V_o = ±10V	±10mA min (±20mA typ)	*	±15mA min (±22mA typ)
Short Circuit Current	25mA	*	25mA
FREQUENCY RESPONSE			
Unity Gain, Small Signal			
@ A = 1 (open loop)	35MHz	*	*
@ A = 100 (closed loop)	1MHz	*	*
Full Power Response	320kHz min (600kHz typ)	400kHz min (600kHz typ)	400kHz min (600kHz typ)
Slew Rate	±20V/μs min (±35V/μs typ)	±25V/μs min (±35V/μs typ)	20V/μs min (±35V/μs typ)
Settling Time (to 0.1%)	900ns	*	*
INPUT OFFSET VOLTAGE			
Initial	5.0mV max (3.0mV typ)	3.0mV max (1.5mV typ)	4mV max (0.5mV typ)
Avg vs Temp, T_{min} to T_{max}	15μV/°C	15μV/°C max (8μV/°C typ)	20μV/°C max (8μV/°C typ)
vs Supply, T_{min} to T_{max}	200μV/V max	100μV/V max	100μV/V max
INPUT BIAS CURRENT			
Initial	25nA max	15nA max	15nA max
T_{min} to T_{max}	40nA max	25nA max	35nA max
INPUT OFFSET CURRENT			
Initial	25nA max	15nA max	15nA max
T_{min} to T_{max}	40nA max	25nA max	35nA max
Avg vs Temp, T_{min} to T_{max}	0.5nA/°C	0.2nA/°C	0.2nA/°C
INPUT IMPEDANCE			
Differential	40MΩ min (300MΩ typ)	*	65MΩ min (500MΩ typ)
Common Mode	1000MΩ	*	*
INPUT VOLTAGE NOISE			
f = 10Hz	100nV/$\sqrt{Hz}$	*	*
f = 100Hz	30nV/$\sqrt{Hz}$	*	*
f = 100kHz	12nV/$\sqrt{Hz}$	*	*
INPUT VOLTAGE RANGE			
Differential, Max Safe	±12.0V	*	*
Common Mode Voltage Range, T_{min} to T_{max}	±11.0V	*	*
Common Mode Rejection @ ±5V, T_{min} to T_{max}	74dB min (100dB typ)	80dB min (100dB typ)	80dB min (100dB typ)
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 20)V	*	*
Current, Quiescent	4.0mA max (3.0mA typ)	*	*
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	−55°C to +125°C
Operating	−25°C to +85°C	*	−65°C to +150°C
Storage	−65°C to +150°C	*	*
PACKAGE OPTION[1]			
H-08A	AD507JH	AD507KH	AD507SH

NOTES
[1]For outline information see Package Information section.
*Specifications same as AD507J.
**AD507S/883 minimum order 10 pieces.



Slew Rate Definition and Test Circuit

APPLICATION CONSIDERATIONS

The AD507 combines excellent dc characteristics and dynamic performance with ease of application. Because it is a wideband, high speed amplifier, care should be exercised in its stabilization. Several practical stabilization techniques are suggested to insure proper operation and minimize user experimentation.

GENERAL PURPOSE WIDEBAND COMPENSATION

The following considerations are intended to provide guidance in critical wideband applications. While not necessary in all cases, the considerations are of prime importance for the user attempting to obtain the highest performance from his circuit design.

High Gain Conditions

The AD507 is fully compensated *internally* for all closed loop gains above 10; however, it is necessary to load the amplifier with 50pF. In many applications this minimum capacitive load will be provided by the load or by a cable at the output of the AD507, making an additional 50pF unnecessary. Figure 1 shows the suggested configuration for general purpose use for closed loop gains above 10.

The 0.1μF ceramic power supply bypass capacitors are considerably more important for the AD507 than for low frequency general purpose amplifiers. Their main purpose is to convert the distributed high frequency ground to a lumped single point (the V+ point). The V+ to V− 0.1μF capacitor equalizes the supply grounds while the 0.1μF capacitor from V+ to signal ground should be returned to signal common. The signal common, which is bypassed to pin 7, is defined as that point at which the input signal source, the feedback network, and the return side of the load are joined to the power common.

Note that the diagrams show each individual capacitor directly connected to the appropriate terminal (pin 7 [V+] and pin 6 [Output]). In addition, it is suggested that all connections be made short and direct, and as physically close to the can as possible, so that the length of any conducting path shared by external components will be minimized.

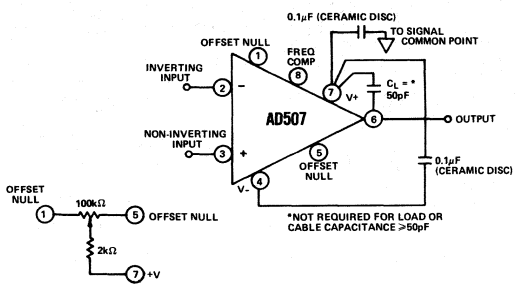


Figure 1. General Purpose Configuration to Closed Loop Gain > 10

Low Gain Conditions

For low closed loop gain applications, the AD507 should be compensated with a 20pF capacitor from pin 8 (frequency compensation) to signal common or pin 7 (V+). This configuration also requires a 30pF feedback capacitor from pin 6 (Output) to pin 8 (see Figure 2). The 50pF minimum load capacitance recommended for uncompensated applications is not required when the AD507 is used in the compensated mode. This compensation results in a unity gain frequency of approximately 10 to 12MHz.

The excellent input characterisitcs of the AD507 make it useful in low frequency applications where both dc and ac performance superior to the 741 type of op amp is desired. Some experimentation may be necessary to optimize the AD507 for the specific requirement. The unity gain bandwidth can be reduced by increasing the value of the compensation capacitor in inverse proportion to the desired bandwidth reduction. It is advisable to increase the feedback capacitor at the same time, maintaining its value about 50% larger than the compensation capacitor. Because the AD507 is fundamentally a wideband amplifier, careful power supply decoupling and compensation component layout are required even in low bandwidth applications.

OFFSET VOLTAGE NULLING

Note that the offset voltage null circuit includes a 2kΩ resistor in series with the wiper arm of the 100kΩ potentiometer. This resistor is not absolutely required, but its use can prevent a condition of false null that can be obtained at the ends of the pot range. The knowledgeable user should have no trouble differentiating between nulling in the pot mid-range and erratic end-range behavior when the wiper is connected directly to V+.

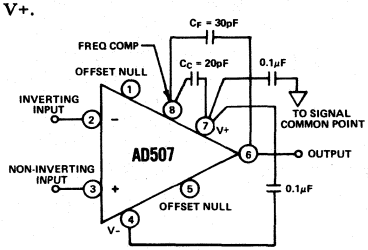


Figure 2. Configuration for Unity Gain Applications

HIGH CAPACITIVE LOADING

Like all wideband amplifiers, the AD507 is sensitive to capacitive loading. Unlike many, however, the AD507 can be used to effectively drive reasonable capacitive loads in virtually all applications, and capacitive loads of several hundred picofarads in a number of specific configurations.

In an inverting gain of ten configuration, the internally compensated amplifier will drive more than 200pF in addition to the recommended 50pF load, or a total of over 250pF. Under such conditions, the slew rate will be only slightly reduced, and the overall settling time somewhat lengthened.

In general, the capacitive drive capability of the AD507 will increase in high gain configurations which reduce closed loop bandwidth.

In any wideband application, it is essential to return the load currents supplied by the amplifier to the power supply without sharing a path with input or feedback signals. This consideration becomes particularly important when driving capacitive loads which may resonate with short lengths of interconnecting wire.

FAST SETTLING TIME

A small capacitor (C_S in Figure 3) will improve the settling time of the AD507, when it is used with large feedback resistors. The AD507 input capacitance (typically 2 or 3pF), together with additional circuit capacitance, will introduce an unwanted pole of open-loop response. The extra phase shift introduced, for example, by 4pF of input capacitance, and

5kΩ input source impedance, will result in an underdamped transient response, and long settling time. A small (1.5 to 3.0pF) feedback capacitor will introduce a zero in the open-loop transfer function, reducing the phase shift and increasing the damping, which will more than compensate for the slight reduction in closed-loop bandwidth.

BIAS COMPENSATION NOT REQUIRED

Circuit applications using conventional op amps generally require that the source resistances be matched at the inputs to cancel the effects of the input currents and take advantage of low offset current. In circuits similar to that shown in Figure 3, the compensation resistance would be equal to the parallel combination of R_I and R_F, and for large values would require a bypass capacitor. The AD507 is specially designed to cancel the input currents so as to reduce them to the offset current level. As a result, optimum performance can be obtained even though no bias compensation is used, and the non-inverting input can be connected directly to the signal common.

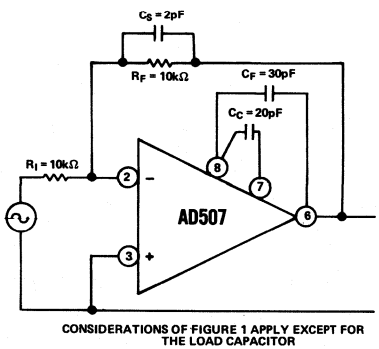
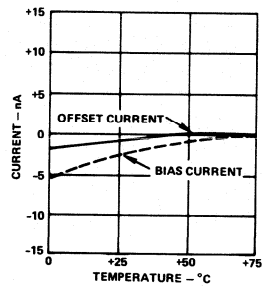
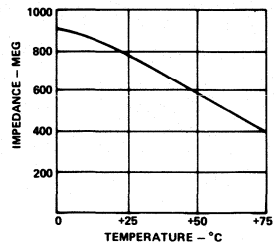


Figure 3. Fast Settling Time Configuration

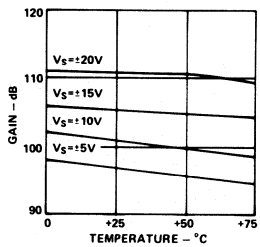
TYPICAL PERFORMANCE CURVES



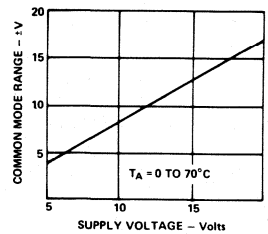
Input Bias Current and Offset Current vs Temperature



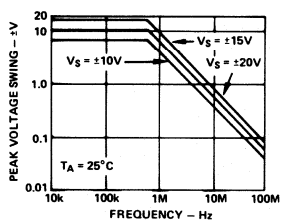
Input Impedance vs Temperature



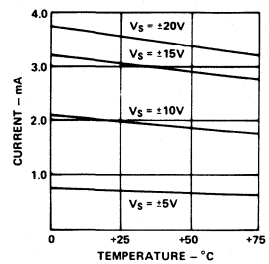
Open Loop Voltage Gain vs Temperature



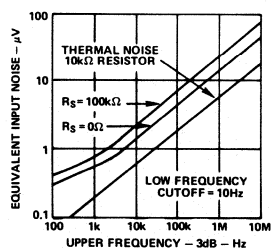
Common Mode Voltage Range vs Supply Voltage



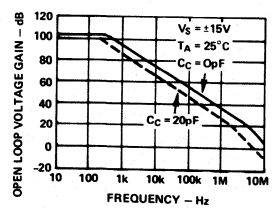
Output Voltage Swing vs Frequency



Power Supply Current vs Temperature



Broadband Input Noise Characteristics



Open Loop Gain vs Frequency

ANALOG DEVICES

High Speed, Fast Settling IC Op Amp

AD509

FEATURES

- Fast Settling Time
  - 0.1% in 500ns max
  - 0.01% in 2.5μs max
- High Slew Rate: 100V/μs min
- Low I_{OS}: 25nA max
- Guaranteed V_{OS} Drift: 30μV/°C max
- High CMRR: 80dB min
- Drives 500pF
- Low Price

APPLICATIONS

- D/A and A/D Conversion
- Wideband Amplifiers
- Multiplexers
- Pulse Amplifiers

PRODUCT DESCRIPTION

The AD509J, AD509K and AD509S are monolithic operational amplifiers specifically designed for applications requiring fast settling times to high accuracy. Other comparable dynamic parameters include a small signal bandwidth of 20MHz, slew rate of 100V/μs min and a full power response of 150kHz min. The devices are internally compensated for all closed loop gains greater than 3, and are compensated with a single capacitor for lower gains.

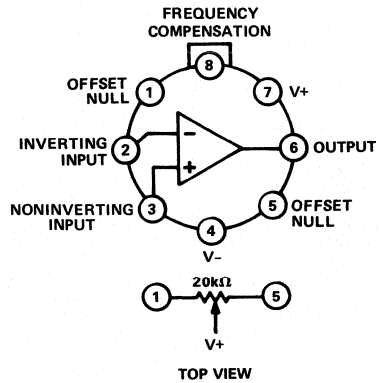
The input characteristics of the AD509 are consistent with 0.01% accuracy over limited temperature ranges; offset current is 25nA max, offset voltage is 8mV max, nullable to zero, and offset voltage drift is limited to 30μV/°C max. PSRR and CMRR are typically 90dB.

The AD509 is designed for use with high speed D/A or A/D converters where the minimum conversion time is limited by the amplifier settling time. If 0.01% accuracy of conversion is required, a conversion cannot be made in a shorter period than the time required for the amplifier to settle to within 0.01% of its final value.

All devices are supplied in the TO-99 package. The AD509J and AD509K are specified for 0 to +70°C temperature range; the AD509S for operation from −55°C to +125°C.

PIN CONFIGURATION

TO-99



TOP VIEW

PRODUCT HIGHLIGHTS

1. The AD509 is internally compensated for all closed loop gains above 3, and compensated with a single capacitor for lower gains thus eliminating the elaborate stabilizing techniques required by other high speed IC op amps.
2. The AD509 will drive capacitive loads of 500pF without deterioration in settling time. Larger capacitive loads can be driven by tailoring the compensation to minimize settling time.
3. Common Mode Rejection, Gain and Noise are compatible with a 0.01% accuracy device.
4. The AD509K and AD509S are 100% tested for minimum slew rate and guaranteed to settle to 0.01% of its final value in less than 2.5μs.

AD509—SPECIFICATIONS (@ ±25°C and V_S = ±15V dc unless otherwise specified)

Model	AD509J Min	AD509J Typ	AD509J Max	AD509K Min	AD509K Typ	AD509K Max	AD509S Min	AD509S Typ	AD509S Max	Units
OPEN LOOP GAIN										
V_O = ±10V, $R_L \geq 2k\Omega$	**7,500**	15,000		**10,000**	15,000		**10,000**	15,000		V/V
T_{min} to T_{max}, R_L = 2kΩ	5,000			7,500			**7,500**			V/V
OUTPUT CHARACTERISTICS										
Voltage @ R_L = 2kΩ, T_{min} to T_{max}	**±10**	±12		**±10**	±12		**±10**	±12		V
FREQUENCY RESPONSE										
Unity Gain Small Signal		20			20			20		MHz
Full Power Response	1.2	1.6		1.5	2.0		1.5	2.0		MHz
Slew Rate, Unity Gain	80	120		80	120		100	120		V/μs
Settling Time										
to 0.1%		200			200			200	500	ms
to 0.01%		1.0			1.0			1.0	2.5	μs
INPUT OFFSET VOLTAGE										
Initial Offset		5	**10**		4	**8**		4	**8**	mV
Input Offset Voltage T_{min} to T_{max}			14			11			**11**	mV
Input Offset Voltage vs. Supply, T_{min} to T_{max}			**200**			**100**			**100**	μV/V
INPUT BIAS CURRENT										
Initial		125	**250**		100	**200**		100	**200**	nA
T_{min} to T_{max}			500			400			**400**	nA
INPUT OFFSET CURRENT										
Initial		20	50		10	25		10	25	nA
T_A = min to max			100			50			50	nA
INPUT IMPEDANCE										
Differential	40	100		50	100		50	100		MΩ
INPUT VOLTAGE RANGE										
Differential		±15			±15			±15		V
Common Mode		±10			±10			±10		V
Common Mode Rejection	**74**	90		**80**	90		**80**	90		dB
INPUT NOISE VOLTAGE										
f = 10Hz		100			100			100		nV/√Hz
f = 100Hz		30			30			30		nV/√Hz
f = 100kHz		19			19			19		nV/√Hz
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating	±5		±20	±5		±20	±5		±20	V
Quiescent Current		4	**6**		4	**6**		4	**6**	mA
TEMPERATURE RANGE										
Operating, Rated Performance	0		+70	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	°C

NOTES
Specifications subject to change without notice.
All min and max specifications are guaranteed.
Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD509JH	0°C to +70°C	H-08A
AD509KH	0°C to +70°C	H-08A
AD509SH	−55°C to +125°C	H-08A

*H-08A = TO-99 Style Metal Can. For outline information see Package Information section.

APPLYING THE AD509

MEASURING SETTLING TIME. Settling time is defined as that period required for an amplifier output to swing from 0 volts to full scale, usually 10 volts, and to settle to within a specified percentage of the final output voltage. For high accuracy systems, the accuracy requirement is normally specified as either 0.1% (10-bit accuracy) or 0.01% (12-bit accuracy) of the 10 volt output level. The settling time period is comprised of an initial propagation delay, an additional time for the amplifier to slew to the vicinity of 10 volts, and a final time period to recover from internal saturation and other effects, and settle within the specified error band. Because settling time depends on both linear and nonlinear factors, there is no simple approach to predicting its final value to different levels of accuracy. In particular, extremely high slew rates do not assure a rapid settling time, since this is only one of many factors affecting settling time. In most high speed amplifiers, after the amplifier has slewed to the vicinity of the final output voltage, it must recover from internal saturation and then allow any overshoot and ringing to damp out. These definitions are illustrated in Figure 1.

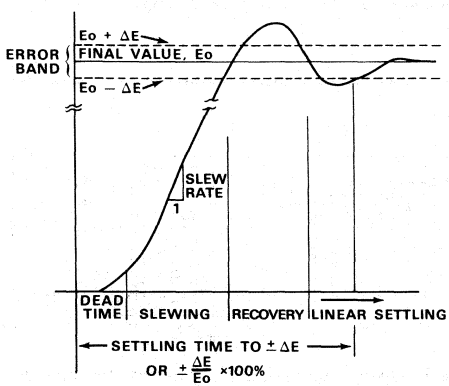


Figure 1. Settling Time

The AD509K and AD509S are guaranteed to settle to 0.1% in 500ns and 0.01% in 2.5μs when tested as shown in Figure 2. There is no appreciable degradation in settling time when the capacitive load is increased to 500pF, as discussed below. The settling time is computed by summing the output and the input into a differential amplifier, which then drives a scope display. The resultant waveform of ($E_O - E_{IN}$) of a typical AD509 is shown in Figure 3. Note that the waveform crosses the 1mV point representing 0.01% accuracy in approximately 1.5μs. The top trace represents the output signal; the bottom trace represents the error signal.

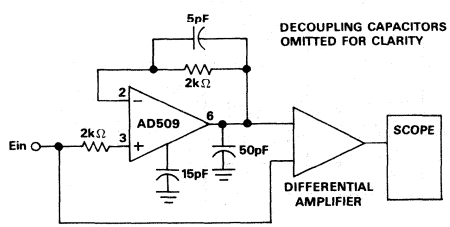


Figure 2. AD509 Settling Time Test Circuit

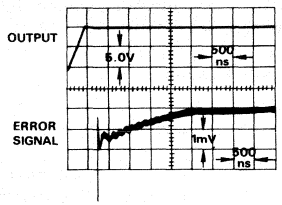


Figure 3. Settling Time of AD509

SETTLING TIME VS. R_f AND R_i. Settling time of an amplifier is a function of the feedback and input resistors, since they interact with the input capacitance of the amplifier. When operating in the non-inverting mode, the source impedance should be kept relatively low; e.g., 5kΩ; in order to insure optimum performance. The small feedback capacitor (5pF) is used in the settling time test circuit in parallel with the feedback resistor to reduce ringing. This capacitor partially cancels the pole formed in the loop gain response as a result of the feedback and input resistors, and the input capacitance.

SETTLING TIME VS. CAPACITIVE LOAD. The AD509 will drive capacitive loads of 500pF without appreciable deterioration in settling time. Larger capacitive loads can be driven by tailoring the compensation to minimize settling time. Figure 4 shows the settling time of a typical AD509, compensated for unity gain with a 15pF capacitor, with a 500pF capacitive load on the output. Note that settling time to 0.01% is still under 2.0μs.

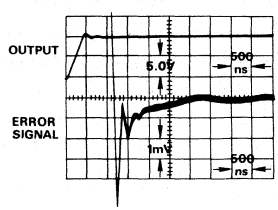


Figure 4. AD509 with 500pF Capacitive Load

SUGGESTIONS FOR MINIMIZING SETTLING TIME. The AD509 has been designed to settle to 0.01% accuracy in 1 to 2.5μs. However, this amplifier is only a building block in a circuit that also has a feedback network, input and output connections, power supply connections, and a number of external components. What has been painstakingly gained in amplifier design can be lost without careful circuit design. Some of the elements of a good high speed design are.....

CONNECTIONS. It is essential that care be taken in the signal and power ground circuits to avoid inducing or generating extraneous voltages in the ground signal paths.

The 0.1μF ceramic power supply bypass capacitors are considerably more important for the AD509 than for low frequency general purpose amplifiers. Their main purpose is to convert the distributed high frequency ground to a lumped single point (the V+ point). The V+ to V− 0.1μF capacitor equalizes the supply grounds while the 0.1μF capacitor from V+ to signal ground should be returned to signal common. The signal common, which is bypassed to pin 7, is defined as that point at which the input signal source, the feedback network, and the return side of the load are joined to the power common.

Note that the diagram shows each individual capacitor directly connected to the appropriate terminal (pin 7 [V+]).

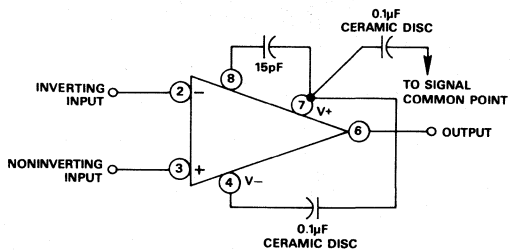


Figure 5. Configuration for Unity Gain Applications

In addition, it is suggested that all connections be short and direct, and as physically close to the case as possible, so that the length of any conducting path shared by external components will be minimized.

COMPONENTS. Resistors are preferably metal film types, because they have less capacitance and stray inductance than wirewound types, and are available with excellent accuracies and temperature coefficients.

Diodes are hot carrier types for the very fastest-settling applications, but 1N914 types are suitable for more routine uses.

Capacitors in critical locations are polystyrene, teflon, or polycarbonate to minimize dielectric absorption.

CIRCUIT. For the fastest settling times, keep leads short, orient components to minimize stray capacitance, keep circuit impedance levels as low as consistent with the output capabilities of the amplifier and the signal source, reduce all external load capacitances to the absolute minimum. Don't overlook sockets or printed circuit board mounting as possible sources of dielectric absorption. Avoid pole-zero mismatches in any feedback networks used with the amplifier. Minimize noise pickup.

DYNAMIC RESPONSE OF AD509

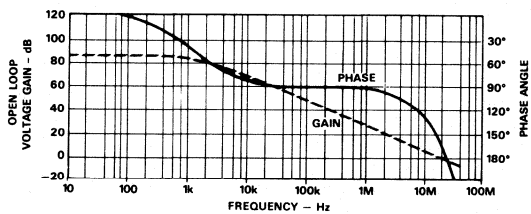


Figure 6. Open Loop Frequency and Phase Response

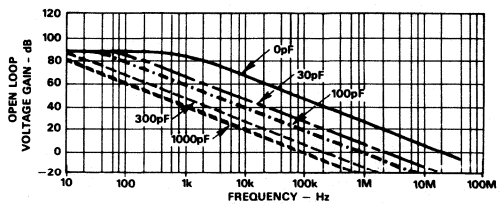


Figure 7. Open Loop Frequency Response for Various C_C's

THE AD509 AS AN OUTPUT AMPLIFIER FOR FAST CURRENT-OUTPUT D-TO-A CONVERTERS

Most fast integrated circuit digital to analog converters have current outputs. That is, the digital input code is translated to an output current proportional to the digital code. In many applications, that output current is converted to a voltage by connecting an operational amplifier in the current-to-voltage conversion mode.

The settling time of the combination depends on the settling time of the DAC and the output amplifier. A good approximation is:

$$t_s \text{ TOTAL} = \sqrt{(t_s \text{ DAC})^2 + (t_s \text{ AMP})^2}$$

Some IC DACs settle to final output value in 100-500 nanoseconds. Since most IC op amps require a longer time to settle to ±0.1% or ±0.01% of final value, amplifier settling time can dominate total settling time. And for a 12-bit DAC, one least significant bit is only 0.024% of full-scale, so low drift and high linearity and precision are also required of the output amplifier.

Figure 8 shows the AD509K connected as an output amplifier with the AD565K, high speed 12-bit IC digital-to-analog converter. The 10 picofarad capacitor, C1, compensates for the 25pF AD565 output capacitance. The voltage output of the AD565K/AD509K combination settles to ±0.01% in one microsecond. The low input voltage drift and high open loop gain of the AD509K assures 12-bit accuracy over the operating temperature range.

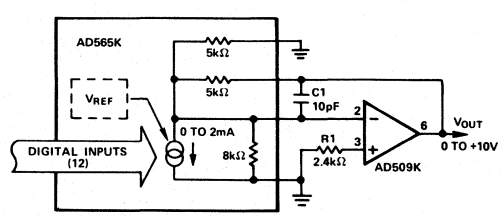


Figure 8. AD509 as an Output Amplifier for a Fast Current-Output D-to-A Converter

ANALOG DEVICES

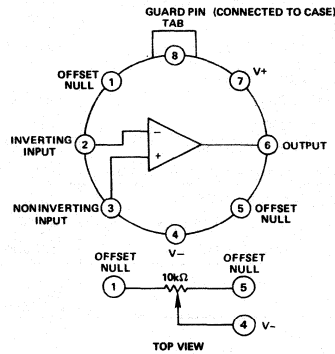
Monolithic Precision, Low Power FET-Input Electrometer Op Amp

AD515A*

FEATURES

Ultralow Bias Current: 75fA max (AD515AL)
150fA max (AD515AK)
300fA max (AD515AJ)
Low Power: 1.5mA max Quiescent Current
(0.6mA typ)
Low Offset Voltage: 1.0mV max (AD515AK & L)
Low Drift: 15μV/°C max (AD515AK)
Low Noise: 4μV p-p, 0.1Hz to 10Hz

PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD515A is a monolithic FET-input operational amplifier with a guaranteed maximum input bias current of 75fA (AD515AL). The AD515A is a monolithic successor to the industry standard AD515 electrometer, and will replace the AD515 in most aplications. The AD515A also delivers laser-trimmed offset voltage, low drift, low noise and low power, a combination of features not previously available in ultralow bias current circuits. All devices are internally compensated, protected against latch-up and are short circuit protected.

The AD515A's combination of low input bias current, low offset voltage and low drift optimizes it for a wide variety of electrometer and very high impedance buffer applications including photo-current detection, vacuum ion-gage measurement, long-term precision integration and low drift sample/hold applications. This amplifier is also an excellent choice for all forms of biomedical instrumentation such as pH/pIon sensitive electrodes, very low current oxygen sensors, and high impedance biological microprobes. In addition, the low cost and pin compatibility of the AD515A with standard FET op amps will allow designers to upgrade the performance of present systems at little or no additional cost. The $10^{15}\Omega$ common-mode input impedance ensures that the input bias current is essentially independent of common-mode voltage.

As with previous electrometer amplifier designs from Analog Devices, the case is brought out to its own connection (Pin 8) so that the case can be independently connected to a point at the same potential as the input, thus minimizing stray leakage to the case. This feature will also shield the input circuitry from external noise and supply transients.

The AD515A is available in three versions of bias current and offset voltage, the "J", "K" and "L"; all are specified for rated performance from 0 to +70°C and supplied in a hermetically sealed TO-99 package.

***Covered by Patent No. 4,639,683.**

PRODUCT HIGHLIGHTS

1. The AD515A provides subpicoampere bias currents in an integrated circuit amplifier.
   - The ultralow input bias currents are specified as the maximum measured at either input with the device fully warmed up on ±15V supplies at +25°C ambient with no heat sink. This parameter is 100% tested.
   - By using ±5V supplies, input bias current can typically be brought below 50fA.
2. The input offset voltage on all grades is laser trimmed, typically less than 500μV.
   - The offset voltage drift is 15μV/°C maximum on the K grade.
   - If additional nulling is desired, the amount required will have a minimal effect on offset drift (approximately 3μV/°C per mV).
3. The low quiescent current drain of 0.6mA typical and 1.5mA maximum, keeps self-heating effects to a minimum and renders the AD515A suitable for a wide range of remote probe applications.
4. The combination of low input noise voltage and very low input noise current is such that for source impedances from 1MΩ to $10^{11}\Omega$, the Johnson noise of the source will easily dominate the noise characteristic.

AD515A—SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc, unless otherwise specified)

Model	AD515AJ	AD515AK	AD515AL
OPEN-LOOP GAIN[1]			
V_{OUT} = ±10V, $R_L \geq 2k\Omega$	**20,000V/V min**	**40,000V/V min**	**25,000V/V min**
$R_L \geq 10k\Omega$	**40,000V/V min**	**100,000V/V min**	**50,000V/V min**
T_A = min to max $R_L \geq 2k\Omega$	**15,000V/V min**	**40,000V/V min**	**25,000V/V min**
OUTPUT CHARACTERISTICS			
Voltage@R_L = 2kΩ, T_A = min to max	**±10V min (±12V typ)**	*	*
@R_L = 10kΩ, T_A = min to max	**±12V min (±13V typ)**	*	*
Load Capacitance[2]	1000pF		
Short-Circuit Current	**10mA min (20mA typ)**		
FREQUENCY RESPONSE			
Unity Gain, Small Signal	1MHz	*	*
Full Power Response	5kHz min (50kHz typ)	*	*
Slew Rate Inverting Unity Gain	0.3V/μs min (3.0V/μs typ)	*	*
Overload Recovery Inverting Unity Gain	100μs max (2μs typ)	*	*
INPUT OFFSET VOLTAGE[3]	**3.0mV max (0.4mV typ)**	**1.0mV max (0.4mV typ)**	**1.0mV max (0.4mV typ)**
vs. Temperature, T_A = min to max	**50μV/°C max**	**15μV/°C max**	**25μV/°C max**
vs. Supply, T_A = min to max	**400μV/V max (50μV/V typ)**	**100μV/V max**	**200μV/V max**
INPUT BIAS CURRENT			
Either Input[4]	**300fA max**	**150fA max**	**75fA max**
INPUT IMPEDANCE			
Differential V_{DIFF} = ±1V	1.6pF‖$10^{13}\Omega$	*	*
Common Mode	0.8pF‖$10^{15}\Omega$	*	*
INPUT NOISE			
Voltage, 0.1Hz to 10Hz	4.0μV (p-p)	*	*
f = 10Hz	75nV/$\sqrt{Hz}$	*	*
f = 100Hz	55nV/$\sqrt{Hz}$	*	*
f = 1kHz	50nV/$\sqrt{Hz}$	*	*
Current, 0.1Hz to 10Hz	0.007pA (p-p)	*	*
10Hz to 10kHz	0.01pA rms	*	*
INPUT VOLTAGE RANGE			
Differential	**±20V min**	*	*
Common Mode, T_A = min to max	**±10V min (+12V, −11 typ)**	*	*
Common-Mode Rejection, V_{IN} = ±10V	**66dB min (94dB typ)**	**80dB min**	**70dB min**
Maximum Safe Input Voltage[5]	±V_S	*	*
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	**±5V min (±18V max)**	*	*
Quiescent Current	**1.5mA max (0.6mA typ)**	*	*
TEMPERATURE			
Operating, Rated Performance	0 to +70°C	*	*
Storage	−65°C to +150°C	*	*
PACKAGE OPTION			
TO-99 (H-08A)	AD515AJH	AD515AKH	AD515ALH

NOTES
*Specifications same as AD515AJ.
[1]Open Loop Gain is specified with or without nulling of V_{OS}.
[2]A conservative design would not exceed 750pF of load capacitance.
[3]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[4]Bias Current specifications are guaranteed after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every +10°C.
[5]If it is possible for the input voltage to exceed the supply voltage, a series protection resistor should be added to limit input current to 0.1mA. The input devices can handle overload currents of 0.1mA indefinitely without damage. See next page.
[6]For outline information see Package Information section.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final test.

ESD PRECAUTIONS

Charges as high as 4000V readily accumulate on the human body and test equipment and discharge without detection. Therefore, reasonable ESD precautions are recommended to avoid functional damage or performance degradation. Unused devices should be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' ESD Prevention Manual.

LAYOUT AND CONNECTIONS CONSIDERATIONS

The design of very high impedance measurement systems introduces a new level of problems associated with the reduction of leakage paths and noise pickup.

1. A primary consideration in high impedance system designs is to attempt to place the measuring device as near to the signal source as possible. This will minimize current leakage paths, noise pickup and capacitive loading. The AD515A, with its combination of low offset voltage (normally eliminating the need for trimming), low quiescent current (minimal source heating, possible battery operation), internal compensation and small physical size lends itself very nicely to installation at the signal source or inside a probe. Also, as a result of the high load capacitance rating, the AD515A can comfortably drive a long signal cable.
2. The use of guarding techniques is essential to realizing the capability of the ultralow input currents of the AD515A. Guarding is achieved by applying a low impedance bootstrap potential to the outside of the insulation material surrounding the high impedance signal line. This bootstrap potential is held at the same level as that of the high impedance line; therefore, there is no voltage drop across the insulation and, hence, no leakage. The guard will also act as a shield to reduce noise pickup and serves an additional function of reducing the effective capacitance to the input line. The case of the AD515A is brought out separately to Pin 8 so that the case can also be connected to the guard potential. This technique virtually eliminates potential leakage paths across the package insulation, provides a noise shield for the sensitive circuitry and reduces common-mode input capacitance to about 0.8pF. Figure 1 shows a proper printed circuit board layout for input guarding and connecting the case guard. Figures 2 and 3 show guarding connections for typical inverting and noninverting applications. If Pin 8 is not used for guarding, it should be connected to ground or a power supply to reduce noise.

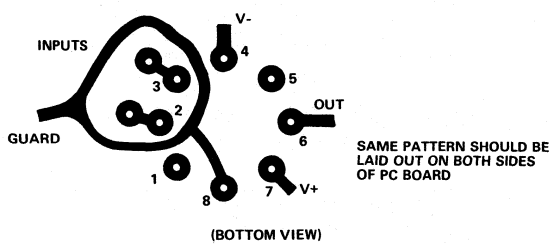


Figure 1. Board Layout for Guarding Inputs with Guarded TO-99 Package

3. Printed circuit board layout and construction is critical for achieving the ultimate in low leakage performance that the AD515A can deliver. The best performance will be realized by using a teflon IC socket for the AD515A; but at least a teflon stand-off should be used for the high impedance lead. If this is not feasible, the input guarding scheme shown in Figure 1 will minimize leakage as much as possible; the guard ring should be applied to both sides of the board. The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on a printed circuit; to minimize noise and leakage, they must be carried in rigid, shielded cables.
4. Another important concern for achieving and maintaining low leakage currents is complete cleanliness of circuit boards and components. Completed assemblies should be washed thoroughly in a low residue solvent such as TMC Freon or high-purity methanol followed by a rinse with deionized water and nitrogen drying. If service is anticipated in a high contaminant or high humidity environment, a high dielectric conformal coating is recommended. All insulation materials except Kel-F or teflon will show rapid degradation of surface leakage at high humidities.

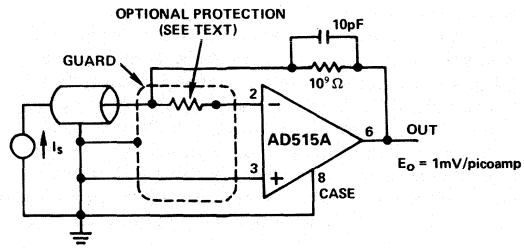


Figure 2. Picoampere Current-to-Voltage Converter Inverting Configuration

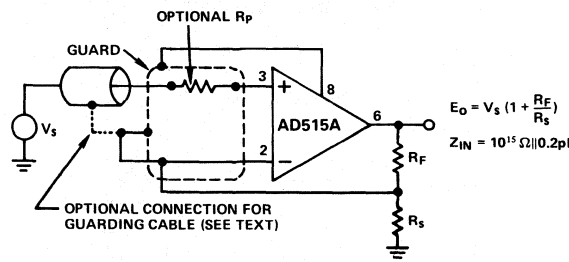


Figure 3. Very High Impedance Noninverting Amplifier

INPUT PROTECTION

The AD515A is guaranteed for a maximum safe input potential equal to the power supply potential.

Many instrumentation situations, such as flame detectors in gas chromatographs, involve measurement of low level currents from high-voltage sources. In such applications, a sensor fault condition may apply a very high potential to the input of the current-to-voltage converting amplifier. This possibility necessitates some form of input protection. Many electrometer type devices, especially CMOS designs, can require elaborate Zener protection schemes which often compromise overall performance. The AD515A requires input protection only if the source is not current limited, and as such is similar to many JFET-input designs. The failure mode would be overheating from excess current rather than voltage breakdown. If the source is not current limited, all that is required is a resistor in series with the affected input terminal so that the maximum overload current is 0.1mA (for example, 1MΩ for a 100V overload). This simple scheme will cause no significant reduction in performance and give complete overload protection. Figures 2 and 3 show proper connections.

COAXIAL CABLE AND CAPACITANCE EFFECTS

If it is not possible to attach the AD515A virtually on top of the signal source, considerable care should be exercised in designing the connecting lines carrying the high impedance signal. Shielded coaxial cable must be used for noise reduction, but use of coaxial cables for high impedance work can add problems from cable leakage, noise and capacitance. Only the best polyethylene or virgin teflon (not reconstituted) should be used to obtain the highest possible insulation resistance.

Cable systems should be made as rigid and vibration free as possible since cable movement can cause noise signals of three types, all significant in high impedance systems. Frictional movement of the shield over the insulation material generates a charge which is sensed by the signal line as a noise voltage. Low noise cable with graphite lubricant such as Amphenol 21-537 will reduce the noise, but short, rigid lines are better. Cable movements will also make small changes in the internal cable capacitance and capacitance to other objects. Since the total charge on these capacitances cannot be changed instantly, a noise voltage results as predicted from: $\Delta V = Q/\Delta C$. Noise voltage is also generated by the motion of a conductor in a magnetic field.

The conductor-to-shield capacitance of coaxial cable is usually about 30pF/foot. Charging this capacitance can cause considerable stretching of high impedance signal rise-time, thus cancelling the low input capacitance feature of the AD515A. There are two ways to circumvent this problem. For inverting signals or low-level current measurements, the signal is carried on the line connected to the inverting input and shielded (guarded) by the ground line as shown in Figure 2. Since the signal is always at virtual ground, no voltage change is required and no capacitances are charged. In many circumstances, this will destabilize the circuit; if so, capacitance from output to inverting input will stabilize the circuit.

Noninverting and buffer situations are more critical since the signal line voltage and therefore charge will change, causing signal delay. This effect can be reduced considerably by connecting the cable shield to a guard potential instead of ground, an option shown in Figure 3. Since such a connection results in positive feedback to the input, the circuit may be destabilized and oscillate. If so, capacitance from positive input to ground must be added to make the net capacitance at Pin 3 positive. This technique can considerably reduce the effective capacitance which must be charged.

Typical Performance Curves

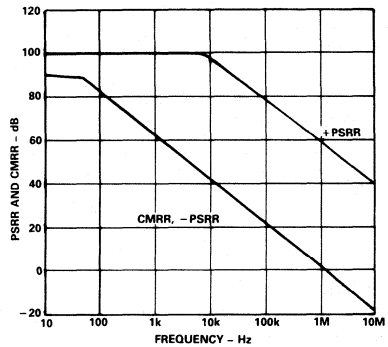


Figure 4. PSRR and CMRR vs. Frequency

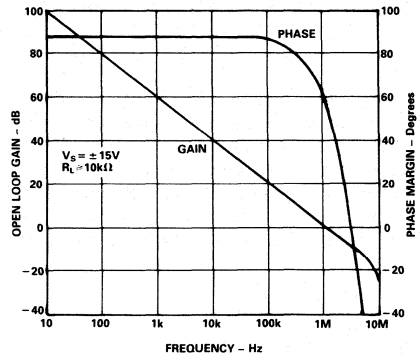


Figure 5. Open Loop Frequency Response

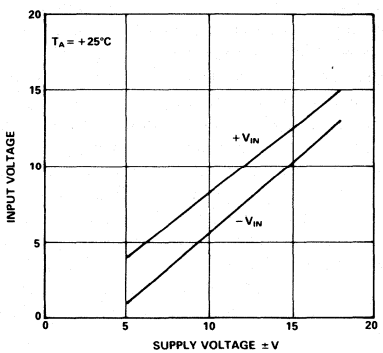


Figure 6. Input Common-Mode Range vs. Supply Voltage

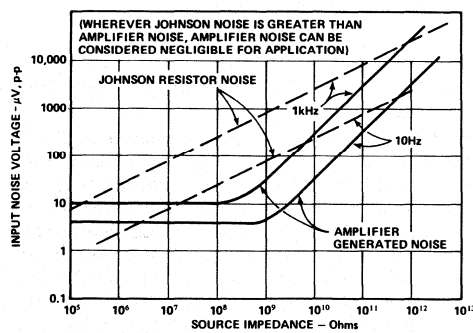


Figure 7. Peak-to-Peak Input Noise Voltage vs. Source Impedance and Bandwidth

ELECTROMETER APPLICATION NOTES

The AD515A offers subpicoampere input bias currents available in an integrated circuit package. This design will open up many new application opportunities for measurements from very high impedance and very low current sources. Performing accurate measurements of this sort requires careful attention to detail; the notes given here will aid the user in realizing the full measurement potential of the AD515A and perhaps extending its performance limits.

1. As with all junction FET input devices, the temperature of the FETs themselves is all important in determining the input bias currents. Over the operating temperature range, the input bias currents closely follow a characteristic of doubling every 10°C; therefore, every effort should be made to minimize device operating temperature.
2. The heat dissipation can be reduced initially by careful investigation of the application. First, if it is possible to reduce the required power supplies, this should be done since internal power consumption contributes the largest component of self-heating. To minimize this effect, the quiescent current of the AD515A has been reduced to less than 1mA. Figure 8 shows typical input bias current and quiescent current versus supply voltage.

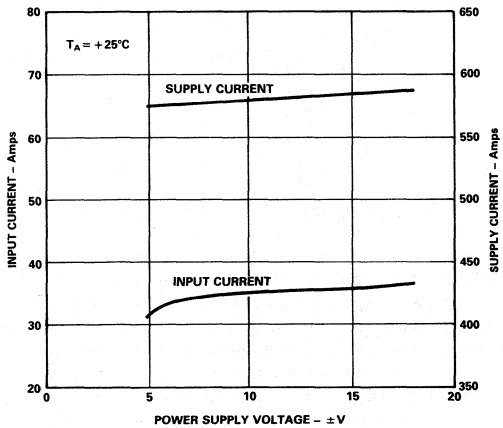


Figure 8. Input Bias Current and Supply Current vs. Supply Voltage

3. Output loading effects, which are normally ignored, can cause a significant increase in chip temperature and therefore bias current. For example, a 2kΩ load driven at 10V at the output will cause at least an additional 25mW dissipation in the output stage (and some in other stages) over the typical 24mW, thereby at least doubling the effects of self-heating. The results of this form of additional power dissipation are demonstrated in Figure 9, which shows normalized input bias current versus additional power dissipated. Therefore, although many dc performance parameters are specified driving a 2kΩ load, to reduce this additional dissipation, we recommend restricting the load resistance to be at least 10kΩ.

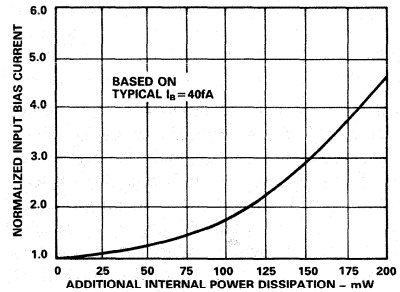


Figure 9. Input Bias Current vs. Additional Power Dissipation

4. Figure 10 shows the AD515A's input current versus differential input voltage. Input current at either terminal stays below a few hundred fA until one input terminal is forced higher than 1 to 1.5V above the other terminal. Input current limits at 30μA under these conditions.

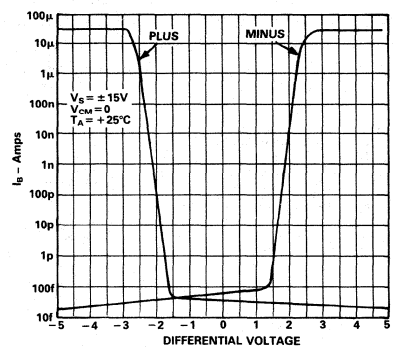


Figure 10. Input Bias Current vs. Differential Input Voltage

AD515A CIRCUIT APPLICATION NOTES

The AD515A is quite simple to apply to a wide variety of applications because of the pretrimmed offset voltage and internal compensation, which minimize required external components and eliminate the need for adjustments to the device itself. The major considerations in applying this device are the external problems of layout and heat control which have already been discussed. In circuit situations employing the use of very high value resistors, such as low level current to voltage converters, electrometer operational amplifiers can be destabilized by a pole created by the small capacitance at the negative input. If this occurs, a capacitor of 2 to 5pF in parallel with the resistor will stabilize the loop. A much larger capacitor may be used if desired to limit bandwidth and thereby reduce wideband noise.

Selection of passive components employed in high impedance situations is critical. High MΩ resistors should be of the carbon film or deposited ceramic oxide to obtain the best in low noise and high stability performance. The best packaging for high MΩ resistors is a glass body sprayed with silicone varnish to minimize humidity effects. These resistors must be handled very carefully to prevent surface contamination. Capacitors for any high impedance or long-term integration situation should be of a polystyrene formulation for optimum performance. Most other types have too low an insulation resistance, or high dielectric absorption.

Unlike situations involving standard operational amplifiers with much higher bias currents, balancing the impedances seen at the input terminals of the AD515A is usually unnecessary and probably undesirable. At the large source impedances where these effects matter, obtaining quality, matched resistors will be difficult. More important, instead of a cancelling effect, as with bias current, the noise voltage of the additional resistor will add by root-sum-of-squares to that of the other resistor thus increasing the total noise by about 40%. Noise currents driving the resistors also add, but in the AD515A are significant only above $10^{11}\Omega$.

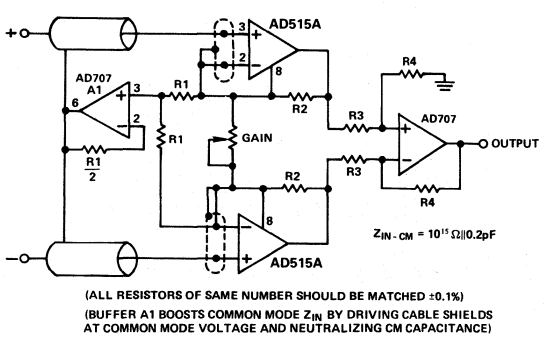


Figure 11. Very High Impedance Instrumentation Amplifier

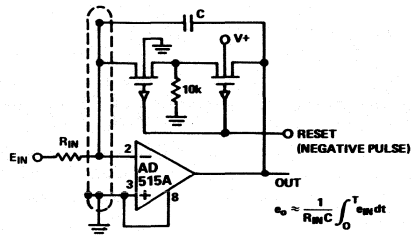


Figure 12. Low Drift Integrator and Low-Leakage Guarded Reset

LOW-LEVEL CURRENT-TO-VOLTAGE CONVERTERS

Figure 2 shows a standard low-level current-to-voltage converter. To obtain higher sensitivity, it is obvious to simply use a higher value feedback resistor. However, high value resistors above $10^9\Omega$ tend to be expensive, large, noisy and unstable. To avoid this, it may be desirable to use a circuit configuration with output gain, as in Figure 13. The drawback is that input errors of offset voltage drift and noise are multiplied by the same gain, but the precision performance of the AD515A makes the tradeoff easier.

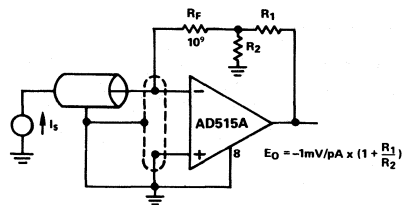


Figure 13. Picoampere to Voltage Converter with Gain

One of the problems with low-level leakage current testing or low-level current transducers (such as Clark oxygen sensors) is finding a way to apply voltage bias to the device while still grounding the device and the bias source. Figure 14 shows a technique in which the desired bias is applied at the noninverting terminal thus forcing that voltage at the inverting terminal. The current is sensed by R_F, and the AD524 instrumentation amplifier converts the floating differential signal to a single-ended output.

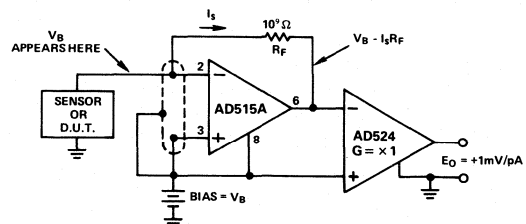


Figure 14. Current-to-Voltage Converters with Grounded Bias and Sensor

ANALOG DEVICES

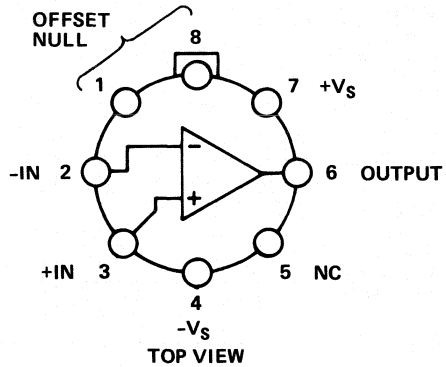
Low Cost, Laser Trimmed, Precision IC Op Amp

AD517

FEATURES

- Low Input Bias Current: 1nA max (AD517L)
- Low Input Offset Current: 0.25nA max (AD517L)
- Low V_{OS}: 50μV max (AD517L), 150μV max (AD517J)
- Low V_{OS} Drift: 1.3μV/°C (AD517L)
- Internal Compensation
- MIL-Standard Parts Available
- 8-Pin TO-99 Hermetic Metal Can
- Available in Chip Form

PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD517 is a high accuracy monolithic op amp featuring extremely low offset voltages and input currents. Analog Devices' thermally-balanced layout and superior IC processing combine to produce a truly precision device at low cost.

The AD517 is laser trimmed at the wafer level (LWT) to produce offset voltages less than 50μV and offset voltage drifts less than 1.3μV/°C unnulled. Superbeta input transistors provide extremely low input bias currents of 1nA max and offset currents as low as 0.25nA max. While these figures are comparable to presently available BIFET amplifiers at room temperature, the AD517 input currents decrease, rather than increase, at elevated temperatures. Open-loop gain in many IC amplifiers is degraded under loaded conditions due to thermal gradients on the chip. However, the AD517 layout is balanced along a thermal axis, maintaining open-loop gain in excess of 1,000,000 for a wide range of load resistances.

The input stage of the AD517 is fully protected, allowing differential input voltages of up to $\pm V_S$ without degradation of gain or bias current due to reverse breakdown. The output stage is short-circuit protected and is capable of driving a load capacitance up to 1000pF.

The AD517 is well suited to applications requiring high precision and excellent long-term stability at low cost, such as stable references, followers, bridge instruments and analog computation circuits.

The circuit is packaged in a hermetically sealed TO-99 metal can, and is available in three performance versions (J, K, and L) specified over the commercial 0 to +70°C range; and one version (AD517S) specified over the extended temperature range, -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. Offset voltage is 100% tested and guaranteed on all models.
2. The AD517 exhibits extremely low input bias currents without sacrificing CMRR (over 100dB) or offset voltage stability.
3. The AD517 inputs are protected (to $\pm V_S$), preventing offset voltage and bias current degradation due to reverse breakdown of the input transistors.
4. Internal compensation is provided, eliminating the need for additional components (often required by high accuracy IC op amps).
5. The AD517 can directly replace 725, 108, and AD510 amplifiers. In addition, it can replace 741-type amplifiers if the offset-nulling potentiometer is removed.
6. Thermally-balanced layout insures high open-loop gain independent of thermal gradients induced by output loading, offset nulling, and power supply variations.
7. Chips are available.

AD517—SPECIFICATIONS (@ +25°C and V_S = ±15V dc)

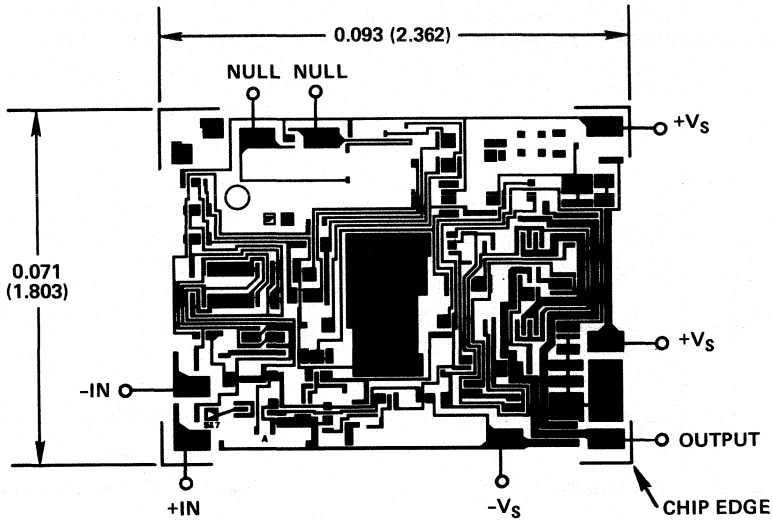
Model	AD517J Min	AD517J Typ	AD517J Max	AD517K Min	AD517K Typ	AD517K Max	AD517L Min	AD517L Typ	AD517L Max	AD517S Min	AD517S Typ	AD517S Max	Units
OPEN LOOP GAIN													
V_O = ±10V, $R_L \geq 2k\Omega$	**10^6**			**10^6**			**10^6**			**10^6**			V/V
T_{min} to T_{max}, $R_L = 2k\Omega$	500,000			500,000			500,000			**250,000**			V/V
OUTPUT CHARACTERISTICS													
Voltage @ $R_L = 2k\Omega$, T_{min} to T_{max}	**±10**			**±10**			**±10**			**±10**			V
Load Capacitance		1000			1000			1000			1000		pF
Output Current	10			10			10			10			mA
Short Circuit Current		25			25			25			25		mA
FREQUENCY RESPONSE													
Unity Gain Small Signal		250			250			250			250		kHz
Full Power Response		1.5			1.5			1.5			1.5		kHz
Slew Rate, Unity Gain		0.10			0.10			0.10			0.10		V/µs
INPUT OFFSET VOLTAGE													
Initial Offset			**150**			**75**			**50**			**75**	µV
Input Offset vs. Temp.			3.0			**1.8**			**1.3**			**1.8**	µV/°C
Input Offset vs. Supply			**25**			**10**			**10**			**10**	µV/V
T_{min} to T_{max}			40			15			15			**20**	µV/V
INPUT BIAS CURRENT													
Initial			5			2			**1.0**			**2.0**	nA
T_{min} to T_{max}			8			3.5			1.5			**10**	nA
vs. Temp, T_{min} to T_{max}			±20			±10			±4			±10	pA/°C
INPUT OFFSET CURRENT													
Initial			**1.0**			**0.75**			**0.25**			**2.0**	nA
T_{min} to T_{max}			1.5			1.25			0.4			**10**	nA
INPUT IMPEDANCE													
Differential		15‖1.5			20‖1.5			20‖1.5			20‖1.5		MΩ‖pF
Common Mode		2.0×10^{11}			2.0×10^{11}			2.0×10^{11}			2.0×10^{11}		Ω
INPUT VOLTAGE RANGE													
Differential		±V_S			±V_S			±V_S			±V_S		V
Common Mode Rejection	**94**			**110**			**110**			**110**			dB
Common Mode Rejection													
T_{min} to T_{max}	94			110			100			**100**			dB
INPUT NOISE													
Voltage, 0.1Hz to 10Hz		2			2			2			2		µV p-p
f = 10Hz		35			35			35			35		nV/$\sqrt{Hz}$
f = 100Hz		25			25			25			25		nV/$\sqrt{Hz}$
f = 1kHz		20			20			20			20		nV/$\sqrt{Hz}$
Current, f = 10kHz		0.05			0.05			0.05			0.05		pA/$\sqrt{Hz}$
f = 100Hz		0.03			0.03			0.03			0.03		pA/$\sqrt{Hz}$
f = 1kHz		0.03			0.03			0.03			0.03		pA/$\sqrt{Hz}$
POWER SUPPLY													
Rated Performance		±15			±15			±15			±15		V
Operating	±5		±18	±5		±18	±5		±18	±5		±18	V
Quiescent Current			**4**			**3**			**3**			**3**	mA
TEMPERATURE RANGE													
Operating, Rated Performance	0		+70	0		+70	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
PACKAGE OPTION[1]													
TO-99 Style (H-08B)		AD517JH			AD517KH			AD517LH			AD517SH		
J and S Grade Chips Also Available													

NOTES
[1]For outline information see Package Information section.
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

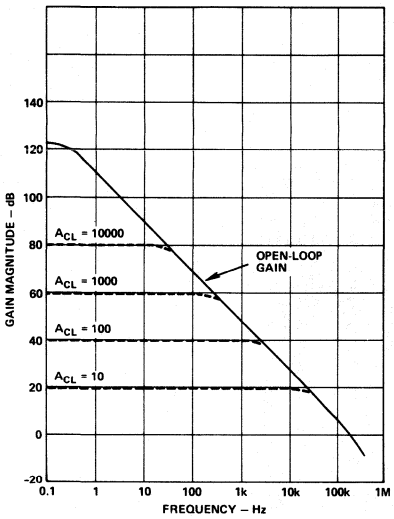
CHIP DIMENSIONS AND BONDING DIAGRAM

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).

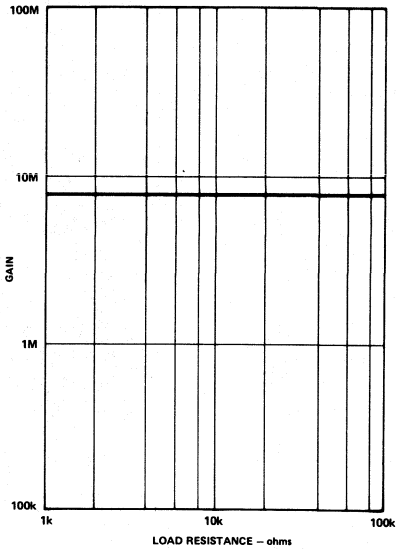


THE AD517 IS AVAILABLE IN
LASER-TRIMMED CHIP FORM.

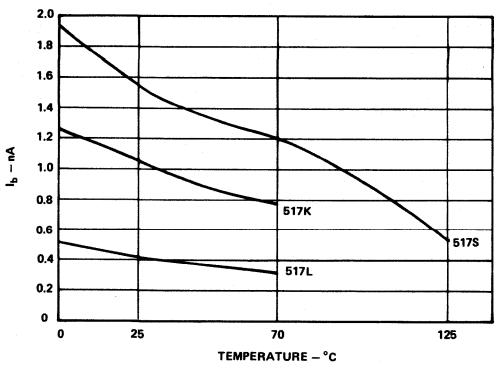
AD517—Typical Performance Curves



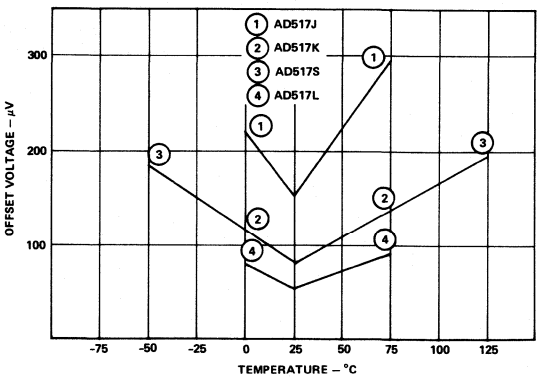
Small-Signal Gain vs. Frequency



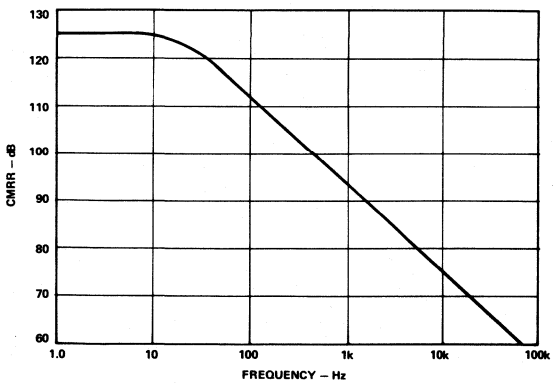
Open-Loop Gain vs. Load Resistance



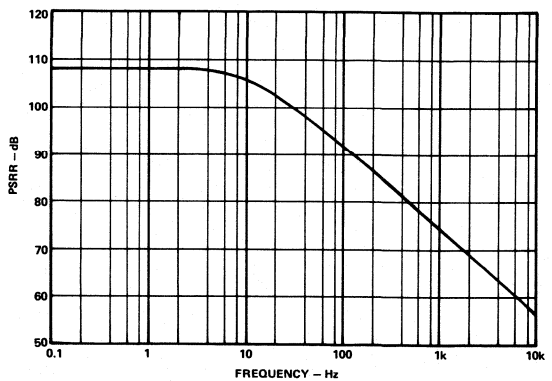
Input Bias Current vs. Temperature



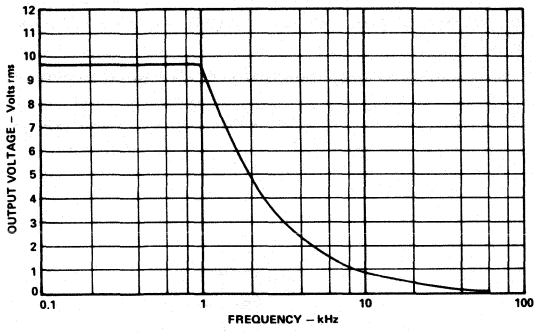
Untrimmed Offset Voltage vs. Temperature



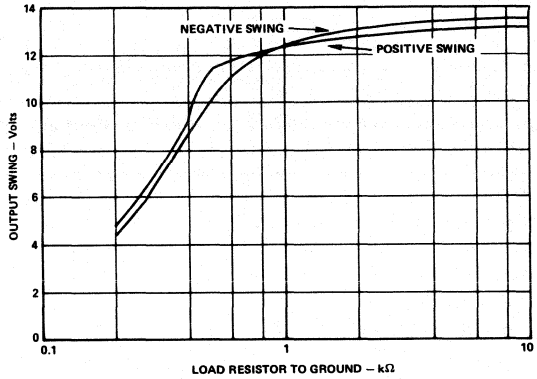
CMRR vs. Frequency



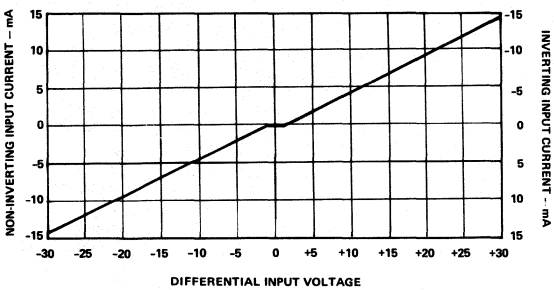
PSRR vs. Frequency



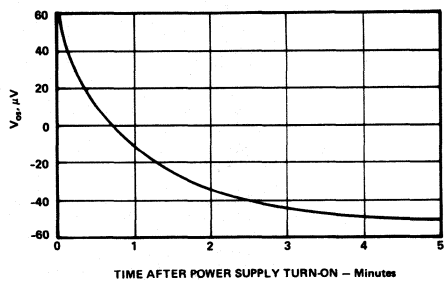
Maximum Undistorted Output vs. Frequency (Distortion ≤ 1%)



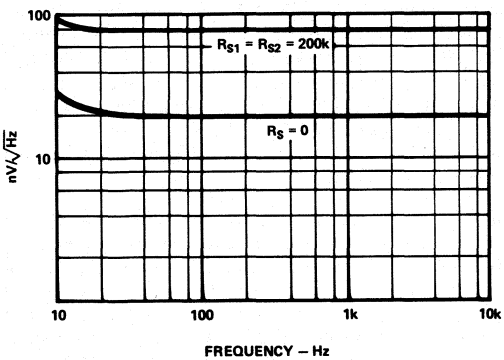
Output Voltage vs. Load Resistance



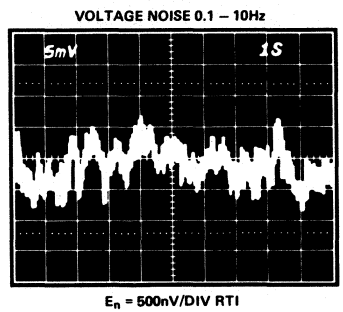
Input Current vs. Differential Input Voltage



Warm-Up Offset Voltage Drift



Total Input Noise Voltage vs. Frequency



Low Frequency Voltage Noise (0.1 to 10Hz)

AD517—Applications

NULLING THE AD517

The internally-trimmed offset voltage of the AD517 will be low enough for most circuits without further nulling. However, in high precision applications, the AD517 may be nulled using either of the following methods:

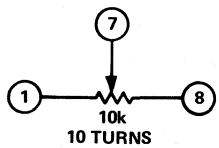
Figure 1A shows a simple circuit using a 10kΩ, ten-turn potentiometer. This circuit allows nulling to within several microvolts.

The circuit of Figure 1B is recommended in applications where nulling to within 1μV is desired. This circuit has the advantage that potentiometer instability effects are reduced by a factor of ten. Values of R_1' and R_2' are calculated as follows:

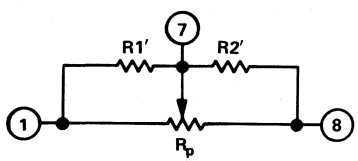
1. Null the offset to zero using a standard 10k pot, as shown in Figure 1A.
2. Measure pot halves R_1 and R_2.
3. Calculate:

$$R_1' = \frac{R_1 \times 50k\Omega}{50k\Omega - R_1} \qquad R_2' = \frac{R_2 \times 50k\Omega}{50k\Omega - R_2}$$

4. Replace the pot with R_1' and R_2' using the closest value 1% metal film resistors.
5. Use a 100k, ten-turn pot for R_p to complete the nulling.



A. Simple



B. High Precision

Figure 1. Nulling Circuits

AN INSTRUMENT INPUT AMPLIFIER USING THE AD517L

The circuit shown in Figure 2 represents a typical input stage for laboratory instruments and panel meters. The amplifier is non-inverting and offers selectable gains from 1 to 1000 in decade steps.

Input impedance of this amplifier is 10 megohms, determined by resistor R_1. The offset nulling network comprised of R_3, R_4 and R_5 is the same one described earlier. If a less precise adjustment can be tolerated, a single 10k potentiometer can be substituted for R_3, R_4 and R_5.

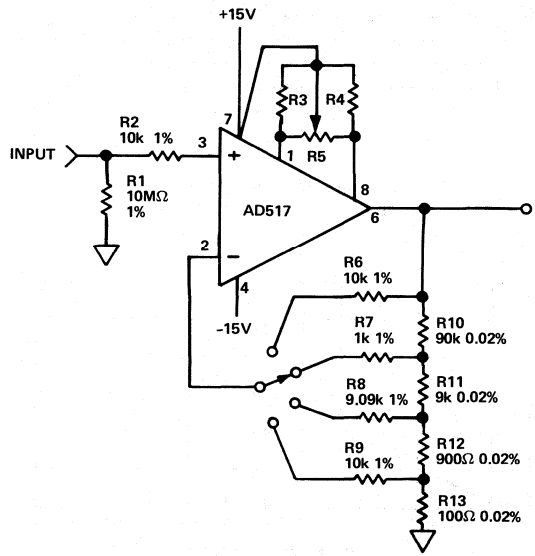


Figure 2. Stable Instrument Input Amplifier

Gain switching is accomplished in the feedback network. The divider consisting of R_{10}, R_{11}, R_{12} and R_{13} determines the gain by dividing the output and returning it to the inverting input of the amplifier. The ratio tolerances of these resistors uniquely determine the gain of the amplifier. The impedance seen by the inverting input is held constant at 10k ohms by R_6, R_7 R_8 or R_9 depending on the gain selected. Since input bias currents flow through equal resistances, the offset voltages produced will cancel each other. The input offset currents will produce an insignificant offset voltage on the order of 1 microvolt. If this offset is nulled out at the highest gain selected, it will be nulled on all ranges.

The AD517 offers excellent temperature stability in this circuit. Once the offset has been zeroed, the error produced by offset current drift will remain quite low due to the extremely low offset current drift of the AD517. A FET-input op amp would not work well in this application, since the input offset currents would double for each 10°C increase in temperature, soon exceeding the input offset currents of the AD517.

ANALOG DEVICES

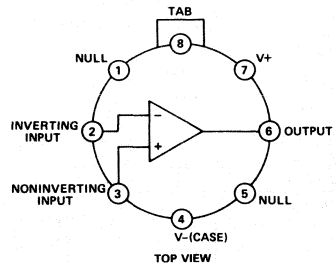
High Performance, BiFET Operational Amplifiers

AD542/AD544/AD547

FEATURES

Ultralow Drift: 1μV/°C – AD547L
Low Offset Voltage: 0.25mV – AD547L
Low Input Bias Currents: 25pA max, Warmed-Up
Low Quiescent Current: 1.5mA
Low Noise: 2μV p-p
High Open Loop Gain: 110dB
High Slew Rate: 13V/μs
Fast Settling to ±0.01%: 3μs
Low Total Harmonic Distortion: 0.0025%
Available in Hermetic Metal Can Packages and Chip Form
MIL-STD-883B Processing Available
Dual Versions Available: AD642, AD644, AD647

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The BiFET series are precision monolithic FET-input operational amplifiers fabricated with the most advanced BiFET and laser trimming technologies. The series offers bias currents significantly lower than currently available BiFET devices, 25pA max, warmed-up.

In addition, the offset voltage is laser trimmed to less than 0.25mV on the AD547L which is achieved by utilizing Analog's exclusive laser-wafer trimming (LWT) process. When combined with the AD547's low offset voltage drift (1μV/°C), these features offer the user IC performance truly superior to existing BiFET op amps–and at low, BiFET pricing.

The AD542 or AD547 is recommended for any operational amplifier application requiring excellent dc performance at low to moderate costs. Precision instrument front ends requiring accurate amplification of millivolt level signals from megohm source impedances will benefit from the device's excellent combination of low offset voltage and drift, low bias current and low 1/f noise. High common mode rejection (80dB, min on the "K" and "L" versions) and high open-loop gain–even under heavy loading–ensures better than "12-bit" linearity in high impedance buffer applications.

The AD544 is recommended for any operational amplifier application requiring excellent ac and dc performance at low cost. The 2MHz bandwidth and low offset of the AD544 make it the first choice as an output amplifier for current output D/A converters such as the AD7541, 12-bit CMOS DAC.

Devices in this series are available in four versions: the "J," "K" and "L" are specified over the 0 to +70°C temperature range and the "S" over the −55°C to +125°C operating temperature range. All devices are packaged in the hermetically-sealed, TO-99 metal can.

PRODUCT HIGHLIGHTS

1. Improved bipolar and JFET processing results in the lowest bias current available in a monolithic FET op amp.
2. Analog Devices, unlike some manufacturers, specifies each device for the maximum bias current at either input in the warmed-up condition, thus assuring the user that the device will meet its published specifications in actual use.
3. Advanced laser wafer trimming techniques reduce offset voltage drift to 1μV/°C max and offset voltage to only 0.25mV max on the AD547L.
4. Low voltage noise (2μV, p-p), and low offset voltage drift enhance performance as a precision op amp.
5. The high slew rate (13.0V/μs) and fast settling time to 0.01% (3.0μs) make the AD544 ideal for D/A, A/D, sample-hold circuits and high speed integrators.
6. Low harmonic distortion (0.0025%) make the AD544 an ideal choice for audio applications.
7. Unmounted chips available for hybrid circuit applications.

AD542/AD544/AD547 — SPECIFICATIONS (@ +25°C and V_S = ±15V dc)

Model	AD542			AD544			AD547			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OPEN LOOP GAIN[1]										
V_{OUT} = ±10V $R_L \geq 2k\Omega$										
J	**100,000**			**30,000**			**100,000**			V/V
K, L, S	**250,000**			**50,000**			**250,000**			V/V
$T_A = T_{min}$ to T_{max}										
J	100,000			20,000			100,000			V/V
S	**100,000**			**20,000**			**100,000**			V/V
K, L	**250,000**			**40,000**			**250,000**			V/V
GUTPUT CHARACTERISTICS										
$V_{OUT} = R_L = 2k\Omega$										
$T_A = T_{min}$ to T_{max}	**±10**	±12		**±10**	±12		**±10**	±12		Volts
$V_{OUT} = R_L = 10k\Omega$										
$T_A = T_{min}$ to T_{max}	**±12**	±13		**±12**	±13		**±12**	±13		Volts
Short Circuit Current		25			25			25		mA
FREQUENCY RESPONSE										
Unity Gain, Small Signal		1.0			2.0			1.0		MHz
Full Power Response		50			200			50		kHz
Slew Rate, Unity Gain	**2.0**	3.0		**8.0**	13.0		**2.0**	3.0		V/µs
Total Harmonic Distortion					0.0025					%
INPUT OFFSET VOLTAGE[2]										
J			**2.0**			**2.0**			**1.0**	mV
K			**1.0**			**1.0**			**0.5**	mV
L			**0.5**			**0.5**			**0.25**	mV
S			**1.0**			**1.0**			**0.5**	mV
vs. Temperature[3]										
J			20			20			5	µV/°C
K			**10**			**10**			**2**	µV/°C
L			5			5			**1**	µV/°C
S			**15**			**15**			5	µV/°C
vs. Supply, $T_A = T_{min}$ to T_{max}										
J			200			200			**200**	µV/V
K, L, S			**100**			**100**			**100**	µV/V
INPUT BIAS CURRENT[4]										
Either Input										
J			**50**			**50**			**50**	pA
K, L, S		10	25		10	25		10	25	pA
Input Offset Current										
J		5	**15**		5	**15**		5	**15**	pA
K, L, S		2	**15**		2	**15**		2	**15**	pA
INPUT IMPEDANCE										
Differential		$10^{12}\Omega\|\|6pF$			$10^{12}\Omega\|\|6pF$			$10^{12}\Omega\|\|6pF$		
Common Mode		$10^{12}\Omega\|\|3pF$			$10^{12}\Omega\|\|3pF$			$10^{12}\Omega\|\|3pF$		
INPUT VOLTAGE[5]										
Differential		±20			±20			±20		Volts
Common Mode	**±10**	±12		**±10**	±12		**±10**	±12		Volts
Common-Mode Rejection										
V_{IN} = ±10V										
J	**76**			**76**			**76**			dB
K, L, S	**80**			**80**			**80**			dB
POWER SUPPLY										
Rated Performance		±15			±15			±15		Volts
Operating	±5		**±18**	±5		**±18**	±5		**±18**	Volts
Quiescent Current		1.1	**1.5**		1.8	**2.5**		1.1	**1.5**	mA
VOLTAGE NOISE										
0.1–10Hz										
J		2.0			2.0			2.0		µV p-p
K, L, S		2.0			2.0				**4.0**	µV p-p
10Hz		70			35			70		$nV/\sqrt{Hz}$
100Hz		45			22			45		$nV/\sqrt{Hz}$
1kHz		30			18			30		$nV/\sqrt{Hz}$
10kHz		25			16			25		$nV/\sqrt{Hz}$
TEMPERATURE RANGE										
Operating, Rated Performance										
J, K, L		0 to +70			0 to +70			0 to +70		°C
S		−55 to +125			−55 to +125			−55 to +125		°C
Storage		−65 to +150			−65 to +165			−65 to +165		°C
TRANSISTOR COUNT	29			29			29			

NOTES
[1]Open Loop Gain is specified with V_{OS} both nulled and unnulled.
[2]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[3]Input Offset Voltage Drift is specified with the offset voltage unnulled. Nulling will induce an additional 3µV/°C/mV of nulled offset.
[4]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.
[5]Defined as the maximum safe voltage between inputs, such that neither exceeds ±10V from ground.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

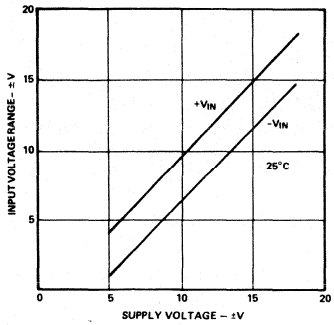


Figure 1. Input Voltage Range vs. Supply Voltage

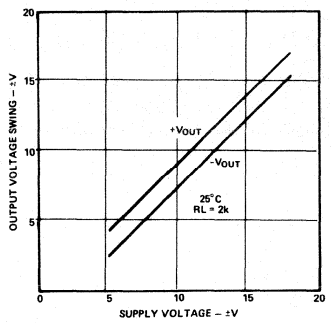


Figure 2. Output Voltage Swing vs. Supply Voltage

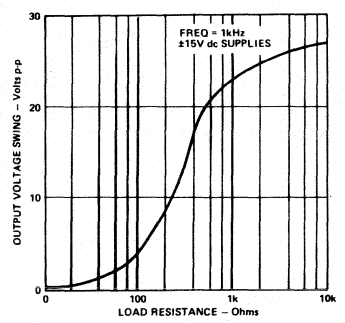


Figure 3. Output Voltage Swing vs. Load Resistance

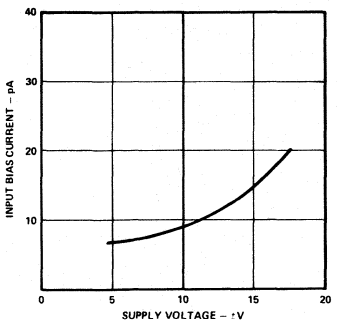


Figure 4. Input Bias Current vs. Supply Voltage

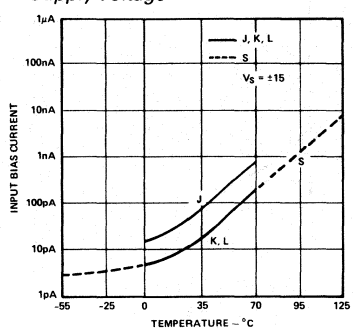


Figure 5. Input Bias Current vs. Temperature

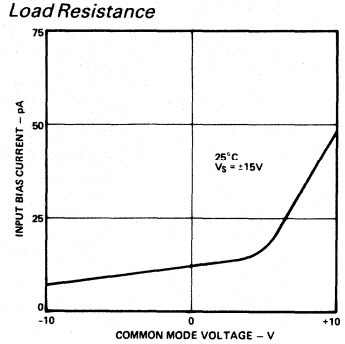


Figure 6. Input Bias Current vs. CMV

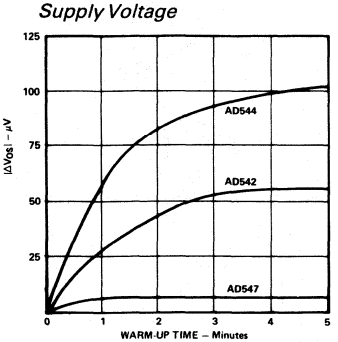


Figure 7. Change in Offset Voltage vs. Warm-Up Time

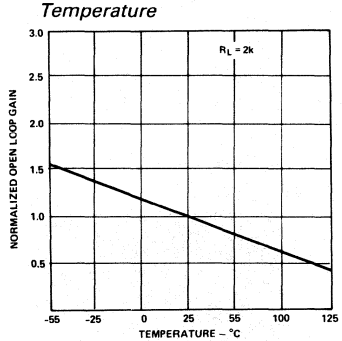


Figure 8. Open Loop Gain vs. Temperature

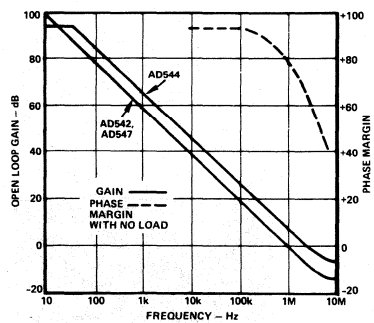


Figure 9. Open Loop Frequency Response

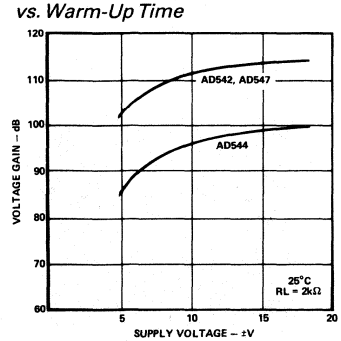


Figure 10. Open Loop Voltage Gain vs. Supply Voltage

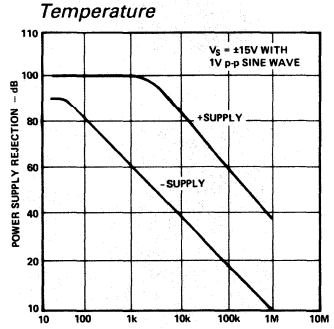


Figure 11. Power Supply Rejection vs. Frequency

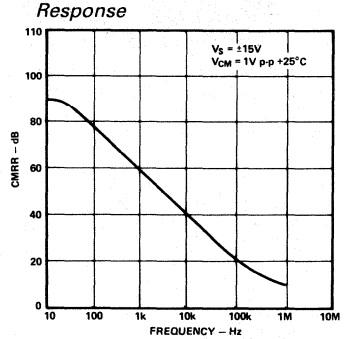


Figure 12. Common Mode Rejection Ratio vs. Frequency

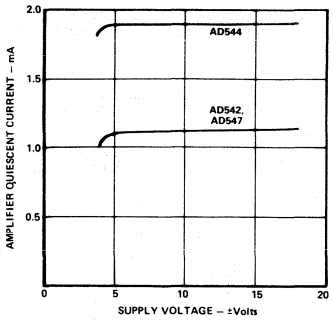


Figure 13. Quiescent Current vs. Supply Voltage

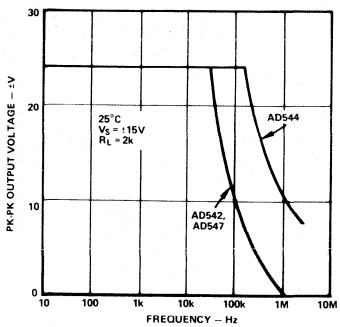


Figure 14. Large Signal Frequency Response

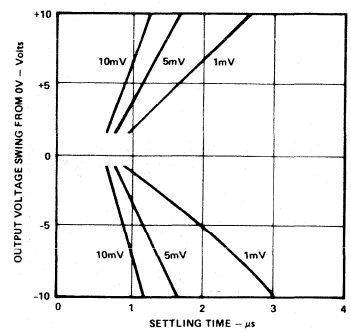


Figure 15. AD544 Output Swing and Error vs. Settling Time

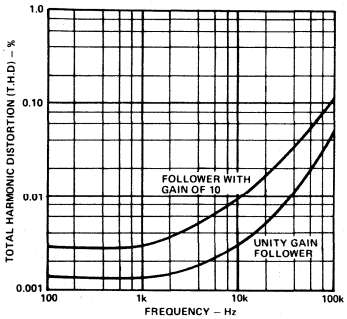


Figure 16. AD544 Total Harmonic Distortion vs. Frequency

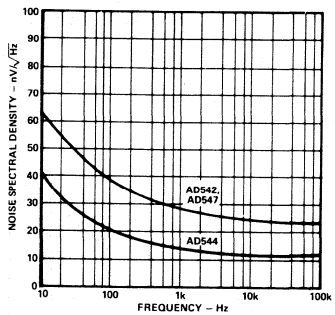


Figure 17. Input Noise Voltage Spectral Density

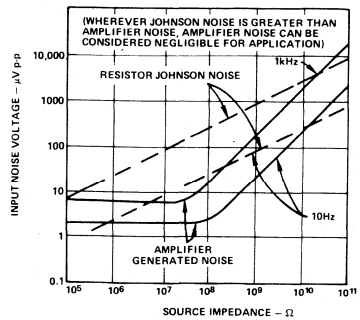
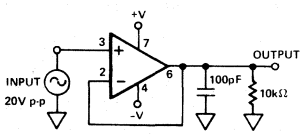
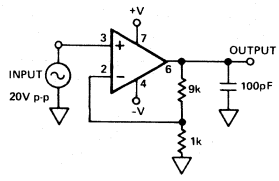


Figure 18. Total RMS Noise vs. Source Impedance



a. Unity Gain Follower



b. Follower with Gain = 10

Figure 19. T.H.D. Test Circuits

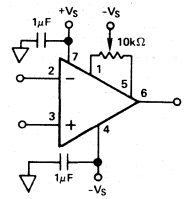


Figure 20. Standard Null Circuit

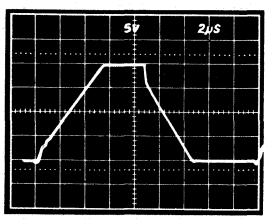


Figure 21a. Unity Gain Follower Pulse Response (Large Signal)

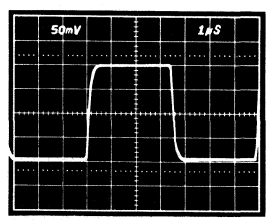


Figure 21b. Unity Gain Follower Pulse Response (Small Signal)

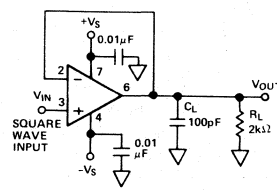


Figure 21c. Unity Gain Follower–AD542/AD547

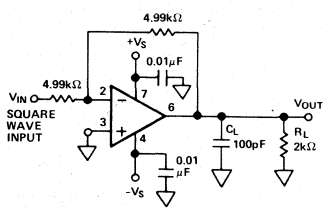


Figure 22a. Unity Gain Inverter–AD542/AD547

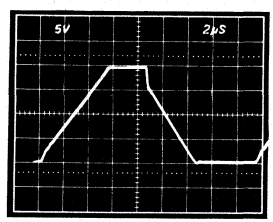


Figure 22b. Unity Gain Inverter Pulse Response (Large Signal)

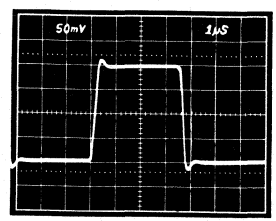


Figure 22c. Unity Gain Inverter Pulse Response (Small Signal)

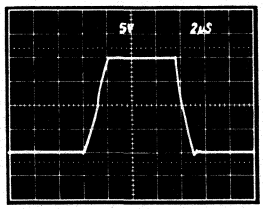


Figure 23a. Unity Gain Follower Pulse Response (Large Signal)

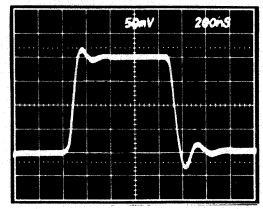


Figure 23b. Unity Gain Follower Pulse Response (Small Signal)

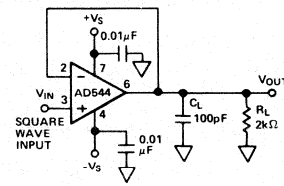


Figure 23c. Unity Gain Follower

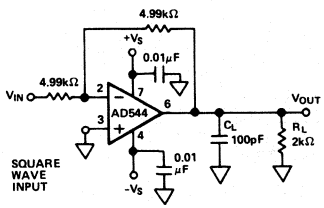


Figure 24a. Unity Gain Inverter

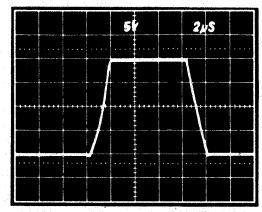


Figure 24b. Unity Gain Inverter Pulse Response (Large Signal)

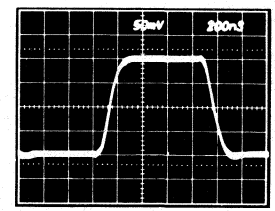


Figure 24c. Unity Gain Inverter Pulse Response (Small Signal)

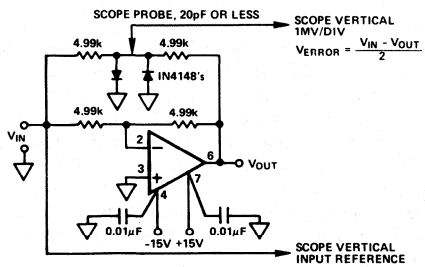


Figure 25. Settling Time Test Circuit

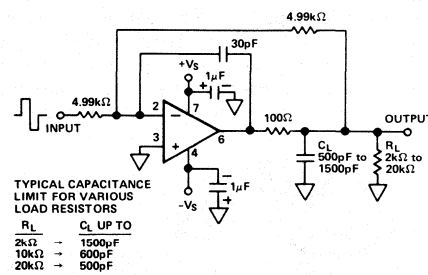


Figure 27. Circuit for Driving a Large Capacitance Load

The upper trace of the oscilloscope photograph of Figure 26 shows the settling characteristic of the AD544. The lower trace represents the input to Figure 27. The AD544 has been designed for fast settling to 0.01%, however, feedback components, circuit layout and circuit design must be carefully considered to obtain the optimum settling time.

The circuit in Figure 27 employs a 100Ω isolation resistor which enables the amplifier to drive capacitance loads exceeding 500pF; the resistor effectively isolates the high frequency feedback from the load and stabilizes the circuit. Low frequency feedback is returned to the amplifier summing junction via the low pass filter formed by the 100Ω series resistor and the load capacitance, C_L.

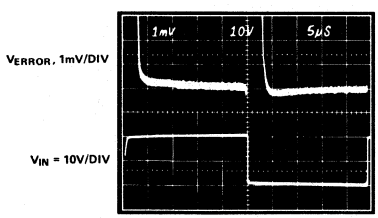


Figure 26. Settling Characteristic Detail – AD544

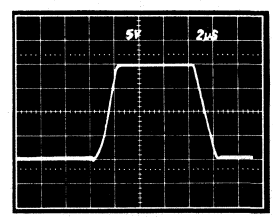


Figure 28. Transient Response $R_L = 2k\Omega$ $C_L = 500pF$–AD544

BiFET Application Hints

APPLICATION NOTES

The BiFET series was designed for high performance op-amp applications that require true dc precision. To capitalize on all of the performance available from the BiFETs there are some practical error sources that should be considered.

The bias currents of JFET input amplifiers double with every 10°C increase in chip temperature. Therefore, minimizing the junction temperature of the chip will result in extending the performance limits of the device.

1. Heat dissipation due to power consumption is the main contributor to self-heating and can be minimized by reducing the power supplies to the lowest level allowed by the application.
2. The effects of output loading should be carefully considered. Greater power dissipation increases bias currents and decreases open loop gain.

GUARDING

The low input bias current (25pA) and low noise characteristics of the high performance BiFET op amp make it suitable for electrometer applications such as photo diode preamplifiers and picoampere current-to-voltage converters. The use of guarding techniques in printed circuit board layout and construction is critical for achieving the ultimate in low leakage performance available from these amplifiers. The input guarding scheme shown in Figure 29 will minimize leakage as much as possible; the guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on a printed circuit.

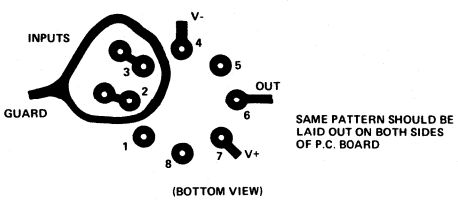


Figure 29. Board Layout for Guarding Inputs

INPUT PROTECTION

The BiFET series is guaranteed for a maximum safe input potential equal to the power supply potential. The input stage design also allows differential input voltages of up to ± 1 volt while maintaining the full differential input resistance of $10^{12}\Omega$. This makes the BiFET series suitable for comparator situations employing a direct connection to high impedance source.

Many instrumentation situations, such as flame detectors in gas chromatographs, involve measurement of low level currents from high-voltage sources. In such applications, a sensor fault condition may apply a very high potential to the input of the current-to-voltage converting amplifier. This possibility necessitates some form of input protection. Many electrometer type devices, especially CMOS designs, can require elaborate zener protection schemes which often compromise overall performance. The BiFET series requires input protection only if the source is not current-limited, and as such is similar to many JFET-input designs. The failure mode would be overheating from excess current rather than voltage breakdown. If the source is not current-limited, all that is required is a resistor in series with the affected input terminal so that the maximum overload current is 1.0mA (for example, 100kΩ for a 100 volt overload). This simple scheme will cause no significant reduction in performance and give complete overload protection. Figure 30 shows proper connections.

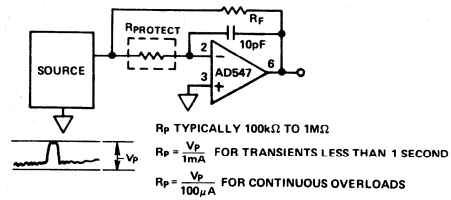


Figure 30. Input Protection

D/A CONVERTER APPLICATIONS

The BiFET series of operational amplifiers can be used with CMOS DACs to perform both 2-quadrant and 4-quadrant operation. The output impedance of a CMOS DAC varies with the digital word, thus changing the noise gain of the amplifier circuit. The effect will cause a nonlinearity the magnitude of which is dependent on the offset voltage of the amplifier. The BiFET series with trimmed offset will minimize this effect. Additionally, the Schottky protection diodes recommended for use with many older CMOS DACs are not required when using one of the BiFET series amplifiers.

Figure 31a shows the AD547 and AD7541 configured for unipolar binary (2-quadrant multiplication) operation. With a dc reference voltage or current (positive or negative polarity) applied at pin 17, the circuit operates as a unipolar converter. With an ac reference voltage or current, the circuit provides 2-quadrant multiplication (digitally controlled attenuation).

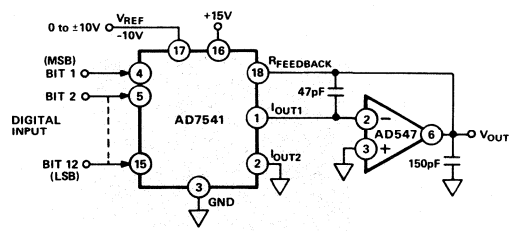


Figure 31a. AD547 Used as DAC Output Amplifier

The oscilloscope photo of Figure 31b shows the output of the circuit of Figure 31a. The upper trace represents the reference input, and the bottom trace shows the output voltage for a digital input of all ones on the DAC (Gain $1-2^{-n}$). The 47pF capacitor across the feedback resistor compensates for the DAC output capacitance, and the 150pF load capacitor serves to minimize output glitches.

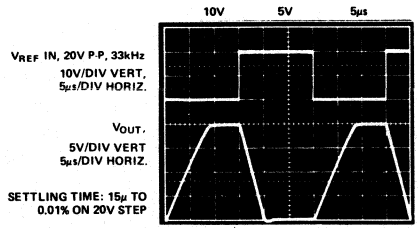


Figure 31b. Voltage Output DAC Settling Characteristic

Figure 32a illustrates the 10-bit digital-to-analog converter, AD7533, connected for bipolar operation. Since the digital input can accept bipolar numbers and V_{REF} can accept a bipolar analog input, the circuit can perform a 4-quadrant multiplying function.

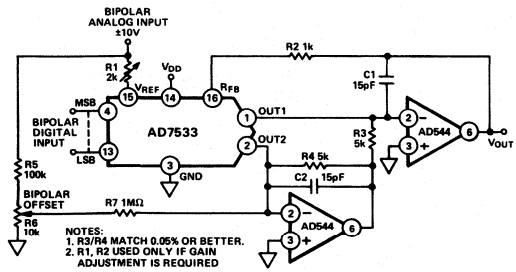


Figure 32a. AD544 Used as DAC Output Amplifiers

The photos exhibit the response to a step input at V_{REF}. Figure 32b is the large signal response and Figure 32c is the small signal response. C1 phase compensation (15pF) is required for stability when using high speed amplifiers. C1 is used to cancel the pole formed by the DAC internal feedback resistance and the output capacitance of the DAC.

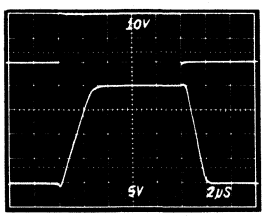


Figure 32b. Large Signal Response

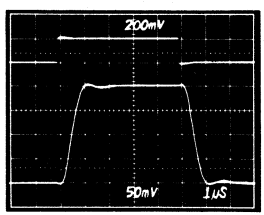


Figure 32c. Small Signal Response

USING THE AD547 IN LOG AMPLIFIER APPLICATIONS

Log amplifiers or log ratio amplifiers are useful in applications requiring compression of wide-range analog input data, linearization of transducers having exponential outputs, and analog computing, ranging from simple translation of natural relationships in log form (e.g., computing absorbence as the log-ratio of input currents), to the use of logarithms in facilitating analog computation of terms involving arbitrary exponents and multi-term products and ratios.

The picoamp level input current and low offset voltage of the AD547 make it suitable for wide dynamic range log amplifiers. Figure 33 is a schematic of a log ratio circuit employing the AD547 that can achieve less than 1% conformance error over 5 decades of current input, 1nA to 100µA. For voltage inputs, the dynamic range is typically 50mV to 10V for 1% error, limited on the low end by the amplifiers' input offset voltage.

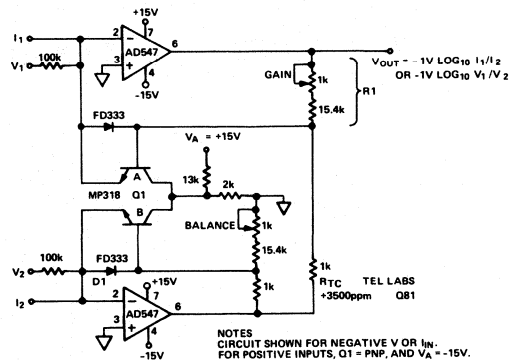


Figure 33. Log-Ratio Amplifier

The conversion between current (or voltage) input and log output is accomplished by the base emitter junctions of the dual transistor Q1. Assuming Q1 has $\beta>100$, which is the case for the specified transistor, the base-emitter voltage on side 1 is to a close approximation:

$$V_{BE\,A} = kT/q \ln I_1/I_{S1}$$

This circuit is arranged to take the difference of the V_{BE}'s of Q1A and Q1B, thus producing an output voltage proportional to the log of the *ratio* of the inputs:

$$V_{OUT} = -K(V_{BE\,A} - V_{BE\,B}) = -\frac{Kkt}{q}(\ln I_1/I_{S1} - \ln I_2/I_{S2})$$

$$V_{OUT} = -K\,kT/q \ln I_1/I_2$$

The scaling constant, K is set by R1 and R_{TC} to about 16, to produce 1V change in output voltage per decade difference in input signals. R_{TC} is a special resistor with a +3500ppm/°C temperature coefficient, which makes K inversely proportional

to temperature, compensating for the "T" in kT/q. The log-ratio transfer characteristic is therefore independent of temperature.

This particular log ratio circuit is free from the dynamic problems that plague many other log circuits. The −3dB bandwidth is 50kHz over the top 3 decades, 100nA to 100μA, and decreases smoothly at lower input levels. This circuit needs no additional frequency compensation for stable operation from input current sources, such as photodiodes, that may have 100pF of shunt capacitance. For larger input capacitances a 20pF integration capacitor around each amplifier will provide a smoother frequency response.

This log ratio amplifier can be readily adjusted for optimum accuracy by following this simple procedure. First, apply V1 = V2 = −10.00V and adjust "Balance" for V_{OUT} = 0.00V. Next apply V1 = −10.00V, V2 = −1.00V and adjust gain for V_{OUT} = +1.00V. Repeat this procedure until gain and balance readings are within 2mV of ideal values.

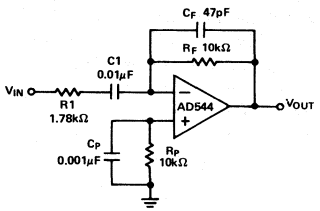


Figure 34. Differentiator

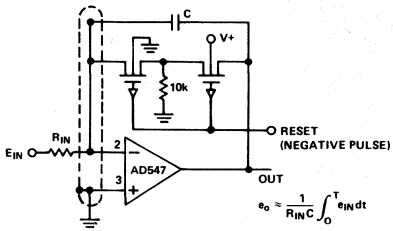


Figure 35. Low Drift Integrator and Low-Leakage Guarded Reset

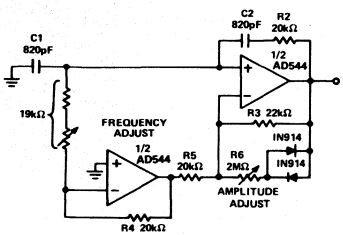


Figure 36. Wien-Bridge Oscillator – f_o = 10kHz

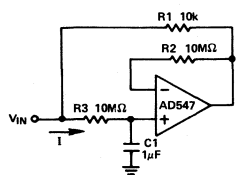


Figure 37. Capacitance Multiplier

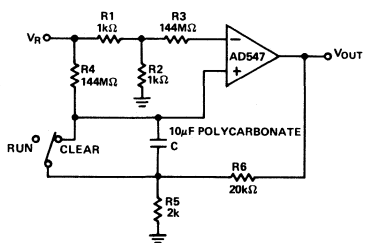


Figure 38. Long Interval Timer – 1,000 Seconds

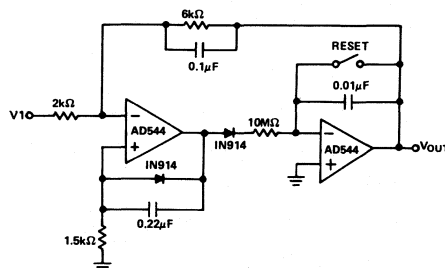


Figure 39. Positive Peak Detector

ORDERING GUIDE

Model	Initial Offset Voltage	Offset Voltage Drift	Settling Time to ±0.012% for 10V Step	Package Option*
AD542JH	2.0mV	20μV/°C	5μs	H-08A
AD542KH	1.0mV	10μV/°C	5μs	H-08A
AD542LH	0.5mV	5μV/°C	5μs	H-08A
AD542SH	1.0mV	15μV/°C	5μs	H-08A
AD547JH	1.0mV	5μV/°C	5μs	H-08A
AD547KH	0.5mV	2μV/°C	5μs	H-08A
AD547LH	0.25mV	1μV/°C	5μs	H-08A
AD547SH	0.5mV	5μV/°C	5μs	H-08A
AD544JH	2.0mV	20μV/°C	3μs	H-08A
AD544KH	1.0mV	10μV/°C	3μs	H-08A
AD544LH	0.5mV	5μV/°C	3μs	H-08A
AD544SH	1.0mV	15μV/°C	3μs	H-08A

*H-08A = TO-99 (Hermetic Metal Can). For outline information see Package Information section.

ANALOG DEVICES

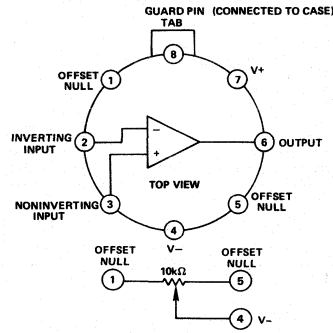
Monolithic Precision, Low Drift FET-Input Op Amp

AD545A*

FEATURES

Low Offset Voltage: 0.5mV max (AD545AL)
0.25mV max (AD545AM)
Low Offset Voltage Drift: 5μV/°C max (AD545AL),
3μV/°C max (AD545AM)
Low Power: 1.5mA max
Low Bias Current: 1pA max (AD545AK, L, M)
Low Noise: 3μV p-p, 0.1Hz to 10Hz

PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD545A is a monolithic precision FET-input operational amplifier. It is a successor to the AD545 and will replace the AD545 in most applications. Bias current is specified as 2pA max for the AD545AJ and 1pA max for the AD545AK, L and M. Offset voltage is laser trimmed to 0.5mV max for the AD545AL, 0.25mV max for the AD545AM. All devices also feature low voltage noise and power consumption. The AD545A is internally compensated, short circuit protected and free of latch-up.

The AD545A series offers a broad combination of performance features. For precision applications the AD545AM specifies a 0.25mV max offset voltage, 3μV/°C max drift and 1pA max bias current. The AD545AJ, with a 1mV max offset voltage, 25μV/°C max drift and 2pA max bias current, is the best price performance choice.

These devices are recommended for a variety of general purpose and precision applications requiring low bias currents and high input impedance such as pH/pIon sensitive electrodes, photocurrent detectors, biological microprobes, long-term precision integrators and vacuum ion gage measurements. The versatility of the AD545A is further enhanced by its excellent low frequency noise (3μV p-p, 0.1Hz to 10Hz) and low power consumption (1.5mA max) for portable applications.

As with previous electrometer amplifier designs from Analog Devices, the case is guarded thus minimizing stray leakage. This feature will also shield the input circuitry from external noise and supply transients.

The AD545A is available in four versions of bias current and offset voltage, the "J," "K," "L," and "M." All are specified from 0 to +70°C and supplied in a hermetically sealed TO-99 package.

***Covered by U.S. Patent No. 4,639,683.**

PRODUCT HIGHLIGHTS

1. The offset voltage on the AD545A is laser trimmed to a level typically less than 250μV. Offset voltage drift is only 3μV/°C max for the AD545AM. If additional external nulling is desired, the effect on drift is minimal (approximately 2.5μV/°C mV, nulled).
2. Bias current is specified as the maximum measured at either input with the device fully warmed up on ±15V supplies at +25°C ambient.
3. The low quiescent current drain of 0.6mA typical, and 1.5mA max keeps self-heating to a minimum.
4. The combination of low input noise voltage and very low input noise current is such that for source impedances from much over one MΩ up to $10^{11}\Omega$, the Johnson noise of the source will easily dominate the noise characteristics.

AD545A—SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc, unless otherwise specified)

Model	AD545AJ	AD545AK	AD545AL	AD545AM
OPEN LOOP GAIN[1]				
V_{OUT} = ±10V, $R_L \geq 2k\Omega$	**20,000V/V min**	**40,000V/V min**	**40,000V/V min**	**40,000V/V min**
$R_L \geq 10k\Omega$	**40,000V/V min**	**50,000V/V min**	**50,000V/V min**	**50,000V/V min**
T_A = min to max $R_L \geq 2k\Omega$	**15,000V/V min**	**25,000V/V min**	**40,000V/V min**	**40,000V/V min**
OUTPUT CHARACTERISTICS				
Voltage@R_L = 2kΩ, T_A = min to max	**±10V min (±12V typ)**	*	*	*
@R_L = 10kΩ, T_A = min to max	**±12V min (±13V typ)**	*	*	*
Load Capacitance[2]	500pF	*	*	*
Short Circuit Current	**10mA min (20mA typ)**	*	*	*
FREQUENCY RESPONSE				
Unity Gain, Small Signal	1MHz	*	*	*
Full Power Response	5kHz min (30kHz typ)	*	*	*
Slew Rate Inverting Unity Gain	0.3V/μs min (2.0V/μs typ)	*	*	*
Overload Recovery Inverting Unity Gain	100μs max (2μs typ)	*	*	*
INPUT OFFSET VOLTAGE[3]	**1.0mV max**	**1.0mV max**	**0.5mV max**	**0.25mV max**
vs. Temperature, T_A = min to max	**25μV/°C max**	**15μV/°C max**	**5μV/°C max**	**3μV/°C max**
vs. Supply, T_A = min to max	**400μV/V max (50μV/V typ)**	**200μV/V max**	**200μV/V max**	**200μV/V max**
INPUT BIAS CURRENT				
Either Input[4]	**2pA max**	**1pA max**	**1pA max**	**1pA max**
INPUT IMPEDANCE				
Differential V_{IN} = ±1V	$1.6pF \| 10^{13}\Omega$	*	*	*
Common Mode	$0.8pF \| 10^{15}\Omega$	*	*	*
INPUT NOISE				
Voltage, 0.1Hz to 10Hz	3.0μV (p-p)	*	*	**5μV (p-p) max**
f = 10Hz	$55nV/\sqrt{Hz}$	*	*	*
f = 100Hz	$45nV/\sqrt{Hz}$	*	*	*
f = 1kHz	$35nV/\sqrt{Hz}$	*	*	*
Current, 0.1Hz to 10Hz	0.03pA (p-p)	*	*	*
10Hz to 10kHz	0.05pA rms	*	*	*
INPUT VOLTAGE RANGE				
Differential	±20V min	*	*	*
Common Mode, T_A = min to max	±10V min	*	*	*
Common-Mode Rejection, V_{IN} = ±10V	**66dB min (80dB typ)**	**70dB min**	**76dB min**	**76dB min**
Maximum Safe Input Voltages[5]	±V_S	*	*	*
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	**±5V min (±18V max)**	*	*	*
Quiescent Current	**1.5mA max (0.6mA typ)**	*	*	*
TEMPERATURE				
Operating, Rated Performance	0 to +70°C	*	*	*
Storage	−65°C to +150°C	*	*	*
PACKAGE OPTION[6]	H-08A	*	*	*

NOTES

*Specifications same as AD545AJ.

[1]Open Loop Gain is specified with or without nulling of V_{OS}.

[2]A conservative design would not exceed 500pF of load capacitance.

[3]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[4]Bias Current specifications are guaranteed after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every +10°C.

[5]If it is possible for the input voltage to exceed the supply voltage, a series protection resistor should be added to limit input current to 0.1mA. The input devices can handle overload currents of 0.1mA indefinitely without damage.

[6]For outline information see Package Information section.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final test.

LAYOUT AND CONNECTIONS CONSIDERATIONS

The design of very high impedance measurement systems introduces a new level of problems associated with the reduction of leakage paths and noise pickup.

1. A primary consideration in high impedance system designs is to attempt to place the measuring device as near to the signal source as possible. This will minimize current leakage paths, noise pickup and capacitive loading.
2. The use of guarding techniques is essential to realizing the capability of the low input currents of the AD545A. Guarding is achieved by applying a low impedance bootstrap potential to the outside of the insulation material surrounding the high impedance signal line. This bootstrap potential is held at the same level as that of the high impedance line; therefore, there is no voltage drop across the insulation, and hence, no leakage. The guard will also act as a shield to reduce noise pickup and serves an additional function of reducing the effective capacitance to the input line. The case of the AD545A is brought out separately to Pin 8 so that it can also be connected to the guard potential. This technique virtually eliminates potential leakage paths across the package insulation, provides a noise shield for the sensitive circuitry, and reduces common-mode input capacitance to about 0.8pF. Figure 10 shows a proper printed circuit board layout for input guarding and connecting the case guard. Figures 2 and 3 show guarding connections for typical inverting and noninverting applications. If Pin 8 is not used for guarding, it should be connected to ground or one of the amplifier's power supplies to reduce noise.
3. Printed circuit board layout and construction is critical for achieving low leakage performance. The best performance will be realized by using a teflon IC socket for the AD545A but at least a teflon stand-off should be used for the high-impedance lead. If this is not feasible, the input guarding scheme shown in Figure 10 will minimize leakage as much as possible and should be applied to both sides of the board.

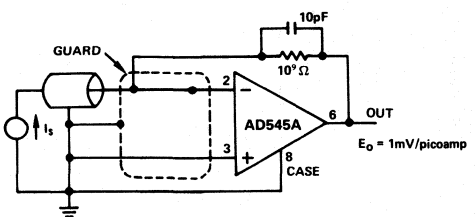


Figure 1. Picoampere Current-to-Voltage Converter Inverting Configuration

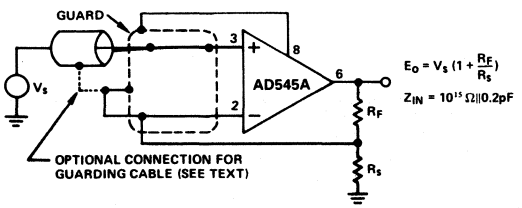


Figure 2. Very High Impedance Noninverting Amplifier

The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on a printed circuit; to minimize noise and leakage, they must be carried in rigid, shielded cables.

APPLICATION NOTES

The AD545A offers one of the lowest input bias currents available in an integrated circuit package. Performing accurate measurements with this device requires careful attention to detail; the notes given here will aid the user in realizing the full measurement potential of the AD545A and extending its performance limits.

1. As with all junction FET input devices, the temperature of the FETs themselves is all-important in determining the input bias currents. Over the operating temperature range, the input bias currents closely follow a characteristic of doubling every 10°C; therefore, every effort should be made to minimize device operating temperature.
2. The heat dissipation can be reduced initially by careful investigation of the application. First, if possible, reduce the required voltage power supplies, since internal power consumption contributes the largest component of self-heating. The effects of this are shown in Figure 7, which shows typical input bias current versus supply voltage.
3. Output loading effects, which are normally ignored, can cause a significant increase in chip temperature and therefore bias current. For example, a 2kΩ load driven at 10V at the output will cause at least an additional 25mW dissipation in the output stage (and some in other stages) over the typical 24mW, thereby at least doubling the effects of self-heating. The results of this form of additional power dissipation are demonstrated in Figure 9, which shows normalized input bias current versus additional power dissipated (it doubles every 10°C); we recommend restricting the load impedance to be at least 10kΩ.
4. Figure 8 shows the AD545A's input currents versus differential input voltage. Input current at either terminal stays below a few hundred fA until one input terminal is forced higher than 1V to 1.5V above the other terminal. Input current limits at 30μA under these conditions.

AD545A–Typical Performance Curves

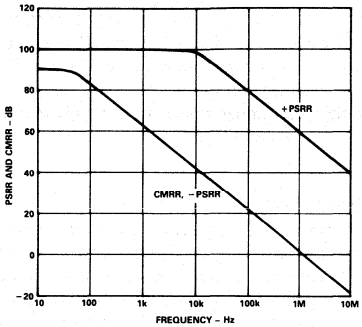


Figure 3. PSRR and CMRR vs. Frequency

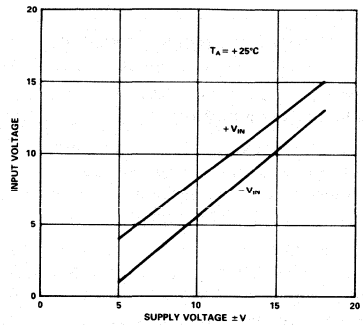


Figure 4. Input Common-Mode Range vs. Supply Voltage

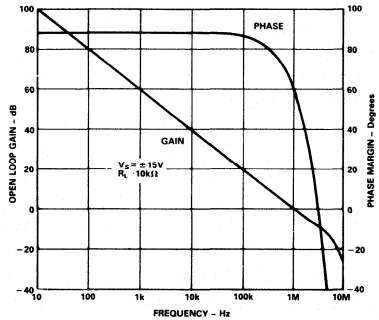


Figure 5. Open Loop Frequency Response

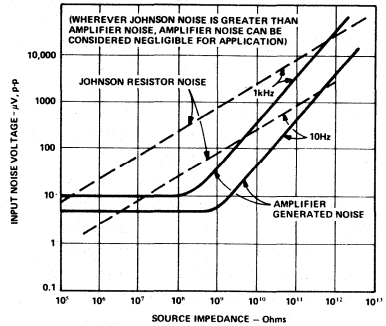


Figure 6. Total Input Noise Voltage vs. Source Impedance and Bandwidth

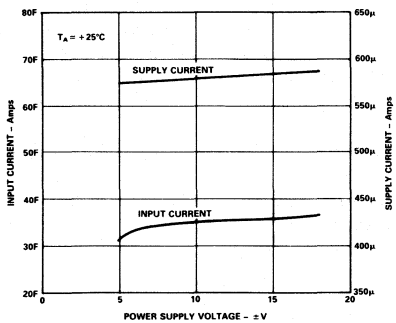


Figure 7. Input Bias Current and Supply Current vs. Supply Voltage

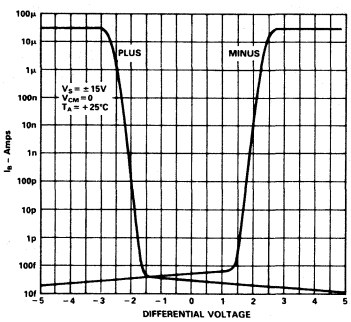


Figure 8. Input Bias Current vs. Differential Input Voltage

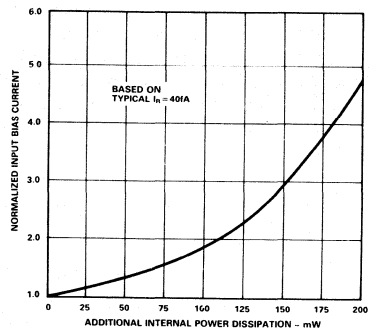


Figure 9. Input Bias Current vs. Additional Power Dissipation

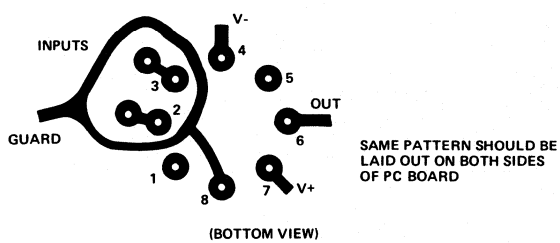


Figure 10. Board Layout for Guarding Inputs with Guarded TO-99 Package

1 pA Monolithic Electrometer Operational Amplifier

AD546*

FEATURES

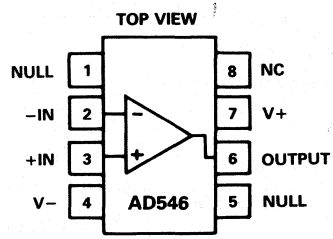
DC PERFORMANCE
- 1 mV max Input Offset Voltage
- Low Offset Drift: 20 μV/°C
- 1 pA max Input Bias Current
- Input Bias Current Guaranteed Over Full Common-Mode Voltage Range

AC PERFORMANCE
- 3 V/μs Slew Rate
- 1 MHz Unity Gain Bandwidth
- Low Input Voltage Noise: 4 μV p–p, 0.1 Hz to 10 Hz
- Available in a Low Cost, 8-Pin Plastic Mini-DIP
- Standard Op Amp Pinout

APPLICATIONS
- Electrometer Amplifiers
- Photodiode Preamps
- pH Electrode Buffers
- Log Ratio Amplifiers

CONNECTION DIAGRAM

8-Pin Plastic
Mini-DIP Package



PRODUCT DESCRIPTION

The AD546 is a monolithic electrometer combining the virtues of low (1 pA) input bias current with the cost effectiveness of a plastic mini-DIP package. Both input offset voltage and input offset voltage drift are laser trimmed, providing very high performance for such a low cost amplifier.

Input bias currents are reduced significantly by using "topgate" JFET technology. The 10^{15} Ω common-mode impedance, resulting from a bootstrapped input stage, insures that input bias current is essentially independent of common-mode voltage variations.

The AD546 is suitable for applications requiring both minimal levels of input bias current and low input offset voltage. Applications for the AD546 include use as a buffer amplifier for current output transducers such as photodiodes and pH probes. It may also be used as a precision integrator or as a low droop rate sample and hold amplifier. The AD546 is pin compatible with standard op amps; its plastic mini-DIP package is ideal for use with automatic insertion equipment.

The AD546 is available in two performance grades, all rated over the 0 to +70°C commercial temperature range, and packaged in an 8-pin plastic mini-DIP.

PRODUCT HIGHLIGHTS

1. The input bias current of the AD546 is specified, 100% tested and guaranteed with the device in the fully warmed-up condition.
2. The input offset voltage of the AD546 is laser trimmed to less than 1 mV (AD546K).
3. The AD546 is packaged in a standard, low cost, 8-pin mini-DIP.
4. A low quiescent supply current of 700 μA minimizes any thermal effects which might degrade input bias current and input offset voltage specifications.

*Covered by Patent No. 4,639,683

AD546—SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD546J Min	AD546J Typ	AD546J Max	AD546K Min	AD546K Typ	AD546K Max	Units
INPUT BIAS CURRENT[1]								
Either Input	V_{CM} = 0 V		0.2	**1**		0.2	**0.5**	pA
Either Input	V_{CM} = ±10 V		0.2	1		0.2	0.5	pA
Either Input @ T_{max}	V_{CM} = 0 V		40			20		pA
Either Input	V_{CM} = ±10 V		40			20		pA
Offset Current	V_{CM} = 0 V		0.17			0.09		pA
Offset Current @ T_{max}	V_{CM} = 0 V		13			7		pA
INPUT OFFSET VOLTAGE[2]								
Initial Offset				**2**			**1**	mV
Offset @ T_{max}				3			2	mV
vs. Temp.			20			20		µV/°C
vs. Supply				**100**			**100**	µV/V
vs. Supply	T_{min}–T_{max}			100			100	µV/V
Long Term Stability			20			20		µV/month
INPUT VOLTAGE NOISE								
	f = 0.1 Hz to 10 Hz		4			4		µV p–p
	f = 10 Hz		90			90		nV/√Hz
	f = 100 Hz		60			60		nV/√Hz
	f = 1 kHz		35			35		nV/√Hz
	f = 10 kHz		35			35		nV/√Hz
INPUT CURRENT NOISE								
	f = 0.1 Hz to 10 Hz		1.3			1.3		fA rms
	f = 1 kHz		0.4			0.4		fA/√Hz
INPUT IMPEDANCE								
Differential	V_{DIFF} = ±1 V		10^{13}‖1			10^{13}‖1		Ω‖pF
Common Mode	V_{CM} = ±10 V		10^{15}‖0.8			10^{15}‖0.8		Ω‖pF
OPEN LOOP GAIN	V_O = ±10 V							
	R_{LOAD} = 10 kΩ	**300**	1000		**300**	1000		V/mV
T_{min}–T_{max}	V_O = ±10 V							
	R_{LOAD} = 10 kΩ	300	800		300	800		V/mV
	V_O = ±10 V							
	R_{LOAD} = 2 kΩ	**100**	250		**100**	250		V/mV
T_{min}–T_{max}	V_O = ±10 V							
	R_{LOAD} = 2 kΩ	80	200		80	200		V/mV
INPUT VOLTAGE RANGE								
Differential[3]			±20			±20		V
Common-Mode Voltage		**−10**		**+10**	**−10**		**+10**	V
Common-Mode Rejection Ratio	V_{CM} = ±10 V	**80**	90		**84**	100		dB
	T_{min} to T_{max}	76	80		76	80		dB
OUTPUT CHARACTERISTICS								
Voltage	R_{LOAD} = 10 kΩ	**−12**		**+12**	**−12**		**+12**	V
	R_{LOAD} = 2 kΩ	**−10**		**+10**	**−10**		**+10**	V
Current	Short Circuit	**15**	20	35	**15**	20	35	mA
Load Capacitance Stability	Gain = +1		4000			4000		pF

Model	Conditions	AD546J Min	AD546J Typ	AD546J Max	AD546K Min	AD546K Typ	AD546K Max	Units
FREQUENCY RESPONSE								
Gain BW, Small Signal	G = −1	0.7	1.0		0.7	1.0		MHz
Full Power Response	V_O = 20 V p-p		50			50		kHz
Slew Rate, Unity Gain	G = −1	2	3		2	3		V/μs
Settling Time	to 0.1%		4.5			4.5		μs
	to 0.01%		5			5		μs
Overload Recovery	50% Overdrive Gain = −1		2			2		μs
POWER SUPPLY								
Rated Performance			±15			±15		V
Operating Range		±5		±18	±5		±18	V
Quiescent Current			0.60	0.7		0.60	0.7	mA
Transistor Count	# of Transistors		50			50		
PACKAGE OPTIONS[4]								
Plastic Mini-DIP (N-8)			AD546JN			AD546KN		

NOTES
[1]Bias current specifications are guaranteed maximum, at either input, after 5 minutes of operation at T_A = +25°C. Bias current increases by a factor of 2.3 for every 10°C rise in temperature.
[2]Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[3]Defined as max continuous voltage between inputs, such that neither exceeds ±10 V from ground.
[4]For outline information see Package Information section.

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation . . . . . 500 mW
Input Voltage[2] . . . . . ±18 V
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range . . . . . −65°C to +125°C
Operating Temperature Range . . . . . 0 to +70°C
Lead Temperature Range
(Soldering 60 seconds) . . . . . 300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

ESD PRECAUTIONS

Charges as high as 4000 V readily accumulate on the human body and test equipment and discharge without detection. Therefore, reasonable ESD precautions are recommended to avoid functional damage or performance degradation. Unused devices should be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' *ESD Prevention Manual*.

AD546—Typical Characteristics (V_S = ±15 V, unless otherwise specified)

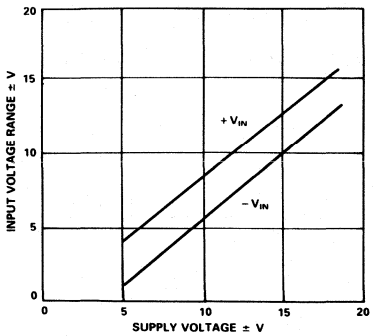


Figure 1. Input Voltage Range vs. Supply Voltage

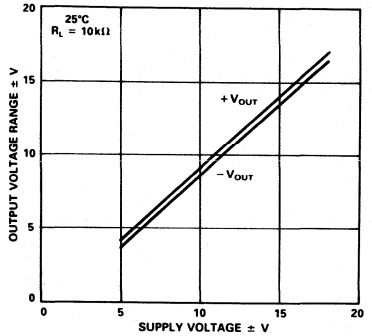


Figure 2. Output Voltage Range vs. Supply Voltage

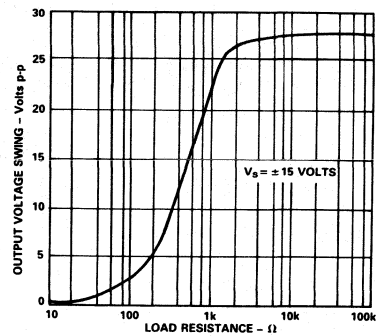


Figure 3. Output Voltage Swing vs. Load Resistance

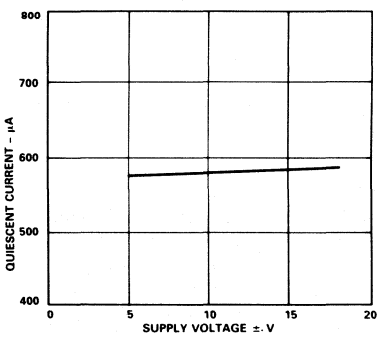


Figure 4. Quiescent Current vs. Supply Voltage

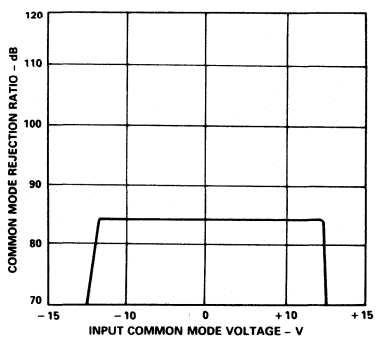


Figure 5. CMRR vs. Input Common-Mode Voltage

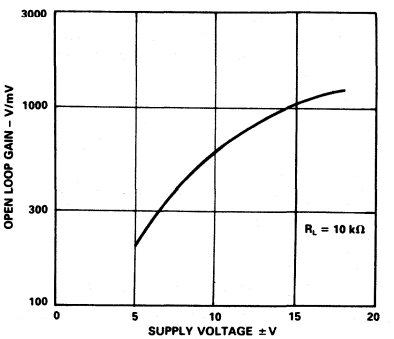


Figure 6. Open Loop Gain vs. Supply Voltage

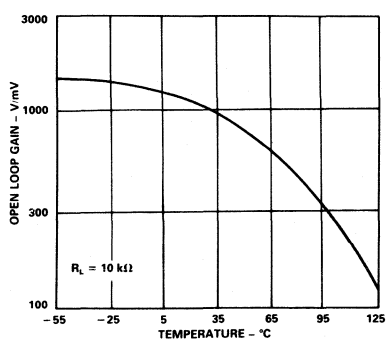


Figure 7. Open Loop Gain vs. Temperature

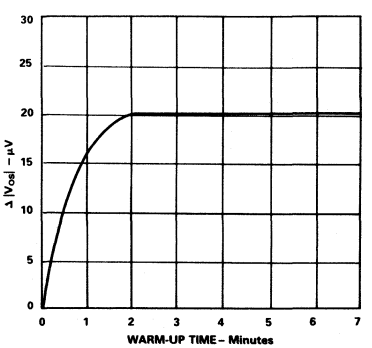


Figure 8. Change in Offset Voltage vs. Warm-Up Time

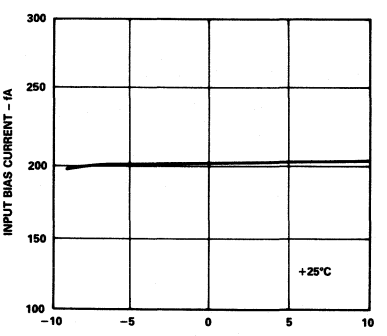


Figure 9. Input Bias Current vs. Common-Mode Voltage

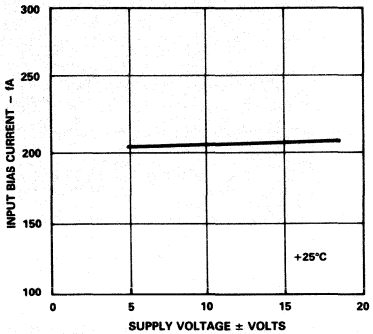


Figure 10. Input Bias Current vs. Supply Voltage

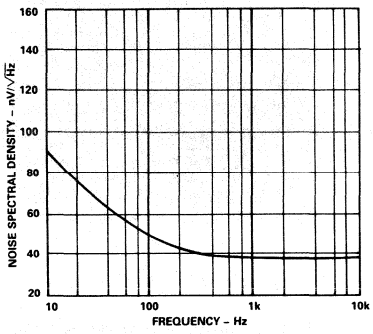


Figure 11. Input Voltage Noise Spectral Density vs. Frequency

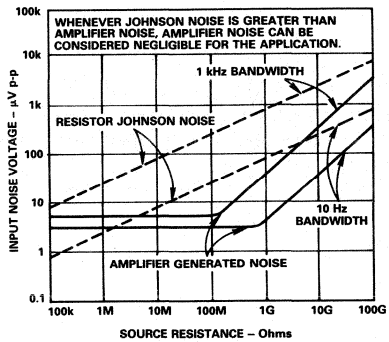


Figure 12. Noise vs. Source Resistance

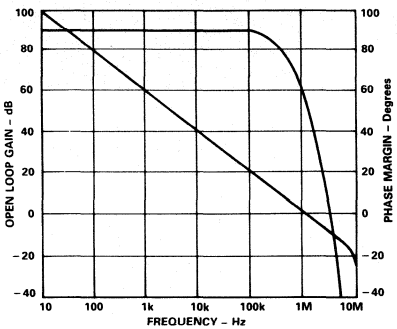


Figure 13. Open Loop Frequency Response

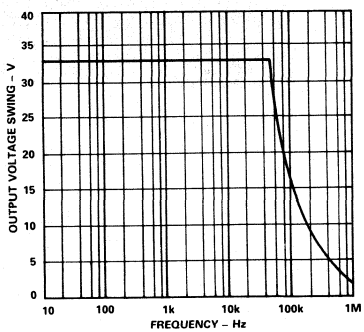


Figure 14. Large Signal Frequency Response

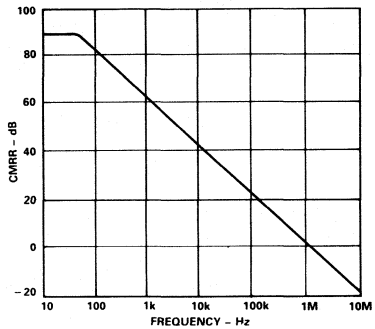


Figure 15. CMRR vs. Frequency

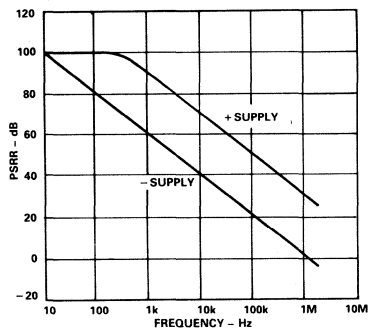


Figure 16. PSRR vs. Frequency

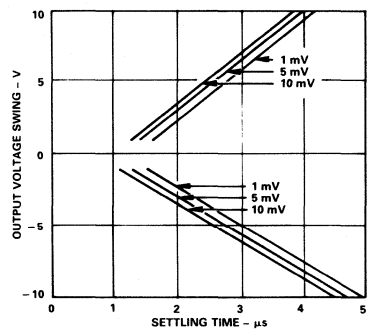


Figure 17. Output Swing and Error Voltage vs. Output Settling Time

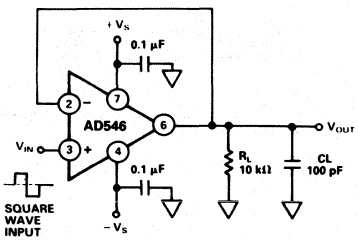


Figure 18. Unity Gain Follower

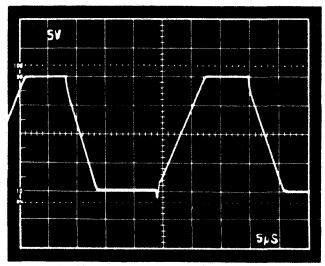


Figure 19. Unity Gain Follower Large Signal Pulse Response

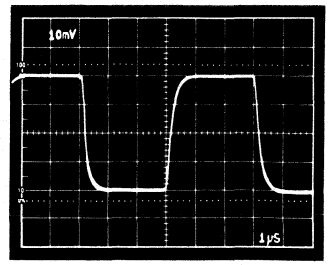


Figure 20. Unity Gain Follower Small Signal Pulse Response

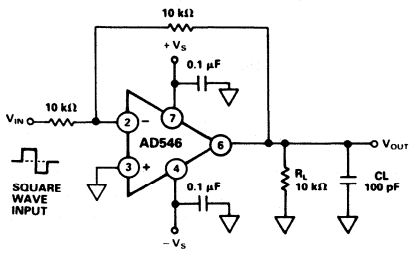


Figure 21. Unity Gain Inverter

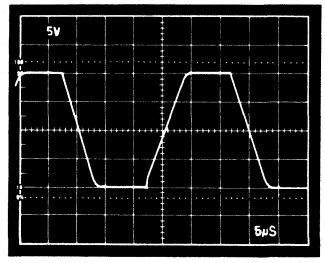


Figure 22. Unity Gain Inverter Large Signal Pulse Response

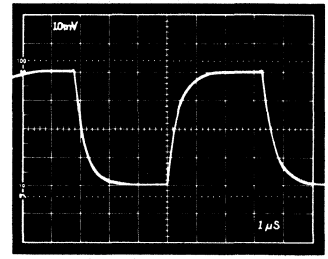


Figure 23. Unity Gain Inverter Small Signal Pulse Response

MINIMIZING INPUT CURRENT

The AD546 is guaranteed to have less than 1 pA max input bias current at room temperature. Careful attention to how the amplifier is used will reduce input currents in actual applications.

The amplifier operating temperature should be kept as low as possible to minimize input current. Like other JFET input amplifiers, the AD546's input current is sensitive to chip temperature, rising by a factor of 2.3 for every 10°C rise. This is illustrated in Figure 24, a plot of AD546 input current versus ambient temperature.

On-chip power dissipation will raise chip operating temperature causing an increase in input bias current. Due to the AD546's low quiescent supply current, chip temperature when the (unloaded) amplifier is operated with 15 V supplies, is less than 3°C higher than ambient. The difference in input current is negligible.

However, heavy output loads can cause a significant increase in chip temperature and a corresponding increase in input current. Maintaining a minimum load resistance of 10 kΩ is recommended. Input current versus additional power dissipation due to output drive current is plotted in Figure 25.

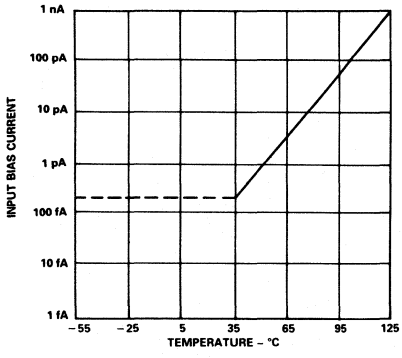


Figure 24. AD546 Input Bias Current vs. Ambient Temperature

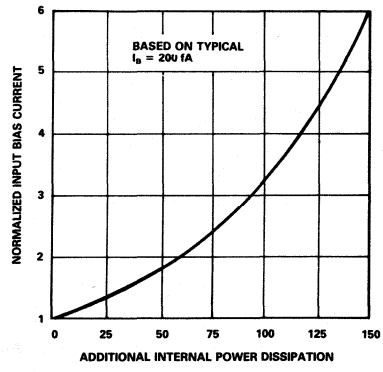


Figure 25. AD546 Input Bias Current vs. Additional Power Dissipation

Circuit Board Notes

The AD546 is designed for through hole mount into PC boards. Maintaining picoampere level resolution in that environment requires a lot of care. Since both the printed circuit board and the amplifier's package have a finite resistance, the voltage difference between the amplifier's input pin and other pins (or traces on the PC board) will cause parasitic currents to flow into (or out of) the signal path (see Figure 26). These currents can easily exceed the 1 pA input current level of the AD546 unless special precautions are taken. Two successful methods for minimizing leakage are guarding the AD546's input lines and maintaining adequate insulation resistance.

The AD546's positive input (Pin 3) is located next to the negative supply voltage pin (Pin 4). The negative input (Pin 2) is next to the balance adjust pin (Pin 1) which is biased at a potential close to the negative supply voltage. The layouts shown in Figures 27a and 27b for the inverter and follower connections will guard against the effects of low surface resistance of the board. Note that the guard traces should be placed on *both* sides of the board. In addition the input trace should be guarded on both of its edges along its entire length.

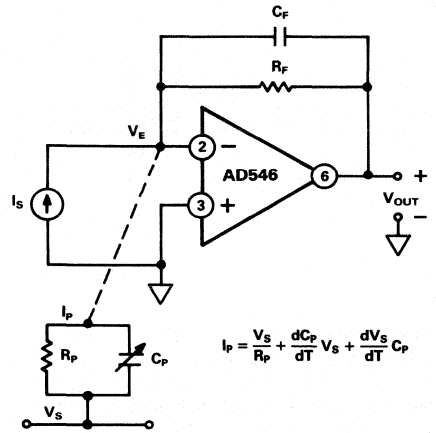
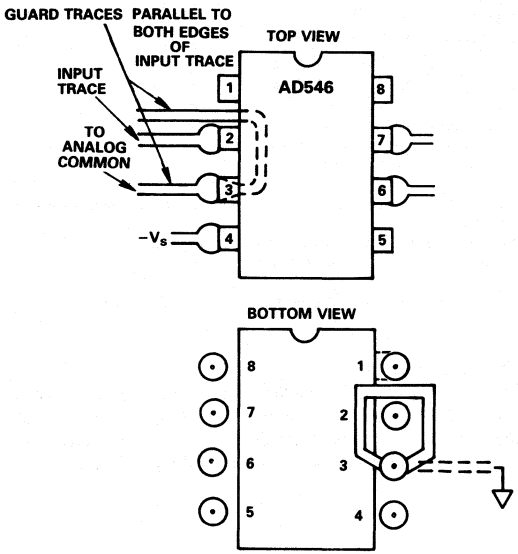


Figure 26. Sources of Parasitic Leakage Currents



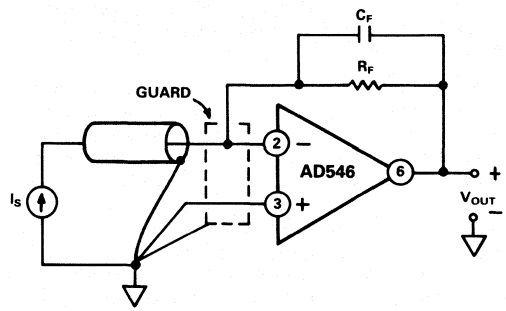
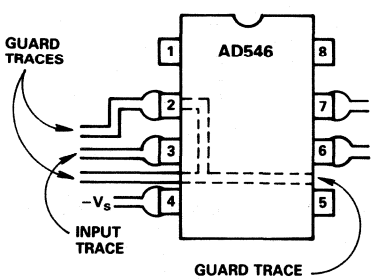


Figure 27a. Guarding Scheme—Inverter



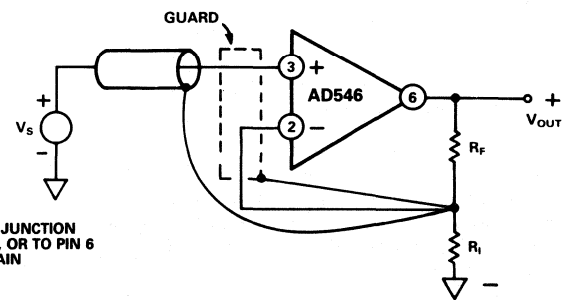


Figure 27b. Guarding Scheme—Follower

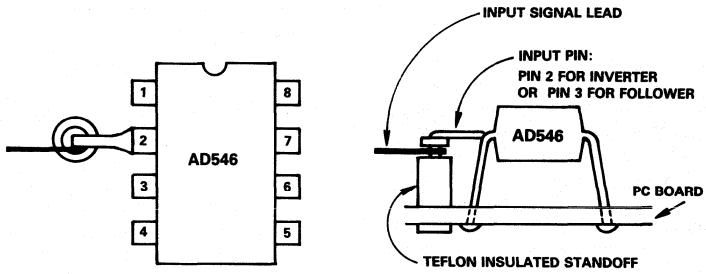


Figure 28. Input Pin to Insulating Standoff

Leakage through the bulk of the circuit board will still occur with the guarding schemes shown in Figures 27a and 27b. Standard "G10" type printed circuit board material may not have high enough volume resistivity to hold leakages at the sub-picoampere level particularly under high humidity conditions. One option that eliminates all effects of board resistance is shown in Figure 28. The AD546's sensitive input pin (either Pin 2 when connected as an inverter, or Pin 3 when connected as a follower) is bent up and soldered directly to a Teflon* insulated standoff. Both the signal input and feedback component leads must also be insulated from the circuit board by Teflon standoffs or low-leakage shielded cable.

Contaminants such as solder flux on the board's surface and on the amplifier's package can greatly reduce the insulation resistance between the input pin and those traces with supply or signal voltages. Both the package and the board must be kept clean and dry. An effective cleaning procedure is to first swab the surface with high grade isopropyl alcohol, then rinse it with deionized water and, finally, bake it at 80°C for 1 hour. Note that if either polystyrene or polypropylene capacitors are used on the printed circuit board, a baking temperature of 70°C is safer, since both of these plastic compounds begin to melt at approximately +85°C.

Other guidelines include making the circuit layout as compact as possible and reducing the length of input lines. Keeping circuit board components rigid and minimizing vibration will reduce triboelectric and piezoelectric effects. All precision high impedance circuitry requires shielding from electrical noise and interference. For example, a ground plane should be used under all high value (i.e., greater than 1 MΩ) feedback resistors. In some cases, a shield placed over the resistors, or even the entire amplifier, may be needed to minimize electrical interference originating from other circuits. Referring to the equation in Figure 26, this coupling can take place in either, or both, of two different forms—coupling via time varying fields:

$$\frac{dV}{dT} C_P$$

or by injection of parasitic currents by changes in capacitance due to mechanical vibration:

$$\frac{dCp}{dt} V$$

Both proper shielding and rigid mechanical mounting of components help minimize error currents from both of these sources. Table I lists various insulators and their properties.

Material[1]	Volume Resistivity (Ω–CM)	Minimal Triboelectric Effects	Minimal Piezoelectric Effects	Resistance to Water Absorption
Teflon*	10^{17}–10^{18}	W	W	G
Kel-F**	10^{17}–10^{18}	W	M	G
Sapphire	10^{16}–10^{18}	M	G	G
Polyethylene	10^{14}–10^{18}	M	G	M
Polystyrene	10^{12}–10^{18}	W	M	M
Ceramic	10^{12}–10^{14}	W	M	W
Glass Epoxy	10^{10}–10^{17}	W	M	W
PVC	10^{10}–10^{15}	G	M	G
Phenolic	10^{5} –10^{12}	W	G	W

G–Good with Regard to Property
M–Moderate with Regard to Property
W–Weak with Regard to Property

[1]*Electronic Measurements*, pp.15–17, Keithley Instruments, Inc., Cleveland, Ohio, 1977.
*Teflon is a registered trademark of E.I. DuPont Co.
**Kel-F is a registered trademark of 3-M Company.

Table I. Insulating Materials and Characteristics

OFFSET NULLING

The AD546's input offset voltage can be nulled by using balance Pins 1 and 5, as shown in Figure 29. Nulling the input offset voltage in this fashion will introduce an added input offset voltage drift component of 2.4 μV/°C per millivolt of nulled offset.

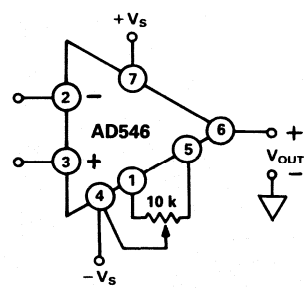


Figure 29. Standard Offset Null Circuit

The circuit in Figure 30 can be used when the amplifier is used as an inverter. This method introduces a small voltage in series with the amplifier's positive input terminal. The amplifier's input offset voltage drift with temperature is not affected. However, variation of the power supply voltages will cause offset shifts.

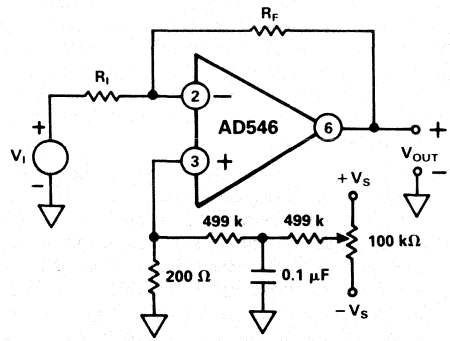


Figure 30. Alternate Offset Null Circuit for Inverter

AC RESPONSE WITH HIGH VALUE SOURCE AND FEEDBACK RESISTANCE

Source and feedback resistances greater than 100 kΩ will magnify the effect of input capacitances (stray and inherent to the AD546) on the ac behavior of the circuit. The effects of common-mode and differential input capacitances should be taken into account since the circuit's bandwidth and stability can be adversely affected.

In a follower, the source resistance, R_S, and input common-mode capacitance, C_S (including capacitance due to board and capacitance inherent to the AD546), form a pole that limits circuit bandwidth to $1/2\pi R_S C_S$. Figure 31 shows the follower pulse response from a 1 MΩ source resistance with the amplifier's input pin isolated from the board, only the effect of the AD546's input common-mode capacitance is seen.

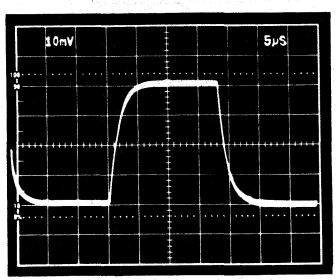


Figure 31. Follower Pulse Response from 1 MΩ Source Resistance

In an inverting configuration, the differential input capacitance forms a pole in the circuit's loop transmission. This can create peaking in the ac response and possible instability. A feedback capacitance can be used to stabilize the circuit. The inverter pulse response with R_F and R_S equal to 1 MΩ, and the input pin isolated from the board appears in Figure 32. Figure 33 shows the response of the same circuit with a 1 pF feedback capacitance. Typical differential input capacitance for the AD546 is 1 pF.

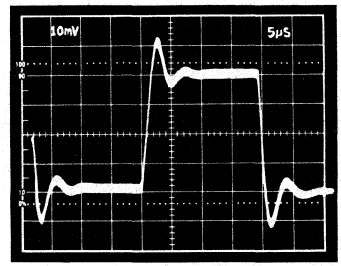


Figure 32. Inverter Pulse Response with 1 MΩ Source and Feedback Resistance

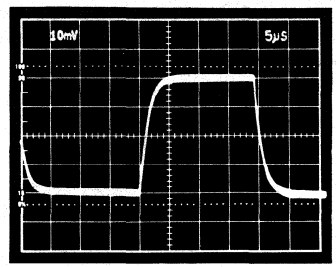


Figure 33. Inverter Pulse Response with 1 MΩ Source and Feedback Resistance, 1 pF Feedback Capacitance

COMMON-MODE INPUT VOLTAGE OVERLOAD

The rated common-mode input voltage range of the AD546 is from 3 V less than the positive supply voltage to 5 V greater than the negative supply voltage. Exceeding this range will degrade the amplifier's CMRR. Driving the common-mode voltage above the positive supply will cause the amplifier's output to saturate at the upper limit of output voltage. Recovery time is typically 2 μs after the input has been returned to within the normal operating range. Driving the input common-mode voltage within 1 V of the negative supply causes phase reversal of the output signal. In this case, normal operation is typically resumed within 0.5 ms of the input voltage returning within range.

DIFFERENTIAL INPUT VOLTAGE OVERLOAD

A plot of the AD546's input current versus differential input voltage (defined as $V_{IN}+ - V_{IN}-$) appears in Figure 34. The

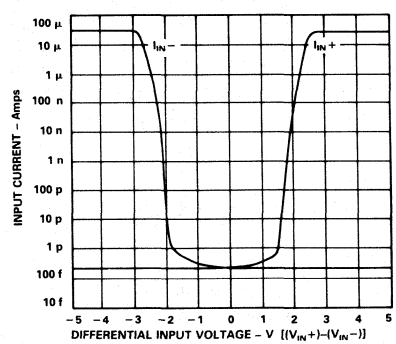


Figure 34. Input Current vs. Differential Input Voltage

input current at either terminal stays below a few hundred femtoamps until one input terminal is forced higher than 1 to 1.5 V above the other terminal. Under these conditions, the input current limits at 30 μA.

INPUT PROTECTION

The AD546 safely handles any input voltage within the supply voltage range. Subjecting the input terminals to voltages beyond the power supply can destroy the device or cause shifts in input current or offset voltage if the amplifier is not protected.

A protection scheme for the amplifier as an inverter is shown in Figure 35. The protection resistor, R_P, is chosen to limit the current through the inverting input to 1 mA for expected transient (less than 1 second) overvoltage conditions, or to 100 μA for a continuous overload. Since R_P is inside the feedback loop, and is much lower in value than the amplifier's input resistance, it does not affect the inverter's dc gain. However, the Johnson noise of the resistor will add root sum of squares to the amplifier's input noise.

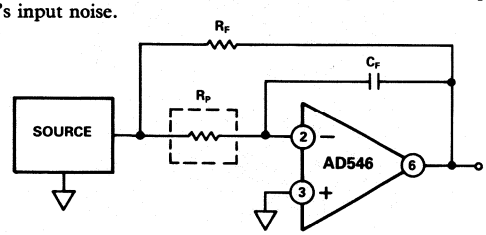


Figure 35. Inverter with Input Current Limit

In the corresponding version of this scheme for a follower, shown in Figure 36, R_P and the capacitance at the positive input terminal will produce a pole in the signal frequency response at a $f = 1/2\pi RC$. Again, the Johnson noise of R_P will add to the amplifier's input voltage noise.

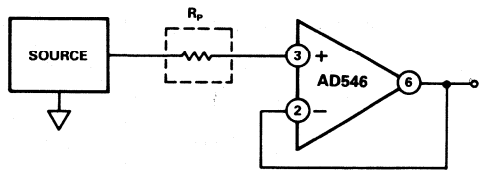


Figure 36. Follower with Input Current Limit

Figure 37 is a schematic of the AD546 as an inverter with an input voltage clamp. Bootstrapping the clamp diodes at the inverting input minimizes the voltage across the clamps and keeps the leakage due to the diodes low. Low leakage diodes (less than 1 pA), such as the FD333's should be used, and should be shielded from light to keep photocurrents from being generated. Even with these precautions, the diodes will measurably increase the input current and capacitance.

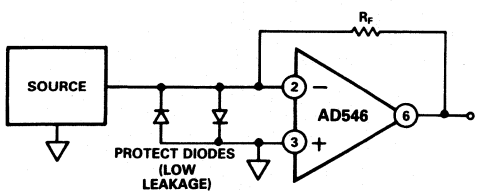


Figure 37. Input Voltage Clamp with Diodes

In order to achieve the low input bias currents of the AD546, it is not possible to use the same on-chip protection as used in other Analog Devices op amps. This makes the AD546 sensitive to handling and precautions should be taken to minimize ESD exposure whenever possible.

MEASURING ELECTROMETER LEAKAGE CURRENTS

There are a number of methods used to test electrometer leakage currents, including current integration and direct current to voltage conversion. Regardless of the method used, board and interconnect cleanliness, proper choice of insulating materials (such as Teflon or Kel-F), correct guarding and shielding techniques and care in physical layout are essential for making accurate leakage measurements.

Figure 38 is a schematic of the sample and difference circuit which is useful for measuring the leakage currents of the AD546 and other electrometer amplifiers. The circuit uses two AD549 electrometer amplifiers (A and B) as current to voltage converters with high value (10^{10} Ω) sense resistors (RSa and RSb). R1 and R2 provide for an overall circuit sensitivity of 10 fA/mV (10 pA full scale). C_C and C_F provide noise suppression and loop compensation. C_C should be a low leakage polystyrene capacitor. An ultralow-leakage Kel-F test socket is used for contacting the device under test. Rigid Teflon coaxial cable is used to make connections to all high impedance nodes. The use of rigid coax affords immunity to error induced by mechanical vibration and provides an outer conductor for shielding. The entire circuit is enclosed in a grounded metal box.

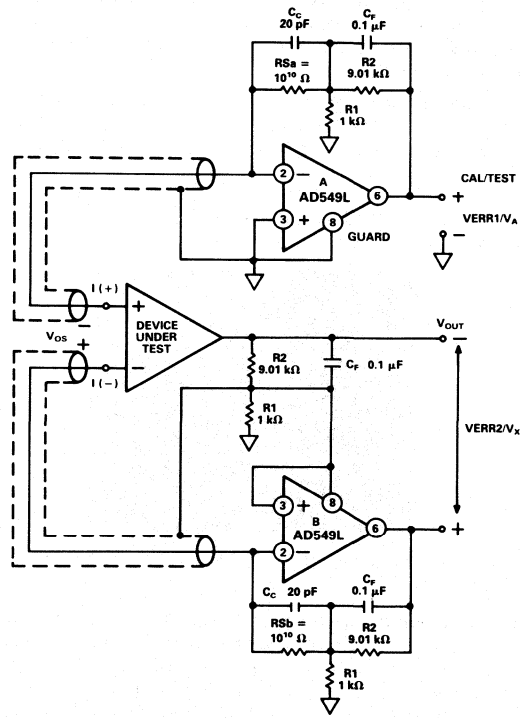


Figure 38. Sample and Difference Circuit for Measuring Electrometer Leakage Currents

The test apparatus is calibrated without a device under test present. A five minute stabilization period after the power is turned on is required. First, V_{ERR1} and V_{ERR2} are measured. These voltages are the errors caused by offset voltages and leakage currents of the current to voltage converters.

$$V_{ERR1} = 10\,(V_{OS}A - I_BA \times RSa)$$
$$V_{ERR2} = 10\,(V_{OS}B - I_BB \times RSb)$$

Once measured, these errors are subtracted from the readings taken with a device under test present. Amplifier B closes the feedback loop to the device under test, in addition to providing current to voltage conversion. The offset error of the device under test appears as a common-mode signal and does not affect the test measurement. As a result, only the leakage current of the device under test is measured.

$$V_A - V_{ERR1} = 10[RSa \times I_B(+)]$$
$$V_X - V_{ERR2} = 10[RSb \times I_B(-)]$$

Although a series of devices can be tested after only one calibration measurement, calibration should be updated periodically to compensate for any thermal drift of the current-to-voltage converters or changes in the ambient environment. Laboratory results have shown that repeatable measurements within 10 fA can be realized when this apparatus is properly implemented. These results are achieved in part by the design of the circuit, which eliminates relays and other parasitic leakage paths in the high impedance signal lines, and in part by the inherent cancellation of errors through the calibration and measurement procedure.

PHOTODIODE INTERFACE

The AD546's 1 pA current and low input offset voltage make it a good choice for very sensitive photodiode preamps (Figure 39). The photodiode develops a signal current, I_S, equal to:

$$I_S = R \times P$$

where P is light power incident on the diode's surface in watts and R is the photodiode responsivity in amps/watt. R_F converts the signal current to an output voltage:

$$V_{OUT} = R_F \times I_S$$

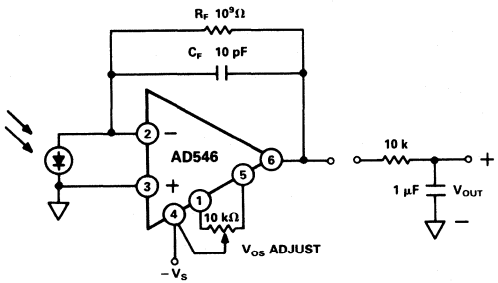


Figure 39. Photodiode Preamp

DC error sources and an equivalent circuit for a small area (0.2 mm square) photodiode are indicated in Figure 40.

Input current, I_B, will contribute an output voltage error, V_{E1}, proportional to the feedback resistance:

$$V_{E1} = I_B \times R_F$$

The op amp's input voltage offset will cause an error current through the photodiode's shunt resistance, R_S:

$$I = V_{OS}/R_S$$

The error current will result in an error voltage (V_{E2}) at the amplifier's output equal to:

$$V_{E2} = (1+R_F/R_S)\,V_{OS}$$

Given typical values of photodiode shunt resistance (on the order of $10^9\ \Omega$), R_F/R_S can be greater than one, especially if a large feedback resistance is used. Also, R_F/R_S will increase with temperature, as photodiode shunt resistance typically drops by a factor of two for every 10°C rise in temperature. An op amp with low offset voltage and low drift helps maintain accuracy.

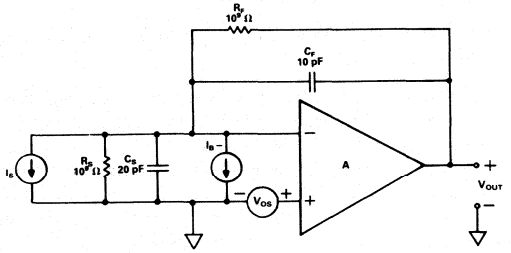


Figure 40. Photodiode Preamp DC Error Sources

Photodiode Preamp Noise

Noise limits the signal resolution obtainable with the preamp. The output voltage noise divided by the feedback resistance is the minimum current signal that can be detected. This minimum detectable current divided by the responsivity of the photodiode represents the lowest light power that can be detected by the preamp.

Noise sources associated with the photodiode, amplifier, and feedback resistance are shown in Figure 41; Figure 42 is the voltage spectral density versus frequency plot of each of the noise source's contribution to the output voltage noise (circuit parameters in Figure 40 are assumed). Each noise source's rms contribution to the total output voltage noise is obtained by integrating the square of its spectral density function over frequency. The rms value of the output voltage noise is the square root of the sum of all contributions. Minimizing the total area under these curves will optimize the preamplifier's resolution for a given bandwidth.

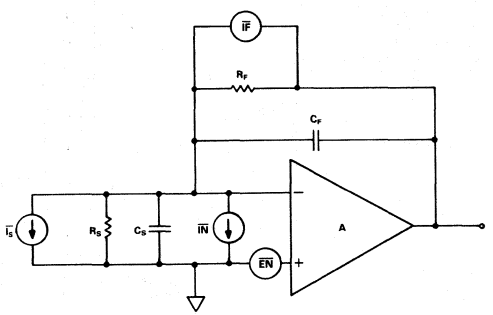


Figure 41. Photodiode Preamp Noise Sources

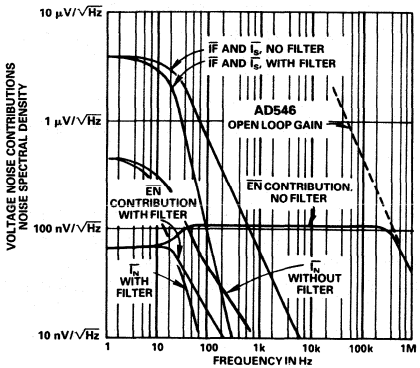


Figure 42. Photodiode Preamp Noise Sources' Spectral Density vs. Frequency

The photodiode preamp in Figure 39 can detect a signal current of 26 fA rms at a bandwidth of 16 Hz, which assuming a photodiode responsivity of 0.5 A/W, translates to a 52 fW rms minimum detectable power. The photodiode used has a high source resistance and low junction capacitance. C_F sets the signal bandwidth with R_F and also limits the "peak" in the noise gain that multiplies the op amp's input voltage noise contribution. A single pole filter at the amplifier's output limits the op amp's output voltage noise bandwidth to 26 Hz, a frequency comparable to the signal bandwidth. This greatly improves the preamplifier's signal to noise ratio (in this case, by a factor of three).

Photodiode Array Processor

The AD546 is a cost effective preamp for multichannel applications, such as amplifying signals from photo diode arrays, as illustrated in Figure 43. An AD546 preamp converts each of the diodes' output currents to a voltage. An 8 to 1 multiplexer switches a particular preamp output to the input of an AD1380 16-bit sampling ADC. The output of the ADC can be displayed or put onto a databus. Additional preamps and muxes can be added to handle larger arrays. Layout of multichannel circuits is critical. Refer to "PC board notes" for guidance.

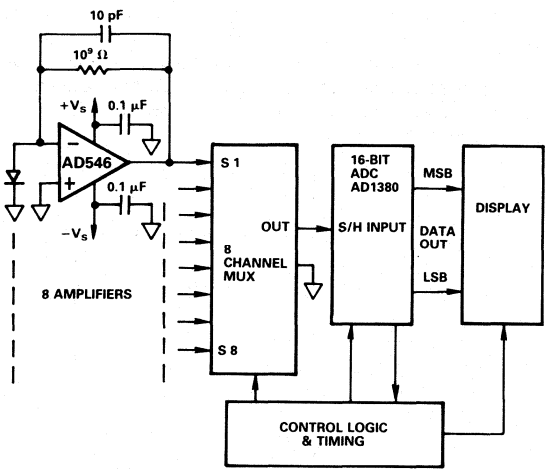


Figure 43. Photodiode Array Processor

pH PROBE AMPLIFIER

A pH probe can be modeled as a mV-level voltage source with a series source resistance dependent upon the electrode's composition and configuration. The glass bulb resistance of a typical pH electrode pair falls between 10^6 and 10^9 Ω. It is therefore important to select an amplifier with low enough input currents such that the voltage drop produced by the amplifier's input bias current and the electrode resistance does not become an appreciable percentage of a pH unit.

The circuit in Figure 44 illustrates the use of the AD546 as a pH probe amplifier. As with other electrometer applications, the use of guarding, shielding, Teflon standoffs, etc., is a must in order to capitalize on the AD546's low input current. If an AD546J (1 pA max input current) is used, the error contributed by input current will be held below 10 mV for pH electrode source impedances up to 10^9 Ω. Input offset voltage (which can be trimmed) will be below 2 mV. Refer to AD549 data sheet for temperature compensated pH probe amplifier circuit.

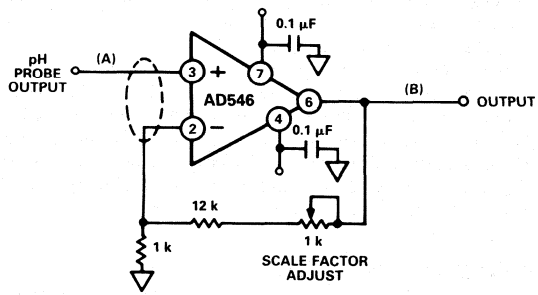


Figure 44. pH Probe Amplifier

ANALOG DEVICES

Precision, Low Power BiFET Op Amp

AD548

FEATURES

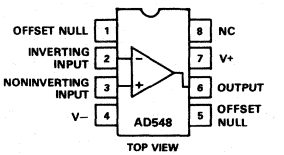
Enhanced Replacement for LF441 and TL061
DC Performance:
- **200μA max Quiescent Current**
- **10pA max Bias Current, Warmed Up (AD548C)**
- **250μV max Offset Voltage (AD548C)**
- **2μV/°C max Drift (AD548C)**
- **2μV p-p Noise, 0.1 to 10Hz**

AC Performance:
- **1.8V/μs Slew Rate**
- **1MHz Unity Gain Bandwidth**

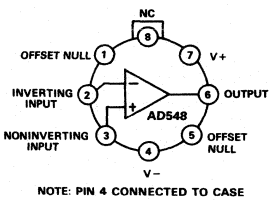
Available in Plastic, Hermetic Cerdip and Hermetic Metal Can Packages and in Chip Form
Available in Tape and Reel in Accordance with EIA-481A Standard
MIL-STD-883B Parts Available
Dual Version Available: AD648
Surface Mount (SOIC) Package Available

CONNECTION DIAGRAMS

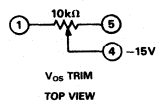
Plastic Mini-DIP (N) Package,
Cerdip (Q) Package
and
SOIC (R) Package



TO-99
(H) Package



NOTE: PIN 4 CONNECTED TO CASE



PRODUCT DESCRIPTION

The AD548 is a low power, precision monolithic operational amplifier. It offers both low bias current (10pA max, warmed up) and low quiescent current (200μA max) and is fabricated with ion-implanted FET and laser wafer trimming technologies. Input bias current is guaranteed over the AD548's entire common-mode voltage range.

The economical J grade has a maximum guaranteed input offset voltage of less than 2mV and an input offset voltage drift of less than 20μV/°C. The C grade reduces input offset voltage to less than 0.25mV and offset voltage drift to less than 2μV/°C. This level of dc precision is achieved utilizing Analog's laser wafer drift trimming process. The combination of low quiescent current and low offset voltage drift minimizes changes in input offset voltage due to self-heating effects. Five additional grades are offered over the commercial, industrial and military temperature ranges.

The AD548 is recommended for any dual supply op amp application requiring low power and excellent dc and ac performance. In applications such as battery-powered, precision instrument front ends and CMOS DAC buffers, the AD548's excellent combination of low input offset voltage and drift, low bias current and low 1/f noise reduces output errors. High common-mode rejection (86dB, min on the "C" grade) and high open-loop gain ensures better than 12-bit linearity in high impedance, buffer applications.

The AD548 is pinned out in a standard op amp configuration and is available in seven performance grades. The AD548J and AD548K are rated over the commercial temperature range of 0 to +70°C. The AD548A, AD548B and AD548C are rated over the industrial temperature range of −40°C to +85°C. The AD548S and AD548T are rated over the military temperature range of −55°C to +125°C and are available processed to MIL-STD-883B, Rev. C.

Extended reliability PLUS screening is available for parts specified over the commercial and industrial temperature ranges. PLUS screening includes 168-hour burn-in, as well as other environmental and physical tests.

The AD548 is available in an 8-pin plastic mini-DIP, cerdip, TO-99 metal can, surface mount (SOIC), or in chip form.

PRODUCT HIGHLIGHTS

1. A combination of low supply current, excellent dc and ac performance and low drift makes the AD548 the ideal op amp for high-performance, low-power applications.
2. The AD548 is pin compatible with industry standard op amps such as the LF441, TL061, and AD542, enabling designers to improve performance while achieving a reduction in power dissipation of up to 85%.
3. Guaranteed low input offset voltage (2mV max) and drift (20μV/°C max) for the AD548J are achieved utilizing Analog Devices' laser drift trimming technology, eliminating the need for external trimming.
4. Analog Devices specifies each device in the warmed-up condition, insuring that the device will meet its published specifications in actual use.
5. A dual version, the AD648 is also available.
6. Enhanced replacement for LF441 and TL061.

AD548 — SPECIFICATIONS (@ +25°C and V_S = ±15V dc, unless otherwise noted)

Model	AD548J/A/S			AD548K/B/T			AD548C			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
INPUT OFFSET VOLTAGE[1]										
Initial Offset		0.75	**2.0**		0.3	**0.5**		0.10	**0.25**	mV
T_{min} to T_{max}			**3.0/3.0/3.0**			**0.7/0.8/1.0**			**0.4**	mV
vs. Temp.			20			5			**2.0**	µV/°C
vs. Supply	**80**			**86**			**86**			dB
vs. Supply, T_{min} to T_{max}	**76/76/76**			**80**			**80**			dB
Long-Term Offset Stability		15			15			15		µV/month
INPUT BIAS CURRENT										
Either Input[2], V_{CM} = 0		5	**20**		3	**10**		3	**10**	pA
Either Input[2] at T_{max}, V_{CM} = 0			0.45/1.3/20			0.25/0.65/10			0.65	nA
Max Input Bias Current Over Common-Mode Voltage Range			**30**			**15**			**15**	pA
Offset Current, V_{CM} = 0		5	**10**		2	**5**		2	**5**	pA
Offset Current at T_{max}			0.25/0.65/10			0.15/0.35/5			0.35	nA
INPUT IMPEDANCE										
Differential		$1 \times 10^{12} \| 3$			$1 \times 10^{12} \| 3$			$1 \times 10^{12} \| 3$		Ω‖pF
Common Mode		$3 \times 10^{12} \| 3$			$3 \times 10^{12} \| 3$			$3 \times 10^{12} \| 3$		Ω‖pF
INPUT VOLTAGE RANGE										
Differential[3]		±20			±20			±20		V
Common Mode	**±11**	±12		**±11**	±12		**±11**	±12		V
Common-Mode Rejection										
V_{CM} = ±10V	**76**	90		**82**	92		**86**	98		dB
T_{min} to T_{max}	**76/76/76**	90		**82**	92		**86**	98		dB
V_{CM} = ±11V	**70**	84		**76**	86		**76**	90		dB
T_{min} to T_{max}	**70/70/70**	84		**76**	86		**76**	90		dB
INPUT VOLTAGE NOISE										
Voltage 0.1Hz to 10Hz		2			2			2	**4.0**	µV p-p
f = 10Hz		80			80			80		nV/√Hz
f = 100Hz		40			40			40		nV/√Hz
f = 1kHz		30			30			30		nV/√Hz
f = 10kHz		30			30			30		nV/√Hz
INPUT CURRENT NOISE										
f = 1kHz		1.8			1.8			1.8		fA/√Hz
FREQUENCY RESPONSE										
Unity Gain, Small Signal	0.8	1.0		0.8	1.0		0.8	1.0		MHz
Full Power Response		30			30			30		kHz
Slew Rate, Unity Gain	**1.0**	1.8		**1.0**	1.8		**1.0**	1.8		V/µs
Settling Time to ±0.01%		8			8			8		µs
OPEN LOOP GAIN										
V_O = ±10V, $R_L \geq 10k\Omega$	**300**	1000		**300**	1000		**300**	1000		V/mV
T_{min} to T_{max}, $R_L \geq 10k\Omega$	**300/300/300**	700		**300**	700		**300**	700		V/mV
V_O = ±10V, $R_L \geq 5k\Omega$	**150**	500		**150**	500		**150**	500		V/mV
T_{min} to T_{max}, $R_L \geq 5k\Omega$	**150/150/150**	300		**150**	300		**150**	300		V/mV
OUTPUT CHARACTERISTICS										
Voltage @ $R_L \geq 10k\Omega$,	**±12**	±13		**±12**	±13		**±12**	±13		V
T_{min} to T_{max}	±12/±12/**±12**			**±12**			**±12**			
Voltage @ $R_L \geq 5k\Omega$,	**±11**	±12.3		**±11**	±12.3		**±11**	±12.3		V
T_{min} to T_{max}	±11/±11/**±11**			**±11**			**±11**			
Short Circuit Current		15			15			15		mA
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating Range	**±4.5**		**±18**	**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current		170	**200**		170	**200**		170	**200**	µA
TEMPERATURE RANGE										
Operating, Rated Performance										
Commercial (0 to +70°C)		AD548J			AD548K					
Industrial (−40°C to +85°C)		AD548A			AD548B			AD548C		
Military (−55°C to +125°C)		AD548S			AD548T					
PACKAGE OPTIONS[4]										
Plastic (N-8)	AD548JN			AD548KN						
Cerdip (Q-8)	AD548AQ, AD548SQ			AD548BQ, AD548TQ			AD548CQ			
Metal Can (H-08A)	AD548AH, AD548SH			AD548BH, AD548TH			AD548CH			
SOIC (R-8)	AD548AR, AD548JR			AD548BR						
Tape and Reel	AD548AR-REEL, AD548JR-REEL			AD548BR-REEL						
J and S Chips Also Available	AD548J CHIPS, AD548S CHIPS									

NOTES

[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperature, the current doubles every 10°C.

[3]Defined as voltages between inputs, such that neither exceeds ±10V from ground.

[4]For outline information see Package Information section.

Specifications subject to change without notice.

Specifications in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18V
Internal Power Dissipation[2]	500mW
Input Voltage[3]	±18V
Output Short Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range (Q, H)	−65°C to +150°C
(N, R)	−65°C to +125°C
Operating Temperature Range	
AD548J/K	0 to +70°C
AD548A/B/C	−40°C to +85°C
AD548S/T	−55°C to +125°C
Lead Temperature Range (Soldering 60sec)	300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Thermal Characteristics

8-Pin SOIC Package: $\theta_{JA} = 160°C/W$, $\theta_{JC} = 42°C/W$

8-Pin Plastic Package: $\theta_{JA} = 90°C/W$

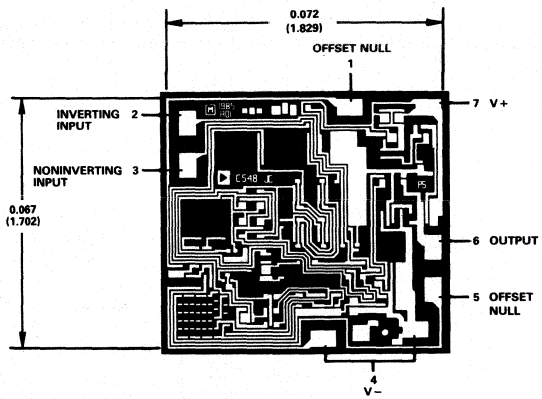
8-Pin Cerdip Package: $\theta_{JC} = 22°C/W$, $\theta_{JA} = 110°C/W$

8-Pin Metal Can Package: $\theta_{JC} = 65°C/W$, $\theta_{JA} = 150°C/W$

[3]For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



2

Typical Characteristics

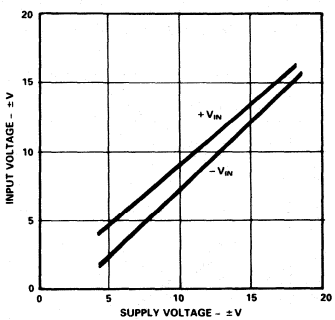


Figure 1. Input Voltage Range vs. Supply Voltage

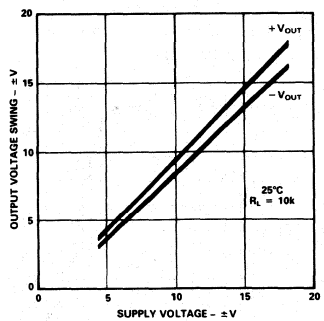


Figure 2. Output Voltage Swing vs. Supply Voltage

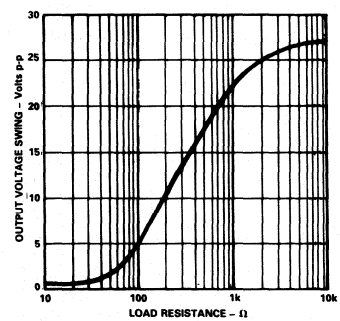


Figure 3. Output Voltage Swing vs. Load Resistance

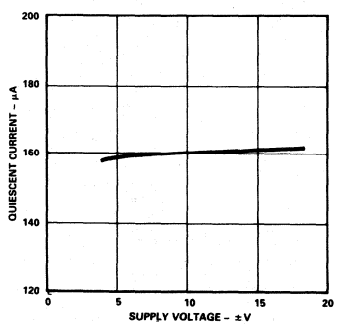


Figure 4. Quiescent Current vs. Supply Voltage

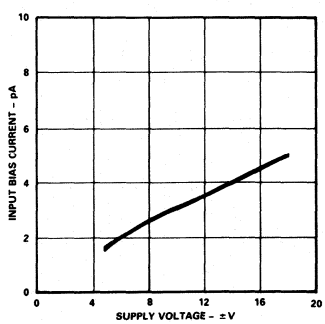


Figure 5. Input Bias Current vs. Supply Voltage

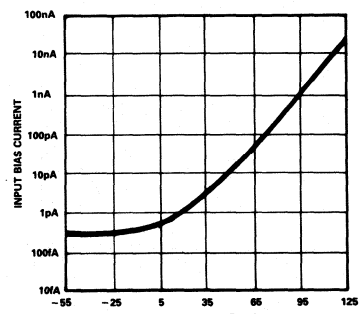


Figure 6. Input Bias Current vs. Temperature

AD548—Typical Characteristics

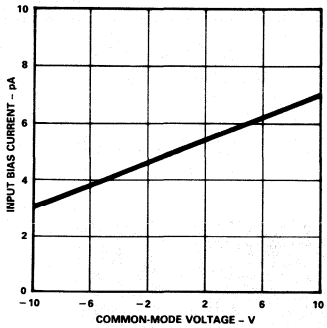


Figure 7. Input Bias Current vs. Common-Mode Voltage

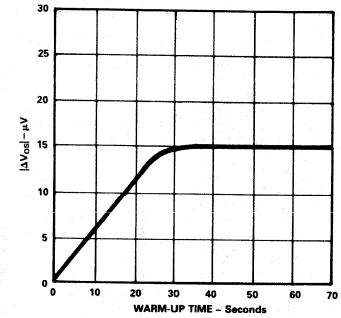


Figure 8. Change in Offset Voltage vs. Warm-Up Time

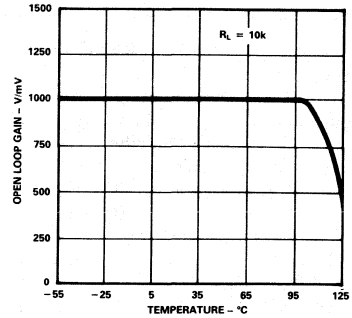


Figure 9. Open Loop Gain vs. Temperature

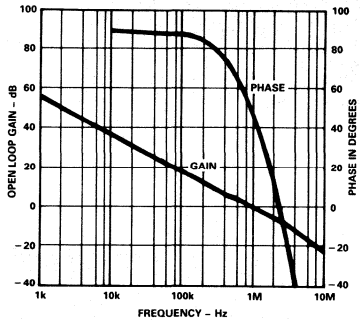


Figure 10. Open Loop Frequency Response

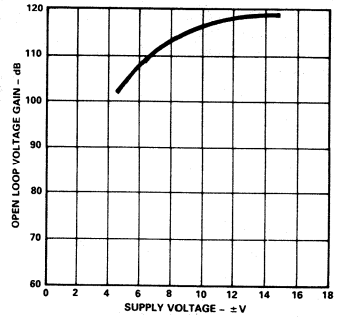


Figure 11. Open Loop Voltage Gain vs. Supply Voltage

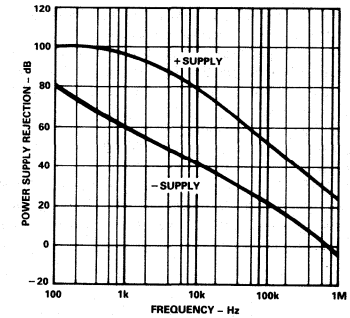


Figure 12. PSRR vs. Frequency

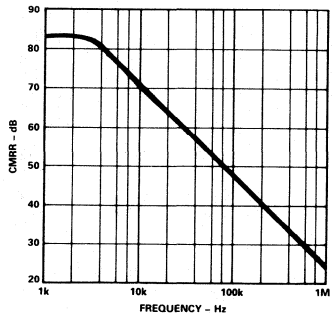


Figure 13. CMRR vs. Frequency

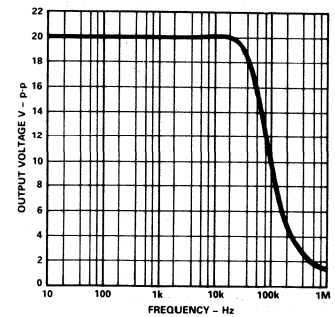


Figure 14. Large Signal Frequency Response

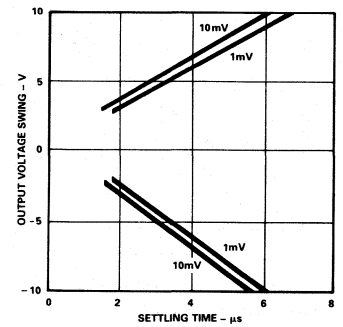


Figure 15. Output Swing and Error Voltage vs. Output Settling Time

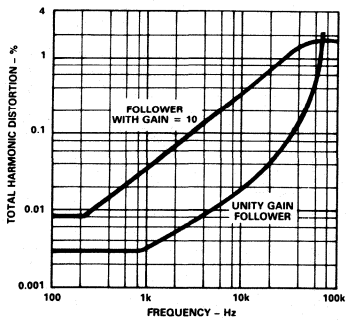


Figure 16. Total Harmonic Distortion vs. Frequency

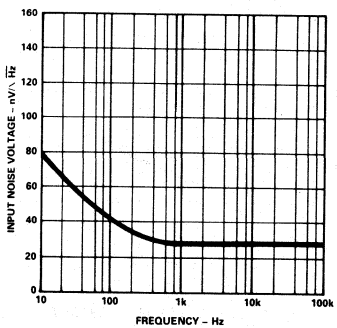


Figure 17. Input Noise Voltage Spectral Density

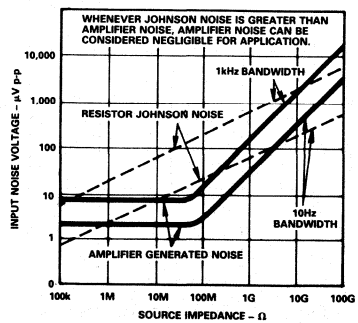


Figure 18. Total Noise vs. Source Impedance

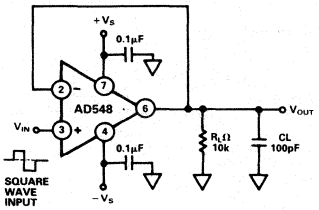


Figure 19a. Unity Gain Follower

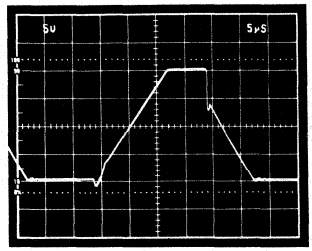


Figure 19b. Unity Gain Follower Pulse Response (Large Signal)

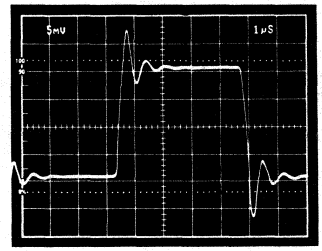


Figure 19c. Unity Gain Follower Pulse Response (Small Signal)

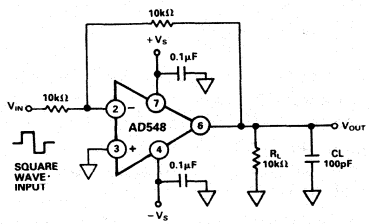


Figure 20a. Unity Gain Inverter

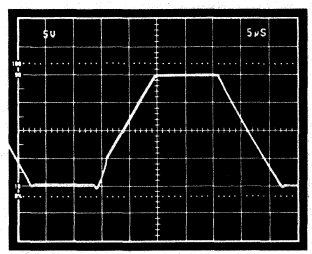


Figure 20b. Unity Gain Inverter Pulse Response (Large Signal)

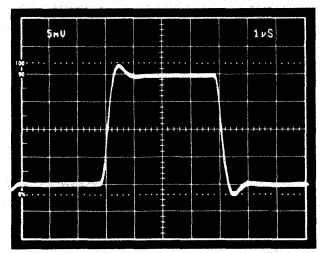


Figure 20c. Unity Gain Inverter Pulse Response (Small Signal)

Applying the AD548

APPLICATION NOTES

The AD548 is a JFET-input op amp with a guaranteed maximum I_B of less than 10pA, and offset and drift laser-trimmed to 0.25mV and 2μV/°C respectively (AD548C). AC specs include 1MHz bandwidth, 1.8V/μs typical slew rate and 8μs settling time for a 20V step to ±0.01% – all at a supply current less than 200μA. To capitalize on the device's performance, a number of error sources should be considered.

The minimal power drain and low offset drift of the AD548 reduce self-heating or "warm-up" effects on input offset voltage, making the AD548 ideal for on/off battery powered applications. The power dissipation due to the AD548's 200μA supply current has a negligible effect on input current, but heavy output loading will raise the chip temperature. Since a JFET's input current doubles for every 10°C rise in chip temperature, this can be a noticeable effect.

The amplifier is designed to be functional with power supply voltages as low as ±4.5V. It will exhibit a higher input offset voltage than at the rated supply voltage of ±15V, due to power supply rejection effects. The common-mode range of the AD548 extends from 3V more positive than the negative supply to 1V more negative than the positive supply. Designed to cleanly drive up to 10kΩ and 100pF loads, the AD548 will drive a 2kΩ load with reduced open loop gain.

OFFSET NULLING

Unlike bipolar input amplifiers, zeroing the input offset voltage of a BiFET op amp will not minimize offset drift. Using balance Pins 1 and 5 to adjust the input offset voltage as shown in Figure 21 will induce an added drift of 0.24μV/°C per 100μV of nulled offset. The low initial offset (0.25mV) of the AD548C results in only 0.6μV/°C of additional drift.

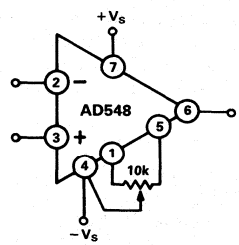


Figure 21. Offset Null Configuration

LAYOUT

To take full advantage of the AD548's 10pA max input current, parasitic leakages must be kept below an acceptable level. The practical limit of the resistance of epoxy or phenolic circuit board material is between $1 \times 10^{12}\Omega$ and $3 \times 10^{12}\Omega$. This can result in an additional leakage of 5pA between an input of 0V and a −15V supply line. Teflon or a similar low leakage material (with a resistance exceeding $10^{17}\Omega$) should be used to isolate high impedance input lines from adjacent lines carrying high voltages. The insulator should be kept clean, since contaminants will degrade the surface resistance.

A metal guard completely surrounding the high impedance nodes and driven by a voltage near the common-mode input potential can also be used to reduce some parasitic leakages. The guarding pattern in Figure 22 will reduce parasitic leakage due to finite board surface resistance; but it will not compensate for a low volume resistivity board.

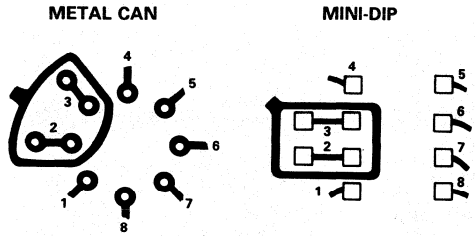


Figure 22. Board Layout for Guarding Inputs

INPUT PROTECTION

The AD548 is guaranteed to withstand input voltages equal to the power supply potential. Exceeding the negative supply voltage on either input will forward bias the substrate junction of the chip. The induced current may destroy the amplifier due to excess heat.

Input protection is required in applications such as a flame detector in a gas chromatograph, where a very high potential may be applied to the input terminals during a sensor fault condition. Figure 23 shows a simple current limiting scheme that can be used. $R_{PROTECT}$ should be chosen such that the maximum overload current is 1.0mA (100kΩ for a 100V overload, for example).

Exceeding the negative common-mode range on either input terminal causes a phase reversal at the output, forcing the amplifier output to the corresponding high or low state. Exceeding the negative common-mode on both inputs simultaneously forces the output high. Exceeding the positive common-mode range on a single input doesn't cause a phase reversal, but if both inputs exceed the limit the output will be forced high. In all cases, normal amplifier operation is resumed when input voltages are brought back within the common-mode range.

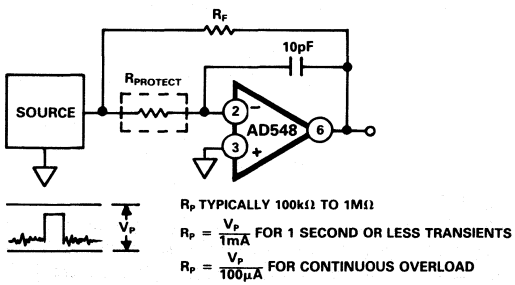


Figure 23. Input Protection of IV Converter

D/A CONVERTER OUTPUT BUFFER

The circuit in Figure 24 shows the AD548 and AD7545 12-bit CMOS D/A converter in a unipolar binary configuration. V_{OUT} will be equal to V_{REF} attenuated by a factor depending on the digital word. V_{REF} sets the full scale. Overall gain is trimmed by adjusting R_{IN}. The AD548's low input offset voltage, low drift and clean dynamics make it an attractive low power output buffer.

The input offset voltage of the AD548 output amplifier results in an output error voltage. This error voltage equals the input offset voltage of the op amp times the noise gain of the amplifier.

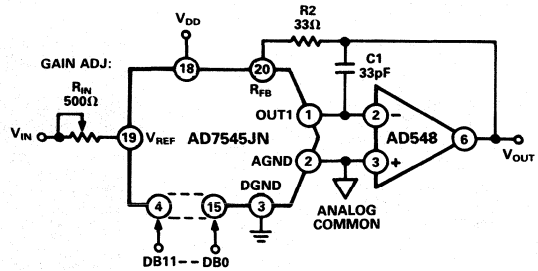


Figure 24. AD548 Used as DAC Output Amplifier

That is:

$$V_{OS}\ \text{Output} = V_{OS}\ \text{Input}\left(1+\frac{R_{FB}}{R_O}\right)$$

R_{FB} is the feedback resistor for the op amp, which is internal to the DAC. R_O is the DAC's R-2R ladder output resistance. The value of R_O is code dependent. This has the effect of changing the offset error voltage at the amplifier's output. An output amplifier with a sub millivolt input offset voltage is needed to preserve the linearity of the DAC's transfer function.

The AD548 in this configuration provides a 700kHz small signal bandwidth and 1.8V/μs typical slew rate. The 33pF capacitor across the feedback resistor optimizes the circuit's response. The oscilloscope photos in Figures 25 and 26 show small and large signal outputs of the circuit in Figure 24. Upper traces show the input signal V_{IN}. Lower traces are the resulting output voltage with the DAC's digital input set to all 1s. The AD548 settles to ±0.01% for a 20V input step in 14μs.

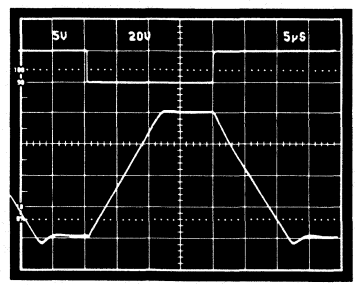


Figure 25. Response to ±20V p-p Reference Square Wave

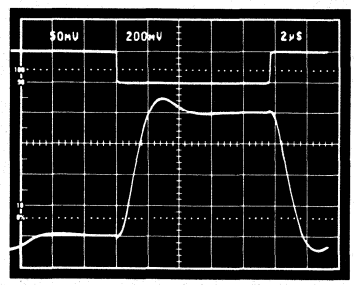


Figure 26. Response to ±100mV p-p Reference Square Wave

PHOTODIODE PREAMP

The performance of the photodiode preamp shown in Figure 27 is enhanced by the AD548's low input current, input voltage offset and offset voltage drift. The photodiode sources a current proportional to the incident light power on its surface. R_F converts the photodiode current to an output voltage equal to $R_F \times I_S$.

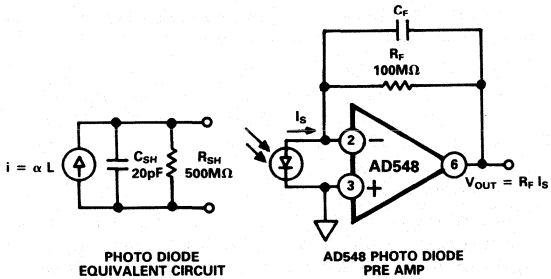


Figure 27.

An error budget illustrating the importance of low amplifier input current, voltage offset and offset voltage drift to minimize output voltage errors can be developed by considering the equivalent circuit for the small (0.2mm² area) photodiode shown in Figure 27. The input current results in an error proportional to the feedback resistance used. The amplifier's offset will produce an error proportional to the preamp's noise gain ($1 + R_F/R_{SH}$), where R_{SH} is the photodiode shunt resistance. The amplifier's input current will double with every 10°C rise in temperature, and the photodiode's shunt resistance halves with every 10°C rise. The error budget in Figure 28 assumes a room temperature photodiode R_{SH} of 500MΩ, and the maximum input current and input offset voltage specs of an AD548C.

TEMP °C	R_{SH} (MΩ)	V_{OS} (μV)	$(1 + R_F/R_{SH})V_{OS}$	I_B (pA)	$I_B R_F$	TOTAL
−25	15,970	150	151μV	0.30	30μV	181μV
0	2,830	200	207μV	2.26	262μV	469μV
+25	500	250	300μV	10.00	1.0mV	1.30mV
+50	88.5	300	640μV	56.6	5.6mV	6.24mV
+75	15.6	350	2.6mV	320	32mV	34.6mV
+85	7.8	370	5.1mV	640	64mV	69.1mV

Figure 28. Photo Diode Pre-Amp Errors Over Temperature

The capacitance at the amplifier's negative input (the sum of the photodiode's shunt capacitance, the op amp's differential input capacitance, stray capacitance due to wiring, etc.) will cause a rise in the preamp's noise gain over frequency. This can result in excess noise over the bandwidth of interest. C_F reduces the noise gain "peaking" at the expense of bandwidth.

INSTRUMENTATION AMPLIFIER

The AD548C's maximum input current of 10pA makes it an excellent building block for the high input impedance instrumentation amplifier shown in Figure 29. Total current drain for this circuit is under 600μA. This configuration is optimal for conditioning differential voltages from high impedance sources.

The overall gain of the circuit is controlled by R_G, resulting in the following transfer function:

$$\frac{V_{OUT}}{V_{IN}} = 1 + \frac{(R_1 + R_2)}{R_G}$$

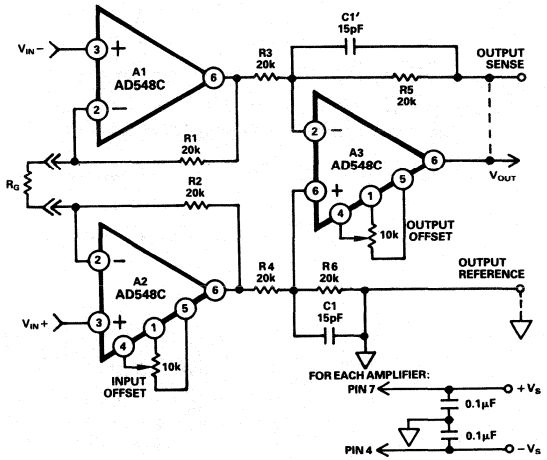


Figure 29. Low Power Instrumentation Amplifier

Gains of 1 to 100 can be accommodated with gain nonlinearities of less than 0.01%. Referred to input errors, which contribute an output error proportional to in amp gain, include a maximum untrimmed input offset voltage of 0.5mV and an input offset voltage drift over temperature of 4μV/°C. Output errors, which are independent of gain, will contribute an additional 0.5mV offset and 4μV/°C drift. The maximum input current is 15pA over the common-mode range, with a common-mode impedance of over $1 \times 10^{12}\Omega$. Resistor pairs R3/R5 and R4/R6 should be ratio matched to 0.01% to take full advantage of the AD548's high common mode rejection. Capacitors C1 and C1′ compensate for peaking in the gain over frequency caused by input capacitance when gains of 1 to 3 are used.

The −3dB small signal bandwidth for this low power instrumentation amplifier is 700kHz for a gain of 1 and 10kHz for a gain of 100. The typical output slew rate is 1.8V/μs.

LOG RATIO AMPLIFIER

Log ratio amplifiers are useful for a variety of signal conditioning applications, such as linearizing exponential transducer outputs and compressing analog signals having a wide dynamic range. The AD548's picoamp level input current and low input offset voltage make it a good choice for the front-end amplifier of the log ratio circuit shown in Figure 30. This circuit produces an output voltage equal to the log base 10 of the ratio of the input currents I_1 and I_2. Resistive inputs R1 and R2 are provided for voltage inputs.

Input currents I_1 and I_2 set the collector currents of Q1 and Q2, a matched pair of logging transistors. Voltages at points A and B are developed according to the following familiar diode equation:

$$V_{BE} = (kT/q) \ln (I_C/I_{ES})$$

In this equation, k is Boltzmann's constant, T is absolute temperature, q is an electron charge, and I_{ES} is the reverse saturation current of the logging transistors. The difference of these two voltages is taken by the subtractor section and scaled by a factor of approximately 16 by resistors R9, R10, and R8. Temperature

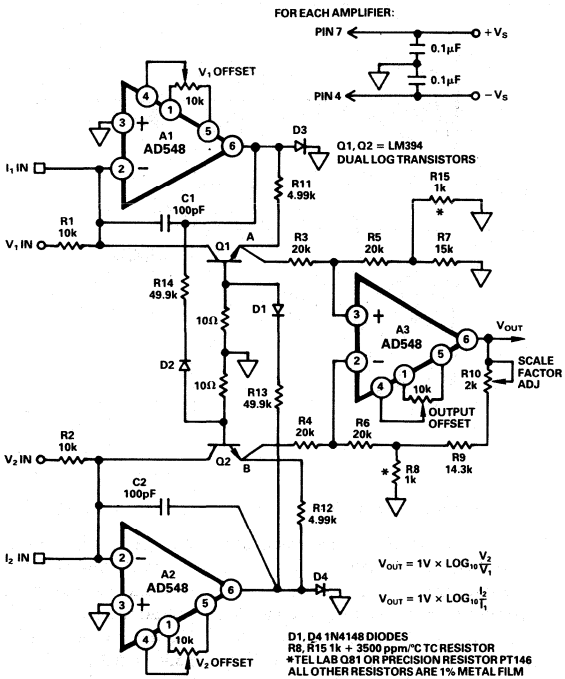


Figure 30. Log Ratio Amplifier

compensation is provided by resistors R8 and R15, which have a positive 3500 ppm/°C temperature coefficient. The transfer function for the output voltage is:

$$V_{OUT} = 1V \log_{10} (I_2/I_1)$$

Frequency compensation is provided by R11, R12, C1, and C2. Small signal bandwidth is approximately 300kHz at input currents above 100μA and will proportionally decrease with lower signal levels. D1, D2, R13, and R14 compensate for the effects of the two logging transistors' ohmic emitter resistance.

To trim this circuit, set the two input currents to 10μA and adjust V_{OUT} to zero by adjusting the potentiometer on A3. Then set I_2 to 1μA and adjust the scale factor such that the output voltage is 1V by trimming potentiometer R10. Offset adjustment for A1 and A2 is provided to increase the accuracy of the voltage inputs.

This circuit ensures a 1% log conformance error over an input current range of 300pA to 1mA, with low level accuracy limited by the AD548's input current. The low level input voltage accuracy of this circuit is limited by the input offset voltage and drift of the AD548.

ANALOG DEVICES

Ultralow Input Bias Current Operational Amplifier

AD549*

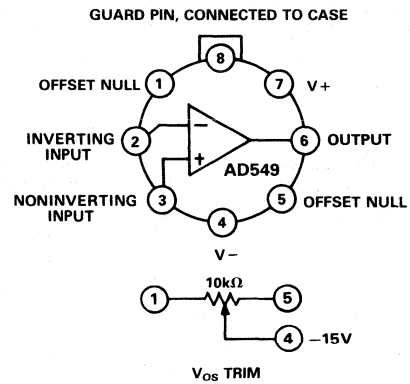
FEATURES

Ultralow Bias Current: 60 fA max (AD549L)
250 fA max (AD549J)
Input Bias Current Guaranteed Over Common-Mode Voltage Range
Low Offset Voltage: 0.25 mV max (AD549K)
1.00 mV max (AD549J)
Low Offset Drift: 5 μV/°C max (AD549K)
20 μV/°C max (AD549J)
Low Power: 700 μA max Supply Current
Low Input Voltage Noise: 4 μV p–p 0.1 to 10 Hz
MIL-STD-883B Parts Available

APPLICATIONS

Electrometer Amplifiers
Photodiode Preamp
pH Electrode Buffer
Vacuum Ion Gage Measurement

CONNECTION DIAGRAM



PRODUCT DESCRIPTION

The AD549 is a monolithic electrometer operational amplifier with very low input bias current. Input offset voltage and input offset voltage drift are laser trimmed for precision performance. The AD549's ultralow input current is achieved with "Topgate" JFET technology, a process development exclusive to Analog Devices. This technology allows the fabrication of extremely low input current JFETs compatible with a standard junction-isolated bipolar process. The 10^{15} Ω common-mode impedance, a result of the bootstrapped input stage, insures that the input current is essentially independent of common-mode voltage.

The AD549 is suited for applications requiring very low input current and low input offset voltage. It excels as a preamp for a wide variety of current output transducers such as photodiodes, photomultiplier tubes, or oxygen sensors. The AD549 can also be used as a precision integrator or low droop sample and hold. The AD549 is pin compatible with standard FET and electrometer op amps, allowing designers to upgrade the performance of present systems at little additional cost.

The AD549 is available in a TO-99 hermetic package. The case is connected to Pin 8 so that the metal case can be independently connected to a point at the same potential as the input terminals, minimizing stray leakage to the case.

The AD549 is available in four performance grades. The J, K, and L versions are rated over the commercial temperature range 0 to +70°C. The S grade is specified over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev C. Extended reliability PLUS screening is also available. PLUS screening includes 168-hour burn-in, as well as other environmental and physical tests derived from MIL-STD-883B, Rev C.

PRODUCT HIGHLIGHTS

1. The AD549's input currents are specified, 100% tested and guaranteed after the device is warmed up. Input current is guaranteed over the entire common-mode input voltage range.
2. The AD549's input offset voltage and drift are laser trimmed to 0.25 mV and 5 μV/°C (AD549K), 1 mV and 20 μV/°C (AD549J).
3. A maximum quiescent supply current of 700 μA minimizes heating effects on input current and offset voltage.
4. AC specifications include 1 MHz unity gain bandwidth and 3 V/μs slew rate. Settling time for a 10 V input step is 5 μs to 0.01%.
5. The AD549 is an improved replacement for the AD515, OPA104, and 3528.

*Protected by Patent No. 4,639,683.

AD549—SPECIFICATIONS (@ +25°C and V_S = +15 V dc, unless otherwise noted)

Model	AD549J			AD549K			AD549L			AD549S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
INPUT BIAS CURRENT[1]													
Either Input, V_{CM} = 0 V		150	250		75	100		40	60		75	100	fA
Either Input, V_{CM} = ±10 V		150	250		75	100		40	60		75	100	fA
Either Input at T_{max}, V_{CM} = 0 V		11			4.2			2.8			420		pA
Offset Current		50			30			20			30		fA
Offset Current at T_{max}		2.2			1.3			0.85			125		pA
INPUT OFFSET VOLTAGE[2]													
Initial Offset		0.5	1.0		0.15	0.25		0.3	0.5		0.3	0.5	mV
Offset at T_{max}			1.9			0.4			0.9			2.0	mV
vs. Temperature		10	20		2	5		5	10		10	15	μV/°C
vs. Supply		32	100		10	32		10	32		10	32	μV/V
vs. Supply, T_{min} to T_{max}		32	100		10	32		10	32		32	50	μV/V
Long-Term Offset Stability		15			15			15			15		μV/Month
INPUT VOLTAGE NOISE													
f = 0.1 Hz to 10 Hz		4			4	6		4			4		μV p-p
f = 10 Hz		90			90			90			90		nV/√Hz
f = 100 Hz		60			60			60			60		nV/√Hz
f = 1 kHz		35			35			35			35		nV/√Hz
f = 10 kHz		35			35			35			35		nV/√Hz
INPUT CURRENT NOISE													
f = 0.1 Hz to 10 Hz		0.7			0.5			0.36			0.5		fA rms
f = 1 kHz		0.22			0.16			0.11			0.16		fA/√Hz
INPUT IMPEDANCE													
Differential V_{DIFF} = ±1		10^{13}‖1			10^{13}‖1			10^{13}‖1			10^{13}‖1		Ω‖pF
Common Mode V_{CM} = ±10		10^{15}‖0.8			10^{15}‖0.8			10^{15}‖0.8			10^{15}‖0.8		Ω‖pF
OPEN-LOOP GAIN													
V_O @ ±10 V, R_L = 10 k	300	1000		300	1000		300	1000		300	1000		V/mV
V_O @ ±10 V, R_L = 10 k, T_{min} to T_{max}	300	800		300	800		300	800		300	800		V/mV
V_O = ±10 V, R_L = 2 k	100	250		100	250		100	250		100	250		V/mV
V_O = ±10 V, R_L = 2 k, T_{min} to T_{max}	80	200		80	200		80	200		25	150		V/mV
INPUT VOLTAGE RANGE													
Differential[3]			±20			±20			±20			±20	V
Common-Mode Voltage	−10		+10	−10		+10	−10		+10	−10		+10	V
Common-Mode Rejection Ratio													
V = +10 V, −10 V	80	90		90	100		90	100		90	100		dB
T_{min} to T_{max}	76	80		80	90		80	90		80	90		dB
OUTPUT CHARACTERISTICS													
Voltage @ R_L = 10 k, T_{min} to T_{max}	−12		+12	−12		+12	−12		+12	−12		+12	V
Voltage @ R_L = 2 k, T_{min} to T_{max}	−10		+10	−10		+10	−10		+10	−10		+10	V
Short Circuit Current	15	20	35	15	20	35	15	20	35	15	20	35	mA
T_{min} to T_{max}	9			9			9			6			mA
Load Capacitance Stability G = +1		4000			4000			4000			4000		pF
FREQUENCY RESPONSE													
Unity Gain, Small Signal	0.7	1.0		0.7	1.0		0.7	1.0		0.7	1.0		MHz
Full Power Response		50			50			50			50		kHz
Slew Rate	2	3		2	3		2	3		2	3		V/μs
Settling Time, 0.1%		4.5			4.5			4.5			4.5		μs
0.01%		5			5			5			5		μs
Overload Recovery, 50% Overdrive, G = −1		2			2			2			2		μs

Model	AD549J Min	AD549J Typ	AD549J Max	AD549K Min	AD549K Typ	AD549K Max	AD549L Min	AD549L Typ	AD549L Max	AD549S Min	AD549S Typ	AD549S Max	Units
POWER SUPPLY													
Rated Performance		±15			±15			±15			±15		V
Operating	±5		**±18**	±5		**±18**	±5		**±18**	±5		**±18**	V
Quiescent Current		0.60	**0.70**		0.60	**0.70**		0.60	**0.70**		0.60	**0.70**	mA
TEMPERATURE RANGE													
Operating, Rated Performance	0		+70	0		+70	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
PACKAGE OPTION[4]													
TO-99 (H-08A)		AD549JH			AD549KH			AD549LH			AD549SH, AD549SH/883B		
Chips		AD549JChips											

NOTES
[1]Bias current specifications are guaranteed after 5 minutes of operation at T_A = +25°C. Bias current increases by a factor of 2.3 for every 10°C rise in temperature.
[2]Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[3]Defined as max continuous voltage between the inputs such that neither input exceeds ±10 V from ground.
[4]For outline information see Package Information section.

Specifications subject to change without notice.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

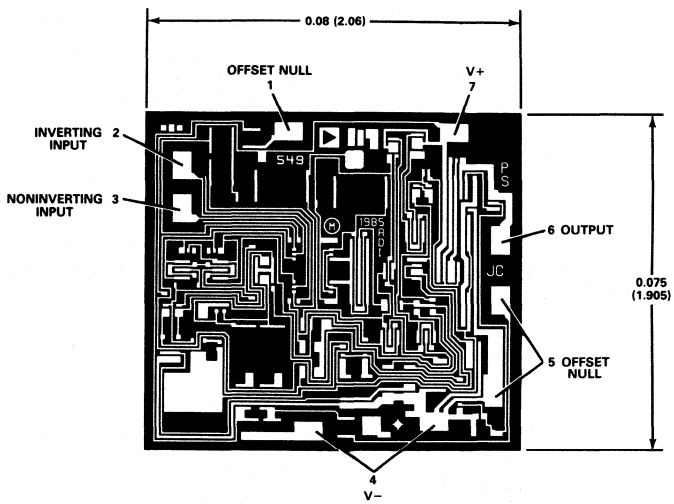
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation . . . . . 500 mW
Input Voltage . . . . . ±18 V[2]
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range (H) . . . . . −65°C to +150°C
Operating Temperature Range
AD549J, K, L . . . . . 0 to +70°C
AD549S . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



CAUTION:

ESD (electrostatic discharge) sensitive device. Charges as high as 4000 V readily accumulate on the human body and test equipment and discharge without detection. Therefore, reasonable ESD precautions are recommended to avoid functional damage or performance degradation. Unused devices should be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' *ESD Prevention Manual.*

AD549—Typical Characteristics

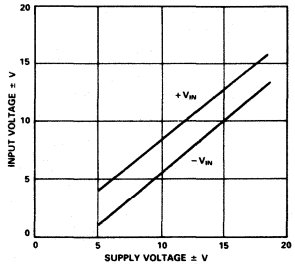


Figure 1. Input Voltage Range vs. Supply Voltage

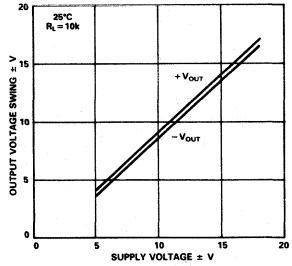


Figure 2. Output Voltage Swing vs. Supply Voltage

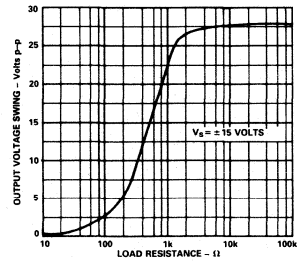


Figure 3. Output Voltage Swing vs. Load Resistance

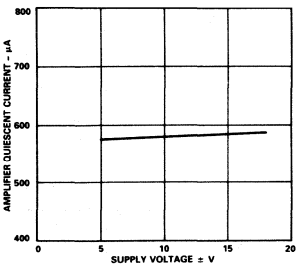


Figure 4. Quiescent Current vs. Supply Voltage

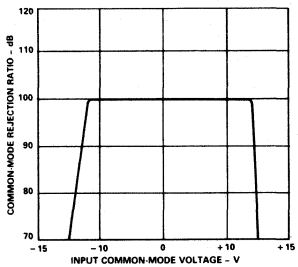


Figure 5. CMRR vs. Input Common-Mode Voltage

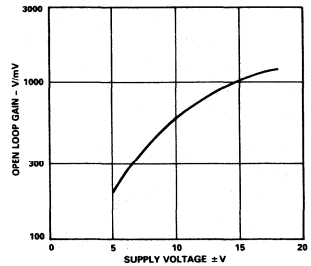


Figure 6. Open-Loop Gain vs. Supply Voltage

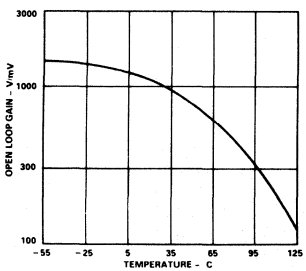


Figure 7. Open-Loop Gain vs. Temperature

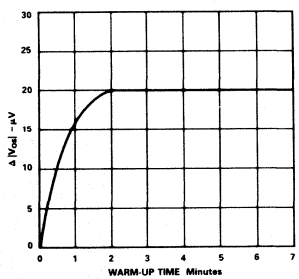


Figure 8. Change in Offset Voltage vs. Warm-Up Time

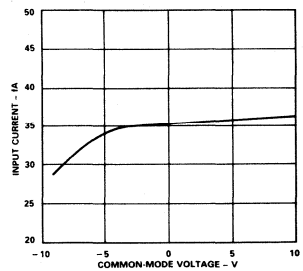


Figure 9. Input Bias Current vs. Common-Mode Voltage

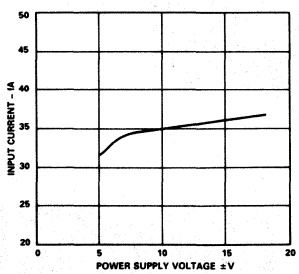


Figure 10. Input Bias Current vs. Supply Voltage

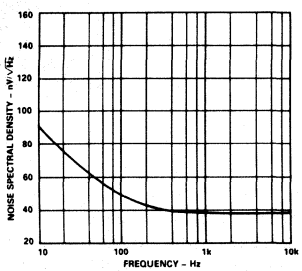


Figure 11. Input Voltage Noise Spectral Density

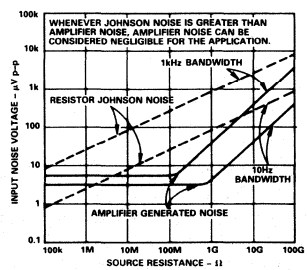


Figure 12. Noise vs. Source Resistance

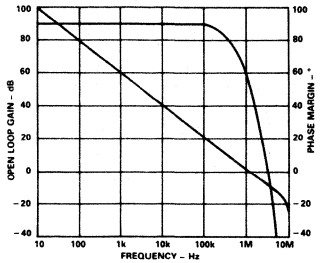


Figure 13. Open-Loop Frequency Response

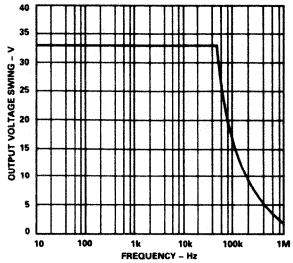


Figure 14. Large Signal Frequency Response

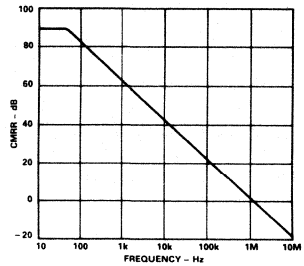


Figure 15. CMRR vs. Frequency

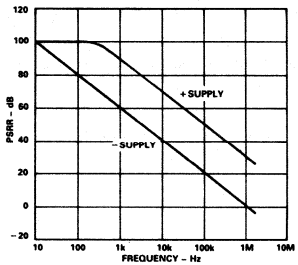


Figure 16. PSRR vs. Frequency

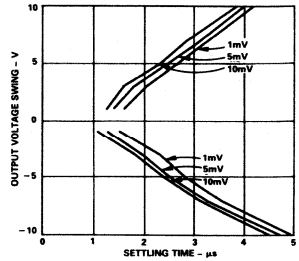


Figure 17. Output Voltage Swing and Error vs. Settling Time

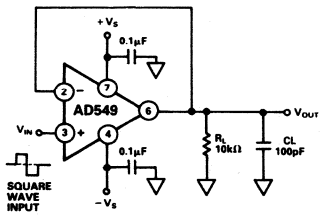


Figure 18. Unity Gain Follower

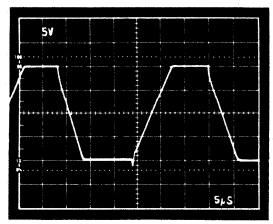


Figure 19. Unity Gain Follower Large Signal Pulse Response

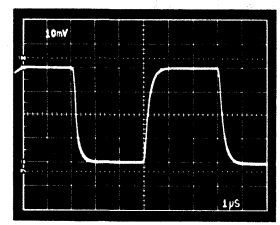


Figure 20. Unity Gain Follower Small Signal Pulse Response

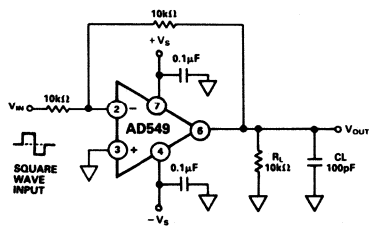


Figure 21. Unity Gain Inverter

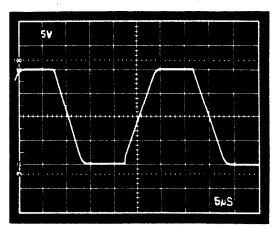


Figure 22. Unity Gain Inverter Large Signal Pulse Response

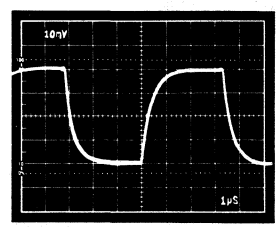


Figure 23. Unity Gain Inverter Small Signal Pulse Response

MINIMIZING INPUT CURRENT

The AD549 has been optimized for low input current and offset voltage. Careful attention to how the amplifier is used will reduce input currents in actual applications.

The amplifier operating temperature should be kept as low as possible to minimize input current. Like other JFET input amplifiers, the AD549's input current is sensitive to chip temperature, rising by a factor of 2.3 for every 10°C rise. This is illustrated in Figure 24, a plot of AD549 input current versus ambient temperature.

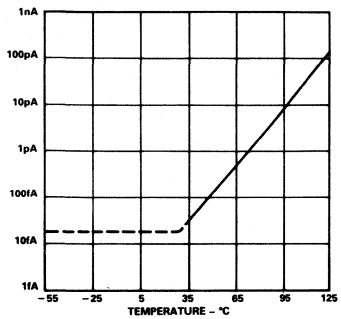


Figure 24. AD549 Input Bias Current vs. Ambient Temperature

On-chip power dissipation will raise chip operating temperature causing an increase in input bias current. Due to the AD549's low quiescent supply current, chip temperature when the (unloaded) amplifier is operated with 15 V supplies, is less than 3°C higher than ambient. The difference in input current is negligible.

However, heavy output loads can cause a significant increase in chip temperature and a corresponding increase in input current. Maintaining a minimum load resistance of 10 Ω is recommended. Input current versus additional power dissipation due to output drive current is plotted in Figure 25.

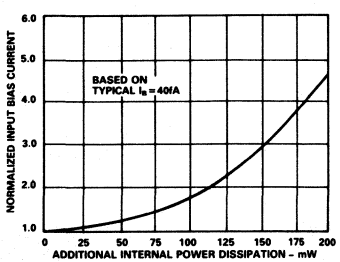


Figure 25. AD549 Input Bias Current vs. Additional Power Dissipation

CIRCUIT BOARD NOTES

There are a number of physical phenomena that generate spurious currents that degrade the accuracy of low current measurements. Figure 26 is a schematic of an I-to-V converter with these parasitic currents modeled.

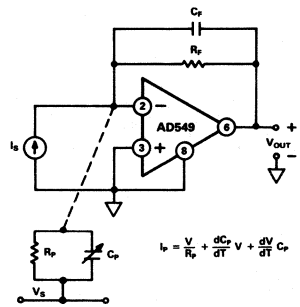


Figure 26. Sources of Parasitic Leakage Currents

Finite resistance from input lines to voltages on the board, modeled by resistor R_P, results in parasitic leakage. Insulation resistance of over 10^{15} Ω must be maintained between the amplifier's signal and supply lines in order to capitalize on the AD549's low input currents. Standard PC board material does not have high enough insulation resistance. Therefore, the AD549's input leads should be connected to standoffs made of insulating material with adequate volume resistivity (e.g., Teflon*). The surface of the insulator's surface must be kept clean in order to preserve surface resistivity. For Teflon, an effective cleaning procedure consists of swabbing the surface with high-grade isopropyl alcohol, rinsing with deionized water, and baking the board at 80°C for 10 minutes.

In addition to high volume and surface resistivity, other properties are desirable in the insulating material chosen. Resistance to water absorption is important since surface water films drastically reduce surface resistivity. The insulator chosen should also exhibit minimal piezoelectric effects (charge emission due to mechanical stress) and triboelectric effects (charge generated by friction). Charge imbalances generated by these mechanisms can appear as parasitic leakage currents. These effects are modeled by variable capacitor C_P in Figure 26. The table in Figure 27 lists various insulators and their properties.[1]

Material	Volume Resistivity (Ω–CM)	Minimal Triboelectric Effects	Minimal Piezoelectric Effects	Resistance to Water Absorption
Teflon	10^{17}–10^{18}	W	W	G
Kel-F**	10^{17}–10^{18}	W	M	G
Sapphire	10^{16}–10^{18}	M	G	G
Polyethylene	10^{14}–10^{18}	M	G	M
Polystyrene	10^{12}–10^{18}	W	M	M
Ceramic	10^{12}–10^{14}	W	M	W
Glass Epoxy	10^{10}–10^{17}	W	M	W
PVC	10^{10}–10^{15}	G	M	G
Phenolic	10^{5} –10^{12}	W	G	W

G–Good with Regard to Property
M–Moderate with Regard to Property
W–Weak with Regard to Property

Figure 27. Insulating Materials and Characteristics

[1]Electronic Measurements, pp.15–17, Keithley Instruments, Inc., Cleveland, Ohio, 1977.

*Teflon is a registered trademark of E.I. DuPont Co.

**Kel-F is a registered trademark of 3-M Company.

Guarding the input lines by completely surrounding them with a metal conductor biased near the input lines' potential has two major benefits. First, parasitic leakage from the signal line is reduced since the voltage between the input line and the guard is very low. Second, stray capacitance at the input node is minimized. Input capacitance can substantially degrade signal bandwidth and the stability of the I-to-V converter. The case of the AD549 is connected to Pin 8 so that it can be bootstrapped near the input potential. This minimizes pin leakage and input common-mode capacitance due to the case. Guard schemes for inverting and noninverting amplifier topologies are illustrated in Figures 28 and 29.

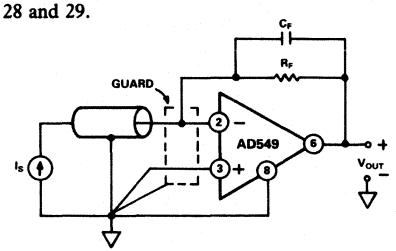


Figure 28. Inverting Amplifier with Guard

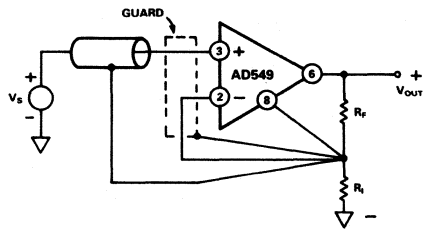


Figure 29. Noninverting Amplifier with Guard

Other guidelines include keeping the circuit layout as compact as possible and input lines short. Keeping the assembly rigid and minimizing sources of vibration will reduce triboelectric and piezoelectric effects. All precision high impedance circuitry requires shielding against interference noise. Low noise coax or triax cables should be used for remote connections to the input signal lines.

OFFSET NULLING

The AD549's input offset voltage can be nulled by using balance Pins 1 and 5, as shown in Figure 30. Nulling the input offset voltage in this fashion will introduce an added input offset voltage drift component of 2.4 μV/°C per millivolt of nulled offset (a maximum additional drift of 0.6 μV/°C for the AD549K, 1.2 μV/°C for the AD549L, 2.4 μV/°C for the AD549J).

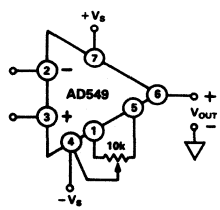


Figure 30. Standard Offset Null Circuit

The approach in Figure 31 can be used when the amplifier is used as an inverter. This method introduces a small voltage referenced to the power supplies in series with the amplifier's positive input terminal. The amplifier's input offset voltage drift with temperature is not affected. However, variation of the power supply voltages will cause offset shifts.

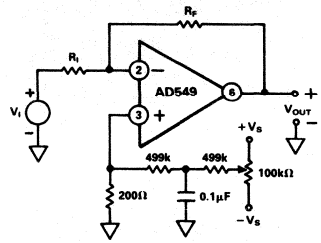


Figure 31. Alternate Offset Null Circuit for Inverter

AC RESPONSE WITH HIGH VALUE SOURCE AND FEEDBACK RESISTANCE

Source and feedback resistances greater than 100 kΩ will magnify the effect of input capacitances (stray and inherent to the AD549) on the ac behavior of the circuit. The effects of common-mode and differential input capacitances should be taken into account since the circuit's bandwidth and stability can be adversely affected.

In a follower, the source resistance and input common-mode capacitance form a pole that limits the bandwidth to $1/2\pi R_S C_S$. Bootstrapping the metal case by connecting Pin 8 to the output minimizes capacitance due to the package. Figures 32 and 33 show the follower pulse response from a 1 MΩ source resistance with and without the package connected to the output. Typical common-mode input capacitance for the AD549 is 0.8 pF.

In an inverting configuration, the differential input capacitance forms a pole in the circuit's loop transmission. This can create peaking in the ac response and possible instability. A feedback capacitance can be used to stabilize the circuit. The inverter pulse response with R_F and R_S equal to 1 MΩ appears in Figure 34. Figure 35 shows the response of the same circuit with a 1 pF feedback capacitance. Typical differential input capacitance for the AD549 is 1 pF.

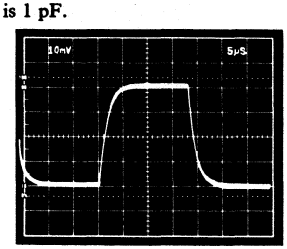


Figure 32. Follower Pulse Response from 1 MΩ Source Resistance, Case Not Bootstrapped

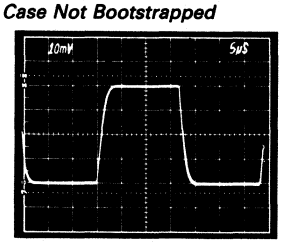


Figure 33. Follower Pulse Response from 1 MΩ Source Resistance, Case Bootstrapped

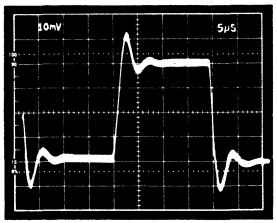


Figure 34. Inverter Pulse Response with 1 MΩ Source and Feedback Resistance

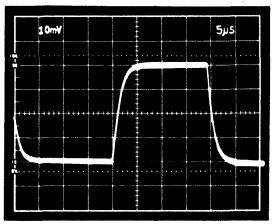


Figure 35. Inverter Pulse Response with 1 MΩ Source and Feedback Resistance, 1 pF Feedback Capacitance

COMMON-MODE INPUT VOLTAGE OVERLOAD

The rated common-mode input voltage range of the AD549 is from 3 V less than the positive supply voltage to 5 V greater than the negative supply voltage. Exceeding this range will degrade the amplifier's CMRR. Driving the common-mode voltage above the positive supply will cause the amplifier's output to saturate at the upper limit of output voltage. Recovery time is typically 2 µs after the input has been returned to within the normal operating range. Driving the input common-mode voltage within 1 V of the negative supply causes phase reversal of the output signal. In this case, normal operation is typically resumed within 0.5 µs of the input voltage returning within range.

DIFFERENTIAL INPUT VOLTAGE OVERLOAD

A plot of the AD549's input currents versus differential input voltage (defined as $V_{IN}+ - V_{IN}-$) appears in Figure 36. The input current at either terminal stays below a few hundred femtoamps until one input terminal is forced higher than 1 to 1.5 V above the other terminal. Under these conditions, the input current limits at 30 µA.

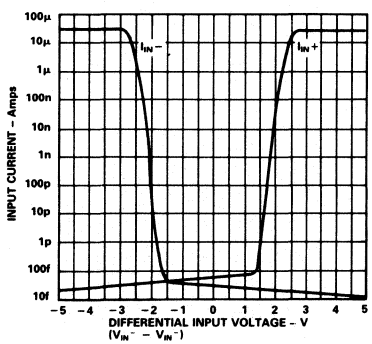


Figure 36. Input Current vs. Differential Input Voltage

INPUT PROTECTION

The AD549 safely handles any input voltage within the supply voltage range. Subjecting the input terminals to voltages beyond the power supply can destroy the device or cause shifts in input current or offset voltage if the amplifier is not protected.

A protection scheme for the amplifier as an inverter is shown in Figure 37. R_P is chosen to limit the current through the inverting input to 1 mA for expected transient (less than 1 second) overvoltage conditions, or to 100 µA for a continuous overload. Since R_P is inside the feedback loop, and is much lower in value than the amplifier's input resistance, it does not affect the inverter's dc gain. However, the Johnson noise of the resistor will add root sum of squares to the amplifier's input noise.

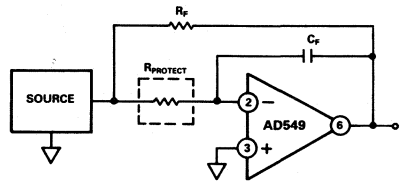


Figure 37. Inverter with Input Current Limit

In the corresponding version of this scheme for a follower, shown in Figure 38, R_P and the capacitance at the positive input terminal will produce a pole in the signal frequency response at a $f = 1/2\pi RC$. Again, the Johnson noise R_P will add to the amplifier's input voltage noise.

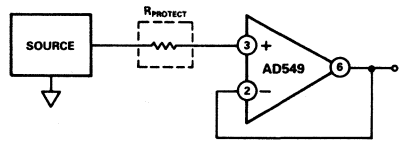


Figure 38. Follower with Input Current Limit

Figure 39 is a schematic of the AD549 as an inverter with an input voltage clamp. Bootstrapping the clamp diodes at the inverting input minimizes the voltage across the clamps and keeps the leakage due to the diodes low. Low leakage diodes, such as the FD333's should be used, and should be shielded from light to keep photocurrents from being generated. Even with these precautions, the diodes will measurably increase the input current and capacitance.

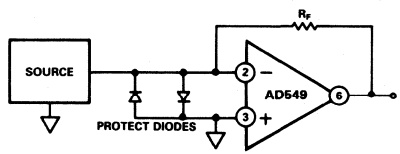


Figure 39. Input Voltage Clamp with Diodes

SAMPLE AND DIFFERENCE CIRCUIT TO MEASURE ELECTROMETER LEAKAGE CURRENTS

There are a number of methods used to test electrometer leakage currents, including current integration and direct current to voltage conversion. Regardless of the method used, board and interconnect cleanliness, proper choice of insulating materials (such as Teflon or Kel-F), correct guarding and shielding techniques and care in physical layout are essential to making accurate leakage measurements.

Figure 40 is a schematic of the sample and difference circuit. It uses two AD549 electrometer amplifiers (A and B) as current-to-voltage converters with high value (10^{10} Ω) sense resistors (RSa and RSb). R1 and R2 provide for an overall circuit sensitivity of 10 fA/mV (10 pA full scale). C_C and C_F provide noise suppression and loop compensation. C_C should be a low leakage polystyrene capacitor. An ultralow leakage Kel-F test socket is used for contacting the device under test. Rigid Teflon coaxial cable is used to make connections to all high impedance nodes. The use of rigid coax affords immunity to error induced by mechanical vibration and provides an outer conductor for shielding. The entire circuit is enclosed in a grounded metal box.

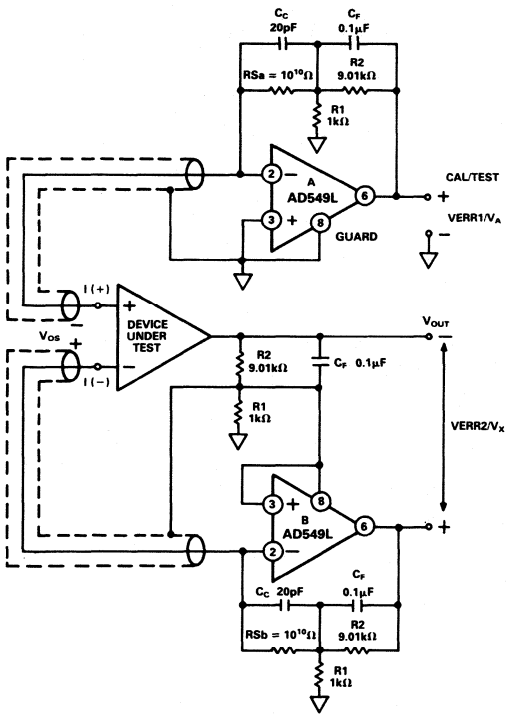


Figure 40. Sample and Difference Circuit for Measuring Electrometer Leakage Currents

The test apparatus is calibrated without a device under test present. A five minute stabilization period after the power is turned on is required. First, V_{ERR1} and V_{ERR2} are measured. These voltages are the errors caused by offset voltages and leakage currents of the current to voltage converters.

$$V_{ERR1} = 10\ (V_{OS}A - I_BA \times RSa)$$
$$V_{ERR2} = 10\ (V_{OS}B - I_BB \times RSb)$$

Once measured, these errors are subtracted from the readings taken with a device under test present. Amplifier B closes the feedback loop to the device under test, in addition to providing current to voltage conversion. The offset error of the device under test appears as a common-mode signal and does not affect the test measurement. As a result, only the leakage current of the device under test is measured.

$$V_A - V_{ERR1} = 10[RSa \times I_B(+)]$$
$$V_X - V_{ERR2} = 10[RSb \times I_B(-)]$$

Although a series of devices can be tested after only one calibration measurement, calibration should be updated periodically to compensate for any thermal drift of the current to voltage converters or changes in the ambient environment. Laboratory results have shown that repeatable measurements within 10 fA can be realized when this apparatus is properly implemented. These results are achieved in part by the design of the circuit, which eliminates relays and other parasitic leakage paths in the high impedance signal lines, and in part by the inherent cancellation of errors through the calibration and measurement procedure.

PHOTODIODE INTERFACE

The AD549's low input current and low input offset voltage make it an excellent choice for very sensitive photodiode preamps (Figure 41). The photodiode develops a signal current, I_S equal to:

$$I_S = R \times P$$

where P is light power incident on the diode's surface in Watts and R is the photodiode responsivity in Amps/Watt. R_F converts the signal current to an output voltage:

$$V_{OUT} = R_F \times I_S$$

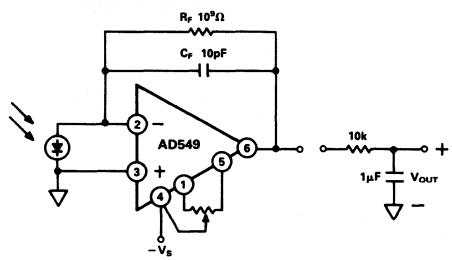


Figure 41. Photodiode Preamp

DC error sources and an equivalent circuit for a small area (0.2 mm square) photodiode are indicated in Figure 42.

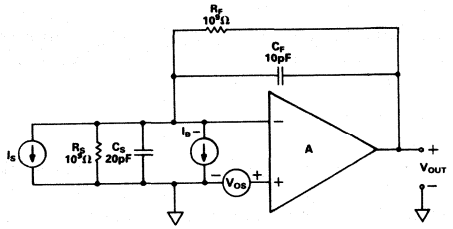


Figure 42. Photodiode Preamp DC Error Sources

Input current, I_B, will contribute an output voltage error, V_{E1}, proportional to the feedback resistance:

$$V_{E1} = I_B \times R_F$$

The op amp's input voltage offset will cause an error current through the photodiode's shunt resistance, R_S:

$$I = V_{OS}/R_S$$

The error current will result in an error voltage (V_{E2}) at the amplifier's output equal to:

$$V_{E2} = (1+R_F/R_S)\, V_{OS}$$

Given typical values of photodiode shunt resistance (on the order of 10^9 Ω), R_F/R_S can easily be greater than one, especially if a large feedback resistance is used. Also, R_F/R_S will increase with temperature, as photodiode shunt resistance typically drops by a factor of two for every 10°C rise in temperature. An op amp with low offset voltage and low drift must be used in order to maintain accuracy. The AD549K offers guaranteed maximum 0.25 mV offset voltage, and 5 mV/°C drift for very sensitive applications.

Photodiode Preamp Noise

Noise limits the signal resolution obtainable with the preamp. The output voltage noise divided by the feedback resistance is the minimum current signal that can be detected. This minimum detectable current divided by the responsivity of the photodiode represents the lowest light power that can be detected by the preamp.

Noise sources associated with the photodiode, amplifier, and feedback resistance are shown in Figure 43; Figure 44 is the spectral density versus frequency plot of each of the noise source's contribution to the output voltage noise (circuit parameters in Figure 42 are assumed). Each noise source's rms contribution to the total output voltage noise is obtained by integrating the square of its spectral density function over frequency. The rms value of the output voltage noise is the square root of the sum of all contributions. Minimizing the total area under these curves will optimize the preamplifier's resolution for a given bandwidth.

The photodiode preamp in Figure 41 can detect a signal current of 26 fA rms at a bandwidth of 16 Hz, which assuming a photodiode responsivity of 0.5 A/W, translates to a 52 fW rms minimum detectable power. The photodiode used has a high source resistance and low junction capacitance. C_F sets the signal bandwidth with R_F and also limits the "peak" in the noise gain that multiplies the op amp's input voltage noise contribution. A single pole filter at the amplifier's output limits the op amp's output voltage noise bandwidth to 26 Hz, a frequency comparable to the signal bandwidth. This greatly improves the preamplifier's signal to noise ratio (in this case, by a factor of three).

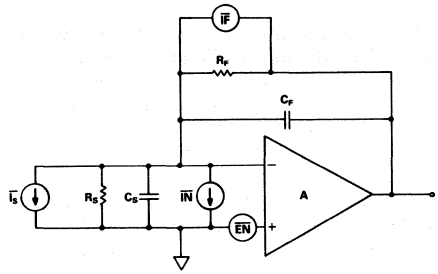


Figure 43. Photodiode Preamp Noise Sources

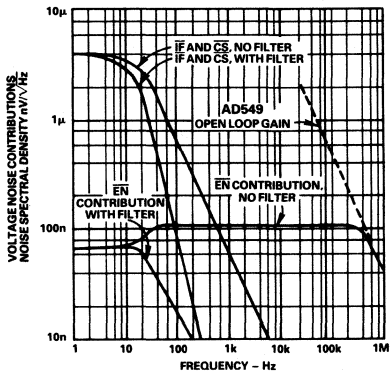


Figure 44. Photodiode Preamp Noise Sources' Spectral Density vs. Frequency

Log Ratio Amplifier

Logarithmic ratio circuits are useful for processing signals with wide dynamic range. The AD549L's 60 fA maximum input current makes it possible to build a log ratio amplifier with 1% log conformance for input current ranging from 10 pA to 1 mA, a dynamic range of 160 dB.

The log ratio amplifier in Figure 45 provides an output voltage proportional to the log base 10 of the ratio of the input currents I1 and I2. Resistors R1 and R2 are provided for voltage inputs. Since NPN devices are used in the feedback loop of the front-end amplifiers that provide the log transfer function, the output is valid only for positive input voltages and input currents. The input currents set the collector currents IC1 and IC2 of a matched pair of log transistors Q1 and Q2 to develop voltages VA and VB:

$$VA, B = -(kT/q) \ln IC/IES$$

where IES is the transistors' saturation current.

The difference of VA and VB is taken by the subtractor section to obtain:

$$VC = (kT/q) \ln (IC2/IC1)$$

VC is scaled up by the ratio of (R9+R10)/R8, which is equal to approximately 16 at room temperature, resulting in the output voltage:

$$V_{OUT} = 1 \times \log (IC2/IC1)\ V.$$

R8 is a resistor with a positive 3500 ppm/°C temperature coefficient to provide the necessary temperature compensation. The parallel combination of R15 and R7 is provided to keep the subtractor section's gain for positive and negative inputs matched over temperature.

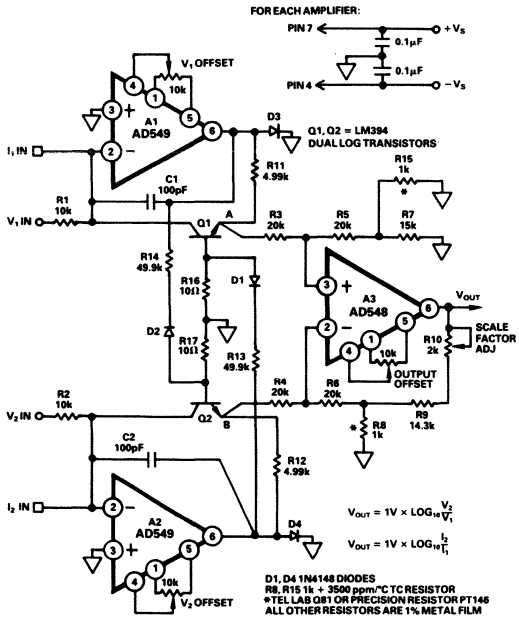


Figure 45. Log Ratio Amplifier

Frequency compensation is provided by R11, R12, and C1 and C2. The bandwidth of the circuit is 300 kHz at input signals greater than 50 μA, and decreases smoothly with decreasing signal levels.

To trim the circuit, set the input currents to 10 μA and trim A3's offset using the amplifier's trim potentiometer so the output equals 0. Then set I1 to 1 μA and adjust the output to equal 1 V by trimming R10. Additional offset trims on the amplifiers A1 and A2 can be used to increase the voltage input accuracy and dynamic range.

The very low input current of the AD549 makes this circuit useful over a very wide range of signal currents. The total input current (which determines the low level accuracy of the circuit) is the sum of the amplifier input current, the leakage across the compensating capacitor (negligible if polystyrene or Teflon capacitor is used), and the collector to collector, and collector to base leakages of one side of the dual log transistors. The magnitude of these last two leakages depend on the amplifier's input offset voltage and are typically less than 10 fA with 1 mV offsets. The low level accuracy is limited primarily by the amplifier's input current, only 60 fA maximum when the AD549L is used.

The effects of the emitter resistance of Q1 and Q2 can degrade the circuit's accuracy at input currents above 100 μA. The networks composed of R13, D1, R16, and R14, D2, R17 compensate for these errors, so that this circuit has less than 1% log conformance error at 1 mA input currents. The correct value for R13 and R14 depends on the type of log transistors used. 49.9 kΩ resistors were chosen for use with LM394 transistors. Smaller resistance values will be needed for smaller log transistors.

TEMPERATURE COMPENSATED pH PROBE AMPLIFIER

A pH probe can be modeled as a mV-level voltage source with a series source resistance dependent upon the electrode's composition and configuration. The glass bulb resistance of a typical pH electrode pair falls between 10^6 and 10^9 Ω. It is therefore important to select an amplifier with low enough input currents such that the voltage drop produced by the amplifier's input bias current and the electrode resistance does not become an appreciable percentage of a pH unit.

The circuit in Figure 46 illustrates the use of the AD549 as a pH probe amplifier. As with other electrometer applications, the use of guarding, shielding, Teflon standoffs, etc., is a must in order to capitalize on the AD549's low input current. If an AD549L (60 fA max input current) is used, the error contributed by input current will be held below 60 μV for pH electrode source impedances up to 10^9 Ω. Input offset voltage (which can be trimmed) will be below 0.5 mV.

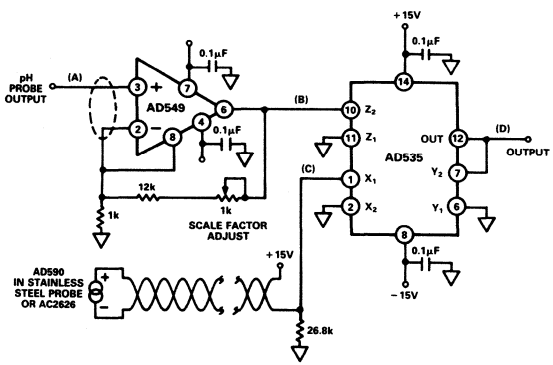


Figure 46. Temperature Compensated pH Probe Amplifier

The pH probe output is ideally zero volts at a pH of 7 independent of temperature. The slope of the probe's transfer function, though predictable, is temperature dependent (−54.2 mV/pH at 0 and −74.04 mV/pH at 100°C). By using an AD590 temperature sensor and an AD535 analog divider, an accurate temperature compensation network can be added to the basic pH probe

amplifier. The table in Figure 47 shows voltages at various points and illustrates the compensation. The AD549 is set for a noninverting gain of 13.51. The output of the AD590 circuitry (point C) will be equal to 10 V at 100°C and decrease by 26.8 mV/°C. The output of the AD535 analog divider (point D) will be a temperature compensated output voltage centered at zero volts for a pH of 7, and having a transfer function of −1.00V/pH unit. The output range spans from −7.00 V (pH=14) to +7.00 V (pH=0).

PROBE TEMP	A (PROBE OUTPUT)	B (A×13.51)	C (590 OUTPUT)	D (10 B/C)
0	54.20 mV	0.732 V	7.32 V	1.00 V
25°C	59.16 mV	0.799 V	7.99 V	1.00 V
37°C	61.54 mV	0.831 V	8.31 V	1.00 V
60°C	66.10 mV	0.893 V	8.93 V	1.00 V
100°C	74.04 mV	1.000 V	10.00 V	1.00 V

Figure 47. Table Illustrating Temperature Compensation

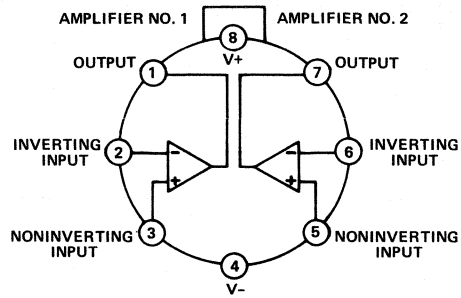
Precision, Low Cost Dual BiFET Op Amp

AD642

FEATURES

Matched Offset Voltage
Matched Offset Voltage Over Temperature
Matched Bias Current
Crosstalk-124dB at 1kHz
Low Bias Current: 35pA max Warmed Up
Low Offset Voltage: 500μV max
Low Input Voltage Noise: 2μV p-p
High Open Loop Gain
Low Quiescent Current: 2.8mA max
Low Total Harmonic Distortion
Standard Dual Amplifier Pin Out
Available in Hermetic Metal Can Package and Chip Form
MIL-STD-883B Processing Available
Single Version Available: AD542

PIN CONFIGURATION



PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

TOP VIEW

PRODUCT DESCRIPTION

The AD642 is a pair of matched high speed monolithic Bi-FET operational amplifier fabricated with the most advanced bipolar, JFET and laser trimming technologies. The AD642 offers matched bias currents that are significantly lower than currently available monolithic dual FET input operational amplifiers: 35pA max matched to 25pA for the AD642K and L; 75pA max, matched to 35pA for the AD642J and S. In addition, the offset voltage is laser trimmed to less than 0.5mV and matched to 0.25mV for the AD642L, 1.0mV and matched to 0.5mV for the AD642K, utilizing Analog's laser-wafer trimming (LWT) process.

The tight matching and temperature tracking between the operational amplifiers is achieved by ion-implanted JFETs and laser-wafer trimming. Ion-implantation permits the fabrication of precision, matched JFETs on a monolithic bipolar chip. This optimizes the process to product matched bias currents which have lower initial bias currents than other popular BiFET op amps. Laser-wafer trimming each amplifier's input offset voltage assures tight initial match and combined with superior IC processing guarantees offset voltage tracking over the temperature range.

The AD642 is recommended for applications in which excellent ac and dc performance is required. The matched amplifiers provide a low-cost solution for true instrumentation amplifiers, log ratio amplifiers, and output amplifiers for four quadrant multiplying D/A converters such as the AD7541.

The AD642 is available in four versions: the "J", "K" and "L," all specified over the 0 to +70°C temperature range and one version, "S," over the -55°C to +125°C extended operating temperature range. All devices are packaged in the hermetically-sealed, TO-99 metal can or available in chip form.

PRODUCT HIGHLIGHTS

1. The AD642 has tight matching specifications to ensure high performance, eliminating the need to match individual devices.
2. Analog Devices, unlike some manufacturers, specifies each device for the maximum bias current at either input in the warmed-up condition, thus assuring the user that the AD642 will meet its published specifications in actual use.
3. Laser-wafer-trimming reduces offset voltage to as low as 0.5mV max and matched side to side to 0.25mV (AD642L), thus eliminating the need for external nulling.
4. Low voltage noise (2μV, p-p), and high open loop gain enhance the AD642's performance as a precision op amp.
5. The standard dual amplifier pin out allows the AD642 to replace lower performance duals without redesign.
6. The AD642 is available in chip form.

AD642—SPECIFICATIONS (@ +25°C and V_S = ±15V dc)

Model	AD642J Min	AD642J Typ	AD642J Max	AD642K Min	AD642K Typ	AD642K Max	AD642L Min	AD642L Typ	AD642L Max	AD642S Min	AD642S Typ	AD642S Max	Units
OPEN LOOP GAIN													
V_O = ±10V, $R_L \geq 2k\Omega$	**100,000**			**250,000**			**250,000**			**250,000**			V/V
T_{min} to T_{max}, $R_L = 2k\Omega$	100,000			250,000			250,000			100,000			V/V
OUTPUT CHARACTERISTICS													
Voltage @ $R_L = 2k\Omega$, T_{min} to T_{max}	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Voltage @ $R_L = 10k\Omega$, T_{min} to T_{max}	**±12**	±13		**±12**	±13		**±12**	±13		**±12**	±13		V
Short Circuit Current		25			25			25			25		mA
FREQUENCY RESPONSE													
Unity Gain Small Signal		1.0			1.0			1.0			1.0		MHz
Full Power Response		50			50			50			50		kHz
Slew Rate, Unity Gain	**2.0**	3.0		**2.0**	3.0		**2.0**	3.0		**2.0**	3.0		V/µs
INPUT OFFSET VOLTAGE[1]													
Initial Offset			**2.0**			**1.0**			**0.5**			**1.0**	mV
Input Offset Voltage T_{min} to T_{max}			3.5			**2.0**			**1.0**			**3.5**	mV
Input Offset Voltage vs. Supply, T_{min} to T_{max}			200			**100**			**100**			**100**	µV/V
INPUT BIAS CURRENT[2]													
Either Input		10	**75**		10	**35**		10	**35**		10	**35**	pA
Offset Current		5			2			2			2		pA
MATCHING CHARACTERISTICS[3]													
Input Offset Voltage			**1.0**			**0.5**			**0.25**			**0.5**	mV
Input Offset Voltage T_{min} to T_{max}			3.5			**2.0**			**1.0**			**3.5**	mV
Input Bias Current			**35**			**25**			**25**			**35**	pA
Crosstalk		−124			−124			−124			−124		dB
INPUT IMPEDANCE													
Differential		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		MΩ|pF
Common Mode		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		MΩ|pF
INPUT VOLTAGE RANGE													
Differential[4]		±20			±20			±20			±20		V
Common Mode	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Common Mode Rejection	**76**			**80**			**80**			**80**			dB
INPUT NOISE													
Voltage 0.1Hz to 10Hz		2			2			2			2		µV p-p
f = 10Hz		70			70			70			70		nV/√Hz
f = 100Hz		45			45			45			45		nV/√Hz
f = 1kHz		30			30			30			30		nV/√Hz
f = 10kHz		25			25			25			25		nV/√Hz
POWER SUPPLY													
Rated Performance		±15			±15			±15			±15		V
Operating	±5		±18	±5		±15	±5		±15	±5		±15	V
Quiescent Current			**2.8**			**2.8**			**2.8**			**2.8**	mA
TEMPERATURE RANGE													
Operating, Rated Performance	0		+70	0		+70	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
TRANSISTOR COUNT		58			58			58			58		
PACKAGE OPTION[5]													
TO-99 Style (H-08B)		AD642JH			AD642KH			AD642LH			AD642SH		
Chips		AD642JChips			AD642KChips						AD642SChips		

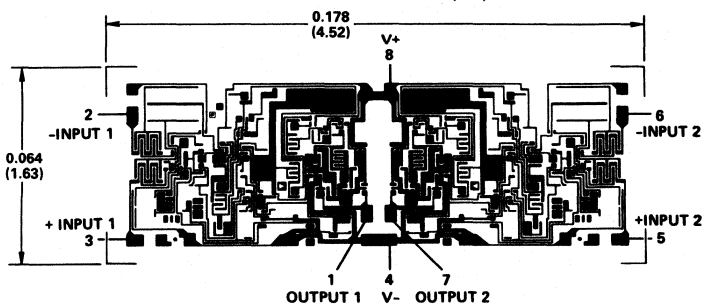
NOTES
[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[2]Bias Current specifications are guaranteed at maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.
[3]Matching is defined as the difference between parameters of the two amplifiers.
[4]Defined as the maximum safe voltage between inputs, such that neither exceeds ±10V from ground.
[5]For outline information see Package Information section.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm)



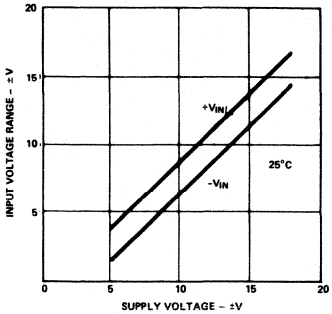


Figure 1. Input Voltage Range vs. Supply Voltage

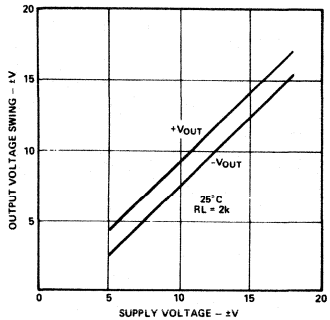


Figure 2. Output Voltage Swing vs. Supply Voltage

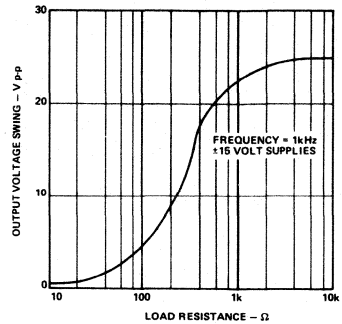


Figure 3. Output Voltage Swing vs. Load Resistance

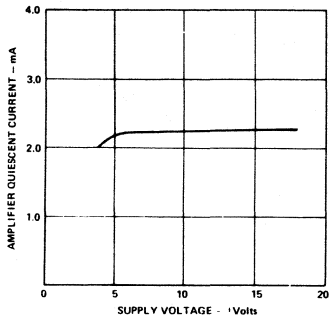


Figure 4. Quiescent Current vs. Supply Voltage

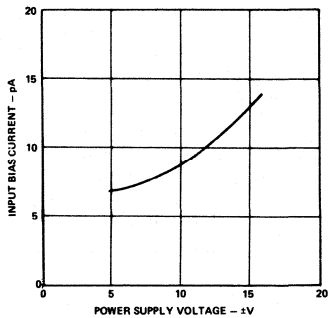


Figure 5. Input Bias Current vs. Power Supply Voltage

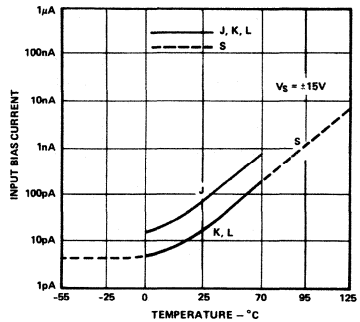


Figure 6. Input Bias Current vs. Temperature

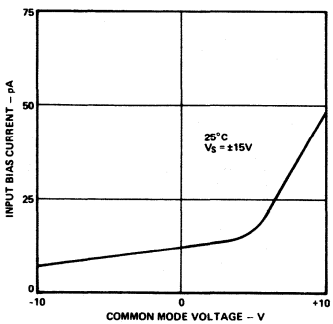


Figure 7. Input Bias Current vs. CMV

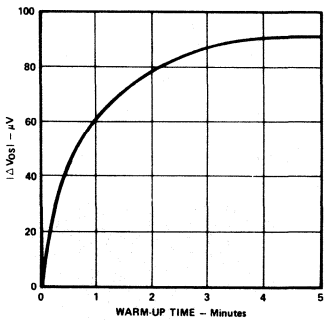


Figure 8. Change in Offset vs. Warm-Up Time

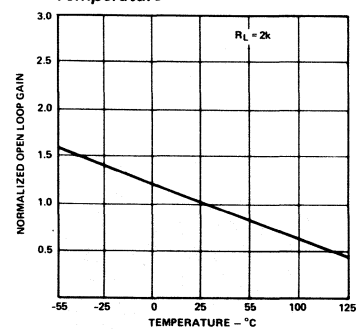


Figure 9. Open Loop Gain vs. Temperature

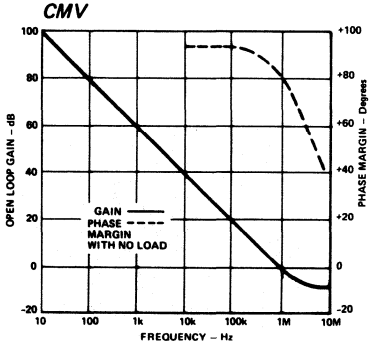


Figure 10. Open Loop Frequency Response

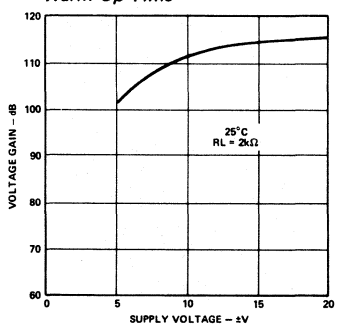


Figure 11. Open Loop Voltage Gain vs. Supply Voltage

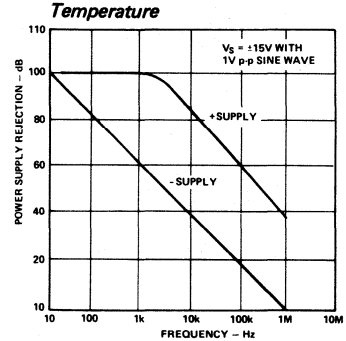


Figure 12. Power Supply Rejection vs. Frequency

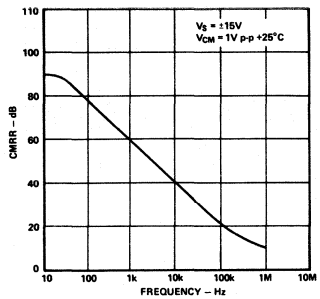


Figure 13. Common Mode Rejection Ratio vs. Frequency

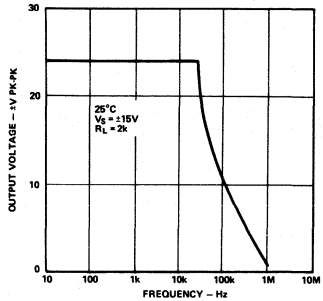


Figure 14. Large Signal Frequency Response

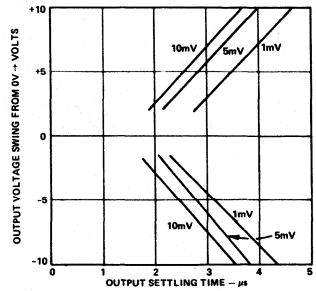


Figure 15. Output Swing and Error vs. Output Settling Time (Circuit of Figure 23)

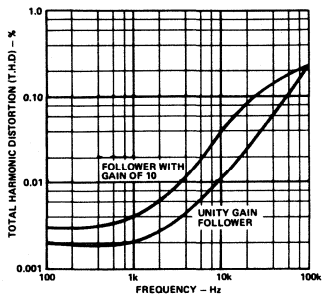


Figure 16. Total Harmonic Distortion vs. Frequency

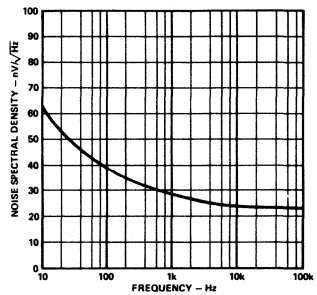


Figure 17. Input Noise Voltage Spectral Density

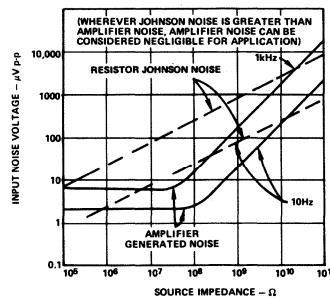
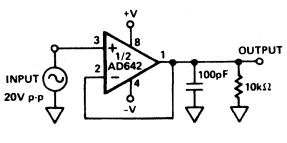
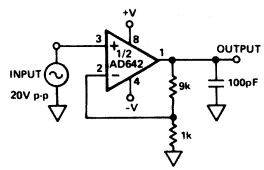


Figure 18. Total Noise vs. Source Impedance



a. Unity Gain Follower



b. Follower with Gain = 10

Figure 19. T.H.D. Test Circuits

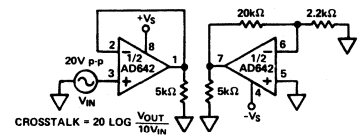


Figure 20. Crosstalk Test Circuit

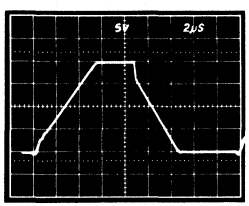


Figure 21a. Unity Gain Follower Pulse Response (Large Signal)

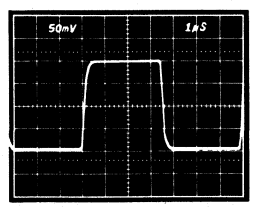


Figure 21b. Unity Gain Follower Pulse Response (Small Signal)

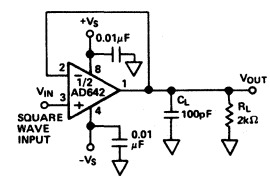


Figure 21c. Unity Gain Follower

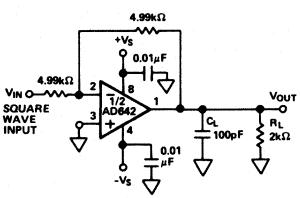


Figure 22a. Unity Gain Inverter

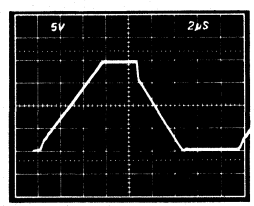


Figure 22b. Unity Gain Inverter Pulse Response (Large Signal)

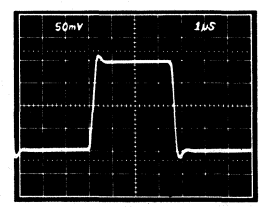


Figure 22c. Unity Gain Inverter Pulse Response (Small Signal)

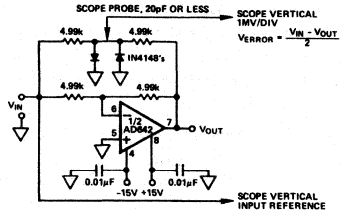


Figure 23. Settling Time Test Circuit

Fast settling time (8μs to 0.01% for 20V p-p step), low power and low offset voltage make the AD642 an excellent choice for use as an output amplifier for current output D/A converters such as the AD7541.

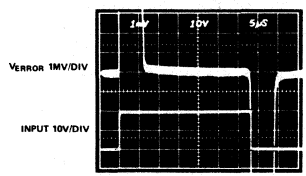


Figure 24. Settling Characteristic Detail

The upper trace of the oscilloscope photograph of Figure 24 shows the settling characteristic of the AD642. The lower trace represents the input to Figure 23. The AD642 has been designed for fast settling to 0.01%, however, feedback components, circuit layout and circuit design must be carefully considered to obtain optimum settling time.

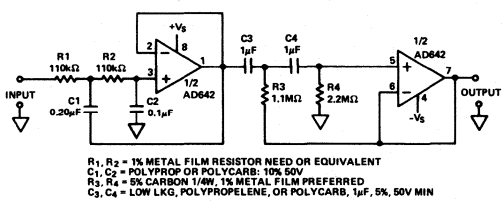


Figure 25. 0.1Hz to 10Hz 2nd Order Bandpass Filter, Maximally Flat

The low frequency (1/f) noise has a power spectrum that is inversely proportional to frequency. Typically this noise is not important above 10Hz, but it can be important for low frequency-high gain applications.

The low noise characteristics of the AD642 make it ideal for 1/f noise testing circuits. The circuit of Figure 25 is a 0.1Hz to 10Hz bandpass filter with second order filter characteristics.

The circuit illustrated in Figure 26 uses two AD642s to construct an instrumentation amplifier with low input current (35pA max), high linearity and low offset voltage and offset voltage drift. The AD644 may be substituted for increased speed, but the higher open-loop gain of the AD642 maintains better linearity over the gain range of 1 to 1000. Amplifier A1 is an AD642L for low input offset voltage (250μV max) and low input offset voltage drift at high gains because matching and tracking are very important for the balanced input stage. Amplifier A2 serves two nonrelated functions, output amplifier and active data-guard drive, and does not require close matching between sections; thus it may be an AD642J.

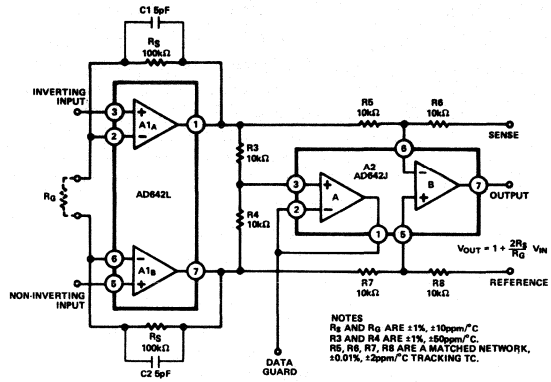


Figure 26. Precision FET Input Instrumentation Amplifier

The output impedance of a CMOS DAC varies with the digital word thus changing the noise of the amplifier circuit. This effect will cause a nonlinearity whose magnitude is dependent on the offset voltage of the amplifier. The AD642K with trimmed offset will minimize the effect. The Schottky protection diodes recommended for use with many older CMOS DACs are not required when using the AD642.

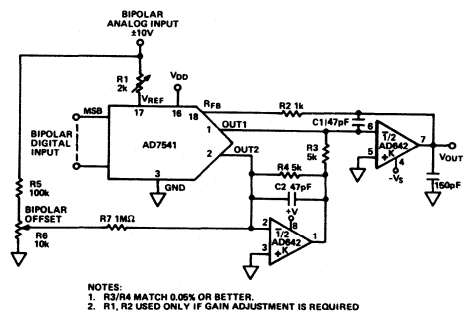


Figure 27a. AD642 Used as DAC Output Amplifier

Figure 27a illustrates the AD7541 12-bit digital-to-analog converter, connected for bipolar operation. Since the digital input can accept bipolar numbers and V_{REF} can accept a bipolar analog input, the circuit can perform a 4-quadrant multiplication.

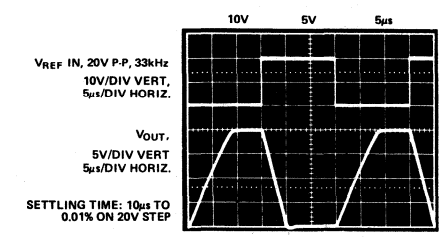


Figure 27b. Voltage Output DAC Settling Characteristic

The photo above shows the output of the circuit of Figure 27a. The upper trace represents the reference input, and the bottom trace shows the output voltage for a digital input of all ones on the DAC. The 47pF capacitor across the feedback

resistor compensates for the DAC output capacitance, and the 150pF load capacitor serves to minimize output glitches.

Log amplifiers or log ratio amplifiers are useful in applications requiring compression of wide-range analog input data, linearization of transducers having exponential outputs, and analog computing, ranging from simple translation of natural relationships in log form (e.g., computing absorbance as the log-ratio of input currents), to the use of logarithms in facilitating analog computation of terms involving arbitrary exponents and multi-term products and ratios.

The picoamp level input current and low offset voltage of the AD642 make it suitable for wide dynamic range log amplifiers. Figure 28 is a schematic of a log ratio circuit employing the AD642 that can achieve less than 1% conformance error over 5 decades of current input, 1nA to 100μA. For voltage inputs, the dynamic range is typically 50mV to 10V for 1% error, limited on the low end by the amplifiers' input offset voltage.

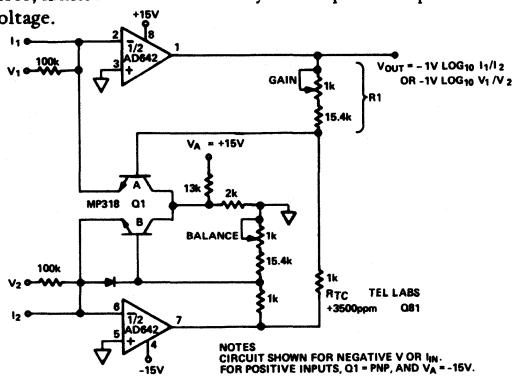


Figure 28. Log-Ratio Amplifier

The conversion between current (or voltage) input and log output is accomplished by the base emitter junctions of the dual transistor Q1. Assuming Q1 has $\beta > 100$, which is the case for the specified transistor, the base-emitter voltage on side 1 is to a close approximation:

$$V_{BE\,A} = kT/q \ln I_1/I_{S1}$$

This circuit is arranged to take the difference of the V_{BE}'s of Q1A and Q1B, thus producing an output voltage proportional to the log of the *ratio* of the inputs:

$$V_{OUT} = -K(V_{BE\,A} - V_{BE\,B}) = -\frac{KkT}{q}(\ln I_1/I_{S1} - \ln I_2/I_{S2})$$

$$V_{OUT} = -K\,kT/q \ln I_1/I_2$$

The scaling constant, K is set by R1 and R_{TC} to about 16, to produce 1V change in output voltage per decade difference in input signals. R_{TC} is a special resistor with a +3500ppm/°C temperature coefficient, which makes K inversely proportional to temperature, compensating for the "T" in kT/q. The log-ratio transfer characteristic is therefore independent of temperature.

This particular log ratio circuit is free from the dynamic problems that plague many other log circuits. The -3dB bandwidth is 50kHz over the top 3 decades, 100nA to 100μA, and decreases smoothly at lower input levels. This circuit needs no additional frequency compensation for stable operation from input current sources, such as photodiodes, that may have 100pF of shunt capacitance. For larger input capacitances a 20pF integration capacitor around each amplifier will provide a smoother frequency response.

This log ratio amplifier can be readily adjusted for optimum accuracy by following this simple procedure. First, apply V1 = V2 = -10.00V and adjust "Balance" for V_{OUT} = 0.00V. Next apply V1 = -10.00V, V2 = -1.00V and adjust gain for V_{OUT} = +1.00V. Repeat this procedure until gain and balance readings are within 2mV of ideal values.

The low input bias current (35pA) and low noise characteristics of the AD642 make it suitable for electrometer applications such as photo diode preamplifiers and picoampere current-to-voltage converters. The use of guarding techniques in printed circuit board layout and construction is critical for achieving the ultimate in low leakage performance that the AD642 can deliver. The input guarding scheme shown in Figure 29 will minimize leakage as much as possible; the guard ring should be applied to both sides of the board. The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on a printed circuit; to minimize noise and leakage, they must be carried in rigid shielded cables.

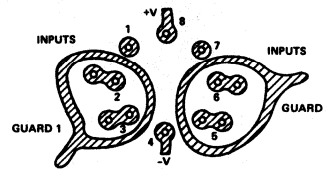


Figure 29. Board Layout for Guarding Inputs

INPUT PROTECTION

The AD642 is guaranteed for a maximum safe input potential equal to the power supply potential. The input stage design also allows differential input voltages of up to ±0.5 volts while maintaining the full differential input resistance of $10^{12}\Omega$. This makes the AD642 suitable for low speed voltage comparators directly connected to a high impedance source.

Many instrumentation situations, such as flame detectors in gas chromatographs, involve measurement of low level currents from high-voltage sources. In such applications, a sensor fault condition may apply a very high potential to the input of the current-to-voltage converting amplifier. This possibility necessitates some form of input protection. Many electrometer type devices, especially CMOS designs, can require elaborate zener protection schemes which often compromise overall performance. The AD642 requires input protection only if the source is not current-limited, and as such is similar to many JFET-input designs. The failure mode would be overheating from excess current rather than voltage breakdown. If the source is not current-limited, all that is required is a resistor in series with the affected input terminal so that the maximum overload current is 1.0mA (for example, 100kΩ for a 100 volt overload). This simple scheme will cause no significant reduction in performance and give complete overload protection. Figure 30 shows proper connections.

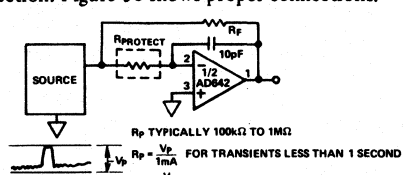


Figure 30. AD642 Input Protection

ANALOG DEVICES

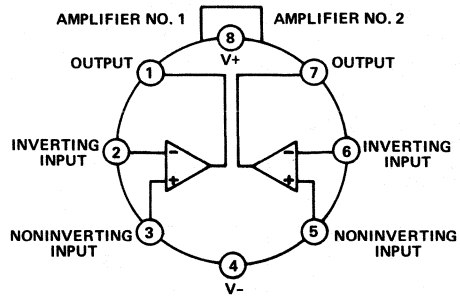
Dual High Speed, Implanted BiFET Op Amp

AD644

FEATURES

- Matched Offset Voltage
- Matched Offset Voltage Over Temperature
- Matched Bias Currents
- Crosstalk -124dB at 1kHz
- Low Bias Current: 35pA max Warmed Up
- Low Offset Voltage: 500μV max
- Low Input Voltage Noise: 2μV p-p
- High Slew Rate: 13V/μs
- Low Quiescent Current: 4.5mA max
- Fast Settling to ±0.01%: 3μs
- Low Total Harmonic Distortion: 0.0015% at 1kHz
- Standard Dual Amplifier Pin Out
- Available in Hermetic Metal Can Package and Chip Form
- MIL-STD-883B Processing Available
- Single Version Available: AD544

PIN CONFIGURATION



PIN 4 IS IN ELECTRICAL CONTACT WITH THE CASE

TOP VIEW

PRODUCT DESCRIPTION

The AD644 is a pair of matched high speed monolithic FET-input operational amplifiers fabricated with the most advanced bipolar, JFET and laser-trimming technologies. The AD644 offers matched bias currents that are significantly lower than currently available monolithic dual BiFET operational amplifiers: 35pA max, matched to 25pA for the AD644K and L, 75pA max matched to 35pA for the AD644J and S. In addition, the offset voltage is laser trimmed to less than 0.5mV, and matched to 0.25mV for the AD644L, 1.0mV and matched to 0.5mV for the AD644K, utilizing Analog Devices' laser-wafer trimming (LWT) process.

The tight matching and temperature tracking between the operational amplifiers is achieved by ion-implanted JFETs and laser-wafer trimming. Ion-implantation permits the fabrication of precision, matched JFETs on a monolithic bipolar chip. This process optimizes the ability to produce matched amplifiers which have lower initial bias currents than other popular BiFET op amps. Laser-wafer trimming each amplifier's input offset voltage assures tight initial match and superior IC processing guarantees offset voltage tracking over the temperature range.

The AD644 is recommended for applications in which both excellent ac and dc performance is required. The matched amplifiers provide a low cost solution to true wideband instrumentation amplifiers, low dc drift active filters and output amplifiers for four quadrant multiplying D/A converters such as the AD7541, 12-bit CMOS DAC.

The AD644 is available in four versions: the "J", "K" and "L" are specified over the 0 to +70°C temperature range and the "S" over the -55°C to +125°C operating temperature range. All devices are packaged in the hermetically sealed, TO-99 metal can or available in chip form.

PRODUCT HIGHLIGHTS

1. The AD644 has tight side to side matching specifications to ensure high performance without matching individual devices.
2. Analog Devices, unlike some manufacturers, specifies each device for the maximum bias current at either input in the warmed-up condition, thus assuring the user that the AD644 will meet its published specifications in actual use.
3. Laser-wafer-trimming reduces offset voltage to as low as 0.5mV max matched side to side to 0.25mV (AD644L), thus eliminating the need for external nulling.
4. Improved bipolar and JFET processing on the AD644 result in the lowest matched bias current available in a high speed monolithic FET op amp.
5. Low voltage noise (2μV p-p) and high open loop gain enhance the AD644's performance as a precision op amp.
6. The high slew rate (13.0V/μs) and fast settling time to 0.01% (3.0μs) make the AD644 ideal for D/A, A/D, sample-hold circuits and dual high speed integrators.
7. Low harmonic distortion (0.0015%) and low crosstalk (-124dB) make the AD644 an ideal choice for stereo audio applications.
8. The standard dual amplifier pin out allows the AD644 to replace lower performance duals without redesign.
9. The AD644 is available in chip form.

AD644—SPECIFICATIONS (@ +25°C and V_S = ±15V dc)

Model	AD644J			AD644K			AD644L			AD644S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OPEN LOOP GAIN													
V_O = ±10V, $R_L \geq 2k\Omega$	**30,000**			**50,000**			**50,000**			**50,000**			V/V
T_{min} to T_{max}, $R_L = 2k\Omega$	20,000			**40,000**			**40,000**			**20,000**			V/V
OUTPUT CHARACTERISTICS													
Voltage @ $R_L = 2k\Omega$, T_{min} to T_{max}	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Voltage @ $R_L = 10k\Omega$, T_{min} to T_{max}	**±12**	±13		**±12**	±13		**±12**	±13		**±12**	±13		V
Short-Circuit Current		25			25			25			25		mA
FREQUENCY RESPONSE													
Unity Gain Small Signal		2.0			2.0			2.0			2.0		MHz
Full Power Response		200			200			200			200		kHz
Slew Rate, Unity Gain	**8.0**	13.0		**8.0**	13.0		**8.0**	13.0		**8.0**	13.0		V/µs
Total Harmonic Distortion		0.0015			0.0015			0.0015			0.0015		%
INPUT OFFSET VOLTAGE[1]													
Initial Offset			**2.0**			**1.0**			**0.5**			**1.0**	mV
Input Offset Voltage T_{min} to T_{max}			3.5			**2.0**			**1.0**			**3.5**	mV
Input Offset Voltage vs. Supply, T_{min} to T_{max}			200			**100**			**100**			**100**	µV/V
INPUT BIAS CURRENT[2]													
Either Input		10	**75**		10	**35**		10	**35**		10	**35**	pA
Offset Current		10			5			5			5		pA
MATCHING CHARACTERISTICS[3]													
Input Offset Voltage			**1.0**			**0.5**			**0.25**			**0.5**	mV
Input Offset Voltage T_{min} to T_{max}			3.5			**2.0**			**1.0**			**3.5**	mV
Input Bias Current			**35**			**25**			**25**			**35**	pA
Crosstalk		−124			−124			−124			−124		dB
INPUT IMPEDANCE													
Differential		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		MΩ‖pF
Common Mode		$10^{12}\|3$			$10^{12}\|3$			$10^{12}\|3$			$10^{12}\|3$		MΩ‖pF
INPUT VOLTAGE RANGE													
Differential[4]		±20			±20			±20			±20		V
Common Mode	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Common Mode Rejection	**76**			**80**			**80**			**80**			dB
INPUT NOISE													
Voltage 0.1Hz to 10Hz		2			2			2			2		µV p-p
f = 10Hz		35			35			35			35		nV/√Hz
f = 100Hz		22			22			22			22		nV/√Hz
f = 1kHz		18			18			18			18		nV/√Hz
f = 10kHz		16			16			16			16		nV/√Hz
POWER SUPPLY													
Rated Performance		±15			±15			±15			±15		V
Operating	±5		±18	±5		±18	±5		±18	±5		±18	V
Quiescent Current		3.5	**4.5**		3.5	**4.5**		3.5	**4.5**		3.5	**4.5**	mA
TEMPERATURE RANGE													
Operating, Rated Performance	0		+70	0		+70	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
PACKAGE OPTION[5]													
TO-99 Style (H-08B)		AD644JH			AD644KH			AD644LH			AD644SH		
Chips		AD644JChips			AD644KChips						AD644SChips		

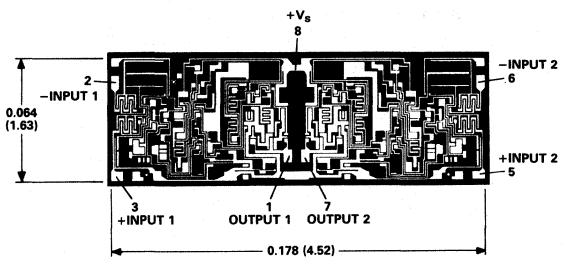
NOTES
[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[2]Bias Current specifications are guaranteed at maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.
[3]Matching is defined as the difference between parameters of the two amplifiers.
[4]Defined as voltage between inputs, such that neither exceeds ±10V from ground.
[5]For outline information see Package Information section.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

METALIZATION PHOTOGRAPHY

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



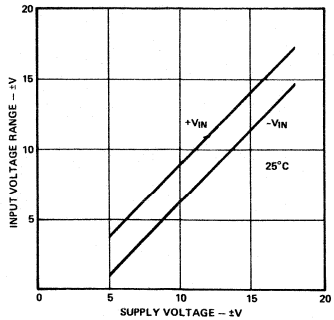


Figure 1. Input Voltage Range vs. Supply Voltage

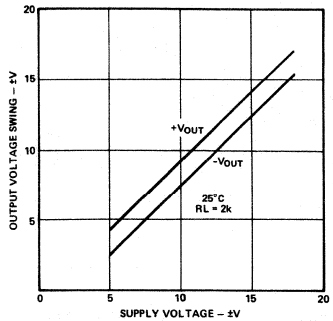


Figure 2. Output Voltage Swing vs. Supply Voltage

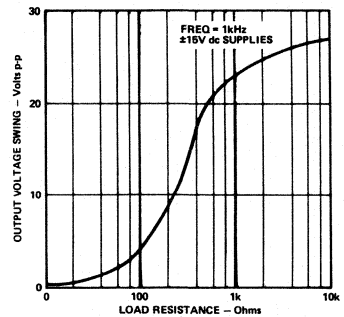


Figure 3. Output Voltage Swing vs. Load Resistance

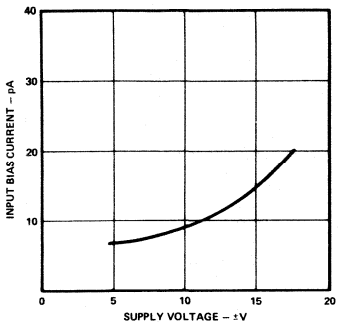


Figure 4. Input Bias Current vs. Supply Voltage

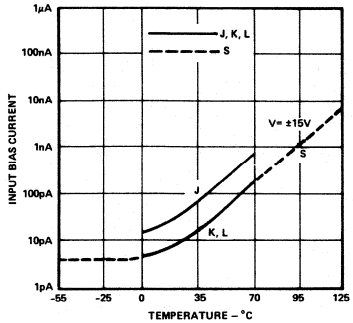


Figure 5. Input Bias Current vs. Temperature

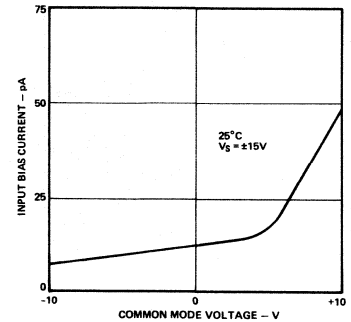


Figure 6. Input Bias Current vs. CMV

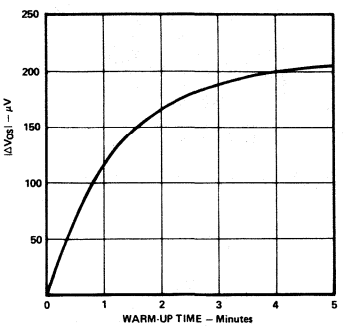


Figure 7. Change in Offset Voltage vs. Warm-Up Time

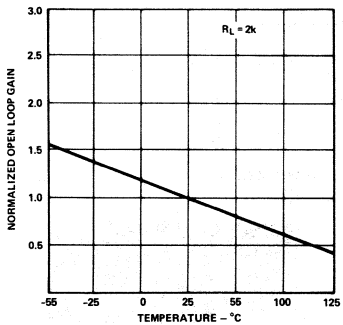


Figure 8. Open Loop Gain vs. Temperature

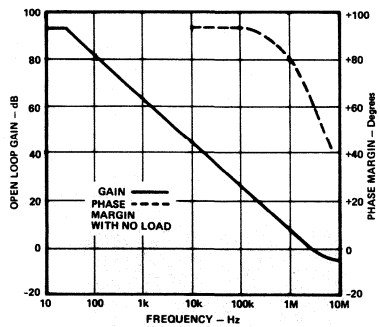


Figure 9. Open Loop Frequency Response

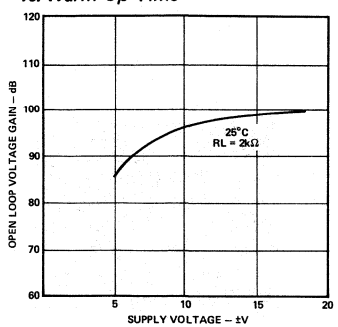


Figure 10. Open Loop Voltage Gain vs. Supply Voltage

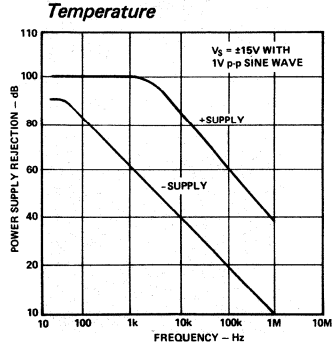


Figure 11. Power Supply Rejection vs. Frequency

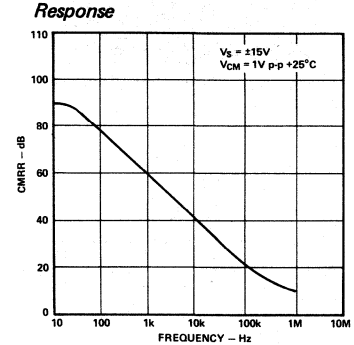


Figure 12. Common Mode Rejection Ratio vs. Frequency

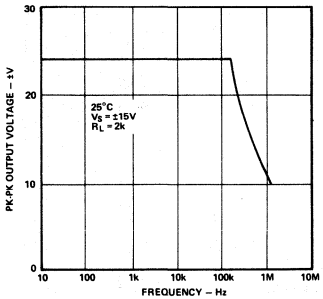


Figure 13. Large Signal Frequency Response

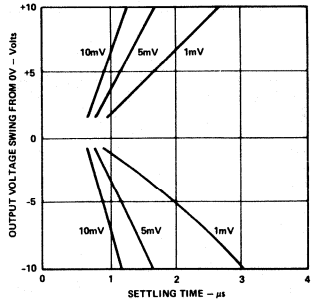


Figure 14. Output Swing and Error vs. Settling Time (Circuit of Figure 23a)

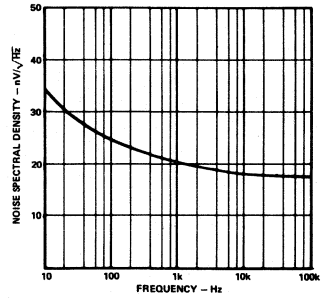


Figure 15. Noise Spectral Density

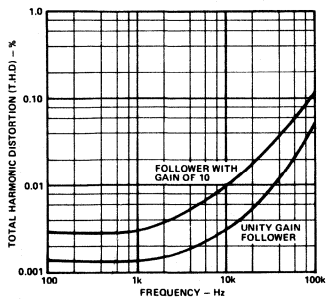


Figure 16. Total Harmonic Distortion vs. Frequency

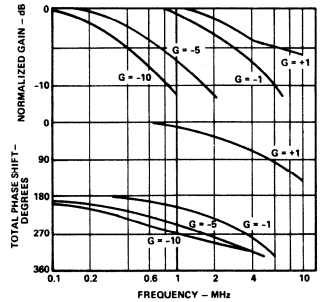


Figure 17. Closed Loop Gain & Phase vs. Frequency

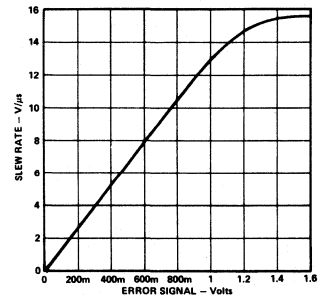
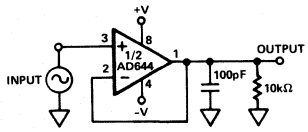
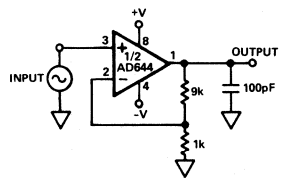


Figure 18. Slew Rate vs. Error Signal



a. Unity Gain Follower



b. Follower with Gain = 10

Figure 19. T.H.D. Test Circuits

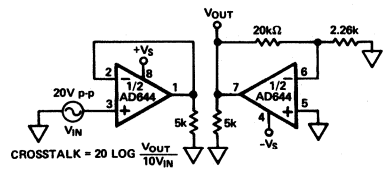


Figure 20. Crosstalk Test Circuit

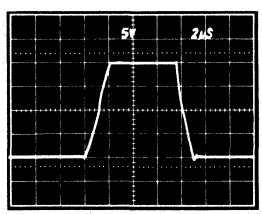


Figure 21a. Unity Gain Follower Pulse Response (Large Signal)

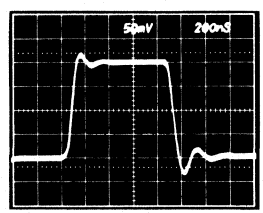


Figure 21b. Unity Gain Follower Pulse Response (Small Signal)

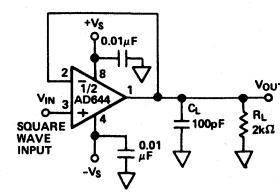


Figure 21c. Unity Gain Follower

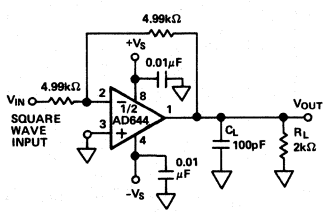


Figure 22a. Unity Gain Inverter

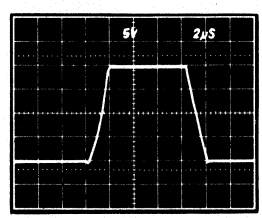


Figure 22b. Unity Gain Inverter Pulse Response (Large Signal)

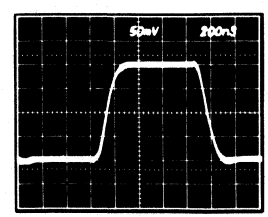


Figure 22c. Unity Gain Inverter Pulse Response (Small Signal)

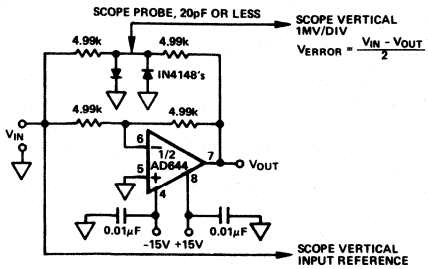


Figure 23a. Settling Time Test Circuit

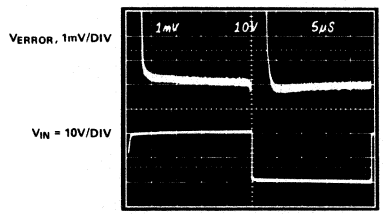


Figure 23b. Settling Characteristic Detail

The fast settling time (3.0μs to 0.01% for 20V p-p step) and low offset voltage make the AD644 an excellent choice as an output amplifier for current output D/A converters such as the AD7541. The upper trace of the oscilloscope photograph of Figure 23b shows the settling characteristics of the AD644. The lower trace represents the input to Figure 23a. The AD644 has been designed for fast settling to 0.01%, however, feedback components, circuit layout and circuit design must be carefully considered to obtain the optimum settling time.

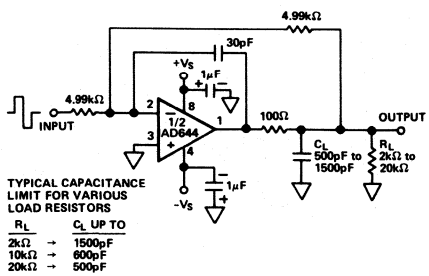
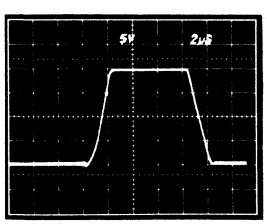


Figure 24. Circuit for Driving a Large Capacitive Load



Transient Response $R_L = 2k\Omega$ $C_L = 500pF$

The circuit in Figure 24 employs a 100Ω isolation resistor which enables the amplifier to drive capacitive loads exceeding 500pF; the resistor effectively isolates the high frequency feedback from the load and stabilizes the circuit. Low frequency feedback is returned to the amplifier summing junction via the low pass filter formed by the 100Ω series resistor and the load capacitance, C_L.

The low input bias current (35pA), low noise, high slew rate and high bandwidth characteristics of the AD644 make it suitable for electrometer applications such as photodiode preamplifiers and picoampere current-to-voltage converters. The use of guarding techniques in printed circuit board layout and construction is critical for achieving the ultimate in low leakage performance that the AD644 can deliver. The input guarding scheme shown in Figure 25 will minimize leakage as much as possible. The same layout should be used on both sides of a double side board. The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on a printed circuit; to minimize noise and leakage, such conductors should be replaced by rigid shielded cables.

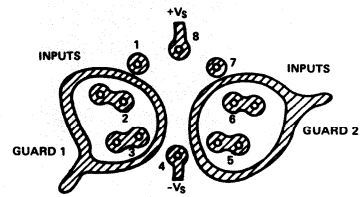


Figure 25. Board Layout for Guarding Inputs

INPUT PROTECTION

The AD644 is guaranteed for a maximum safe input potential equal to the power supply potential. The input stage design also allows differential input voltages of up to ±1 volt while maintaining the full differential input resistance of $10^{12}\Omega$. This makes the AD644 suitable for comparator situations employing a direct connection to high impedance source.

Many instrumentation situations, such as flame detectors in gas chromatographs, involve measurement of low level currents from high-voltage sources. In such applications, a sensor fault condition may apply a very high potential to the input of the current-to-voltage converting amplifier. This possibility necessitates some form of input protection. Many electrometer type devices, especially CMOS designs, can require elaborate zener protection schemes which often compromise overall performance. The AD644 requires input protection only if the source is not current-limited, and as such is similar to many JFET-input designs. The failure mode would be overheating from excess current rather than voltage breakdown. If the source is not current-limited, all that is required is a resistor in series with the affected input terminal so that the maximum overload current is 1.0mA (for example, 100kΩ for a 100 volt overload). This simple scheme will cause no significant reduction in performance and give complete overload protection. Figure 26 shows proper connections.

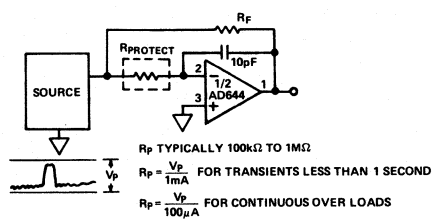


Figure 26. AD644 Input Protection

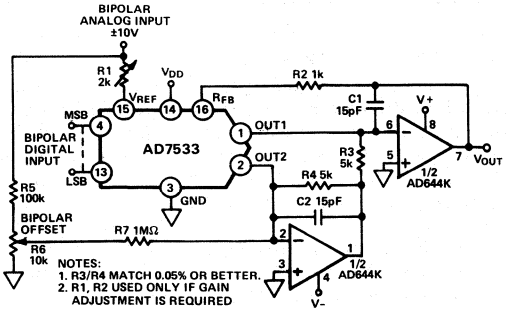


Figure 27a. AD644 Used as DAC Output Amplifiers

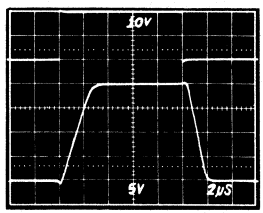


Figure 27b. Large Signal Response

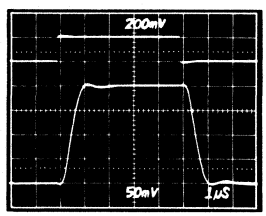


Figure 27c. Small Signal Response

Figure 27a illustrates the 10-bit digital-to-analog converter, AD7533, connected for bipolar operation. Since the digital input can accept bipolar numbers and V_{REF} can accept a bipolar analog input, the circuit can perform a 4-quadrant multiplying function. The photos exhibit the response to a step input at V_{REF}. Figure 27b is the large signal response and Figure 27c is the small signal response.

The output impedance of a CMOS DAC varies with the digital word thus changing the noise gain of the amplifier circuit. The effect will cause a nonlinearity the magnitude of which is dependent on the offset voltage of the amplifier. The AD644K with trimmed offset will minimize the effect. The Schottky protection diodes recommended for use with many older CMOS DACs are not required when using the AD644.

ACTIVE FILTERS

Literature on active filter techniques and characteristics based on operational amplifiers is readily available. The successful application of an active filter however, depends on the component selection to achieve the desired performance. The AD644 is recommended for filters in medical, instrumentation, data acquisition and audio applications, because of its high gain bandwidth figure, symmetrical slewing, low noise, and low offset voltage.

The state variable filter (Figure 28) is stable, easily tuned and is independent of circuit Q and gain. The use of the AD644 with its low input bias current simplifies the resistor (R3, R4) selection for the passband center frequency, circuit Q and voltage gain.

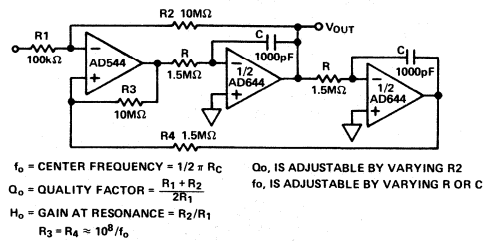


Figure 28. Band Pass State Variable Filter

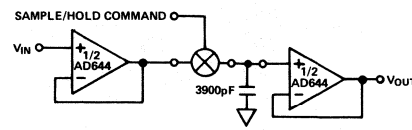


Figure 29. Sample and Hold Circuit

The sample and hold circuit, shown in Figure 29 is suitable for use with 8-bit A/D converters. The acquisition time using a 3900pF capacitor and fast CMOS SPST (ADG200) switch is 15μs.

The droop rate is very low 25 X 10^{-9} V/μs due to the low input bias currents of the AD644. Care should be taken to minimize leakage paths. Leakages around the hold capacitor will increase the droop rate and degrade performance.

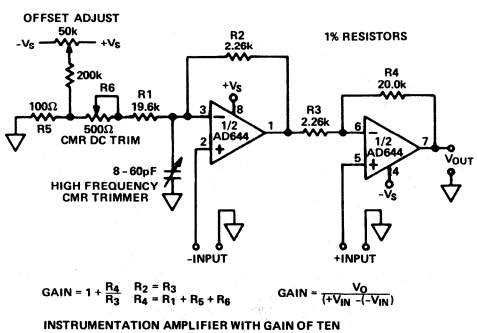


Figure 30. Wide Bandwidth Instrumentation Amplifier

The AD644 in the circuit of Figure 30 provides highly accurate signal conditioning with high frequency input signals. It provides an offset voltage drift of 10μV/°C, CMRR of 80dB over the range of dc to 10kHz and a bandwidth of 200kHz (-3dB) at 1V p-p output. The circuit of Figure 30 can be configured for a gain range of 2 to 1000 with a typical nonlinearity of 0.01% at a gain of 10.

Low Noise, Low Drift FET Op Amp

AD645

FEATURES

Improved Replacement for Burr-Brown OPA-111 and OPA-121 Op Amp

LOW NOISE

2 μV p–p max, 0.1 Hz to 10 Hz

10 nV/√Hz max at 10 kHz

11 fA p–p Current Noise 0.1 Hz to 10 Hz

HIGH DC ACCURACY

250 μV max Offset Voltage

1 μV/°C max Drift

1.5 pA max Input Bias Current

114 dB Open-Loop Gain

Available in Plastic Mini-DIP or 8-Pin Header Packages

Both "A" Grade and MIL-STD-883B Chips (Die) Are Available

APPLICATIONS

Low Noise Photodiode Preamps

CT Scanners

Precision I-V Converters

IMPROVED DRIFT

PRODUCT DESCRIPTION

The AD645 is a low noise, precision FET input op amp. It offers the pico amp level input currents of a FET input device coupled with offset drift and input voltage noise comparable to a high performance bipolar input amplifier.

The AD645 has been improved to offer the lowest offset drift in a FET op amp, 1 μV/°C. Offset voltage drift is measured and trimmed at wafer level for the lowest cost possible. An inherently low noise architecture and advanced manufacturing techniques result in a device with a guaranteed low input voltage noise of 2 μV p–p, 0.1 Hz to 10 Hz. This level of dc performance along with low input currents make the AD645 an excellent choice for high impedance applications where stability is of prime concern.

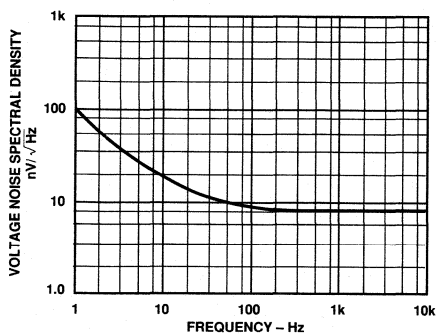
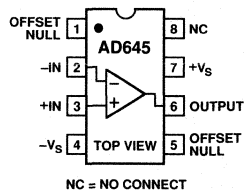


Figure 1. AD645 Voltage Noise Spectral Density vs. Frequency

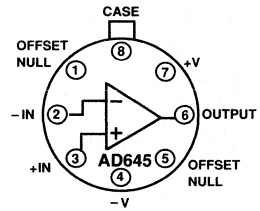
CONNECTION DIAGRAMS

8-Pin Plastic Mini-DIP (N) Package



NC = NO CONNECT

TO-99 (H) Package



NOTE: CASE IS CONNECTED TO PIN 8

The AD645 is available in six performance grades. The AD645J and AD645K are rated over the commercial temperature range of 0°C to +70°C. The AD645A, AD645B, and the ultraprecision AD645C are rated over the industrial temperature range of −40°C to 85°C. The AD645S is rated over the military temperature range of −55°C to 125°C and is available processed to MIL-STD-883B.

The AD645 is available in an 8-pin plastic mini-DIP, 8-pin header, or in die form.

PRODUCT HIGHLIGHTS

1. Guaranteed and tested low frequency noise of 2 μV p–p max and 20 nV/√Hz at 100 Hz makes the AD645C ideal for low noise applications where a FET input op amp is needed.
2. Low V_{OS} drift of 1 μV/°C max makes the AD645C an excellent choice for applications requiring ultimate stability.
3. Low input bias current and current noise (11 fA p–p 0.1 Hz to 10 Hz) allow the AD645 to be used as a high precision preamp for current output sensors such as photodiodes, or as a buffer for high source impedance voltage output sensors.

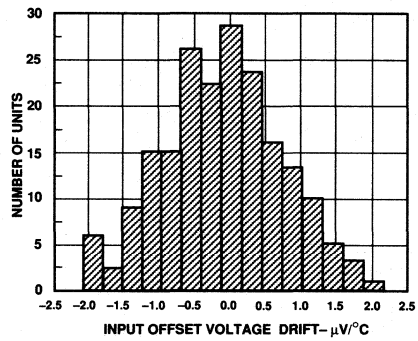


Figure 2. Typical Distribution of Average Input Offset Voltage Drift (196 Units)

AD645—SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD645J/A			AD645K/B			AD645C			AD645S			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
INPUT OFFSET VOLTAGE[1]														
Initial Offset			100	500		50	250		50	250		100	500	μV
Offset	T_{MIN}–T_{MAX}		300	1000		100	400		75	300		500	1500	μV
Drift (Average)			3	10/5		1	5/2		0.5	1		4	10	μV/°C
vs. Supply (PSRR)		90	110		94	110		94	110		90	110		dB
vs. Supply	T_{MIN}–T_{MAX}		100		90	100		90	100		86	95		dB
INPUT BIAS CURRENT[2]														
Either Input	V_{CM} = 0 V		0.7/1.8	3/5		0.7/1.8	1.5/3		1.8	3		1.8	5	pA
Either Input @ T_{MAX}	V_{CM} = 0 V		16/115			16/115			115			1800		pA
Either Input	V_{CM} = +10 V		0.8/1.9			0.8/1.9			1.9			1.9		pA
Offset Current	V_{CM} = 0 V		0.1	1.0		0.1	0.5		0.1	0.5		0.1	1.0	pA
Offset Current @ T_{MAX}	V_{CM} = 0 V		2/6			2/6			6			100		pA
INPUT VOLTAGE NOISE	0.1 to 10 Hz		1.0	3.0		1.0	2.5		1	2		1.0	3.3	μV p–p
	f = 10 Hz		20	50		20	40		20	40		20	50	nV/√Hz
	f = 100 Hz		10	30		10	20		10	20		10	30	nV/√Hz
	f = 1 kHz		9	15		9	12		9	12		9	15	nV/√Hz
	f = 10 kHz		8	10		8	10		8	10		8	10	nV/√Hz
INPUT CURRENT NOISE	f = 0.1 to 10 Hz		11	20		11	15		11	15		11	20	fA p–p
	f = 0.1 thru 20 kHz		0.6	1.1		0.6	0.8		0.6	0.8		0.6	1.1	fA/√Hz
FREQUENCY RESPONSE														
Unity Gain, Small Signal			2			2			2			2		MHz
Full Power Response	V_O = 20 V p–p													
	R_{LOAD} = 2 kΩ	16	32		16	32		16	32		16	32		kHz
Slew Rate, Unity Gain	V_{OUT} = 20 V p–p													
	R_{LOAD} = 2 kΩ	1	2		1	2		1	2		1	2		V/μs
SETTLING TIME[3]														
To 0.1%			6			6			6			6		μs
To 0.01%			8			8			8			8		μs
Overload Recovery[4]	50% Overdrive		5			5			5			5		μs
Total Harmonic Distortion	f = 1 kHz, R_{LOAD} ≥ 2 kΩ, V_O = 3 V rms		0.0006			0.0006			0.0006			0.0006		%
INPUT IMPEDANCE														
Differential	V_{DIFF} = ±1 V		10^{12}‖1			10^{12}‖1			10^{12}‖1			10^{12}‖1		Ω‖pF
Common-Mode			10^{14}‖2.2			10^{14}‖2.2			10^{14}‖2.2			10^{14}‖2.2		Ω‖pF
INPUT VOLTAGE RANGE														
Differential[5]			±20			±20			±20			±20		V
Common-Mode Voltage		±10	+11,−10.4		±10	+11,−10.4		±10	+11,−10.4		±10	+11,−10.4		V
Over Max Oper. Range		±10			±10			±10			±10			V
Common-Mode Rejection Ratio	V_{CM} = ±10 V	90	110		94	110		94	110		90	110		dB
	T_{MIN}–T_{MAX}		100		90	100		90	100		86	100		dB
OPEN-LOOP GAIN	V_O = ±10 V													
	R_{LOAD} ≥ 2 kΩ	114	130		120	130		120	130		114	130		dB
	T_{MIN}–T_{MAX}				114			114			110			dB
OUTPUT CHARACTERISTICS														
Voltage	R_{LOAD} ≥ 2 kΩ	±10	±11		±10	±11		±10	±11		±10	±11		V
	T_{MIN}–T_{MAX}	±10			±10			±10			±10			V
Current	V_{OUT} = ±10 V	±5	±10		±5	±10		±5	±10		±5	±10		mA
	Short Circuit		±15			±15			±15			±15		mA
POWER SUPPLY														
Rated Performance			±15			±15			±15			±15		V
Operating Range		±5		±18	±5		±18	±5		±18	±5		±18	V
Quiescent Current			3.0	3.5		3.0	3.5		3.0	3.5		3.0	3.5	mA
Transistor Count	# of Transistors		62			62			62			62		

NOTES

[1]Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperature, the current doubles every 10°C.

[3]Gain = −1, R_{LOAD} = 2 kΩ.

[4]Defined as the time required for the amplifier's output to return to normal operation after removal of a 50% overload from the amplifier input.

[5]Defined as the maximum continuous voltage between the inputs such that neither input exceeds ±10 V from ground.

All min and max specifications are guaranteed.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2] (@ T_A = +25°C)
8-Pin Header Package . . . . . 500 mW
8-Pin Mini-DIP Package . . . . . 750 mW
Input Voltage . . . . . $\pm V_S$
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range (H) . . . . . −65°C to +150°C
Storage Temperature Range (N) . . . . . −65°C to +125°C
Operating Temperature Range
AD645J/K . . . . . 0°C to +70°C
AD645A/B/C . . . . . −40°C to +85°C
AD645S . . . . . −55°C to +125°C
Lead Temperature Range
(Soldering 60 seconds) . . . . . 300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Thermal Characteristics:
8-Pin Plastic Mini-DIP Package: θ_{JA} = 100°C/Watt
8-Pin Header Package: θ_{JA} = 200°C/Watt

2

CAUTION

ESD (electrostatic discharge) sensitive device. Charges as high as 4000 V readily accumulate on the human body and test equipment and discharge without detection. Therefore, reasonable ESD precautions are recommended to avoid functional damage or performance degradation. Unused devices should be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' *ESD Prevention Manual.*

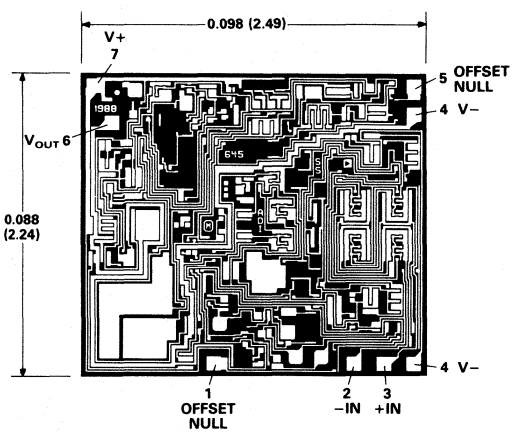
ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
AD645JN	0°C to +70°C	N-8
AD645KN	0°C to +70°C	N-8
AD645AH	−40°C to +85°C	H-08A
AD645BH	−40°C to +85°C	H-08A
AD645CH	−40°C to +85°C	H-08A
AD645SH	−55°C to +125°C	H-08A
AD645SH/883B	−55°C to +125°C	H-08A

NOTES
[1]"A" and "S" Grade Chips are also available.
[2]N = Plastic mini-DIP; H = Metal Can. For outline information see Package Information section.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



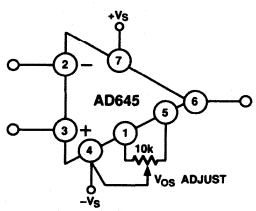


Figure 3. AD645 Offset Null Configuration

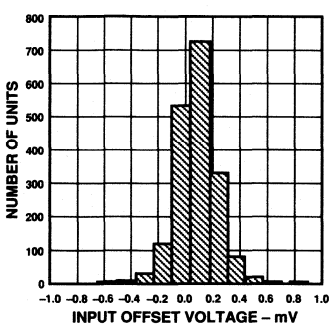


Figure 4. Typical Distribution of Input Offset Voltage (1855 Units)

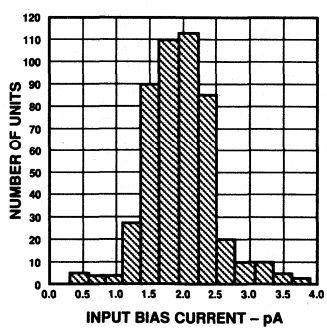


Figure 5. Typical Distribution of Input Bias Current (576 Units)

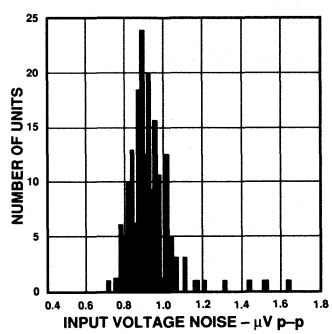


Figure 6. Typical Distribution of 0.1 Hz to 10 Hz Voltage Noise (202 Units)

AD645—Typical Characteristics (@ +25°C, ±15 V unless otherwise stated)

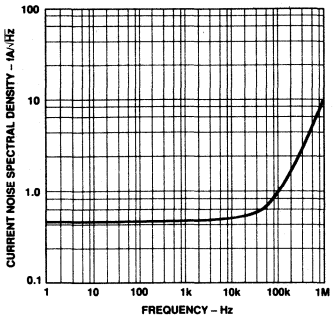


Figure 7. Current Noise Spectral Density vs. Frequency

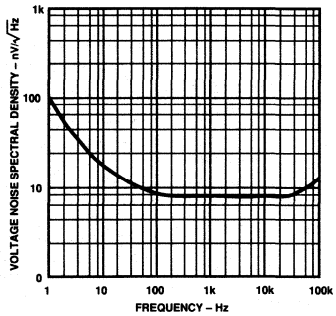


Figure 8. Voltage Noise Spectral Density vs. Frequency

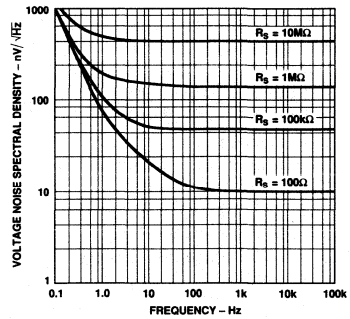


Figure 9. Voltage Noise Spectral Density vs. Frequency for Various Source Resistances

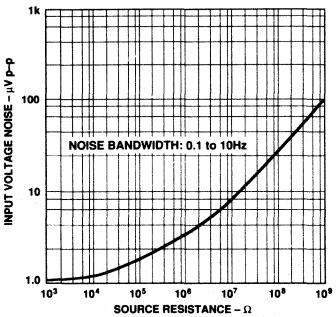


Figure 10. Input Voltage Noise vs. Source Resistance

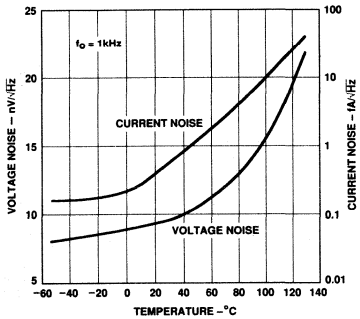


Figure 11. Voltage and Current Noise Spectral Density vs. Temperature

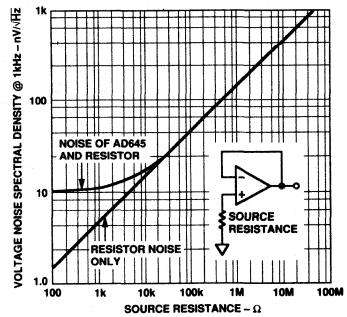


Figure 12. Voltage Noise Spectral Density @ 1 kHz vs. Source Resistance

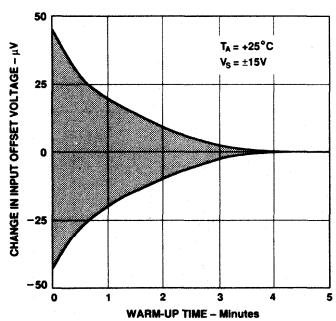


Figure 13. Change in Input Offset Voltage vs. Warmup Time

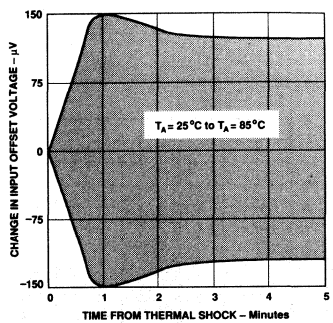


Figure 14. Change in Input Offset Voltage vs. Time from Thermal Shock

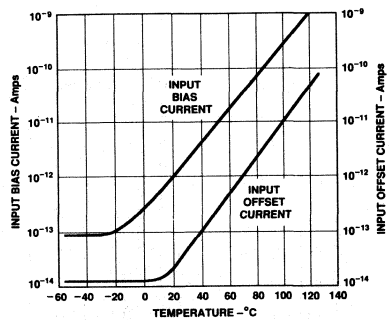


Figure 15. Input Bias and Offset Currents vs. Temperature

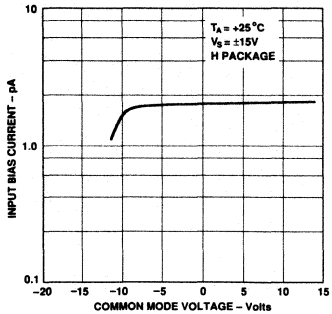


Figure 16. Input Bias Current vs. Common-Mode Voltage

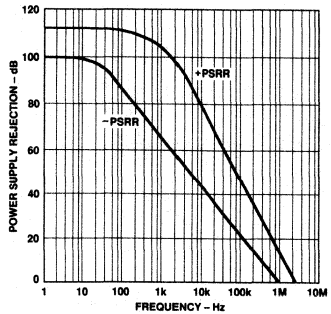


Figure 17. Power Supply Rejection vs. Frequency

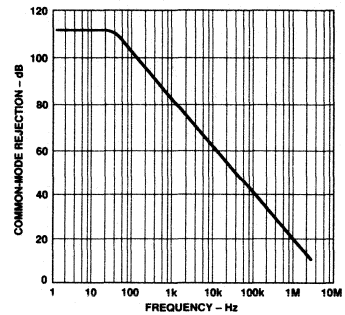


Figure 18. Common-Mode Rejection vs. Frequency

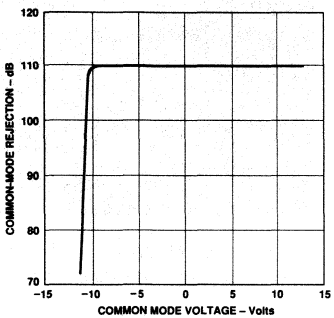


Figure 19. Common-Mode Rejection vs. Input Common-Mode Voltage

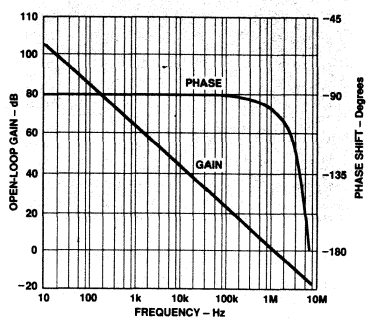


Figure 20. Open-Loop Gain and Phase Shift vs. Frequency

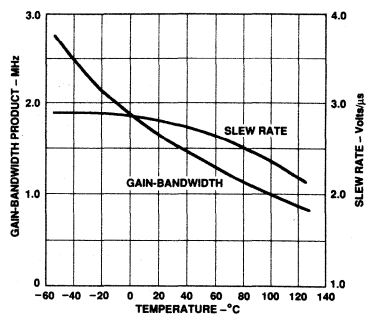


Figure 21. Gain-Bandwidth Product and Slew Rate vs. Temperature

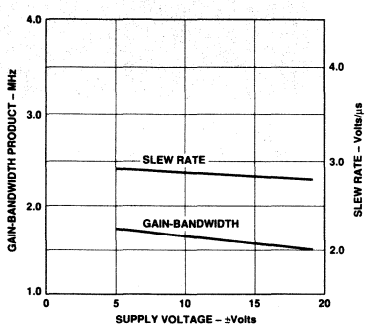


Figure 22. Gain-Bandwidth and Slew Rate vs. Supply Voltage

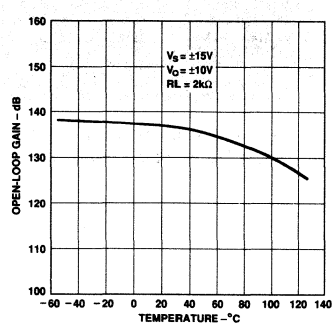


Figure 23. Open-Loop Gain vs. Temperature

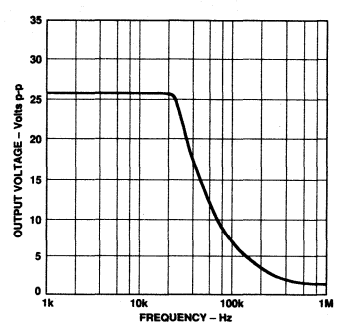


Figure 24. Large Signal Frequency Response

AD645—Typical Characteristics

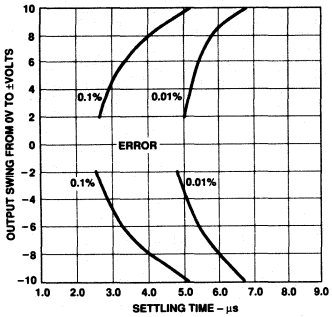


Figure 25. Output Swing and Error vs. Settling Time

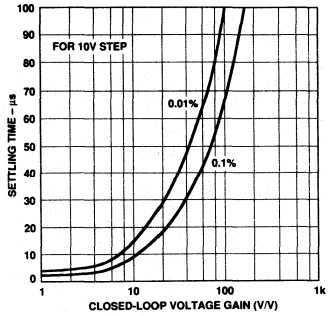


Figure 26. Settling Time vs. Closed-Loop Voltage Gain

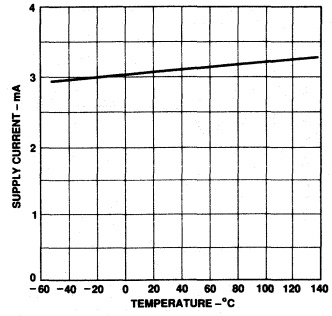


Figure 27. Supply Current vs. Temperature

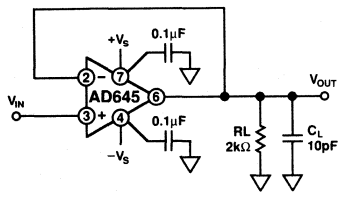


Figure 28a. Unity-Gain Follower

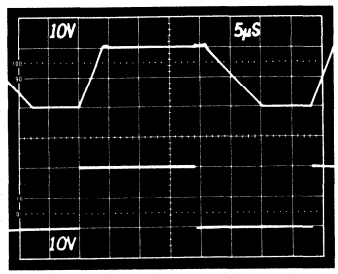


Figure 28b. Unity-Gain Follower Large Signal Pulse Response

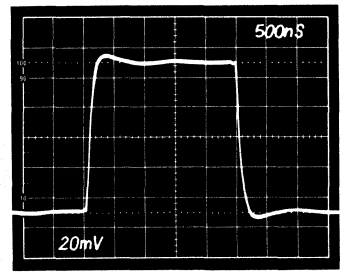


Figure 28c. Unity-Gain Follower Small Signal Pulse Response

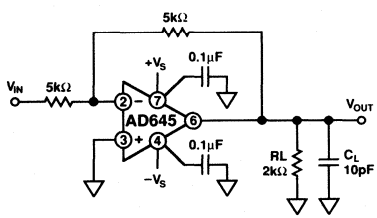


Figure 29a. Unity-Gain Inverter

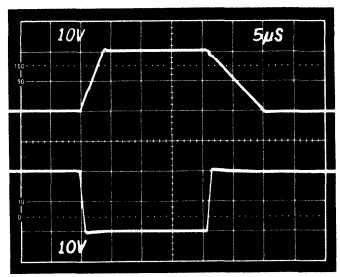


Figure 29b. Unity-Gain Inverter Large Signal Pulse Response

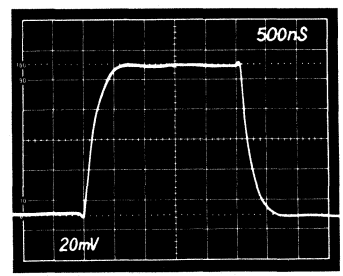


Figure 29c. Unity-Gain Inverter Small Signal Pulse Response

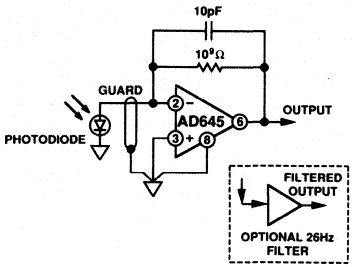


Figure 30. The AD645 Used as a Sensitive Preamplifier

Preamplifier Applications

The low input current and offset voltage levels of the AD645 together with its low voltage noise make this amplifier an excellent choice for preamplifiers used in sensitive photodiode applications. In a typical preamp circuit, shown in Figure 30, the output of the amplifier is equal to:

$$V_{OUT} = I_D\,(Rf) = Rp\,(P)\,Rf$$

where:

I_D = photodiode signal current (Amps)

Rp = photodiode sensitivity (Amp/Watt)

Rf = the value of the feedback resistor, in ohms.

P = light power incident to photodiode surface, in watts.

An equivalent model for a photodiode and its dc error sources is shown in Figure 31. The amplifier's input current, I_B, will contribute an output voltage error which will be proportional to the value of the feedback resistor. The offset voltage error, V_{OS}, will cause a "dark" current error due to the photodiode's finite shunt resistance, Rd. The resulting output voltage error, V_E, is equal to:

$$V_E = (1 + Rf/Rd)\,V_{OS} + Rf\,I_B$$

A shunt resistance on the order of 10^9 ohms is typical for a small photodiode. Resistance Rd is a junction resistance which will typically drop by a factor of two for every 10°C rise in temperature. In the AD645, both the offset voltage and drift are low, this helps minimize these errors.

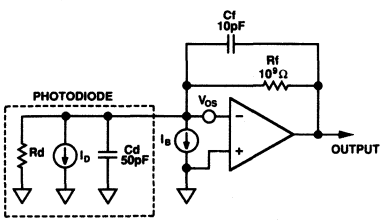


Figure 31. A Photodiode Model Showing DC Error Sources

Minimizing Noise Contributions

The noise level limits the resolution obtainable from any preamplifier. The total output voltage noise divided by the feedback resistance of the op amp defines the minimum detectable signal current. The minimum detectable current divided by the photodiode sensitivity is the minimum detectable light power.

Sources of noise in a typical preamp are shown in Figure 32. The total noise contribution is defined as:

$$\overline{V_{OUT}} = \sqrt{(\overline{i_n}^2 + \overline{i_f}^2 + \overline{i_s}^2)\left(\frac{Rf}{1 + s\,(Cf)\,Rf}\right)^2 + (\overline{en}^2)\left(1 + \frac{Rf}{Rd}\left(\frac{1 + s\,(Cd)\,Rd}{1 + s\,(Cf)\,Rf}\right)\right)^2}$$

Figure 33, a spectral density versus frequency plot of each source's noise contribution, shows that the bandwidth of the amplifier's input voltage noise contribution is much greater than its signal bandwidth. In addition, capacitance at the summing junction results in a "peaking" of noise gain in this configuration. This effect can be substantial when large photodiodes with large shunt capacitances are used. Capacitor Cf sets the signal bandwidth and also limits the peak in the noise gain. Each source's rms or root-sum-square contribution to noise is obtained by integrating the sum of the squares of all the noise sources and then by obtaining the square root of this sum. Minimizing the total area under these curves will optimize the preamplifier's overall noise performance.

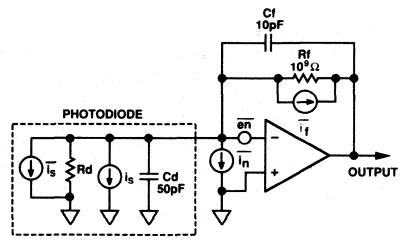


Figure 32. Noise Contributions of Various Sources

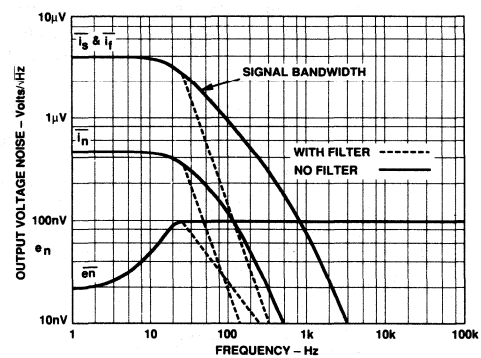


Figure 33. Voltage Noise Spectral Density of the Circuit of Figure 32 with and without an Output Filter

An output filter with a passband close to that of the signal can greatly improve the preamplifier's signal to noise ratio. The photodiode preamplifier shown in Figure 32—without a bandpass filter—has a total output noise of 50 μV rms. Using a 26 Hz single pole output filter, the total output noise drops to 23 μV rms, a factor of 2 improvement with no loss in signal bandwidth.

Using a "T" Network

A "T" network, shown in Figure 34, can be used to boost the effective transimpedance of an I to V converter, for a given feedback resistor value. Unfortunately, amplifier noise and offset voltage contributions are also amplified by the "T" network gain. A low noise, low offset voltage amplifier, such as the AD645, is needed for this type of application.

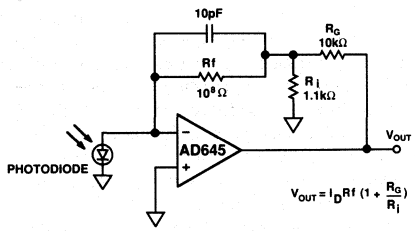


Figure 34. A Photodiode Preamp Employing a "T" Network for Added Gain

A pH Probe Buffer Amplifier

A typical pH probe requires a buffer amplifier to isolate its 10^6 to 10^9 Ω source resistance from external circuitry. Just such an amplifier is shown in Figure 35. The low input current of the AD645 allows the voltage error produced by the bias current and electrode resistance to be minimal. The use of guarding, shielding, high insulation resistance standoffs, and other such standard methods used to minimize leakage are all needed to maintain the accuracy of this circuit.

The slope of the pH probe transfer function, 50 mV per pH unit at room temperature, has a +3300 ppm/°C temperature coefficient. The buffer of Figure 35 provides an output voltage equal to 1 volt/pH unit. Temperature compensation is provided by resistor RT which is a special temperature compensation resistor, part number Q81, 1 kΩ, 1%, +3500 ppm/°C, available from Tel Labs Inc.

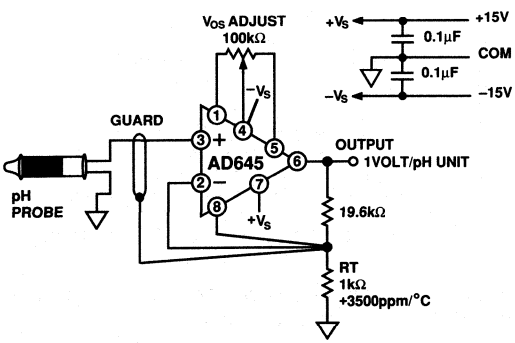


Figure 35. A pH Probe Amplifier

Circuit Board Notes

The AD645 is designed for through hole mount into PC boards. Maintaining picoampere level resolution in that environment requires a lot of care. Since both the printed circuit board and the amplifier's package have a finite resistance, the voltage difference between the amplifier's input pin and other pins (or traces on the PC board) will cause parasitic currents to flow into (or out of) the signal path. These currents can easily exceed the 1.5 pA input current level of the AD645 unless special precautions are taken. Two successful methods for minimizing leakage are: guarding the AD645's input lines and maintaining adequate insulation resistance.

Guarding the input lines by completely surrounding them with a metal conductor biased near the input lines' potential has two major benefits. First, parasitic leakage from the signal line is reduced, since the voltage between the input line and the guard is very low. Second, stray capacitance at the input terminal is minimized which in turn increases signal bandwidth. In the header or can package, the case of the AD645 is connected to Pin 8 so that it may be tied to the input potential (when operating as a follower) or tied to ground (when operating as an inverter). The AD645's positive input (Pin 3) is located next to the negative supply voltage pin (Pin 4). The negative input (Pin 2) is next to the balance adjust pin (Pin 1) which is biased at a potential close to that of the negative supply voltage. Note that any guard traces should be placed on *both* sides of the board. In addition, the input trace should be guarded along both of its edges, along its entire length.

Contaminants such as solder flux, on the board's surface and on the amplifier's package, can greatly reduce the insulation resistance and also increase the sensitivity to atmospheric humidity. Both the package and the board must be kept clean and dry. An effective cleaning procedure is to: first, swab the surface with high grade isopropyl alcohol, then rinse it with deionized water, and finally, bake it at 80°C for 1 hour. Note that if either polystyrene or polypropylene capacitors are used on the printed circuit board that a baking temperature of 70°C is safer, since both of these plastic compounds begin to melt at approximately +85°C.

ANALOG DEVICES

Ultralow Drift, Dual BiFET Op Amp

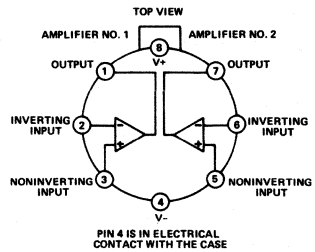
AD647

FEATURES

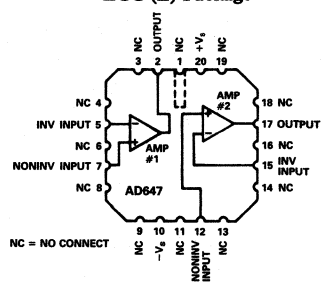
- Low Offset Voltage Drift
- Matched Offset Voltage
- Matched Offset Voltage Over Temperature
- Matched Bias Current
- Crosstalk: −124dB at 1kHz
- Low Bias Current: 35pA max Warmed Up
- Low Offset Voltage: 250μV max
- Low Input Voltage: 2μV p–p
- High Open Loop Gain: 108dB
- Low Quiescent Current: 2.8mA max
- Low Total Harmonic Distortion
- Standard Dual Amplifier Pinout
- Available in Hermetic Metal Can Package, Hermetic Surface Mount (20-Pin LCC) and Chip Form
- MIL-STD-883B Processing Also Available
- Single Version Available: AD547

PIN CONFIGURATIONS

TO-99 (H) Package



LCC (E) Package



PRODUCT DESCRIPTION

The AD647 is an ultralow drift, dual JFET amplifier that combines high performance and convenience in a single package.

The AD647 uses the most advanced ion-implantation and laser wafer drift trimming technologies to achieve the highest performance currently available in a dual JFET. Ion-implantation permits the fabrication of matched JFETs on a monolithic bipolar chip. Laser wafer drift trimming trims both the initial offset voltage and its drift with temperature to provide offsets as low as 100μV (250μV max) and drifts of 2.5μV/°C max.

In addition to outstanding individual amplifier performance, the AD647 offers guaranteed and tested matching performance on critical parameters such as offset voltage, offset voltage drift and bias currents.

The high level of performance makes the AD647 especially well suited for high precision instrumentation amplifier applications that previously would have required the costly selection and matching of space wasting single amplifiers.

The AD647 is offered in four performance grades, three commercial (the J, K and L) and one extended (the S). All are supplied in hermetically sealed 8-pin TO-99 packages and are available processed to MIL-STD-883B. The LCC version is also available processed to MIL-STD-883B.

PRODUCT HIGHLIGHTS

1. The AD647 is guaranteed and tested to tight matching specifications to ensure high performance and to eliminate the selection and matching of single devices.
2. Laser wafer drift trimming reduces offset voltage and offset voltage drifts to 250μV and 2.5μV/°C max.
3. Voltage noise is guraanteed at 4μV p–p max (0.1 to 10Hz) on K, L and S grades.
4. Bias current (35pA K, L, S; 75pA J) is specified after five minutes of operation.
5. Total supply current is a low 2.8mA max.
6. High open loop gain ensures high linearity in precision instrumentation amplifier applications.
7. The standard dual amplifier pinout permits the direct substitution of the AD647 for lower performance devices.
8. The AD647 is available in chip form.

AD647—SPECIFICATIONS (@ +25°C and V_S = ±15V dc)

Model	AD647J Min	AD647J Typ	AD647J Max	AD647K Min	AD647K Typ	AD647K Max	AD647L Min	AD647L Typ	AD647L Max	AD647S Min	AD647S Typ	AD647S Max	Units
OPEN LOOP GAIN													
V_O = ±10V, $R_L \geq 2k\Omega$	**100,000**			**250,000**			**250,000**			**250,000**			V/V
T_{min} to T_{max}, R_L = 2kΩ	100,000			**250,000**			**250,000**			**100,000**			V/V
OUTPUT CHARACTERISTICS													
Voltage @ R_L = 2kΩ, T_{min} to T_{max}	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Voltage @ R_L = 10kΩ, T_{min} to T_{max}	**±12**	±13		**±12**	±13		**±12**	±13		**±12**	±13		V
Short Circuit Current		25			25			25			25		mA
FREQUENCY RESPONSE													
Unity Gain Small Signal		1.0			1.0			1.0			1.0		MHz
Full Power Response		50			50			50			50		kHz
Slew Rate, Unity Gain	**2.0**	3.0		**2.0**	3.0		**2.0**	3.0		**2.0**	3.0		V/μs
INPUT OFFSET VOLTAGE[1]													
Initial Offset			**1.0**			**0.5**			**0.25**			**0.5**	mV
Input Offset Voltage vs. Temp.			**10**			5			**2.5**			**5.0**	μV/°C
Input Offset Voltage vs. Supply, T_{min} to T_{max}			200			**100**			**100**			**100**	μV/V
INPUT BIAS CURRENT[2]													
Either Input		10	75		10	**35**		10	**35**		10	**35**	pA
Offset Current		5			2			2			2		pA
MATCHING CHARACTERISTICS[3]													
Input Offset Voltage			**1.0**			**0.5**			**0.25**			**0.5**	mV
Input Offset Voltage T_{min} to T_{max}			**10**			5			**2.5**			**10.0**	μV/°C
Input Bias Current			**35**			**25**			**25**			**25**	pA
Crosstalk		−124			−124			−124			−124		dB
INPUT IMPEDANCE													
Differential		10^{12}‖6			10^{12}‖6			10^{12}‖6			10^{12}‖6		MΩ‖pF
Common Mode		10^{12}‖6			10^{12}‖6			10^{12}‖6			10^{12}‖6		MΩ‖pF
INPUT VOLTAGE RANGE													
Differential[4]		±20			±20			±20			±20		V
Common Mode	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Common-Mode Rejection	**76**			**80**			**80**			**80**			dB
INPUT NOISE													
Voltage 0.1Hz to 10Hz		2				**4**			**4**			**4**	μV p-p
f = 10Hz		70			70			70			70		nV/√Hz
f = 100Hz		45			45			45			45		nV/√Hz
f = 1kHz		30			30			30			30		nV/√Hz
f = 10kHz		25			25			25			25		nV/√Hz
POWER SUPPLY													
Rated Performance		±15			±15			±15			±15		V
Operating	±5		±18	±5		±18	±5		±18	±5		±18	V
Quiescent Current			**2.8**			**2.8**			**2.8**			**2.8**	mA
TEMPERATURE RANGE													
Operating, Rated Performance	0		+70	0		+70	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
PACKAGE OPTIONS[5]													
TO-99 Style (H-08B)		AD647JH			AD647KH			AD647LH			AD647SH		
LCC (E-20A)											AD647SE, AD647SE/883B		
Chips		AD647JChips									AD647SChips		

NOTES

[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]Bias Current specifications are guaranteed at maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[3]Matching is defined as the difference between parameters of the two amplifiers.

[4]Defined as the maximum safe voltage between inputs, such that neither exceeds ±10V from ground.

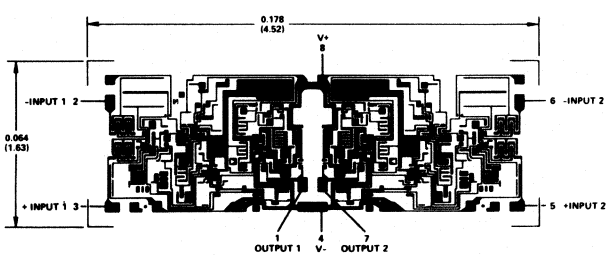
[5]For outline information see Package Information section.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



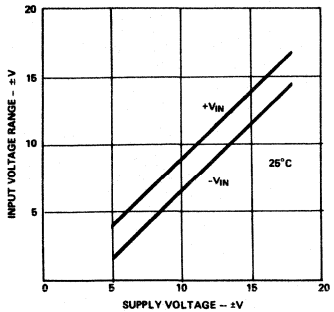


Figure 1. Input Voltage Range vs. Supply Voltage

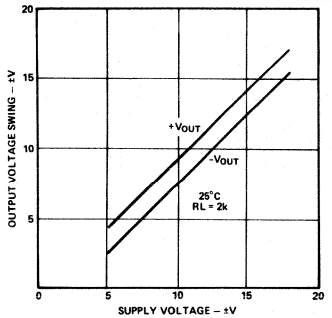


Figure 2. Output Voltage Swing vs. Supply Voltage

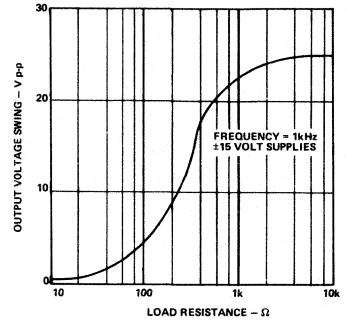


Figure 3. Output Voltage Swing vs. Load Resistance

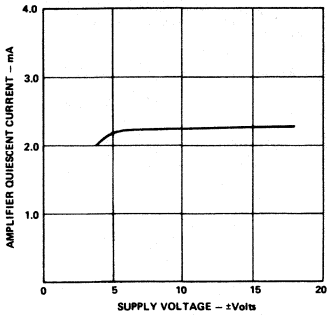


Figure 4. Quiescent Current vs. Supply Voltage

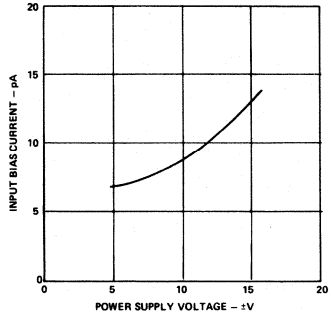


Figure 5. Input Bias Current vs. Power Supply Voltage

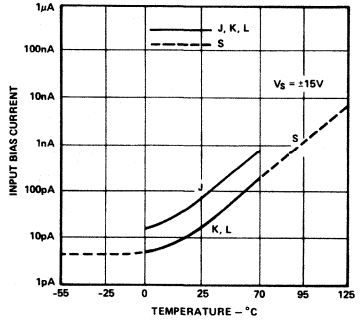


Figure 6. Input Bias Current vs. Temperature

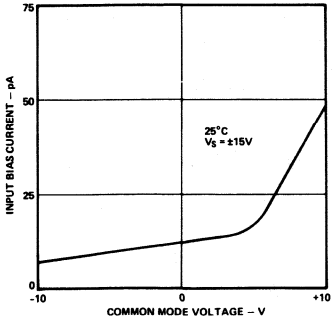


Figure 7. Input Bias Current vs. CMV

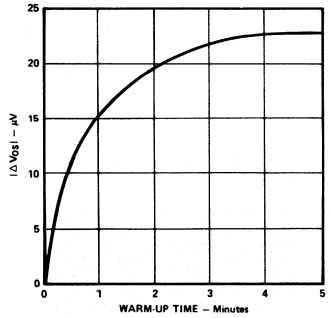


Figure 8. Change in Offset Voltage vs. Warm-Up Time

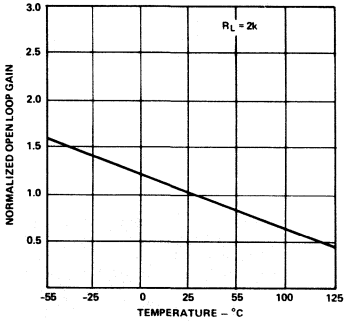


Figure 9. Open Loop Gain vs. Temperature

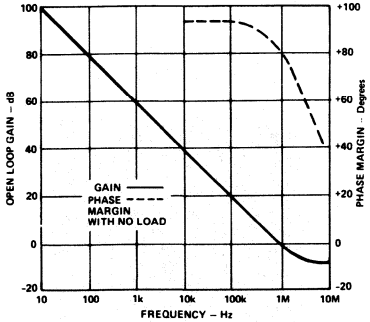


Figure 10. Open Loop Frequency Response

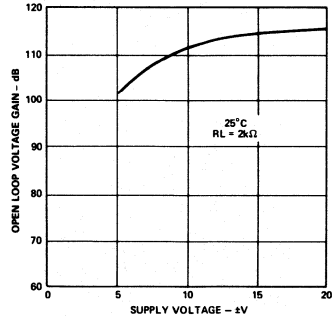


Figure 11. Open Loop Voltage Gain vs. Supply Voltage

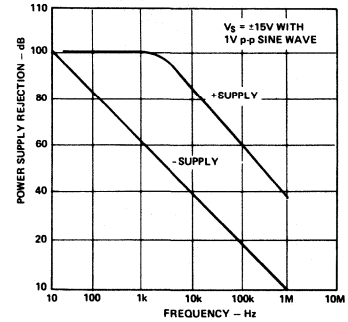


Figure 12. Power Supply Rejection vs. Frequency

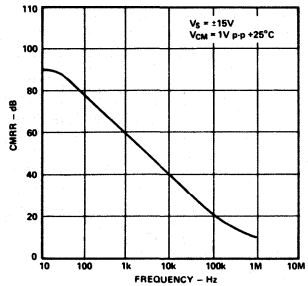


Figure 13. Common-Mode Rejection Ratio vs. Frequency

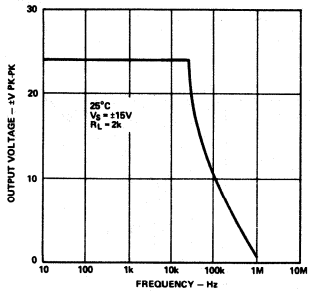


Figure 14. Large Signal Frequency Response

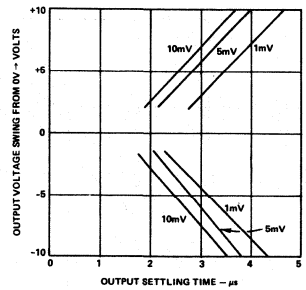


Figure 15. Output Settling Time vs. Output Swing and Error (Circuit of Figure 23)

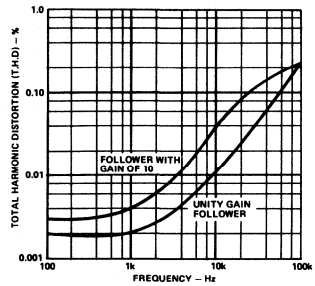


Figure 16. Total Harmonic Distortion vs. Frequency

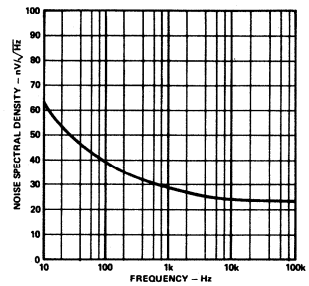


Figure 17. Input Noise Voltage Spectral Density

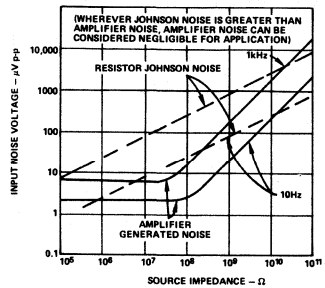
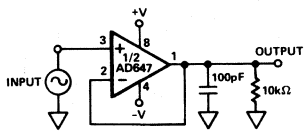
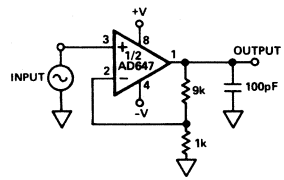


Figure 18. Total RMS Noise vs. Source Impedance



a. Unity Gain Follower



b. Follower with Gain = 10

Figure 19. T.H.D. Test Circuits

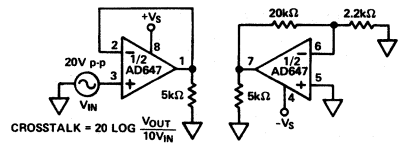


Figure 20. Crosstalk Test Circuit

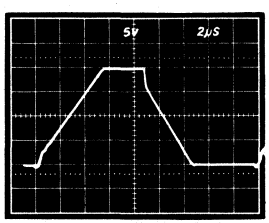


Figure 21a. Unity Gain Follower Pulse Response (Large Signal)

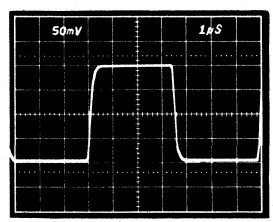


Figure 21b. Unity Gain Follower Pulse Response (Small Signal)

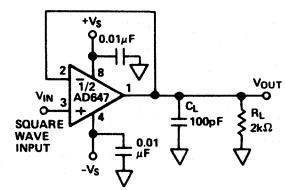


Figure 21c. Unity Gain Follower

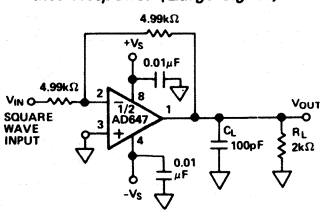


Figure 22a. Unity Gain Inverter

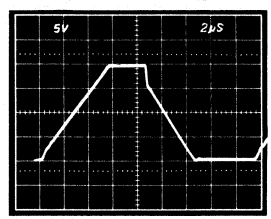


Figure 22b. Unity Gain Inverter Pulse Response (Large Signal)

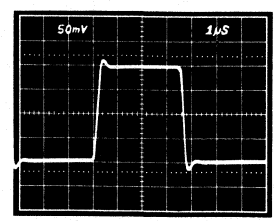


Figure 22c. Unity Gain Inverter Pulse Response (Small Signal)

APPLICATION NOTES

The AD647 is fully specified under actual operating conditions to insure high performance in any application, but there are some steps that will improve on even this high level of performance.

The bias current of a JFET amplifier doubles with every 10°C increase in junction temperature. Any heat source that can be eliminated or minimized will significantly improve bias current performance. To account for normal power dissipation, the largest contributor to chip self-heating, the bias currents of the AD647 are guaranteed fully warmed up with ±15V supplies. A decrease in supply voltage will decrease power consumption, resulting in a corresponding drop in bias currents.

Open loop gain and bias currents, to some extent, are affected by output loading. In applications where high linearity is essential, load impedance should be kept as high as possible to minimize degradation of open loop gain.

The outstanding ac and dc performance of the AD647 make it an ideal choice for critical instrumentation applications. In such applications, leakage paths, line losses and external noise sources should be considered in the layout of printed circuit boards. A guard ring surrounding the inputs and connected to a low impedance potential (at the same level as the inputs) should be placed on both sides of the circuit board. This will eliminate leakage paths that could degrade bias current performance. All signal paths should be shielded to minimize noise pick-up.

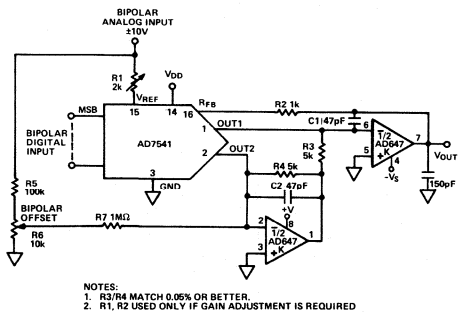


Figure 23. AD647 Used as DAC Output Amplifier

A CMOS DAC AMPLIFIER

The output impedance of a CMOS DAC, such as the AD7541, varies with digital input code. This causes a corresponding variation in the noise gain of the DAC-amplifier combination. This noise gain modulation introduces a nonlinearity whose magnitude is dependent on the amount of offset voltage present.

Laser wafer drift trimming lowers the initial offset voltage and the offset voltage drift of the AD647, therefore minimizing the effect of this nonlinearity and its drift with temperature. This, in conjunction with the low bias current and high open loop gain, makes the AD647 ideal for DAC output amplifier applications.

THE AD647 USED WITH THE AD7546

Figure 24 shows the AD647 used with the AD7546 16-bit segment DAC. In this application, amplifier performance is critical to the overall performance of the AD7546. A1 is used as a dual precision buffer. Here the offset voltage match, low offset voltage and high open loop gain of the AD647 ensure monotonicity and high linearity over the entire operating temperature range. A2 serves a dual function: amplifier A is a Track and Hold circuit that deglitches the DAC output and amplifier B acts as an output amplifier. The performance of the amplifiers of A2 is crucial to the accuracy of the system. The errors of these amplifiers are added to the errors due strictly to DAC imperfections. For this reason great care should be used in the selection of these amplifiers. The matching characteristics, low bias current and low temperature coefficients of the AD647 make it ideal for this application.

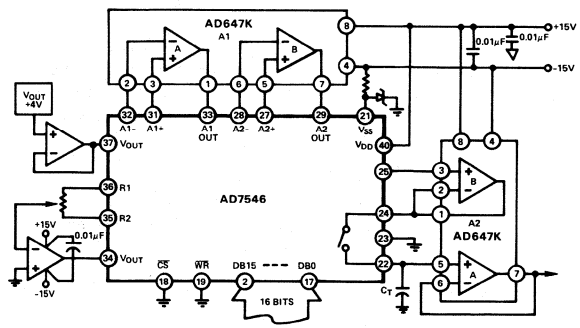


Figure 24. AD647 Used with AD7546 16-Bit DAC

USING THE AD647 IN LOG AMPLIFIER APPLICATIONS

Log amplifiers or log ratio amplifiers are useful in a wide range of analog computational applications, ranging from the simple linearization of exponential transducer outputs to the use of logarithms in computations involving multi-term products or arbitrary exponents. Log amps also facilitate the compression of wide ranging analog input signals into a range that can be easily handled using standard circuit techniques.

The picoamp level input current and low offset voltage of the AD647 make it suitable for wide dynamic range log amplifiers. Figure 27 is a schematic of a log ratio circuit employing the AD647 that can achieve less than 1% conformance error over 5 decades of current input, 1nA to 100μA. For voltage inputs, the dynamic range is typically 50mV to 10V for 1% error, limited on the low end by the amplifiers' input offset voltage.

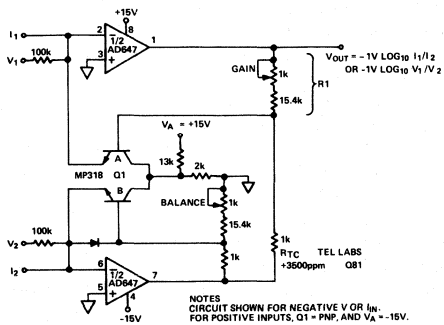


Figure 25. Log-Ratio Amplifier

The conversion between current (or voltage) input and log output is accomplished by the base-emitter junctions of the dual transistor Q1. Assuming Q1 has $\beta > 100$, which is the case for the specified transistor, the base-emitter voltage on side 1 is to a close approximation:

$$V_{BE\ A} = kT/q \ln I_1/I_{S1}$$

This circuit is arranged to take the difference of the V_{BE}'s of Q1A and Q1B, thus producing an output voltage proportional to the log of the *ratio* of the inputs:

$$V_{OUT} = -K(V_{BE\ A} - V_{BE\ B}) = -\frac{KkT}{q}(\ln I_1/I_{S1} - \ln I_2/I_{S2})$$

$$V_{OUT} = -K\,kT/q \ln I_1/I_2$$

The scaling constant, K is set by R1 and R_{TC} to about 16, to produce a 1V change in output voltage per decade difference in input signals. R_{TC} is a special resistor with a +3500ppm/°C temperature coefficient, which makes K inversely proportional to temperature, compensating for the "T" in kT/q. The log-ratio transfer characteristic is therefore independent of temperature.

This particular log ratio circuit is free from the dynamic problems that plague many other log circuits. The -3dB bandwidth is 50kHz over the top 3 decades, 100nA to 100μA, and decreases smoothly at lower input levels. This circuit needs no additional frequency compensation for stable operation from input current sources, such as photodiodes, which may have 100pF of shunt capacitance. For larger input capacitances a 20pF integration capacitor around each amplifier will provide a smoother frequency response.

This log ratio amplifier can be readily adjusted for optimum accuracy by following this simple procedure. First, apply V1 = V2 = -10.00V and adjust "Balance" for V_{OUT} = 0.00V. Next apply V1 = -10.00V, V2 = -1.00V and adjust gain for V_{OUT} = +1.00V. Repeat this procedure until gain and balance readings are within 2mV of ideal values.

ACTIVE FILTERS

In active low pass filtering applications the dc accuracy of the amplifiers used is critical to the performance of the filter circuits. DC error sources such as offset voltage and bias currents represent the largest individual contributors to output error. Offset voltages will be passed by the filtering network and may, depending on the design of the filter circuit, be amplified and generate unacceptable output offset voltages. In filter circuits for low frequency ranges large value resistors are used to generate the low pass filter function. Input bias currents passing through these resistors will generate an additional offset voltage that will also be passed to the output of the filter.

The use of the AD647 will minimize these error sources and, therefore, maximize filter accuracy. The wide variety of performance levels of the AD647 allows for just the amount of accuracy required for any given application.

AD647 AS AN INSTRUMENTATION AMPLIFIER

The circuit shown in Figure 26 uses the AD647 to construct an ultra high precision instrumentation amplifier. In this type of application the matching characteristics of a monolithic dual amplifier are crucial to ensure high performance.

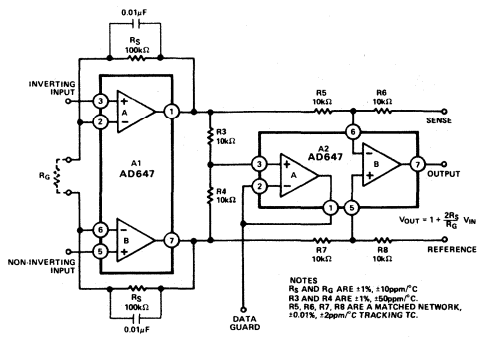


Figure 26. Precision FET Input Instrumentation Amplifier

The use of an AD647L as the input amplifier A1, guarantees maximum offset voltage of 250μV, drift of 2.5μV/°C and bias currents of 35pA. A2 serves two less critical functions in the amplifier and, therefore can be an AD647J. Amplifier A is an active data guard which increases ac CMRR and minimizes extraneous signal pickup and leakage. Amplifier B is the output amplifier of the instrumentation amplifier. To attain the precision available from this configuration, a great deal of care should be taken when selecting the external components. CMRR will depend on the matching of resistors R1, R2, R3, and R4. The gain drift performance of this circuit will be affected by the matching TC of the resistors used.

ANALOG DEVICES

Dual Precision, Low Power BiFET Op Amp

AD648

FEATURES

DC Performance
- 400 μA max Quiescent Current
- 10 pA max Bias Current, Warmed Up (AD648C)
- 300 μV max Offset Voltage (AD648C)
- 3 μV/°C max Drift (AD648C)
- 2 μV p–p Noise, 0.1 Hz to 10 Hz

AC Performance
- 1.8 V/μs Slew Rate
- 1 MHz Unity Gain Bandwidth

Available in Plastic Mini-DIP, Cerdip, Plastic SOIC and Hermetic Metal Can Packages

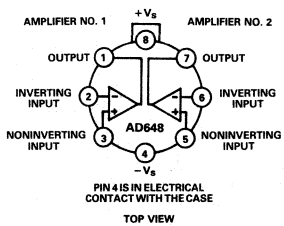
MIL-STD-883B Parts Available

Surface Mount (SOIC) Package Available in Tape and Reel in Accordance with EIA-481A Standard

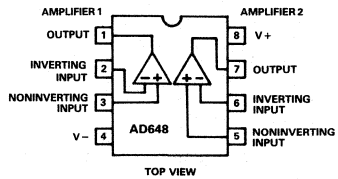
Single Version: AD548

CONNECTION DIAGRAMS

TO-99 (H) Package



Plastic Mini-DIP (N) Package, Plastic SOIC (R) Package and Cerdip (Q) Package



PRODUCT DESCRIPTION

The AD648 is a matched pair of low power, precision monolithic operational amplifiers. It offers both low bias current (10 pA max, warmed up) and low quiescent current (400 μA max) and is fabricated with ion-implanted FET and laser wafer trimming technologies. Input bias current is guaranteed over the AD648's entire common-mode voltage range.

The economical J grade has a maximum guaranteed offset voltage of less than 2 mV and an offset voltage drift of less than 20 μV/°C. The C grade reduces offset voltage to less than 0.30 mV and offset voltage drift to less than 3 μV/°C. This level of dc precision is achieved utilizing Analog's laser wafer drift trimming process. The combination of low quiescent current and low offset voltage drift minimizes changes in input offset voltage due to self-heating effects. Five additional grades are offered over the commercial, industrial and military temperature ranges.

The AD648 is recommended for any dual supply op amp application requiring low power and excellent dc and ac performance. In applications such as battery-powered, precision instrument front ends and CMOS DAC buffers, the AD648's excellent combination of low input offset voltage and drift, low bias current and low 1/f noise reduces output errors. High common-mode rejection (86 dB, min on the "C" grade) and high open-loop gain ensures better than 12-bit linearity in high impedance, buffer applications.

The AD648 is pinned out in a standard dual op amp configuration and is available in seven performance grades. The AD648J and AD648K are rated over the commercial temperature range of 0 to +70°C. The AD648A, AD648B and AD648C are rated over the industrial temperature range of −40°C to +85°C. The AD648S and AD648T are rated over the military temperature range of −55°C to +125°C and are available processed to MIL-STD-883B, Rev. C.

Extended reliability PLUS screening is available for parts specified over the commercial and industrial temperature ranges. PLUS screening includes 168-hour burn-in, as well as other environmental and physical tests.

The AD648 is available in an 8-pin plastic mini-DIP, cerdip, SOIC, TO-99 metal can, or in chip form.

PRODUCT HIGHLIGHTS

1. A combination of low supply current, excellent dc and ac performance and low drift makes the AD648 the ideal op amp for high performance, low power applications.
2. The AD648 is pin compatible with industry standard dual op amps such as the LF442, TL062, and AD642, enabling designers to improve performance while achieving a reduction in power dissipation of up to 85%.
3. Guaranteed low input offset voltage (2 mV max) and drift (20 μV/°C max) for the AD648J are achieved utilizing Analog Devices' laser drift trimming technology.
4. Analog Devices specifies each device in the warmed-up condition, insuring that the device will meet its published specifications in actual use.
5. Matching characteristics are excellent for all grades. The input offset voltage matching between amplifiers in the AD648J is within 2 mV, for the C grade matching is within 0.4 mV.
6. Crosstalk between amplifiers is less than −120 dB at 1 kHz.
7. The AD648 is available in chip form.

AD648—SPECIFICATIONS (@ +25°C and V_S = ±15 V dc, unless otherwise noted)

Model	AD648J/A/S Min	AD648J/A/S Typ	AD648J/A/S Max	AD648K/B/T Min	AD648K/B/T Typ	AD648K/B/T Max	AD648C Min	AD648C Typ	AD648C Max	Units
INPUT OFFSET VOLTAGE[1]										
Initial Offset		0.75	**2.0**		0.3	**1.0**		0.10	**0.3**	mV
T_{min} to T_{max}			3.0/3.0/**3.0**			1.5/1.5/2.0			0.5	mV
vs. Temp.			20			**10**			3.0	µV/°C
vs. Supply	**80**			**86**			86			dB
vs. Supply, T_{min} to T_{max}	76/76/**76**			**80**			**80**			dB
Long-Term Offset Stability		15			15			15		µV/month
INPUT BIAS CURRENT										
Either Input,[2] V_{CM} = 0		5	**20**		3	**10**		3	**10**	pA
Either Input[2] at T_{max}, V_{CM} = 0			0.45/1.3/20			0.25/0.65/10			0.65	nA
Max Input Bias Current Over Common-Mode Voltage Range			**30**			15			15	pA
Offset Current, V_{CM} = 0		5	**10**		2	**5**		2	**5**	pA
Offset Current at T_{max}			0.25/0.7/10			0.15/0.35/5			0.35	nA
MATCHING CHARACTERISTICS[3]										
Input Offset Voltage		1.0	**2.0**		0.5	**1.0**		0.2	**0.4**	mV
Input Offset Voltage T_{min} to T_{max}			3.0/3.0/**3.0**			**1.5/1.5/2.0**			**0.5**	mV
Input Offset Voltage vs. Temp		8			5			2.5		µV/°C
Input Bias Current			**10**			5			**5**	pA
Crosstalk		−120			−120			−120		dB
INPUT IMPEDANCE										
Differential		$1\times10^{12}\|\|3$			$1\times10^{12}\|\|3$			$1\times10^{12}\|\|3$		Ω‖pF
Common Mode		$3\times10^{12}\|\|3$			$3\times10^{12}\|\|3$			$3\times10^{12}\|\|3$		Ω‖pF
INPUT VOLTAGE RANGE										
Differential[4]		±20			±20			±20		V
Common Mode	**±11**	±12		**±11**	±12		**±11**	±12		V
Common-Mode Rejection										
V_{CM} = ±10 V	**76**			**82**			**86**			dB
T_{min} to T_{max}	76/76/**76**			**82**			**86**			dB
V_{CM} = ±11 V	**70**			**76**			**76**			dB
T_{min} to T_{max}	70/70/**70**			**76**			**76**			dB
INPUT VOLTAGE NOISE										
Voltage 0.1 Hz to 10 Hz		2			2			2	**4.0**	µV p–p
f = 10 Hz		80			80			80		nV/√Hz
f = 100 Hz		40			40			40		nV/√Hz
f = 1 kHz		30			30			30		nV/√Hz
f = 10 kHz		30			30			30		nV/√Hz
INPUT CURRENT NOISE										
f = 1 kHz		1.8			1.8			1.8		fA/√Hz
FREQUENCY RESPONSE										
Unity Gain, Small Signal	0.8	1.0		0.8	1.0		0.8	1.0		MHz
Full Power Response		30			30			30		kHz
Slew Rate, Unity Gain	**1.0**	1.8		**1.0**	1.8		**1.0**	1.8		V/µs
Settling Time to ±0.01%		8			8			8		µs
OPEN-LOOP GAIN										
V_O = ±10 V, $R_L \geq$ 10 kΩ	**300**	1000		**300**	1000		**300**	1000		V/mV
T_{min} to T_{max}, $R_L \geq$ 10 kΩ	300/300/**300**	700		**300**	700		**300**	700		V/mV
V_O = ±10 V, $R_L \geq$ 5 kΩ	**150**	500		**150**	500		**150**	500		V/mV
T_{min} to T_{max}, $R_L \geq$ 5 kΩ	150/150/**150**	300		**150**	300		**150**	300		V/mV
OUTPUT CHARACTERISTICS										
Voltage @ $R_L \geq$ 10 kΩ, T_{min} to T_{max}	±12/±12/**±12**	±13		**±12**	±13		**±12**	±13		V
Voltage @ $R_L \geq$ 5 kΩ, T_{min} to T_{max}	±11/±11/**±11**	±12		**±11**	±12		**±11**	±12		V
Short Circuit Current		15			15			15		mA
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating Range	±4.5		**±18**	±4.5		**±18**	±4.5		**±18**	V
Quiescent Current (Both Amplifiers)		340	**400**		340	**400**		340	**400**	µA
TEMPERATURE RANGE										
Operating, Rated Performance										
Commercial (0 to +70°C)		AD648J			AD648K					
Industrial (−40°C to +85°C)		AD648A			AD648B			AD648C		
Military (−55°C to +125°C)		AD648S			AD648T					
PACKAGE OPTIONS										
SOIC (R-8)		AD648JR			AD648KR					
Plastic (N-8)		AD648JN			AD648KN					
Cerdip (Q-8)		AD648AQ, AD648SQ			AD648BQ, AD648TQ			AD648CQ		
Metal Can (H-08A)		AD648AH, AD648SH			AD648BH, AD648TH			AD648CH		
Tape and Reel		AD648JR-REEL			AD648KR-REEL					
Chips Available		AD648JChips, AD648SChips								

NOTES
[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[2]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperature, the current doubles every 10°C.
[3]Matching is defined as the difference between parameters of the two amplifiers.
[4]Defined as voltages between inputs, such that neither exceeds ±10 V from ground.

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed.

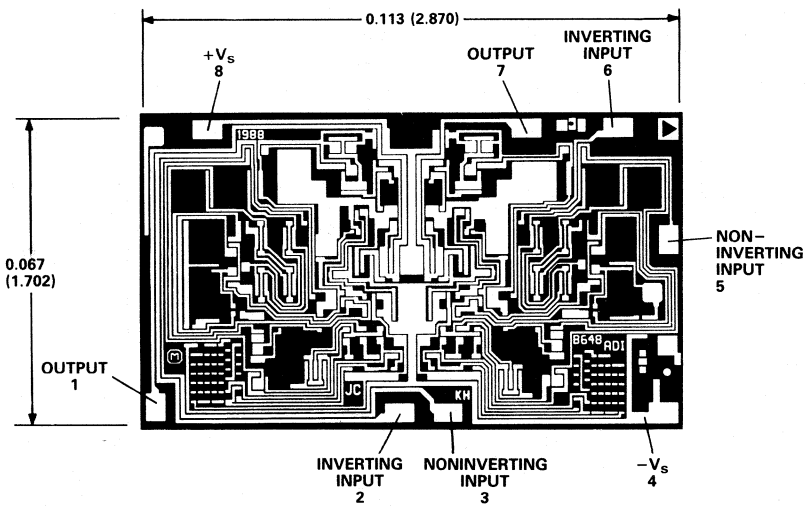
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2] . . . . . 500 mW
Input Voltage[3] . . . . . ±18 V
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range (Q, H) . . . . . −65°C to +150°C
(N, R) . . . . . −65°C to +125°C
Operating Temperature Range
AD648J/K . . . . . 0 to +70°C
AD648A/B/C . . . . . −40°C to +85°C
AD648S/T . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . 300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Thermal Characteristics
8-Pin Plastic DIP Package: θ_{JA} = 165°C/Watt
8-Pin Cerdip Package: θ_{JC} = 22°C/Watt; θ_{JA} = 110°C/Watt
8-Pin Metal Can Package: θ_{JC} = 65°C/Watt; θ_{JA} = 150°C/Watt
8-Pin SOIC Package: θ_{JC} = 42°C/Watt; θ_{JA} = 160°C/Watt
[3]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



AD648—Typical Characteristics

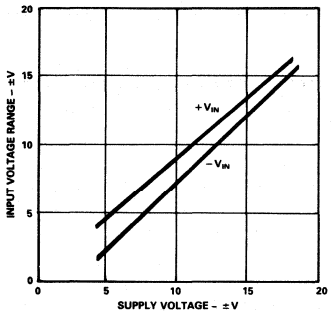


Figure 1. Input Voltage Range vs. Supply Voltage

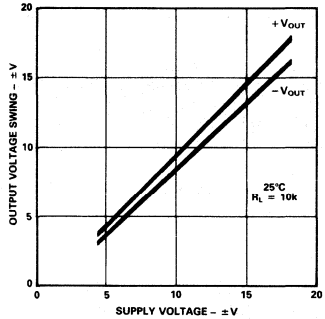


Figure 2. Output Voltage Swing vs. Supply Voltage

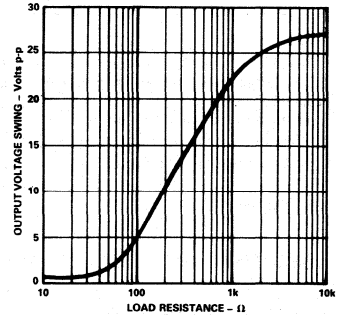


Figure 3. Output Voltage Swing vs. Load Resistance

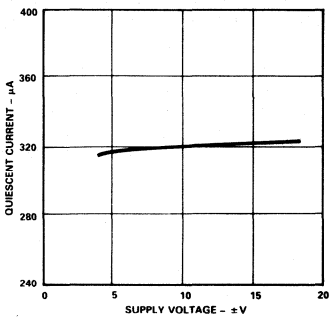


Figure 4. Quiescent Current vs. Supply Voltage

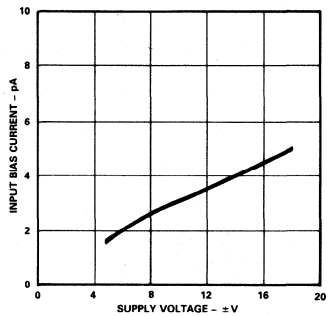


Figure 5. Input Bias Current vs. Supply Voltage

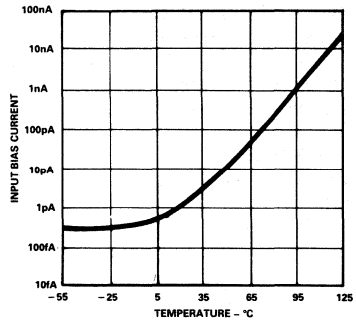


Figure 6. Input Bias Current vs. Temperature

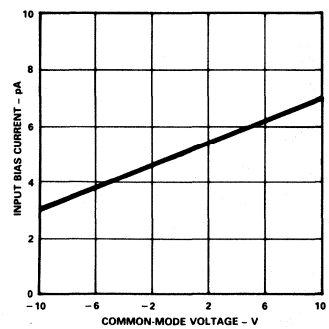


Figure 7. Input Bias Current vs. Common-Mode Voltage

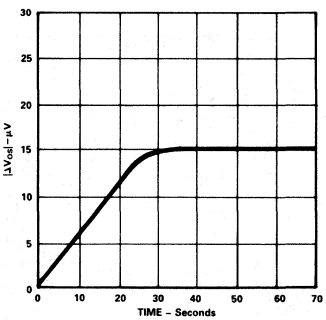


Figure 8. Change in Offset Voltage vs. Warm-Up Time

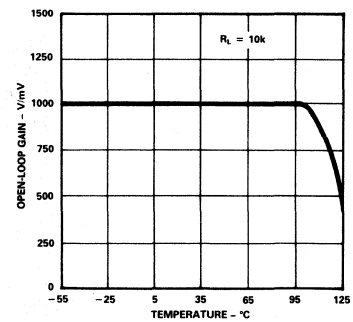


Figure 9. Open-Loop Gain vs. Temperature

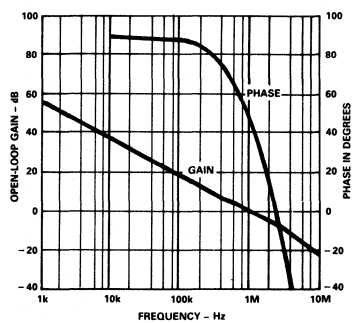


Figure 10. Open-Loop Frequency Response

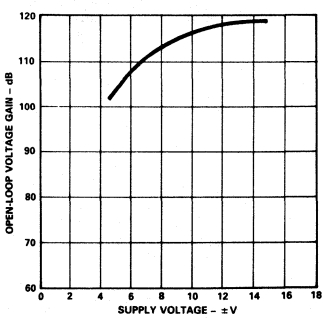


Figure 11. Open-Loop Voltage Gain vs. Supply Voltage

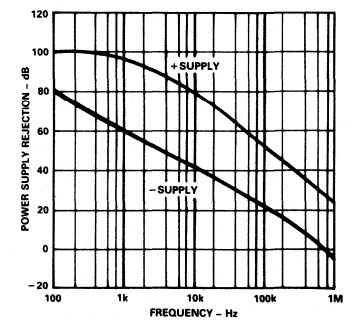


Figure 12. PSRR vs. Frequency

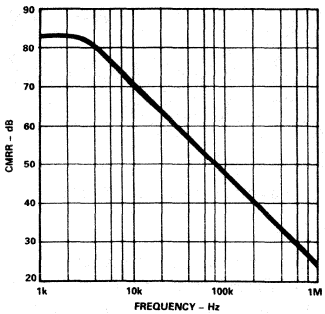


Figure 13. CMRR vs. Frequency

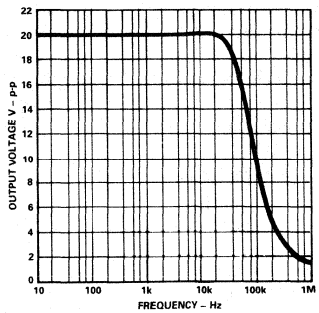


Figure 14. Large Signal Frequency Response

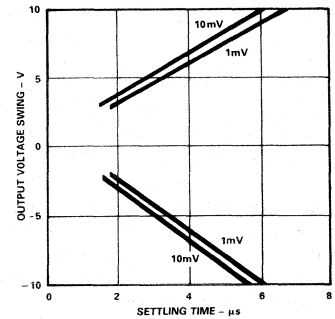


Figure 15. Output Swing and Error Voltage vs. Output Settling Time

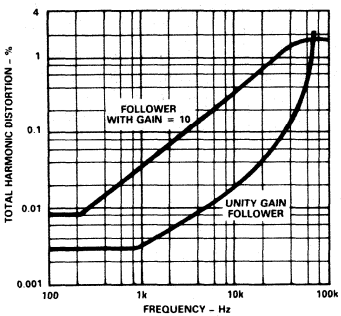


Figure 16. Total Harmonic Distortion vs. Frequency

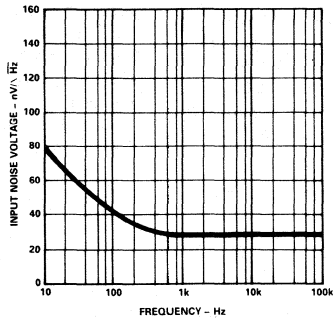


Figure 17. Input Noise Voltage Spectral Density

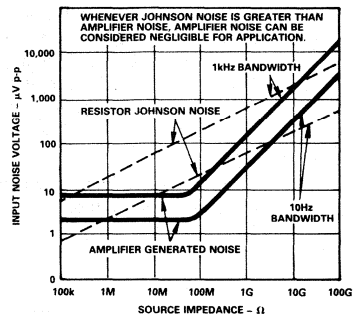


Figure 18. Total Noise vs. Source Impedance

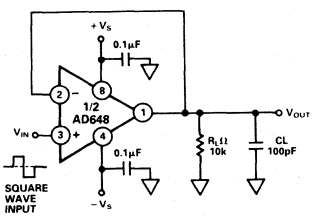


Figure 19a. Unity Gain Follower

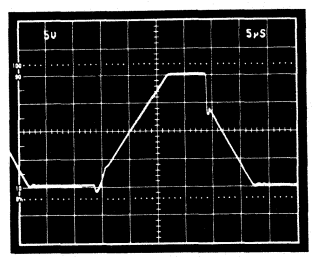


Figure 19b. Unity Gain Follower Pulse Response (Large Signal)

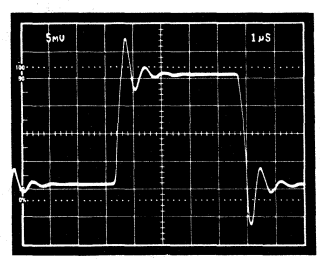


Figure 19c. Unity Gain Follower Pulse Response (Small Signal)

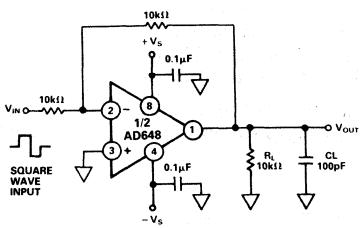


Figure 20a. Unity Gain Inverter

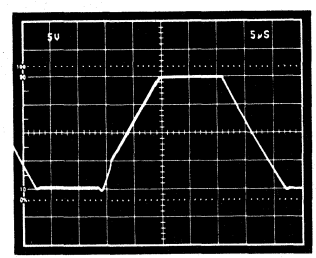


Figure 20b. Unity Gain Inverter Pulse Response (Large Signal)

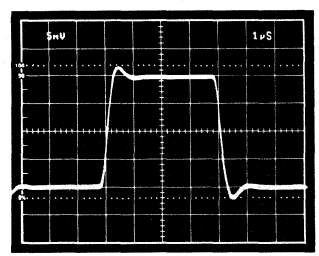


Figure 20c. Unity Gain Inverter Pulse Response (Small Signal)

APPLICATION NOTES

The AD648 is a pair of JFET-input op amps with a guaranteed maximum I_B of less than 10 pA, and offset and drift laser-trimmed to 0.3 mV and 3 μV/°C, respectively (AD648C). AC specs include 1 MHz bandwidth, 1.8 V/μs typical slew rate and 8 μs settling time for a 20 V step to ±0.01%—all at a supply current less than 400 μA. To capitalize on the device's performance, a number of error sources should be considered.

The minimal power drain and low offset drift of the AD648 reduce self-heating or "warm-up" effects on input offset voltage, making the AD648 ideal for on/off battery powered applications. The power dissipation due to the AD648's 400 μA supply current has a negligible effect on input current, but heavy output loading will raise the chip temperature. Since a JFET's input current doubles for every 10°C rise in chip temperature, this can be a noticeable effect.

The amplifier is designed to be functional with power supply voltages as low as ±4.5 V. It will exhibit a higher input offset voltage than at the rated supply voltage of ±15 V, due to power supply rejection effects. Common-mode range extends from 3 V more positive than the negative supply to 1 V more negative than the positive supply. Designed to cleanly drive up to 10 kΩ and 100 pF loads, the AD648 will drive a 2 kΩ load with reduced open-loop gain.

Figure 21 shows the recommended crosstalk test circuit. A typical value for crosstalk is −120 dB at 1 kHz.

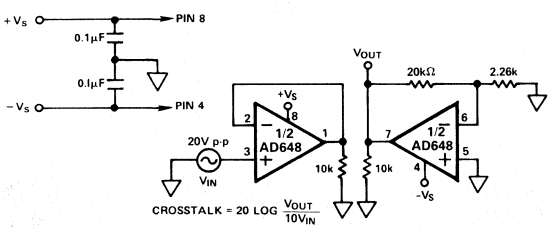


Figure 21. Crosstalk Test Circuit

LAYOUT

To take full advantage of the AD648's 10 pA max input current, parasitic leakages must be kept below an acceptable level. The practical limit of the resistance of epoxy or phenolic circuit board material is between 1×10^{12} Ω and 3×10^{12} Ω. This can result in an additional leakage of 5 pA between an input of 0 V and a −15 V supply line. Teflon or a similar low leakage material (with a resistance exceeding 10^{17} Ω) should be used to isolate high impedance input lines from adjacent lines carrying high voltages. The insulator should be kept clean, since contaminants will degrade the surface resistance.

A metal guard completely surrounding the high impedance nodes and driven by a voltage near the common-mode input potential can also be used to reduce some parasitic leakages. The guarding pattern in Figure 22 will reduce parasitic leakage due to finite board surface resistance; but it will not compensate for a low volume resistivity board.

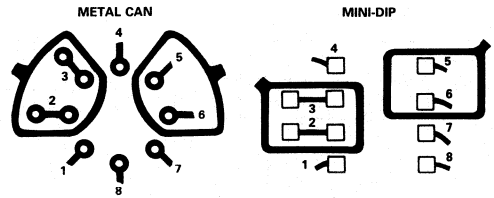


Figure 22. Board Layout for Guarding Inputs

INPUT PROTECTION

The AD648 is guaranteed to withstand input voltages equal to the power supply potential. Exceeding the negative supply voltage on either input will forward bias the substrate junction of the chip. The induced current may destroy the amplifier due to excess heat.

Input protection is required in applications such as a flame detector in a gas chromatograph, where a very high potential may be applied to the input terminals during a sensor fault condition. Figures 23a and 23b show simple current limiting schemes that can be used. $R_{PROTECT}$ should be chosen such that the maximum overload current is 1.0 mA (for example 100 kΩ for a 100 V overload).

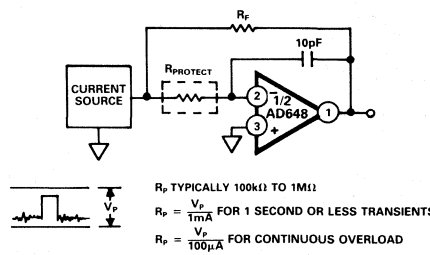


Figure 23a. Input Protection of I-to-V Converter

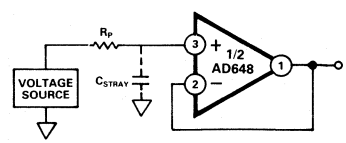


Figure 23b. Voltage Follower Input Protection Method

Figure 23b shows the recommended method for protecting a voltage follower from excessive currents due to high voltage breakdown. The protection resistor, R_p, limits the input current. A nominal value of 100 kΩ will limit the input current to less than 1 mA with a 100 volt input voltage applied.

The stray capacitance between the summing junction and ground will produce a high frequency roll-off with a corner frequency equal to:

$$f_{corner} = \frac{1}{2\pi R_p C_{stray}}$$

Accordingly, a 100 kΩ value for R_p with a 3 pF C_{stray} will cause a 3 dB corner frequency to occur at 531 kHz.

Figure 23c shows a diode clamp protection scheme for an I-to-V converter using low leakage diodes. Because the diodes are connected to the op amp's summing junction, which is a virtual ground, their leakage contribution is minimal.

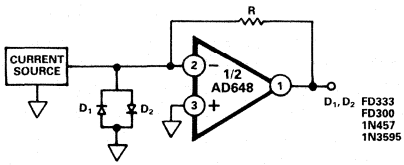


Figure 23c. I-to-V Converter with Diode Input Protection

Exceeding the negative common-mode range on either input terminal causes a phase reversal at the output, forcing the amplifier output to the corresponding high or low state. Exceeding the negative common-mode on both inputs simultaneously forces the output high. Exceeding the positive common-mode range on a single input doesn't cause a phase reversal; but if both inputs exceed the limit, the output will be forced high. In all cases, normal amplifier operation is resumed when input voltages are brought back within the common-mode range.

D/A CONVERTER BIPOLAR OUTPUT BUFFER

The circuit in Figure 24 provides 4 quadrant multiplication with a resolution of 12 bits. The AD648 is used to convert the AD7545 CMOS DAC's output current to a voltage and provides the necessary level shifting to achieve a bipolar voltage output. The circuit operates with a 12-bit plus sign input code. The transfer function is shown in Figure 25.

The AD7592 is a fully protected dual CMOS SPDT switch with data latches. R4 and R5 should match to within 0.01% to maintain the accuracy of the converter. A mismatch between R4 and R5 introduces a gain error. Overall gain is trimmed by adjusting R_{IN}. The AD648's low input offset voltage, low drift over temperature, and excellent dynamics make it an attractive low power output buffer.

The input offset voltage of the AD648 output amplifier results in an output error voltage. This error voltage equals the input offset voltage of the op amp times the noise gain of the amplifier.

That is:

$$V_{OS}\ Output = V_{OS}\ Input \left(1 + \frac{R_{FB}}{R_O}\right)$$

R_{FB} is the feedback resistor for the op amp, which is internal to the DAC. R_O is the DAC's R-2R ladder output resistance. The value of R_O is code dependent. This has the effect of changing the offset error voltage at the amplifier's output. An output amplifier with a sub millivolt input offset voltage is needed to preserve the linearity of the DAC's transfer function.

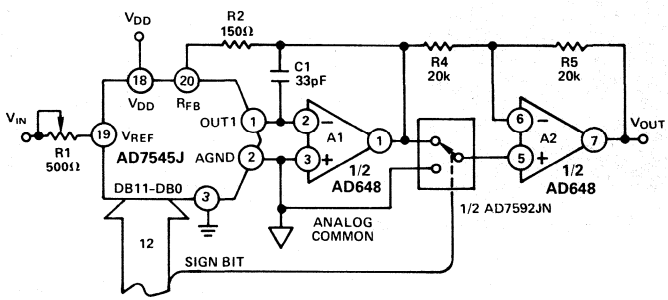


Figure 24. 12-Bit Plus Sign Magnitude D/A Converter

SIGN BIT	BINARY NUMBER IN DAC REGISTER	ANALOG OUTPUT
0	1111 1111 1111	$+V_{IN} \times (4095/4096)$
0	0000 0000 0000	0 VOLTS
1	0000 0000 0000	0 VOLTS
1	1111 1111 1111	$-V_{IN} \times (4095/4096)$

NOTE: SIGN BIT AT "0" CONNECTS THE NONINVERTING INPUT OF A2 TO ANALOG COMMON

Figure 25. Sign Magnitude Code Table

The AD648 in this configuration provides a 700 kHz small signal bandwidth and 1.8 V/μs typical slew rate. The 33 pF capacitor across the feedback resistor optimizes the circuit's response. The oscilloscope photos in Figures 26a and 26b show small and large signal outputs of the circuit in Figure 24. Upper traces show the input signal V_{IN}. Lower traces are the resulting output voltage with the DAC's digital input set to all 1s. The circuit settles to ±0.01% for a 20 V input step in 14 μs.

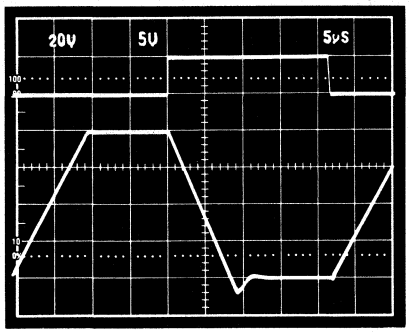


Figure 26a. Response to ±20 V p–p Reference Square Wave

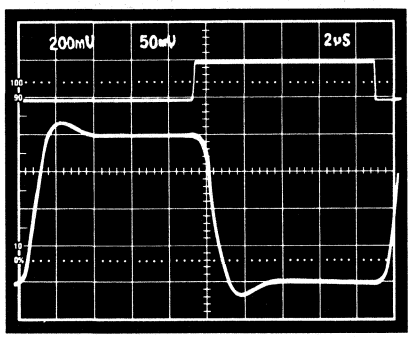


Figure 26b. Response to ±100 mV p–p Reference Square Wave

DUAL PHOTODIODE PREAMP

The performance of the dual photodiode preamp shown in Figure 27 is enhanced by the AD648's low input current, input voltage offset, and offset voltage drift. Each photodiode sources a current proportional to the incident light power on its surface. R_F converts the photodiode current to an output voltage equal to $R_F \times I_S$.

An error budget illustrating the importance of low amplifier input current, voltage offset, and offset voltage drift to minimize output voltage errors can be developed by considering the equivalent circuit for the small (0.2 mm^2 area) photodiode shown in Figure 27. The input current results in an error proportional to the feedback resistance used. The amplifier's offset will produce an error proportional to the preamp's noise gain $(1+R_F/R_{SH})$, where R_{SH} is the photodiode shunt resistance. The amplifier's input current will double with every 10°C rise in temperature, and the photodiode's shunt resistance halves with every 10°C rise. The error budget in Figure 28 assumes a room temperature photodiode R_{SH} of 500 MΩ, and the maximum input current and input offset voltage specs of an AD648C.

The capacitance at the amplifier's negative input (the sum of the photodiode's shunt capacitance, the op amp's differential input capacitance, stray capacitance due to wiring, etc.) will cause a rise in the preamp's noise gain over frequency. This can result in excess noise over the bandwidth of interest. C_F reduces the noise gain "peaking" at the expense of signal bandwidth.

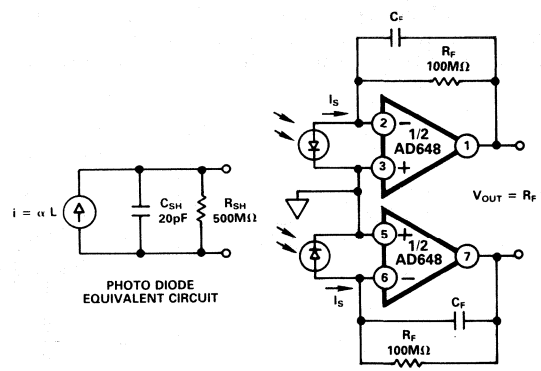


Figure 27. A Dual Photodiode Pre-Amp

TEMP °C	R_{SH} (MΩ)	V_{OS} (μV)	$(1 + R_F/R_{SH})\ V_{OS}$	I_B (pA)	$I_B R_F$	TOTAL
−25	15,970	150	151 μV	0.30	30 μV	181 μV
0	2,830	225	233 μV	2.26	262 μV	495 μV
+25	500	300	360 μV	10.00	1.0 mV	1.36 mV
+50	88.5	375	800 μV	56.6	5.6 mV	6.40 mV
+75	15.6	450	3.33 mV	320	32 mV	35.3 mV
+85	7.8	480	6.63 mV	640	64 mV	70.6 mV

Figure 28. Photodiode Pre-Amp Errors over Temperature

INSTRUMENTATION AMPLIFIER

The AD648J's maximum input current of 20 pA per amplifier makes it an excellent building block for the high input impedance instrumentation amplifier shown in Figure 29. Total current drain for this circuit is under 600 μA. This configuration is optimal for conditioning differential voltages from high impedance sources.

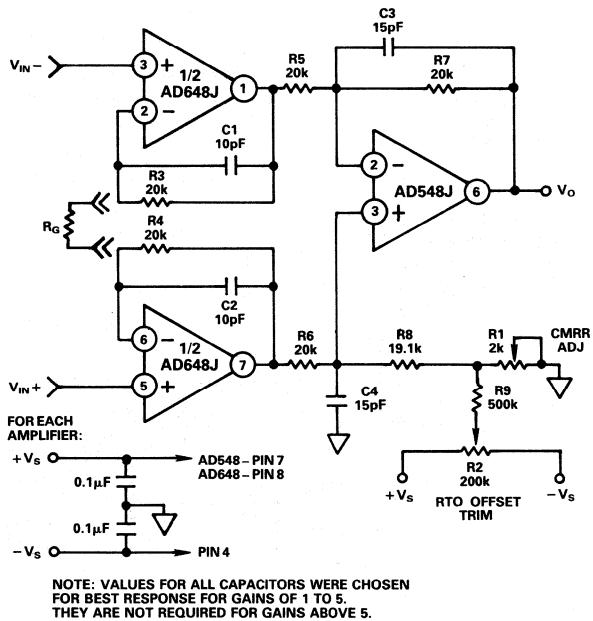
The overall gain of the circuit is controlled by R_G, resulting in the following transfer function:

$$\frac{V_{OUT}}{V_{IN}} = 1 + \frac{(R_3 + R_4)}{R_G}$$

Gains of 1 to 100 can be accommodated with gain nonlinearities of less than 0.01%. The maximum input current is 30 pA over the common-mode range, with a common-mode impedance of over $1 \times 10^{12}\Omega$. The capacitors C1, C2, C3 and C4 compensate for peaking in the gain over frequency which is caused by input capacitance.

To calibrate this circuit, first adjust trimmer R1 for common-mode rejection with +10 volts dc applied to the input pins. Next, adjust R2 for zero offset at V_{OUT} with both inputs grounded. Trim the circuit a second time for optimal performance.

The −3 dB small signal bandwidth for this low power instrumentation amplifier is 700 kHz for a gain of 1 and 10 kHz for a gain of 100. The typical output slew rate is 1.8 V/μs.



NOTE: VALUES FOR ALL CAPACITORS WERE CHOSEN FOR BEST RESPONSE FOR GAINS OF 1 TO 5. THEY ARE NOT REQUIRED FOR GAINS ABOVE 5.

Figure 29. Low Power Instrumentation Amplifier

LOG RATIO AMPLIFIER

Log ratio amplifiers are useful for a variety of signal conditioning applications, such as linearizing exponential transducer outputs and compressing analog signals having a wide dynamic range. The AD648's picoamp level input current and low input offset voltage make it a good choice for the front-end amplifier of the log ratio circuit shown in Figure 30. This circuit produces an output voltage equal to the log base 10 of the ratio of the input currents I_1 and I_2. Resistive inputs R1 and R2 are provided for voltage inputs.

Input currents I_1 and I_2 set the collector currents of Q1 and Q2, a matched pair of logging transistors. Voltages at points A and B are developed according to the following familiar diode equation:

$$V_{BE} = (kT/q)\ 1n\ (I_C/I_{ES})$$

In this equation, k is Boltzmann's constant, T is absolute temperature, q is an electron charge, and I_{ES} is the reverse saturation current of the logging transistors. The difference of these two voltages is taken by the subtractor section and scaled by a factor of approximately 16 by resistors R9, R10 and R8. Temperature compensation is provided by resistors R8 and R15, which have a positive 3500 ppm/°C temperature coefficient. The transfer function for the output voltage is:

$$V_{OUT} = 1Vlog_{10}\ (I_2/I_1)$$

Frequency compensation is provided by R11, R12, C1, and C2. Small signal bandwidth is approximately 300 kHz at input currents above 100 μA and will proportionally decrease with lower signal levels. D1, D2, R13, and R14 compensate for the effects of the two logging transistors' ohmic emitter resistance.

To trim this circuit, set the two input currents to 10 μA and adjust V_{OUT} to zero by adjusting the potentiometer on A3. Then set I_2 to 1 μA and adjust the scale factor such that the output voltage is 1 V by trimming potentiometer R10. Offset adjustment for A1 and A2 is provided to increase the accuracy of the voltage inputs.

This circuit ensures a 1% log conformance error over an input current range of 300 pA to 1 mA, with low level accuracy limited by the AD648's input current. The low level input voltage accuracy of this circuit is limited by the input offset voltage and drift of the AD648.

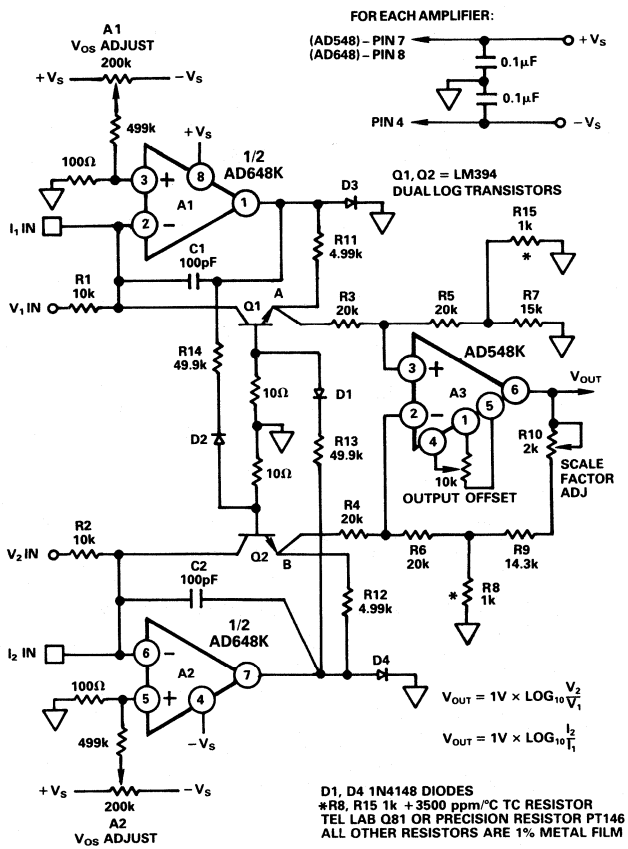


Figure 30. Precision Log Ratio Amplifier

Quad Picoampere Input Current Bipolar Op Amp

AD704

FEATURES

HIGH DC PRECISION
- 75 μV max Offset Voltage
- 1 μV/°C max Offset Voltage Drift
- 150 pA max Input Bias Current
- 0.2 pA/°C typical I_B Drift

LOW NOISE
- 0.5 μV p–p typical Noise, 0.1 Hz to 10 Hz

LOW POWER
- 600 μA max Supply Current per Amplifier

Chips & MIL-STD-883B Processing Available
Available in Tape and Reel in Accordance with EIA-481A Standard
Single Version: AD705, Dual Version: AD706

PRIMARY APPLICATIONS
Industrial/Process Controls
Weigh Scales
ECG/EKG Instrumentation
Low Frequency Active Filters

PRODUCT DESCRIPTION

The AD704 is a quad, low power bipolar op amp that has the low input bias current of a BiFET amplifier but which offers a significantly lower I_B drift over temperature. It utilizes Super-beta bipolar input transistors to achieve picoampere input bias current levels (similar to FET input amplifiers at room temperature), while its I_B typically only increases by 5× at +125°C (unlike a BiFET amp, for which I_B doubles every 10°C resulting in a 1000× increase at +125°C). Furthermore the AD704 achieves 75 μV offset voltage and low noise characteristics of a precision bipolar input op amp.

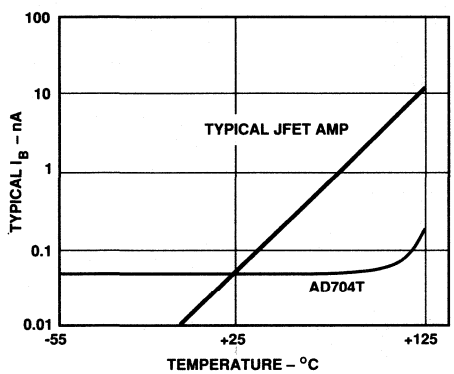
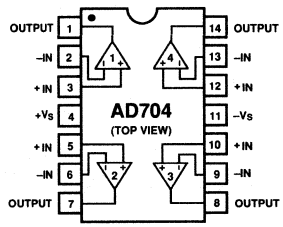


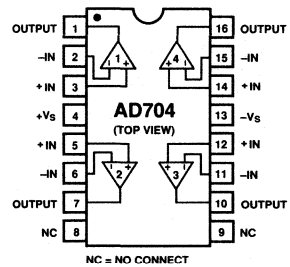
Figure 1. Input Bias Current Over Temperature

CONNECTION DIAGRAMS

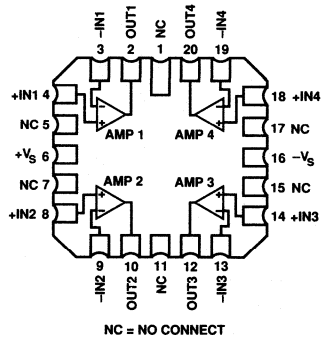
14-Pin Plastic DIP (N)
14-Pin Cerdip (Q) Packages



16-Pin SOIC
(R) Package



20-Terminal LCC
(E) Package



Since it has only 1/20 the input bias current of an AD OP-07, the AD704 does not require the commonly used "balancing" resistor. Furthermore, the current noise is 1/5 that of the AD OP-07 which makes the AD704 usable with much higher source impedances. At 1/6 the supply current (per amplifier) of the AD OP-07, the AD704 is better suited for today's higher density circuit boards and battery powered applications.

The AD704 is an excellent choice for use in low frequency active filters in 12- and 14-bit data acquisition systems, in precision instrumentation, and as a high quality integrator. The AD704 is internally compensated for unity gain and is available in five performance grades. The AD704J and AD704K are rated over the commercial temperature range of 0°C to +70°C. The AD704A and AD704B are rated over the industrial temperature of −40°C to +85°C. The AD704T is rated over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

AD704—SPECIFICATIONS (@ T_A = +25°C, V_{CM} = 0 V, and ±15 V dc, unless otherwise noted)

Model	Conditions	AD704J/A Min	AD704J/A Typ	AD704J/A Max	AD704K/B Min	AD704K/B Typ	AD704K/B Max	AD704T Min	AD704T Typ	AD704T Max	Units
INPUT OFFSET VOLTAGE											
Initial Offset			50	150		30	75		30	100	μV
Offset	T_{min}–T_{max}		100	250		50	150		80	150	μV
vs. Temp, Average TC			0.2	1.5		0.2	1.0			1.0	μV/°C
vs. Supply (PSRR)	V_S = ±2 to ±18 V	100	132		112	132		112	132		dB
T_{min}–T_{max}	V_S = +2.5 to ±18 V	100	126		108	126		108	126		dB
Long Term Stability			0.3			0.3			0.3		μV/month
INPUT BIAS CURRENT[1]	V_{CM} = 0 V		100	270		80	150		80	200	pA
	V_{CM} = ±13.5 V			300			200			250	pA
vs. Temp, Average TC			0.3			0.2			1.0		pA/°C
T_{min}–T_{max}	V_{CM} = 0 V			300			200			600	pA
T_{min}–T_{max}	V_{CM} = ±13.5 V			400			300			700	pA
INPUT OFFSET CURRENT	V_{CM} = 0 V		80	250		30	100		50	150	pA
	V_{CM} = ±13.5 V			300			150			200	pA
vs. Temp, Average TC			0.6			0.4			0.4		pA/°C
T_{min}–T_{max}	V_{CM} = 0 V		100	300		80	200		80	400	pA
T_{min}–T_{max}	V_{CM} = ±13.5 V		100	400		80	300		100	500	pA
MATCHING CHARACTERISTICS											
Offset Voltage				250			130			150	μV
	T_{min}–T_{max}			400			200			250	μV
Input Bias Current[2]				500			300			400	pA
	T_{min}–T_{max}			600			400			600	pA
Common-Mode Rejection[3]		94			110			104			dB
	T_{min}–T_{max}	94			104			104			dB
Power Supply Rejection[4]		94			110			110			dB
	T_{min}–T_{max}	94			106			106			dB
Crosstalk[5]	f = 10 Hz										
	R_{LOAD} = 2 kΩ		150			150			150		dB
FREQUENCY RESPONSE											
UNITY GAIN											
Crossover Frequency			0.8			0.8			0.8		MHz
Slew Rate, Unity Gain	G = −1		0.15			0.15			0.15		V/μs
Slew Rate	T_{min}–T_{max}		0.1			0.1			0.1		V/μs
INPUT IMPEDANCE											
Differential			40||2			40||2			40||2		MΩ||pF
Common-Mode			300||2			300||2			300||2		GΩ||pF
INPUT VOLTAGE RANGE											
Common-Mode Voltage		±13.5	±14		±13.5	±14		±13.5	±14		V
Common-Mode Rejection Ratio	V_{CM} = ±13.5 V	100	132		114	132		110	132		dB
	T_{min}–T_{max}	98	128		108	128		108	128		dB
INPUT CURRENT NOISE	0.1 to 10 Hz		3			3			3		pA p–p
	f = 10 Hz		50			50			50		fA/$\sqrt{Hz}$
INPUT VOLTAGE NOISE	0.1 to 10 Hz		0.5			0.5	2.0		0.5	2.0	μV p–p
	f = 10 Hz		17			17			17		nV/$\sqrt{Hz}$
	f = 1 kHz		15	22		15	22		15	22	nV/$\sqrt{Hz}$
OPEN-LOOP GAIN	V_O = ±12 V										
	R_{LOAD} = 10 kΩ	200	2000		400	2000		400	2000		V/mV
	T_{min}–T_{max}	150	1500		300	1500		300	1500		V/mV
	V_O = ±10 V										
	R_{LOAD} = 2 kΩ	200	1000		300	1000		200	1000		V/mV
	T_{min}–T_{max}	150	1000		200	1000		100	1000		V/mV

Model	Conditions	AD704J/A Min	AD704J/A Typ	AD704J/A Max	AD704K/B Min	AD704K/B Typ	AD704K/B Max	AD704T Min	AD704T Typ	AD704T Max	Units
OUTPUT CHARACTERISTICS											
Voltage Swing	R_{LOAD} = 10 kΩ										
	T_{min}–T_{max}	±13	±14		±13	±14		±13	±14		V
Current	Short Circuit		±15			±15			±15		mA
CAPACITIVE LOAD											
Drive Capability	Gain = +1		10,000			10,000			10,000		pF
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		±2.0		±18	±2.0		±18	±2.0		±18	V
Quiescent Current			1.5	2.4		1.5	2.4		1.5	2.4	mA
	T_{min}–T_{max}		1.6	2.6		1.6	2.6		1.6	2.6	mA
TRANSISTOR COUNT	# of Transistors		180			180			180		

NOTES
[1]Bias current specifications are guaranteed maximum at either input.
[2]Input bias current match is the maximum difference between corresponding inputs of all four amplifiers.
[3]CMRR match is the difference of $\Delta V_{OS}/\Delta V_{CM}$ between any two amplifiers, expressed in dB.
[4]PSRR match is the difference between $\Delta V_{OS}/\Delta V_{SUPPLY}$ for any two amplifiers, expressed in dB.
[5]See Figure 2a for test circuit.

All min and max specifications are guaranteed.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation (+25°C) . . . . . .See Note 2
Input Voltage . . . . . $\pm V_S$
Differential Input Voltage[3] . . . . . ±0.7 V
Output Short Circuit Duration (Single Input) . . . . . Indefinite
Storage Temperature Range
(Q) . . . . . −65°C to +150°C
(N, R) . . . . . −65°C to +125°C
Operating Temperature Range
AD704J/K . . . . . 0°C to +70°C
AD704A/B . . . . . −40°C to +85°C
AD704T . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 10 seconds) . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air:
14-Pin Plastic Package: θ_{JA} = 150°C/Watt
14-Pin Cerdip Package: θ_{JA} = 110°C/Watt
16-Pin SOIC Package: θ_{JA} = 100°C/Watt
20-Terminal LCC Package: θ_{JA} = 150°C/Watt
[3]The input pins of this amplifier are protected by back-to-back diodes. If the differential voltage exceeds ±0.7 volts, external series protection resistors should be added to limit the input current to less than 25 mA.

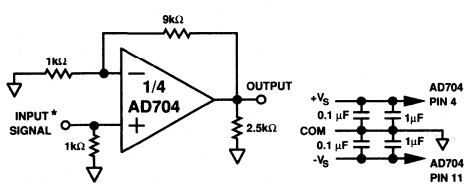
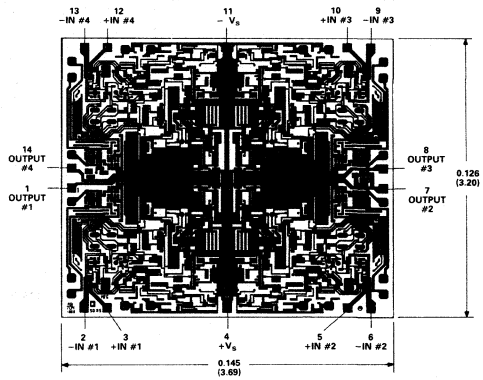


Figure 2a. Crosstalk Test Circuit

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



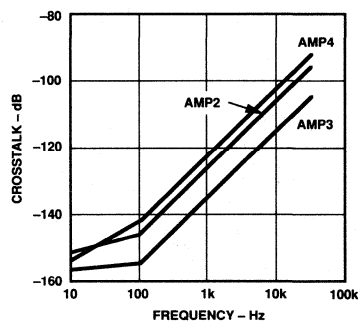


Figure 2b. Crosstalk vs. Frequency

AD704—Typical Characteristics (@ +25°C, V_S = ±15 V, unless otherwise noted)

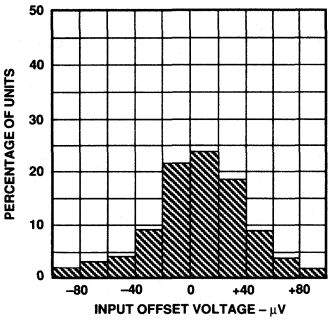


Figure 3. Typical Distribution of Input Offset Voltage

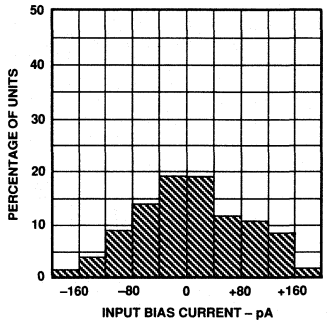


Figure 4. Typical Distribution of Input Bias Current

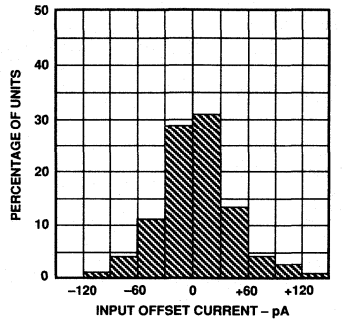


Figure 5. Typical Distribution of Input Offset Current

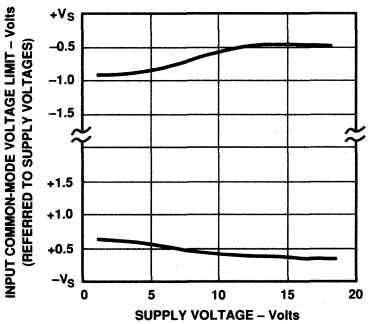


Figure 6. Input Common-Mode Voltage Range vs. Supply Voltage

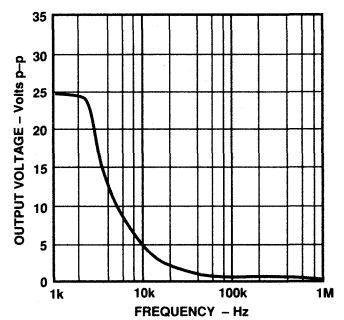


Figure 7. Large Signal Frequency Response

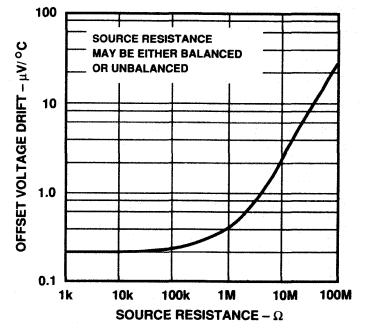


Figure 8. Offset Voltage Drift vs. Source Resistance

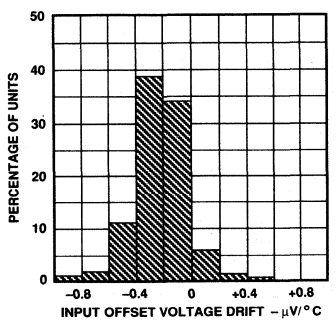


Figure 9. Typical Distribution of Offset Voltage Drift

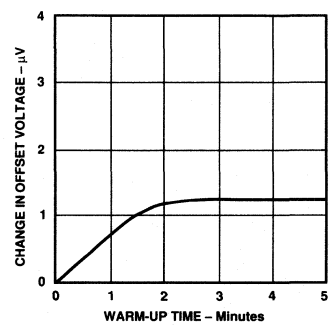


Figure 10. Change in Input Offset Voltage vs. Warm-Up Time

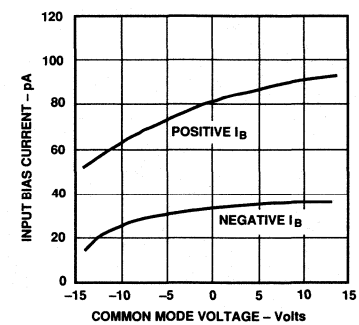


Figure 11. Input Bias Current vs. Common-Mode Voltage

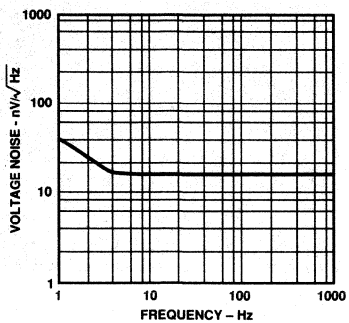


Figure 12. Input Noise Voltage Spectral Density

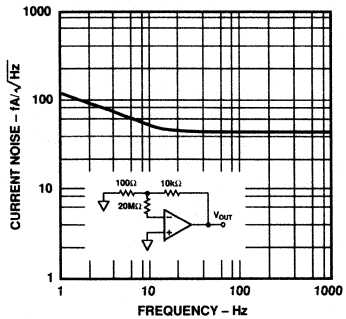


Figure 13. Input Noise Current Spectral Density

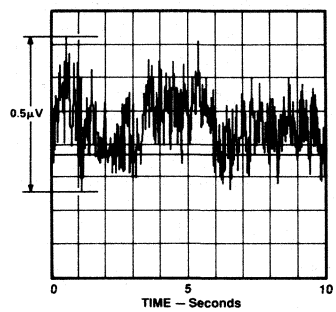


Figure 14. 0.1 Hz to 10 Hz Noise Voltage

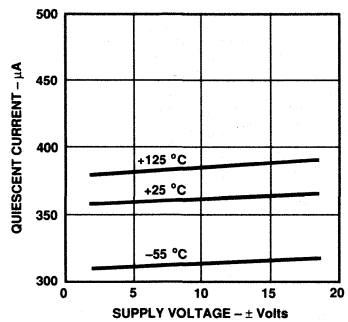


Figure 15. Quiescent Supply Current vs. Supply Voltage (per Amplifier)

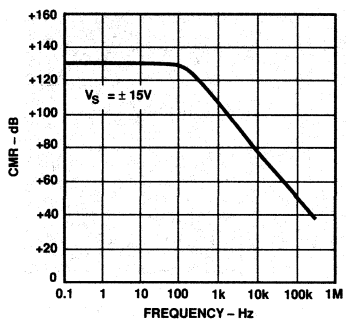


Figure 16. Common-Mode Rejection vs. Frequency

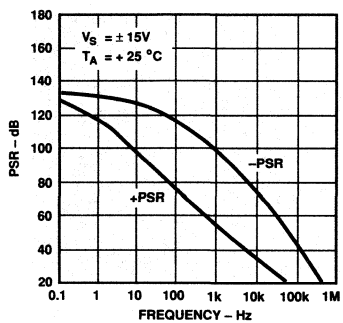


Figure 17. Power Supply Rejection vs. Frequency

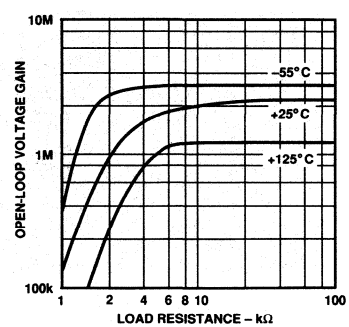


Figure 18. Open-Loop Gain vs. Load Resistance Over Temperature

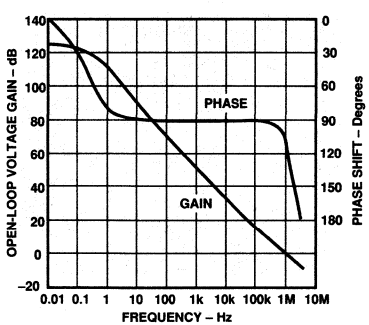


Figure 19. Open-Loop Gain and Phase vs. Frequency

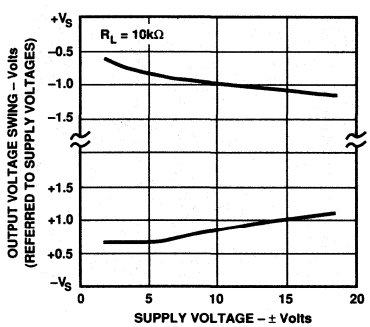


Figure 20. Output Voltage Swing vs. Supply Voltage

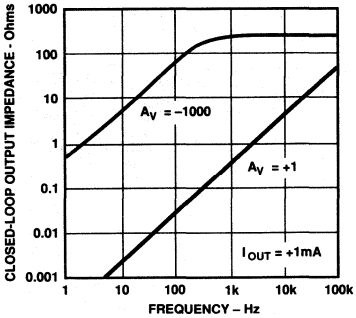


Figure 21. Closed-Loop Output Impedance vs. Frequency

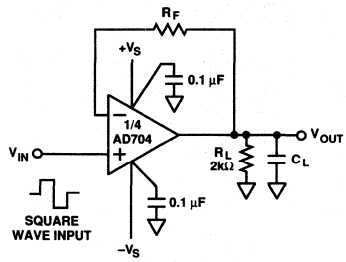


Figure 22a. Unity Gain Follower (For Large Signal Applications, Resistor R_F Limits the Current Through the Input Protection Diodes)

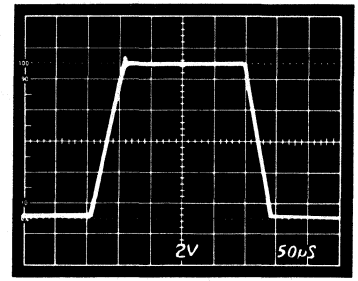


Figure 22b. Unity Gain Follower Large Signal Pulse Response R_F = 10 kΩ, C_L = 1,000 pF

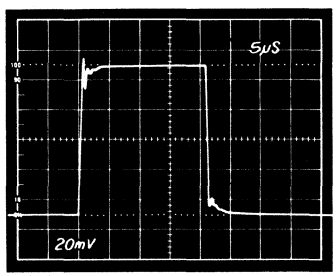


Figure 22c. Unity Gain Follower Small Signal Pulse Response R_F = 0 Ω, C_L = 100 pF

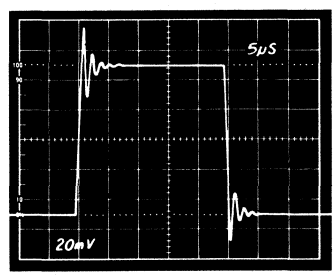


Figure 22d. Unity Gain Follower Small Signal Pulse Response R_F = 0 Ω, C_L = 1,000 pF

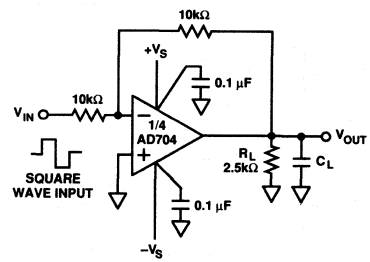


Figure 23a. Unity Gain Inverter Connection

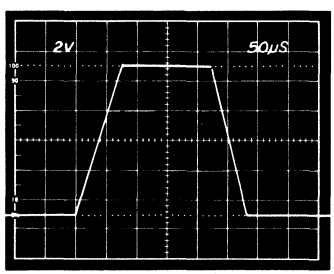


Figure 23b. Unity Gain Inverter Large Signal Pulse Response C_L = 1,000 pF

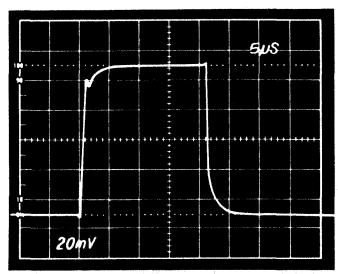


Figure 23c. Unity Gain Inverter Small Signal Pulse Response C_L = 100 pF

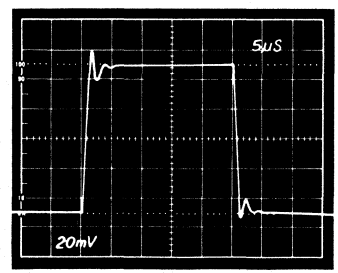


Figure 23d. Unity Gain Inverter Small Signal Pulse Response C_L = 1,000 pF

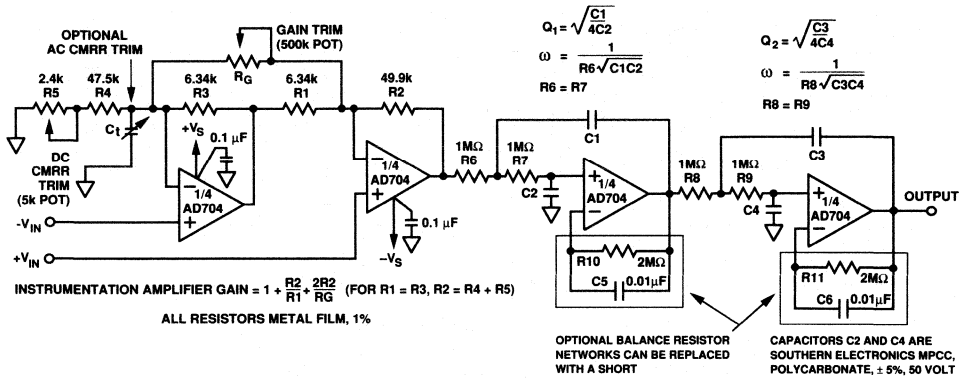


Figure 24. Gain of 10 Instrumentation Amplifier with Post Filtering

The instrumentation amplifier with post filtering (Figure 24) combines two applications which benefit greatly from the AD704. This circuit achieves low power and dc precision over temperature with a minimum of components.

The instrumentation amplifier circuit offers many performance benefits including BiFET level input bias currents, low input offset voltage drift and only 1.2 mA quiescent current. It will operate for gains G ≥ 2, and at lower gains it will benefit from the fact that there is no output amplifier offset and noise contribution as encountered in a 3 op amp design. Good low frequency CMRR is achieved even without the optional AC CMRR trim (Figure 25). Table I provides resistance values for 3 common circuit gains. For other gains, use the following equations:

$$R2 = R4 + R5 = 49.9\ k\Omega$$

$$R1 = R3 = \frac{49.9\ k\Omega}{0.9\ G - 1}$$

$$Max\ Value\ of\ R_G = \frac{99.8k}{0.06\ G}$$

$$C_t \approx \frac{1}{2\ \pi\ (R3)\ 5 \times 10^5}$$

Table I. Resistance Values for Various Gains

Circuit Gain (G)	R1 & R3	R_G (Max Value of Trim Potentiometer)	Bandwidth (−3 dB), Hz
10	6.34 kΩ	166 kΩ	50k
100	526 Ω	16.6 kΩ	5k
1,000	56.2 Ω	1.66 kΩ	0.5k

The 1 Hz, 4-pole active filter offers dc precision with a minimum of components and cost. The low current noise, I_{OS}, and I_B allow the use of 1 MΩ resistors without sacrificing the 1 µV/°C drift of the AD704. This means lower capacitor values may be used, reducing cost and space. Furthermore, since the AD704's I_B is as low as its I_{OS}, over most of the MIL temperature range, most applications do not require the use of the normal balancing resistor (with its stability capacitor). Adding the optional balancing resistor enhances performance at high temperatures, as shown in Figure 26. Table II gives capacitor values for several common low pass responses.

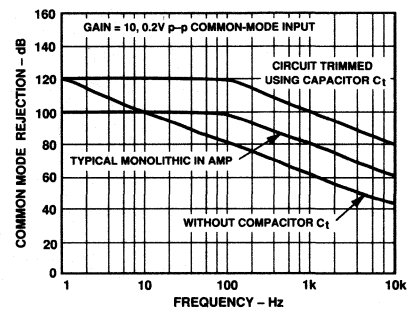


Figure 25. Common-Mode Rejection vs. Frequency with and without Capacitor C_t

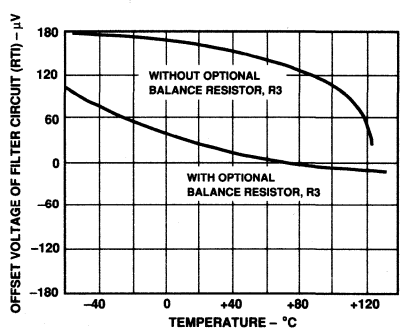


Figure 26. V_{OS} vs. Temperature Performance of the 1 Hz Filter Circuit

Table II. 1 Hz, 4-Pole Low Pass Filter Recommended Component Values

Desired Low Pass Response	Section 1 Frequency (Hz)	Q	Section 2 Frequency (Hz)	Q	C1 (μF)	C2 (μF)	C3 (μF)	C4 (μF)
Bessel	1.43	0.522	1.60	0.806	0.116	0.107	0.160	0.0616
Butterworth	1.00	0.541	1.00	1.31	0.172	0.147	0.416	0.0609
0.1 dB Chebychev	0.648	0.619	0.948	2.18	0.304	0.198	0.733	0.0385
0.2 dB Chebychev	0.603	0.646	0.941	2.44	0.341	0.204	0.823	0.0347
0.5 dB Chebychev	0.540	0.705	0.932	2.94	0.416	0.209	1.00	0.0290
1.0 dB Chebychev	0.492	0.785	0.925	3.56	0.508	0.206	1.23	0.0242

Specified Values are for a −3 dB point of 1.0 Hz. For other frequencies simply scale capacitors C1 through C4 directly; i.e., for 3 Hz Bessel response, C1 = 0.0387 μF, C2 = 0.0357 μF, C3 = 0.0533 μF, C4 = 0.0205 μF.

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD704JN	0°C to +70°C	N-14
AD704JR	0°C to +70°C	R-16
AD704JR-/REEL	0°C to +70°C	Tape and Reel
AD704KN	0°C to +70°C	N-14
AD704AN	−40°C to +85°C	N-14
AD704AQ	−40°C to +85°C	Q-14
AD704AR	−40°C to +85°C	R-16
AD704AR-REEL	−40°C to +85°C	Tape and Reel
AD704BQ	−40°C to +85°C	Q-14
AD704SE/883B	−55°C to +125°C	E-20A
AD704TQ	−55°C to +125°C	Q-14
AD704TQ/883B	−55°C to +125°C	Q-14

Chips are also available.
*E = Leadless Ceramic Chip Carrier; N = Plastic DIP; Q = Cerdip; R = Small Outline (SOIC). For outline information see Package Information section.

Picoampere Input Current Bipolar Op Amp

AD705

2

FEATURES

DC PERFORMANCE
- 25 μV max Offset Voltage (AD705T)
- 0.6 μV/°C max Drift (AD705K/T)
- 100 pA max Input Bias Current (AD705K)
- 250 pA max I_B Over MIL Temperature Range (AD705T)
- 114 dB min CMRR (AD705K/T)
- 114 dB min PSRR (AD705T)
- 200 V/mV min Open Loop Gain
- 0.5 μV p–p typ Noise, 0.1 Hz to 10 Hz
- 600 μA max Supply Current

AC PERFORMANCE
- 0.15 V/μs Slew Rate
- 800 kHz Unity Gain Crossover Frequency
- 10,000 pF Capacitive Load Drive Capability
- Low Cost
- Available in 8 Pin Plastic Mini-DIP, Hermetic Cerdip, Surface Mount (SOIC) Packages and in Chip Form
- Available in Tape and Reel in Accordance with EIA-481A Standard
- MIL-STD-883B Processing Available
- Dual Version Available: AD706
- Quad Version: AD704

APPLICATIONS
- Low Frequency Active Filters
- Precision Instrumentation
- Precision Integrators

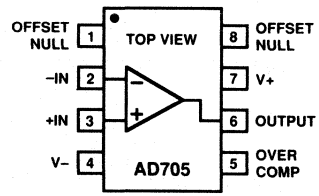
PRODUCT DESCRIPTION

The AD705 is a low power bipolar op amp that has the low input bias current of a BiFET amplifier but which offers a significantly lower I_B drift over temperature. The AD705 offers many of the advantages of BiFET and bipolar op amps without their inherent disadvantages. It utilizes superbeta bipolar input transistors to achieve the picoampere input bias current levels of FET input amplifiers (at room temperature), while its I_B typically only increases 5 times vs. BiFET amplifiers which exhibit a 1000X increase over temperature. This means that, at room temperature, while a typical BiFET may have less I_B than the AD705, the BiFET's input current will increase to a level of several nA at +125°C. Superbeta bipolar technology also permits the AD705 to achieve the microvolt offset voltage and low noise characteristics of a precision bipolar input amplifier.

The AD705 is a high quality replacement for the industry-standard OP-07 amplifier while drawing only one sixth of its power supply current. Since it has only 1/20th the input bias current of an OP-07, the AD705 can be used with much higher source impedances, while providing the same level of dc precision. In addition, since the input bias currents are at picoAmp levels, the commonly used "balancing" resistor (connected between the noninverting input of a bipolar op amp and ground) is not required.

CONNECTION DIAGRAM

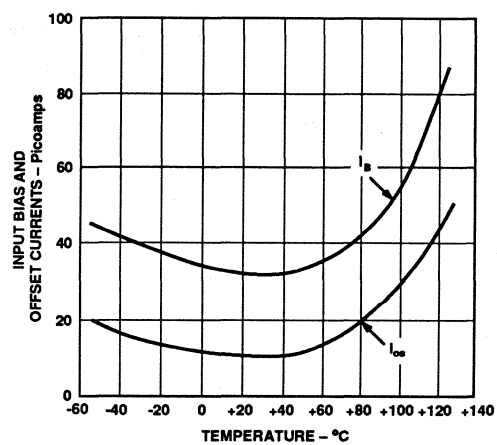
Plastic Mini-DIP (N)
Cerdip (Q) and
Plastic SOIC (R) Packages



The AD705 is an excellent choice for use in low frequency active filters in 12- and 14-bit data acquisition systems, in precision instrumentation and as a high quality integrator.

The AD705 is internally compensated for unity gain and is available in five performance grades. The AD705J and AD705K are rated over the commercial temperature range of 0 to +70°C. The AD705A and AD705B are rated over the industrial temperature range of −40°C to +85°C. The AD705T is rated over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

The AD705 is offered in three varieties of 8-pin package: plastic DIP, hermetic cerdip and surface mount (SOIC). "J" grade chips are also available.



AD705—SPECIFICATIONS (@ T_A = +25°C, V_{CM} = 0 V, and V_S = ±15 V dc, unless otherwise noted)

Parameter	Conditions	AD705J/A Min	AD705J/A Typ	AD705J/A Max	AD705K/B Min	AD705K/B Typ	AD705K/B Max	AD705T Min	AD705T Typ	AD705T Max	Units
INPUT OFFSET VOLTAGE											
Initial Offset			30	**90**		10	**35**		10	**25**	μV
Offset	T_{min} to T_{max}		45	150		25	**60**		25	**60**	μV
vs. Temp, Average TC			0.2	1.2		0.2	0.6		0.2	**0.6**	μV/°C
vs. Supply (PSRR)	V_S = ±2 V to ±18 V	**110**	129		**110**	129		**114**	129		dB
T_{min} to T_{max}	V_S = ±2.5 V to ±18 V	108	126		108	126		**108**	126		dB
Long Term Stability			0.3			0.3			0.3		μV/month
INPUT BIAS CURRENT[1]											
	V_{CM} = 0 V		60	**150**		30	**100**		30	**100**	pA
	V_{CM} = ±13.5 V		80	200		50	**150**		50	**150**	pA
vs. Temp, Average TC			0.3			0.3			0.6		pA/°C
T_{min} to T_{max}	V_{CM} = 0 V		80	250		50	150		90	**250**	pA
T_{min} to T_{max}	V_{CM} = ±13.5 V		100	450		70	350		120	**450**	pA
INPUT OFFSET CURRENT	V_{CM} = 0 V		40	**150**		30	**100**		30	**100**	pA
	V_{CM} = ±13.5 V		40	200		30	**150**		30	**150**	pA
vs. Temp, Average TC			0.3			0.3			0.4		pA/°C
T_{min} to T_{max}	V_{CM} = 0 V		80	250		50	150		80	**250**	pA
T_{min} to T_{max}	V_{CM} = ±13.5 V		80	450		50	350		80	**450**	pA
FREQUENCY RESPONSE											
Unity Gain											
Crossover Frequency		0.4	0.8		0.4	0.8		0.4	0.8		MHz
Slew Rate, Unity Gain	G = −1	0.1	0.15		0.1	0.15		0.1	0.15		V/μs
Slew Rate	T_{min} to T_{max}	0.05	0.15		0.05	0.15		0.05	0.15		V/μs
INPUT IMPEDANCE											
Differential			40//2			40//2			40//2		MΩ//pF
Common Mode			300//2			300//2			300//2		GΩ//pF
INPUT VOLTAGE RANGE											
Common Mode Voltage		±13.5	±14		±13.5	±14		±13.5	±14		V
COMMON MODE											
REJECTION RATIO	V_{CM} = ±13.5 V	**110**	132		**114**	132		**114**	132		dB
	T_{min} to T_{max}	108	128		108	128		**108**	128		dB
INPUT VOLTAGE NOISE	0.1 Hz to 10 Hz		0.5			0.5	1.0		0.5	1.0	μV p-p
	f = 10 Hz		17			17			17		nV/$\sqrt{Hz}$
	f = 1 kHz		15	22		15	22		15	22	nV/$\sqrt{Hz}$
INPUT CURRENT NOISE	f = 10 Hz		50			50			50		fA/$\sqrt{Hz}$
OPEN LOOP GAIN	V_O = ±12 V										
	R_{LOAD} = 10 kΩ	**300**	2000		**400**	2000		**400**	2000		V/mV
	T_{min} to T_{max}	200	1500		300	1500		300	1500		V/mV
	V_O = ±10 V										
	R_{LOAD} = 2 kΩ	**200**	1000		**300**	1000		**300**	1000		V/mV
	T_{min} to T_{max}	150	1000		200	1000		**100**	1000		V/mV
OUTPUT CHARACTERISTICS											
Voltage Swing	R_{LOAD} = 10 kΩ	±13	±14		±13	±14		±13	±14		V
	T_{min} to T_{max}	**±13**	±14		**±13**	±14		**±13**	±14		V
Current	Short Circuit		±15			±15			±15		mA
Capacitive Load											
Drive Capability	Gain = +1		10,000			10,000			10,000		pF
Output Resistance	Open Loop		200			200			200		Ω
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		**±2.0**		**±18**	**±2.0**		**±18**	**±2.0**		**±18**	V
Quiescent Current			380	**600**		380	**600**		380	**600**	μA
	T_{min} to T_{max}		400	800		400	800		400	**800**	μA
TEMPERATURE RANGE											
FOR RATED PERFORMANCE											
Commercial (0 to +70°C)			AD705J			AD705K					
Industrial (−40°C to +85°C)			AD705A			AD705B					
Military (−55°C to +125°C)									AD705T		

Parameter	Conditions	AD705J/A Min	AD705J/A Typ	AD705J/A Max	AD705K/B Min	AD705K/B Typ	AD705K/B Max	AD705T Min	AD705T Typ	AD705T Max	Units
PACKAGE OPTIONS[2]											
8-Pin Cerdip (Q-8)			AD705AQ			AD705BQ			AD705TQ		
8-Pin Plastic Mini-DIP (N-8)			AD705JN			AD705KN					
8-Pin SOIC (R-8)			AD705JR								
Tape + Reel			AD705JR-REEL								
Chips			AD705JCHIPS								
TRANSISTOR COUNT	# of Transistors		45			45			45		

NOTES
[1]Bias Current Specifications are guaranteed maximum at either input.
[2]For outline information see Package Information section.
All min and max specifications are guaranteed.
Specifications in **boldface** are tested on all production units at final electrical test.
Results from those tests are used to calculate outgoing quality levels.
Specifications subject to change without notice.

2

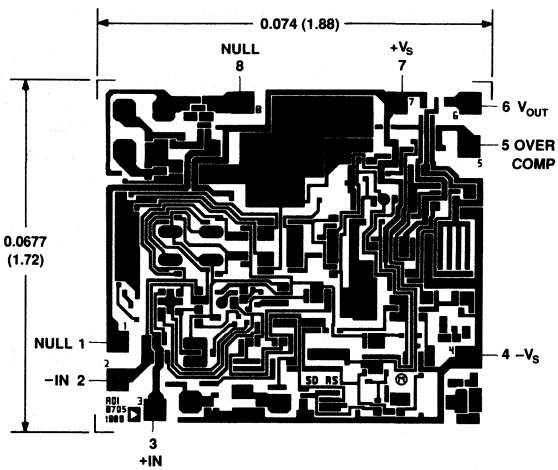
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2] . . . . . 650 mW
Input Voltage . . . . . $\pm V_S$
Differential Input Voltage[3] . . . . . ±0.7 Volts
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range (Q) . . . . . −65°C to +150°C
Storage Temperature Range (N, R) . . . . . −65°C to +125°C
Operating Temperature Range
AD705J/K . . . . . 0 to +70°C
AD705A/B . . . . . −40°C to +85°C
AD705T . . . . . −55°C to +125°C
Lead Temperature Range
(Soldering 60 seconds) . . . . . 300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Pin Plastic Package: θ_{JA} = 165°C/Watt
8-Pin Cerdip Package: θ_{JA} = 110°C/Watt
8-Pin Small Outline Package: θ_{JA} = 155°C/Watt
[3]The Input pins of this amplifier are protected by back-to-back diodes. If the differential voltage exceeds ±0.7 volts, external series protection resistors should be added to limit the input current to less than 25 mA.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



AD705—Typical Characteristics (@ +25°C, V_S = ±15 V, unless otherwise noted)

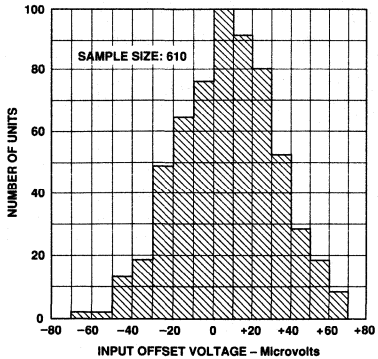


Figure 1. Typical Distribution of Input Offset Voltage

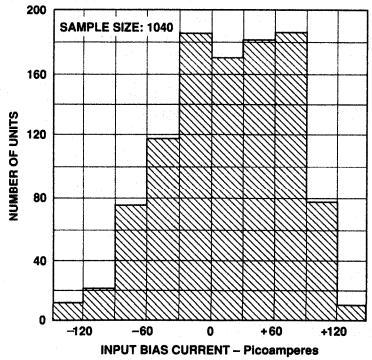


Figure 2. Typical Distribution of Input Bias Current

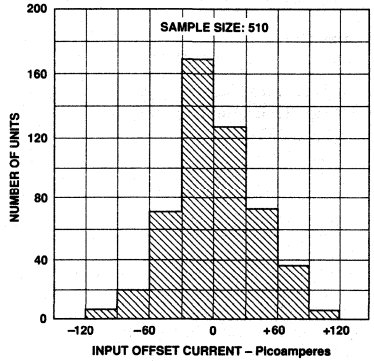


Figure 3. Typical Distribution of Input Offset Current

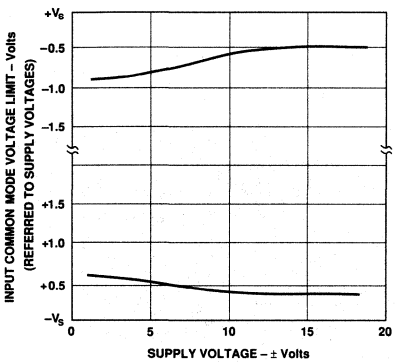


Figure 4. Input Common Mode Voltage Range vs. Supply Voltage

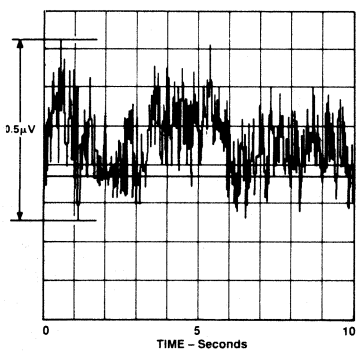


Figure 5. 0.1 Hz to 10 Hz Noise Voltage

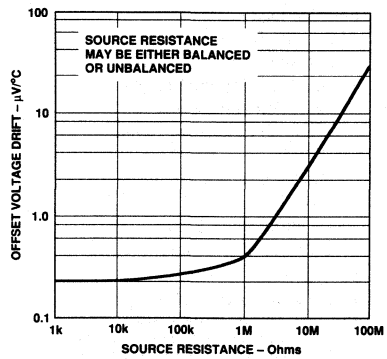


Figure 6. Offset Voltage Drift vs. Source Resistance

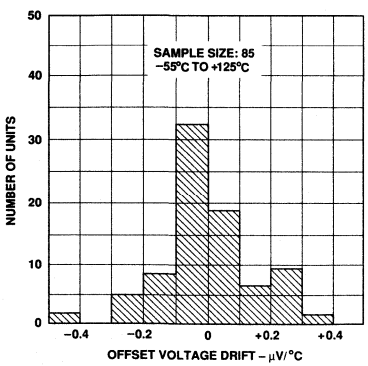


Figure 7. Typical Distribution of Offset Voltage Drift

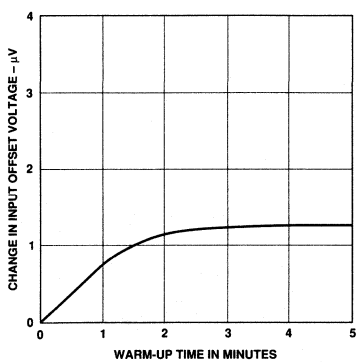


Figure 8. Change in Input Offset Voltage vs. Warm-Up Time

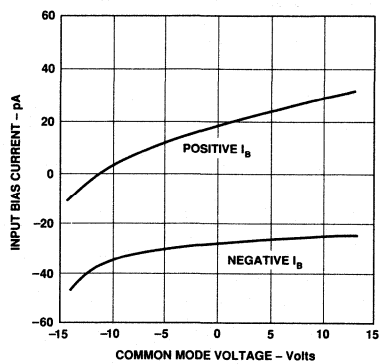


Figure 9. Input Bias Current vs. Common Mode Voltage

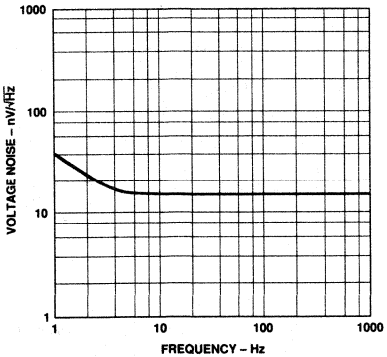


Figure 10. Input Noise Voltage Spectral Density

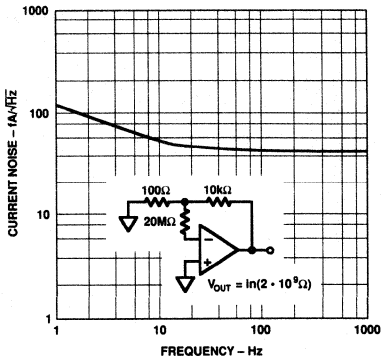


Figure 11. Input Noise Current Spectral Density

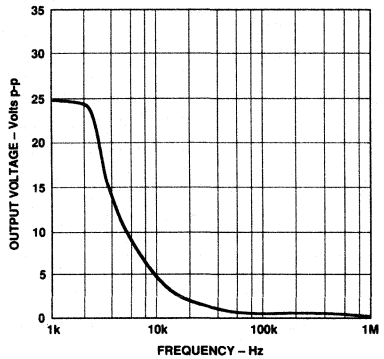


Figure 12. Large Signal Frequency Response

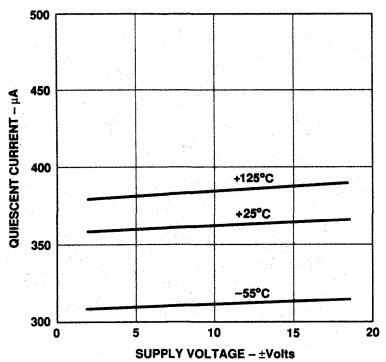


Figure 13. Quiescent Supply Current vs. Supply Voltage

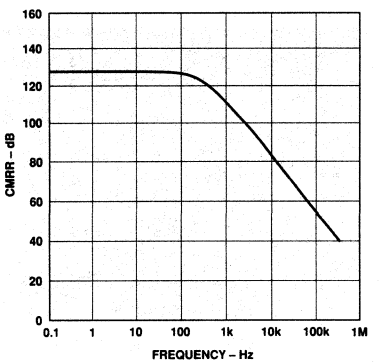


Figure 14. Common Mode Rejection vs. Frequency

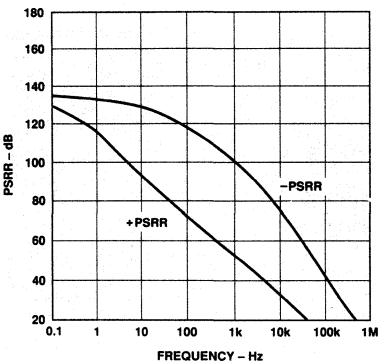


Figure 15. Power Supply Rejection vs. Frequency

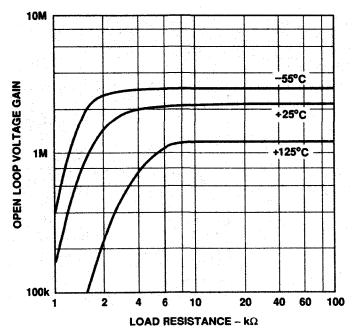


Figure 16. Open Loop Gain vs. Load Resistance over Temperature

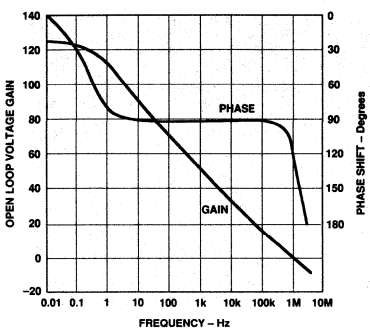


Figure 17. Open Loop Gain and Phase Shift vs. Frequency

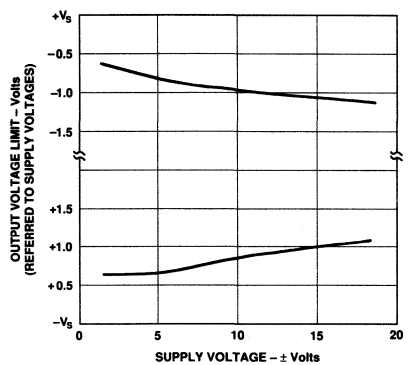


Figure 18. Output Voltage Limit vs. Supply Voltage

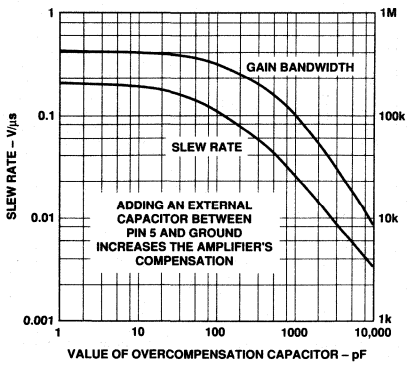


Figure 19. Slew Rate & Gain Bandwidth Product vs. Value of Overcompensation Capacitor

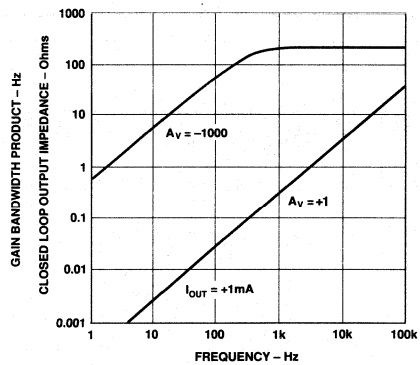


Figure 20. Magnitude of Closed Loop Output Impedance vs. Frequency

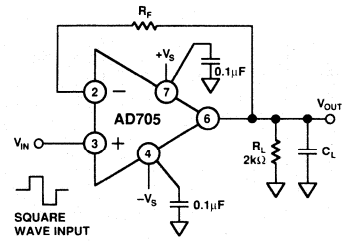


Figure 21a. Unity Gain Follower (For Large Signal Applications, Resistor R_F Limits the Current Through the Input Protection Diodes)

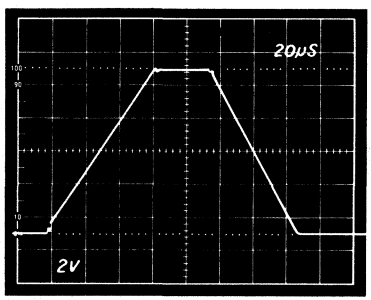


Figure 21b. Unity Gain Follower Large Signal Pulse Response
R_F = 10 kΩ, C_L = 50 pF

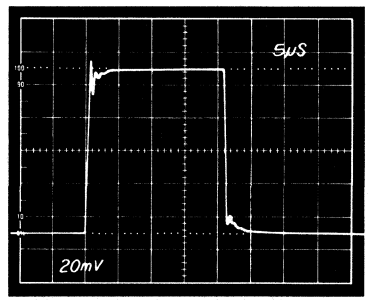


Figure 21c. Unity Gain Follower Small Signal Pulse Response
R_F = 0 Ω, C_L = 100 pF

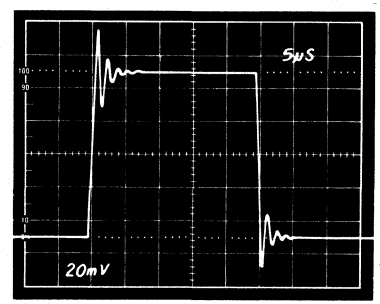


Figure 21d. Unity Gain Follower Small Signal Pulse Response
R_F = 0 Ω, C_L = 1000 pF

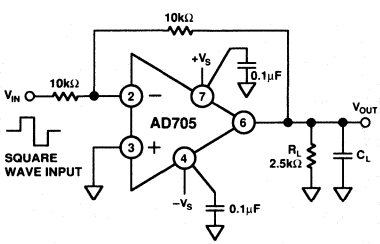


Figure 22a. Unity Gain Inverter

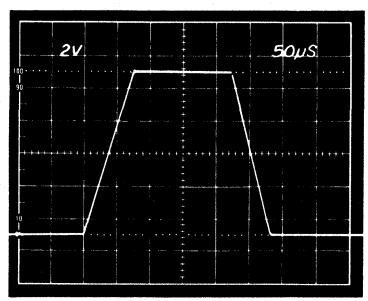


Figure 22b. Unity Gain Inverter Large Signal Pulse Response
C_L = 50 pF

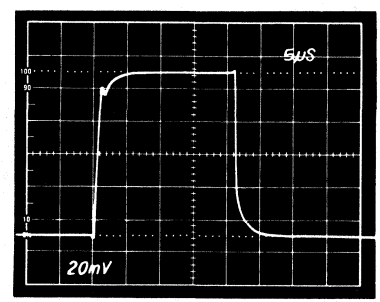


Figure 22c. Unity Gain Inverter Small Signal Pulse Response
C_L = 100 pF

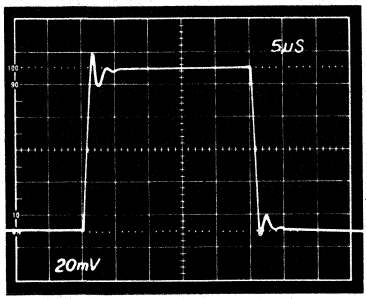


Figure 22d. Unity Gain Inverter Small Signal Pulse Response C_L = 1000 pF

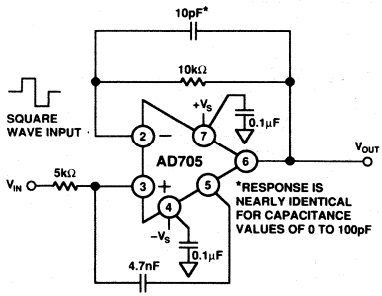


Figure 23a. Follower Connected in Feed-Forward Mode

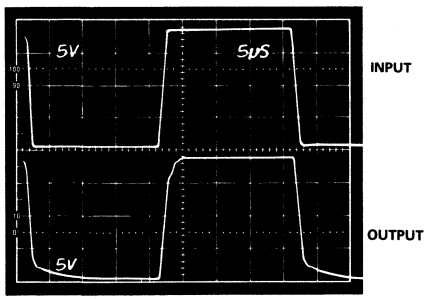


Figure 23b. Follower Feed-Forward Pulse Response

A High Performance Differential Amplifier Circuit

Figure 25 shows a high input impedance, differential amplifier circuit that features a high common mode voltage, and which operates at low power. Table I details its performance with changes in gain. To optimize the common mode rejection of this circuit at low frequencies and dc, apply a 1 volt, 1 Hz sine wave to both inputs. Measuring the output with an oscilloscope, adjust trimming potentiometer R6 for minimum output. For the best CMR at higher frequencies, capacitor C2 should be replaced with a 1.5 pF to 20 pF trimmer capacitor.

Both the IC socket and any standoffs at the op amp's input terminals should be made of Teflon* to maintain low input current drift over temperature.

*Teflon is a registered trademark of E.I. DuPont, Co.

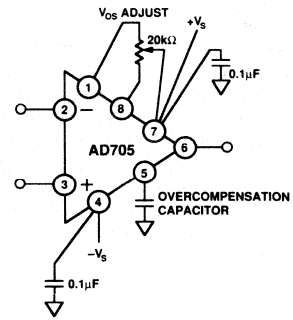


Figure 24. Offset Null and Overcompensation Connections

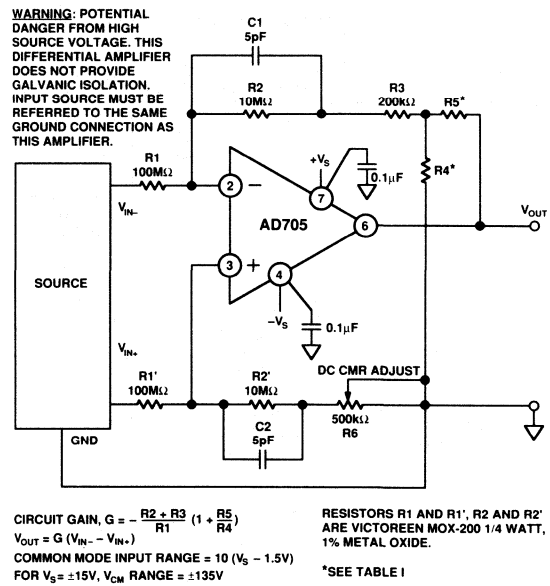


Figure 25. A High Performance Differential Amplifier Circuit

Table I. Typical Performance of Differential Amplifier Circuit Operating at Various Gains

Circuit Gain	R4 (Ω)	R5 (Ω)	Trimmed DC CMR (dB)	RTI Average Drift TC (μV/°C)	Circuit Bandwidth −3 dB
1	1.13 kΩ	10 kΩ	≥85	30	4.4 kHz
10	100 Ω	9.76 kΩ	≥85	30	2.8 kHz
100	10.2 Ω	10 kΩ	≥85	30	930 Hz

A 1 Hz, 2-Pole, Active Filter

Table II gives recommended component values for the 1 Hz filter of Figure 26. An unusual characteristic of the AD705 is that both the input bias current and the input offset current and their drift remain low over most of the op amps rated temperature range. Therefore, for most applications, there is no need to use the normal balancing resistor tied between the noninverting terminal of the op amp and ground. Eliminating the standard balancing resistor reduces board space and lowers circuit noise. However, this resistor is needed at temperatures above 110°C, because input bias current starts to change rapidly, as shown by Figure 27.

Table II. Recommended Component Values for the 1 Hz Low Pass Filter

Desired Low Pass Response	Pole Frequency (Hz)	Pole Q	C1 Value (μF)	C2 Value (μF)
Bessel Response	1.27	0.58	0.14	0.11
Butterworth Response	1.00	0.707	0.23	0.11
0.1 dB Chebychev	0.93	0.77	0.26	0.11
0.2 dB Chebychev	0.90	0.80	0.28	0.11
0.5 dB Chebychev	0.85	0.86	0.32	0.11
1.0 dB Chebychev	0.80	0.96	0.38	0.10

Specified Values are for a −3 dB point of 1.0 Hz.

For other frequencies, simply scale capacitors C1 and C2 directly; i.e., for 3 Hz Bessel response, C1 = 0.046 μF, C2 = 0.037 μF.

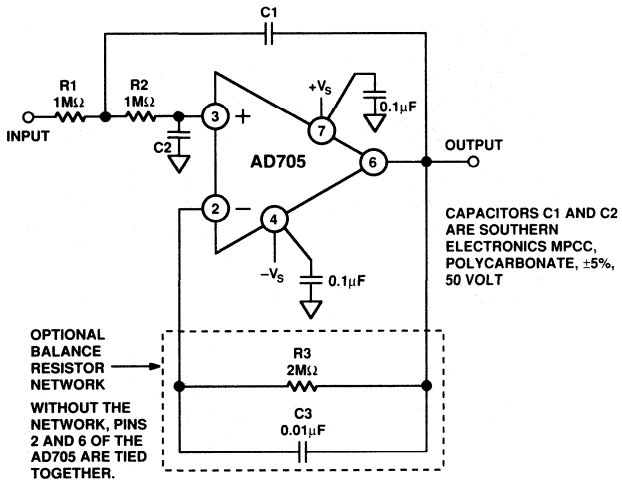


Figure 26. A 1 Hz, 2-Pole Active Filter

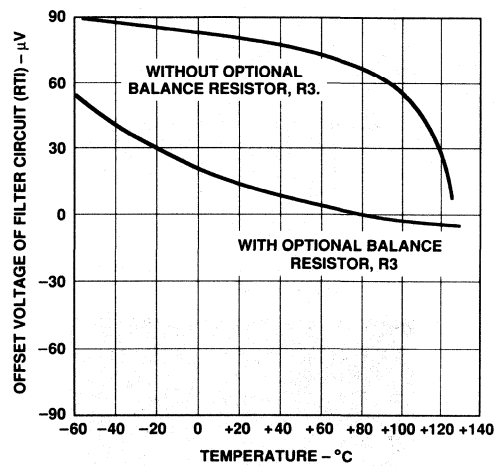


Figure 27. V_{OS} vs. Temperature of 1 Hz Filter

Dual Picoampere Input Current Bipolar Op Amp

AD706

FEATURES

HIGH DC PRECISION
50 μV max Offset Voltage
0.6 μV/°C max Offset Drift
110 pA max Input Bias Current

LOW NOISE
0.5 μV p–p Voltage Noise, 0.1 Hz to 10 Hz

LOW POWER
750 μA Supply Current

Available in 8-Pin Plastic Mini-DIP, Hermetic Cerdip and Surface Mount (SOIC) Packages
Available in Tape and Reel in Accordance with EIA-481A Standard
MIL-STD-883B Processing Available
Single Version: AD705, Quad Version (AD704)

PRIMARY APPLICATIONS
Low Frequency Active Filters
Precision Instrumentation
Precision Integrators

PRODUCT DESCRIPTION

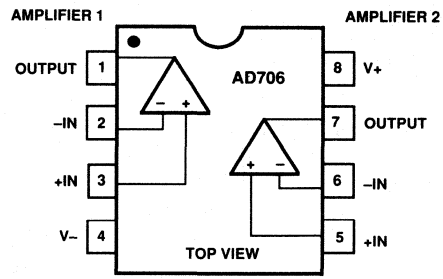
The AD706 is a dual, low power, bipolar op amp that has the low input bias current of a BiFET amplifier but which offers a significantly lower I_B drift over temperature. It utilizes super-beta bipolar input transistors to achieve picoampere input bias current levels (similar to FET input amplifiers at room temperature), while its I_B typically only increases by 5× at 125°C (unlike a BiFET amp, for which I_B doubles every 10°C for a 1000× increase at 125°C). The AD706 also achieves the microvolt offset voltage and low noise characteristics of a precision bipolar input amplifier.

Since it has only 1/20 the input bias current of an OP-07, the AD706 does not require the commonly used "balancing" resistor. Furthermore, the current noise is 1/5 that of the OP-07 which makes this amplifier usable with much higher source impedances. At 1/6 the supply current (per amplifier) of the OP-07, the AD706 is better suited for today's higher density boards.

The AD706 is an excellent choice for use in low frequency active filters in 12- and 14-bit data acquisition systems, in precision instrumentation, and as a high quality integrator. The AD706 is internally compensated for unity gain and is available in five performance grades. The AD706J and AD706K are rated over the commercial temperature range of 0°C to +70°C. The AD706A and AD706B are rated over the industrial temperature range of −40°C to +85°C. The AD706T is rated over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

CONNECTION DIAGRAM

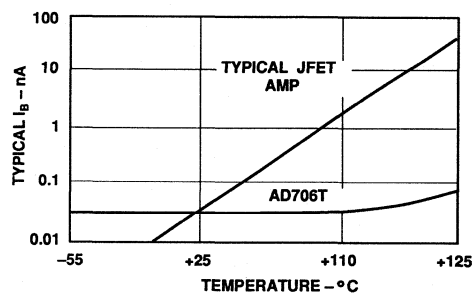
Plastic Mini-DIP (N)
Cerdip (Q) and
Plastic SOIC (R) Packages



The AD706 is offered in three varieties of an 8-pin package: plastic mini-DIP, hermetic cerdip and surface mount (SOIC). "J" grade chips are also available.

PRODUCT HIGHLIGHTS

1. The AD706 is a dual low drift op amp that offers BiFET level input bias currents, yet has the low I_B drift of a bipolar amplifier. It may be used in circuits using dual op amps such as the LT1024.
2. The AD706 provides both low drift and high dc precision.
3. The AD706 can be used in applications where a chopper amplifier would normally be required but without the chopper's inherent noise.



AD706—SPECIFICATIONS (@ T_A = +25°C, V_{CM} = 0 V, and ±15 V dc, unless otherwise noted)

Parameter	Conditions	AD706J/A Min	AD706J/A Typ	AD706J/A Max	AD706K/B Min	AD706K/B Typ	AD706K/B Max	AD706T Min	AD706T Typ	AD706T Max	Units
INPUT OFFSET VOLTAGE											
Initial Offset			30	100		10	50		10	50	µV
Offset	T_{min} to T_{max}		40	150		25	100		25	100	µV
vs. Temp, Average TC			0.2	1.5		0.2	0.6		0.2	0.6	µV/°C
vs. Supply (PSRR)	V_S = ±2 V to ±18 V	110	132		112	132		112	132		dB
T_{min} to T_{max}	V_S = ±2.5 V to ±18 V	106	126		108	126		108	126		dB
Long Term Stability			0.3			0.3			0.3		µV/month
INPUT BIAS CURRENT[1]											
	V_{CM} = 0 V		50	200		30	110		30	120	pA
	V_{CM} = ±13.5 V			250			160			170	pA
vs. Temp, Average TC			0.3			0.2			0.2		pA/°C
T_{min} to T_{max}	V_{CM} = 0 V			300			200			400	pA
T_{min} to T_{max}	V_{CM} = ±13.5 V			400			300			600	pA
INPUT OFFSET CURRENT	V_{CM} = 0 V		30	150		30	100		30	100	pA
	V_{CM} = ±13.5 V			250			200			200	pA
vs. Temp, Average TC			0.6			0.4			0.4		pA/°C
T_{min} to T_{max}	V_{CM} = 0 V		80	250		80	200		80	300	pA
T_{min} to T_{max}	V_{CM} = ±13.5 V		80	350		80	300		80	450	pA
MATCHING CHARACTERISTICS											
Offset Voltage				150			75			75	µV
	T_{min} to T_{max}			250			150			200	µV
Input Bias Current[2]				300			150			200	pA
	T_{min} to T_{max}			500			250			400	pA
Common-Mode Rejection		106			110			110			dB
	T_{min} to T_{max}	106			108			108			dB
Power Supply Rejection		106			110			110			dB
	T_{min} to T_{max}	104			106			106			dB
Crosstalk	@ f = 10 Hz										
(Figure 19a)	R_L = 2 kΩ		150			150			150		dB
FREQUENCY RESPONSE											
Unity Gain Crossover											
Frequency			0.8			0.8			0.8		MHz
Slew Rate	G = −1		0.15			0.15			0.15		V/µs
	T_{min} to T_{max}		0.15			0.15			0.15		V/µs
INPUT IMPEDANCE											
Differential			40//2			40//2			40//2		MΩ//pF
Common Mode			300//2			300//2			300//2		GΩ//pF
INPUT VOLTAGE RANGE											
Common-Mode Voltage		±13.5	±14		±13.5	±14		±13.5	±14		V
Common-Mode Rejection											
Ratio	V_{CM} = ±13.5 V	110	132		114	132		114	132		dB
	T_{min} to T_{max}	108	128		108	128		108	128		dB
INPUT CURRENT NOISE	0.1 Hz to 10 Hz		3			3			3		pA p-p
	f = 10 Hz		50			50			50		fA/√Hz
INPUT VOLTAGE NOISE	0.1 Hz to 10 Hz		0.5			0.5	1.0		0.5	1.0	µV p-p
	f = 10 Hz		17			17			17		nV/√Hz
	f = 1 kHz		15	22		15	22		15	22	nV/√Hz
OPEN-LOOP GAIN	V_O = ±12 V										
	R_{LOAD} = 10 kΩ	200	2000		400	2000		400	2000		V/mV
	T_{min} to T_{max}	150	1500		300	1500		300	1500		V/mV
	V_O = ±10 V										
	R_{LOAD} = 2 kΩ	200	1000		300	1000		200	1000		V/mV
	T_{min} to T_{max}	150	1000		200	1000		100	1000		V/mV
OUTPUT CHARACTERISTICS											
Voltage Swing	R_{LOAD} = 10 kΩ	±13	±14		±13	±14		±13	±14		V
	T_{min} to T_{max}	±13	±14		±13	±14		±13	±14		V
Current	Short Circuit		±15			±15			±15		mA
Capacitive Load											
Drive Capability	Gain = +1		10,000			10,000			10,000		pF

Parameter	Conditions	AD706J/A Min	AD706J/A Typ	AD706J/A Max	AD706K/B Min	AD706K/B Typ	AD706K/B Max	AD706T Min	AD706T Typ	AD706T Max	Units
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		±2.0		±18	±2.0		±18	±2.0		±18	V
Quiescent Current, Total			0.75	1.2		0.75	1.2		0.75	1.2	mA
	T_{min} to T_{max}		0.8	1.4		0.8	1.4		0.8	1.6	mA
TRANSISTOR COUNT	# of Transistors		90			90			90		

NOTES
[1]Bias current specifications are guaranteed maximum at either input.
[2]Input bias current match is the difference between corresponding inputs (I_B of −IN of Amplifier #1 minus I_B of −IN of Amplifier #2).
CMRR match is the difference between $\frac{\Delta V_{OS}\#1}{\Delta V_{CM}}$ for amplifier #1 and $\frac{\Delta V_{OS}\#2}{\Delta V_{CM}}$ for amplifier #2 expressed in dB.
PSRR match is the difference between $\frac{\Delta V_{OS}\#1}{\Delta V_{SUPPLY}}$ for amplifier #1 and $\frac{\Delta V_{OS}\#2}{\Delta V_{SUPPLY}}$ for amplifier #2 expressed in dB.
All min and max specifications are guaranteed.
Specifications subject to change without notice.

2

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation
(Total: Both Amplifiers)[2] . . . . . 650 mW
Input Voltage . . . . . $\pm V_S$
Differential Input Voltage[3] . . . . . ±0.7 Volts
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range (Q) . . . . . −65°C to +150°C
Storage Temperature Range (N, R) . . . . . −65°C to +125°C
Operating Temperature Range
AD706J/K . . . . . 0°C to +70°C
AD706A/B . . . . . −40°C to +85°C
AD706T . . . . . −55°C to +125°C
Lead Temperature (Soldering 10 secs) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air:
8-Pin Plastic Package: θ_{JA} = 100°C/Watt
8-Pin Cerdip Package: θ_{JA} = 110°C/Watt
8-Pin Small Outline Package: θ_{JA} = 155°C/Watt
[3]The input pins of this amplifier are protected by back-to-back diodes. If the differential voltage exceeds ±0.7 volts, external series protection resistors should be added to limit the input current to less than 25 mA.

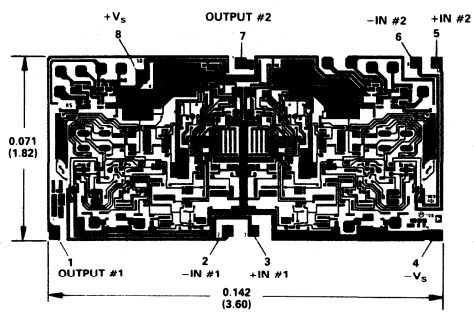
ORDERING GUIDE

Model	Temperature Range	Description	Package Option*
AD706JN	0°C to +70°C	Plastic DIP	N-8
AD706KN	0°C to +70°C	Plastic DIP	N-8
AD706JR	0°C to +70°C	SOIC	R-8
AD706JR-REEL	0°C to +70°C	Tape & Reel	
AD706AQ	−40°C to +85°C	Cerdip	Q-8
AD706BQ	−40°C to +85°C	Cerdip	Q-8
AD706AR	−40°C to +85°C	SOIC	R-8
AD706AR-REEL	−40°C to +85°C	Tape & Reel	
AD706TQ	−55°C to +125°C	Cerdip	Q-8

*For outline information see Package Information section.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



AD706—Typical Characteristics (@ +25°C, V_S = ±15 V, unless otherwise noted)

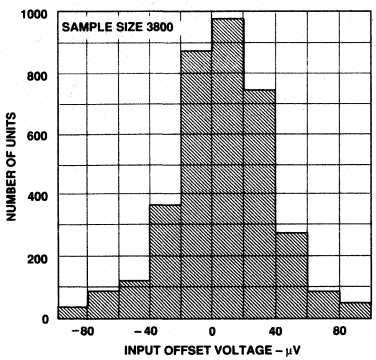


Figure 1. Typical Distribution of Input Offset Voltage

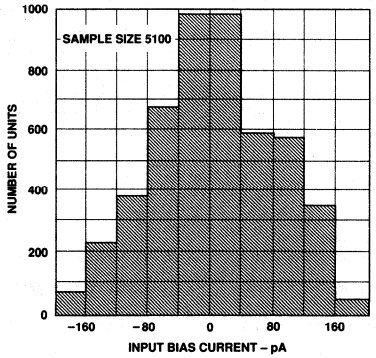


Figure 2. Typical Distribution of Input Bias Current

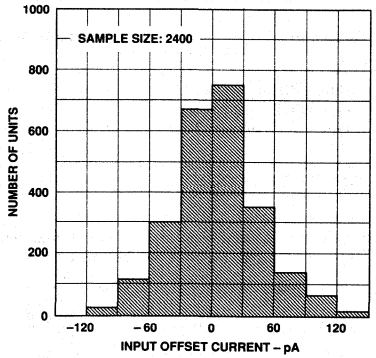


Figure 3. Typical Distribution of Input Offset Current

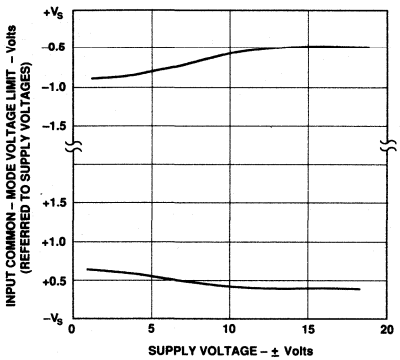


Figure 4. Input Common-Mode Voltage Range vs. Supply Voltage

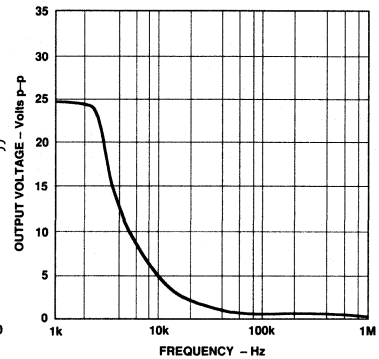


Figure 5. Large Signal Frequency Response

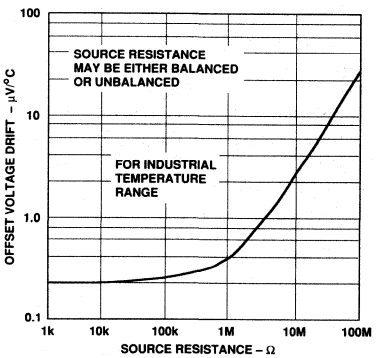


Figure 6. Offset Voltage Drift vs. Source Resistance

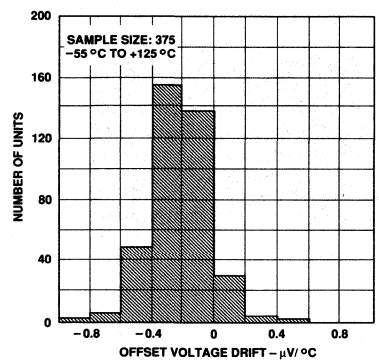


Figure 7. Typical Distribution of Offset Voltage Drift

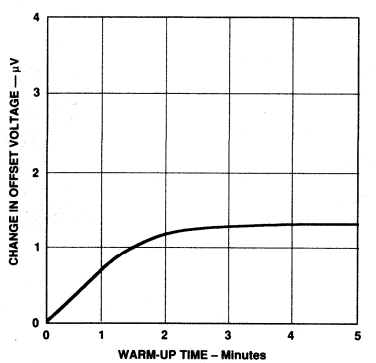


Figure 8. Change in Input Offset Voltage vs. Warm-up Time

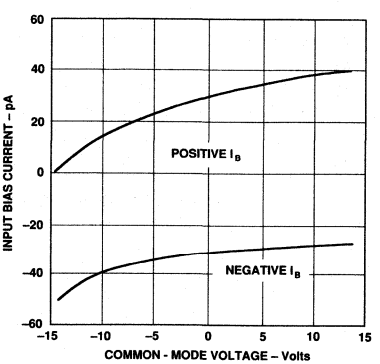


Figure 9. Input Bias Current vs. Common-Mode Voltage

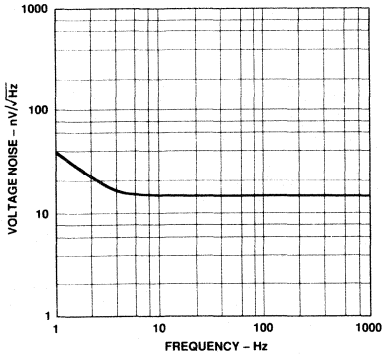


Figure 10. Input Noise Voltage Spectral Density

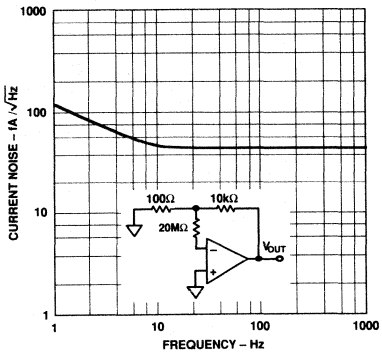


Figure 11. Input Noise Current Spectral Density

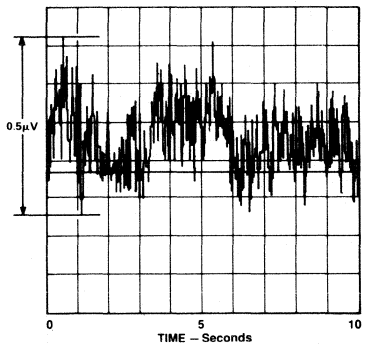


Figure 12. 0.1 Hz to 10 Hz Noise Voltage

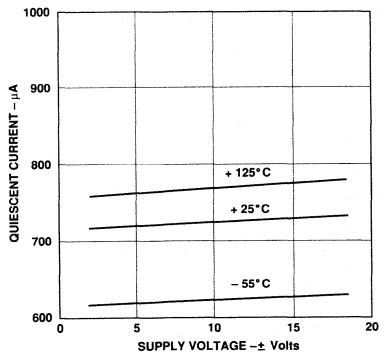


Figure 13. Quiescent Supply Current vs. Supply Voltage

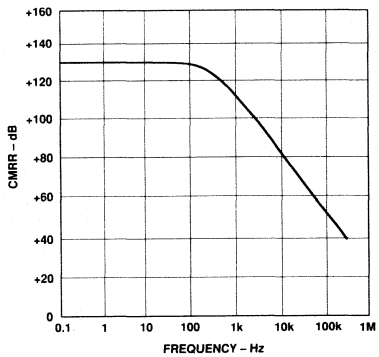


Figure 14. Common-Mode Rejection Ratio vs. Frequency

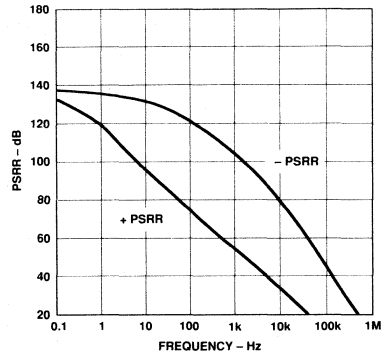


Figure 15. Power Supply Rejection Ratio vs. Frequency

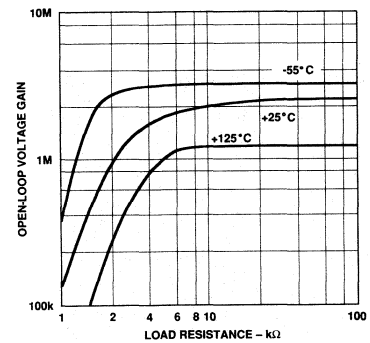


Figure 16. Open-Loop Gain vs. Load Resistance vs. Temperature

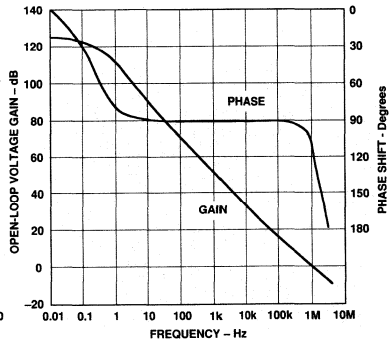


Figure 17. Open-Loop Gain and Phase Shift vs. Frequency

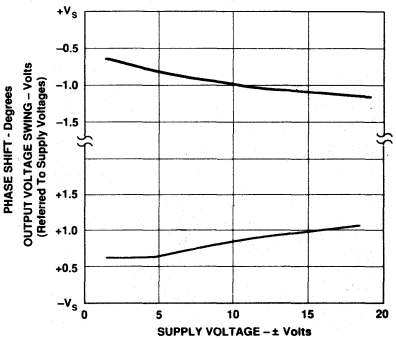


Figure 18. Output Voltage Swing vs. Supply Voltage

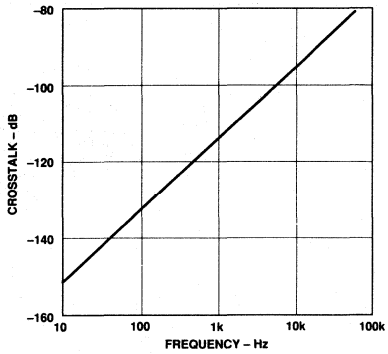


Figure 19a. Crosstalk vs. Frequency

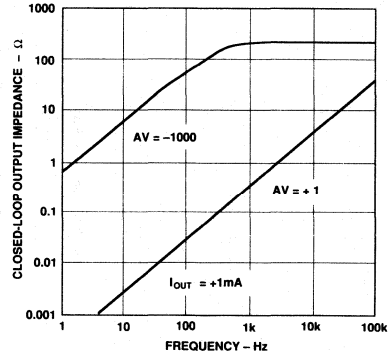


Figure 20. Magnitude of Closed-Loop Output Impedance vs. Frequency

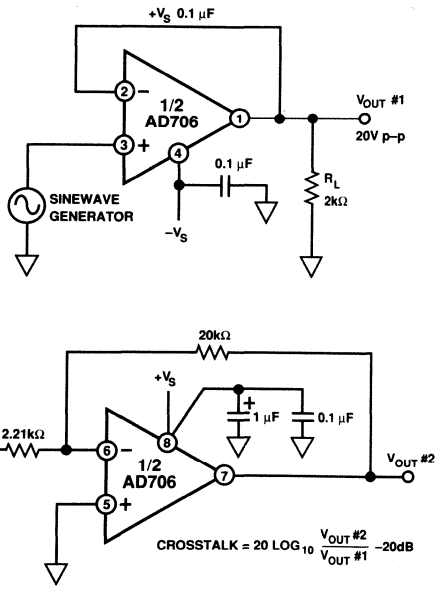


Figure 19b. Crosstalk Test Circuit

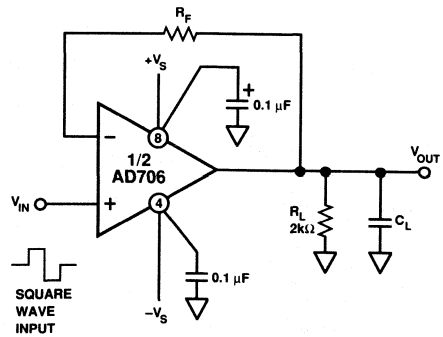


Figure 21a. Unity Gain Follower (For Large Signal Applications, Resistor R_F Limits the Current Through the Input Protection Diodes.)

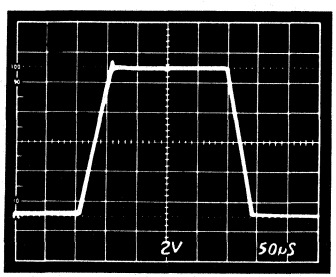


Figure 21b. Unity Gain Follower Large Signal Pulse Response R_F = 10 kΩ, C_L = 1,000 pF

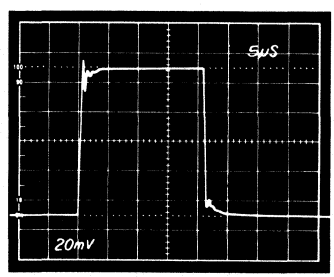


Figure 21c. Unity Gain Follower Small Signal Pulse Response R_F = 0 Ω, C_L = 100 pF

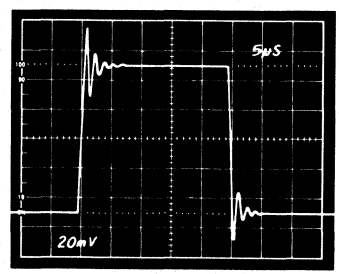


Figure 21d. Unity Gain Follower Small Signal Pulse Response R_F = 0 Ω, C_L = 1000 pF

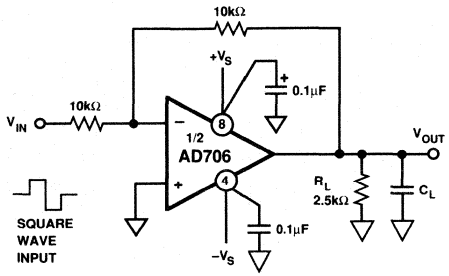


Figure 22a. Unity Gain Inverter Connection

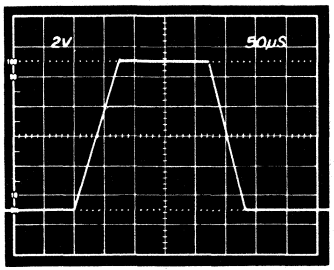


Figure 22b. Unity Gain Inverter Large Signal Pulse Response C_L = 1,000 pF

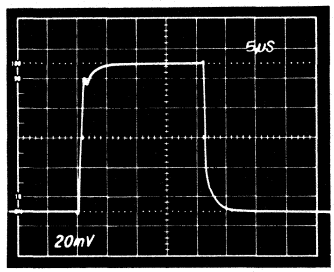


Figure 22c. Unity Gain Inverter Small Signal Pulse Response C_L = 100 pF

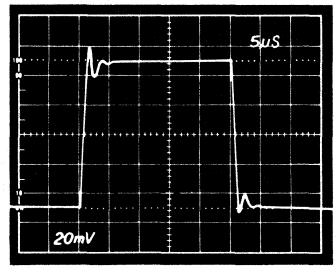


Figure 22d. Unity Gain Inverter Small Signal Pulse Response C_L = 1000 pF

Figure 23 shows an in-amp circuit which has the obvious advantage of requiring only one AD706 rather than three op amps, with subsequent savings in cost and power consumption. The transfer function of this circuit (without R_G) is:

$$V_{OUT} = (V_{IN\#1} - V_{IN\#2})\left(1 + \frac{R_4}{R_3}\right)$$

$$for\ R_1 = R_4\ and\ R_2 = R_3$$

Input resistance is high, thus permitting the signal source to have an unbalanced output impedance.

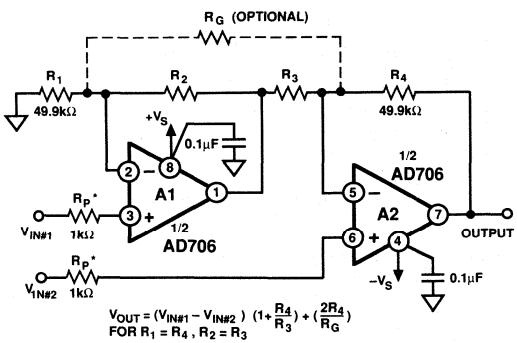


Figure 23. A Two Op-Amp Instrumentation Amplifier

Furthermore, the circuit gain may be fine trimmed using an optional trim resistor, R_G. Like the three op-amp circuit, CMR increases with gain, once initial trimming is accomplished—but CMR is still dependent upon the ratio matching of Resistors R_1 through R_4. Resistor values for this circuit using the optional gain resistor, R_G, can be calculated using:

$$R_1 = R_4 = 49.9\ k\Omega$$

$$R_2 = R_3 = \frac{49.9\ k\Omega}{0.9\ G - 1}$$

$$R_G = \frac{99.8\ k\Omega}{0.06G}$$

$$where\ G = Desired\ Circuit\ Gain$$

Table I provides practical 1% resistance values. (Note that without resistor R_G, R_2 and R_3 = 49.9 kΩ/G−1.)

Table 1. Operating Gains of Amplifiers A1 and A2 and Practical 1% Resistor Values for the Circuit of Figure 23

Circuit Gain	Gain of A1	Gain of A2	R_2, R_3	R_1, R_4
1.10	11.00	1.10	499 kΩ	49.9 kΩ
1.33	4.01	1.33	150 kΩ	49.9 kΩ
1.50	3.00	1.50	100 kΩ	49.9 kΩ
2.00	2.00	2.00	49.9 kΩ	49.9 kΩ
10.1	1.11	10.10	5.49 kΩ	49.9 kΩ
101.0	1.01	101.0	499 Ω	49.9 kΩ
1001	1.001	1001	49.9 Ω	49.9 kΩ

For a much more comprehensive discussion of in-amp applications, refer to the *Instrumentation Amplifier Application Guide* —available free from Analog Devices, Inc.

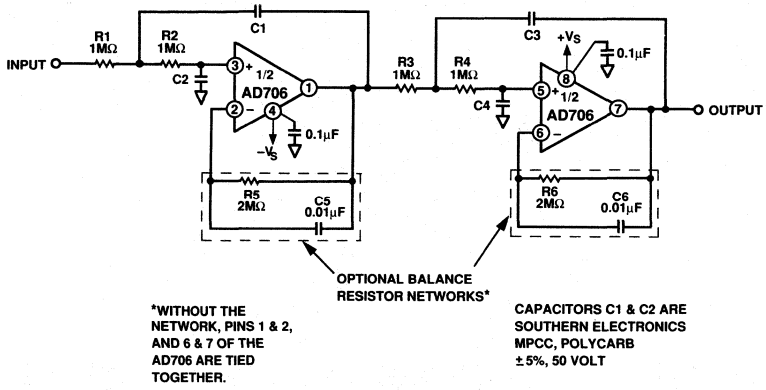


Figure 24. A 1 Hz, 4-Pole Active Filter

A 1 Hz, 4-Pole, Active Filter

Figure 24 shows the AD706 in an active filter application. An important characteristic of the AD706 is that both the input bias current, input offset current and their drift remain low over most of the op amp's rated temperature range. Therefore, for most applications, there is no need to use the normal balancing resistor. Adding the balancing resistor enhances performance at high temperatures, as shown by Figure 25.

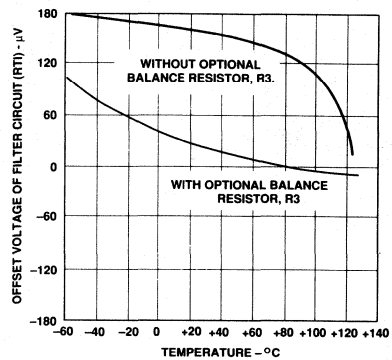


Figure 25. V_{OS} vs. Temperature Performance of the 1 Hz Filter

Table II. 1 Hz, 4-Pole, Low Pass Filter Recommended Component Values

Desired Low Pass Response	Section 1 Frequency (Hz)	Q	Section 2 Frequency (Hz)	Q	C1 (μF)	C2 (μF)	C3 (μF)	C4 (μF)
Bessel	1.43	0.522	1.60	0.806	0.116	0.107	0.160	0.0616
Butterworth	1.00	0.541	1.00	1.31	0.172	0.147	0.416	0.0609
0.1 dB Chebychev	0.648	0.619	0.948	2.18	0.304	0.198	0.733	0.0385
0.2 dB Chebychev	0.603	0.646	0.941	2.44	0.341	0.204	0.823	0.0347
0.5 dB Chebychev	0.540	0.705	0.932	2.94	0.416	0.209	1.00	0.0290
1.0 dB Chebychev	0.492	0.785	0.925	3.56	0.508	0.206	1.23	0.0242

NOTE
Specified Values are for a −3 dB point of 1.0 Hz. For other frequencies simply scale capacitors C1 through C4 directly; i.e.: for 3 Hz Bessel response, C1 = 0.0387 μF, C2 = 0.0357μF, C3 = 0.0533 μF, C4 = 0.0205 μF.

ANALOG DEVICES

Ultralow Drift Op Amp

AD707

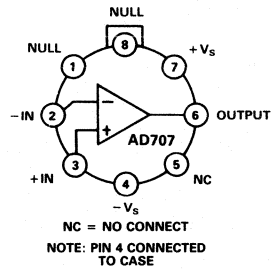
FEATURES

Very High DC Precision
15 μV max Offset Voltage
0.1 μV/°C max Offset Voltage Drift
0.35 μV p–p max Voltage Noise (0.1 Hz to 10 Hz)
8 V/μV min Open-Loop Gain
130 dB min CMRR
120 dB min PSRR
1 nA max Input Bias Current

AC Performance
0.3 V/μs Slew Rate
0.9 MHz Closed-Loop Bandwidth
Dual Version: AD708
Available in Tape and Reel in Accordance with EIA-481A Standard

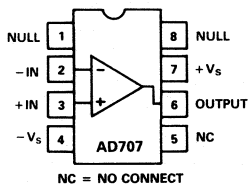
CONNECTION DIAGRAMS

TO-99 (H) Package



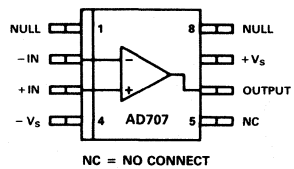
NC = NO CONNECT
NOTE: PIN 4 CONNECTED TO CASE

Plastic (N) and Cerdip (Q) Packages



NC = NO CONNECT

SOIC (R) Package



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD707 is a low cost, high precision op amp with state-of-the-art performance that makes it ideal for a wide range of precision applications. The offset voltage spec of less than 15 μV is the best available in a bipolar op amp, and maximum input offset current is 1.0 nA. The top grade is the first bipolar monolithic op amp to offer a maximum offset voltage drift of 0.1 μV/°C, and offset current drift and input bias current drift are both specified at 25 pA/°C maximum.

The AD707's open-loop gain is 8 V/μV minimum over the full ±10 V output range when driving a 1 kΩ load. Maximum input voltage noise is 350 nV p–p (0.1 Hz to 10 Hz). CMRR and PSRR are 130 dB and 120 dB minimum, respectively.

The AD707 is available in versions specified over commercial, industrial and military temperature ranges. It is offered in 8-pin plastic mini-DIP, small outline (SOIC), hermetic cerdip and hermetic TO-99 metal can packages. Chips, MIL-STD-883B, Rev. C, and tape & reel parts are also available.

APPLICATION HIGHLIGHTS

1. The AD707's 13 V/μV typical open-loop gain and 140 dB typical common-mode rejection ratio make it ideal for precision instrumentation applications.
2. The precision of the AD707 makes tighter error budgets possible at a lower cost.
3. The low offset voltage drift and low noise of the AD707 allow the designer to amplify very small signals without sacrificing overall system performance.
4. The AD707 can be used where chopper amplifiers are required, but without the inherent noise and application problems.
5. The AD707 is an improved pin-for-pin replacement for the LT1001.

AD707—SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

	Conditions	AD707J/A Min	AD707J/A Typ	AD707J/A Max	AD707K/B/S Min	AD707K/B/S Typ	AD707K/B/S Max	AD707C/T Min	AD707C/T Typ	AD707C/T Max	Units
INPUT OFFSET VOLTAGE											
Initial			30	**90**		10	**25**		5	**15**	μV
vs. Temperature			0.3	1.0		0.1	**0.3**		0.03	**0.1**	μ V/°C
	T_{min} to T_{max}		50	100		15	**45**		7/8/8	**25**	μV
Long-Term Stability			0.3			0.3			0.2		μV/month
Adjustment Range	R2 = 20 kΩ (Figure 19)		±4			±4			±4		mV
INPUT BIAS CURRENT			1.0	**2.5**		0.5	**1.5**		0.5	**1.0**	nA
	T_{min} to T_{max}		2.0	4.0		1.5	**3.0**		1.0	**2.0**	nA
Average Drift			15	40		15	25/25/35		10	25	pA/°C
OFFSET CURRENT	V_{CM} = 0 V		0.5	**2.0**		0.3	**1.5**		0.1	**1.0**	nA
	T_{min} to T_{max}		2.0	4.0		1.0	**2.0**		0.2	**1.5**	nA
Average Drift			2	40		1	25/25/35		1	25	pA/°C
INPUT VOLTAGE NOISE	0.1 to 10 Hz		0.23	0.6		0.23	0.6		0.23	**0.35**	μV p–p
	f = 10 Hz		10.3	15		10.3	14		10.3	13	nV/√Hz
	f = 100 Hz		10.0	13.0		10.0	12		10.0	11.0	nV/√Hz
	f = 1 kHz		9.6	11.0		9.6	11.0		9.6	11.0	nV/√Hz
INPUT CURRENT NOISE	0.1 Hz to 10 Hz		14	35		14	30		14	**30**	pA p–p
	f = 10 Hz		0.32	0.9		0.32	0.8		0.32	0.8	pA/√Hz
	f = 100 Hz		0.14	0.27		0.14	0.23		0.14	0.23	pA/√Hz
	f = 1 kHz		0.12	0.18		0.12	0.17		0.12	0.17	pA/√Hz
COMMON-MODE											
REJECTION RATIO	V_{CM} = ±13 V	**120**	140		**130**	140		**130**	140		dB
	T_{min} to T_{max}	120	140		**130**	140		**130**	140		dB
OPEN-LOOP GAIN	V_O = ±10 V										
	R_{LOAD}≥2 kΩ	**3**	13		**5**	13		**8**	13		V/μV
	T_{min} to T_{max}	3	13		**5**	13		**8**	13		V/μV
	R_{LOAD}≥1 kΩ	**3**	13		**5**	13		**8**	13		V/μV
POWER SUPPLY											
REJECTION RATIO	V_S = ±3 V to ±18 V	**110**	130		**115**	130		**120**	130		dB
	T_{min} to T_{max}	110	130		**115**	130		**120**	130		dB
FREQUENCY RESPONSE											
Closed-Loop Bandwidth			0.5	0.9		0.5	0.9		0.5	0.9	MHz
Slew Rate			0.15	0.3		0.15	0.3		0.15	0.3	V/μs
INPUT RESISTANCE											
Differential			24	100		45	200		60	200	MΩ
Common Mode				200			300			400	GΩ
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD}≥10 kΩ	**13.5**	14		**13.5**	14		**13.5**	14		±V
	R_{LOAD}≥2 kΩ	**12.5**	13.0		**12.5**	13.0		**12.5**	13.0		±V
	R_{LOAD}≥1 kΩ	**12.0**	12.5		**12.0**	12.5		**12.0**	12.5		±V
	R_{LOAD}≥2 kΩ										
	T_{min} to T_{max}	12.0	13.0		**12.0**	13.0		**12.0**	13.0		±V
OPEN-LOOP OUTPUT											
RESISTANCE			60			60			60		Ω
POWER SUPPLY											
Current, Quiescent			2.5	**3**		2.5	**3**		2.5	**3**	mA
Power Consumption, No Load	V_S = ±15 V		75	**90**		75	**90**		75	**90**	mW
	V_S = ±3 V		7.5	**9.0**		7.5	**9.0**		7.5	**9.0**	mW
TEMPERATURE RANGE											
Operating, Rated Performance											
Commercial	0 to +70°C	AD707JN, AD707JR			AD707KN, AD707KR[1]						
Industrial	−40°C to +85°C	AD707AQ, AD707AH AD707AR			AD707BQ, AD707BH			AD707CQ, AD707CH			
Military	−55°C to +125°C				AD707SQ, AD707SH			AD707TQ, AD707TH			

	Conditions	AD707J/A Min	Typ	Max	AD707K/B/S Min	Typ	Max	AD707C/T Min	Typ	Max	Units
PACKAGE OPTIONS[2]											
Plastic (N-8)		AD707JN			AD707KN						
Cerdip (Q-8)		AD707AQ			AD707BQ/SQ, AD707SQ/883B			AD707CQ/TQ, AD707TQ/883B			
TO-99 (H-08A)		AD707AH			AD707BH/SH, AD707SH/883B			AD707CH/TH, AD707TH/883B			
SOIC (R-8)		AD707JR, AD707AR			AD707KR						
Tape and Reel		AD707JR-Reel, AD707AR-Reel			AD707KR-Reel						
Chips		AD707J-Chips			AD707S-Chips						

NOTES
[1]AD707KR devices are production tested at +25°C only. All T_{min} to T_{max} specifications are guaranteed but not 100% tested for this grade.
[2]For outline information see Package Information section.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.
Specifications subject to change without notice.

2

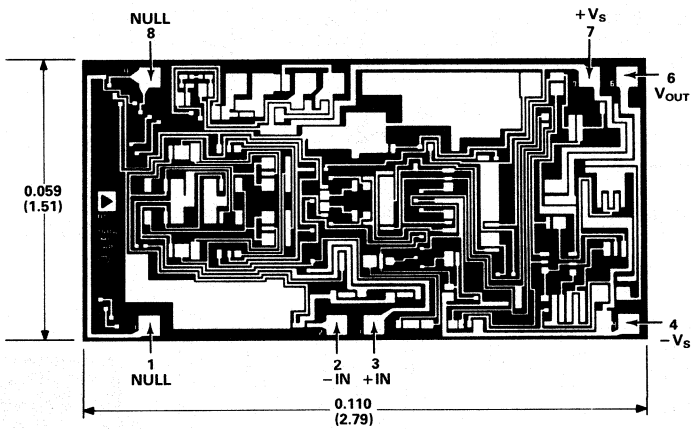
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±22 V
Internal Power Dissipation[2] . . . . . 500 mW
Input Voltage . . . . . $\pm V_S$
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range (Q, H) . . . . . −65°C to +150°C
Storage Temperature Range (N, R) . . . . . −65°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-pin plastic package: θ_{JA} = 165°C/Watt; 8-pin cerdip package: θ_{JA} = 110°C/Watt; 8-pin small outline package: θ_{JA} = 155°C/Watt; 8-pin header package: θ_{JA} = 200°C/Watt.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



AD707—Typical Characteristics

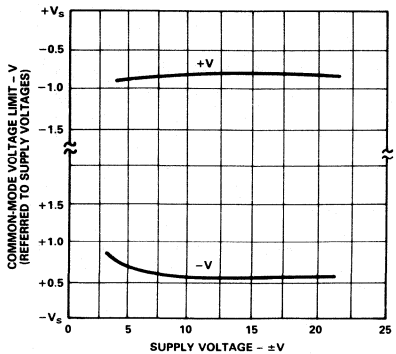


Figure 1. Input Common-Mode Range vs. Supply Voltage

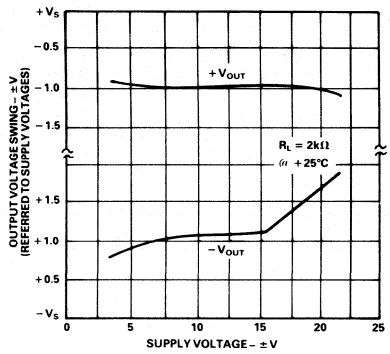


Figure 2. Output Voltage Swing vs. Supply Voltage

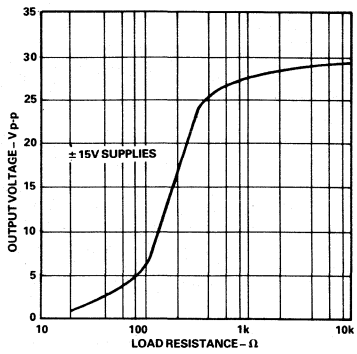


Figure 3. Output Voltage Swing vs. Load Resistance

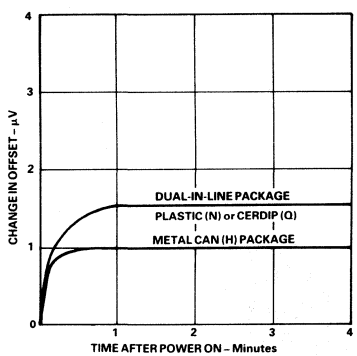


Figure 4. Offset Voltage Warm-Up Drift

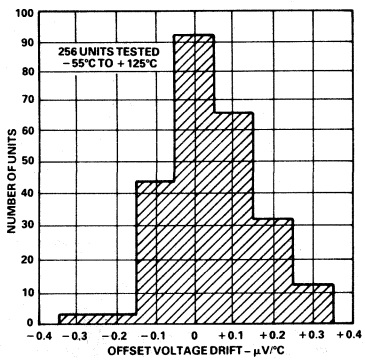


Figure 5. Typical Distribution of Offset Voltage Drift

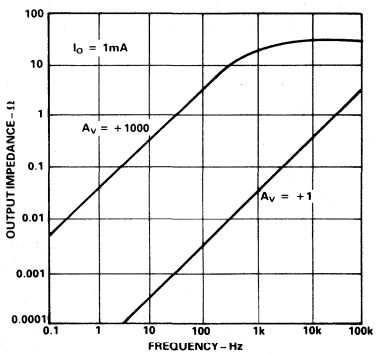


Figure 6. Output Impedance vs. Frequency

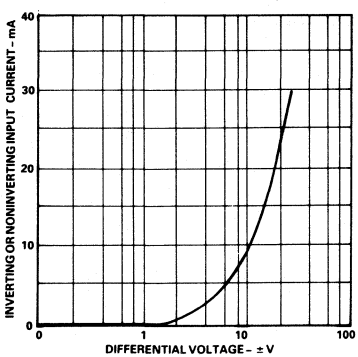


Figure 7. Input Current vs. Differential Input Voltage

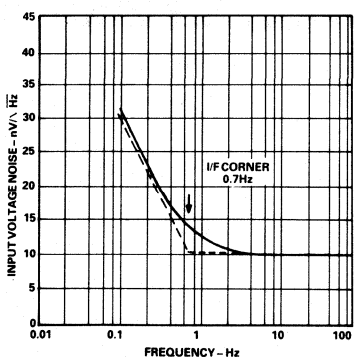


Figure 8. Input Noise Spectral Density

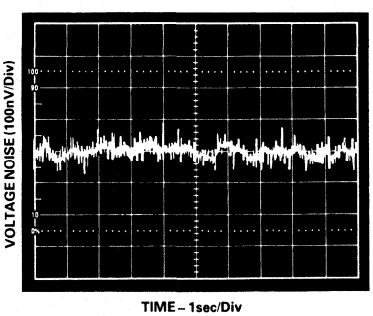


Figure 9. 0.1 Hz to 10 Hz Voltage Noise

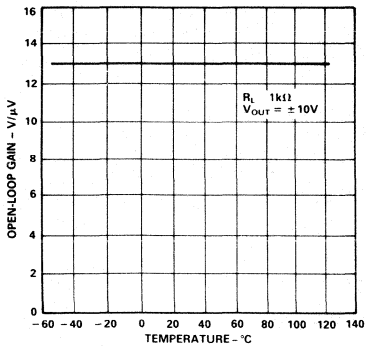


Figure 10. Open-Loop Gain vs. Temperature

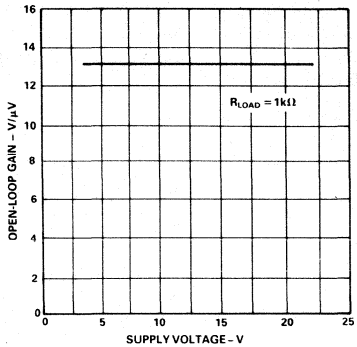


Figure 11. Open-Loop Gain vs. Supply Voltage

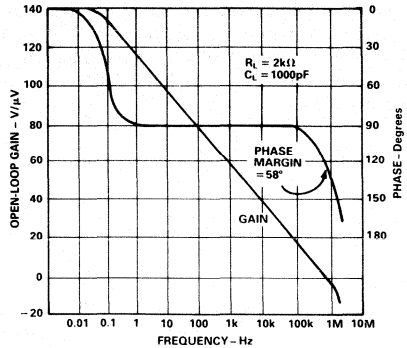


Figure 12. Open-Loop Gain and Phase vs. Frequency

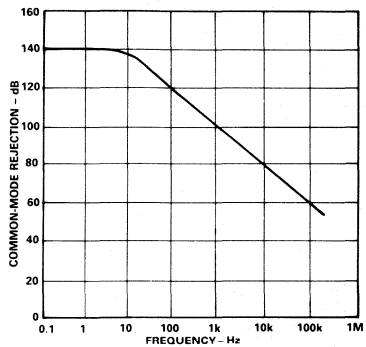


Figure 13. Common-Mode Rejection vs. Frequency

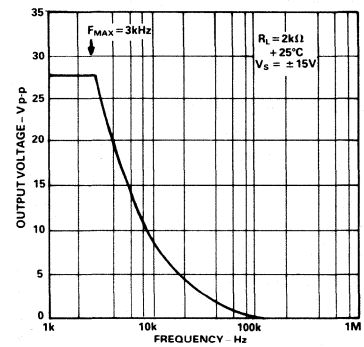


Figure 14. Large Signal Frequency Response

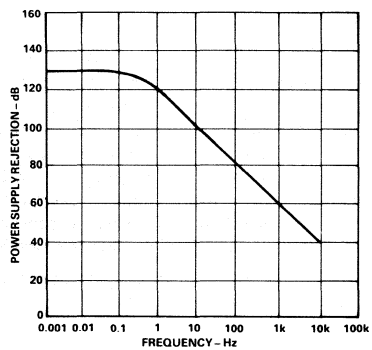


Figure 15. Power Supply Rejection vs. Frequency

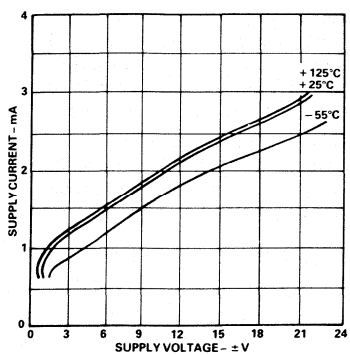


Figure 16. Supply Current vs. Supply Voltage

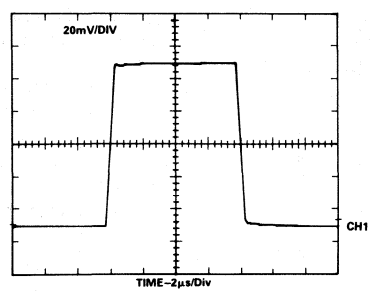


Figure 17. Small Signal Transient Response;
A_V = +1, R_L = 2 kΩ, C_L = 50 pF

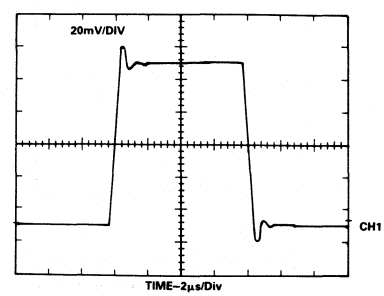


Figure 18. Small Signal Transient Response;
A_V = +1, R_L = 2 kΩ, C_L = 1000 pF

OFFSET NULLING

The input offset voltage of the AD707 is the lowest available in a bipolar op amp, but if additional nulling is required, the circuit shown in Figure 19 offers a null range of 200 μV. For wider null capability, omit R1 and substitute a 20 kΩ potentiometer for R2.

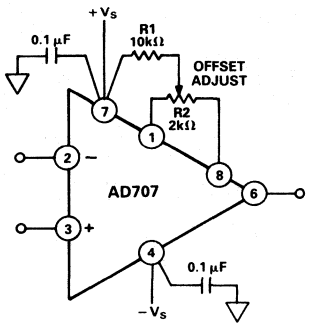


Figure 19. External Offset Nulling and Power Supply Bypassing

GAIN LINEARITY INTO A 1 kΩ LOAD

The gain and gain linearity of the AD707 are the highest available among monolithic bipolar amplifiers. Unlike other dc precision amplifiers, the AD707 shows no degradation in gain or gain linearity when driving loads in excess of 1 kΩ over a ±10 V output swing. This means high gain accuracy is assured over the output range. Figure 20 shows the gain of the AD707, AD OP-07, and the OP-77 amplifiers when driving a 1 kΩ load.

The AD707 will drive 10 mA of output current with no significant effect on its gain or linearity.

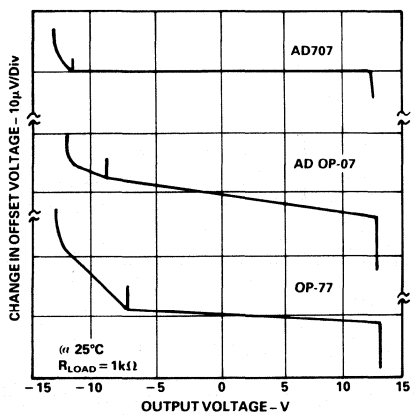


Figure 20. Gain Linearity of the AD707 vs. Other DC Precision Op Amps

OPERATION WITH A GAIN OF 100

Demonstrating the outstanding dc precision of the AD707 in practical applications, Table I shows an error budget calculation for the gain of −100 configuration shown in Figure 21.

Table I. Error Budget

Error Source	Maximum Error Contribution A_V = 100 (C Grade) (Full Scale: V_{OUT} = 10 V, V_{IN} = 100 mV)	
V_{OS}	15 μV/100 mV	= 150 ppm
I_{OS}	(100 Ω)(1 nA)/100 mV	= 1 ppm
Gain (2 kΩ Load)	(100 V/8 × 10^6)100 mV	= 13 ppm
Noise	0.35 μV/100 mV	= 4 ppm
V_{OS} Drift	(0.1 V/°C)/100 mV	= 1 ppm/°C
		= 168 ppm
		+1 ppm/°C

Total Unadjusted Error
@ +25°C = 168 ppm>12 Bits
@ −55°C to +125°C = 268 ppm>11 Bits
With Offset Calibrated Out
@ +25°C = 17 ppm>15 Bits
@ −55°C to +125°C = 117 ppm>13 Bits

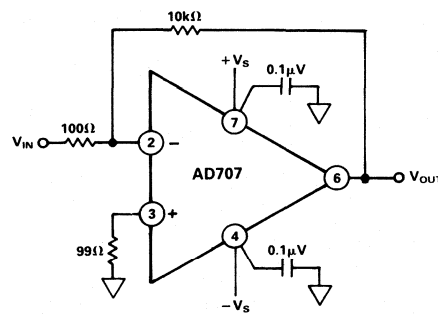


Figure 21. Gain of −100 Configuration

Although the initial offset voltage of the AD707 is very low, it is nonetheless the major contributor to system error. In cases requiring additional accuracy, the circuit shown in Figure 19 can be used to null out the initial offset voltage. This method will also cancel the effects of input offset current error. With the offsets nulled, the AD707C will add less than 17 ppm of error.

This error budget assumes no error in the resistor ratio and no errors from power supply variation (the 120 dB minimum PSRR of the AD707C makes this a good assumption). The external resistors can cause gain error from mismatch and drift over temperature.

18-BIT SETTLING TIME

Figure 22 shows the AD707 settling to within 80 μV of its final value for a 20 V output step in less than 100 μs (in the test configuration shown in Figure 23). To achieve settling to 18 bits, any amplifier specified to have a gain of 4 V/μV would appear to be good enough, however, this is not the case. In order to truly achieve 18-bit accuracy, the gain linearity must be better than 4 ppm.

The gain nonlinearity of the AD707 does not contribute to the error, and the gain itself only contributes 0.1 ppm. The gain error, along with the V_{OS} and V_{OS} drift errors do not comprise 1 LSB of error in a 18-bit system over the military temperature range. If calibration is used to null offset errors, the AD707 resolves up to 20 bits at +25°C.

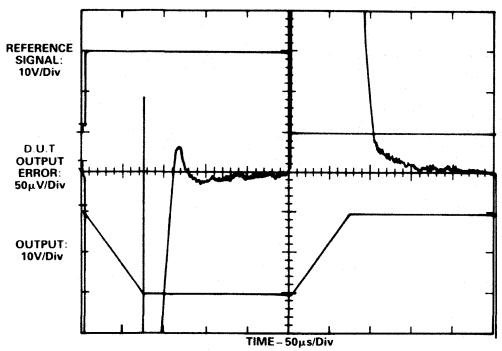


Figure 22. 18-Bit Settling

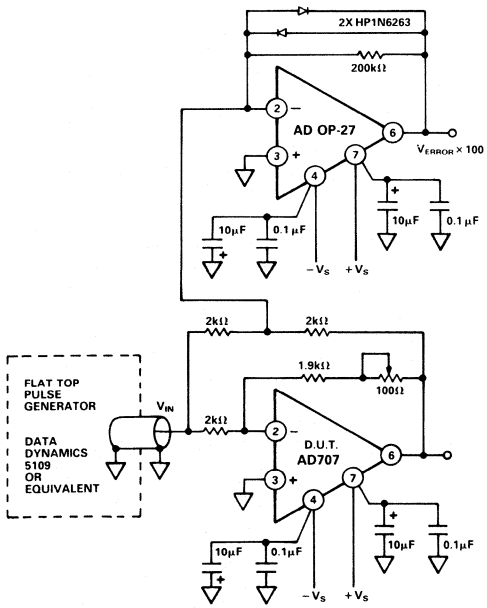


Figure 23. Op Amp Settling Time Test Circuit

140 dB CMRR INSTRUMENTATION AMPLIFIER

The extremely tight dc specifications of the AD707 enable the designer to build very high performance, high gain instrumentation amplifiers without having to select matched op amps for the crucial first stage. For the second stage, the lowest grade AD707 is ideally suited. The CMRR is typically the same as the high grade parts, but does not exact a premium for drift performance (which is less critical in the second stage). Figure 24 shows an example of the classic instrumentation amp. Figure 25 shows that the circuit has at least 140 dB of common-mode rejection for a ±10 V common-mode input at a gain of 1001 (R_G = 20 Ω).

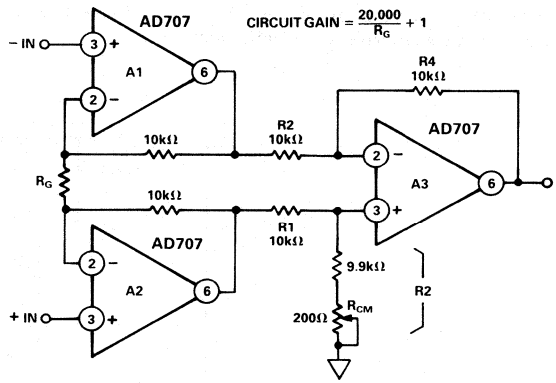


Figure 24. A 3 Op Amp Instrumentation Amplifier

High CMRR is obtained by first adjusting R_{CM} until the output does not change as the input is swept through the full common-mode range. The value of R_G should then be selected to achieve the desired gain. Matched resistors should be used for the output stage so that R_{CM} is as small as possible. The smaller the value of R_{CM}, the lower the noise introduced by potentiometer wiper vibrations. To maintain the CMRR at 140 dB over a 20°C range, the resistor ratios in the output stage, R1/R2 and R3/R4, must track each other better than 10 ppm/°C.

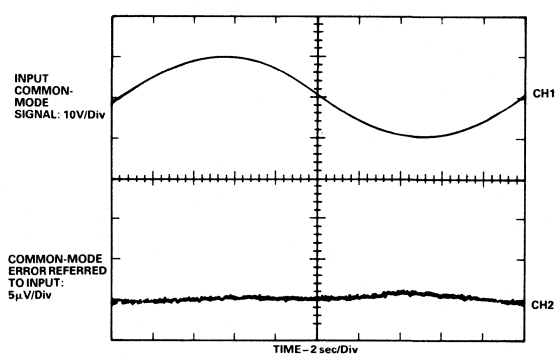


Figure 25. Instrumentation Amplifier Common-Mode Rejection

PRECISION CURRENT TRANSMITTER

The AD707's excellent dc performance, especially the low offset voltage, low offset voltage drift and high CMRR, makes it possible to make a high precision voltage-controlled current transmitter using a variation of the Howland Current Source circuit (Figure 26). This circuit provides a bidirectional load current which is derived from a differential input voltage.

The performance and accuracy of this circuit will depend almost entirely on the tolerance and selection of the resistors. The scale resistor (R_{SCALE}) and the four feedback resistors directly affect the accuracy of the load current and should be chosen carefully or trimmed.

As an example of the accuracy achievable, assume I_L must be 10 mA, and the available V_{IN} is only 10 mV.

R_{SCALE} = 10 mV/10 mA = 1 Ω

I_{ERROR} due to the AD707C:

Maximum I_{ERROR} = $2(V_{OS})/R_{SCALE} + 2(V_{OS}$ Drift$)/R_{SCALE} + I_{OS}$ (100 k/R_{SCALE})

= 2 (15 μV)/1 Ω + 2 (0.1 μV/°C)/1 Ω + 1 nA (100 k)/1 Ω (1.5 nA @ 125°C)

= 30 μA + 0.2 μA/°C + 100 μA (150 μA @ 125°C)

= 130 μA/10 mA = 1.3% @ 25°C

= 120 μA/10 mA = 2.00.25% @ 125°C

Low drift, high accuracy resistors are required to achieve high precision.

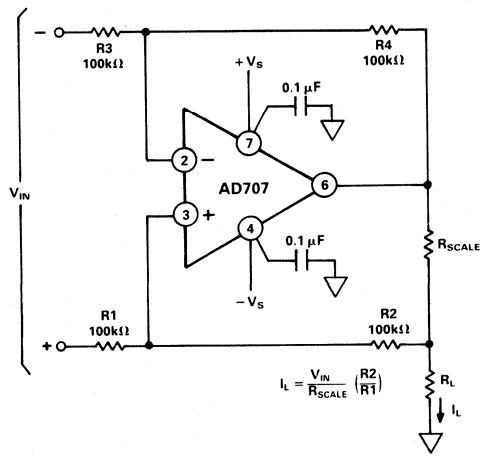


Figure 26. Precision Current Source/Sink

ANALOG DEVICES

Ultralow Offset Voltage Dual Op Amp

AD708

FEATURES

Very High dc Precision
- **30μV max Offset Voltage**
- **0.3μV/°C max Offset Voltage Drift**
- **0.35μV p-p max Voltage Noise (0.1 to 10Hz)**
- **5 Million V/V min Open Loop Gain**
- **130dB min CMRR**
- **120dB min PSRR**

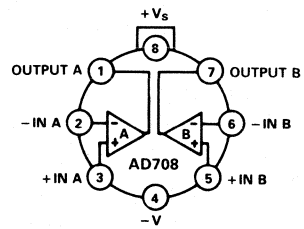
Matching Characteristics
- **30μV max Offset Voltage Match**
- **0.3μV/°C max Offset Voltage Drift Match**
- **130dB min CMRR Match**

Single Version: AD707

Available in 8-Pin Plastic Mini-DIP, Hermetic Cerdip and TO-99 Metal Can Packages. Chips and /883B Parts Available.

CONNECTION DIAGRAMS

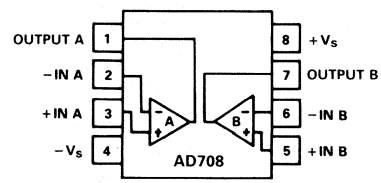
TO-99 (H) Package



TOP VIEW

NOTE: PIN 4 CONNECTED TO CASE

Plastic (N), and Cerdip (Q) Packages



TOP VIEW

PRODUCT DESCRIPTION

The AD708 is a very high precision, dual monolithic operational amplifier. Each amplifier individually offers excellent dc precision with the best available max offset voltage and offset voltage drift of any dual bipolar op amp. In addition, the matching specifications are the best available in any dual op amp.

The AD708 sets a new standard for dual precision op amps by providing 5V/μV min open loop gain and guaranteed max input voltage noise of 350nV p-p (0.1 to 10Hz). All dc specifications show excellent stability over temperature, with offset voltage drift typically 0.1μV/°C and input bias current drift of 25pA/°C max. Both CMRR (130dB min) and PSRR (120dB min) are an order of magnitude improved over any available single monolithic op amp except the AD707.

The AD708 is available in four performance grades. The AD708J is rated over the commercial temperature range of 0 to +70°C and is available in a plastic mini-DIP package. The AD708A and AD708B are rated over the industrial temperature range of −40°C to +85°C and are available in a cerdip and TO-99 package. The AD708S is rated over the military temperature range of −55°C to +125°C and is available in cerdip and TO-99 packages. Military versions are available processed to MIL-STD-883B, Rev. C.

APPLICATION HIGHLIGHTS

1. The combination of outstanding matching and individual specifications makes the AD708 ideal for constructing high gain, precision instrumentation amplifiers.
2. The low offset voltage drift and noise of the AD708 allows the designer to amplify very small signals without sacrificing overall system performance.
3. The AD708's 10V/μV typical open loop gain and 140dB common-mode rejection make it ideal for precision applications.
4. Unmounted dice are available for hybrid circuit applications.
5. The AD708 is an improved replacement for the LT1002.

AD708—SPECIFICATIONS (@+25°C and ±15V dc, unless otherwise noted)

Model	Conditions	AD708J/A Min	AD708J/A Typ	AD708J/A Max	AD708B Min	AD708B Typ	AD708B Max	AD708S Min	AD708S Typ	AD708S Max	Units
INPUT OFFSET VOLTAGE[1]			30	**100**		5	**50**		5	**30**	μV
	T_{min}–T_{max}		50	150		15	65		15	**50**	μV
Drift			0.3	1.0		0.1	0.4		0.1	**0.3**	μV/°C
Long Term Stability			0.3			0.3			0.3		μV/month
INPUT BIAS CURRENT			1.0	**2.5**		0.5	**1.0**		0.5	**1**	nA
	T_{min}–T_{max}		2.0	4.0		1.0	2.0		1.0	**4**	nA
Average Drift			15	40		10	25		10	30	pA/°C
OFFSET CURRENT	V_{CM}=0V		0.5	**2.0**		0.1	**1.0**		0.1	**1**	nA
	T_{min}–T_{max}		2.0	4.0		0.2	1.5		0.2	**1.5**	nA
Average Drift			2	60		1	25		1	25	pA/°C
MATCHING CHARACTERISTICS[2]											
Offset Voltage				**80**			**50**			**30**	μV
	T_{min}–T_{max}			150			75			**50**	μV
Offset Voltage Drift				1.0			0.4			**0.3**	μV/°C
Input Bias Current				**4.0**			**1.0**			**1.0**	nA
	T_{min}–T_{max}			5.0			2.0			**2.0**	nA
Common-Mode Rejection		**120**	140		**130**	140		**130**	140		dB
	T_{min}–T_{max}	110			130			**130**			dB
Power Supply Rejection		**110**			**120**			**120**			dB
	T_{min}–T_{max}	110			120			**120**			dB
Channel Separation		135			140			140			dB
INPUT VOLTAGE NOISE	0.1Hz to 10Hz		0.23	0.6		0.23	0.6		0.23	**0.35**	μV p-p
	f=10Hz		10.3	18		10.3	12		10.3	12	nV/$\sqrt{Hz}$
	f=100Hz		10.0	13.0		10.0	11.0		10.0	11	nV/$\sqrt{Hz}$
	f=1kHz		9.6	11.0		9.6	11.0		9.6	11	nV/$\sqrt{Hz}$
INPUT CURRENT NOISE	0.1Hz to 10Hz		14	35		14	35		14	35	pA p-p
	f=10Hz		0.32	0.9		0.32	0.8		0.32	0.8	pA/$\sqrt{Hz}$
	f=100Hz		0.14	0.27		0.14	0.23		0.14	0.23	pA/$\sqrt{Hz}$
	f=1kHz		0.12	0.18		0.12	0.17		0.12	0.17	pA/$\sqrt{Hz}$
COMMON-MODE REJECTION RATIO	V_{CM}=±13V	**120**	140		**130**	140		**130**	140		dB
	T_{min}–T_{max}	120	140		130	140		**130**	140		dB
OPEN LOOP GAIN	V_O=±10V										
	R_{LOAD}≥2kΩ	**3**	10		5	10		**4**	10		V/μV
	T_{min}–T_{max}	3	10		5	10		**4**	7		V/μV
POWER SUPPLY REJECTION RATIO	V_S=±3V to ±18V	**110**	130		**120**	130		**120**	130		dB
	T_{min}–T_{max}	110	130		120	130		**120**	130		dB
FREQUENCY RESPONSE											
Closed Loop Bandwidth			0.5	0.9		0.5	0.9		0.5	0.9	MHz
Slew Rate			0.15	0.3		0.15	0.3		0.15	0.3	V/μs
INPUT RESISTANCE											
Differential				60			200			200	MΩ
Common Mode				200			400			400	GΩ
OUTPUT VOLTAGE	R_{LOAD}≥10kΩ	**13.5**	14		**13.5**	14		**13.5**	14		±V
	R_{LOAD}≥2kΩ	**12.5**	13.0		**12.5**	13.0		**12.5**	13		±V
	R_{LOAD}≥1kΩ	**12.0**	12.5		**12.0**	12.5		**12.0**	12.5		±V
	R_{LOAD}≥2kΩ T_{min}–T_{max}	12.0	13.0		12.0	13.0		**12.0**	13		±V
OPEN LOOP OUTPUT RESISTANCE			60			60			60		Ω

Model	Conditions	AD708J/A Min	AD708J/A Typ	AD708J/A Max	AD708B Min	AD708B Typ	AD708B Max	AD708S Min	AD708S Typ	AD708S Max	Units
POWER SUPPLY											
Current, Quiescent			4.5	5.5		4.5	5.5		4.5	5.5	mA
Power Consumption	$V_S = \pm 15V$										
	No Load		135	**165**		135	**165**		135	**165**	mW
	$V_S = \pm 3V$		12	**18**		12	**18**		12	**18**	mW
Operating Range		±3		±18	±3		±18	±3		±18	V

NOTES
[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C
[2]Matching is defined as the difference between parameters of the two amplifiers.
All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.
Specifications subject to change without notice.

2

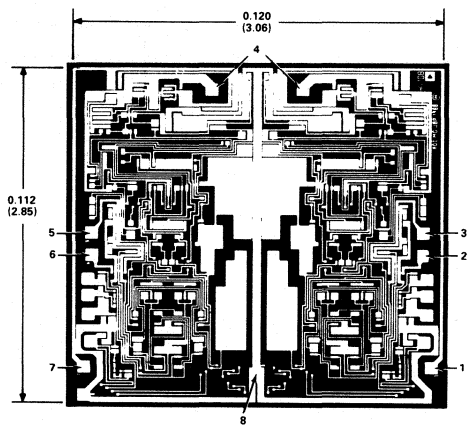
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±22V
Internal Power Dissipation[2]
Input Voltage[3] . . . . . $\pm V_S$
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range (Q, H) . . . . . −65°C to +150°C
Storage Temperature Range (N) . . . . . −65°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Thermal Characteristics
8-Pin Plastic Package: θ_{JC} = 33°C/Watt, θ_{JA} = 100°C/Watt
8-Pin Cerdip Package: θ_{JC} = 30°C/Watt, θ_{JA} = 110°C/Watt
8-Pin Metal Can Package: θ_{JC} = 65°C/Watt, θ_{JA} = 150°C/Watt
[3]For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD708JN	0°C to +70°C	8-Pin Plastic DIP	N-8
AD708AQ	−40°C to +85°C	8-Pin Cerdip	Q-8
AD708BQ	−40°C to +85°C	8-Pin Cerdip	Q-8
AD708SQ	−55°C to +125°C	8-Pin Cerdip	Q-8
AD708AH	−40°C to +85°C	8-Pin Header	H-08A
AD708BH	−40°C to +85°C	8-Pin Header	H-08A
AD708SH	−55°C to +125°C	8-Pin Header	H-08A
AD708SH/883B	−55°C to +125°C	8-Pin Header	H-08A
AD708J Grade Chips	0°C to +70°C	Die	
AD708S Grade Chips	−55°C to +125°C	Die	

*N = Plastic DIP; Q = Cerdip; H = Hermetic Metal Can. For outline information see Package Information section.

AD708—Typical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise noted)

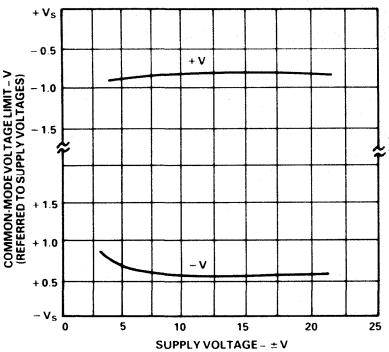


Figure 1. Input Common-Mode Range vs. Supply Voltage

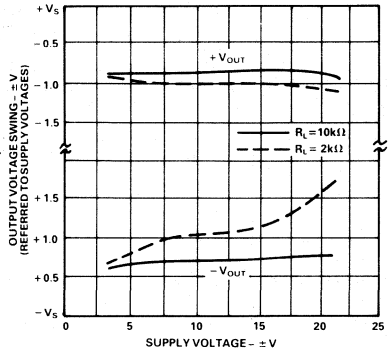


Figure 2. Output Voltage Swing vs. Supply Voltage

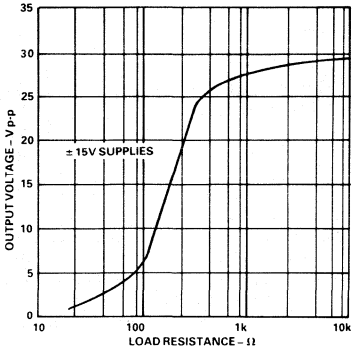


Figure 3. Output Voltage Swing vs. Load Resistance

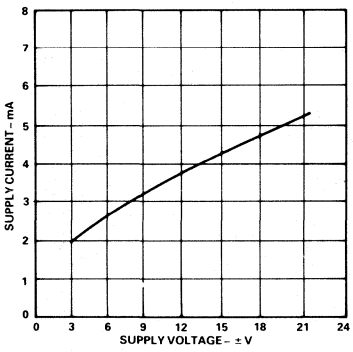


Figure 4. Supply Current vs. Supply Voltage

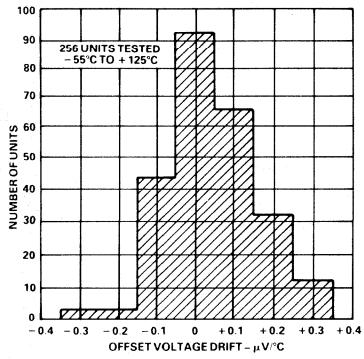


Figure 5. Typical Distribution of Offset Voltage Drift

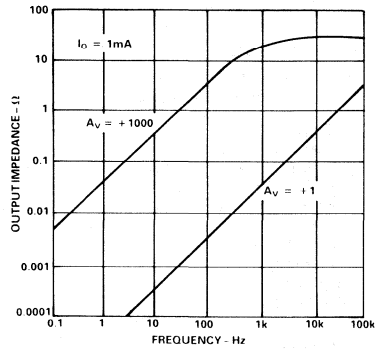


Figure 6. Output Impedance vs. Frequency

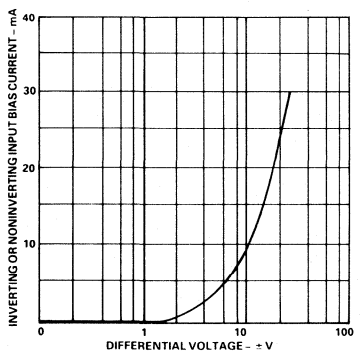


Figure 7. Input Bias Current vs. Differential Input Voltage

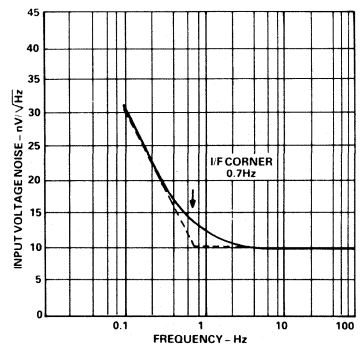


Figure 8. Input Noise Spectral Density

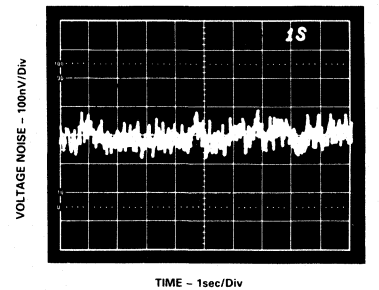


Figure 9. 0.1Hz to 10Hz Voltage Noise

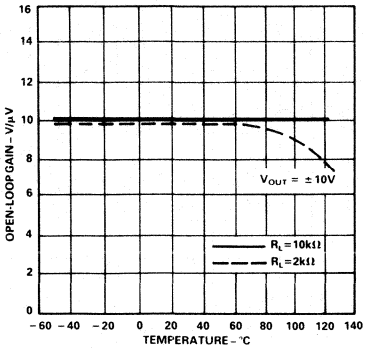


Figure 10. Open-Loop Gain vs. Temperature

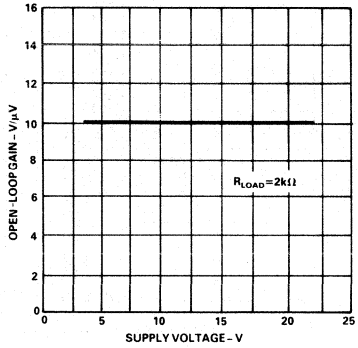


Figure 11. Open-Loop Gain vs. Supply Voltage

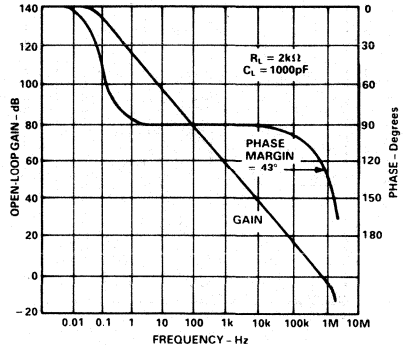


Figure 12. Open-Loop Gain and Phase vs. Frequency

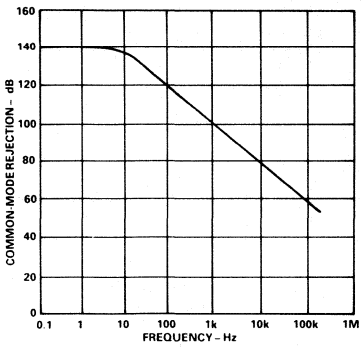


Figure 13. Common-Mode Rejection vs. Frequency

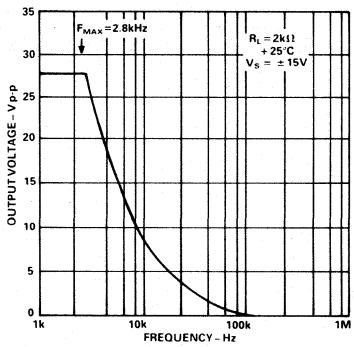


Figure 14. Large Signal Frequency Response

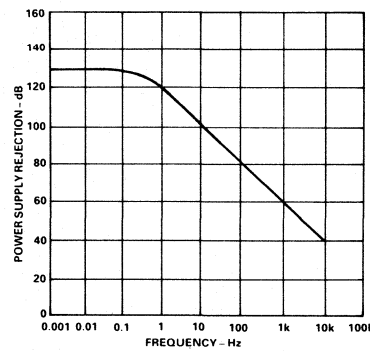


Figure 15. Power Supply Rejection vs. Frequency

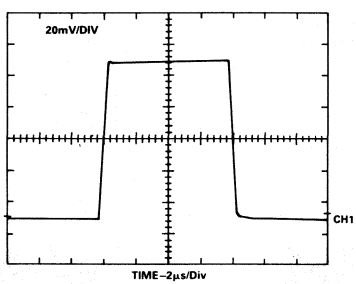


Figure 16. Small Signal Transient Response;
A_V = +1, R_L = 2kΩ, C_L = 50pF

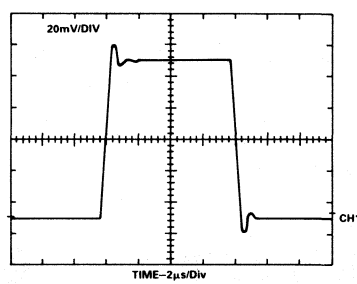


Figure 17. Small Signal Transient Response;
A_V = +1, R_L = 2kΩ, C_L = 1000pF

AD708—Matching Characteristics

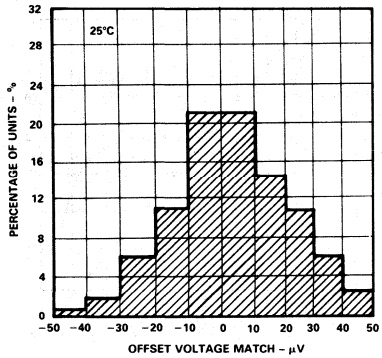


Figure 18. Typical Distribution of Offset Voltage Match

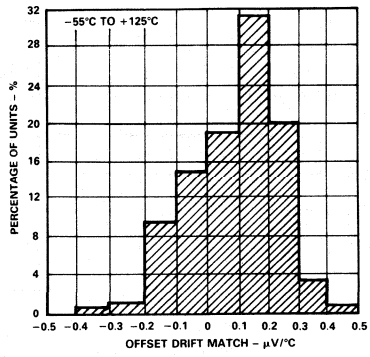


Figure 19. Typical Distribution of Offset Voltage Drift Match

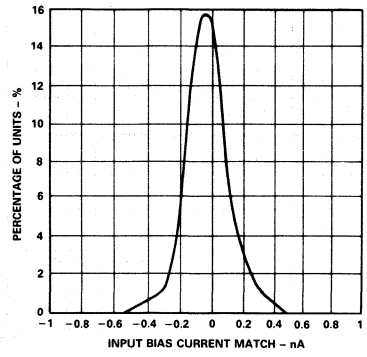


Figure 20. Typical Distribution of Input Bias Current Match

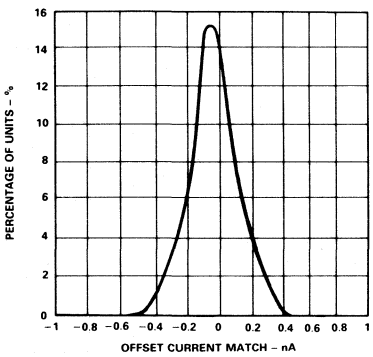


Figure 21. Typical Distribution of Input Offset Current Match

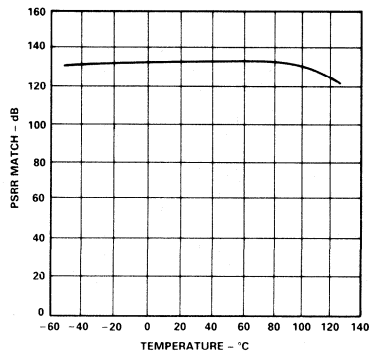


Figure 22. PSRR Match vs. Temperature

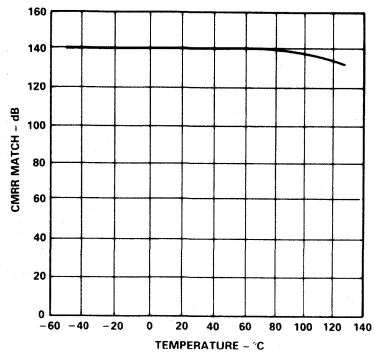


Figure 23. CMRR Match vs. Temperature

Crosstalk from Thermal Effects of Power Dissipation

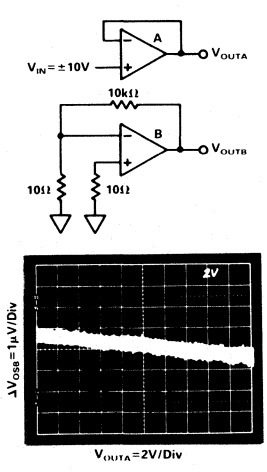


Figure 24. Crosstalk with No Load

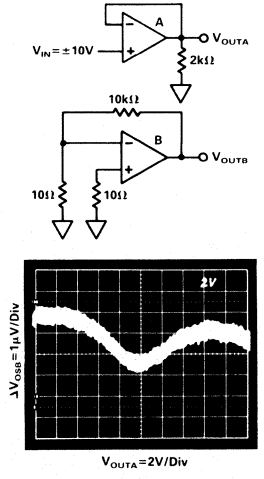


Figure 25. Crosstalk with 2kΩ Load

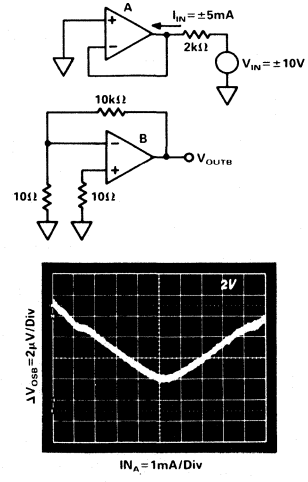


Figure 26. Crosstalk under Forced Source and Sink Conditions

CROSSTALK PERFORMANCE OF THE AD708

The AD708 exhibits very low crosstalk as shown in Figures 24, 25 and 26. Figure 24 shows the offset voltage induced in side B of the AD708 when side A's output is moving slowly (0.2Hz) from −10V to +10V under no load. This is the least stressful situation to the part since the overall power in the chip does not change; only the location of the power in the output devices changes. Figure 25 shows side B's input offset voltage change when side A is driving a 2kΩ load. Here the power is being changed in the chip with the maximum power change occurring at ±7.5V. Figure 26 shows crosstalk under the most severe conditions. Side A is connected as a follower with 0V input, and is now forced to sink and source ±5mA of output current (Power = (30V)(5mA) = 150mW). Even this large change in power causes only an 8μV (linear) change in side B's input offset voltage.

OPERATION WITH A GAIN OF −100

To show the outstanding dc precision of the AD708 in real application, Table I shows an error budget calculation for a gain of −100 configuration shown in Figure 27.

Table I.

Error Sources	Maximum Error Contribution $A_V = 100$ (S Grade) (Full Scale: $V_{OUT} = 10V$, $V_{IN} = 100mV$)	
V_{OS}	30μV/100mV	= 300ppm
I_{OS}	(100kΩ)(1nA)/10V	= 10ppm
Gain (2kΩ load)	(10V/(5*10⁶))/100mV	= 20ppm
Noise	0.35μV/100mV	= 4ppm
V_{OS} Drift	(0.3μV/°C)/100mV	= 3ppm/°C
		= 334ppm
		+ 3ppm/°C
Total Unadjusted Error	@ 25°C	= 334ppm>11 Bits
	−55°C to +125°C	= 634ppm>10 Bits
With Offset Calibrated Out	@ 25°C	= 34ppm>14 Bits
	−55°C to +125°C	= 334ppm>11 Bits

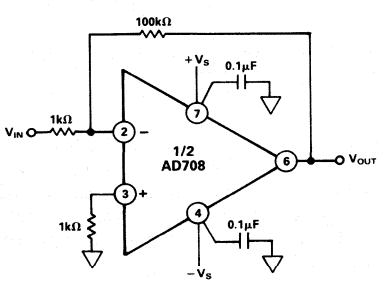


Figure 27. Gain of −100 Configuration

This error budget assumes no error in the resistor ratio and no error from power supply variation (the 120dB minimum PSRR of the AD708S makes this a good assumption). The external resistors can cause gain error from mismatch and drift over temperature.

High Precision Programmable Gain Amplifier

The three op amp programmable gain amplifier shown in Figure 28 takes advantage of the outstanding matching characteristics of

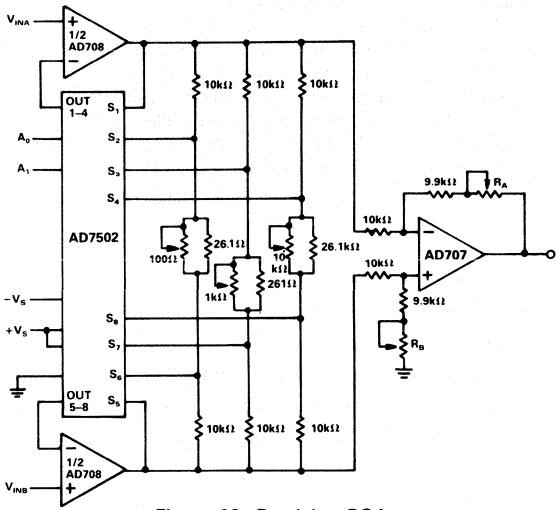


Figure 28. Precision PGA

the AD708 to achieve high dc precision. The gains of the circuit are controlled by the select lines, A0 and A1 of the AD7502 multiplexer, and are 1, 10, 100 and 1000 in this design.

The input stage attains very high dc precision due to the 30μV maximum offset voltage match of the AD708S and the 1nA maximum input bias current match. The accuracy is maintained over temperature because of the ultralow drift performance of the AD708. The output stage uses an AD707J and well matched resistors configured as a precision subtracter.

To achieve 0.1% gain accuracy, along with high common-mode rejection, the circuit should be trimmed as follows:

To maximize common-mode rejection:

1. Set the select lines for Gain = 1 and ground V_{INB}.
2. Apply a precision dc voltage to V_{INA} and trim R_A until $V_O = -V_{INA}$ to the required precision.
3. Next connect V_{INB} to V_{INA} and apply an input voltage equal to the full-scale common-mode expected.
4. Trim R_B until $V_O = 0V$.

To minimize gain errors:

1. Select Gain = 10 with the control lines and apply a differential input voltage.
2. Adjust the 100Ω potentiometer such that $V_O = 10V_{IN}$ (adjust V_{IN} magnitude as necessary).
3. Repeat for Gain = 100 and Gain = 1000, adjusting 1kΩ and 10kΩ potentiometers, respectively.

The design shown should allow for 0.1% gain accuracy and 0.1μV/V common-mode rejection when ±1% resistors and ±5% potentiometers are used.

BRIDGE SIGNAL CONDITIONER

The AD708 can be used in the circuit in Figure 29 to produce an accurate and inexpensive dynamic bridge conditioner. The low offset voltage match and low offset voltage drift match of the AD708 combine to achieve circuit performance better than all but the best instrumentation amplifiers. The AD708's out-

BRIDGE SIGNAL CONDITIONER

The AD708 can be used in the circuit in Figure 29 to produce an accurate and inexpensive dynamic bridge conditioner. The low offset voltage match and low offset voltage drift match of the AD708 combine to achieve circuit performance better than all but the best instrumentation amplifiers. The AD708's outstanding specs: open loop gain, input offset currents and low input bias currents, do not limit circuit accuracy.

As configured, the circuit only requires a gain resistor, R_G, of suitable accuracy and a stable, accurate voltage reference. The transfer function is:

$$V_O = V_{REF}\,[\Delta R/(R+\Delta R)][R_G/R]$$

and the only significant errors due to the AD708S are:

$$V_{OS}\text{out} = (V_{OS}\text{match})(2R_G/R) = 25\text{mV}$$

$$V_{OS}\text{out(T)} = (V_{OS}\text{drift})(2R_G/R) = 0.3\text{mV/°C}$$

To achieve high accuracy, the resistor R_G should be 0.1% or better and have a low drift coefficient.

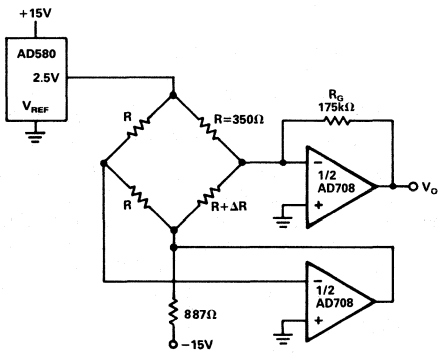


Figure 29. Bridge Signal Conditioning Circuit

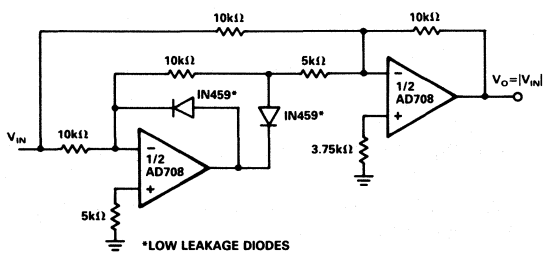


Figure 30. Precision Absolute Value Circuit

PRECISION ABSOLUTE VALUE CIRCUIT

The AD708 is ideally suited to the precision absolute value circuit shown in Figure 30. The low offset voltage match of the AD708 enables this circuit to accurately resolve the input signal. In addition, the tight offset voltage drift match maintains the resolution of the circuit over the full military temperature range. The AD708's high dc open loop gain and exceptional gain linearity allows the circuit to perform well at both large and small signal levels.

In this circuit, the only significant dc errors are due to the offset voltage of the two amplifiers, the input offset current match of the amplifiers, and the mismatch of the resistors. Errors associated with the AD708S contribute less than 0.001% error over −55°C to +125°C.

Maximum error at 25°C

$$\frac{30\mu V + (10k\Omega)(1nA)}{10V} = 40\mu V/10V = 4ppm \text{ Maximum}$$

error at +125°C or −55°C

$$\frac{50\mu V + (2nA)(10k\Omega)}{10V} = 7ppm\ @\ +125°C$$

Figure 31 shows V_{OUT} vs. V_{IN} for this circuit with a ±3mV input signal at 0.05Hz. Note that the circuit exhibits very low offset at the zero crossing. This circuit can also produce $V_{OUT} = -|V_{IN}|$ by reversing the polarity of the two diodes.

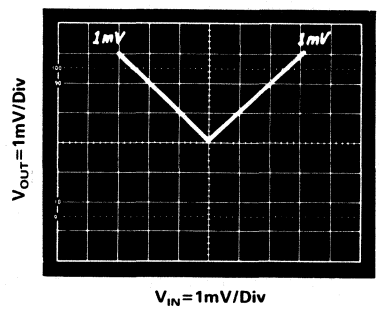


Figure 31. Absolute Value Circuit Performance (Input signal = 0.05Hz)

SELECTION OF PASSIVE COMPONENTS

To take full advantage of the high precision and low drift characteristics of the AD708, high quality passive components must be used. Discrete resistors and resistor networks with temperature coefficients of less than 10ppm/°C are available from Vishay, Caddock, PRP and others.

ANALOG DEVICES

Precision, Low Cost, High Speed BiFET Op Amp

AD711

FEATURES

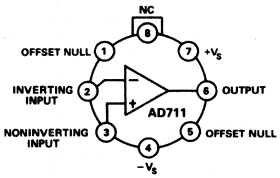
Enhanced Replacement for LF411 and TL081
AC PERFORMANCE:
- **Settles to ±0.01% in 1μs**
- **16V/μs min Slew Rate (AD711J)**
- **3MHz min Unity Gain Bandwidth (AD711J)**

DC PERFORMANCE:
- **0.25mV max Offset Voltage: (AD711C)**
- **3μV/°C max Drift: (AD711C)**
- **200V/mV min Open-Loop Gain (AD711K)**
- **4μV p–p max Noise, 0.1Hz to 10Hz (AD711C)**

Available in Plastic Mini-DIP, Plastic SO, Hermetic Cerdip, and Hermetic Metal Can Packages
MIL-STD-883B Parts Available
Available in Tape and Reel in Accordance with EIA-481A Standard
Surface Mount (SOIC)
Dual Version: AD712
Quad Version: AD713

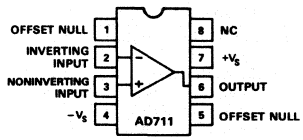
CONNECTION DIAGRAMS

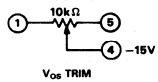
TO-99 (H) Package



NOTE: PIN 4 CONNECTED TO CASE
NC = NO CONNECT

Plastic Mini-DIP (N) Package
Plastic Small Outline (R) and Cerdip (Q) Package





PRODUCT DESCRIPTION

The AD711 is a high speed, precision monolithic operational amplifier offering high performance at very modest prices. Its very low offset voltage and offset voltage drift are the results of advanced laser wafer trimming technology. These performance benefits allow the user to easily upgrade existing designs that use older precision BiFETs and, in many cases, bipolar op amps.

The superior ac and dc performance of this op amp makes it suitable for active filter applications. With a slew rate of 16V/μs and a settling time of 1μs to ±0.01%, the AD711 is ideal as a buffer for 12-bit D/A and A/D Converters and as a high-speed integrator. The settling time is unmatched by any similar IC amplifier.

The combination of excellent noise performance and low input current also make the AD711 useful for photo diode preamps. Common-mode rejection of 88dB and open loop gain of 400V/mV ensure 12-bit performance even in high-speed unity gain buffer circuits.

The AD711 is pinned out in a standard op amp configuration and is available in seven performance grades. The AD711J and AD711K are rated over the commercial temperature range of 0 to +70°C. The AD711A, AD711B and AD711C are rated over the industrial temperature range of −40°C to +85°C. The AD711S and AD711T are rated over the military temperature range of −55°C to +125°C and are available processed to MIL-STD-883B, Rev. C.

Extended reliability PLUS screening is available, specified over the commercial and industrial temperature ranges. PLUS screening includes 168-hour burn-in, as well as other environmental and physical tests.

The AD711 is available in an 8-pin plastic mini-DIP, small outline, cerdip, TO-99 metal can or in chip form.

PRODUCT HIGHLIGHTS

1. The AD711 offers excellent overall performance at very competitive prices.
2. Analog Devices' advanced processing technology and with 100% testing guarantees a low input offset voltage (0.25mV max, C grade, 2mV max, J grade). Input offset voltage is specified in the warmed-up condition. Analog Devices' laser wafer drift trimming process reduces input offset voltage drifts to 3μV/°C max on the AD711C.
3. Along with precision dc performance, the AD711 offers excellent dynamic response. It settles to ±0.01% in 1μs and has a 100% tested minimum slew rate of 16V/μs. Thus this device is ideal for applications such as DAC and ADC buffers which require a combination of superior ac and dc performance.
4. The AD711 has a guaranteed and tested maximum voltage noise of 4μV p-p, 0.1 to 10Hz (AD711C).
5. Analog Devices' well-matched, ion-implanted JFETs ensure a guaranteed input bias current (at either input) of 25pA max (AD711C) and an input offset current of 10pA max (AD711C). Both input bias current and input offset current are guaranteed in the warmed-up condition.

AD711—SPECIFICATIONS (@ +25°C and V_S = ±15V dc, unless otherwise noted)

Model	AD711J/A/S			AD711K/B/T			AD711C			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
INPUT OFFSET VOLTAGE[1]										
Initial Offset		0.3	2/1/1		0.2	0.5		0.1	0.25	mV
T_{min} to T_{max}			3/2/2			1.0			0.45	mV
vs. Temp.		7	20/20/20		5	10		2	3	µV/°C
vs. Supply	76	95		80	100		86	110		dB
vs. Supply, T_{min} to T_{max}	76/76/76			80			86			dB
Long Term Offset Stability		15			15			15		µV/month
INPUT BIAS CURRENT[2]										
Either Input, V_{CM} = 0		15	50		15	50		15	25	pA
Either Input at T_{max}, V_{CM} = 0 (70°C/85°C/125°C)			1.1/3.2/51			1.1/3.2/51			1.6	nA
Either Input, V_{CM} = +10V		20	100		20	100		20	50	pA
Offset Current, V_{CM} = 0		10	25		5	25		5	10	pA
Offset Current at T_{max} (70°C/85°C/125°C)			0.57/1.6/26			0.57/1.6/26			0.65	nA
FREQUENCY RESPONSE										
Unity Gain, Small Signal	3.0	4		3.4	4		3.4	4		MHz
Full Power Response		200			200			200		kHz
Slew Rate, Unity Gain	16	20		18	20		18	20		V/µs
Settling Time to 0.01%[3]		1	1.2		1	1.2		1	1.2	µs
Total Harmonic Distortion f = 1kHz										
$R_L \geq 2k\Omega$, V_O = 3V RMS		0.0003			0.0003			0.0003		%
INPUT IMPEDANCE										
Differential		$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$		Ω‖pF
Common-Mode		$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$		Ω‖pF
INPUT VOLTAGE RANGE										
Differential[4]		±20			±20			±20		V
Common-Mode Voltage		+14.5, −11.5			+14.5, −11.5			+14.5, −11.5		
Over Max Operating Range[5]	$-V_S+4V$		$+V_S-2V$	$-V_S+4V$		$+V_S-2V$	$-V_S+4V$		$+V_S-2V$	V
Common-Mode Rejection Ratio										
V_{CM} = ±10V	76	88		80	88		86	94		dB
T_{min} to T_{max}	76/76/76	84		80	84		86	90		dB
V_{CM} = ±11V	70	84		76	84		76	90		dB
T_{min} to T_{max}	70/70/70	80		74	80		74	84		dB
INPUT VOLTAGE NOISE										
Voltage 0.1Hz to 10Hz		2			2			2	4.0	µV p-p
f = 10Hz		45			45			45		nV/√Hz
f = 100Hz		22			22			22		nV/√Hz
f = 1kHz		18			18			18		nV/√Hz
f = 10kHz		16			16			16		nV/√Hz
INPUT CURRENT NOISE										
f = 1kHz		0.01			0.01			0.01		pA/√Hz
OPEN LOOP GAIN[6]										
V_O = ±10V, $R_L \geq 2k\Omega$	150	400		200	400		200	400		V/mV
V_O = ±10V, $R_L \geq 2k\Omega$, T_{min} to T_{max}	100/100/100			100			100			V/mV
OUTPUT CHARACTERISTICS										
Voltage @ $R_L \geq 2k\Omega$	+13, −12.5	+13.9, −13.3		+13, −12.5	+13.9, −13.3		+13, −12.5	+13.9, −13.3		V
Voltage @ $R_L \geq 2k\Omega$, T_{min} to T_{max}	±12/±12/±12	+13.8, −13.1		±12	+13.8, −13.1		±12	+13.8, −13.1		V
Short-Circuit Current		25			25			25		mA
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating Range	±4.5		±18	±4.5		±18	±4.5		±18	V
Quiescent Current		2.5	3.4		2.5	3.0		2.5	2.8	mA
TEMPERATURE RANGE										
Operating, Rated Performance										
Commercial (0 to +70°C)		AD711J			AD711K					
Industrial (−40°C to +85°C)		AD711A			AD711B			AD711C		
Military (−55°C to +125°C)		AD711S			AD711T					
PACKAGE OPTIONS[7]										
Plastic (N-8)		AD711JN			AD711KN					
SOIC (R-8)		AD711JR			AD711KR					
Cerdip (Q-8)		AD711AQ, AD711SQ			AD711BQ, AD711TQ			AD711CQ		
TO-99 (H-08A)		AD711AH, AD711SH			AD711BH, AD711TH			AD711CH		
Tape and Reel		AD711JR-REEL			AD711KR-REEL					
Chips		AD711J Chips			AD711K Chips			AD711S Chips		
TRANSISTOR COUNT		30			30			30		

NOTES
[1]Input offset voltage specifications are guaranteed after 5 minutes of operation at $T_A = +25°C$.
[2]Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at $T_A = +25°C$. For higher temperature, the current doubles every 10°C.
[3]Refer to Figure 29.
[4]Defined as voltage between inputs, such that neither exceeds ±10V from ground.
[5]Typically exceeding −14.1V negative common-mode voltage on either input results in an output phase reversal.
[6]Open-Loop Gain is specified with V_{OS} both nulled and unnulled.
[7]H = Metal Can; N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.

Specifications subject to change without notice.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

2

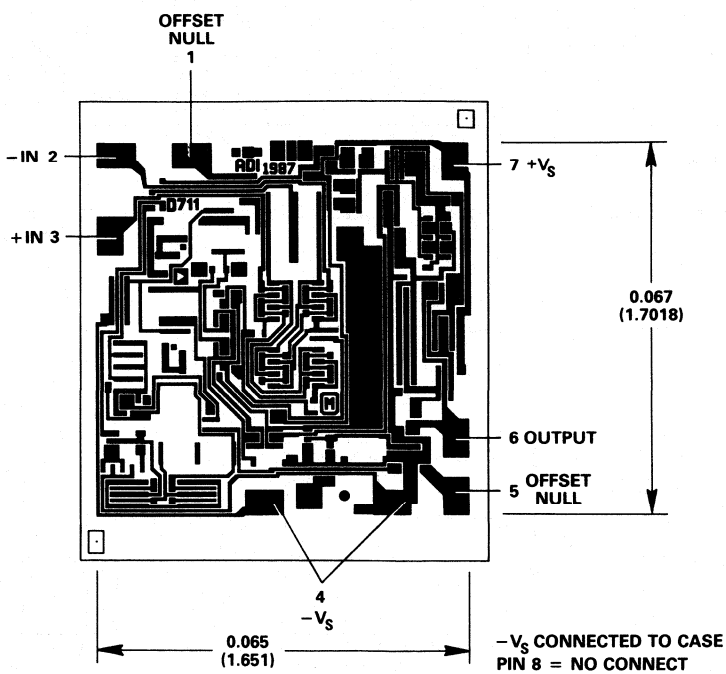
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18V
Internal Power Dissipation[2]	500mW
Input Voltage[3]	±18V
Output Short Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range (Q, H)	−65°C to +150°C
Storage Temperature Range (N)	−65°C to +125°C
Operating Temperature Range	
AD711J/K	0 to +70°C
AD711A/B/C	−40°C to +85°C
AD711S/T	−55°C to +125°C
Lead Temperature Range (Soldering 60 seconds)	300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Thermal Characteristics:
8-Pin Plastic Package: $\theta_{JC} = 33°C/W$; $\theta_{JA} = 100°C/W$
8-Pin Cerdip Package: $\theta_{JC} = 22°C/W$; $\theta_{JA} = 110°C/W$
8-Pin Metal Can Package: $\theta_{JC} = 65°C/W$; $\theta_{JA} = 150°C/W$
[3]For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.

METALLIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



AD711—Typical Characteristics

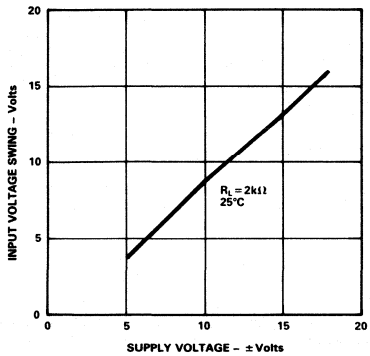


Figure 1. Input Voltage Swing vs. Supply Voltage

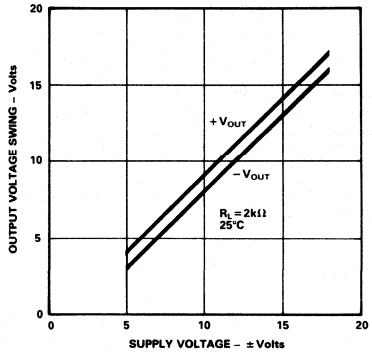


Figure 2. Output Voltage Swing vs. Supply Voltage

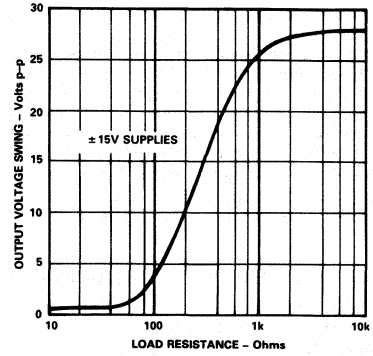


Figure 3. Output Voltage Swing vs. Load Resistance

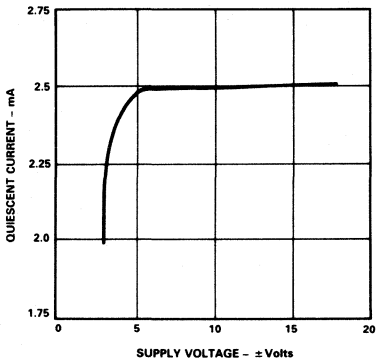


Figure 4. Quiescent Current vs. Supply Voltage

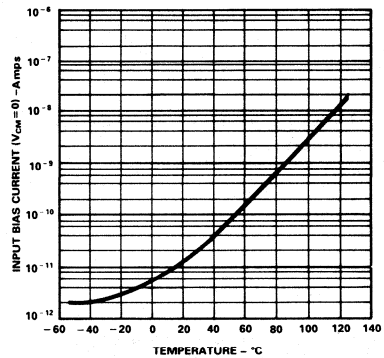


Figure 5. Input Bias Current vs. Temperature

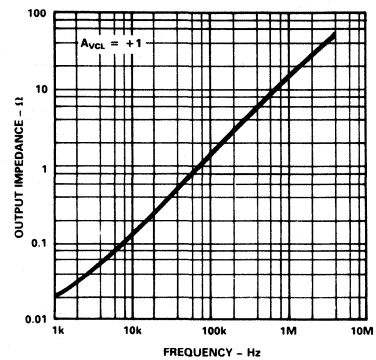


Figure 6. Output Impedance vs. Frequency

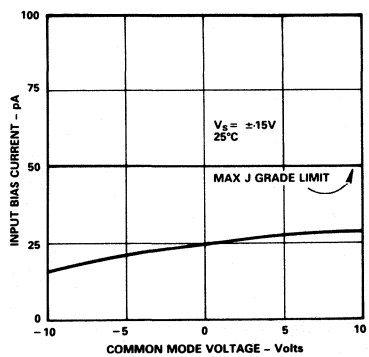


Figure 7. Input Bias Current vs. Common Mode Voltage

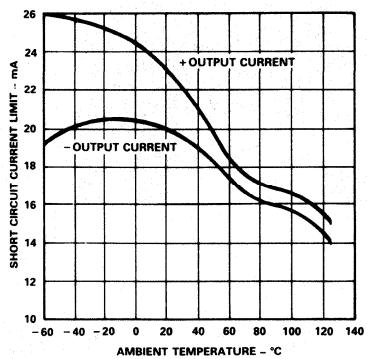


Figure 8. Short Circuit Current Limit vs. Temperature

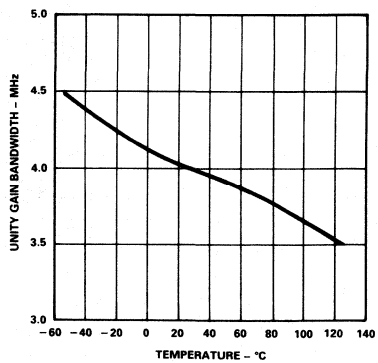


Figure 9. Unity Gain Bandwidth vs. Temperature

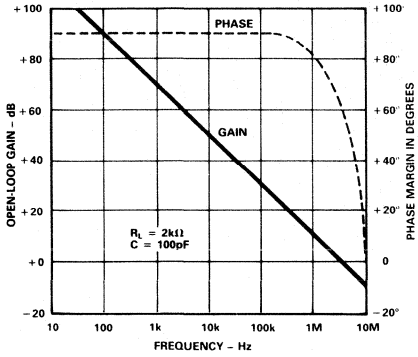


Figure 10. Open-Loop Gain and Phase Margin vs. Frequency

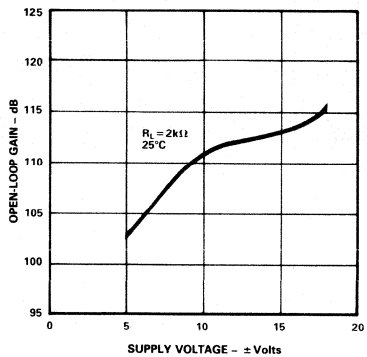


Figure 11. Open-Loop Gain vs. Supply Voltage

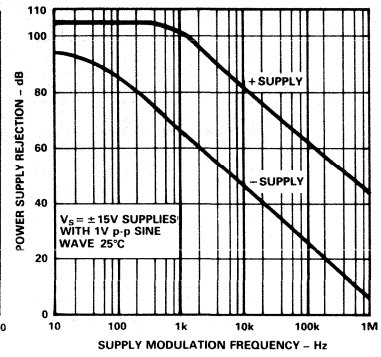


Figure 12. Power Supply Rejection vs. Frequency

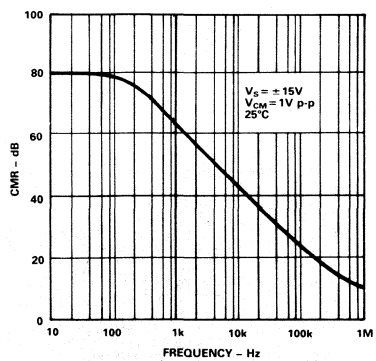


Figure 13. Common Mode Rejection vs. Frequency

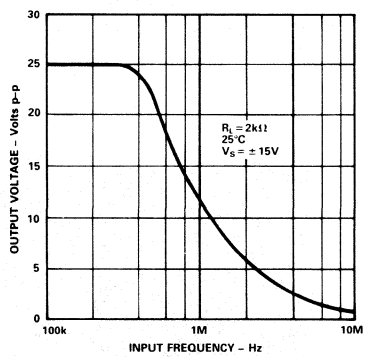


Figure 14. Large Signal Frequency Response

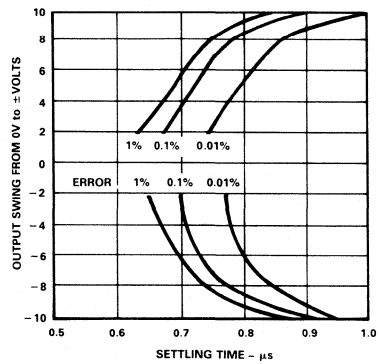


Figure 15. Output Swing and Error vs. Settling Time

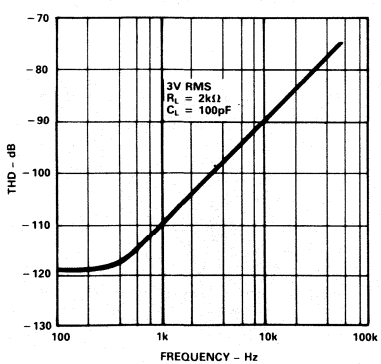


Figure 16. Total Harmonic Distortion vs. Frequency

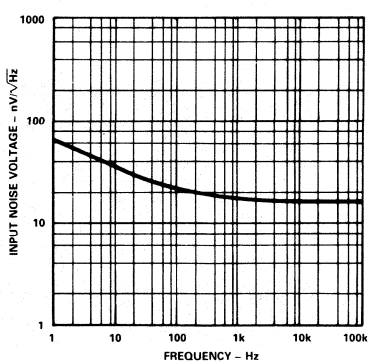


Figure 17. Input Noise Voltage Spectral Density

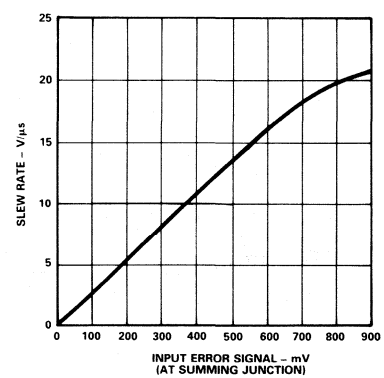


Figure 18. Slew Rate vs. Input Error Signal

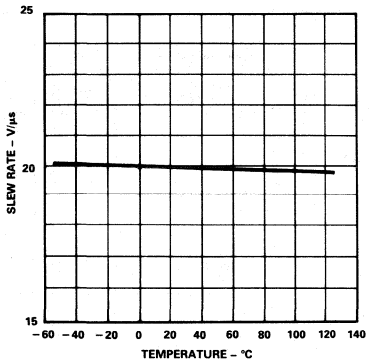


Figure 19. Slew Rate vs. Temperature

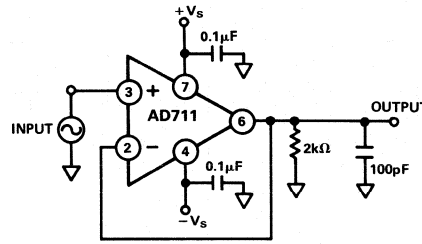


Figure 20. T.H.D. Test Circuit

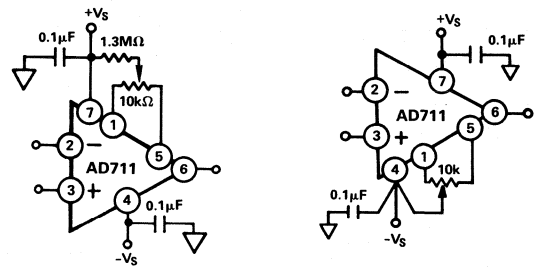


Figure 21. Offset Null Configurations

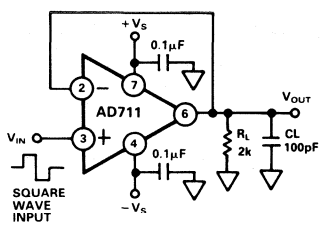


Figure 22a. Unity Gain Follower

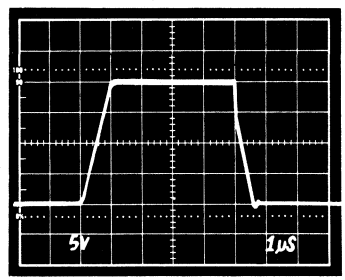


Figure 22b. Unity Gain Follower Pulse Response (Large Signal)

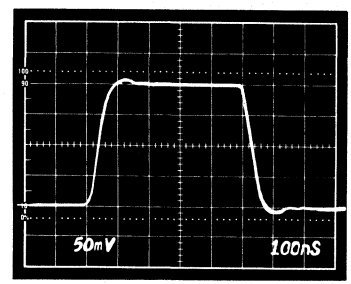


Figure 22c. Unity Gain Follower Pulse Response (Small Signal)

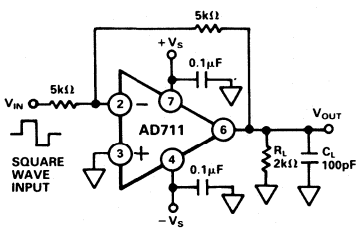


Figure 23a. Unity Gain Inverter

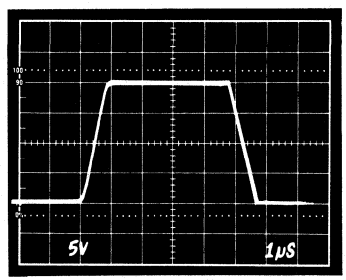


Figure 23b. Unity Gain Inverter Pulse Response (Large Signal)

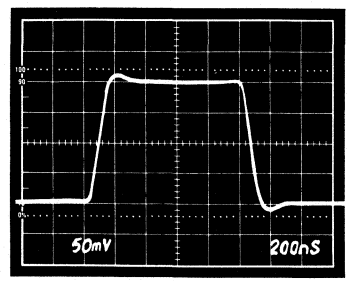


Figure 23c. Unity Gain Inverter Pulse Response (Small Signal)

OPTIMIZING SETTLING TIME

Most bipolar high-speed D/A converters have curent outputs; therefore, for most applications, an external op amp is required for current-to-voltage conversion. The settling time of the converter/op amp combination depends on the settling time of the DAC and output amplifier. A good approximation is:

$$t_s \text{ Total} = \sqrt{(t_s \text{ DAC})^2 + (t_s \text{ AMP})^2}$$

The settling time of an op amp DAC buffer will vary with the noise gain of the circuit, the DAC output capacitance, and with the amount of external compensation capacitance across the DAC output scaling resistor.

Settling time for a bipolar DAC is typically 100 to 500ns. Previously, conventional op amps have required much longer settling times than have typical state-of-the-art DACs; therefore, the amplifier settling time has been the major limitation to a high-speed voltage-output D-to-A function. The introduction of the AD711/712 family of op amps with their 1μs (to ±0.01% of final value) settling time now permits the full high-speed capabilities of most modern DACs to be realized.

In addition to a significant improvement in settling time, the low offset voltage, low offset voltage drift, and high open-loop gain of the AD711 family assures 12-bit accuracy over the full operating temperature range.

The excellent high-speed performance of the AD711 is shown in the oscilloscope photos of Figure 25. Measurements were taken using a low input capacitance amplifier connected directly to the summing junction of the AD711 – both photos show the worst case situation: a full-scale input transition. The DAC's 4kΩ [10kΩ‖8kΩ = 4.4kΩ] output impedance together with a 10kΩ feedback resistor produce an op amp noise gain of 3.25. The current output from the DAC produces a 10V step at the op amp output (0 to −10V Figure 25a, −10V to 0V Figure 25b.)

Therefore, with an ideal op amp, settling to ±1/2LSB (±0.01%) requires that 375μV or less appears at the summing junction. This means that the error between the input and output (that voltage which appears at the AD711 summing junction) must be less than 375μV. As shown in Figure 25, the total settling time for the AD711/AD565 combination is 1.2 microseconds.

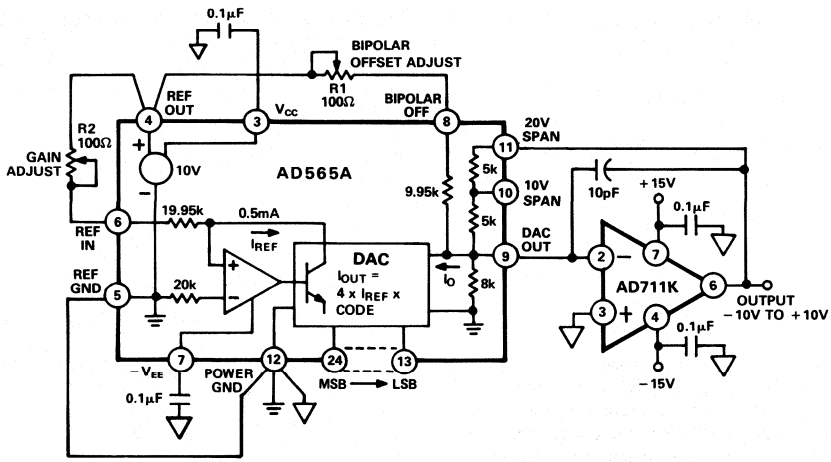
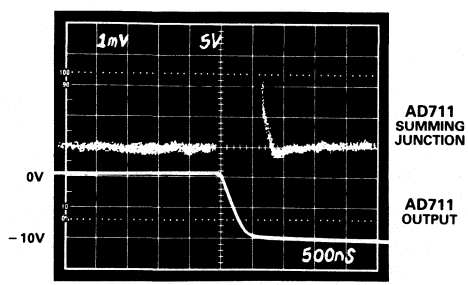
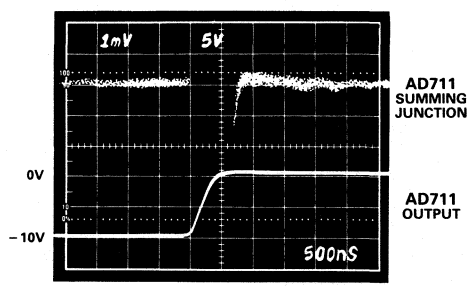


Figure 24. ±10V Voltage Output Bipolar DAC



a. (Full-Scale Negative Transition)



b. (Full-Scale Positive Transition)

Figure 25. Settling Characteristics for AD711 with AD565A

OP AMP SETTLING TIME – A MATHEMATICAL MODEL

The design of the AD711 gives careful attention to optimizing individual circuit components; in addition, a careful tradeoff was made: the gain bandwidth product (4MHz) and slew rate (20V/μs) were chosen to be high enough to provide very fast settling time but not too high to cause a significant reduction in phase margin (and therefore stability). Thus designed, the AD711 settles to ±0.01%, with a 10V output step, in under 1μs, while retaining the ability to drive a 100pF load capacitance when operating as a unity gain follower.

If an op amp is modeled as an ideal integrator with a unity gain crossover frequency of $\omega_O/2\pi$, Equation 1 will accurately describe the small signal behavior of the circuit of Figure 26a, consisting of an op amp connected as an I-to-V converter at the output of a bipolar or CMOS DAC. This equation would completely describe the output of the system if not for the op amp's finite slew rate and other nonlinear effects.

Equation 1.

$$\frac{V_O}{I_{IN}} = \frac{-R}{\frac{R(C_f + C_X)}{\omega_o} s^2 + \left(\frac{G_N}{\omega_o} + RC_f\right) s + 1}$$

where $\frac{\omega_o}{2\pi}$ = op amp's unity gain frequency

G_N = "noise" gain of circuit $\left(1 + \frac{R}{R_O}\right)$

This equation may then be solved for C_f:

Equation 2.

$$C_f = \frac{2 - G_N}{R\omega_o} + \frac{2\sqrt{RC_X\omega_o + (1 - G_N)}}{R\omega_o}$$

In these equations, capacitor C_X is the total capacitance appearing at the inverting terminal of the op amp. When modeling a DAC buffer application, the Norton equivalent circuit of Figure 26a can be used directly; capacitance C_X is the total capacitance of the output of the DAC plus the input capacitance of the op amp (since the two are in parallel).

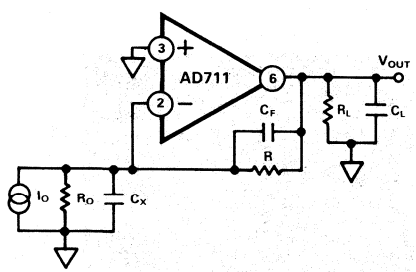


Figure 26a. Simplified Model of the AD711 Used as a Current-Out DAC Buffer

When R_O and I_O are replaced with their Thevenin V_{IN} and R_{IN} equivalents, the general purpose inverting amplifier of Figure 26b is created. Note that when using this general model, capacitance C_X is EITHER the input capacitance of the op amp if a simple inverting op amp is being simulated OR it is the combined capacitance of the DAC output and the op amp input if the DAC buffer is being modeled.

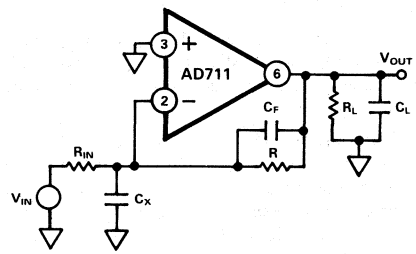


Figure 26b. Simplified Model of the AD711 Used as an Inverter

In either case, the capacitance C_X causes the system to go from a one-pole to a two-pole response; this additional pole increases settling time by introducing peaking or ringing in the op amp output. Since the value of C_X can be estimated with reasonable accuracy, Equation 2 can be used to choose a small capacitor, C_F, to cancel the input pole and optimize amplifier response. Figure 27 is a graphical solution of Equation 2 for the AD711 with R = 4kΩ.

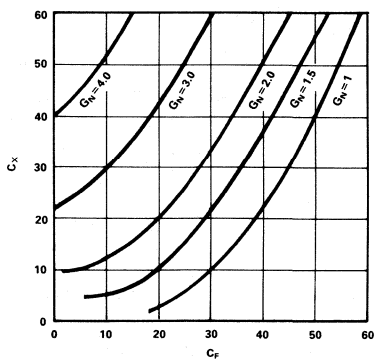


Figure 27. Value of Capacitor C_F vs. Value of C_X

The photos of Figures 28a and 28b show the dynamic response of the AD711 in the settling test circuit of Figure 29.

The input of the settling time fixture is driven by a flat-top pulse generator. The error signal output from the false summing node of A1 is clamped, amplified by A2 and then clamped again. The error signal is thus clamped twice: once to prevent overloading amplifier A2 and then a second time to avoid overloading the oscilloscope preamp. The Tektronix oscilloscope preamp type 7A26 was carefully chosen because it does not overload with these input levels. Amplifier A2 needs to be a very high speed FET-input op amp; it provides a gain of 10, amplifying the error signal output of A1.

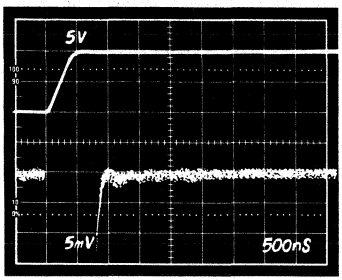


Figure 28a. Settling Characteristics 0 to +10V Step
Upper Trace: Output of AD711 Under Test (5V/Div)
Lower Trace: Amplified Error Voltage (0.01%/Div)

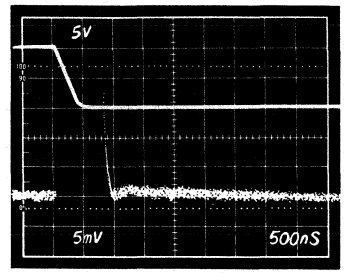


Figure 28b. Settling Characteristics 0 to −10V Step
Upper Trace: Output of AD711 Under Test (5V/Div)
Lower Trace: Amplified Error Voltage (0.01%/Div)

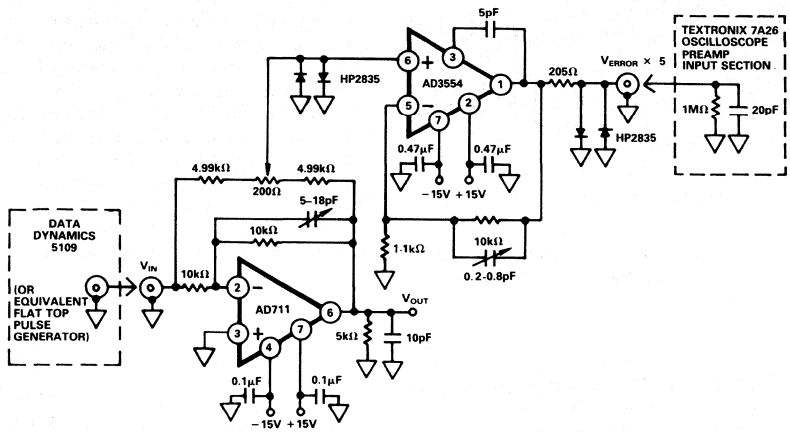


Figure 29. Settling Time Test Circuit

GUARDING

The low input bias current (15pA) and low noise characteristics of the AD711 BiFET op amp make it suitable for electrometer applications such as photo diode preamplifiers and picoampere current-to-voltage converters. The use of a guarding technique such as that shown in Figure 30, in printed circuit board layout and construction is critical to minimize leakage currents. The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on the printed circuit board.

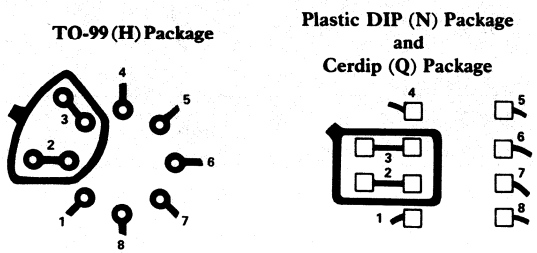


Figure 30. Board Layout for Guarding Inputs

D/A CONVERTER APPLICATIONS

The AD711 is an excellent output amplifier for CMOS DACs. It can be used to perform both 2 quadrant and 4 quadrant operation. The output impedance of a DAC using an inverted R-2R ladder approaches R for codes containing many 1s, 3R for codes containing a single 1, and for codes containing all zero, the output impedance is infinite.

For example, the output resistance of the AD7545 will modulate between 11kΩ and 33kΩ. Therefore, with the DAC's internal feedback resistance of 11kΩ, the noise gain will vary from 2 to 4/3. This changing noise gain modulates the effect of the input offset voltage of the amplifier, resulting in nonlinear DAC-amplifier performance.

The AD711K with guaranteed 500μV offset voltage minimizes this effect to achieve 12-bit performance.

Figures 31 and 32 show the AD711 and AD7545 (12-bit CMOS DAC) configured for unipolar binary (2-quadrant multiplication) or bipolar (4-quadrant multiplication) operation. Capacitor C1 provides phase compensation to reduce overshoot and ringing.

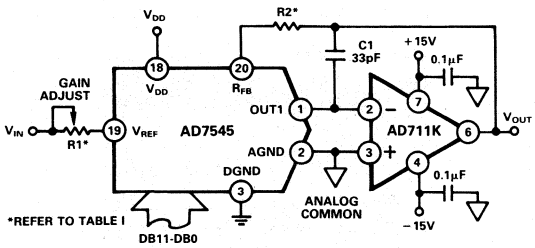


Figure 31. Unipolar Binary Operation

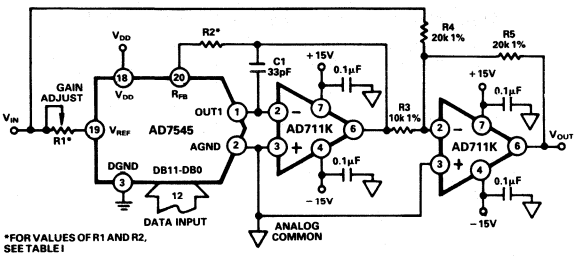


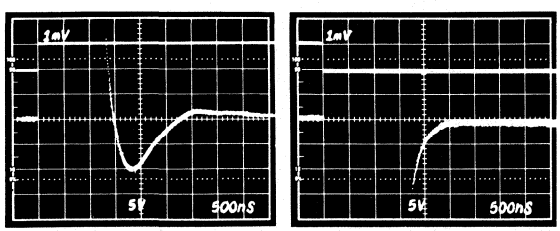
Figure 32. Bipolar Operation

R1 and R2 calibrate the zero offset and gain error of the DAC. Specific values for these resistors depend upon the grade of AD7545 and are shown below.

TRIM RESISTOR	JN/AQ/SD	KN/BQ/TD	LN/CQ/UD	GLN/GCQ/GUD
R1	500Ω	200Ω	100Ω	20Ω
R2	150Ω	68Ω	33Ω	6.8Ω

Table I. Recommended Trim Resistor Values vs. Grades of the AD7545 for V_{DD} = +5V

Figures 33a and 33b show the settling time characteristics of the AD711 when used as a DAC output buffer for the AD7545.



a. Full-Scale Positive Transition

b. Full-Scale Negative Transition

Figure 33. Settling Characteristics for AD711 with AD7545

NOISE CHARACTERISTICS

The random nature of noise, particularly in the 1/f region, makes it difficult to specify in practical terms. At the same time, designers of precision instrumentation require certain guaranteed maximum noise levels to realize the full accuracy of their equipment.

The AD711C grade is specified at a maximum level of 4.0μV p-p, in a 0.1 to 10Hz bandwidth. Each AD711C receives a 100% noise test for two 10-second intervals; devices with any excursion in excess of 4.0μV are rejected. The screened lot is then submitted to Quality Control for verification on an AQL basis.

All other grades of the AD711 are sample-tested on an AQL basis to a limit of 6μV p-p, 0.1 to 10Hz.

DRIVING THE ANALOG INPUT OF AN A/D CONVERTER

An op amp driving the analog input of an A/D converter, such as that shown in Figure 34, must be capable of maintaining a constant output voltage under dynamically changing load conditions. In successive-approximation converters, the input current is compared to a series of switched trial currents. The comparison point is diode clamped but may deviate several hundred millivolts resulting in high frequency modulation of A/D input current. The output impedance of a feedback amplifier is made artificially low by the loop gain. At high frequencies, where the loop gain is low, the amplifier output impedance can approach its open loop value. Most IC amplifiers exhibit a minimum open loop output impedance of 25Ω due to current limiting resistors. A few hundred microamps reflected from the change in converter

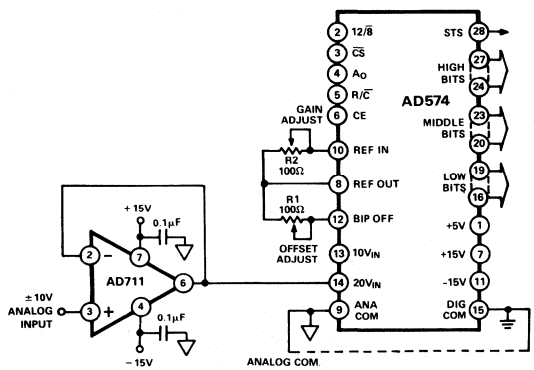
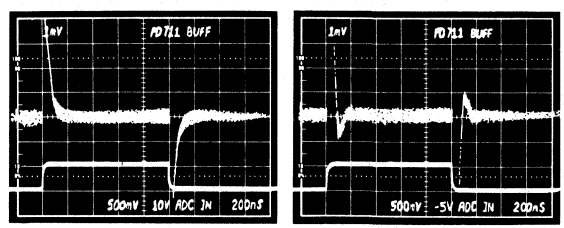


Figure 34. AD711 as ADC Unity Gain Buffer



a. Source Current = 2mA

b. Sink Current = 1mA

Figure 35. ADC Input Unity Gain Buffer Recovery Times

loading can introduce errors in instantaneous input voltage. If the A/D conversion speed is not excessive and the bandwidth of the amplifier is sufficient, the amplifier's output will return to the nominal value before the converter makes its comparison. However, many amplifiers have relatively narrow bandwidth yielding slow recovery from output transients. The AD711 is ideally suited to drive high speed A/D converters since it offers both wide bandwidth and high open-loop gain.

DRIVING A LARGE CAPACITIVE LOAD

The circuit in Figure 36 employs a 100Ω isolation resistor which enables the amplifier to drive capacitive loads exceeding 1500pF; the resistor effectively isolates the high frequency feedback from the load and stabilizes the circuit. Low frequency feedback is returned to the amplifier summing junction via the low pass filter formed by the 100Ω series resistor and the load capacitance, C_L. Figure 37 shows a typical transient response for this connection.

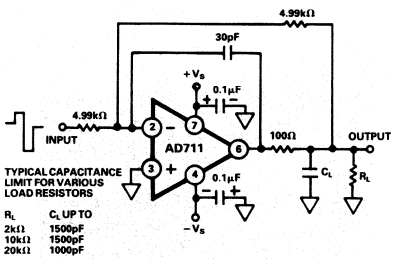


Figure 36. Circuit for Driving a Large Capacitive Load

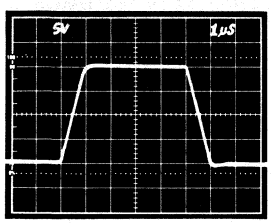


Figure 37. Transient Response R_L = 2kΩ, C_L = 500pF

ACTIVE FILTER APPLICATIONS

In active filter applications using op amps, the dc accuracy of the amplifier is critical to optimal filter performance. The amplifier's offset voltage and bias current contribute to output error. Offset voltage will be passed by the filter and may be amplified to produce excessive output offset. For low frequency applications requiring large value input resistors, bias currents flowing through these resistors will also generate an offset voltage.

In addition, at higher frequencies, an op amp's dynamics must be carefully considered. Here, slew rate, bandwidth, and open-loop gain play a major role in op amp selection. The slew rate must be fast as well as symmetrical to minimize distortion. The amplifier's bandwidth in conjunction with the filter's gain will dictate the frequency response of the frequency response of the filter.

The use of a high performance amplifier such as the AD711 will minimize both dc and ac errors in all active filter applications.

SECOND ORDER LOW PASS FILTER

Figure 38 depicts the AD711 configured as a second order Butterworth low pass filter. With the values as shown, the corner frequency will be 20kHz; however, the wide bandwidth of the AD711 permits a corner frequency as high as several hundred kilohertz. Equations for component selection are shown below.

$$R1 = R2 = \text{user selected (typical values: } 10k\Omega - 100k\Omega)$$

$$C1 = \frac{1.414}{(2\pi)\,(f_{cutoff})\,(R1)}, \quad C2 = \frac{0.707}{(2\pi)\,(f_{cutoff})\,(R1)}$$

Where C1 and C2 are in farads.

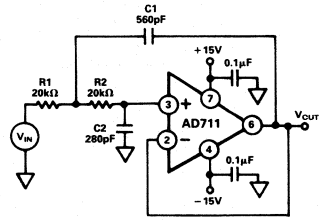


Figure 38. Second Order Low Pass Filter

An important property of filters is their out-of-band rejection. The simple 20kHz low pass filter shown in Figure 38, might be used to condition a signal contaminated with clock pulses or sampling glitches which have considerable energy content at high frequencies.

The low output impedance and high bandwidth of the AD711 minimize high frequency feedthrough as shown in Figure 39.

The upper trace is that of another low cost BiFET op amp showing 17dB more feedthrough at 5MHz.

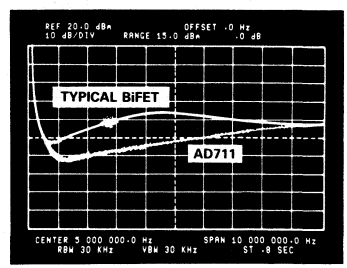


Figure 39.

9 POLE CHEBYCHEV FILTER

Figure 40 shows the AD711 and its dual counterpart, the AD712, as a 9 pole Chebychev filter using active frequency dependent negative resistors (FDNR). With a cutoff frequency of 50kHz and better than 90dB rejection, it may be used as an anti-aliasing filter for a 12-bit Data Acquisition System with 100kHz throughput.

As shown in Figure 40, the filter is comprised of four FDNRs (A, B, C, D) having values of 4.9395×10^{-15} and 5.9276×10^{-15} farad-seconds. Each FDNR active network provides a two-pole response; for a total of 8 poles. The 9th pole consists of a 0.001μF capacitor and a 124kΩ resistor at Pin 3 of amplifier A2. Figure 41 depicts the circuits for each FDNR with the proper selection of R. To achieve optimal performance, the 0.001μF capacitors must be selected for 1% or better matching and all resistors should have 1% or better tolerance.

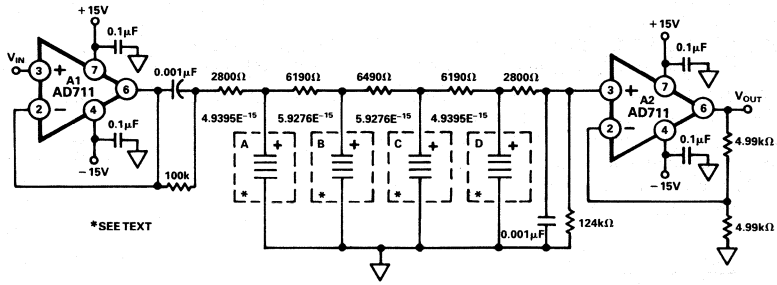


Figure 40. 9 Pole Chebychev Filter

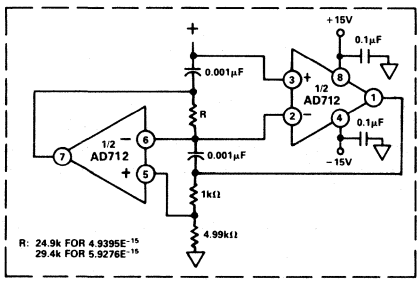


Figure 41. FDNR for 9 Pole Chebychev Filter

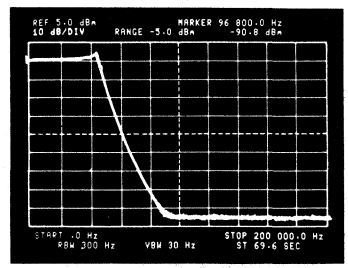


Figure 42. High Frequency Response for 9 Pole Chebychev Filter

ANALOG DEVICES

Dual Precision, Low Cost, High Speed, BiFET Op Amp

AD712

FEATURES

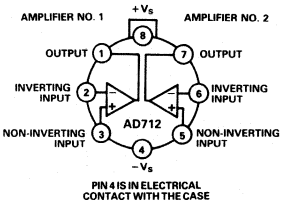
Enhanced Replacement for LF412 and TL082
AC PERFORMANCE:
- **Settles to ±0.01% in 1μs**
- **16V/μs min Slew Rate (AD712J)**
- **3MHz min Unity Gain Bandwidth (AD712J)**

DC PERFORMANCE:
- **0.30mV max Offset Voltage: (AD712C)**
- **5μV/°C max Drift: (AD712C)**
- **200V/mV min Open Loop Gain (AD712K)**
- **4μV p–p max Noise, 0.1Hz to 10Hz (AD712C)**

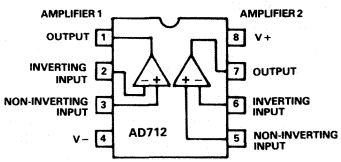
Surface Mount Available in Tape and Reel in Accordance with EIA-481A Standard
MIL-STD-883B Parts Available
Single Version Available: AD711
Quad Version: AD713
Available in Plastic Mini-DIP, Plastic SOIC, Hermetic Cerdip, Hermetic Metal Can Packages and Chip Form

FUNCTIONAL BLOCK DIAGRAMS

TO-99
(H) Package



Plastic Mini-DIP (N) Package,
Cerdip (Q) Package
and SOIC (R) Package



PRODUCT DESCRIPTION

The AD712 is a high speed, precision monolithic operational amplifier offering high performance at very modest prices. Its very low offset voltage and offset voltage drift are results of advanced laser wafer trimming technology. These performance benefits allow the user to easily upgrade existing designs that use older precision BiFETs and, in many cases, bipolar op amps.

The superior ac and dc performance of this op amp makes it suitable for active filter applications. With a slew rate of 16V/μs and a settling time of 1μs to ±0.01%, the AD712 is ideal as a buffer for 12-bit D/A and A/D Converters and as a high-speed integrator. The settling time is unmatched by any similar IC amplifier.

The combination of excellent noise performance and low input current also make the AD712 useful for photo diode preamps. Common-mode rejection of 88dB and open loop gain of 400V/mV ensure 12-bit performance even in high-speed unity gain buffer circuits.

The AD712 is pinned out in a standard op amp configuration and is available in seven performance grades. The AD712J and AD712K are rated over the commercial temperature range of 0 to +70°C. The AD712A, AD712B and AD712C are rated over the industrial temperature range of −40°C to +85°C. The AD712S and AD712T are rated over the military temperature range of −55°C to +125°C and are available processed to MIL-STD-883B, Rev. C.

Extended reliability PLUS screening is available, specified over the commercial and industrial temperature ranges. PLUS screening includes 168-hour burn-in, as well as other environmental and physical tests.

The AD712 is available in an 8-pin plastic mini-DIP, cerdip, SOIC, TO-99 metal can, or in chip form.

PRODUCT HIGHLIGHTS

1. The AD712 offers excellent overall performance at very competitive prices.
2. Analog Devices' advanced processing technology and with 100% testing guarantees a low input offset voltage (0.3mV max, C grade, 3mV max, J grade). Input offset voltage is specified in the warmed-up condition. Analog Devices' laser wafer drift trimming process reduces input offset voltage drifts to 5μV/°C max on the AD712C.
3. Along with precision dc performance, the AD712 offers excellent dynamic response. It settles to ±0.01% in 1μs and has a 100% tested minimum slew rate of 16V/μs. Thus this device is ideal for applications such as DAC and ADC buffers which require a combination of superior ac and dc performance.
4. The AD712 has a guaranteed and tested maximum voltage noise of 4μV p–p, 0.1 to 10Hz (AD712C).
5. Analog Devices' well-matched, ion-implanted JFETs ensure a guaranteed input bias current (at either input) of 50pA max (AD712C) and an input offset current of 10pA max (AD712C). Both input bias current and input offset current are guaranteed in the warmed-up condition.

AD712—SPECIFICATIONS (@ +25°C and V_S = ±15 V dc, unless otherwise noted)

Model	AD712J/A/S			AD712K/B/T			AD712C			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
INPUT OFFSET VOLTAGE[1]										
Initial Offset		0.3	**3/1/1**		0.2	**1/0.7/0.7**		0.1	**0.30**	mV
T_{min} to T_{max}			**4/2/2**			**2/1.5/1.5**			**0.60**	mV
vs. Temp.		7	**20/20/20**		7	**10**		3	**5**	µV/°C
vs. Supply	**76**	95		**80**	100		**86**	110		dB
vs. Supply, T_{min} to T_{max}	**76/76/76**			**80**			**86**			dB
Long-Term Offset Stability		15			15			15		µV/month
INPUT BIAS CURRENT[2]										
Either Input, V_{CM} = 0		25	**75**		20	75		20	**50**	pA
Either Input at T_{max},										
V_{CM} = 0 (70°C/85°C/125°C)		0.6/1.6/26	1.7/4.8/**77**		0.5/1.3/20	1.7/4.8/**77**		1.3	3.2	nA
Either Input, V_{CM} = +10V			**100**			**100**			**75**	pA
Offset Current, V_{CM} = 0		10	**25**		5	**25**		5	**10**	pA
Offset Current at T_{max}										
(70°C/85°C/125°C)		0.3/0.7/11	0.6/1.6/26		0.1/0.3/5	0.6/1.6/26		0.3	0.7	nA
MATCHING CHARACTERISTICS[3]										
Input Offset Voltage			**3/1/1**			**1/0.7/0.7**			**0.3**	mV
Input Offset Voltage T_{min} to T_{max}			**4/2/2**			**2/1.5/1.5**			**0.6**	mV
Input Offset Voltage vs. Temp			**20/20/20**			**10**			**5**	µV/°C
Input Bias Current			**25**			**25**			**10**	pA
Crosstalk[4] @ 1kHz		120			120			120		dB
@ 100kHz		90			90			90		dB
FREQUENCY RESPONSE										
Unity Gain, Small Signal	3.0	4		3.4	4		3.4	4		MHz
Full Power Response		200			200			200		kHz
Slew Rate, Unity Gain	**16**	20		**18**	20		**18**	20		V/µs
Settling Time to 0.01%[5]		1	1.2		1	1.2		1	1.2	µs
Total Harmonic Distortion										
f = 1kHz, $R_L \geq 2k\Omega$, V_O = 3V rms		0.0003			0.0003			0.0003		%
INPUT IMPEDANCE										
Differential		$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$		Ω‖pF
Common Mode		$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$			$3 \times 10^{12} \| 5.5$		Ω‖pF
INPUT VOLTAGE RANGE										
Differential[6]		±20			±20			±20		V
Common-Mode Voltage										
Over Max Operating Range[7]	$-V_S+4V$	+14.5, −11.5	$+V_S-2V$	$-V_S+4V$	+14.5, −11.5	$+V_S-2V$	$-V_S+4V$	+14.5, −11.5	$+V_S-2V$	V
Common-Mode Rejection Ratio										
V_{CM} = ±10V	**76**	88		**80**	88		**86**	94		dB
T_{min} to T_{max}	76/76/**76**	84		**80**	84		**86**	90		dB
V_{CM} = ±11V	**70**	84		**76**	84		**76**	90		dB
T_{min} to T_{max}	70/70/**70**	80		**74**	80		**74**	84		dB
INPUT VOLTAGE NOISE										
Voltage 0.1Hz to 10Hz		2			2			2	**4**	µV p-p
f = 10Hz		45			45			45		nV/√Hz
f = 100Hz		22			22			22		nV/√Hz
f = 1kHz		18			18			18		nV/√Hz
f = 10kHz		16			16			16		nV/√Hz
INPUT CURRENT NOISE										
f = 1kHz		0.01			0.01			0.01		pA/√Hz
OPEN LOOP GAIN										
V_O = ±10V, $R_L \geq 2k\Omega$	**150**	400		**200**	400		**200**	400		V/mV
T_{min} to T_{max}, $R_L \geq 2k\Omega$	100/100/**100**			**100**			**100**			V/mV
OUTPUT CHARACTERISTICS										
Voltage @ $R_L \geq 2k\Omega$	**+13, −12.5**	+13.9, −13.3		**+13, −12.5**	+13.9, −13.3		**+13, −12.5**	+13.9, −13.3		V
T_{min} to T_{max}	±12, ±12, **±12**	+13.8, −13.1		**±12**	+13.8, −13.1		**±12**	+13.8, −13.1		V
Short Circuit Current		25			25			25		mA
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating Range	**±4.5**		**±18**	**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current,										
Both Amplifiers		5	**6.8**		5	**6.0**		5	**5.6**	mA
TEMPERATURE RANGE										
Operating, Rated Performance										
Commercial (0 to +70°C)		AD712J			AD712K					
Industrial (−40°C to +85°C)		AD712A			AD712B			AD712C		
Military (−55°C to +125°C)		AD712S			AD712T					
PACKAGE OPTIONS[8]										
SOIC (R-8)		AD712JR			AD712KR					
Plastic (N-8)		AD712JN			AD712KN					
Cerdip (Q-8)		AD712AQ, AD712SQ			AD712BQ, AD712TQ			AD712CQ		
TO-99 (H-08A)		AD712AH, AD712SH			AD712BH, AD712TH			AD712CH		
Tape and Reel		AD712JR-REEL			AD712KR-REEL					
A, J and S Grade Chips Available										

NOTES
[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at $T_A = +25°C$.
[2]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at $T_A = +25°C$. For higher temperature, the current doubles every 10°C.
[3]Matching is defined as the difference between parameters of the two amplifiers.
[4]Refer to Figure 21.
[5]Refer to Figure 29.
[6]Defined as voltage between inputs, such that neither exceeds ±10V from ground.
[7]Typically exceeding −14.1V negative common-mode voltage on either input results in an output phase reversal.
[8]For outline information see Package Information section.

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

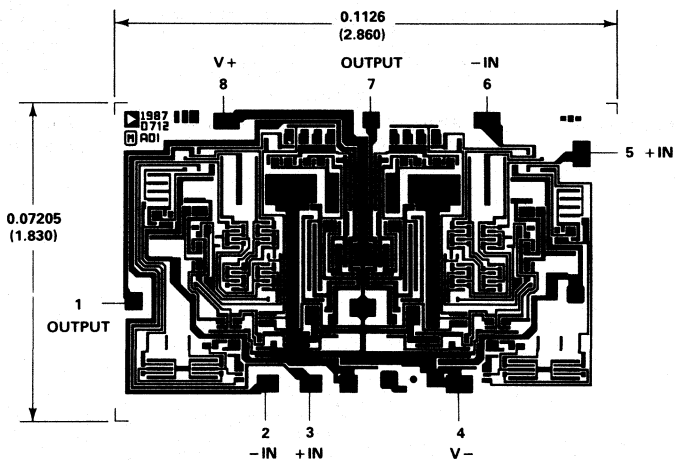
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18V
Internal Power Dissipation[2]
Input Voltage[3] . . . . . ±18V
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range (Q, H) . . . . . −65°C to +150°C
Storage Temperature Range (N, R) . . . . . −65°C to +125°C
Operating Temperature Range
AD712J/K . . . . . 0 to +70°C
AD712A/B/C . . . . . −40°C to +85°C
AD712S/T . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 seconds) . . . . 300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Thermal Characteristics:
8-Pin Plastic Package: $\theta_{JA} = 165°C/W$.
8-Pin Cerdip Package: $\theta_{JC} = 22°C/W$, $\theta_{JA} = 110°C/W$.
8-Pin Metal Can Package: $\theta_{JC} = 65°C/W$, $\theta_{JA} = 150°C/W$.
8-Pin SOIC Package: $\theta_{JA} = 100°C$.
[3]For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



AD712—Typical Characteristics

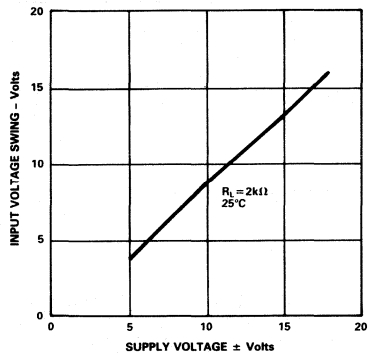


Figure 1. Input Voltage Swing vs. Supply Voltage

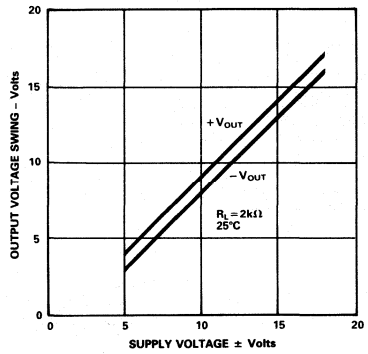


Figure 2. Output Voltage Swing vs. Supply Voltage

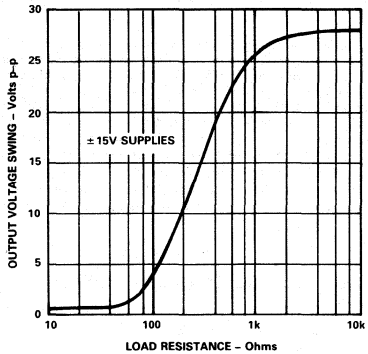


Figure 3. Output Voltage Swing vs. Load Resistance

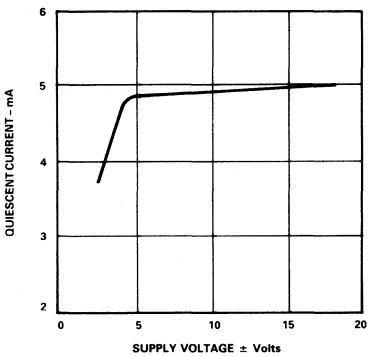


Figure 4. Quiescent Current vs. Supply Voltage

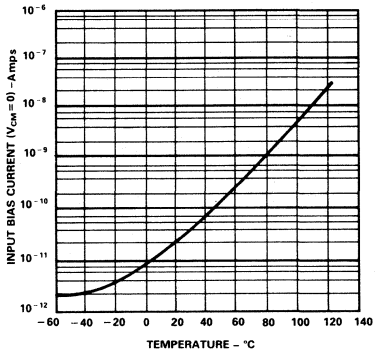


Figure 5. Input Bias Current vs. Temperature

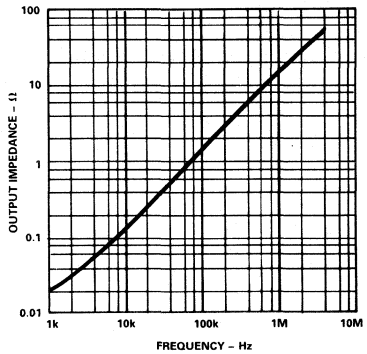


Figure 6. Output Impedance vs. Frequency

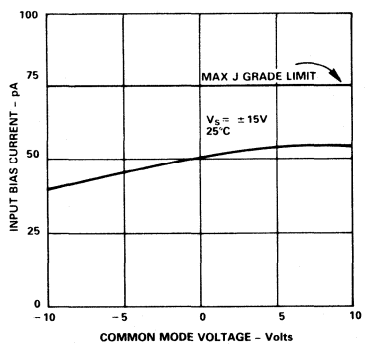


Figure 7. Input Bias Current vs. Common Mode Voltage

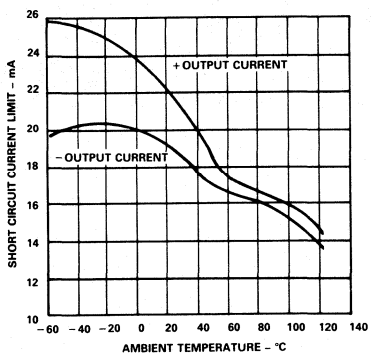


Figure 8. Short Circuit Current Limit vs. Temperature

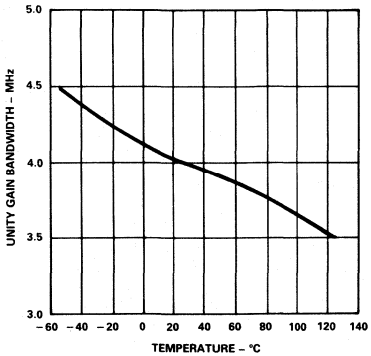


Figure 9. Unity Gain Bandwidth vs. Temperature

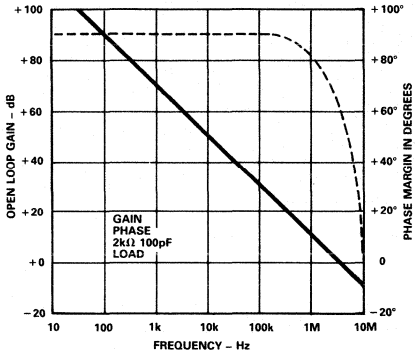


Figure 10. Open Loop Gain and Phase Margin vs. Frequency

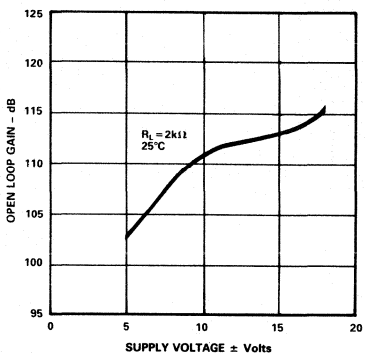


Figure 11. Open Loop Gain vs. Supply Voltage

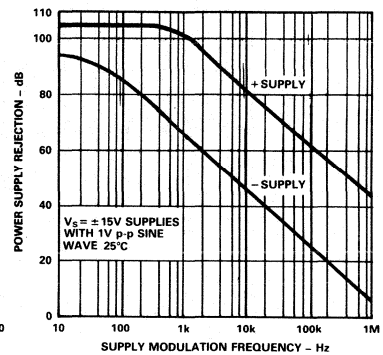


Figure 12. Power Supply Rejection vs. Frequency

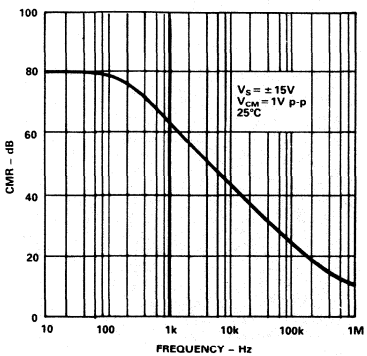


Figure 13. Common Mode Rejection vs. Frequency

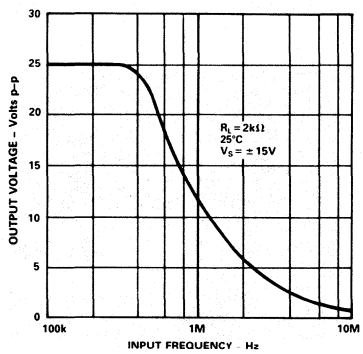


Figure 14. Large Signal Frequency Response

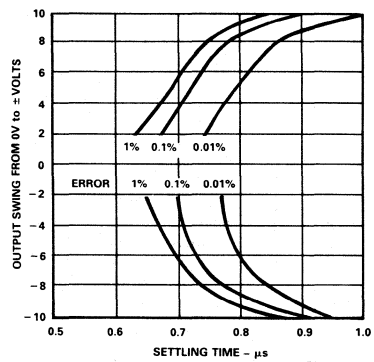


Figure 15. Output Swing and Error vs. Settling Time

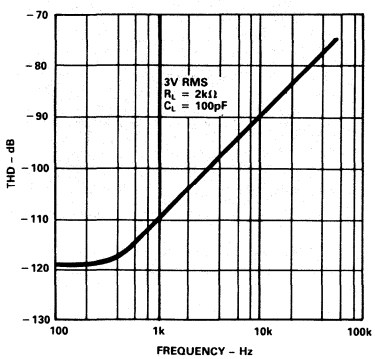


Figure 16. Total Harmonic Distortion vs. Frequency

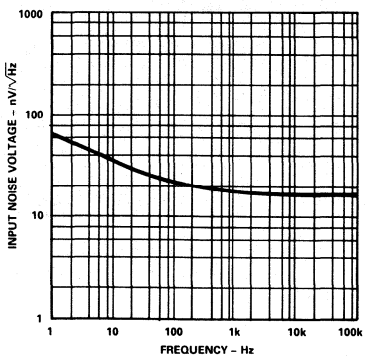


Figure 17. Input Noise Voltage Spectral Density

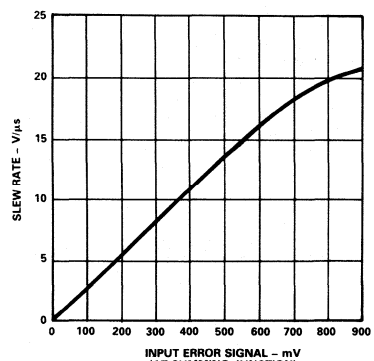


Figure 18. Slew Rate vs. Input Error Signal

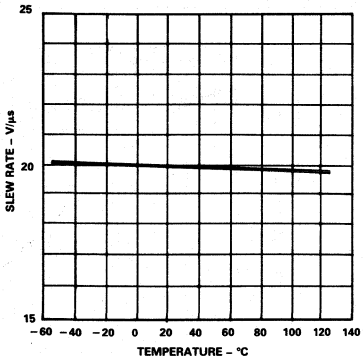


Figure 19. Slew Rate vs. Temperature

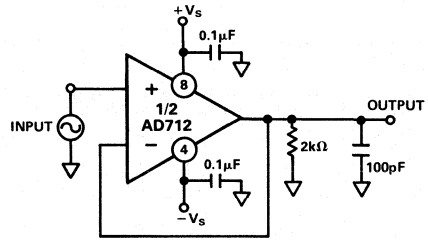


Figure 20. T.H.D. Test Circuit

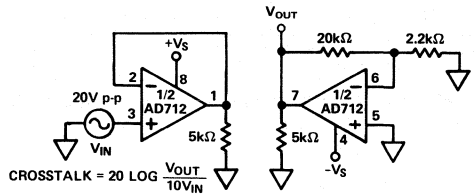


Figure 21. Crosstalk Test Circuit

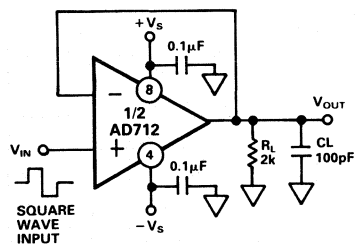


Figure 22a. Unity Gain Follower

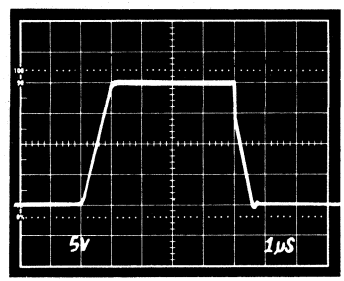


Figure 22b. Unity Gain Follower Pulse Response (Large Signal)

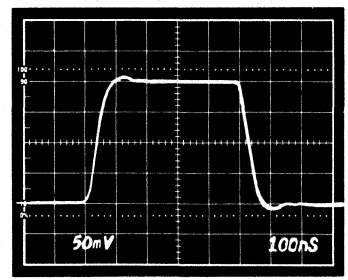


Figure 22c. Unity Gain Follower Pulse Response (Small Signal)

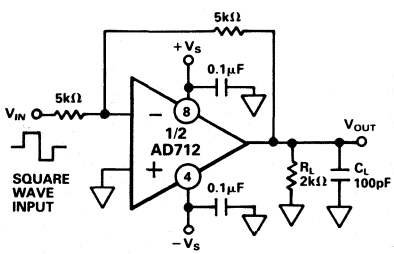


Figure 23a. Unity Gain Inverter

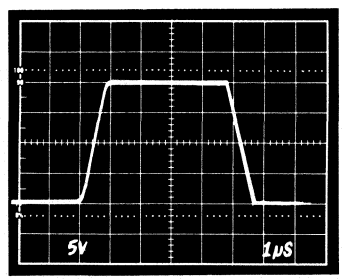


Figure 23b. Unity Gain Inverter Pulse Response (Large Signal)

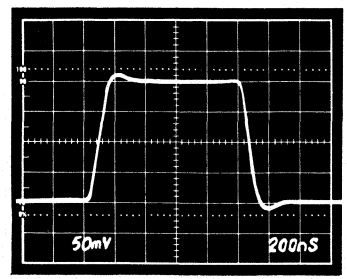


Figure 23c. Unity Gain Inverter Pulse Response (Small Signal)

OPTIMIZING SETTLING TIME

Most bipolar high-speed D/A converters have curent outputs; therefore, for most applications, an external op amp is required for current-to-voltage conversion. The settling time of the converter/op amp combination depends on the settling time of the DAC and output amplifier. A good approximation is:

$$t_s \text{ Total} = \sqrt{(t_s \text{ DAC})^2 + (t_s \text{ AMP})^2}$$

The settling time of an op amp DAC buffer will vary with the noise gain of the circuit, the DAC output capacitance, and with the amount of external compensation capacitance across the DAC output scaling resistor.

Settling time for a bipolar DAC is typically 100 to 500ns. Previously, conventional op amps have required much longer settling times than have typical state-of-the-art DACs; therefore, the amplifier settling time has been the major limitation to a high-speed voltage-output D-to-A function. The introduction of the AD711/712 family of op amps with their 1μs (to ±0.01% of final value) settling time now permits the full high-speed capabilities of most modern DACs to be realized.

In addition to a significant improvement in settling time, the low offset voltage, low offset voltage drift, and high open-loop gain of the AD711/AD712 family assures 12-bit accuracy over the full operating temperature range.

The excellent high-speed performance of the AD712 is shown in the oscilloscope photos of Figure 25. Measurements were taken using a low input capacitance amplifier connected directly to the summing junction of the AD712 – both photos show the worst case situation: a full-scale input transition. The DAC's 4kΩ [10kΩ‖8kΩ = 4.4kΩ] output impedance together with a 10kΩ feedback resistor produce an op amp noise gain of 3.25. The current output from the DAC produces a 10V step at the op amp output (0 to −10V Figure 25a, −10V to 0V Figure 25b.)

Therefore, with an ideal op amp, settling to ±1/2LSB (±0.01%) requires that 375μV or less appears at the summing junction. This means that the error between the input and output (that voltage which appears at the AD712 summing junction) must be less than 375μV. As shown in Figure 25, the total settling time for the AD712/AD565 combination is 1.2 microseconds.

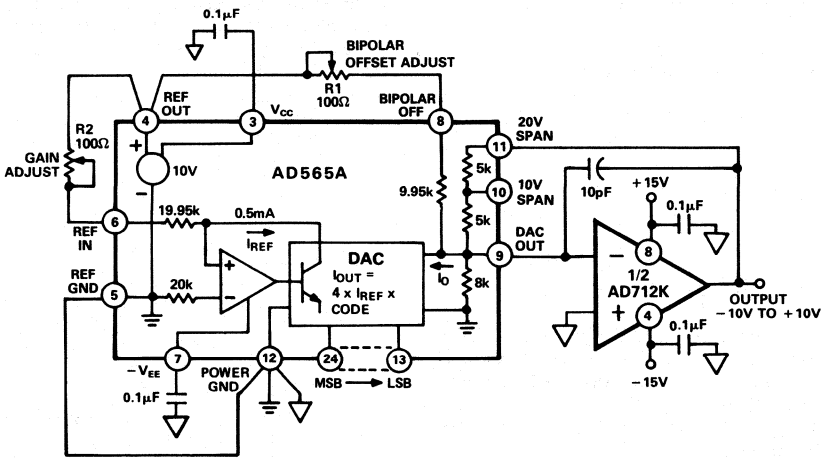
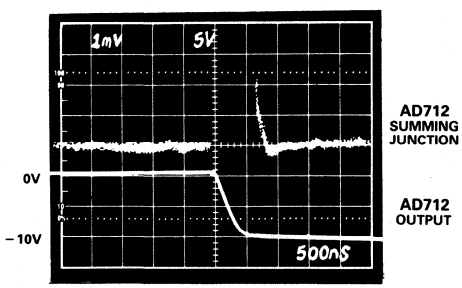
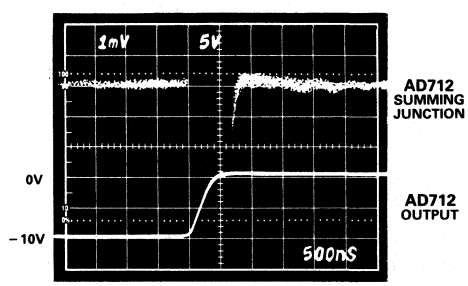


Figure 24. ±10V Voltage Output Bipolar DAC



a. (Full-Scale Negative Transition)



b. (Full-Scale Positive Transition)

Figure 25. Settling Characteristics for AD712 with AD565A

OP AMP SETTLING TIME–A MATHEMATICAL MODEL

The design of the AD712 gives careful attention to optimizing individual circuit components; in addition, a careful tradeoff was made: the gain bandwidth product (4MHz) and slew rate (20V/μs) were chosen to be high enough to provide very fast settling time but not too high to cause a significant reduction in phase margin (and therefore stability). Thus designed, the AD712 settles to ±0.01%, with a 10V output step, in under 1μs, while retaining the ability to drive a 250pF load capacitance when operating as a unity gain follower.

If an op amp is modeled as an ideal integrator with a unity gain crossover frequency of $\omega_O/2\pi$, Equation 1 will accurately describe the small signal behavior of the circuit of Figure 26a, consisting of an op amp connected as an I-to-V converter at the output of a bipolar or CMOS DAC. This equation would completely describe the output of the system if not for the op amp's finite slew rate and other nonlinear effects.

Equation 1.

$$\frac{V_O}{I_{IN}} = \frac{-R}{\frac{R(C_f + C_X)}{\omega_o} s^2 + \left(\frac{G_N}{\omega_o} + RC_f\right) s + 1}$$

where $\frac{\omega_o}{2\pi}$ = op amp's unity gain frequency

G_N = "noise" gain of circuit $\left(1 + \frac{R}{R_O}\right)$

This equation may then be solved for C_f:

Equation 2.

$$C_f = \frac{2 - G_N}{R\omega_o} + \frac{2\sqrt{RC_X\omega_o + (1 - G_N)}}{R\omega_o}$$

In these equations, capacitor C_X is the total capacitance appearing at the inverting terminal of the op amp. When modeling a DAC buffer application, the Norton equivalent circuit of Figure 26a can be used directly; capacitance C_X is the total capacitance of the output of the DAC plus the input capacitance of the op amp (since the two are in parallel).

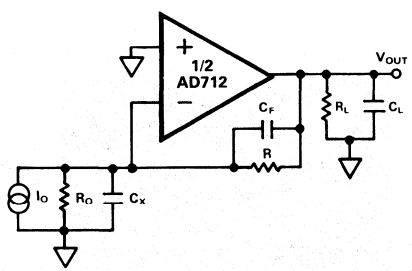


Figure 26a. Simplified Model of the AD712 Used as a Current-Out DAC Buffer

When R_O and I_O are replaced with their Thevenin V_{IN} and R_{IN} equivalents, the general purpose inverting amplifier of Figure 26b is created. Note that when using this general model, capacitance C_X is EITHER the input capacitance of the op amp if a simple inverting op amp is being simulated OR it is the combined capacitance of the DAC output and the op amp input if the DAC buffer is being modeled.

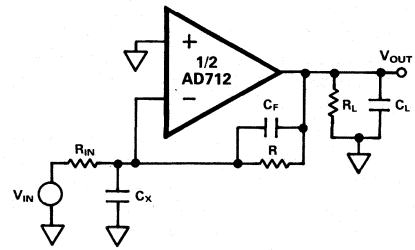


Figure 26b. Simplified Model of the AD712 Used as an Inverter

In either case, the capacitance C_X causes the system to go from a one-pole to a two-pole response; this additional pole increases settling time by introducing peaking or ringing in the op amp output. Since the value of C_X can be estimated with reasonable accuracy, Equation 2 can be used to choose a small capacitor, C_F, to cancel the input pole and optimize amplifier response. Figure 27 is a graphical solution of Equation 2 for the AD712 with R = 4kΩ.

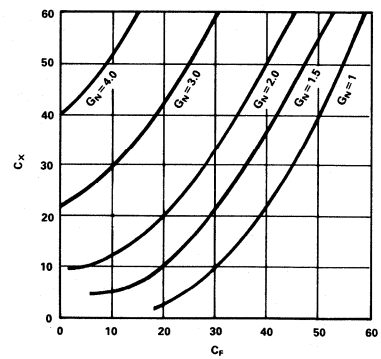


Figure 27. Value of Capacitor C_F vs. Value of C_X

The photos of Figures 28a and 28b show the dynamic response of the AD712 in the settling test circuit of Figure 29.

The input of the settling time fixture is driven by a flat-top pulse generator. The error signal output from the false summing node of A1 is clamped, amplified by A2 and then clamped again. The error signal is thus clamped twice: once to prevent overloading amplifier A2 and then a second time to avoid overloading the oscilloscope preamp. The Tektronix oscilloscope preamp type 7A26 was carefully chosen because it does not overload with these input levels. Amplifier A2 needs to be a very high-speed, FET-input op amp; it provides a gain of 10, amplifying the error signal output of A1.

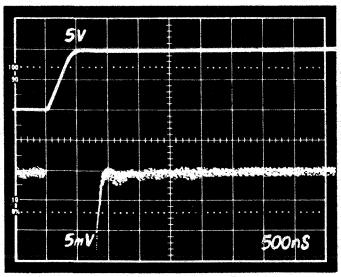


Figure 28a. Settling Characteristics 0 to +10V Step
Upper Trace: Output of AD712 Under Test (5V/Div)
Lower Trace: Amplified Error Voltage (0.01%/Div)

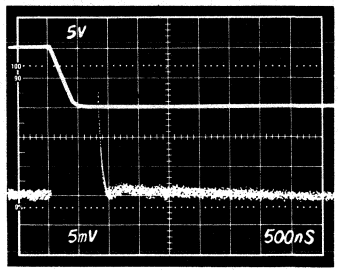


Figure 28b. Settling Characteristics 0 to −10V Step
Upper Trace: Output of AD712 Under Test (5V/Div)
Lower Trace: Amplified Error Voltage (0.01%/Div)

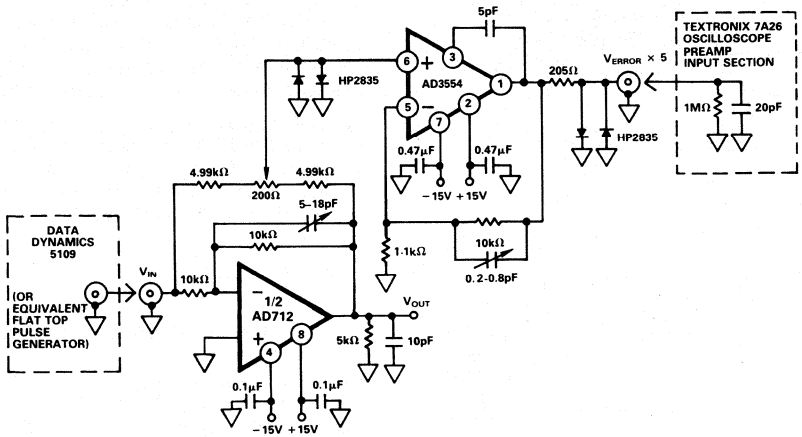


Figure 29. Settling Time Test Circuit

GUARDING

The low input bias current (15pA) and low noise characteristics of the AD712 BiFET op amp make it suitable for electrometer applications such as photo diode preamplifiers and picoampere current-to-voltage converters. The use of a guarding technique such as that shown in Figure 30, in printed circuit board layout and construction is critical to minimize leakage currents. The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on the printed circuit board.

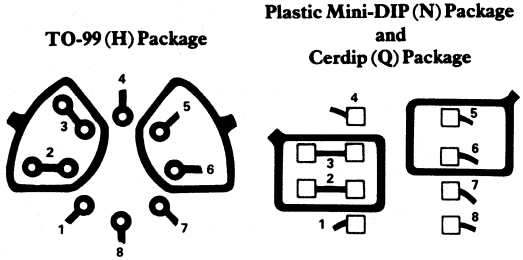


Figure 30. Board Layout for Guarding Inputs

D/A CONVERTER APPLICATIONS

The AD712 is an excellent output amplifier for CMOS DACs. It can be used to perform both 2 quadrant and 4 quadrant operation. The output impedance of a DAC using an inverted R-2R ladder approaches R for codes containing many 1s, 3R for codes containing a single 1, and for codes containing all zero, the output impedance is infinite.

For example, the output resistance of the AD7545 will modulate between 11kΩ and 33kΩ. Therefore, with the DAC's internal feedback resistance of 11kΩ, the noise gain will vary from 2 to 4/3. This changing noise gain modulates the effect of the input offset voltage of the amplifier, resulting in nonlinear DAC-amplifier performance.

The AD712K with guaranteed 700μV offset voltage minimizes this effect to achieve 12-bit performance.

Figures 31 and 32 show the AD712 and AD7545 (12-bit CMOS DAC) configured for unipolar binary (2-quadrant multiplication) or bipolar (4-quadrant multiplication) operation. Capacitor C1 provides phase compensation to reduce overshoot and ringing.

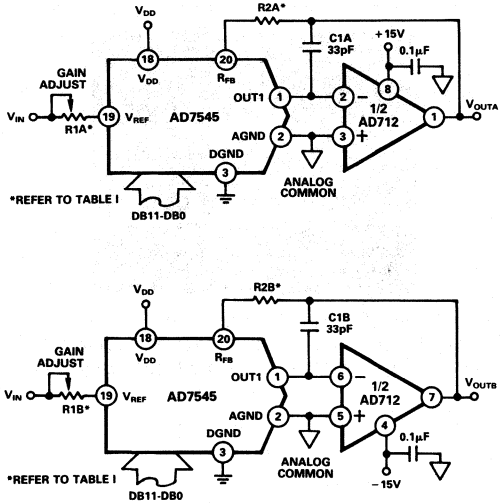


Figure 31. Unipolar Binary Operation

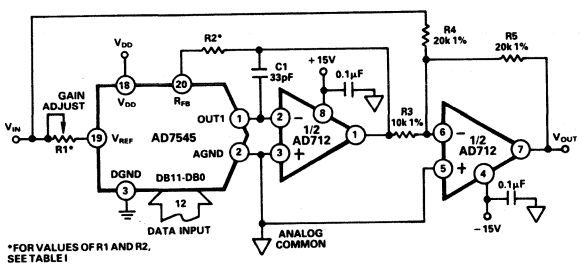


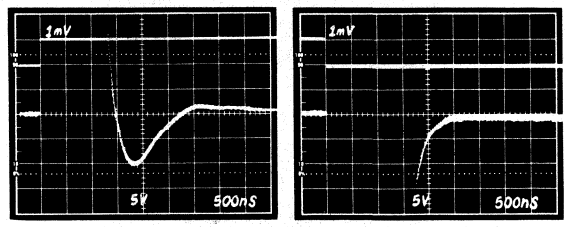
Figure 32. Bipolar Operation

R1 and R2 calibrate the zero offset and gain error of the DAC. Specific values for these resistors depend upon the grade of AD7545 and are shown below.

TRIM RESISTOR	JN/AQ/SD	KN/BQ/TD	LN/CQ/UD	GLN/GCQ/GUD
R1	500Ω	200Ω	100Ω	20Ω
R2	150Ω	68Ω	33Ω	6.8Ω

Table I. Recommended Trim Resistor Values vs. Grades of the AD7545 for V_{DD} = +5V

Figures 33a and 33b show the settling time characteristics of the AD712 when used as a DAC output buffer for the AD7545.



a. Full-Scale Positive Transition

b. Full-Scale Negative Transition

Figure 33. Settling Characteristics for AD712 with AD7545

NOISE CHARACTERISTICS

The random nature of noise, particularly in the l/f region, makes it difficult to specify in practical terms. At the same time, designers of precision instrumentation require certain guaranteed maximum noise levels to realize the full accuracy of their equipment.

The AD712C grade is specified at a maximum level of 4.0μV p-p, in a 0.1 to 10Hz bandwidth. Each AD712C receives a 100% noise test for two 10-second intervals; devices with any excursion in excess of 4.0μV are rejected. The screened lot is then submitted to Quality Control for verification on an AQL basis.

All other grades of the AD712 are sample-tested on an AQL basis to a limit of 6μV p-p, 0.1 to 10Hz.

DRIVING THE ANALOG INPUT OF AN A/D CONVERTER

An op amp driving the analog input of an A/D converter, such as that shown in Figure 34, must be capable of maintaining a constant output voltage under dynamically changing load conditions. In successive-approximation converters, the input current is compared to a series of switched trial currents. The comparison point is diode clamped but may deviate several hundred millivolts resulting in high frequency modulation of A/D input current. The output impedance of a feedback amplifier is made artificially low by the loop gain. At high frequencies, where the loop gain is low, the amplifier output impedance can approach its open loop value. Most IC amplifiers exhibit a minimum open loop output impedance of 25Ω due to current limiting resistors. A

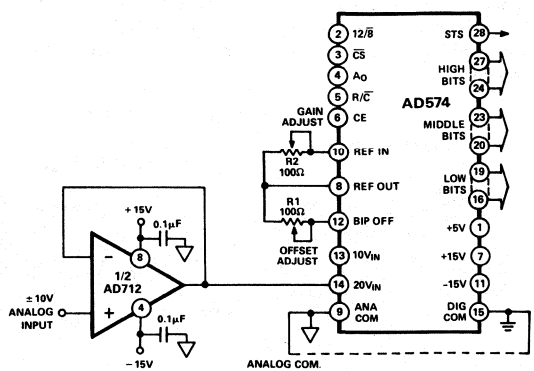
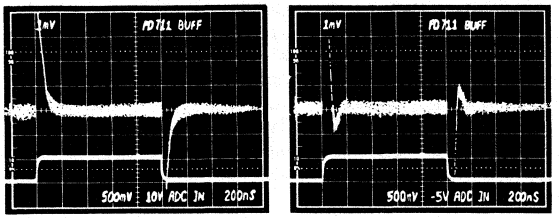


Figure 34. AD712 as ADC Unity Gain Buffer



a. Source Current = 2mA *b. Sink Current = 1mA*

Figure 35. ADC Input Unity Gain Buffer Recovery Times

few hundred microamps reflected from the change in converter loading can introduce errors in instantaneous input voltage. If the A/D conversion speed is not excessive and the bandwidth of the amplifier is sufficient, the amplifier's output will return to the nominal value before the converter makes its comparison. However, many amplifiers have relatively narrow bandwidth yielding slow recovery from output transients. The AD712 is ideally suited to drive high-speed A/D converters since it offers both wide bandwidth and high open-loop gain.

DRIVING A LARGE CAPACITIVE LOAD

The circuit in Figure 36 employs a 100Ω isolation resistor which enables the amplifier to drive capacitive loads exceeding 1500pF; the resistor effectively isolates the high frequency feedback from the load and stabilizes the circuit. Low frequency feedback is returned to the amplifier summing junction via the low pass filter formed by the 100Ω series resistor and the load capacitance, C_L. Figure 37 shows a typical transient response for this connection.

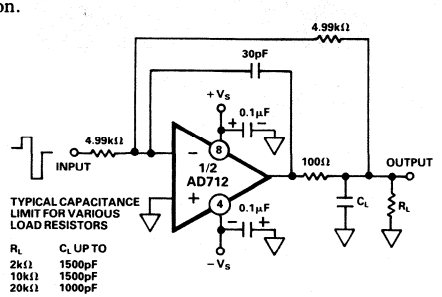


Figure 36. Circuit for Driving a Large Capacitive Load

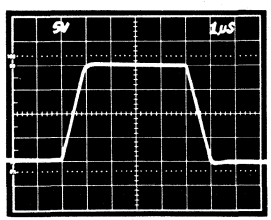


Figure 37. Transient Response R_L = 2kΩ, C_L = 500pF

ACTIVE FILTER APPLICATIONS

In active filter applications using op amps, the dc accuracy of the amplifier is critical to optimal filter performance. The amplifier's offset voltage and bias current contribute to output error. Offset voltage will be passed by the filter and may be amplified to produce excessive output offset. For low frequency applications requiring large value input resistors, bias currents flowing through these resistors will also generate an offset voltage.

In addition, at higher frequencies, an op amp's dynamics must be carefully considered. Here, slew rate, bandwidth, and open-loop gain play a major role in op amp selection. The slew rate must be fast as well as symmetrical to minimize distortion. The amplifier's bandwidth in conjunction with the filter's gain will dictate the frequency response of the filter.

The use of a high performance amplifier such as the AD712 will minimize both dc and ac errors in all active filter applications.

SECOND ORDER LOW PASS FILTER

Figure 38 depicts the AD712 configured as a second order Butterworth low pass filter. With the values as shown, the corner frequency will be 20kHz; however, the wide bandwidth of the AD712 permits a corner frequency as high as several hundred kilohertz. Equations for component selection are shown below.

$$R1 = R2 = \text{user selected (typical values: } 10k\Omega - 100k\Omega)$$

$$C1 \text{ (in farads)} = \frac{1.414}{(2\pi)\,(f_{cutoff})\,(R1)} \qquad C2 = \frac{0.707}{(2\pi)\,(f_{cutoff})\,(R1)}$$

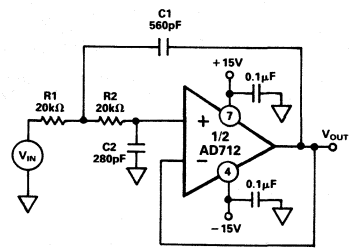


Figure 38. Second Order Low Pass Filter

An important property of filters is their out-of-band rejection. The simple 20kHz low pass filter shown in Figure 38, might be used to condition a signal contaminated with clock pulses or sampling glitches which have considerable energy content at high frequencies.

The low output impedance and high bandwidth of the AD712 minimize high frequency feedthrough as shown in Figure 39.

The upper trace is that of another low-cost BiFET op amp showing 17dB more feedthrough at 5MHz.

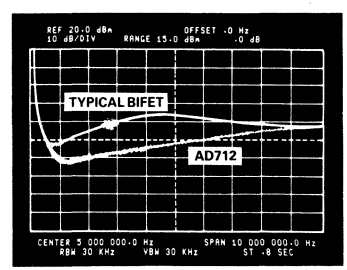


Figure 39.

9-POLE CHEBYCHEV FILTER

Figure 40 shows the AD712 and its single counterpart, the AD711, as a 9-pole Chebychev filter using active frequency dependent negative resistors (FDNR). With a cutoff frequency of 50kHz and better than 90dB rejection, it may be used as an antialiasing filter for a 12-bit Data Acquisition System with 100kHz throughput.

As shown in Figure 40, the filter is comprised of four FDNRs (A, B, C, D) having values of 4.9395×10^{-15} and 5.9276×10^{-15} farad-seconds. Each FDNR active network provides a two-pole response; for a total of 8 poles. The 9th pole consists of a 0.001μF capacitor and a 124kΩ resistor at Pin 3 of amplifier A2. Figure 41 depicts the circuits for each FDNR with the proper selection of R. To achieve optimal performance, the 0.001μF capacitors must be selected for 1% or better matching and all resistors should have 1% or better tolerance.

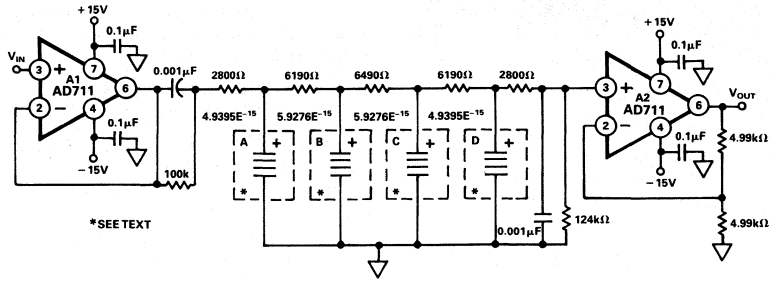


Figure 40. 9-Pole Chebychev Filter

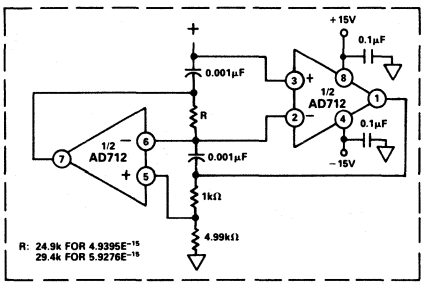


Figure 41. FDNR for 9-Pole Chebychev Filter

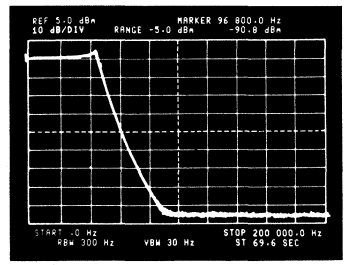


Figure 42. High Frequency Response for 9-Pole Chebychev Filter

Quad Precision, Low Cost, High Speed BiFET Op Amp

AD713

FEATURES

Enhanced Replacement for LF347 and TL084

AC PERFORMANCE

- **1μs Settling to 0.01% for 10V Step**
- **20V/μs Slew Rate**
- **0.0003% Total Harmonic Distortion (THD)**
- **4MHz Unity Gain Bandwidth**

DC PERFORMANCE

- **0.5mV max Offset Voltage (AD713K)**
- **20μV/°C max Drift (AD713K)**
- **200V/mV min Open Loop Gain (AD713K)**
- **2μV p–p typ Noise, 0.1Hz to 10Hz**

True 14-Bit Accuracy

Single Version: AD711, Dual Version: AD712

Available in 16-Pin SOIC, 14-Pin Plastic DIP and Hermetic Cerdip Packages and in Chip Form

MIL-STD-883B Processing Available

Standard Military Drawing Available

APPLICATIONS

Active Filters

Quad Output Buffers for 12- and 14-Bit DACs

Input Buffers for Precision ADCs

Photo Diode Preamplifier Applications

PRODUCT DESCRIPTION

The AD713 is a quad operational amplifier, consisting of four AD711 BiFET op amps. These precision monolithic op amps offer excellent dc characteristics plus rapid settling times, high slew rates, and ample bandwidths. In addition, the AD713 provides the close matching ac and dc characteristics inherent to amplifiers sharing the same monolithic die.

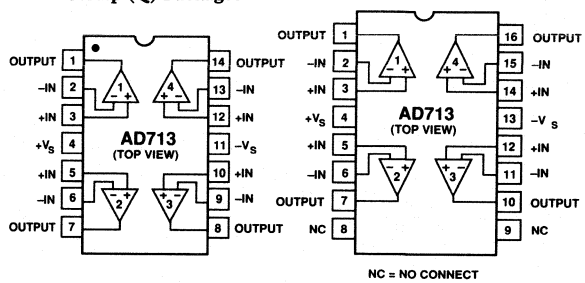
The single-pole response of the AD713 provides fast settling: 1μs to 0.01%. This feature, combined with its high dc precision, makes it suitable for use as a buffer amplifier for 12- or 14-bit DACs and ADCs. It is also an excellent choice for use in active filters in 12-, 14- and 16-bit data acquisition systems. Furthermore, the AD713's low total harmonic distortion (THD) level of 0.0003% and very close matching ac characteristics make it an ideal amplifier for many demanding audio applications.

The AD713 is internally compensated for stable operation at unity gain and is available in seven performance grades. The AD713J and AD713K are rated over the commercial temperature range of 0 to +70°C. The AD713A and AD713B are rated over the industrial temperature of −40°C to +85°C. The AD713S and AD713T are rated over the military temperature range of −55°C to +125°C and are available processed to MIL-STD-883B, Rev. C.

CONNECTION DIAGRAMS

Plastic (N) and Cerdip (Q) Packages

SOIC (R) Package



The AD713 is offered in a 16-pin SOIC, 14-pin plastic DIP and hermetic cerdip package, or in chip form.

PRODUCT HIGHLIGHTS

1. The AD713 is a high speed BiFET op amp that offers excellent performance at competitive prices. It upgrades the performance of circuits using op amps such as the TL074/TL084, LT1058, LF347 and OPA404.
2. Slew rate is 100% tested for a guaranteed minimum of 16V/μs (J, A and S Grades).
3. The combination of Analog Devices' advanced processing technology, laser wafer drift trimming and well-matched ion-implanted JFETs provides outstanding dc precision. Input offset voltage, input bias current and input offset current are specified in the warmed-up condition and are 100% tested.
4. Very close matching of ac characteristics between the four amplifiers makes the AD713 ideal for high quality active filter applications.

AD713—SPECIFICATIONS (@ +25°C and ±15V dc, unless otherwise noted)

Model	Conditions	AD713J/A/S Min	AD713J/A/S Typ	AD713J/A/S Max	AD713K/B/T Min	AD713K/B/T Typ	AD713K/B/T Max	Units
INPUT OFFSET VOLTAGE[1]								
Initial Offset			0.3	**1.5**		0.2	**0.5**	mV
Offset	T_{min} to T_{max}		0.5	2/2/2		0.4	**0.7/0.7/1.0**	mV
vs. Temp.			5			5	**20/20/15**	μV/°C
vs. Supply		**78**	95		**84**	100		dB
vs. Supply	T_{min} to T_{max}	76/76/**76**	95		**84**	100		dB
Long-Term Stability			15			15		μV/month
INPUT BIAS CURRENT[2]								
Either Input	V_{CM}=0V		40	**150**		40	**75**	pA
Either Input @ T_{max} = 70°C/85°C/125°C	V_{CM}=0V			3.4/9.6/154			1.7/4.8/**77**	nA
Either Input	V_{CM}=+10V		55	200		55	**120**	pA
Offset Current	V_{CM}=0V		10	**75**		10	**35**	pA
Offset Current @ T_{max} = 70°C/85°C/125°C	V_{CM}=0V			1.7/4.8/**77**			0.8/2.2/**36**	nA
MATCHING CHARACTERISTICS								
Input Offset Voltage			0.5	**1.8**		0.4	**0.8**	mV
Input Offset Voltage	T_{min} to T_{max}		0.7	2.3/2.3/**2.3**		0.6	**1.0/1.0/1.3**	mV
Input Offset Voltage Drift			8			6	25	μV/°C
Input Bias Current			10	**100**		10	**35**	pA
Crosstalk (See Figure 20)	@ 1kHz			−130			−130	dB
	@ 100kHz			−95			−95	dB
FREQUENCY RESPONSE								
Gain BW, Small Signal	G=−1	3	4		3.4	4		MHz
Full Power Response	V_O=20V p-p		200			200		kHz
Slew Rate, Unity Gain	G=−1	**16**	20		**18**	20		V/μs
Settling Time to 0.01%	G=−1 (Fig. 23)		1	1.2		1	1.2	μs
Total Harmonic Distortion (See Figures 16 and 30)	f=1kHz, Rl≥2kΩ, V_O=3V rms		0.0003			0.0003		%
INPUT IMPEDANCE								
Differential			$3\times10^{12}\|\|5.5$			$3\times10^{12}\|\|5.5$		Ω||pF
Common Mode			$3\times10^{12}\|\|5.5$			$3\times10^{12}\|\|5.5$		Ω||pF
INPUT VOLTAGE RANGE								
Differential[3]			±20			±20		V
Common-Mode Voltage[4]			+14.5, −11.5			+14.5, −11.5		V
T_{min} to T_{max}		−**11**		+13	**−11**		+13	V
Common-Mode Rejection Ratio	V_{CM}=±10V	**78**	88		**84**	94		dB
	T_{min} to T_{max}	76/76/**76**	84		**82**	90		dB
	V_{CM}=±11V	**72**	84		**78**	90		dB
	T_{min} to T_{max}	70/70/**70**	80		**74**	84		dB
INPUT VOLTAGE NOISE	Noise 0.1 to 10Hz		2			2		μV p-p
	f=10Hz		45			45		nV/$\sqrt{Hz}$
	f=100Hz		22			22		nV/$\sqrt{Hz}$
	f=1kHz		18			18		nV/$\sqrt{Hz}$
	f=10kHz		16			16		nV/$\sqrt{Hz}$
INPUT CURRENT NOISE	f=1kHz		0.01			0.01		pA/$\sqrt{Hz}$
OPEN LOOP GAIN	V_O=±10V							
	R_{LOAD}≥2kΩ	**150**	400		**200**	400		V/mV
	T_{min} to T_{max}	100/100/**100**			**100**			V/mV
OUTPUT CHARACTERISTICS								
Voltage	R_{LOAD}≥2kΩ	**+13, −12.5**	+13.9, −13.3		**+13, −12.5**	+13.9, −13.3		V
	T_{min} to T_{max}	±12/±12/**±12**	+13.8, −13.1		**±12**	+13.8, −13.1		V
Current	Short Circuit		25			25		mA

Model	Conditions	AD713J/A/S Min	AD713J/A/S Typ	AD713J/A/S Max	AD713K/B/T Min	AD713K/B/T Typ	AD713K/B/T Max	Units
POWER SUPPLY								
Rated Performance			±15			±15		V
Operating Range		±4.5		±18	±4.5		±18	V
Quiescent Current			10.0	13.5		10.0	12.0	mA
TRANSISTOR COUNT	# of Transistors		120			120		

NOTES
[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[2]Bias Current Specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperature, the current doubles every 10°C.
[3]Defined as voltage between inputs, such that neither exceeds ±10V from ground.
[4]Typically exceeding −14.1V negative common-mode voltage on either input results in an output phase reversal.

Specifications subject to change without notice.
All min and max specifications are guaranteed.
Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

2

ABSOLUTE MAXIMUM RATINGS[1, 2]

Supply Voltage . . . . . ±18V
Internal Power Dissipation[2]
Input Voltage[3] . . . . . ±18V
Output Short Circuit Duration
(For One Amplifier) . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range (Q) . . . . . −65°C to +150°C
Storage Temperature Range (N, R) . . . . . −65°C to +125°C
Operating Temperature Range
AD713J/K . . . . . 0 to +70°C
AD713A/B . . . . . −40°C to +85°C
AD713S/T . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Thermal characteristics:
14-pin plastic package: θ_{JA} = 100°C/W, θ_{JC} = 30°C/W
14-pin cerdip package: θ_{JA} = 110°C/W; θ_{JC} = 30°C/W.
16-pin SOIC package: θ_{JA} = 100°C/W; θ_{JC} = 30°C/W.
[3]For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.

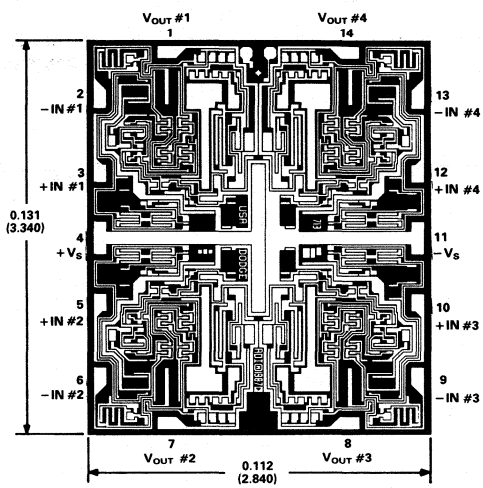
ORDERING GUIDE

Model	Temperature Range	Description	Package Option*
AD713JN	Commercial 0°C to +70°C	14-Pin Plastic Mini-DIP	N-14
AD713JR	Commercial 0°C to +70°C	16-Pin Plastic SOIC	R-16
AD713KN	Commercial 0°C to +70°C	14-Pin Plastic Mini-DIP	N-14
AD713AQ	Industrial −40°C to +85°C	14-Pin Cerdip	Q-14
AD713BQ	Industrial −40°C to +85°C	14-Pin Cerdip	Q-14
AD713SQ	Military −55°C to +125°C	14-Pin Cerdip	Q-14
AD713SQ/883B	Military −55°C to +125°C	14-Pin Cerdip	Q-14
AD713TQ	Military −55°C to +125°C	14-Pin Cerdip	Q-14
AD713TQ/883B	Military −55°C to +125°C	14-Pin Cerdip	Q-14
AD713JR-REEL	Commercial 0°C to +70°C	Tape and Reel	
AD713J Chips	Commercial 0°C to +70°C	Die	
AD713S Chips	Military −55°C to +125°C	Die	

*N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



AD713—Typical Characteristics

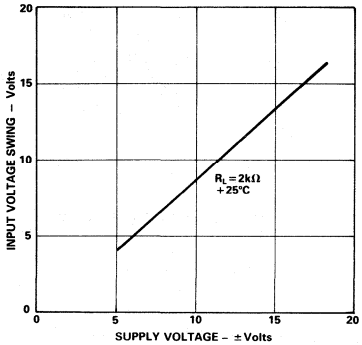


Figure 1. Input Voltage Swing vs. Supply Voltage

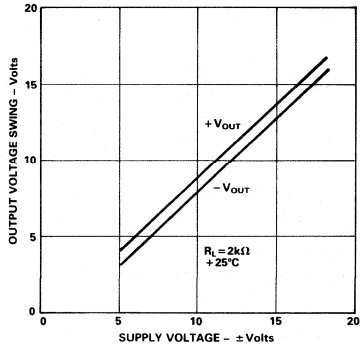


Figure 2. Output Voltage Swing vs. Supply Voltage

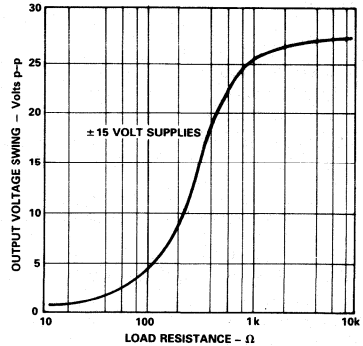


Figure 3. Output Voltage Swing vs. Load Resistance

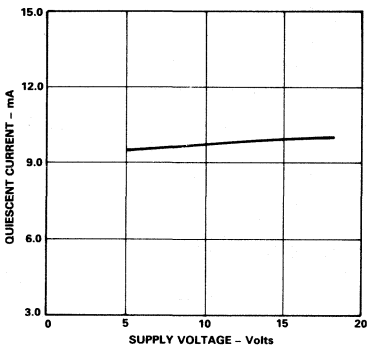


Figure 4. Quiescent Current vs. Supply Voltage

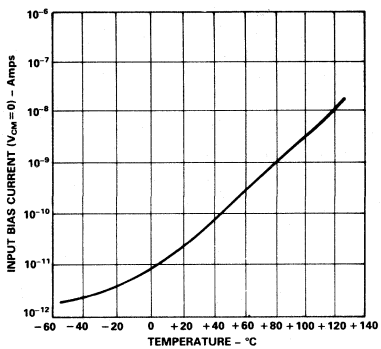


Figure 5. Input Bias Current vs. Temperature

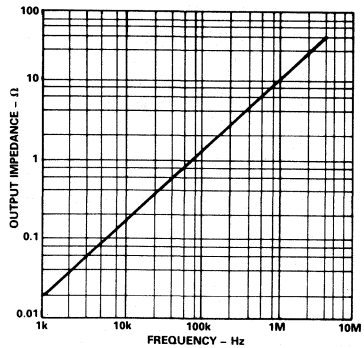


Figure 6. Output Impedance vs. Frequency, G = 1

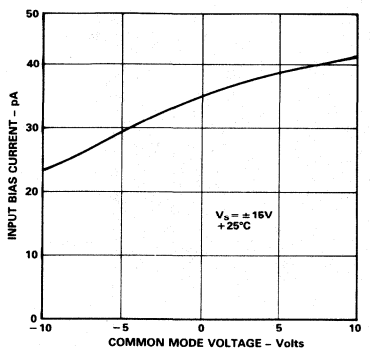


Figure 7. Input Bias Current vs. Common Mode Voltage

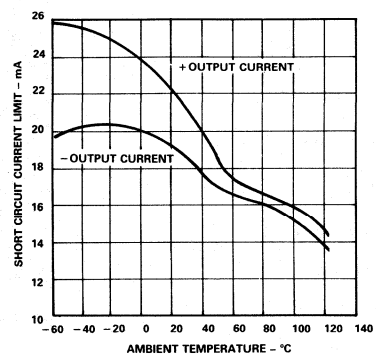


Figure 8. Short Circuit Current Limit vs. Temperature

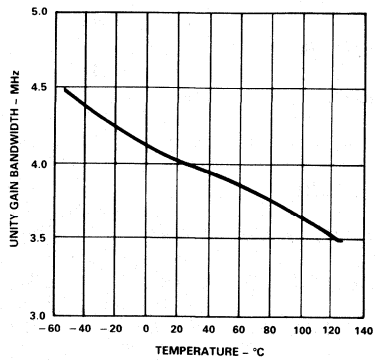


Figure 9. Gain Bandwidth Product vs. Temperature

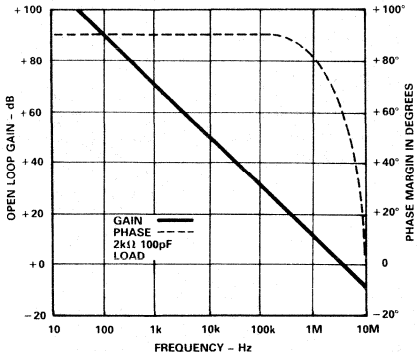


Figure 10. Open Loop Gain and Phase Margin vs. Frequency

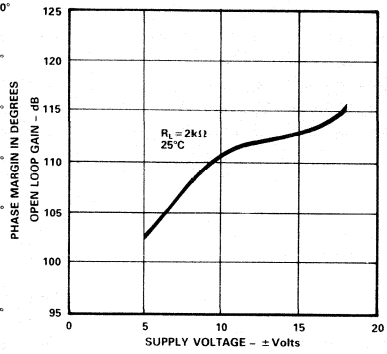


Figure 11. Open Loop Gain vs. Supply Voltage

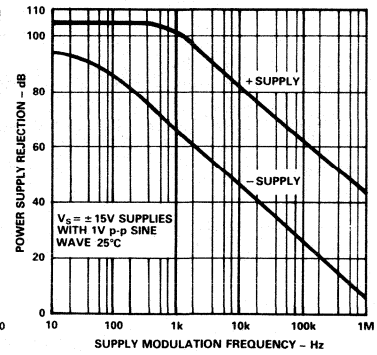


Figure 12. Power Supply Rejection vs. Frequency

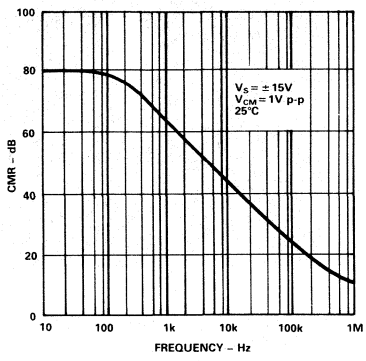


Figure 13. Common Mode Rejection vs. Frequency

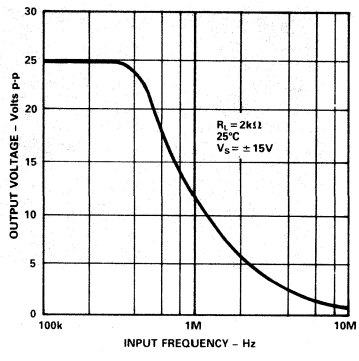


Figure 14. Large Signal Frequency Response

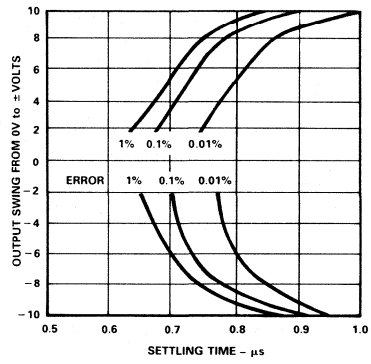


Figure 15. Output Swing and Error vs. Settling Time

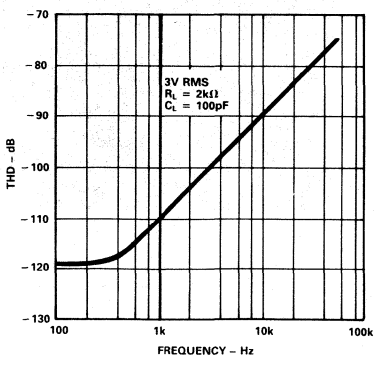


Figure 16. Total Harmonic Distortion vs. Frequency

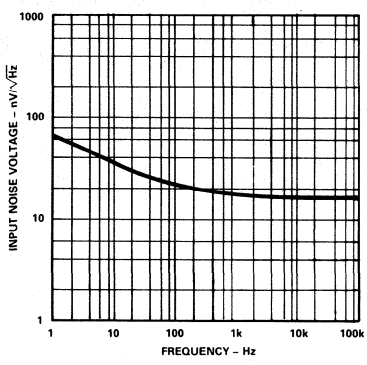


Figure 17. Input Noise Voltage Spectral Density

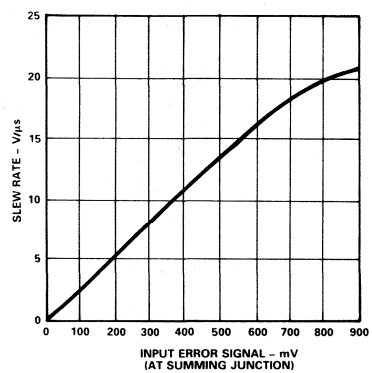
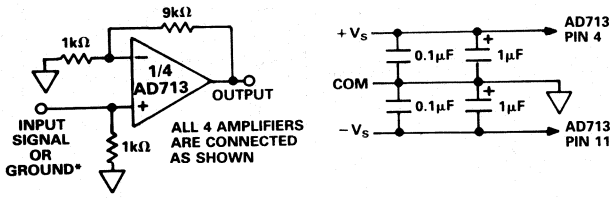


Figure 18. Slew Rate vs. Input Error Signal



*THE SIGNAL INPUT (1kHz SINEWAVE, 2V p-p) IS APPLIED TO ONE AMPLIFIER AT A TIME. THE OUTPUTS OF THE OTHER THREE AMPLIFIERS ARE THEN MEASURED FOR CROSSTALK.

Figure 19. Crosstalk Test Circuit

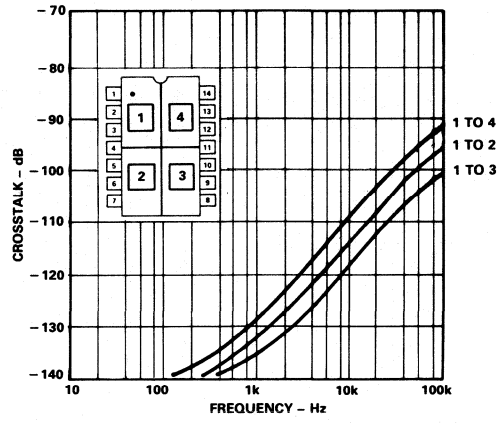


Figure 20. Crosstalk vs. Frequency

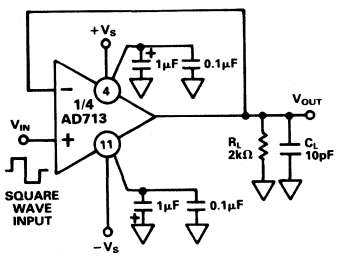


Figure 21a. Unity Gain Follower

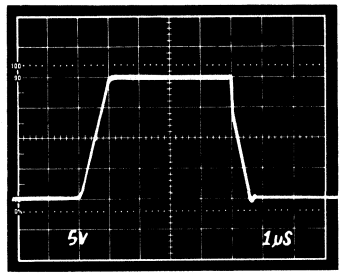


Figure 21b. Unity Gain Follower Large Signal Pulse Response

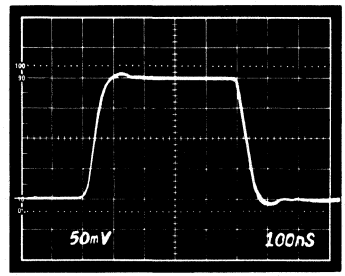


Figure 21c. Unity Gain Follower Small Signal Pulse Response

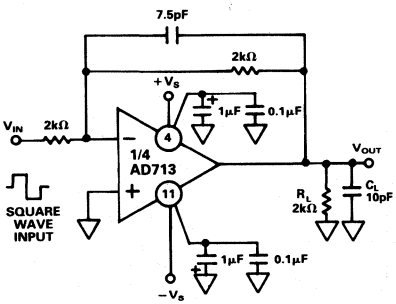


Figure 22a. Unity Gain Inverter

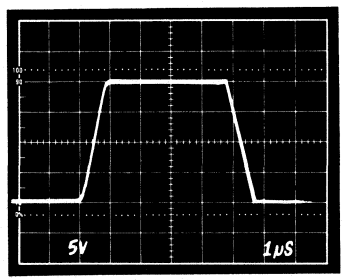


Figure 22b. Unity Gain Inverter Large Signal Pulse Response

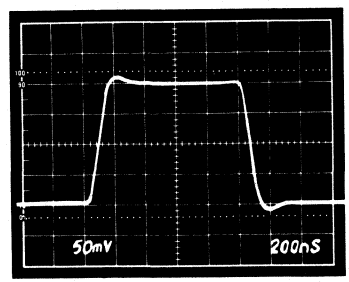


Figure 22c. Unity Gain Inverter Small Signal Pulse Response

MEASURING AD713 SETTLING TIME

The photos of Figures 24 and 25 show the dynamic response of the AD713 while operating in the settling time test circuit of Figure 23. The input of the settling time fixture is driven by a flat-top pulse generator. The error signal output from the false summing node of A1, the AD713 under test, is clamped, amplified by op amp A2 and then clamped again.

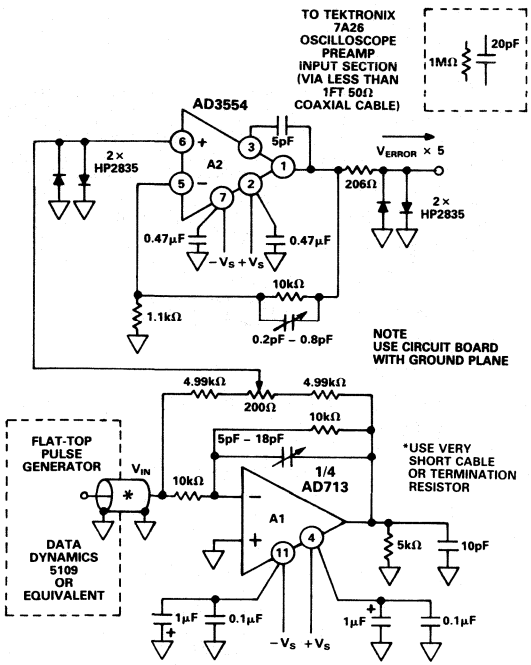


Figure 23. Settling Time Test Circuit

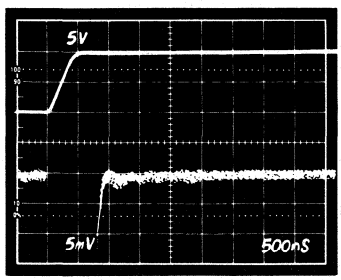


Figure 24. Settling Characteristics 0 to +10V Step. Upper Trace: Output of AD713 Under Test (5V/div). Lower Trace: Amplified Error Voltage (0.01%/div)

The error signal is thus clamped twice: once to prevent overloading amplifier A2 and then a second time to avoid overloading the oscilloscope preamp. A Tektronix oscilloscope preamp type 7A26 was carefully chosen because it recovers from the approximately 0.4 volt overload quickly enough to allow accurate measurement of the AD713's 1μs settling time. Amplifier A2 is a very high speed FET input op amp; it provides a voltage gain of 10, amplifying the error signal output of the AD713 under test (providing an overall gain of 5).

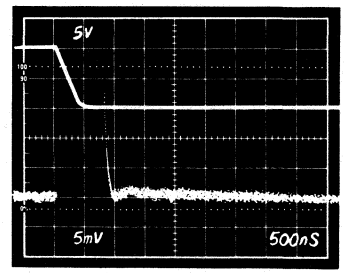


Figure 25. Settling Characteristics to −10V Step. Upper Trace: Output of AD713 Under Test (5V/div). Lower Trace: Amplified Error Voltage (0.01%/div)

POWER SUPPLY BYPASSING

The power supply connections to the AD713 must maintain a low impedance to ground over a bandwidth of 4MHz or more. This is especially important when driving a significant resistive or capacitive load, since all current delivered to the load comes from the power supplies. Multiple high quality bypass capacitors are recommended for each power supply line in any critical application. A 0.1μF ceramic and a 1μF electrolytic capacitor as shown in Figure 26 placed as close as possible to the amplifier (with short lead lengths to power supply common) will assure adequate high frequency bypassing in most applications. A minimum bypass capacitance of 0.1μF should be used for any application.

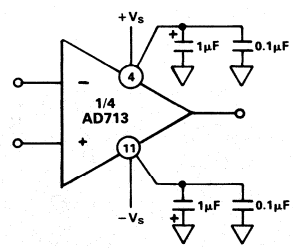


Figure 26. Recommended Power Supply Bypassing

A HIGH SPEED INSTRUMENTATION AMPLIFIER CIRCUIT

The instrumentation amplifier circuit shown in Figure 27 can provide a range of gains from unity up to 1000 and higher using only a single AD713. The circuit bandwidth is 1.2MHz at a gain of 1 and 250kHz at a gain of 10; settling time for the entire circuit is less than 5μs to within 0.01% for a 10 volt step, (G = 10). Other uses for amplifier A4 include an active data guard and an active sense input.

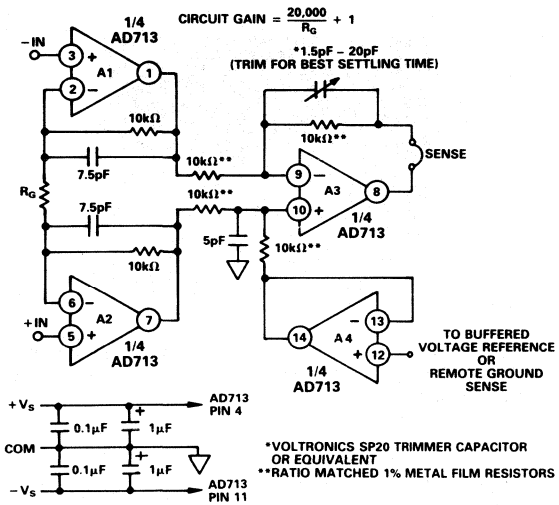


Figure 27. A High Speed Instrumentation Amplifier Circuit

Table I provides a performance summary for this circuit. The photo of Figure 28 shows the pulse response of this circuit for a gain of 10.

Gain	R_G	Bandwidth	T Settle (0.01%)
1	NC	1.2MHz	2μs
2	20kΩ	1.0MHz	2μs
10	4.04kΩ	0.25MHz	5μs

Table I. Performance Summary for the High Speed Instrumentation Amplifier Circuit

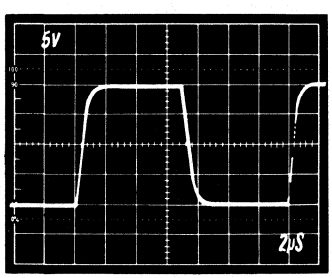


Figure 28. The Pulse Response of the High Speed Instrumentation Amplifier. Gain = 10

A HIGH SPEED FOUR OP AMP CASCADED AMPLIFIER CIRCUIT

Figure 29 shows how the four amplifiers of the AD713 may be connected in cascade to form a high gain, high bandwidth amplifier. This gain of 100 amplifier has a −3dB bandwidth greater than 600kHz.

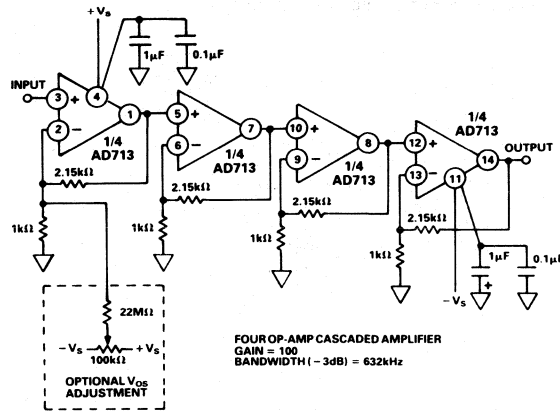


Figure 29. A High Speed Four Op Amp Cascaded Amplifier Circuit

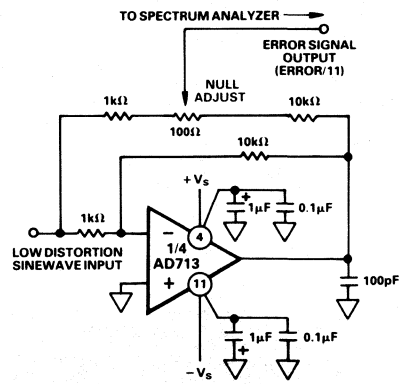


Figure 30. THD Test Circuit

HIGH SPEED OP AMP APPLICATIONS AND TECHNIQUES

DAC Buffers (I-to-V Converters)

The wide input dynamic range of JFET amplifiers makes them ideal for use in both waveform reconstruction and digital-audio-DAC applications. The AD713, in conjunction with the AD1860 DAC, can achieve 0.0016% THD (here at a 4fs or a 176.4kHz update rate) without requiring the use of a deglitcher. Just such a circuit is shown in Figure 31. The 470pF feedback capacitor used with IC2a, along with op amp IC2b and its associated components, together form a 3-pole low-pass filter. Each or all of these poles can be tailored for the desired attenuation and phase characteristics required for a particular application. In this application, one half of an AD713 serves each channel in a two-channel stereo system.

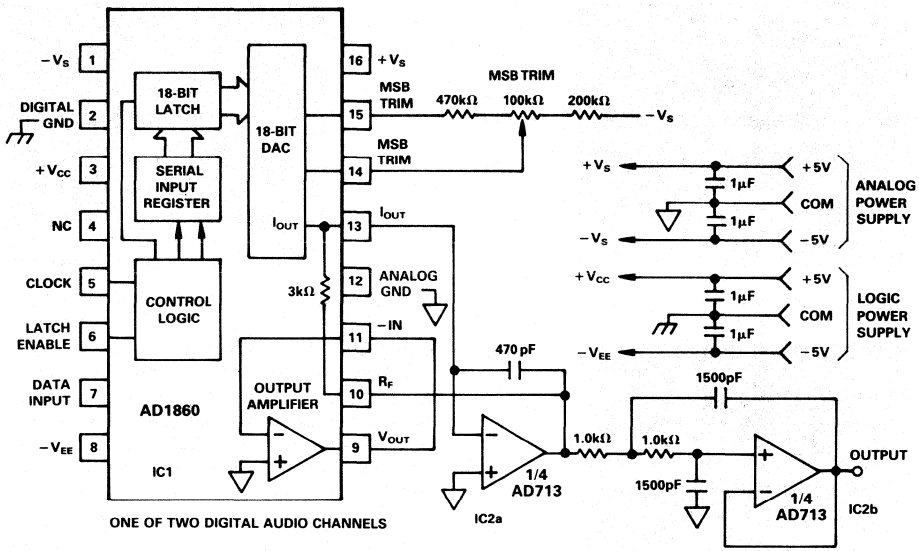


Figure 31. A D/A Converter Circuit for Digital Audio

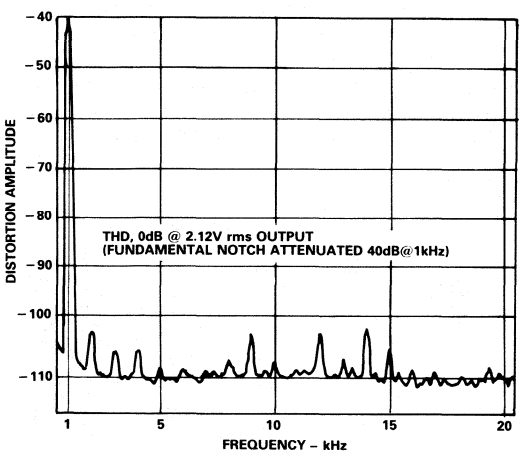


Figure 32. Harmonic Distortion vs. Frequency for the Digital Audio Circuit of Figure 31

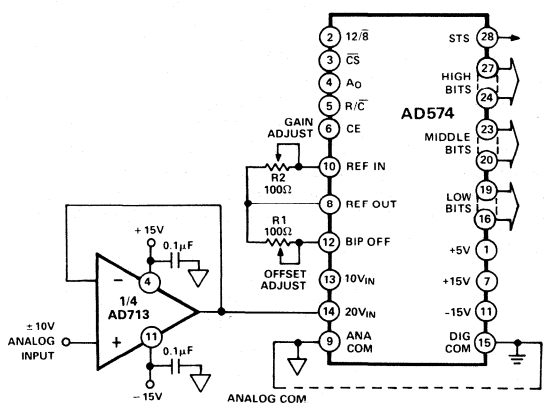


Figure 33. The AD713 as an ADC Buffer

Driving the Analog Input of an A/D Converter

An op amp driving the analog input of an A/D converter, such as that shown in Figure 33, must be capable of maintaining a constant output voltage under dynamically changing load conditions. In successive approximation converters, the input current is compared to a series of switched trial currents. The comparison point is diode clamped but may vary by several hundred millivolts, resulting in high frequency modulation of the A/D input current. The output impedance of a feedback amplifier is made artificially low by its loop gain. At high frequencies, where the loop gain is low, the amplifier output impedance can approach its open loop value.

Most IC amplifiers exhibit a minimum open loop output impedance of 25Ω, due to current limiting resistors. A few hundred microamps reflected from the change in converter loading can introduce errors in instantaneous input voltage. If the A/D conversion speed is not excessive and the bandwidth of the amplifier is sufficient, the amplifier's output will return to the nominal value before the converter makes its comparison. However, many amplifiers have relatively narrow bandwidths, yielding slow recovery from output transients. The AD713 is ideally suited as a driver for A/D converters since it offers both a wide bandwidth and a high open loop gain.

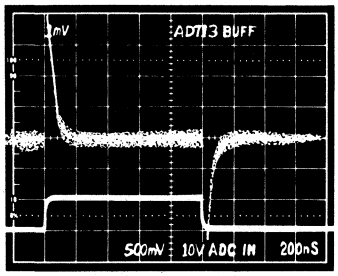


Figure 34. Buffer Recovery Time Source Current = 2mA

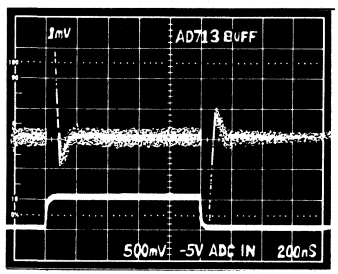


Figure 35. Buffer Recovery Time Sink Current = 1mA

Driving A Large Capacitive Load

The circuit of Figure 36 employs a 100Ω isolation resistor which enables the amplifier to drive capacitive loads exceeding 1500pF; the resistor effectively isolates the high frequency feedback from the load and stabilizes the circuit. Low frequency feedback is returned to the amplifier summing junction via the low pass filter formed by the 100Ω series resistor and the load capacitance, Cl. Figure 37 shows a typical transient response for this connection.

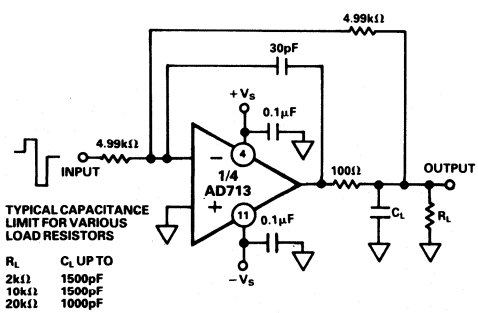


Figure 36. Circuit for Driving a Large Capacitance Load

Trim Resistor	JN/AQ/ SD	KN/BQ/ TD	LN/CQ/ UD	GLN/GCQ/ GUD
R1	500Ω	200Ω	100Ω	20Ω
R2	150Ω	68Ω	33Ω	6.8Ω

Table II. Recommended Trim Resistor Values vs. Grades for AD7545 for V_D = +5V

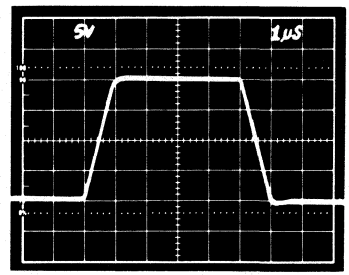


Figure 37. Transient Response, R_L = 2kΩ, C_L = 500pF

CMOS DAC APPLICATIONS

The AD713 is an excellent output amplifier for CMOS DACs. It can be used to perform both 2 and 4 quadrant operation. The output impedance of a DAC using an inverted R-2R ladder approaches R for codes containing many "1"s, 3R for codes containing a single "1" and infinity for codes containing all zeros.

For example, the output resistance of the AD7545 will modulate between 11kΩ and 33kΩ. Therefore, with the DAC's internal feedback resistance of 11kΩ , the noise gain will vary from 2 to 4/3. This changing noise gain modulates the effect of the input offset voltage of the amplifier, resulting in nonlinear DAC-amplifier performance. The AD713, with its guaranteed 1.5mV input offset voltage, minimizes this effect achieving 12-bit performance.

Figures 38 and 39 show the AD713 and a 12-bit CMOS DAC, the AD7545, configured for either a unipolar binary (2-quadrant multiplication) or bipolar (4-quadrant multiplication) operation. Capacitor C1 provides phase compensation which reduces overshoot and ringing.

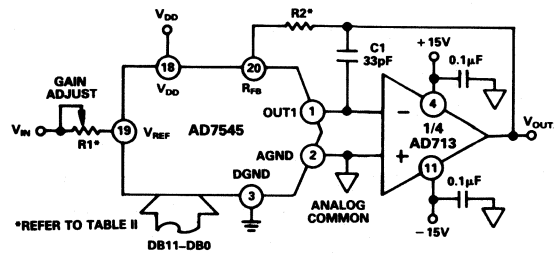


Figure 38. Unipolar Binary Operation

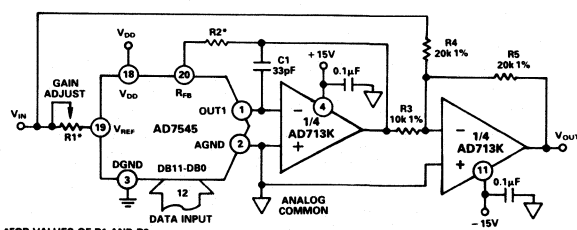
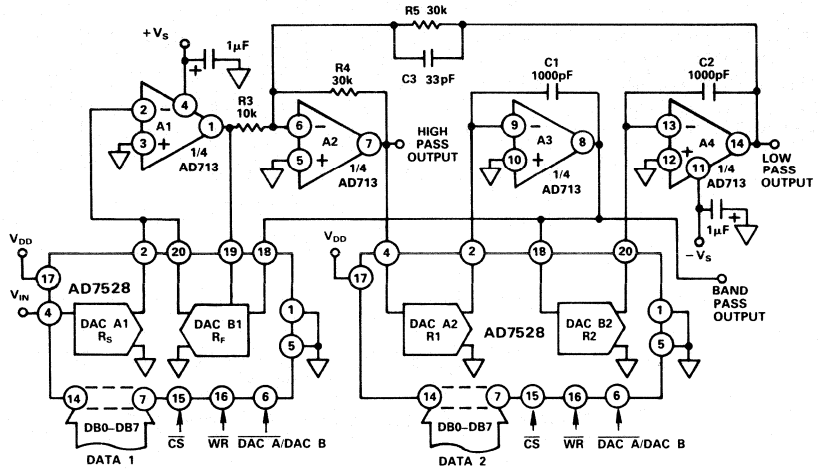


Figure 39. Bipolar Operation



CIRCUIT EQUATIONS

$C_1 = C_2,\ R_1 = R_2,\ R_4 = R_5$

$$f_C = \frac{1}{2\pi R_1 C_1}$$

$$Q = \frac{R_3}{R_4} \cdot \frac{R_F}{R_{FBB1}}$$

$$A_O = -\frac{R_F}{R_S}$$

Note:
DAC equivalent resistance equals
$\frac{256 \times (\text{DAC Ladder resistance})}{\text{DAC Digital Code}}$

Figure 40. A Programmable State Variable Filter Circuit

FILTER APPLICATIONS

A Programmable State Variable Filter

For the state variable or universal filter configuration of Figure 40 to function properly, DACs A1 and B1 need to control the gain and Q of the filter characteristic, while DACs A2 and B2 must accurately track for the simple expression of f_C to be true. This is readily accomplished using two AD7528 DACs and one AD713 quad op amp. Capacitor C3 compensates for the effects of op amp gain-bandwidth limitations.

This filter provides low pass, high pass and band pass outputs and is ideally suited for applications where microprocessor control of filter parameters is required. The programmable range for component values shown is f_C = 0 to 15kHz and Q = 0.3 to 4.5.

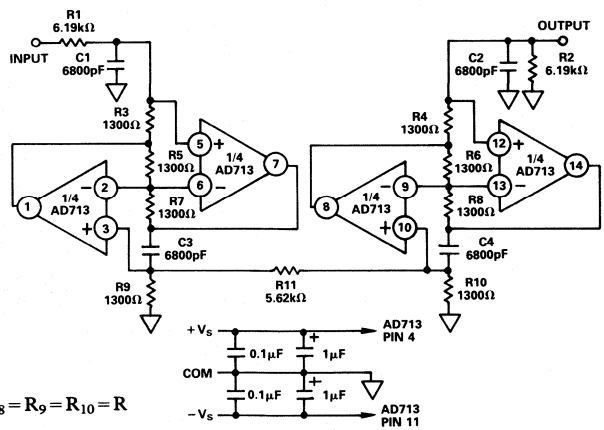
GIC and FDNR FILTER APPLICATIONS

The closely matched and uniform ac characteristics of the AD713 make it ideal for use in GIC (gyrator) and FDNR (frequency dependent negative resistor) filter applications. Figures 41 and 43 show the AD713 used in two typical active filters. The first shows a single AD713 simulating two coupled inductors configured as a one-third octave bandpass filter. A single section of this filter meets ANSI class II specifications and handles a 7.07V rms signal with <0.002% THD (20Hz-20kHz).

Figure 43 shows a 7-pole antialiasing filter for a 2× oversampling (88.2kHz) digital audio application. This filter has <0.05 dB pass band ripple and 19.8 ±0.3µs delay, dc-20kHz and will handle a 5V rms signal (V_S = ±15V) with no overload at any internal nodes.

The filter of Figure 41 can be scaled for any center frequency by using the formula:

$$f_C = \frac{1.11}{2\pi RC}$$



$f_c = \frac{1.11}{2\pi RC}$

$C_1 = C_2 = C_3 = C_4 = C$

$R_1 = R_2 = 4.76R$

$R_{11} = 4.32R$

$R_3 = R_4 = R_5 = R_6 = R_7 = R_8 = R_9 = R_{10} = R$

Figure 41. A 1/3 Octave Filter Circuit

where all resistors and capacitors scale equally. Resistors R3—R8 should not be greater than 2kΩ in value, to prevent parasitic oscillations caused by the amplifier's input capacitance. If this is not practical, small lead capacitances (10-20pF) should be added across R5 and R6. Figures 42 and 44 show the output amplitude vs. frequency of these filters.

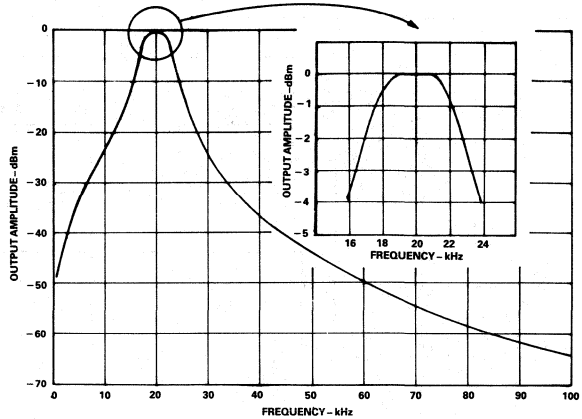


Figure 42. Output Amplitude vs. Frequency of 1/3 Octave Filter

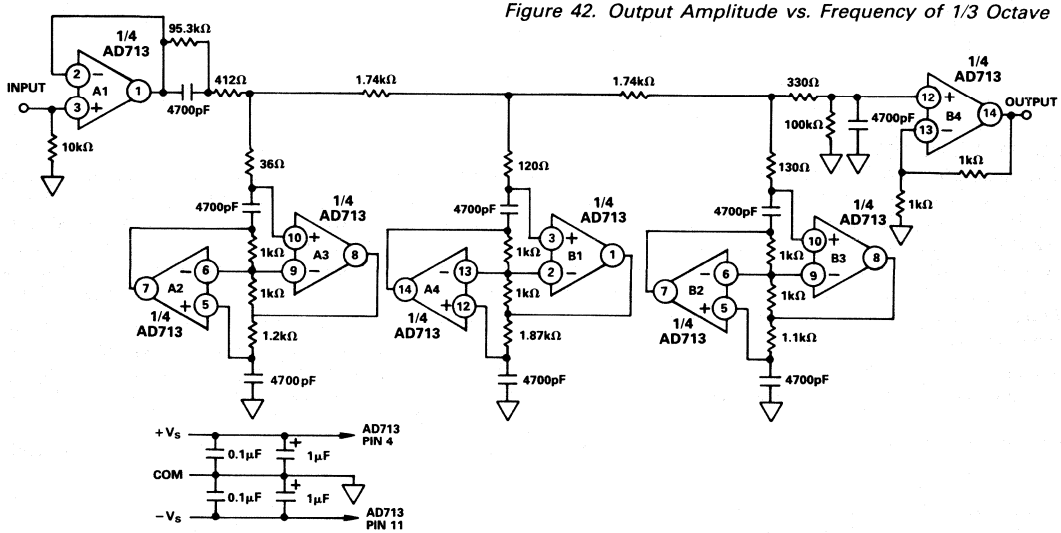


Figure 43. An Antialiasing Filter

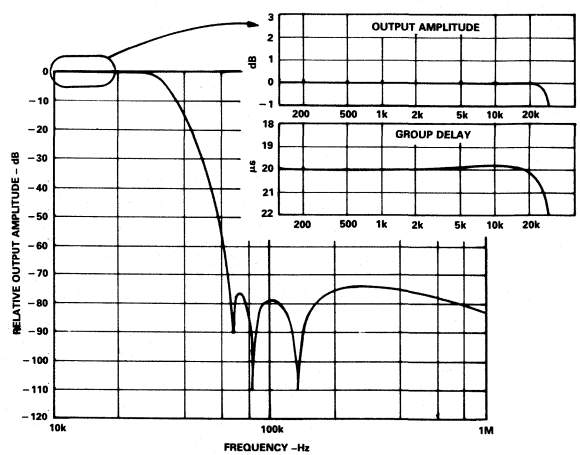


Figure 44. Relative Output Amplitude vs. Frequency of Antialiasing Filter

ANALOG DEVICES

Low Cost, High Accuracy IC Op Amps

AD741 Series

FEATURES

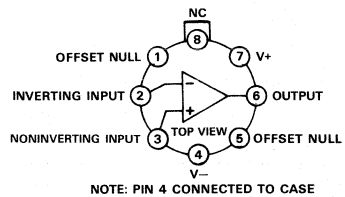
Precision Input Characteristics
- Low V_{OS}: 0.5 mV max (L)
- Low V_{OS} Drift: 5 μV/°C max (L)
- Low I_b: 50 nA max (L)
- Low I_{OS}: 5 nA max (L)
- High CMRR: 90 dB min (K, L)

High Output Capability
- A_{OL} = 25,000 min, 1 kΩ Load (J, S)
  T_{min} to T_{max}
- V_O = ±10 V min, 1 kΩ Load (J, S)

Chips and MIL-STD-883B Parts Available

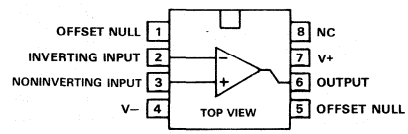
FUNCTIONAL BLOCK DIAGRAMS

TO-99 (H) Package



NOTE: PIN 4 CONNECTED TO CASE

Mini-DIP (N) Package



GENERAL DESCRIPTION

The Analog Devices AD741 Series are high performance monolithic operational amplifiers. All the devices feature full short circuit protection and internal compensation.

The Analog Devices AD741J, AD741K, AD741L, and AD741S are specially tested and selected versions of the standard AD741 operational amplifier. Improved processing and additional electrical testing guarantee the user precision performance at a very-low cost. The AD741J, K and L substantially increase overall accuracy over the standard AD741C by providing maximum limits on offset voltage drift and significantly reducing the errors due to offset voltage, bias current, offset current, voltage gain, power supply rejection, and common-mode rejection. For example, the AD741L features maximum offset voltage drift of 5 μV/°C, offset voltage of 0.5 mV max, offset current of 5 nA max, bias current of 50 nA max, and a CMRR of 90 dB min. The AD741S offers guaranteed performance over the extended temperature range of −55°C to +125°C, with max offset voltage drift of 15 μV/°C, max offset voltage of 4 mV, max offset current of 25 nA, and a minimum CMRR of 80 dB.

HIGH OUTPUT CAPABILITY

Both the AD741J and AD741S offer the user the additional advantages of high guaranteed output current and gain at low values of load impedance. The AD741J guarantees a minimum gain of 25,000 swinging ±10 V into a 1 kΩ load from 0 to +70°C. The AD741S guarantees a minimum gain of 25,000 swinging ±10 V into a 1 kΩ load from −55°C to +125°C.

All devices feature full short circuit protection, high gain, high common-mode range, and internal compensation. The AD741J, K and L are specified for operation from 0 to +70°C, and are available in both the TO-99 and mini-DIP packages. The AD741S is specified for operation from −55°C to +125°C, and is available in the TO-99 package.

AD741 Series—SPECIFICATIONS (typical @ +25°C and ±15 V dc, unless otherwise specified)

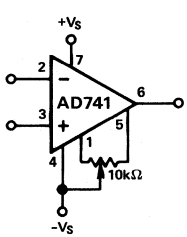
Model	AD741C Min	AD741C Typ	AD741C Max	AD741 Min	AD741 Typ	AD741 Max	AD741J Min	AD741J Typ	AD741J Max	Units
OPEN-LOOP GAIN										
R_L = 1 kΩ, V_O = ±10 V							**50,000**	200,000		V/V
R_L = 2 kΩ, V_O = ±10 V	**20,000**	200,000		**50,000**	200,000					V/V
T_A = min to max R_L = 2 kΩ	**15,000**			**25,000**			**25,000**			V/V
OUTPUT CHARACTERISTICS										
Voltage @ R_L = 1 kΩ, T_A = min to max							**±10**	±13		V
Voltage @ R_L = 2 kΩ, T_A = min to max	**±10**	±13		**±10**	±13					V
Short Circuit Current		25			25			25		mA
FREQUENCY RESPONSE										
Unity Gain, Small Signal		1			1			1		MHz
Full Power Response		10			10			10		kHz
Slew Rate		0.5			0.5			0.5		V/μs
Transient Response (Unity Gain)										
Rise Time $C_L \leq$ 10 V p–p		0.3			0.3			0.3		μs
Overshoot		5.0			5.0			5.0		%
INPUT OFFSET VOLTAGE										
Initial, $R_S \leq$ 10 kΩ, Adjust to Zero		1.0	**6.0**		1.0	**5.0**		1.0	**3.0**	mV
T_A = min to max		1.0	**7.5**		1.0	**6.0**			**4.0**	mV
Average vs. Temperature (Untrimmed)									20	μV/°C
vs. Supply, T_A = min to max								30	100	μV/V
INPUT OFFSET CURRENT										
Initial		20	**200**		20	**200**		5	**50**	nA
T_A = min to max		40	**300**		85	500			**100**	nA
Average vs. Temperature								0.1		nA/°C
INPUT BIAS CURRENT										
Initial		80	**500**		80	**500**		40	**200**	nA
T_A = min to max		120	**800**		300	1,500			**400**	nA
Average vs. Temperature								0.6		nA/°C
INPUT IMPEDANCE DIFFERENTIAL	0.3	2.0		0.3	2.0			1.0		MΩ
INPUT VOLTAGE RANGE[1]										
Differential, max Safe									±30	V
Common-Mode, max Safe	±12	±13		±12	±13			±15		V
Common-Mode Rejection,										
R_S = ≤ 10 kΩ, T_A = min to max,										
V_{IN} = ±12 V	**70**	90		**70**	90		**80**	90		dB
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating							±5		±18	V
Power Supply Rejection Ratio		30	**150**		30	**150**				μV/V
Quiescent Current		1.7	**2.8**		1.7	**2.8**		2.2	**3.3**	mA
Power Consumption		50	85		50	85		50	85	mW
T_A = min					60	100				mW
T_A = max					45	75				mW
TEMPERATURE RANGE										
Operating Rated Performance	0		+70	−55		+125	0		+70	°C
Storage	−65		+150	−65		+150	−65		+150	°C

NOTES

[1]For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

Specifications subject to change without notice.

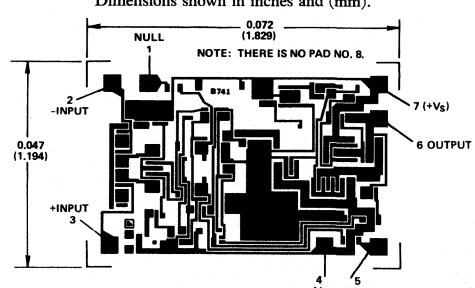
All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.



Standard Nulling Offset Circuit

METALIZATION PHOTOGRAPH

All versions of the AD741 are available in chip form.
Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-99 8 PIN METAL PACKAGE.

Model	AD741K Min	AD741K Typ	AD741K Max	AD741L Min	AD741L Typ	AD741L Max	AD741S Min	AD741S Typ	AD741S Max	Units
OPEN-LOOP GAIN										
R_L = 1 kΩ, V_O = ±10 V							**50,000**	200,000		V/V
R_L = 2 kΩ, V_O = ±10 V	**50,000**	200,000		**50,000**	200,000					V/V
T_A = min to max R_L = 2 kΩ	**25,000**			**25,000**			**25,000**			V/V
OUTPUT CHARACTERISTICS										
Voltage @ R_L = 1 kΩ, T_A = min to max										
Voltage @ R_L = 2 kΩ, T_A = min to max	**±10**	±13		**±10**	±13		+10	+13		V
Short Circuit Current		25			25			25		mA
FREQUENCY RESPONSE										
Unity Gain, Small Signal		1			1			1		MHz
Full Power Response		10			10			10		kHz
Slew Rate		0.5			0.5			0.5		V/μs
Transient Response (Unity Gain)										
Rise Time		0.3			0.3			0.3		μs
Overshoot		5.0			5.0			5.0		%
INPUT OFFSET VOLTAGE										
Initial, $R_S \leq$ 10 kΩ, Adjust to Zero		0.5	**2.0**		0.2	**0.5**		1.0	**2**	mV
T_A = min to max			**3.0**			**1.0**			**4**	mV
Average vs. Temperature (Untrimmed)		6.0	15.0		2.0	5.0		6.0	15.0	μV/°C
vs. Supply, T_A = min to max		5	15.0		5	15.0		30	100	μV/V
INPUT OFFSET CURRENT										
Initial		2	**10**		2	**5**		2	**10**	nA
T_A = min to max			**15**			**10**			**25**	nA
Average vs. Temperature		0.02	0.02		0.02	0.1		0.1	0.25	nA/°C
INPUT BIAS CURRENT										
Initial		30	**75**		30	**50**		30	**75**	nA
T_A = min to max			**120**			**100**			**250**	nA
Average vs. Temperature		0.6	1.5		0.6	1.0		0.6	2.0	nA/°C
INPUT IMPEDANCE DIFFERENTIAL		2			2			2		MΩ
INPUT VOLTAGE RANGE[1]										
Differential, max Safe		±30			±30			±30		V
Common-Mode, max Safe		±15			±15			±15		V
Common-Mode Rejection,										
R_S = ≤ 10 kΩ, T_A = min to max,										
V_{IN} = ±12 V	**90**	100		**90**	100		**90**	100		dB
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating	±5		±22	±5		±22	±5		±22	V
Power Supply Rejection Ratio		20			20			20		μV/V
Quiescent Current		1.7	**2.8**		1.7	**2.8**		2.0	**2.8**	mA
Power Consumption		50	85		50	85		50	85	mW
T_A = min								60	100	mW
T_A = max								75	115	mW
TEMPERATURE RANGE										
Operating Rated Performance	0		+70	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	°C

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings	AD741, J, K, L, S	AD741C
Supply Voltage	±22 V	±18 V
Internal Power Dissipation	500 mW[1]	500 mW
Differential Input Voltage	±30 V	±30 V
Input Voltage	±15 V	± 15 V
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	+300°C	+300°C
Output Short Circuit Duration	Indefinite[2]	Indefinite

NOTES
[1]Rating applies for case temperature to +125°C. Derate TO-99 linearity at 6.5 mW/°C for ambient temperatures above +70°C.
[2]Rating applies for shorts to ground or either supply at case temperatures to +125°C or ambient temperatures to +75°C.

ORDERING GUIDE

Model[1]	Temperature Range	Initial Off Set Voltage	Package Description	Package Option[2]
AD741CN	0 to +70°C	6.0 mV	Mini-DIP	(N-8)
AD741CH	0 to +70°C	6.0 mV	TO-99	(H-08A)
AD741JN	0 to +70°C	3.0 mV	Mini-DIP	(N-8)
AD741JH	0 to +70°C	3.0 mV	TO-99	(H-08A)
AD741KN	0 to +70°C	2.0 mV	Mini-DIP	(N-8)
AD741KH	0 to +70°C	2.0 mV	TO-99	(H-08A)
AD741LN	0 to +70°C	0.5 mV	Mini-DIP	(N-8)
AD741LH	0 to +70°C	0.5 mV	TO-99	(H-08A)
AD741H	−55°C to +125°C	5.0 mV	TO-99	(H-08A)
AD741SH	−55°C to +125°C	2.0 mV	TO-99	(H-08A)

NOTES
[1]J, K and S grade chips also available.
[2]For outline information see Package Information section.

AD741 Series—Typical Performance Curves

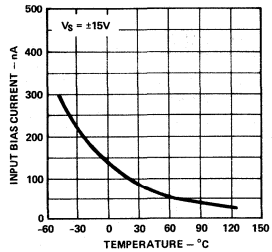


Figure 1. Input Bias Current vs. Temperature

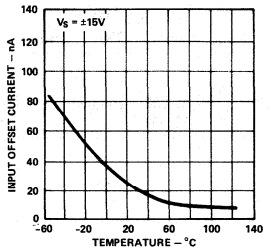


Figure 2. Input Offset Current vs. Temperature

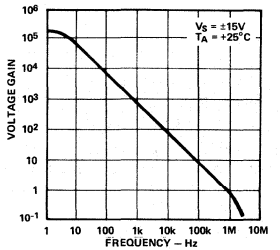


Figure 3. Open-Loop Gain vs. Frequency

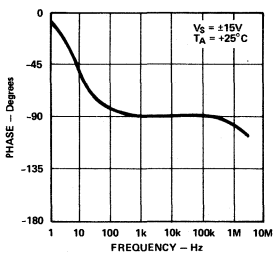


Figure 4. Open-Loop Phase Response vs. Frequency

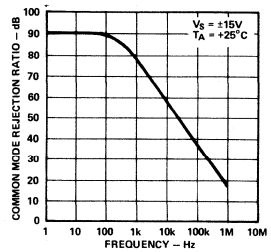


Figure 5. Common-Mode Rejection vs. Frequency

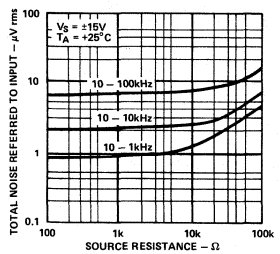


Figure 6. Broad Band Noise vs. Source Resistance

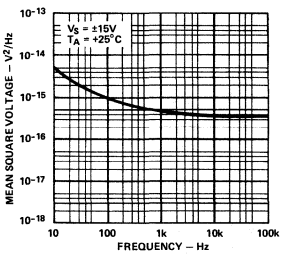


Figure 7. Input Noise Voltage vs. Frequency

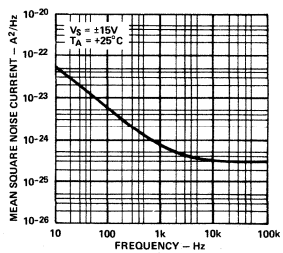


Figure 8. Input Noise Current vs. Frequency

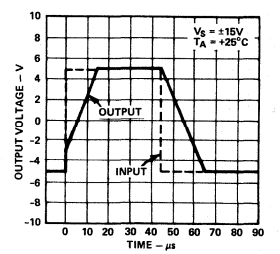


Figure 9. Voltage Follower Large Signal Pulse Response

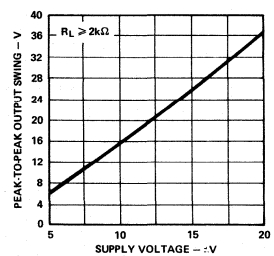


Figure 10. Output Voltage Swing vs. Supply Voltage

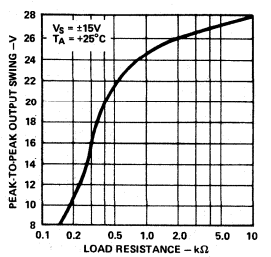


Figure 11. Output Voltage Swing vs. Load Resistance

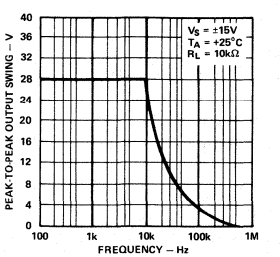


Figure 12. Output Voltage Swing vs. Frequency

ANALOG DEVICES

Ultralow Noise BiFET Op Amp

AD743

FEATURES

ULTRALOW NOISE PERFORMANCE
- 2.9 nV/$\sqrt{Hz}$ at 10 kHz
- 0.38 μV p–p, 0.1 to 10 Hz
- 6.9 fA/$\sqrt{Hz}$ Current Noise at 1 kHz

EXCELLENT DC PERFORMANCE
- 0.5 mV max Offset Voltage
- 250 pA max Input Bias Current
- 1000 V/mV min Open-Loop Gain

AC PERFORMANCE
- 2.8 V/μs Slew Rate
- 4.5 MHz Unity-Gain Bandwidth
- THD = 0.0003% @ 1 kHz
- Available in Tape and Reel in Accordance with EIA-481A Standard

APPLICATIONS
- Sonar Preamplifiers
- High Dynamic Range Filters (>140 dB)
- Photodiode and IR Detector Amplifiers
- Accelerometers

PRODUCT DESCRIPTION

The AD743 is an ultralow noise precision, FET input, monolithic operational amplifier. It offers a combination of the ultralow voltage noise generally associated with bipolar input op amps and the very low input current of a FET-input device. Furthermore, the AD743 does not exhibit an output phase reversal when the negative common-mode voltage limit is exceeded.

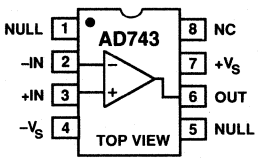
The AD743's guaranteed, maximum input voltage noise of 4.0 nV/$\sqrt{Hz}$ at 10 kHz is unsurpassed for a FET-input monolithic op amp, as is the maximum 1.0 μV p–p, 0.1 to 10 Hz noise. The AD743 also has excellent dc performance with 250 pA maximum input bias current and 0.5 mV maximum offset voltage.

The AD743 is specifically designed for use as a preamp in capacitive sensors, such as ceramic hydrophones. It is available in five performance grades. The AD743J and AD743K are rated over the commercial temperature range of 0°C to +70°C. The AD743A and AD743B are rated over the industrial temperature range of −40°C to +85°C. The AD743S is rated over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

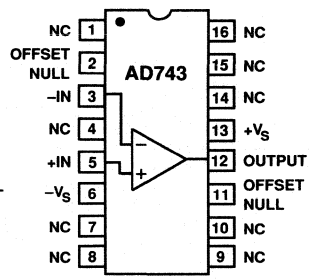
The AD743 is available in 8-pin plastic mini-DIP, 8-pin cerdip, 16-pin SOIC, or in chip form.

CONNECTION DIAGRAMS

8-Pin Plastic Mini-DIP (N) and 8-Pin Cerdip (Q) Packages

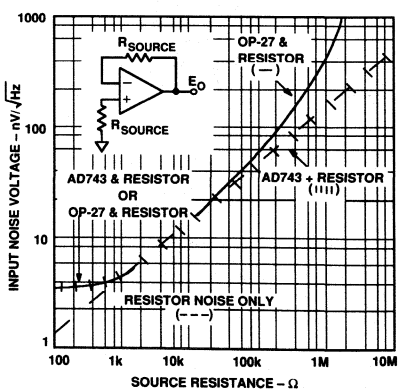


16-Pin SOIC (R) Package



PRODUCT HIGHLIGHTS

1. The low offset voltage and low input offset voltage drift of the AD743 coupled with its ultralow noise performance mean that the AD743 can be used for upgrading many applications now using bipolar amplifiers.
2. The combination of low voltage and low current noise make the AD743 ideal for charge sensitive applications such as accelerometers and hydrophones.
3. The low input offset voltage and low noise level of the AD743 provide >140 dB dynamic range.
4. The typical 10 kHz noise level of 2.9 nV/$\sqrt{Hz}$ permits a three op amp instrumentation amplifier, using three AD743s, to be built which exhibits less than 4.2 nV/$\sqrt{Hz}$ noise at 10 kHz and which has low input bias currents.



Input Noise Voltage vs. Source Resistance

AD743—SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD743J/A Min	AD743J/A Typ	AD743J/A Max	AD743K/B Min	AD743K/B Typ	AD743K/B Max	AD743S Min	AD743S Typ	AD743S Max	Units
INPUT OFFSET VOLTAGE[1]											
Initial Offset			0.25	1.0/0.8		0.1	0.5/0.25		0.25	1.0	mV
Initial Offset	T_{min} to T_{max}			1.5			1.0/0.50			2.0	mV
vs. Temp.	T_{min} to T_{max}		2			1			2		μV/°C
vs. Supply (PSRR)	12 V to 18 V[2]	90	96		100	106		90	96		dB
vs. Supply (PSRR)	T_{min} to T_{max}	88			98	100		88			dB
INPUT BIAS CURRENT[3]											
Either Input	V_{CM} = 0 V		150	400		150	250		150	400	pA
Either Input @ T_{max}	V_{CM} = 0 V			8.8/25.6			5.5/16			413	nA
Either Input	V_{CM} = +10 V		250	600		250	400		300	600	pA
Either Input, V_S = ±5 V	V_{CM} = 0 V		30	200		30	125		30	200	pA
INPUT OFFSET CURRENT	V_{CM} = 0 V		40	150		30	75		40	150	pA
Offset Current @ T_{max}	V_{CM} = 0 V			2.2/6.4			1.1/3.2			102	nA
FREQUENCY RESPONSE											
Gain BW, Small Signal	G = −1		4.5			4.5			4.5		MHz
Full Power Response	V_O = 20 V p-p		25			25			25		kHz
Slew Rate, Unity Gain	G = −1		2.8			2.8			2.8		V/μs
Settling Time to 0.01%			6			6			6		μs
Total Harmonic Distortion[4] (Fig. 16)	f = 1 kHz G = −1		0.0003			0.0003			0.0003		%
INPUT IMPEDANCE											
Differential			$1 \times 10^{10}\|\|20$			$1 \times 10^{10}\|\|20$			$1 \times 10^{10}\|\|20$		Ω||pF
Common Mode			$3 \times 10^{11}\|\|18$			$3 \times 10^{11}\|\|18$			$3 \times 10^{11}\|\|18$		Ω||pF
INPUT VOLTAGE RANGE											
Differential[5]			±20			±20			±20		V
Common-Mode Voltage			+13.3, −10.7			+13.3, −10.7			+13.3, −10.7		V
Over Max Operating Range[6]		−10		+12	−10		+12	−10		+12	V
Common-Mode Rejection Ratio	V_{CM} = ±10 V	80	95		90	102		80	95		dB
	T_{min} to T_{max}	78			88			78			dB
INPUT VOLTAGE NOISE	0.1 to 10 Hz		0.38			0.38	1.0		0.38		μV p-p
	f = 10 Hz		5.5			5.5	10.0		5.5		$nV/\sqrt{Hz}$
	f = 100 Hz		3.6			3.6	6.0		3.6		$nV/\sqrt{Hz}$
	f = 1 kHz		3.2	5.0		3.2	5.0		3.2	5.0	$nV/\sqrt{Hz}$
	f = 10 kHz		2.9	4.0		2.9	4.0		2.9	4.0	$nV/\sqrt{Hz}$
INPUT CURRENT NOISE	f = 1 kHz		6.9			6.9			6.9		$fA/\sqrt{Hz}$
OPEN LOOP GAIN	V_O = ±10 V										
	$R_{LOAD} \geq$ 2 kΩ	1000	4000		2000	4000		1000	4000		V/mV
	T_{min} to T_{max}	800			1800			800			V/mV
	R_{LOAD} = 600 Ω		1200			1200			1200		V/mV
OUTPUT CHARACTERISTICS											
Voltage	$R_{LOAD} \geq$ 600 Ω	+13, −12			+13, −12			+13, −12			V
	$R_{LOAD} \geq$ 600 Ω		+13.6, −12.6			+13.6, −12.6			+13.6, −12.6		V
	T_{min} to T_{max}	+12, −10			+12, −10			+12, −10			V
	$R_{LOAD} \geq$ 2 kΩ	±12	+13.8, −13.1		±12	+13.8, −13.1		±12	+13.8, −13.1		V
Current	Short Circuit	20	40		20	40		20	40		mA
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		±4.8		±18	±4.8		±18	±4.8		±18	V
Quiescent Current			8.1	10.0		8.1	10.0		8.1	10.0	mA
TRANSISTOR COUNT	# of Transistors		50			50			50		

NOTES
[1]Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[2]Test conditions: $+V_S$ = 15 V, $-V_S$ = 12 V to 18 V and $+V_S$ = 12 V to +18 V, $-V_S$ = 15 V.
[3]Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperature, the current doubles every 10°C.
[4]Gain = −1, R_L = 2 kΩ, C_L = 10 pF.
[5]Defined as voltage between inputs, such that neither exceeds ±10 V from common.
[6]The AD743 does not exhibit an output phase reversal when the negative common-mode limit is exceeded.

All min and max specifications are guaranteed.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
Input Voltage . . . . . $\pm V_S$
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range (Q) . . . . . −65°C to +150°C
Storage Temperature Range (N, R) . . . . . −65°C to +125°C
Operating Temperature Range
AD743J/K . . . . . 0°C to +70°C
AD743A/B . . . . . −40°C to +85°C
AD743S . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 seconds) . . . . . 300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-pin plastic package: θ_{JA} = 100°C/Watt, θ_{JC} = 50°C/Watt
8-pin cerdip package: θ_{JA} = 110°C/Watt, θ_{JC} = 30°C/Watt
16-pin plastic SOIC package: θ_{JA} = 100°C/Watt, θ_{JC} = 30°C/Watt

ESD SUSCEPTIBILITY

An ESD classification per method 3015.6 of MIL STD 883C has been performed on the AD743. The AD743 is a class 1 device, passing at 1000 V and failing at 1500 V on null pins 1 and 5, when tested, using an IMCS 5000 automated ESD tester. Pins other than null pins fail at greater than 2500 V.

2

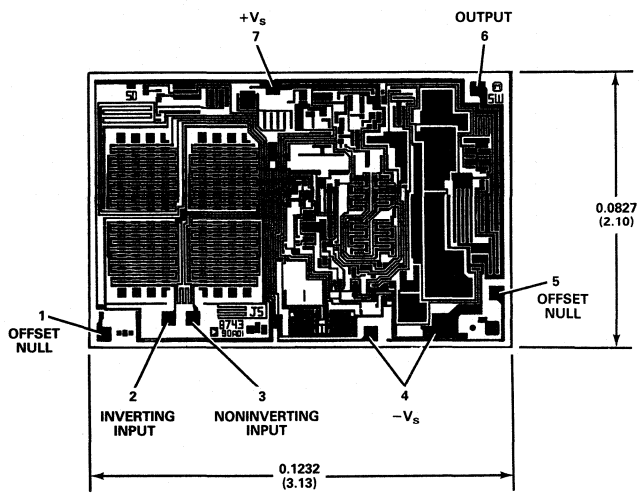
ORDERING GUIDE

Model	Temperature Range	Package Option*
AD743JN	0°C to +70°C	N-8
AD743KN	0°C to +70°C	N-8
AD743AN	−40°C to +85°C	N-8
AD743JR	0°C to +70°C	R-16
AD743KR	0°C to +70°C	R-16
AD743AR	−40°C to +85°C	R-16
AD743AQ	−40°C to +85°C	Q-8
AD743BQ	−40°C to +85°C	Q-8
AD743SQ	−55°C to +125°C	Q-8
AD743SQ/883B	−55°C to +125°C	Q-8
AD743JCHIPS	0°C to +70°C	Die
AD743SCHIPS	−55°C to +125°C	Die
AD743JR-REEL	0°C to +70°C	Tape & Reel
AD743KR-REEL	0°C to +70°C	Tape & Reel
AD743AR-REEL	−40°C to +85°C	Tape & Reel

*N = Plastic DIP; R = Small Outline IC; Q = Cerdip. For outline information see Package Information section.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



AD743—Typical Characteristics (@ +25°C, V_S = +15 V)

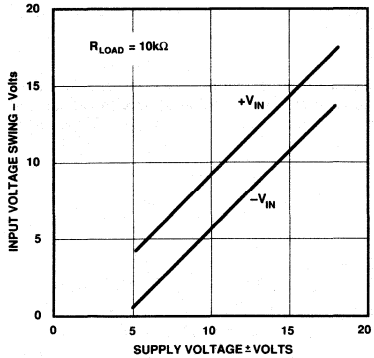


Figure 1. Input Voltage Swing vs. Supply Voltage

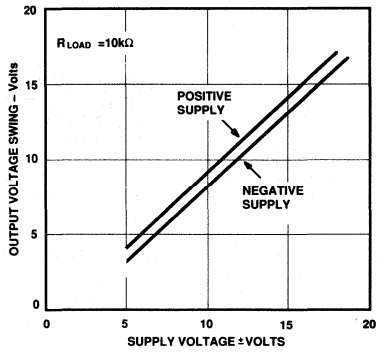


Figure 2. Output Voltage Swing vs. Supply Voltage

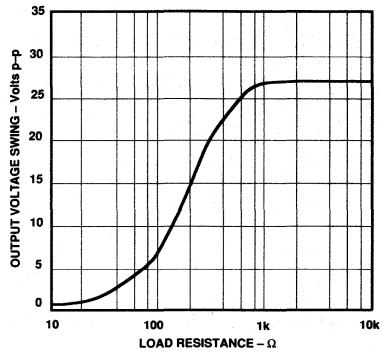


Figure 3. Output Voltage Swing vs. Load Resistance

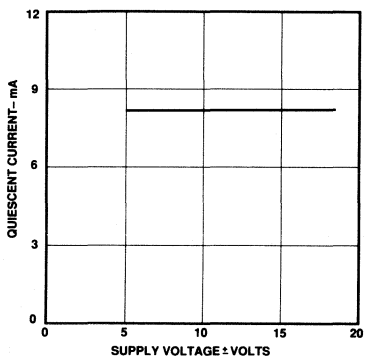


Figure 4. Quiescent Current vs. Supply Voltage

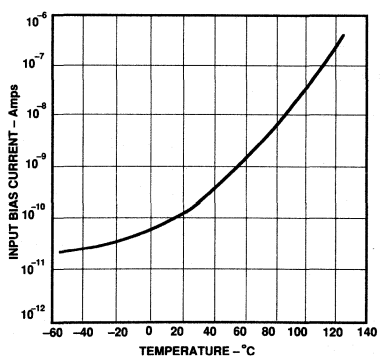


Figure 5. Input Bias Current vs. Temperature

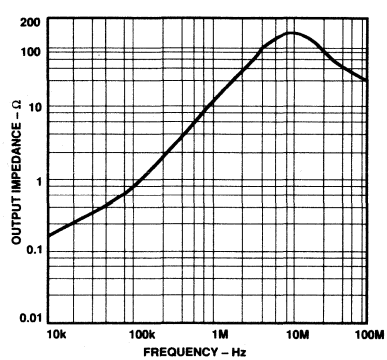


Figure 6. Output Impedance vs. Frequency (Closed Loop Gain = −1)

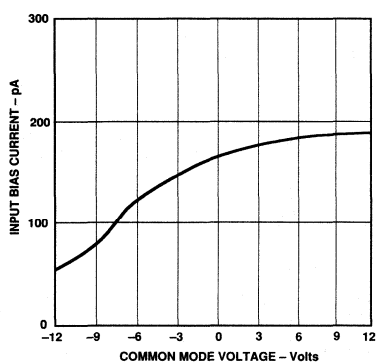


Figure 7. Input Bias Current vs. Common-Mode Voltage

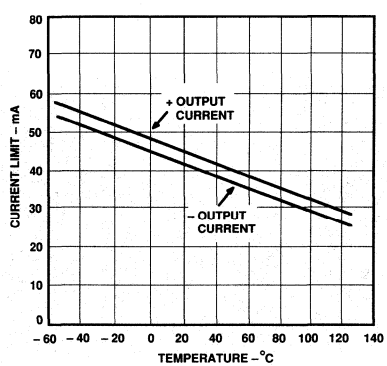


Figure 8. Short Circuit Current Limit vs. Temperature

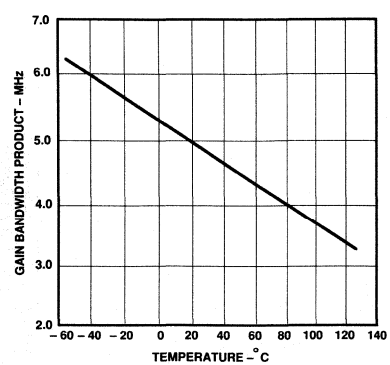


Figure 9. Gain Bandwidth Product vs. Temperature

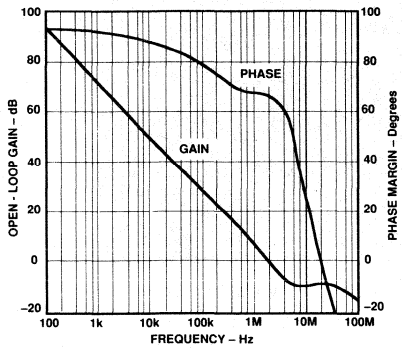


Figure 10. Open-Loop Gain and Phase vs. Frequency

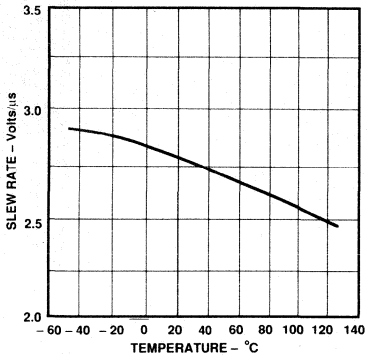


Figure 11. Slew Rate vs. Temperature (Gain = −1)

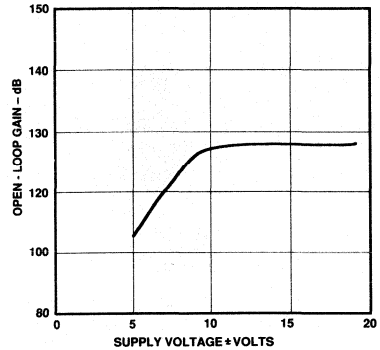


Figure 12. Open-Loop Gain vs. Supply Voltage, R_{LOAD} = 2K

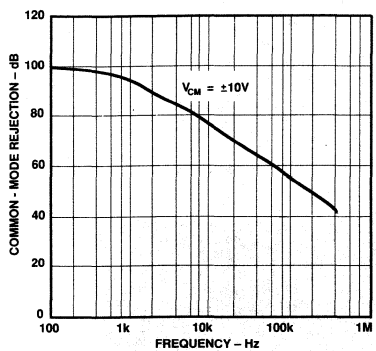


Figure 13. Common-Mode Rejection vs. Frequency

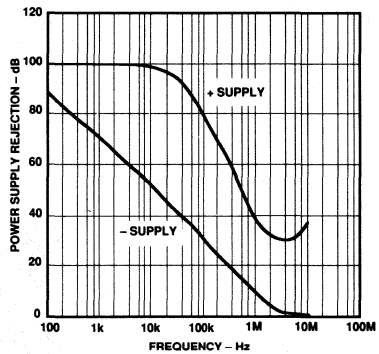


Figure 14. Power Supply Rejection vs. Frequency

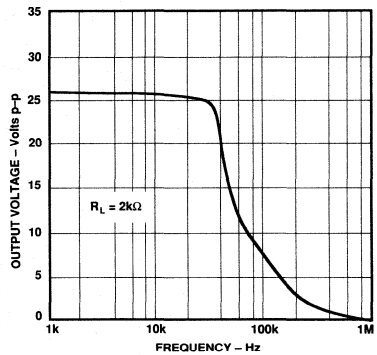


Figure 15. Large Signal Frequency Response

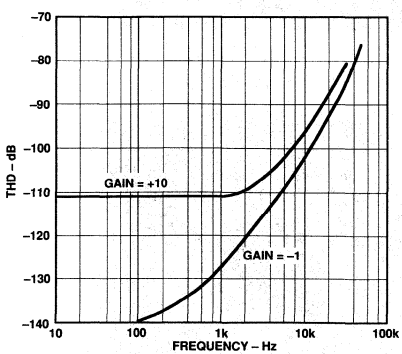


Figure 16. Total Harmonic Distortion vs. Frequency

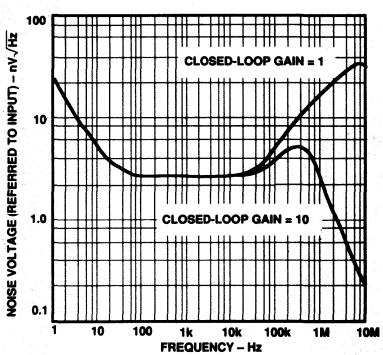


Figure 17. Input Noise Voltage Spectral Density

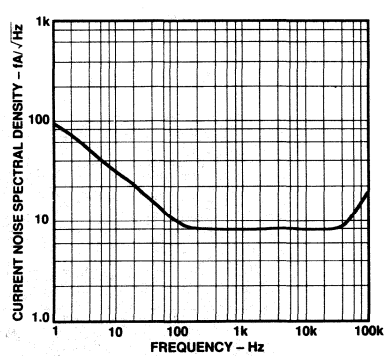


Figure 18. Input Noise Current Spectral Density

AD743—Typical Characteristics

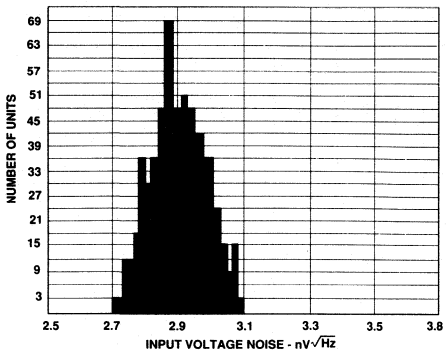


Figure 19. Typical Noise Distribution @ 10 kHz (602 Units)

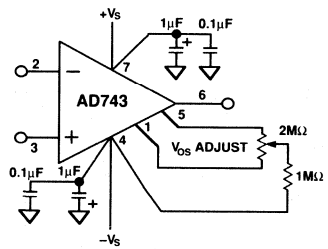


Figure 20. Offset Null Configuration

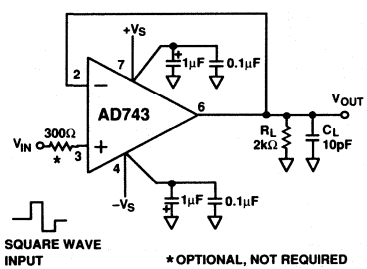


Figure 21. Unity-Gain Follower

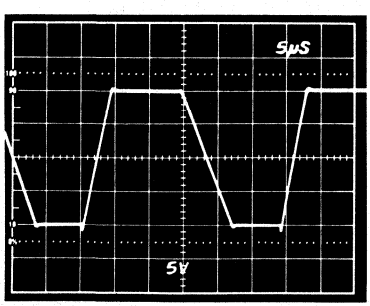


Figure 22a. Unity-Gain Follower Large Signal Pulse Response

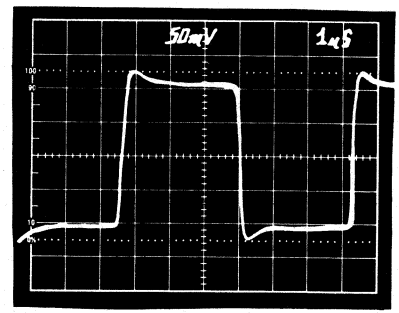


Figure 22b. Unity-Gain Follower Small Signal Pulse Response

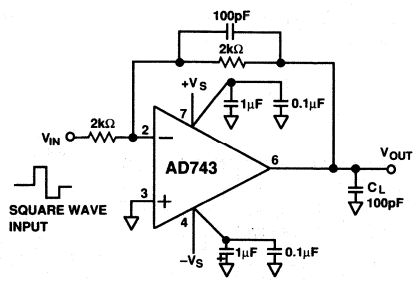


Figure 23a. Unity-Gain Inverter

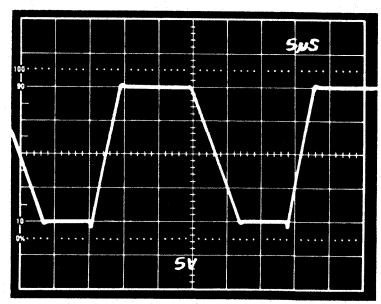


Figure 23b. Unity-Gain Inverter Large Signal Pulse Response

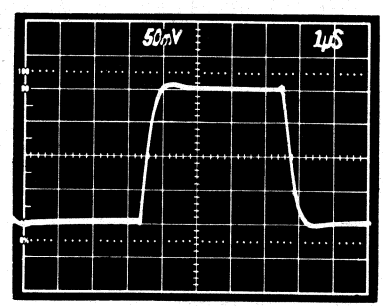


Figure 23c. Unity-Gain Inverter Small Signal Pulse Response

OP AMP PERFORMANCE: JFET VS. BIPOLAR

The AD743 is the first monolithic JFET op amp to offer the low input voltage noise of an industry-standard bipolar op amp without its inherent input current errors. This is demonstrated in Figure 24, which compares input voltage noise vs. input source resistance of the OP-27 and the AD743 op amps. From this figure, it is clear that at high source impedance the low current noise of the AD743 also provides lower total noise. It is also important to note that with the AD743 this noise reduction extends all the way down to low source impedances. The lower dc current errors of the AD743 also reduce errors due to offset and drift at high source impedances (Figure 25).

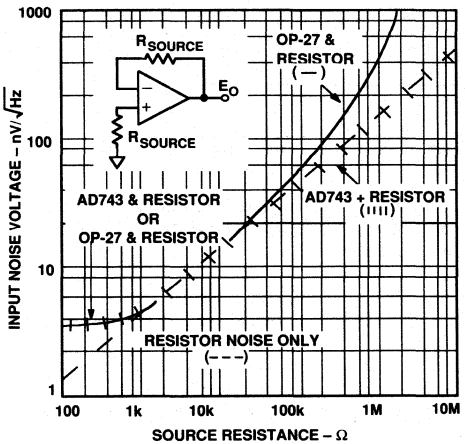


Figure 24. Total Input Noise Spectral Density @ 1 kHz vs. Source Resistance

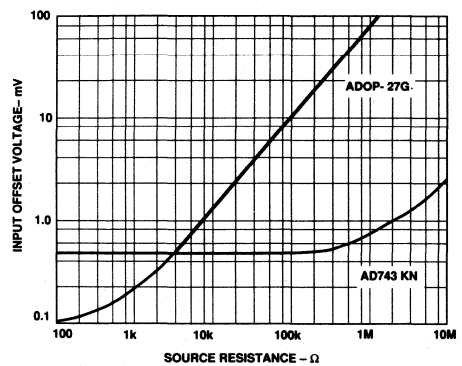


Figure 25. Input Offset Voltage vs. Source Resistance

DESIGNING CIRCUITS FOR LOW NOISE

An op amp's input voltage noise performance is typically divided into two regions: flatband and low frequency noise. The AD743 offers excellent performance with respect to both. The figure of 2.9 nV/$\sqrt{\text{Hz}}$ @10 kHz is excellent for a JFET input amplifier. The 0.1 to 10 Hz noise is typically 0.38 μV p–p. The user should pay careful attention to several design details in order to optimize low frequency noise performance. Random air currents can generate varying thermocouple voltages that appear as low frequency noise: therefore sensitive circuitry should be well shielded from air flow. Keeping absolute chip temperature low also reduces low frequency noise in two ways: first, the low frequency noise is strongly dependent on the ambient temperature and increases above +25°C. Secondly, since the gradient of temperature from the IC package to ambient is greater, the noise generated by random air currents, as previously mentioned, will be larger in magnitude. Chip temperature can be reduced both by operation at reduced supply voltages and by the use of a suitable clip-on heat sink, if possible.

Low frequency current noise can be computed from the magnitude of the dc bias current ($\tilde{I}_n = \sqrt{2qI_B\Delta f}$) and increases below approximately 100 Hz with a 1/f power spectral density. For the AD743 the typical value of current noise is 6.9 fA/$\sqrt{\text{Hz}}$ at 1 kHz. Using the formula, $\tilde{I}_n = \sqrt{4kT/R\Delta f}$, to compute the Johnson noise of a resistor, expressed as a current, one can see that the current noise of the AD743 is equivalent to that of a 3.45×10^8 Ω source resistance.

At high frequencies, the current noise of a FET increases proportionately to frequency. This noise is due to the "real" part of the gate input impedance, which decreases with frequency. This noise component usually is not important, since the voltage noise of the amplifier impressed upon its input capacitance is an apparent current noise of approximately the same magnitude.

In any FET input amplifier, the current noise of the internal bias circuitry can be coupled externally via the gate-to-source capacitances and appears as input current noise. This noise is totally correlated at the inputs, so source impedance matching will tend to cancel out its effect. Both input resistance and input capacitance should be balanced whenever dealing with source capacitances of less than 300 pF in value.

LOW NOISE CHARGE AMPLIFIERS

As stated, the AD743 provides both low voltage and low current noise. This combination makes this device particularly suitable in applications requiring very high charge sensitivity, such as capacitive accelerometers and hydrophones. When dealing with a high source capacitance, it is useful to consider the total input charge uncertainty as a measure of system noise.

Charge (Q) is related to voltage and current by the simply stated fundamental relationships:

$$Q = CV \text{ and } I = \frac{dQ}{dt}$$

As shown, voltage, current and charge noise can all be directly related. The change in open circuit voltage (ΔV) on a capacitor will equal the combination of the change in charge (ΔQ/C) and the change in capacitance with a built in charge (Q/ΔC).

Figures 26 and 27 show two ways to buffer and amplify the output of a charge output transducer. Both require using an amplifier which has a very high input impedance, such as the AD743. Figure 26 shows a model of a charge amplifier circuit. Here, amplification depends on the principle of conservation of charge at the input of amplifier A1, which requires that the charge on capacitor C_S be transferred to capacitor C_F, thus yielding an output voltage of $\Delta Q/C_F$. The amplifiers input voltage noise will appear at the output amplified by the noise gain $(1 + (C_S/C_F))$ of the circuit.

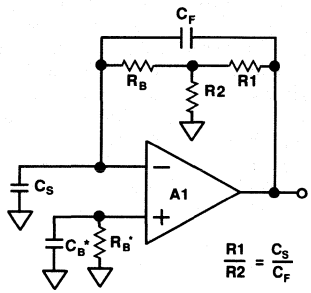


Figure 26. A Charge Amplifier Circuit

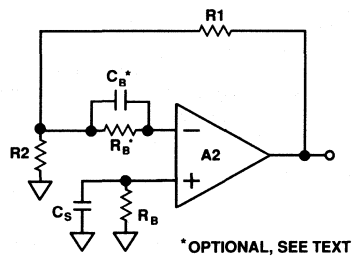


Figure 27. Model for a High Z Follower with Gain

The second circuit, Figure 27, is simply a high impedance follower with gain. Here the noise gain $(1 + (R1/R2))$ is the same as the gain from the transducer to the output. Resistor R_B, in both circuits, is required as a dc bias current return.

There are three important sources of noise in these circuits. Amplifiers A1 and A2 contribute both voltage and current noise, while resistor R_B contributes a current noise of:

$$\widetilde{N} = \sqrt{4\,k\,\frac{T}{R_B}\,\Delta f}$$

where:

k = Boltzman's Constant = 1.381×10^{-23} Joules/Kelvin

T = Absolute Temperature, Kelvin (0°C = +273.2 Kelvin)

Δf = Bandwidth − in Hz (Assuming an Ideal "Brick Wall" Filter)

This must be root-sum-squared with the amplifier's own current noise.

Figure 28 shows that these two circuits have an identical frequency response and the same noise performance (provided that C_S/C_F = R1/R2). One feature of the first circuit is that a "T" network is used to increase the effective resistance of R_B and improve the low frequency cutoff point by the same factor.

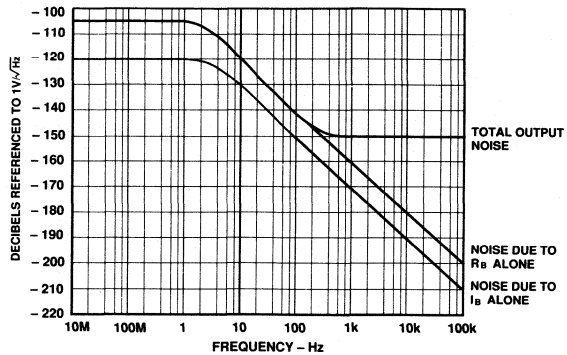


Figure 28. Noise at the Outputs of the Circuits of Figures 26 and 27. Gain = 10, C_S = 3000 pF, R_B = 22 MΩ

However, this does not change the noise contribution of R_B which, in this example, dominates at low frequencies. The graph of Figure 29 shows how to select an R_B large enough to minimize this resistor's contribution to overall circuit noise. When the equivalent current noise of R_B $((\sqrt{4kT})/R)$ equals the noise of I_B $(\sqrt{2qI_B})$, there is diminishing return in making R_B larger.

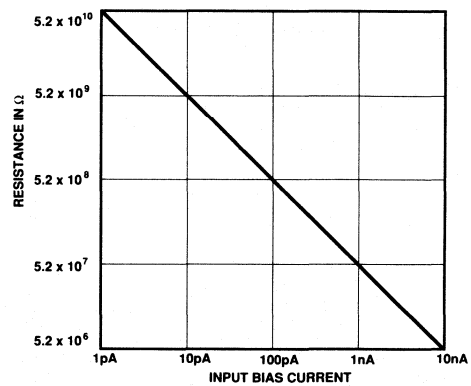


Figure 29. Graph of Resistance vs. Input Bias Current where the Equivalent Noise $\sqrt{4kT/R}$, Equals the Noise of the Bias Current $\sqrt{2qI_B}$

To maximize dc performance over temperature, the source resistances should be balanced on each input of the amplifier. This is represented by the optional resistor R_B in Figures 26 and 27. As previously mentioned, for best noise performance care should be taken to also balance the source capacitance designated by C_B. The value for C_B in Figure 26 would be equal to C_S, in Figure 27. At values of C_B over 300 pF, there is a diminishing impact on noise; capacitor C_B can then be simply a large bypass of 0.01 μF or greater.

HOW CHIP PACKAGE TYPE AND POWER DISSIPATION AFFECT INPUT BIAS CURRENT

As with all JFET input amplifiers, the input bias current of the AD743 is a direct function of device junction temperature, I_B approximately doubling every 10°C. Figure 30 shows the relationship between bias current and junction temperature for the AD743. This graph shows that lowering the junction temperature will dramatically improve I_B.

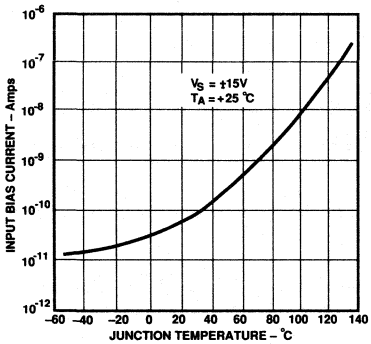
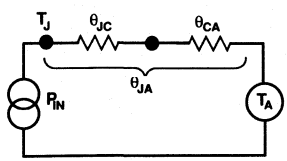


Figure 30. Input Bias Current vs. Junction Temperature

The dc thermal properties of an IC can be closely approximated by using the simple model of Figure 31 where current represents power dissipation, voltage represents temperature, and resistors represent thermal resistance (θ in °C/watt).



WHERE:
P_{IN} = DEVICE DISSIPATION
T_A = AMBIENT TEMPERATURE
T_J = JUNCTION TEMPERATURE
θ_{JC}= THERMAL RESISTANCE – JUNCTION TO CASE
θ_{CA}= THERMAL RESISTANCE – CASE TO AMBIENT

Figure 31. A Device Thermal Model

From this model $T_J = T_A + \theta_{JA}$ Pin. Therefore, I_B can be determined in a particular application by using Figure 30 together with the published data for θ_{JA} and power dissipation. The user can modify θ_{JA} by use of an appropriate clip-on heat sink such as the Aavid #5801. θ_{JA} is also a variable when using the AD743 in chip form. Figure 32 shows bias current vs. supply voltage with θ_{JA} as the third variable. This graph can be used to predict bias current after θ_{JA} has been computed. Again bias current will double for every 10°C. The designer using the AD743 in chip form (Figure 33) must also be concerned with both θ_{JC} and θ_{CA}, since θ_{JC} can be affected by the type of die mount technology used.

Typically, θ_{JC}'s will be in the 3°C to 5°C/watt range; therefore, for normal packages, this small power dissipation level may be ignored. But, with a large hybrid substrate, θ_{JC} will dominate proportionately more of the total θ_{JA}.

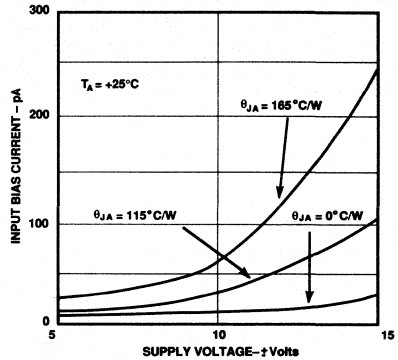


Figure 32. Input Bias Current vs. Supply Voltage for Various Values of θ_{JA}

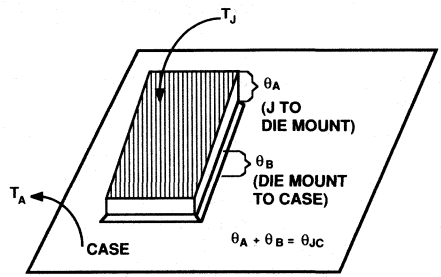
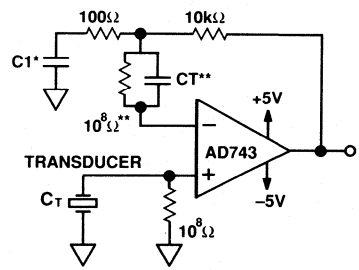


Figure 33. A Breakdown of Various Package Thermal Resistances

REDUCED POWER SUPPLY OPERATION FOR LOWER I_B

Reduced power supply operation lowers I_B in two ways: first, by lowering both the total power dissipation and second, by reducing the basic gate-to-junction leakage (Figure 32). Figure 34 shows a 40 dB gain piezoelectric transducer amplifier, which operates without an ac coupling capacitor, over the −40°C to +85°C temperature range. If the optional coupling capacitor is used, this circuit will operate over the entire −55°C to +125°C military temperature range.



*OPTIONAL DC BLOCKING CAPACITOR
**OPTIONAL, SEE TEXT

Figure 34. A Piezoelectric Transducer

AN INPUT-IMPEDANCE-COMPENSATED, SALLEN-KEY FILTER

The simple high pass filter of Figure 35 has an important source of error which is often overlooked. Even 5 pF of input capacitance in amplifier "A" will contribute an additional 1% of passband amplitude error, as well as distortion, proportional to the C/V characteristics of the input junction capacitance. The addition of the network designated "Z" will balance the source impedance—as seen by "A"—and thus eliminate these errors.

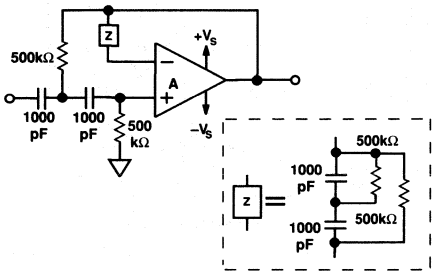


Figure 35. An Input Impedance Compensated Sallen-Key Filter

TWO HIGH PERFORMANCE ACCELEROMETER AMPLIFIERS

Two of the most popular charge-out transducers are hydrophones and accelerometers. Precision accelerometers are typically calibrated for a charge output (pC/g).* Figures 36a and 36b show two ways in which to configure the AD743 as a low noise charge amplifier for use with a wide variety of piezoelectric accelerometers. The input sensitivity of these circuits will be determined by the value of capacitor C1 and is equal to:

$$\Delta V_{OUT} = \frac{\Delta Q_{OUT}}{C1}$$

The ratio of capacitor C1 to the internal capacitance (C_T) of the transducer determines the noise gain of this circuit ($1 + C_T/C1$). The amplifiers voltage noise will appear at its output amplified by this amount. The low frequency bandwidth of these circuits will be dependent on the value of resistor R1. If a "T" network is used, the effective value is: R1 (1 + R2/R3).

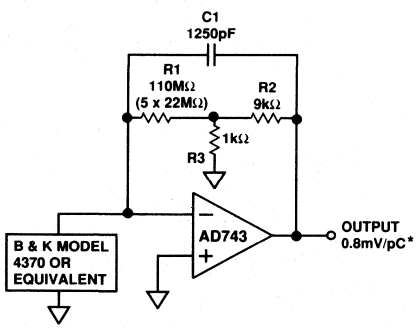


Figure 36a. A Basic Accelerometer Circuit

*pC = Picocoulombs
g = Earth's Gravitational Constant

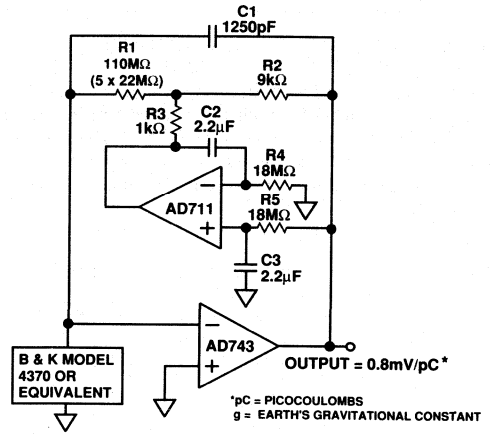


Figure 36b. An Accelerometer Circuit Employing a DC Servo Amplifier

A dc servo-loop (Figure 36b) can be used to assure a dc output which is <10 mV, without the need for a large compensating resistor when dealing with bias currents as large as 100 nA. For optimal low frequency performance, the time constant of the servo loop (R4C2 = R5C3) should be:

$$\text{Time Constant} \geq 10\ R1 \left(1 + \frac{R2}{R3}\right) C1$$

A LOW NOISE HYDROPHONE AMPLIFIER

Hydrophones are usually calibrated in the voltage-out mode. The circuits of Figures 37a and 37b can be used to amplify the output of a typical hydrophone. Figure 37a shows a typical dc coupled circuit. The optional resistor and capacitor serve to counteract the dc offset caused by bias currents flowing through resistor R1. Figure 37b, a variation of the original circuit, has a low frequency cutoff determined by an RC time constant equal to:

$$\text{Time Constant} = \frac{1}{2\pi \times C_C \times 100\ \Omega}$$

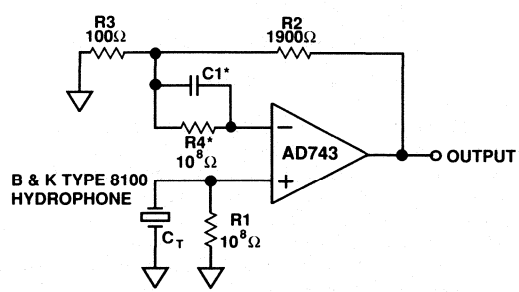


Figure 37a. A Basic Hydrophone Amplifier

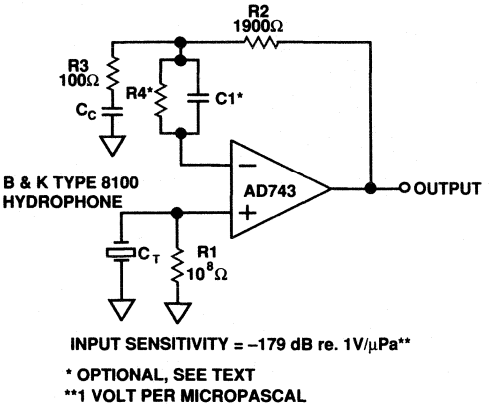


Figure 37b. An AC-Coupled, Low Noise Hydrophone Amplifier

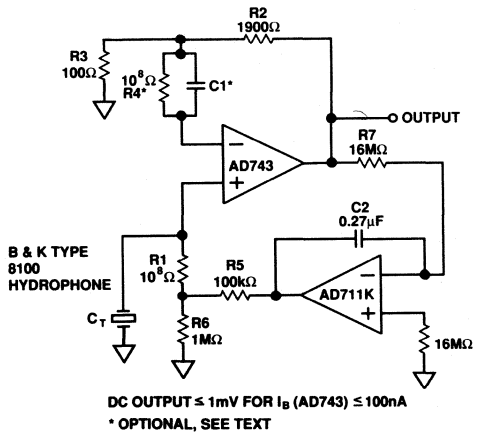


Figure 37c. A Hydrophone Amplifier Incorporating a DC Servo Loop

Where the dc gain is 1 and the gain above the low frequency cutoff ($1/(2\pi C_C(100\ \Omega))$) is the same as the circuit of Figure 37a. The circuit of Figure 37c uses a dc servo loop to keep the dc output at 0 V and to maintain full dynamic range for I_B's up to 100 nA. The time constant of R7 and C2 should be larger than that of R1 and C_T for a smooth low frequency response.

The transducer shown has a source capacitance of 7500 pF. For smaller transducer capacitances (≤300 pF), lowest noise can be achieved by adding a parallel RC network (R4 = R1, C1 = C_T) in series with the inverting input of the AD743.

BALANCING SOURCE IMPEDANCES

As mentioned previously, it is good practice to balance the source impedances (both resistive and reactive) as seen by the inputs of the AD743. Balancing the resistive components will optimize dc performance over temperature because balancing will mitigate the effects of any bias current errors. Balancing input capacitance will minimize ac response errors due to the amplifier's input capacitance and, as shown in Figure 38, noise performance will be optimized. Figure 39 shows the required external components for noninverting (A) and inverting (B) configurations.

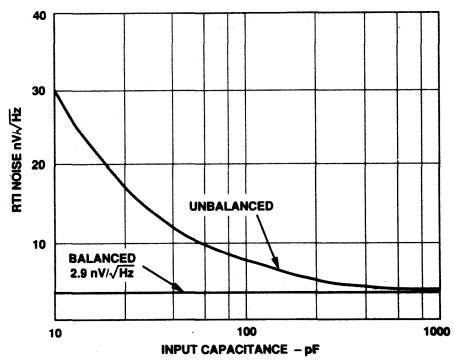


Figure 38. RTI Voltage Noise vs. Input Capacitance

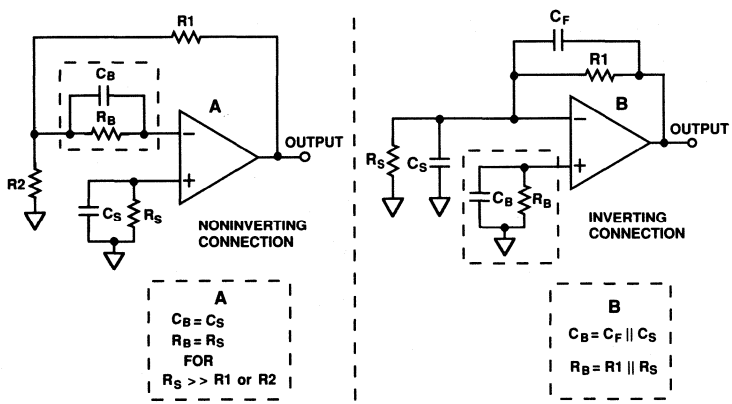


Figure 39. Optional External Components for Balancing Source Impedances

ANALOG DEVICES

Precision, 500ns Settling BiFET Op Amp

AD744

FEATURES

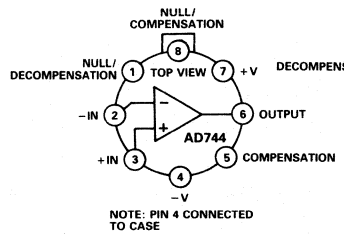
AC PERFORMANCE
- 500ns Settling to 0.01% for 10V Step
- 1.5μs Settling to 0.0025% for 10V Step
- 75V/μs Slew Rate
- 0.0003% Total Harmonic Distortion (THD)
- 13MHz Gain Bandwidth – Internal Compensation
- >200MHz Gain Bandwidth (G = 1000) External Decompensation
- >1000pF Capacitive Load Drive Capability with 10V/μs Slew Rate – External Compensation

DC PERFORMANCE
- 0.25mV max Offset Voltage (AD744C)
- 3μV/°C max Drift (AD744C)
- 250V/mV min Open-Loop Gain (AD744B)
- 4μV p-p max Noise, 0.1Hz to 10Hz (AD744C)
- Available in Plastic Mini-DIP, Plastic SOIC, Hermetic Cerdip, Hermetic Metal Can Packages and Chip Form
- MIL-STD-883B Processing Available
- Surface Mount (SOIC) Package Available in Tape and Reel in Accordance with EIA-481A Standard

APPLICATIONS
- Output Buffers for 12-Bit, 14-Bit and 16-Bit DACs, ADC Buffers, Cable Drivers, Wideband Preamplifiers and Active Filters

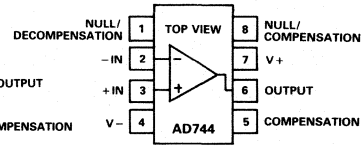
CONNECTION DIAGRAMS

TO-99 (H) Package



NOTE: PIN 4 CONNECTED TO CASE

Plastic Mini-DIP (N), Small Outline (R) and Cerdip (Q) Packages



PRODUCT DESCRIPTION

The AD744 is a fast-settling, precision, FET input, monolithic operational amplifier. It offers the excellent dc characteristics of the AD711 BiFET family with enhanced settling, slew rate, and bandwidth. The AD744 also offers the option of using custom compensation to achieve exceptional capacitive load drive capability.

The single-pole response of the AD744 provides fast settling: 500ns to 0.01%. This feature, combined with its high dc precision, makes it suitable for use as a buffer amplifier for 12-bit, 14-bit or 16-bit DACs and ADCs. Furthermore, the AD744's low total harmonic distortion (THD) level of 0.0003% and gain bandwidth product of 13MHz make it an ideal amplifier for demanding audio applications. It is also an excellent choice for use in active filters in 12-bit, 14-bit and 16-bit data acquisition systems.

The AD744 is internally compensated for stable operation as a unity gain inverter or as a noninverting amplifier with a gain of two or greater. External compensation may be applied to the AD744 for stable operation as a unity gain follower. External compensation also allows the AD744 to drive 1000pF capacitive loads, slewing at 10V/μs with full stability. Alternatively, external decompensation may be used to increase the gain bandwidth of the AD744 to over 200MHz at high gains. This makes the AD744 ideal for use as ac preamps in digital signal processing (DSP) front ends.

The AD744 is available in seven performance grades. The AD744J and AD744K are rated over the commercial temperature range of 0 to +70°C. The AD744A, AD744B and AD744C are rated over the industrial temperature range of −40°C to +85°C. The AD744S and AD744T are rated over the military temperature range of −55°C to +125°C and are available processed to MIL-STD-883B, Rev. C.

Extended reliability PLUS screening is available, specified over the commercial and industrial temperature ranges. PLUS screening includes a 168-hour burn-in, as well as other environmental and physical tests.

The AD744 is available in an 8-pin plastic mini-DIP, 8-pin small outline, 8-pin cerdip or TO-99 metal can.

PRODUCT HIGHLIGHTS

1. The AD744 is a high-speed BiFET op amp that offers excellent performance at competitive prices. It outperforms the OPA602/OPA606, LF356 and LF400.
2. The AD744 offers exceptional dynamic response. It settles to 0.01% in 500ns and has a 100% tested minimum slew rate of 50V/μs (AD744B).
3. The combination of Analog Devices' advanced processing technology, laser wafer drift trimming and well-matched ion-implanted JFETs provide outstanding dc precision. Input offset voltage, input bias current, and input offset current are specified in the warmed-up condition; all are 100% tested.
4. The AD744 has a guaranteed and tested maximum voltage noise of 4μV p-p, 0.1Hz to 10Hz (AD744C).

AD744—SPECIFICATIONS (@ +25°C and ±15V dc, unless otherwise noted)

Model	Conditions	AD744J/A/S Min	AD744J/A/S Typ	AD744J/A/S Max	AD744K/B/T Min	AD744K/B/T Typ	AD744K/B/T Max	AD744C Min	AD744C Typ	AD744C Max	Units
INPUT OFFSET VOLTAGE[1]											
Initial Offset			0.3	**1.0**		0.25	**0.5**		0.10	**0.25**	mV
Offset	$T_{min}-T_{max}$			2/2/2			**1.0**			**0.45**	mV
vs. Temp			5	20/20/**20**		5	**10**		2	**3**	μV/°C
vs. Supply[2]		**82**	95		**88**	100		**92**	110		dB
vs. Supply	$T_{min}-T_{max}$	82/82/**82**			**88**			**92**			dB
Long-Term Stability			15			15			15		μV/month
INPUT BIAS CURRENT[3]											
Either Input	$V_{CM}=0V$		30	**100**		30	**100**		30	**50**	pA
Either Input @T_{max} =	$V_{CM}=0V$										
J, K	70°C		0.7	2.3		0.7	2.3				nA
A, B, C	85°C		1.9	6.4		1.9	6.4		1.9	3.2	nA
S, T	125°C		31	102		31	102				nA
Either Input	$V_{CM}=+10V$		40	150		40	**150**		40	**100**	pA
Offset Current	$V_{CM}=0V$		20	**50**		10	**50**		10	**20**	pA
Offset Current @T_{max} =	$V_{CM}=0V$										
J, K	70°C		0.4	1.1		0.2	1.1				nA
A, B, C	85°C		1.3	3.2		0.6	3.2		0.6	1.3	nA
S, T	125°C		20	52		10	52				nA
FREQUENCY RESPONSE											
Gain BW, Small Signal	$G=-1$	**8**	13		**9**	13		**9**	13		MHz
Full Power Response	$V_O=20V$ p-p		1.2			1.2			1.2		MHz
Slew Rate, Unity Gain	$G=-1$	**45**	75		**50**	75		**50**	75		V/μs
Settling Time to 0.01%[4]	$G=-1$		0.5	0.75		0.5	0.75		0.5	0.75	μs
Total Harmonic	f = 1kHz										
Distortion	R1≥2kΩ										
	$V_O=3V$ rms		0.0003			0.0003			0.0003		%
INPUT IMPEDANCE											
Differential			$3\times10^{12}\|5.5$			$3\times10^{12}\|5.5$			$3\times10^{12}\|5.5$		Ω‖pF
Common Mode			$3\times10^{12}\|5.5$			$3\times10^{12}\|5.5$			$3\times10^{12}\|5.5$		Ω‖pF
INPUT VOLTAGE RANGE											
Differential[5]			±20			±20			±20		V
Common-Mode Voltage			+14.5, −11.5			+14.5, −11.5			+14.5, −11.5		V
Over Max Operating Range[6]		**−11**		**+13**	**−11**		**+13**	**−11**		**+13**	V
Common-Mode Rejection Ratio	$V_{CM}=\pm10V$	**78**	88		**82**	88		**86**	94		dB
	T_{min} to T_{max}	76/76/**76**	84		**80**	84		**86**	90		dB
	$V_{CM}=\pm11V$	**72**	84		**78**	84		**80**	90		dB
	T_{min} to T_{max}	70/70/**70**	80		**74**	80		**76**	84		dB
INPUT VOLTAGE NOISE	0.1 to 10Hz		2			2			2	**4**	μV p-p
	f = 10Hz		45			45			45		nV/√Hz
	f = 100Hz		22			22			22		nV/√Hz
	f = 1kHz		18			18			18		nV/√Hz
	f = 10kHz		16			16			16		nV/√Hz
INPUT CURRENT NOISE	f = 1kHz		0.01			0.01			0.01		pA/√Hz
OPEN LOOP GAIN[7]	$V_O=\pm10V$										
	$R_{LOAD}\geq2k\Omega$	**200**	400		**250**	400		**250**	400		V/mV
	T_{min} to T_{max}	100/100/**100**			**100**			**150**			V/mV
OUTPUT CHARACTERISTICS											
Voltage	$R_{LOAD}\geq2k\Omega$	**+13, −12.5**	+13.9, −13.3		**+13, −12.5**	+13.9, −13.3		**+13, −12.5**	+13.9, −13.3		V
	T_{min} to T_{max}	±12/±12/**±12**	+13.8, −13.1		**±12**	+13.8, −13.1		**±12**	+13.8, −13.1		V
Current	Short-Circuit		25			25			25		mA
Capacitive Load[8]	Gain = −1			**1000**			**1000**			**1000**	pF
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		**±4.5**		**±18**	**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current			3.5	**5.0**		3.5	**4.0**		3.5	**4.0**	mA
TEMPERATURE RANGE											
Operating, Rated Performance											
Commercial (0 to +70°C)			AD744J			AD744K					
Industrial (−40°C to +85°C)			AD744A			AD744B			AD744C		
Military (−55°C to +125°C)			AD744S			AD744T					
PACKAGE OPTIONS[9]											
8-Pin Plastic Mini-DIP (N-8) and SOIC (R-8)			AD744JN, AD744JR			AD744KN, AD744KR					
8-Pin Cerdip (Q-8)			AD744AQ, AD744SQ			AD744BQ, AD744TQ			AD744CQ		
TO-99 Metal Can (H-08A)			AD744AH, AD744SH			AD744BH, AD744TH			AD744CH		
Tape and Reel			AD744JR-REEL			AD744KR-REEL					
Chips Available			AD744JChips						AD744SChips		

NOTES

[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at $T_A=+25°C$.

[2]PSRR test conditions: $+V_S=15V$, $-V_S=-12V$ to $-18V$ and $+V_S=12V$ to $18V$, $-V_S=-15V$.

[3]Bias Current Specifications are guaranteed maximum at either input after 5 minutes of operation at $T_A=+25°C$. For higher temperature, the current doubles every 10°C.

[4]Gain = −1, $R_L=2k$, $C_L=10pF$, refer to Figure 25.

[5]Defined as voltage between inputs, such that neither exceeds ±10V from ground.

[6]Typically exceeding −14.1V negative common-mode voltage on either input results in an output phase reversal.

[7]Open-Loop Gain is specified with V_{OS} both nulled and unnulled.

[8]Capacitive load drive specified for $C_{COMP}=20pF$ with the device connected as shown in Figure 32. Under these conditions, slew rate = 14V/μs and 0.01% settling time = 1.5μs typical. Refer to Table II for optimum compensation while driving a capacitive load.

[9]For outline information see Package Information section.

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±18V
Internal Power Dissipation[2]	500mW
Input Voltage[3]	±18V
Output Short Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range (Q, H)	−65°C to +150°C
Storage Temperature Range (N, R)	−65°C to +125°C
Operating Temperature Range	
AD744J/K	0 to +70°C
AD744A/B/C	−40°C to +85°C
AD744S/T	−55°C to +125°C
Lead Temperature Range (Soldering 60 sec)	300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indited in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Thermal Characteristics

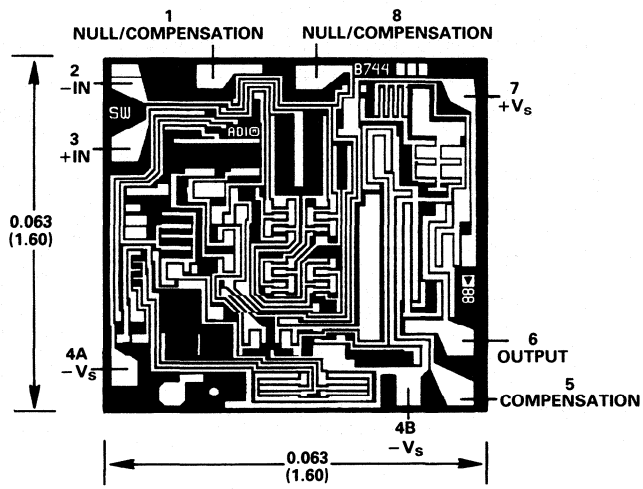
8-Pin Plastic Package: θ_{JC} = 33°C/W, θ_{JA} = 100°C/W
8-Pin Cerdip Package: θ_{JC} = 22°C/W, θ_{JA} = 110°C/W
8-Pin Metal Can Package: θ_{JC} = 65°C/W, θ_{JA} = 150°C/W
8-Pin SOIC Package: θ_{JC} = 42°C/W, θ_{JA} = 160°C/W

[3]For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.

2

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



AD744—Typical Characteristics

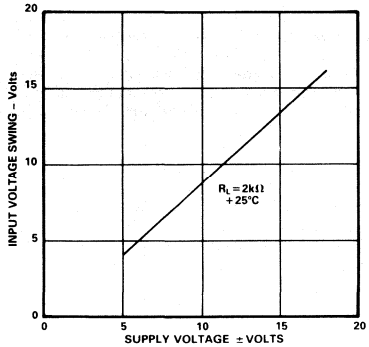


Figure 1. Input Voltage Swing vs. Supply Voltage

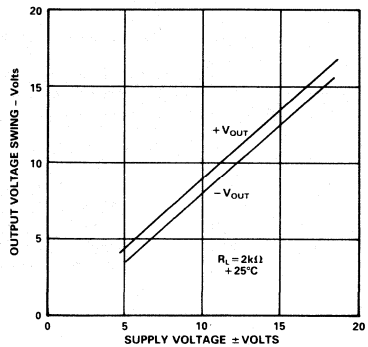


Figure 2. Output Voltage Swing vs. Supply Voltage

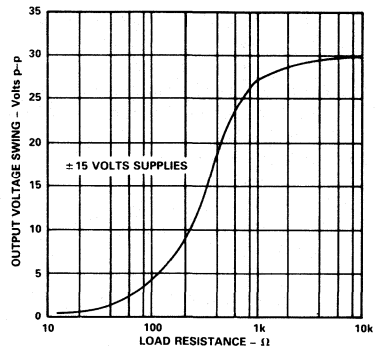


Figure 3. Output Voltage Swing vs. Load Resistance

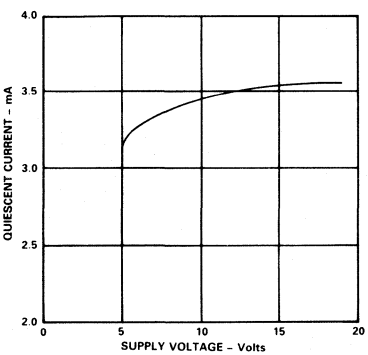


Figure 4. Quiescent Current vs. Supply Voltage

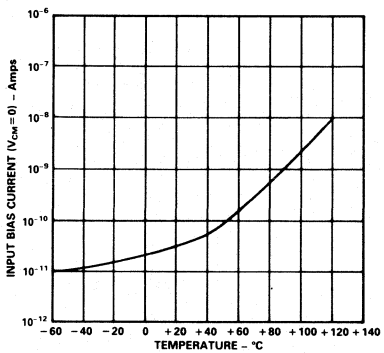


Figure 5. Input Bias Current vs. Temperature

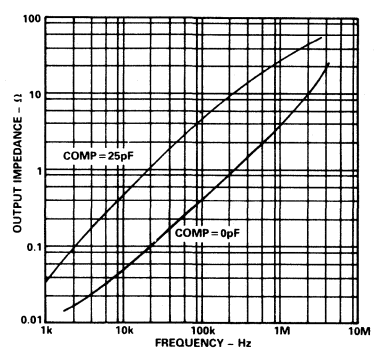


Figure 6. Output Impedance vs. Frequency

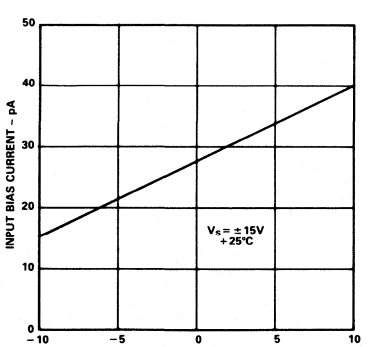


Figure 7. Input Bias Current vs. Common-Mode Voltage

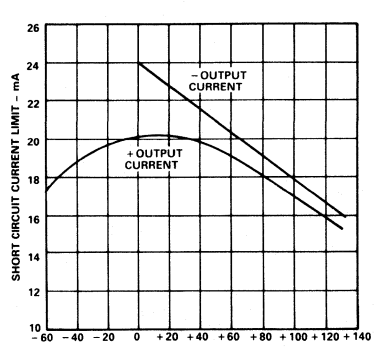


Figure 8. Short Circuit Current Limit vs. Temperature

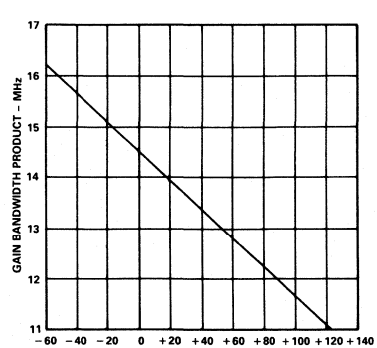


Figure 9. Gain Bandwidth Product vs. Temperature

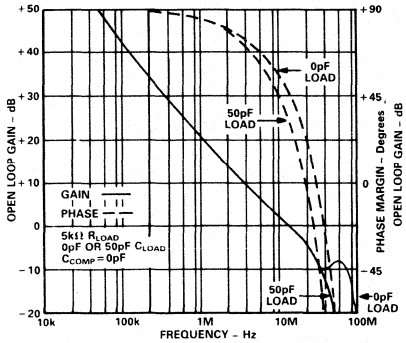


Figure 10. Open Loop Gain and Phase Margin vs. Frequency $C_{COMP} = 0pF$

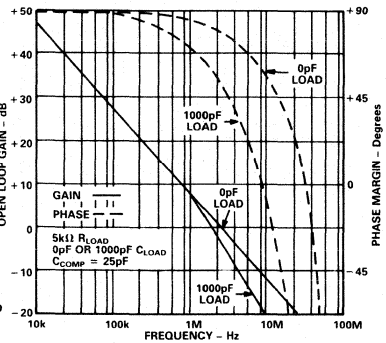


Figure 11. Open Loop Gain and Phase Margin vs. Frequency $C_{COMP} = 25pF$

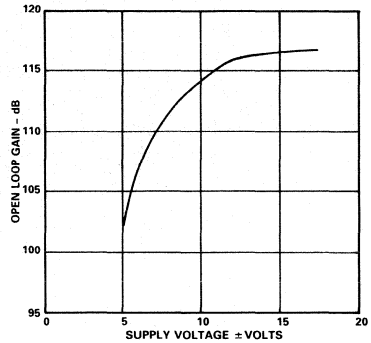


Figure 12. Open Loop Gain vs. Supply Voltage

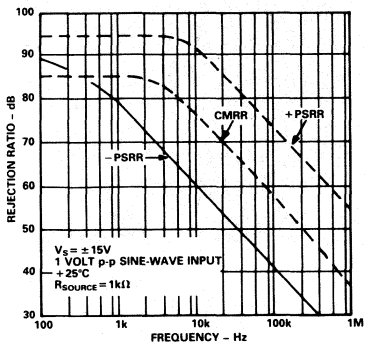


Figure 13. Common-Mode and Power Supply Rejection vs. Frequency

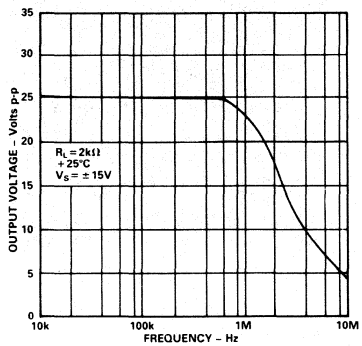


Figure 14. Large Signal Frequency Response

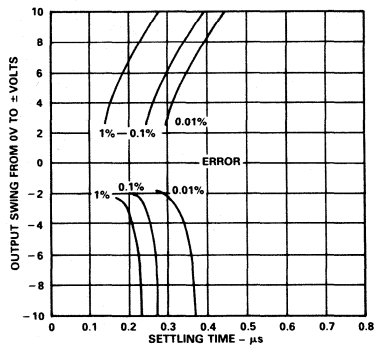


Figure 15. Output Swing and Error vs. Settling Time

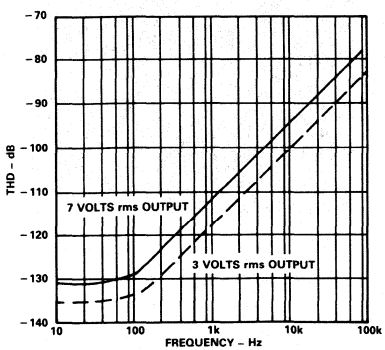


Figure 16. Total Harmonic Distortion vs. Frequency, Circuit of Figure 20 (G = 10)

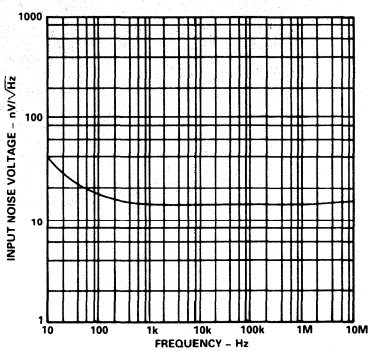


Figure 17. Input Noise Voltage Spectral Density

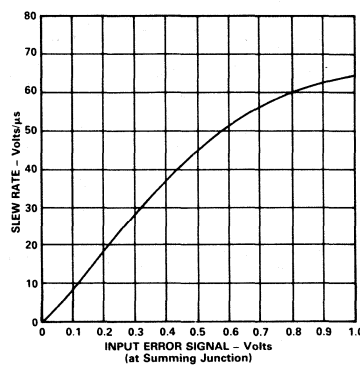


Figure 18. Slew Rate vs. Input Error Signal

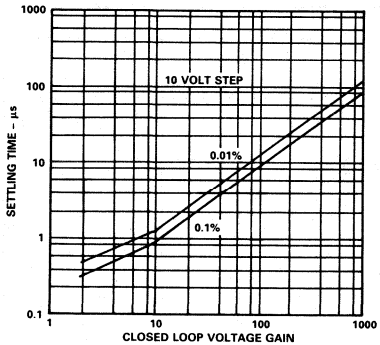


Figure 19. Settling Time vs. Closed Loop Voltage Gain

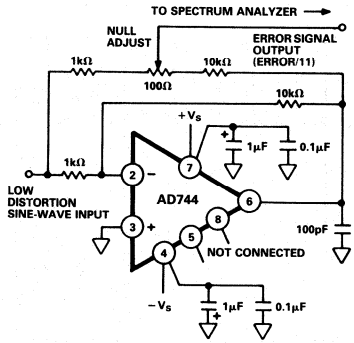


Figure 20. THD Test Circuit

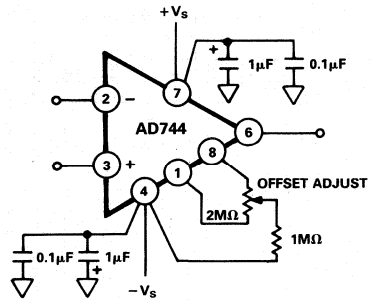


Figure 21. Offset Null Configuration

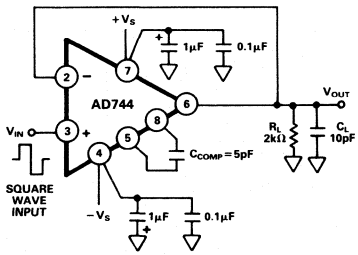


Figure 22a. Unity Gain Follower

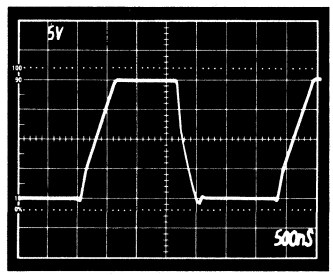


Figure 22b. Unity Gain Follower Large Signal Pulse Response, C_{COMP} = 5pF

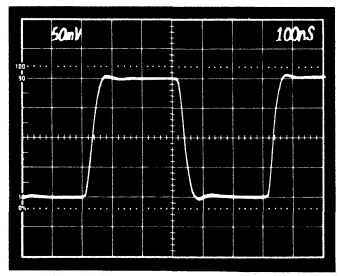


Figure 22c. Unity Gain Follower Small Signal Pulse Response, C_{COMP} = 5pF

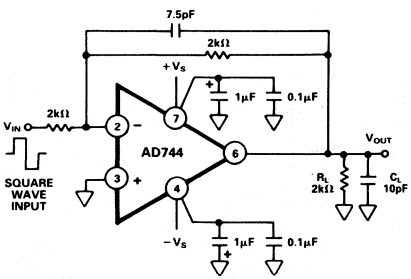


Figure 23a. Unity Gain Inverter

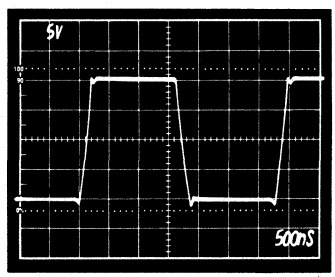


Figure 23b. Unity Gain Inverter Large Signal Pulse Response, C_{COMP} = 0pF

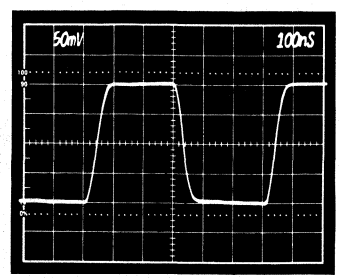


Figure 23c. Unity Gain Inverter Small Signal Pulse Response, C_{COMP} = 0pF

POWER SUPPLY BYPASSING

The power supply connections to the AD744 must maintain a low impedance to ground over a bandwidth of 10MHz or more. This is especially important when driving a significant resistive or capacitive load, since all current delivered to the load comes from the power supplies. Multiple high quality bypass capacitors are recommended for each power supply line in any critical application. A 0.1μF ceramic and a 1μF electrolytic capacitor as shown in Figure 24 placed as close as possible to the amplifier (with short lead lengths to power supply common) will assure adequate high frequency bypassing, in most applications. A minimum bypass capacitance of 0.1μF should be used for any application.

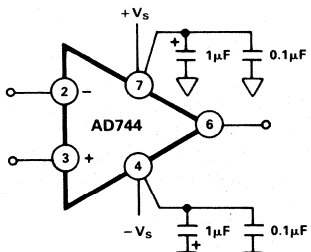


Figure 24. Recommended Power Supply Bypassing

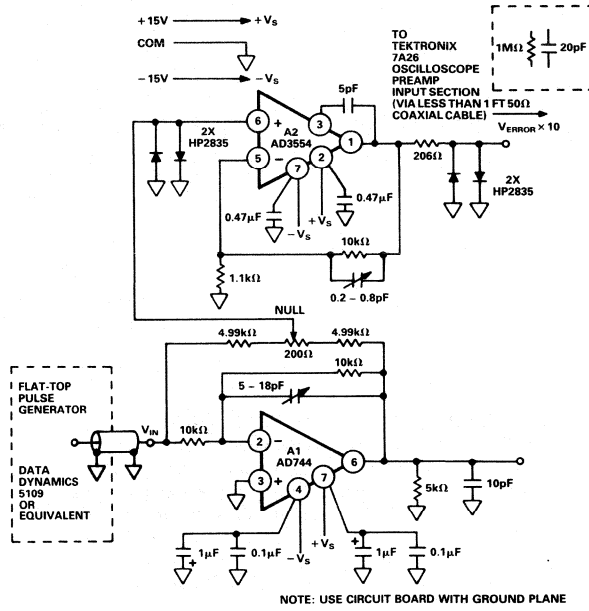


Figure 25. Settling Time Test Circuit

MEASURING AD744 SETTLING TIME

The photos of Figures 26 and 27 show the dynamic response of the AD744 while operating in the settling time test circuit of Figure 25. The input of the settling time fixture is driven by a flat-top pulse generator. The error signal output from the false summing node of A1, the AD744 under test, is clamped, amplified by op amp A2 and then clamped again. The error signal is thus clamped twice: once to prevent overloading amplifier A2 and then a second time to avoid overloading the oscilloscope preamp. A Tektronix oscilloscope preamp type 7A26 was carefully chosen because it recovers from the approximately 0.4V overload quickly enough to allow accurate measurement of the AD744's 500ns settling time. Amplifier A2 is a very high-speed FET-input op amp; it provides a voltage gain of 10, amplifying the error signal output of the AD744 under test.

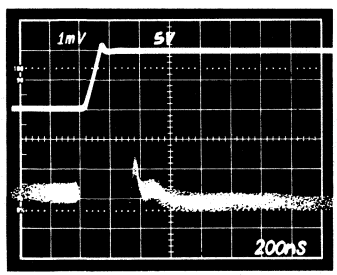


Figure 26. Settling Characteristics 0 to +10V Step
Upper Trace: Output of AD744 Under Test (5V/div.)
Lower Trace: Amplified Error Voltage (0.01%/div.)

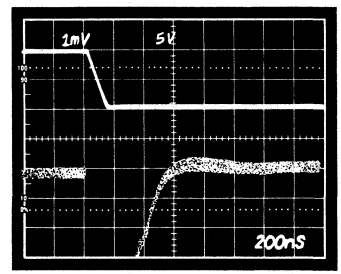


Figure 27. Settling Characteristics 0 to −10V Step
Upper Trace: Output of AD744 Under Test (5V/div.)
Lower Trace: Amplified Error Voltage (0.01%/div.)

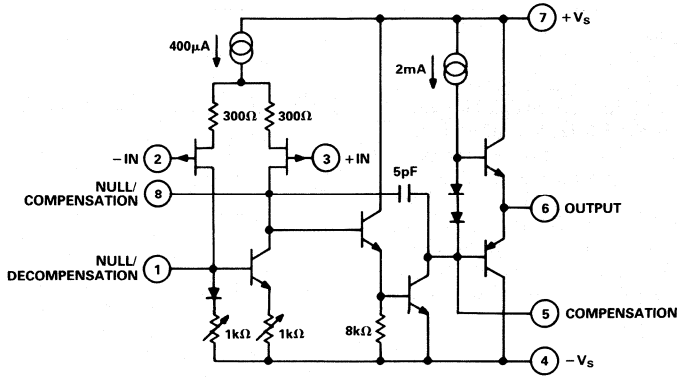


Figure 28. AD744 Simplified Schematic

EXTERNAL FREQUENCY COMPENSATION

Even though the AD744 is useable without compensation in most applications, it may be externally compensated for even more flexibility. This is accomplished by connecting a capacitor between Pins 5 and 8. Figure 28, a simplified schematic of the AD744, shows where this capacitor is connected. This feature is useful because it allows the AD744 to be used as a unity gain voltage follower. It also enables the amplifier to drive capacitive loads up to 2000pF and greater.

The slew rate and gain bandwidth product of the AD744 are inversely proportional to the value of the compensation capacitor, C_{COMP}. Therefore, when trying to maximize the speed of the amplifier, the value of C_{COMP} should be minimized. C_{COMP} can also be used to slow the amplifier to a point where the slew rate is perfectly symmetrical and well controlled. Figure 29 summarizes the effect of external compensation on slew rate and bandwidth.

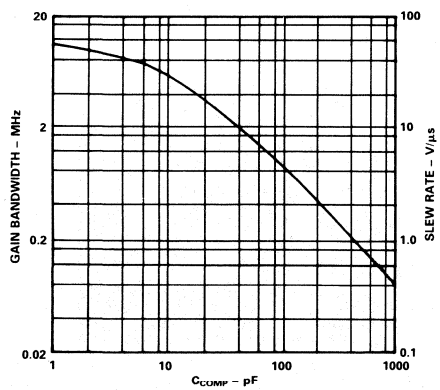


Figure 29. Gain Bandwidth and Slew Rate vs. C_{COMP}

The following section provides tables to show what C_{COMP} values will provide the necessary compensation for given circuit configurations and capacitive loads. In each case, the recommended C_{COMP} is a minimum value. A larger C_{COMP} can always be used, but slew rate and bandwidth performance will be degraded.

Figure 30 shows the AD744 configured as a unity gain voltage follower. In this case, a minimum compensation capacitor of 5pF is necessary for stable operation. Larger compensation capacitors can be used for driving larger capacitive loads. Table I outlines recommended minimum values for C_{COMP} based on the desired capacitive load. It also gives the slew rate and bandwidth that will be achieved for each case.

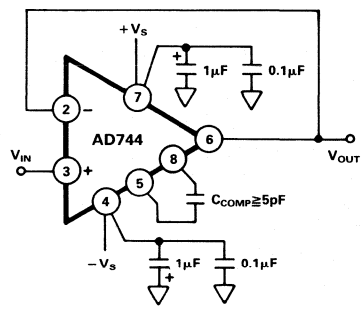


Figure 30. AD744 Connected as a Unity Gain Voltage Follower

Gain	Max C_{LOAD} (pF)	C_{COMP} (pF)	Slew Rate (V/μs)	–3dB Bandwidth (MHz)
1	50	5	37	6.5
1	150	10	25	4.3
1	2000	25	12.5	2.0

Table I. Recommended Values of C_{COMP} vs. Various Capacitive Loads

Figures 31 and 32 show the AD744 as a voltage follower with gain and as an inverting amplifier. In these cases, external compensation is not necessary for stable operation. However, compensation may be applied to drive capacitive loads above 50pF. Table II gives recommended C_{COMP} values, along with expected slew rates and bandwidths for a variety of load conditions and gains for the circuits in Figures 31 and 32.

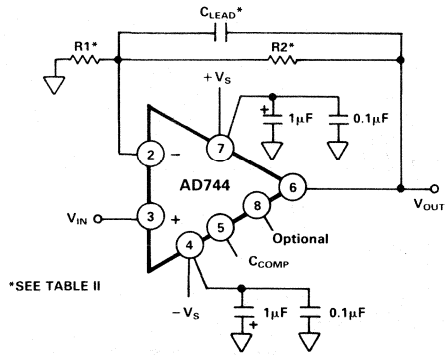


Figure 31. AD744 Connected as a Voltage Follower Operating at Gains of 2 or Greater

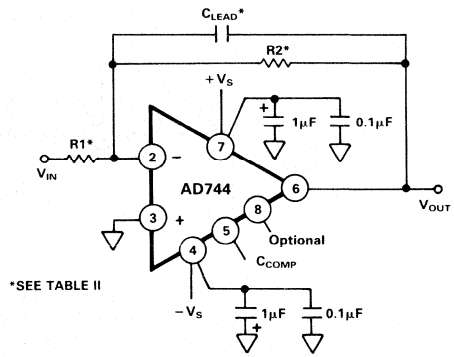


Figure 32. AD744 Connected as an Inverting Amplifier Operating at Gains of 1 or Greater

R1 (Ω)	R2 (Ω)	Gain Follower	Gain Inverter	Max C_{LOAD} (pF)	C_{COMP} (pF)	C_{LEAD} (pF)	Slew Rate (V/μs)	−3dB Bandwidth (MHz)
4.99k	4.99k	2	1	50	0	7	75	2.5**
4.99k	4.99k	2	1	150	5	7	37	2.3**
4.99k	4.99k	2	1	1000	20	–	14	1.2
4.99k	4.99k	2	1	>2000	25	–	12.5*	1.0
499Ω	4.99k	11	10	270	0	–	75	1.2
499Ω	4.99k	11	10	390	2	–	50	0.85
499Ω	4.99k	11	10	1000	5	–	37*	0.60

*Into large capacitive loads the AD744's 25mA output current limit sets the slew rate of the amplifier, in V/μs, equal to 0.025 amps divided by the value of C_{LOAD} in μF. Slew rate is specified into rated max C_{LOAD} except for cases marked *, which are specified with a 50pF load.
**Bandwidth with C_{LEAD} adjusted for minimum settling time.

Table II. Recommended Values of C_{COMP} vs. Various Load Conditions for the Circuits of Figures 31 and 32.

Using Decompensation to Extend the Gain Bandwidth Product

When the AD744 is used in applications where the closed-loop gain is greater than 10, gain bandwidth product may be enhanced by connecting a small capacitor between Pins 1 and 5 (Figure 33). At low frequencies, this capacitor cancels the effects of the chip's internal compensation capacitor, C_{COMP}, effectively decompensating the amplifier.

Due to manufacturing variations in the value of the internal C_{COMP}, it is recommended that the amplifier's response be optimized for the desired gain by using a 2 to 10pF trimmer capacitor rather than using a fixed value.

R1 (Ω)	R2 (Ω)	Gain Follower	Gain Inverter	−3dB Bandwidth	Gain/BW Product
1k	10k	11	10	2.5MHz	25MHz
100	10k	101	100	760kHz	76MHz
100	100k	1001	1000	225kHz	225MHz

Table III. Performance Summary for the Circuit of Figure 33

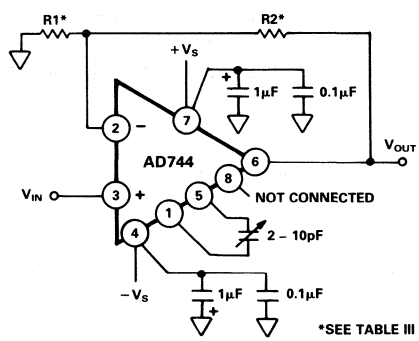


Figure 33. Using the Decompensation Connection to Extend Gain Bandwidth

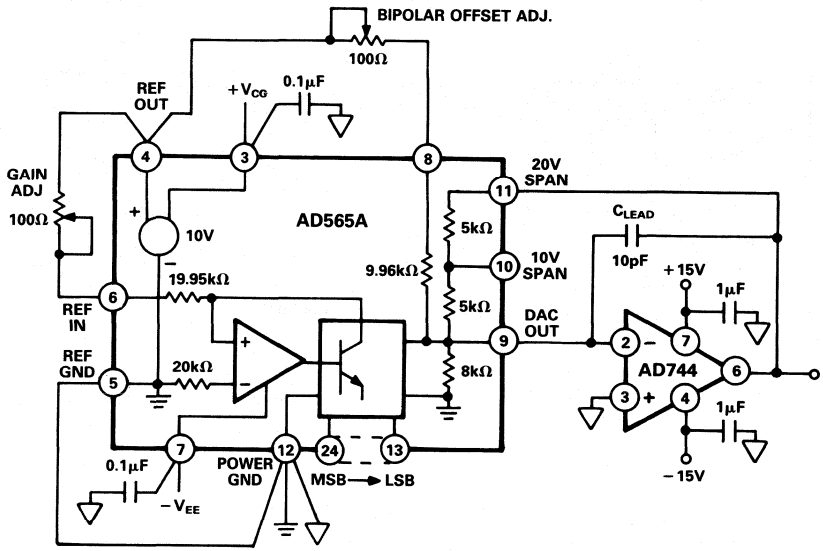


Figure 34. ±10V Voltage Output Bipolar DAC Using the AD744 as an Output Buffer

HIGH-SPEED OP AMP APPLICATIONS AND TECHNIQUES

DAC Buffers (I-to-V Converters)

Digital-to-analog converters which use bipolar transistors to switch currents into (or out of) their outputs can achieve very fast settling times. The AD565A, for example, is specified to settle to 12 bits in less than 250ns, with a current output. However, in many applications, a voltage output is desirable, and it would be useful – perhaps essential – that this I-to-V conversion be accomplished without increasing the settling time or without degrading the accuracy of the DAC.

Figure 34 is a schematic of an AD565A DAC using an AD744 output buffer. The 10pF C_{LEAD} capacitor compensates for the DAC's output capacitance, plus the 5.5pF amplifier input capacitance.

Figure 35 is an oscilloscope photo of the AD744's output voltage with a +10V to 0V step applied; this corresponds to an all "1s" to all "0s" code change on the DAC. Since the DAC is connected in the 20V span mode, 1LSB is equal to 4.88mV. Output settling time for the AD565/AD744 combination is less than 500ns to within a 2.44mV, 1/2LSB error band.

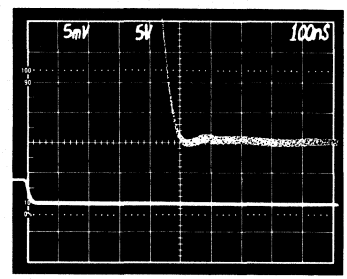


Figure 35. Upper Trace: AD744 Output Voltage for a +10V to 0V Step, Scale: 5mV/div.
Lower Trace: Logic Input Signal, Scale: 5V/div.

A HIGH-SPEED, 3 OP AMP INSTRUMENTATION AMPLIFIER CIRCUIT

The instrumentation amplifier circuit shown in Figure 36 can provide a range of gains from unity up to 1000 and higher. The circuit bandwidth is 4MHz at a gain of 1 and 750kHz at a gain of 10; settling time for the entire circuit is less than 2μs to within 0.01% for a 10V step, (G=10).

While the AD744 is not stable with 100% negative feedback (as when connected as a standard voltage follower), phase margin and therefore stability at unity gain may be increased to an acceptable level by placing the parallel combination of a resistor and a small lead capacitor between each amplifier's output and its inverting input terminal.

The only penalty associated with this method is a small bandwidth reduction at low gains. The optimum value for C_{LEAD} may be determined from the graph of Figure 41. This technique can be used in the circuit of Figure 36 to achieve stable operation at gains from unity to over 1000.

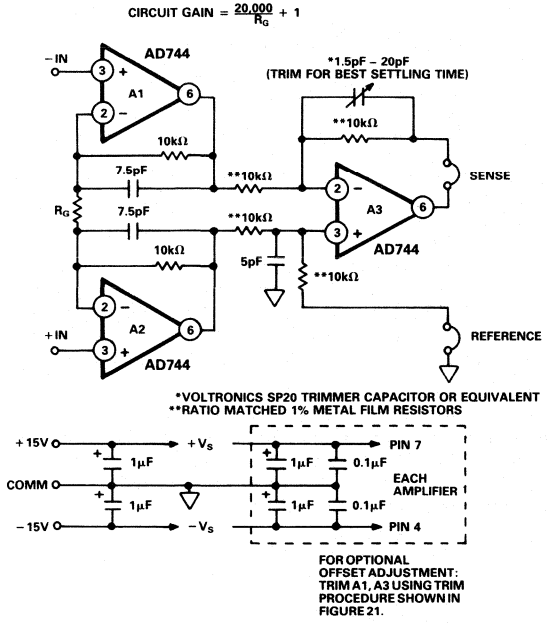


Figure 36. A High Performance, 3 Op Amp Instrumentation Amplifier Circuit

Gain	R_G	Bandwidth	T Settle (0.01%)
1	NC	3.5MHz	1.5μs
2	20kΩ	2.5MHz	1.0μs
10	2.22kΩ	1MHz	2μs
100	202Ω	290kHz	5μs

Table IV. Performance Summary for the 3 Op Amp Instrumentation Amplifier Circuit

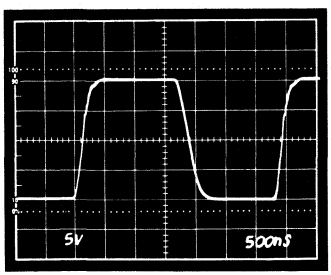


Figure 37. The Pulse Response of the 3 Op Amp Instrumentation Amplifier. Gain = 1, Horizontal Scale: 0.5μV/div., Vertical Scale: 5V/div. (Gain = 10)

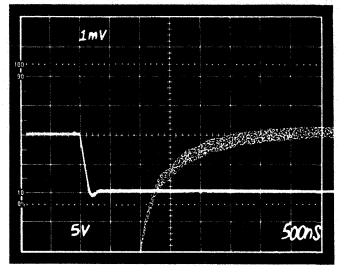


Figure 38. Settling Time of the 3 Op Amp Instrumentation Amplifier. Horizontal Scale: 500ns/div., Vertical Scale, Pulse Input: 5V/div., Output Settling: 1mV/div.

Minimizing Settling Time in Real-World Applications

An amplifier with a "single pole" or "ideal" integrator open-loop frequency response will achieve the minimum possible settling time for any given unity-gain bandwidth. However, when this "ideal" amplifier is used in a practical circuit, the actual settling time is increased above the minimum value because of added time constants which are introduced due to additional capacitance on the amplifier's summing junction. The following discussion will explain how to minimize this increase in settling time by the selection of the proper value for feedback capacitor, C_L.

If an op amp is modeled as an ideal integrator with a unity gain crossover frequency, f_O, Equation 1 will accurately describe the small signal behavior of the circuit of Figure 39. This circuit models an op amp connected as an I-to-V converter.

Equation 1 would completely describe the output of the system if not for the op amp's finite slew rate and other nonlinear effects. Even considering these effects, the fine scale settling to <0.1% will be determined by the op amp's small signal behavior.

Equation 1.

$$\frac{V_O}{I_{IN}} = \frac{-R}{\frac{R\,(C_L + C_X)}{2\pi F_O}\,s^2 + \left(\frac{G_N}{2\pi F_O} + R\,C_L\right)s + 1}$$

Where F_O = the op amp's unity gain crossover frequency

G_N = the "noise" gain of the circuit $\left(1 + \frac{R}{R_O}\right)$

This Equation May Then Be Solved for C_L:

Equation 2.

$$C_L = \frac{2 - G_N}{R\,2\pi F_O} + \frac{2\sqrt{RC_X\,2\pi F_O + (1 - G_N)}}{R\,2\pi F_O}$$

In these equations, capacitance C_X is the total capacitance appearing at the inverting terminal of the op amp. When modeling an I-to-V converter application, the Norton equivalent circuit of Figure 39 can be used directly. Capacitance C_X is the total capacitance of the output of the current source plus the input capacitance of the op amp, which includes any stray capacitance at the op amp's input.

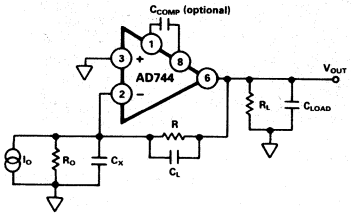


Figure 39. A Simplified Model of the AD744 Used as a Current-to-Voltage Converter

When R_O and I_O are replaced with their Thevenin V_{IN} and R_{IN} equivalents, the general purpose inverting amplifier model of Figure 40 is created. Here capacitor C_X represents the input capacitance of the AD744 (5.5pF) plus any stray capacitance due to wiring and the type of IC package employed.

In either case, the capacitance C_X causes the system to go from a one-pole to a two-pole response; this additional pole increases settling time by introducing peaking or ringing in the op amp's output. If the value of C_X can be estimated with reasonable accuracy, Equation 2 can be used to choose the correct value for a small capacitor, C_L, which will optimize amplifier response. If the value of C_X is not known, C_L should be a variable capacitor.

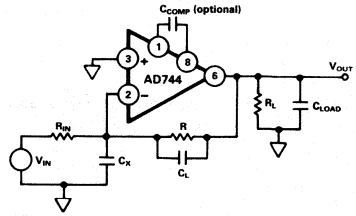


Figure 40. A Simplified Model of the AD744 Used as an Inverting Amplifier

As an aid to the designer, the optimum value of C_L for one specific amplifier connection can be determined from the graph of Figure 41. This graph has been produced for the case where the AD744 is connected as in Figures 39 and 40 with a practical minimum value for C_{STRAY} of 2pF and a total C_X value of 7.5pF.

The approximate value of C_L can be determined for almost any application by solving Equation 2. For example, the AD565/AD744 circuit of Figure 34 constrains all the variables of Equation 2 ($G_N = 3.25$, $R = 10k\Omega$, $F_O = 13MHz$, and $C_X = 32.5pF$). Therefore, under these conditions, $C_L = 10.5pF$.

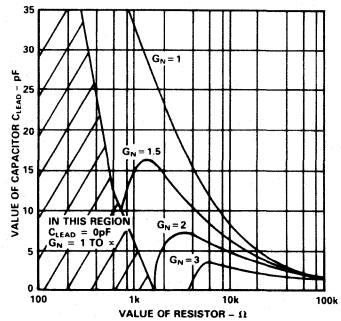


Figure 41. Practical Values of C_L vs. Resistance of R for Various Amplifier Noise Gains

Ultralow Noise, High Speed, BiFET Op Amp

AD745

FEATURES

ULTRALOW NOISE PERFORMANCE
- 2.9 nV/$\sqrt{Hz}$ at 10 kHz
- 0.38 μV p–p, 0.1 Hz to 10 Hz
- 6.9 fA/$\sqrt{Hz}$ Current Noise at 1 kHz

EXCELLENT AC PERFORMANCE
- 12.5 V/μs Slew Rate
- 20 MHz Gain Bandwidth Product
- THD = 0.0002% @ 1 kHz
- Internally Compensated for Gains of +5 (or −4) or Greater

EXCELLENT DC PERFORMANCE
- 0.5 mV max Offset Voltage
- 250 pA max Input Bias Current
- 2000 V/mV min Open Loop Gain
- Available in Tape and Reel in Accordance with EIA-481A Standard

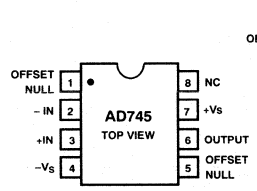
APPLICATIONS
- Sonar
- Photodiode and IR Detector Amplifiers
- Accelerometers
- Low Noise Preamplifiers
- High Performance Audio

PRODUCT DESCRIPTION

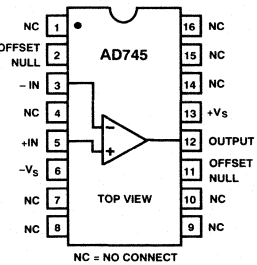
The AD745 is an ultralow noise, high speed, FET input operational amplifier. It offers both the ultralow voltage noise and high speed generally associated with bipolar input op amps and the very low input currents of FET input devices. Its 20 MHz bandwidth and 12.5 V/μs slew rate makes the AD745 an ideal amplifier for high speed applications demanding low noise and high dc precision. Furthermore, the AD745 does not exhibit an output phase reversal.

CONNECTION DIAGRAMS

8-Pin Plastic Mini-DIP (N) & 8-Pin Cerdip (Q) Packages



16-Pin SOIC (R) Package

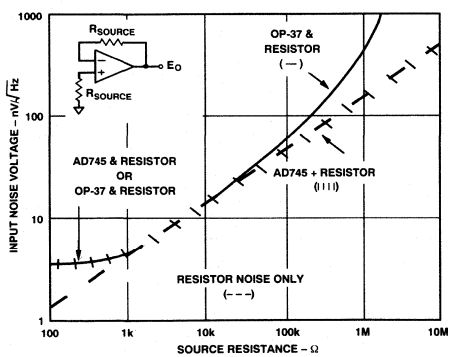


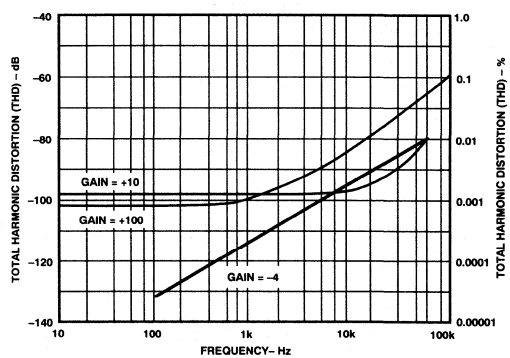
NC = NO CONNECT

The AD745's guaranteed, tested maximum input voltage noise of 4 nV/$\sqrt{Hz}$ at 10 kHz is unsurpassed for a FET-input monolithic op amp, as is its maximum 1.0 μV p–p noise in a 0.1 to 10 Hz bandwidth. The AD745 also has excellent dc performance with 250 pA maximum input bias current and 0.5 mV maximum offset voltage.

The internal compensation of the AD745 is optimized for higher gains, providing a much higher bandwidth and a faster slew rate. This makes the AD745 especially useful as a preamplifier where low level signals require an amplifier that provides both high amplification and wide bandwidth at these higher gains. The AD745 is available in five performance grades. The AD745J and AD745K are rated over the commercial temperature range of 0°C to +70°C. The AD745A and AD745B are rated over the industrial temperature range of −40°C to +85°C. The AD745S is rated over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

The AD745 is available in 8-pin plastic mini-DIP, 8-pin cerdip, 16-pin SOIC, or in chip form.





AD745—SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD745J/A Min	AD745J/A Typ	AD745J/A Max	AD745K/B Min	AD745K/B Typ	AD745K/B Max	AD745S Min	AD745S Typ	AD745S Max	Units
INPUT OFFSET VOLTAGE[1]											
Initial Offset			0.25	1.0/0.8		0.1	0.5/0.25		0.25	1.0	mV
Initial Offset	T_{min} to T_{max}			1.5			1.0/0.50			2.0	mV
vs. Temp.	T_{min} to T_{max}		2			2			2		μV/°C
vs. Supply (PSRR)	12 V to 18 V[2]	90	96		100	106		90	96		dB
vs. Supply (PSRR)	T_{min} to T_{max}	88			98	105		88			dB
INPUT BIAS CURRENT[3]											
Either Input	V_{CM} = 0 V		150	400		150	250		150	400	pA
Either Input @ T_{max}	V_{CM} = 0 V			8.8/25.6			5.5/16			413	nA
Either Input	V_{CM} = +10 V		250	600		250	400		300	600	pA
Either Input, V_S = ±5 V	V_{CM} = 0 V		30	200		30	125		30	200	pA
INPUT OFFSET CURRENT	V_{CM} = 0 V		40	150		30	75		40	150	pA
Offset Current @ T_{max}	V_{CM} = 0 V			2.2/6.4			1.1/3.2			102	nA
FREQUENCY RESPONSE											
Gain BW, Small Signal	G = −4		20			20			20		MHz
Full Power Response	V_O = 20 V p-p		120			120			120		kHz
Slew Rate	G = −4		12.5			12.5			12.5		V/μs
Settling Time to 0.01%			5			5			5		μs
Total Harmonic Distortion[4]	f = 1 kHz G = −4		0.0002			0.0002			0.0002		%
INPUT IMPEDANCE											
Differential			$1 \times 10^{10} \| 20$			$1 \times 10^{10} \| 20$			$1 \times 10^{10} \| 20$		Ω|pF
Common Mode			$3 \times 10^{11} \| 18$			$3 \times 10^{11} \| 18$			$3 \times 10^{11} \| 18$		Ω|pF
INPUT VOLTAGE RANGE											
Differential[5]			±20			±20			±20		V
Common-Mode Voltage			+13.3, −10.7			+13.3, −10.7			+13.3, −10.7		V
Over Max Operating Range[6]		−10		+12	−10		+12	−10		+12	V
Common-Mode Rejection Ratio	V_{CM} = ±10 V	80	95		90	102		80	95		dB
	T_{min} to T_{max}	78			88			78			dB
INPUT VOLTAGE NOISE	0.1 to 10 Hz		0.38			0.38	1.0		0.38		μV p-p
	f = 10 Hz		5.5			5.5	10.0		5.5		nV/√Hz
	f = 100 Hz		3.6			3.6	6.0		3.6		nV/√Hz
	f = 1 kHz		3.2	5.0		3.2	5.0		3.2	5.0	nV/√Hz
	f = 10 kHz		2.9	4.0		2.9	4.0		2.9	4.0	nV/√Hz
INPUT CURRENT NOISE	f = 1 kHz		6.9			6.9			6.9		fA/√Hz
OPEN LOOP GAIN	V_O = ±10 V										
	R_{LOAD} ≥ 2 kΩ	1000	4000		2000	4000		1000	4000		V/mV
	T_{min} to T_{max}	800			1800			800			V/mV
	R_{LOAD} = 600 Ω		1200			1200			1200		V/mV
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD} ≥ 600 Ω	+13, −12			+13, −12			+13, −12			V
	R_{LOAD} ≥ 600 Ω		+13.6, −12.6			+13.6, −12.6			+13.6, −12.6		V
	T_{min} to T_{max}	+12, −10			+12, −10			+12, −10			V
	R_{LOAD} ≥ 2 kΩ	±12	+13.8, −13.1		±12	+13.8, −13.1		±12	+13.8, −13.1		V
Current	Short Circuit	20	40		20	40		20	40		mA
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		±4.8		±18	±4.8		±18	±4.8		±18	V
Quiescent Current			8	10.0		8	10.0		8	10.0	mA
TRANSISTOR COUNT	# of Transistors		50			50			50		

NOTES
[1]Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[2]Test conditions: $+V_S$ = 15 V, $-V_S$ = 12 V to 18 V and $+V_S$ = 12 V to +18 V, $-V_S$ = 15 V.
[3]Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperature, the current doubles every 10°C.
[4]Gain = −4, R_L = 2 kΩ, C_L = 10 pF.
[5]Defined as voltage between inputs, such that neither exceeds ±10 V from common.
[6]The AD745 does not exhibit an output phase reversal when the negative common-mode limit is exceeded.

All min and max specifications are guaranteed.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
Plastic Package . . . . . 1.3 W
Cerdip Package . . . . . 1.1 W
SOIC Package . . . . . 1.2 W
Input Voltage . . . . . $\pm V_S$
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range (Q) . . . . . −65°C to +150°C
Storage Temperature Range (N, R) . . . . . −65°C to +125°C
Operating Temperature Range
AD745J/K . . . . . 0°C to +70°C
AD745A/B . . . . . −40°C to +85°C
AD745S . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 seconds) . . . . . 300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-pin plastic package: θ_{JA} = 100°C/Watt, θ_{JC} = 50°C/Watt
8-pin cerdip package: θ_{JA} = 110°C/Watt, θ_{JC} = 30°C/Watt
16-pin plastic SOIC package: θ_{JA} = 100°C/Watt, θ_{JC} = 30°C/Watt

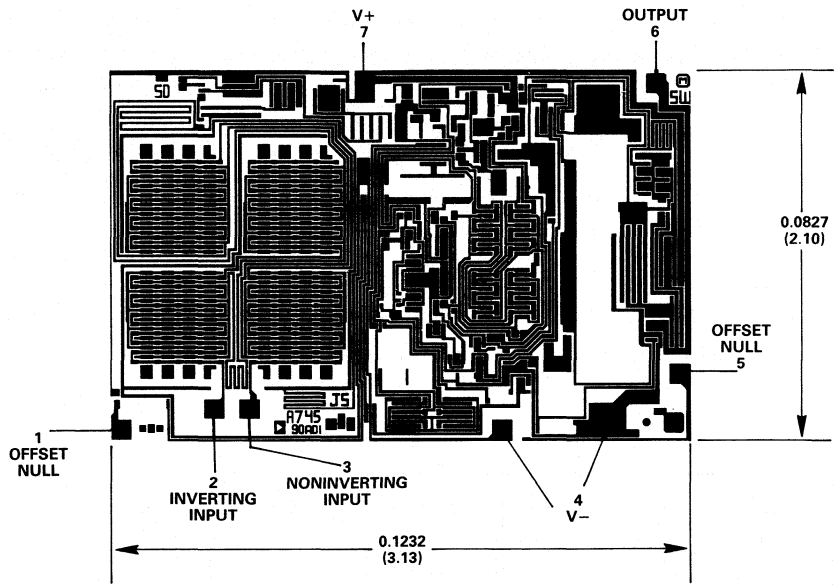
ESD SUSCEPTIBILITY

An ESD classification per method 3015.6 of MIL STD 883C has been performed on the AD745, which is a class 1 device. Using an IMCS 5000 automated ESD tester, the two null pins will pass at voltages up to 1000 volts, while all other pins will pass at voltages exceeding 2500 volts.

2

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



ORDERING GUIDE

Model	Temperature Range	Package Options*
AD745JN	0°C to +70°C	N-8
AD745KN	0°C to +70°C	N-8
AD745AN	−40°C to +85°C	N-8
AD745JR	0°C to +70°C	R-16
AD745AR	−40°C to +85°C	R-16
AD745AQ	−40°C to +85°C	Q-8
AD745BQ	−40°C to +85°C	Q-8
AD745SQ	−55°C to +125°C	Q-8
AD745SQ/883B	−55°C to +125°C	Q-8
AD745J Chips	0°C to +70°C	
AD745S Chips	−55°C to +125°C	

*N = Plastic DIP; R = Small Outline IC; Q = Cerdip. For outline information see Package Information section.

AD745—Typical Characteristics (@ +25°C, V_S = ±15 V unless otherwise noted)

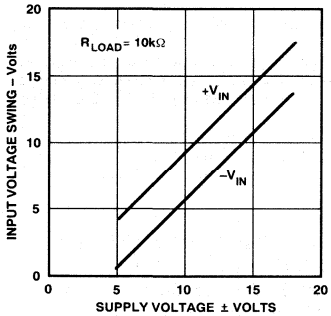


Figure 1. Input Voltage Swing vs. Supply Voltage

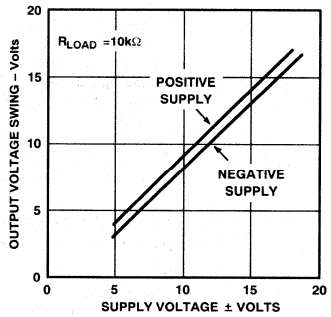


Figure 2. Output Voltage Swing vs. Supply Voltage

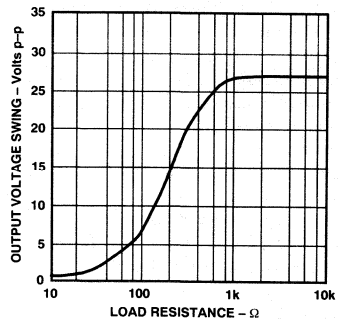


Figure 3. Output Voltage Swing vs. Load Resistance

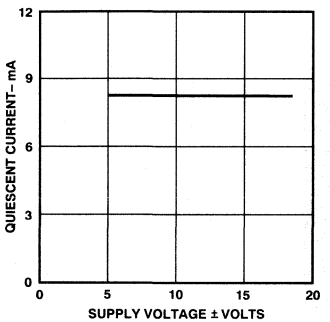


Figure 4. Quiescent Current vs. Supply Voltage

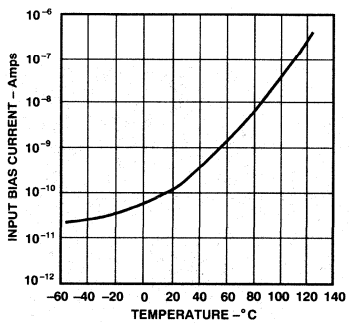


Figure 5. Input Bias Current vs. Temperature

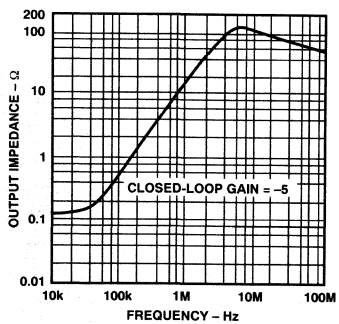


Figure 6. Output Impedance vs. Frequency

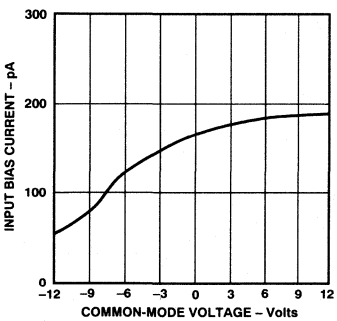


Figure 7. Input Bias Current vs. Common-Mode Voltage

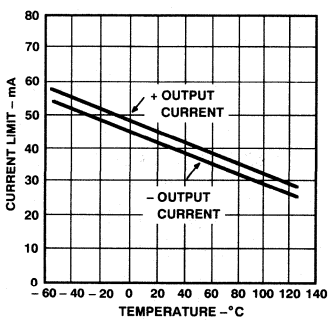


Figure 8. Short Circuit Current Limit vs. Temperature

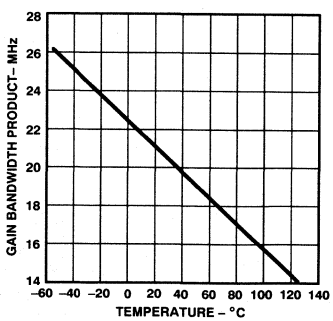


Figure 9. Gain Bandwidth Product vs. Temperature

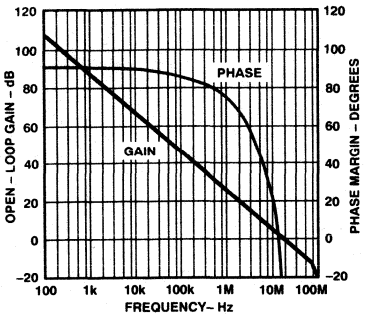


Figure 10. Open-Loop Gain and Phase vs. Frequency

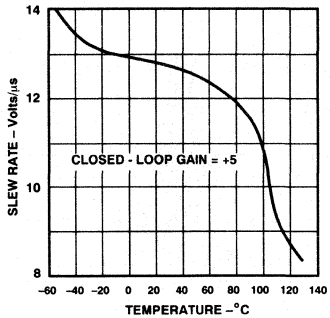


Figure 11. Slew Rate vs. Temperature

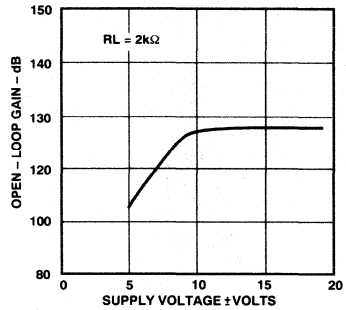


Figure 12. Open-Loop Gain vs. Supply Voltage

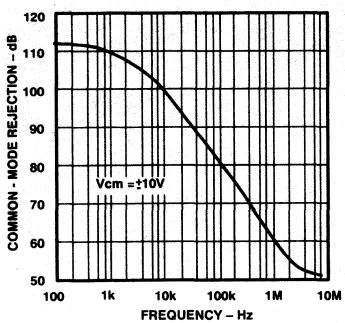


Figure 13. Common-Mode Rejection vs. Frequency

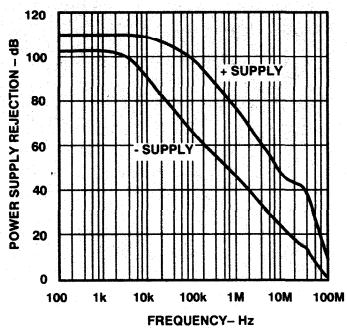


Figure 14. Power Supply Rejection vs. Frequency

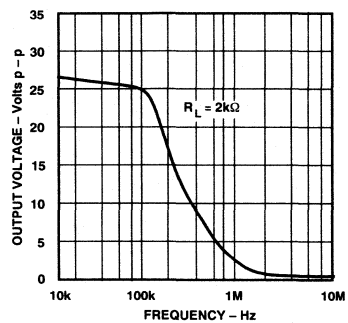


Figure 15. Large Signal Frequency Response

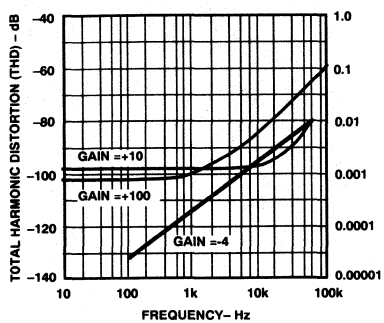


Figure 16. Total Harmonic Distortion vs. Frequency

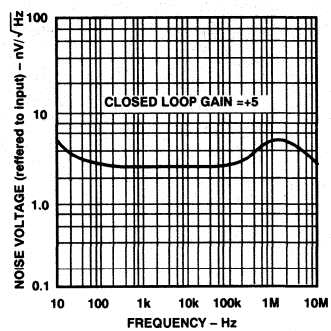


Figure 17. Input Noise Voltage Spectral Density

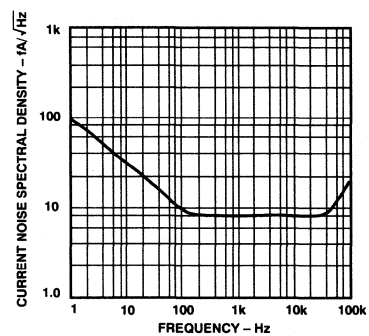


Figure 18. Input Noise Current Spectral Density

AD745—Typical Characteristics

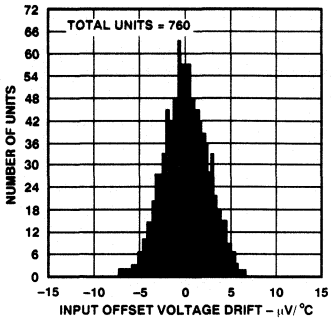


Figure 19. Distribution of Offset Voltage Drift. T_A = +25°C to +125°C

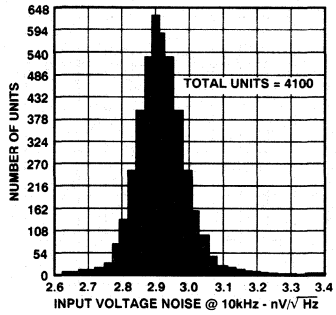


Figure 20. Typical Input Noise Voltage Distribution @ 10 kHz

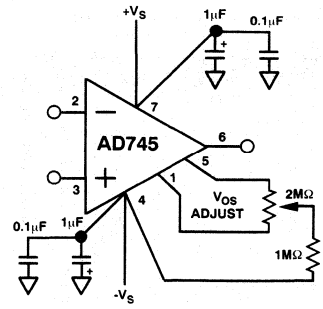


Figure 21 . Offset Null Configuration, 8-Pin Package Pinout

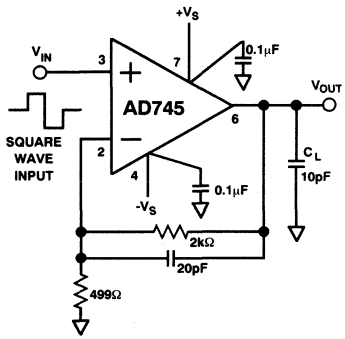


Figure 22a. Gain of 5 Follower, 8-Pin Package Pinout

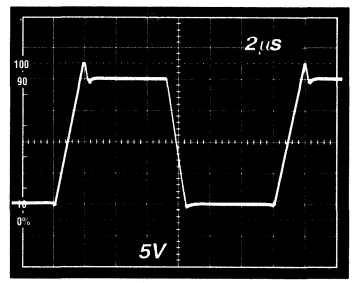


Figure 22b. Gain of 5 Follower Large Signal Pulse Response

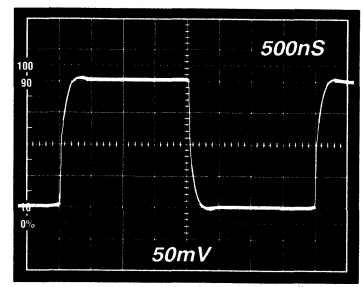


Figure 22c. Gain of 5 Follower Small Signal Pulse Response

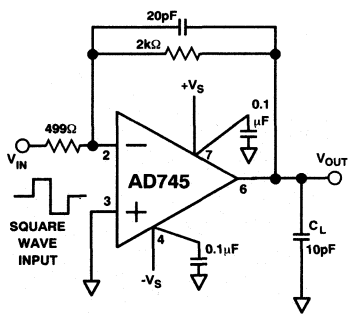


Figure 23a. Gain of 4 Inverter, 8-Pin Package Pinout

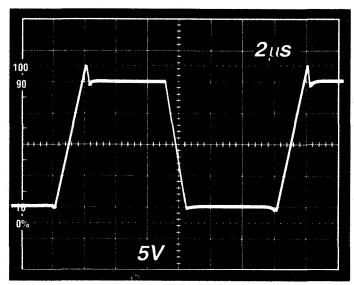


Figure 23b. Gain of 4 Inverter Large Signal Pulse Response

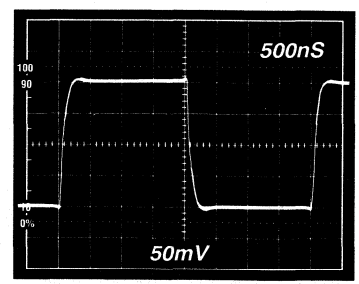


Figure 23c. Gain of 4 Inverter Small Signal Pulse Response

OP AMP PERFORMANCE: JFET VS. BIPOLAR

The AD745 offers the low input voltage noise of an industry-standard bipolar op amp without its inherent input current errors. This is demonstrated in Figure 24, which compares input voltage noise vs. input source resistance of the OP-37 and the AD745 op amps. From this figure, it is clear that at high source impedance the low current noise of the AD745 also provides lower total noise. It is also important to note that with the AD745 this noise reduction extends all the way down to low source impedances. The lower dc current errors of the AD745 also reduce errors due to offset and drift at high source impedances (Figure 25).

The internal compensation of the AD745 is optimized for higher gains, providing a much higher bandwidth and a faster slew rate. This makes the AD745 especially useful as a preamplifier, where low level signals require an amplifier that provides both high amplification and wide bandwidth at these higher gains.

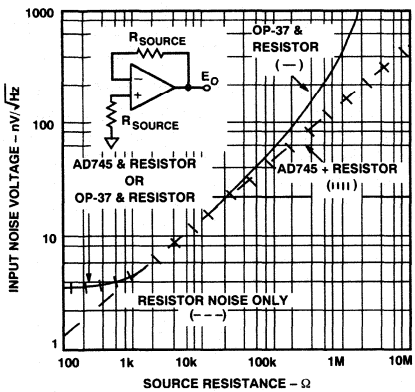


Figure 24. Total Input Noise Spectral Density @ 1 kHz vs. Source Resistance

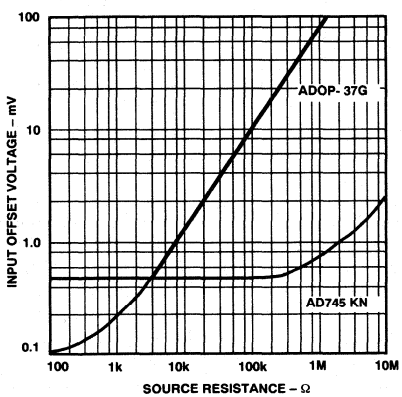


Figure 25. Input Offset Voltage vs. Source Resistance

DESIGNING CIRCUITS FOR LOW NOISE

An op amp's input voltage noise performance is typically divided into two regions: flatband and low frequency noise. The AD745 offers excellent performance with respect to both. The figure of 2.9 nV/$\sqrt{\text{Hz}}$ @ 10 kHz is excellent for a JFET input amplifier. The 0.1 to 10 Hz noise is typically 0.38 μV p–p. The user should pay careful attention to several design details in order to optimize low frequency noise performance. Random air currents can generate varying thermocouple voltages that appear as low frequency noise: therefore sensitive circuitry should be well shielded from air flow. Keeping absolute chip temperature low also reduces low frequency noise in two ways: first, the low frequency noise is strongly dependent on the ambient temperature and increases above +25°C. Secondly, since the gradient of temperature from the IC package to ambient is greater, the noise generated by random air currents, as previously mentioned, will be larger in magnitude. Chip temperature can be reduced both by operation at reduced supply voltages and by the use of a suitable clip-on heat sink, if possible.

Low frequency current noise can be computed from the magnitude of the dc bias current ($\widetilde{I}_n = \sqrt{2qI_B\Delta f}$) and increases below approximately 100 Hz with a 1/f power spectral density. For the AD745 the typical value of current noise is 6.9 fA/$\sqrt{\text{Hz}}$ at 1 kHz. Using the formula, $\widetilde{I}_n = \sqrt{4kT/R\Delta f}$, to compute the Johnson noise of a resistor, expressed as a current, one can see that the current noise of the AD745 is equivalent to that of a 3.45×10^8 Ω source resistance.

At high frequencies, the current noise of a FET increases proportionately to frequency. This noise is due to the "real" part of the gate input impedance, which decreases with frequency. This noise component usually is not important, since the voltage noise of the amplifier impressed upon its input capacitance is an apparent current noise of approximately the same magnitude.

In any FET input amplifier, the current noise of the internal bias circuitry can be coupled externally via the gate-to-source capacitances and appears as input current noise. This noise is totally correlated at the inputs, so source impedance matching will tend to cancel out its effect. Both input resistance and input capacitance should be balanced whenever dealing with source capacitances of less than 300 pF in value.

LOW NOISE CHARGE AMPLIFIERS

As stated, the AD745 provides both low voltage and low current noise. This combination makes this device particularly suitable in applications requiring very high charge sensitivity, such as capacitive accelerometers and hydrophones. When dealing with a high source capacitance, it is useful to consider the total input charge uncertainty as a measure of system noise.

Charge (Q) is related to voltage and current by the simply stated fundamental relationships:

$$Q = CV \text{ and } I = \frac{dQ}{dt}$$

As shown, voltage, current and charge noise can all be directly related. The change in open circuit voltage (ΔV) on a capacitor will equal the combination of the change in charge (ΔQ/C) and the change in capacitance with a built-in charge (Q/ΔC).

Figures 26 and 27 show two ways to buffer and amplify the output of a charge output transducer. Both require using an amplifier which has a very high input impedance, such as the AD745. Figure 26 shows a model of a charge amplifier circuit. Here, amplification depends on the principle of conservation of charge at the input of amplifier A1, which requires that the charge on capacitor C_S be transferred to capacitor C_F, thus yielding an output voltage of $\Delta Q/C_F$. The amplifiers input voltage noise will appear at the output amplified by the noise gain $(1 + (C_S/C_F))$ of the circuit.

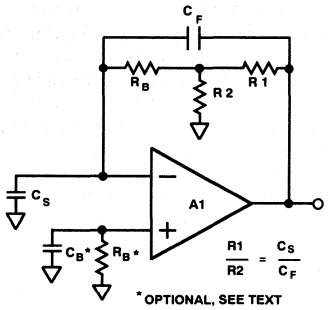


Figure 26. A Charge Amplifier Circuit

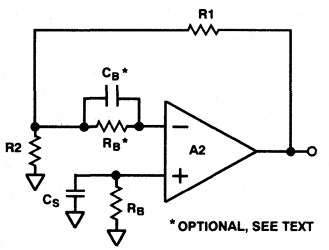


Figure 27. Model for A High Z Follower with Gain

The second circuit, Figure 27, is simply a high impedance follower with gain. Here the noise gain $(1 + (R1/R2))$ is the same as the gain from the transducer to the output. Resistor R_B, in both circuits, is required as a dc bias current return.

There are three important sources of noise in these circuits. Amplifiers A1 and A2 contribute both voltage and current noise, while resistor R_B contributes a current noise of:

$$\tilde{N} = \sqrt{4\,k\,\frac{T}{R_B}}\,\Delta f$$

where:

k = Boltzman's Constant = 1.381×10^{-23} Joules/Kelvin

T = Absolute Temperature, Kelvin (0°C = +273.2 Kelvin)

Δf = Bandwidth – in Hz (Assuming an Ideal "Brick Wall" Filter)

This must be root-sum-squared with the amplifier's own current noise.

Figure 28 shows that these two circuits have an identical frequency response and the same noise performance (provided that C_S/C_F = R1/R2). One feature of the first circuit is that a "T" network is used to increase the effective resistance of R_B and improve the low frequency cutoff point by the same factor.

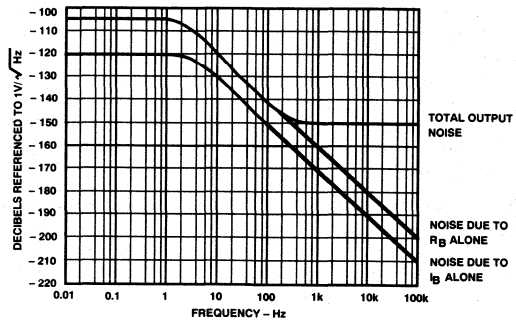


Figure 28. Noise at the Outputs of the Circuits of Figures 26 and 27. Gain = 10, C_S = 3000 pF, R_B = 22 MΩ

However, this does not change the noise contribution of R_B which, in this example, dominates at low frequencies. The graph of Figure 29 shows how to select an R_B large enough to minimize this resistor's contribution to overall circuit noise. When the equivalent current noise of R_B $((\sqrt{4\,kT})/R)$ equals the noise of I_B $(\sqrt{2\,qI_B})$, there is diminishing return in making R_B larger.

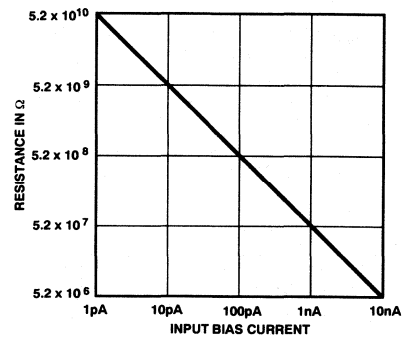


Figure 29. Graph of Resistance vs. Input Bias Current Where the Equivalent Noise $\sqrt{4\,kT/R}$, Equals the Noise of the Bias Current $\sqrt{2\,qI_B}$

To maximize dc performance over temperature, the source resistances should be balanced on each input of the amplifier. This is represented by the optional resistor R_B in Figures 26 and 27. As previously mentioned, for best noise performance care should be taken to also balance the source capacitance designated by C_B. The value for C_B in Figure 26 would be equal to C_S in Figure 27. At values of C_B over 300 pF, there is a diminishing impact on noise; capacitor C_B can then be simply a large mylar bypass capacitor of 0.01 μF or greater.

HOW CHIP PACKAGE TYPE AND POWER DISSIPATION AFFECT INPUT BIAS CURRENT

As with all JFET input amplifiers, the input bias current of the AD745 is a direct function of device junction temperature, I_B approximately doubling every 10°C. Figure 30 shows the relationship between bias current and junction temperature for the AD745. This graph shows that lowering the junction temperature will dramatically improve I_B.

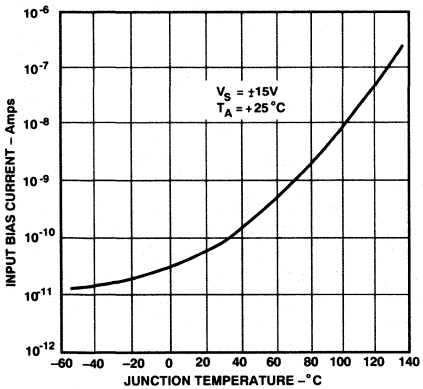
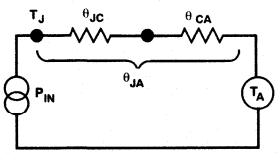


Figure 30. Input Bias Current vs. Junction Temperature

The dc thermal properties of an IC can be closely approximated by using the simple model of Figure 31 where current represents power dissipation, voltage represents temperature, and resistors represent thermal resistance (θ in °C/watt).



WHERE:
P_{IN} = DEVICE DISSIPATION
T_A = AMBIENT TEMPERATURE
T_J = JUNCTION TEMPERATURE
θ_{JC} = THERMAL RESISTANCE – JUNCTION TO CASE
θ_{CA} = THERMAL RESISTANCE – CASE TO AMBIENT

Figure 31. Device Thermal Model

From this model $T_J = T_A + \theta_{JA} P_{IN}$. Therefore, I_B can be determined in a particular application by using Figure 30 together with the published data for θ_{JA} and power dissipation. The user can modify θ_{JA} by use of an appropriate clip-on heat sink such as the Aavid #5801. θ_{JA} is also a variable when using the AD745 in chip form. Figure 32 shows bias current vs. supply voltage with θ_{JA} as the third variable. This graph can be used to predict bias current after θ_{JA} has been computed. Again bias current will double for every 10°C. The designer using the AD745 in chip form (Figure 33) must also be concerned with both θ_{JC} and θ_{CA}, since θ_{JC} can be affected by the type of die mount technology used.

Typically, θ_{JC}'s will be in the 3°C to 5°C/watt range; therefore, for normal packages, this small power dissipation level may be ignored. But, with a large hybrid substrate, θ_{JC} will dominate proportionately more of the total θ_{JA}.

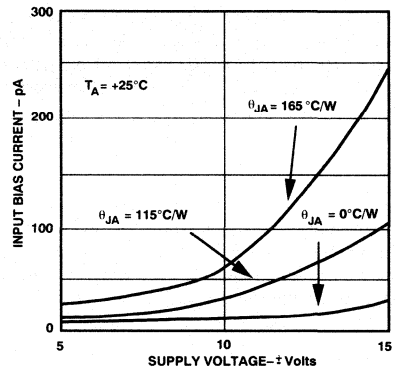


Figure 32. Input Bias Current vs. Supply Voltage for Various Values of θ_{JA}

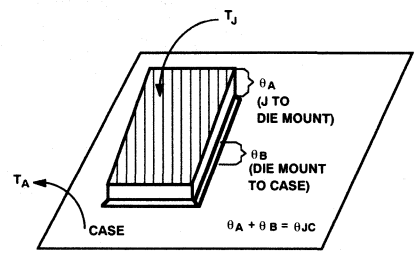
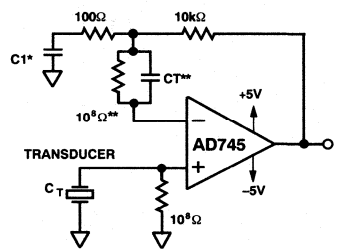


Figure 33. Breakdown of Various Package Thermal Resistance

REDUCED POWER SUPPLY OPERATION FOR LOWER I_B

Reduced power supply operation lowers I_B in two ways: first, by lowering both the total power dissipation and, second, by reducing the basic gate-to-junction leakage (Figure 32). Figure 34 shows a 40 dB gain piezoelectric transducer amplifier, which operates without an ac coupling capacitor, over the −40°C to +85°C temperature range. If the optional coupling capacitor, C_1, is used, this circuit will operate over the entire −55°C to +125°C temperature range.



*OPTIONAL DC BLOCKING CAPACITOR
**OPTIONAL, SEE TEXT

Figure 34. A Piezoelectric Transducer

TWO HIGH PERFORMANCE ACCELEROMETER AMPLIFIERS

Two of the most popular charge-out transducers are hydrophones and accelerometers. Precision accelerometers are typically calibrated for a charge output (pC/g).* Figures 35a and 35b show two ways in which to configure the AD745 as a low noise charge amplifier for use with a wide variety of piezoelectric accelerometers. The input sensitivity of these circuits will be determined by the value of capacitor C1 and is equal to:

$$\Delta V_{OUT} = \frac{\Delta Q_{OUT}}{C1}$$

The ratio of capacitor C1 to the internal capacitance (C_T) of the transducer determines the noise gain of this circuit ($1 + C_T/C1$). The amplifiers voltage noise will appear at its output amplified by this amount. The low frequency bandwidth of these circuits will be dependent on the value of resistor R1. If a "T" network is used, the effective value is: R1 (1 + R2/R3).

*pC = Picocoulombs
g = Earth's Gravitational Constant

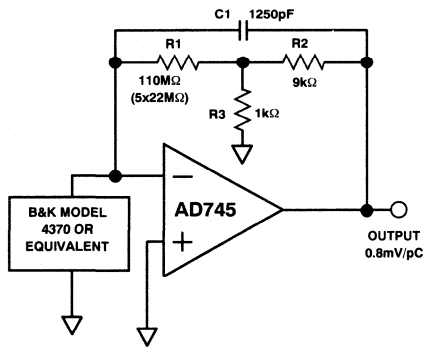


Figure 35a. A Basic Accelerometer Circuit

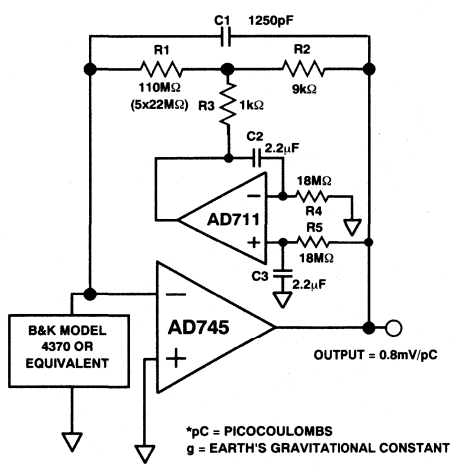


Figure 35b. An Accelerometer Circuit Employing a DC Servo Amplifier

A dc servo loop (Figure 35b) can be used to assure a dc output <10 mV, without the need for a large compensating resistor when dealing with bias currents as large as 100 nA. For optimal low frequency performance, the time constant of the servo loop (R4C2 = R5C3) should be:

$$\text{Time Constant} \geq 10\ R1 \left(1 + \frac{R2}{R3}\right) C1$$

A LOW NOISE HYDROPHONE AMPLIFIER

Hydrophones are usually calibrated in the voltage-out mode. The circuit of Figures 36a can be used to amplify the output of a typical hydrophone. If the optional ac coupling capacitor C_C is used, the circuit will have a low frequency cutoff determined by an RC time constant equal to:

$$\text{Time Constant} = \frac{1}{2\pi \times C_C \times 100\ \Omega}$$

where the dc gain is 1 and the gain above the low frequency cutoff ($1/(2\pi C_C(100\ \Omega))$) is equal to ($1 + R2/R3$). The circuit of Figure 36b uses a dc servo loop to keep the dc output at 0 V and to maintain full dynamic range for I_B's up to 100 nA. The time constant of R7 and C1 should be larger than that of R1 and C_T for a smooth low frequency response.

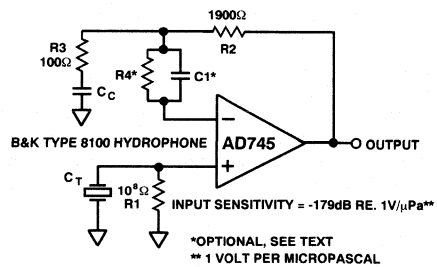


Figure 36a. A Low Noise Hydrophone Amplifier

The transducer shown has a source capacitance of 7500 pF. For smaller transducer capacitances (≤300 pF), lowest noise can be achieved by adding a parallel RC network (R4 = R1, C1 = C_T) in series with the inverting input of the AD745.

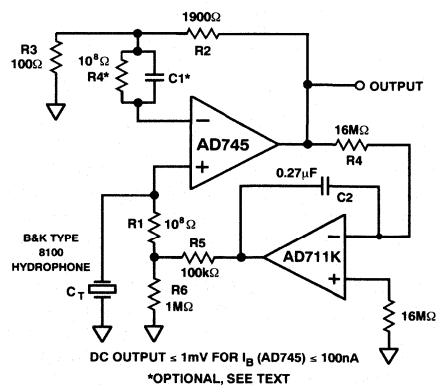


Figure 36b. A Hydrophone Amplifier Incorporating a DC Servo Loop

Design Considerations for I-to-V Converters

There are some simple rules of thumb when designing an I-V converter where there is significant source capacitance (as with a photodiode) and bandwidth needs to be optimized. Consider the circuit of Figure 37. The high frequency noise gain (1 + C_S/C_L) is usually greater than five, so the AD745, with its higher slew rate and bandwidth is ideally suited to this application.

Here both the low current and low voltage noise of the AD745 can be taken advantage of, since it is desirable in some instances to have a large R_F (which increases sensitivity to input current noise) and, at the same time, operate the amplifier at high noise gain.

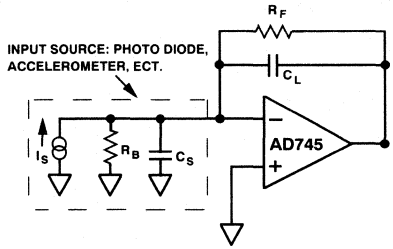


Figure 37. A Model for an I-to-V Converter

In this circuit, the R_F C_S time constant limits the practical bandwidth over which flat response can be obtained, in fact:

$$f_B \approx \sqrt{\frac{f_C}{2\pi R_F C_S}}$$

where:

f_B = signal bandwidth

f_C = gain bandwidth product of the amplifier

With $C_L \approx 1/(2\pi R_F C_S)$ the net response can be adjusted to a provide a two pole system with optimal flatness that has a corner frequency of f_B. Capacitor C_L adjusts the damping of the circuit's response. Note that bandwidth and sensitivity are directly traded off against each other via the selection of R_F. For example, a photodiode with CS = 300 pF and R_F = 100 kΩ will have a maximum bandwidth of 360 kHz when capacitor $C_L \approx 4.5$ pF. Conversely, if only a 100 kHz bandwidth were required, then the maximum value of R_F would be 360 kΩ and that of capacitor C_L still ≈ 4.5 pF.

In either case, the AD745 provides impedance transformation, the effective transresistance, i.e., the I/V conversion gain, may be augmented with further gain. A wideband low noise amplifier such as the AD829 is recommended in this application.

This principle can also be used to apply the AD745 in a high performance audio application. Figure 38 shows that an I-V converter of a high performance DAC, here the AD1862, can be designed to take advantage of the low voltage noise of the AD745 (2.9 nV/$\sqrt{\text{Hz}}$) as well as the high slew rate and bandwidth provided by decompensation. This circuit, with component values shown, has a 12 dB/octave rolloff at 728 kHZ, with a passband ripple of less than 0.001 dB and a phase deviation of less than 2 degrees @ 20 kHz.

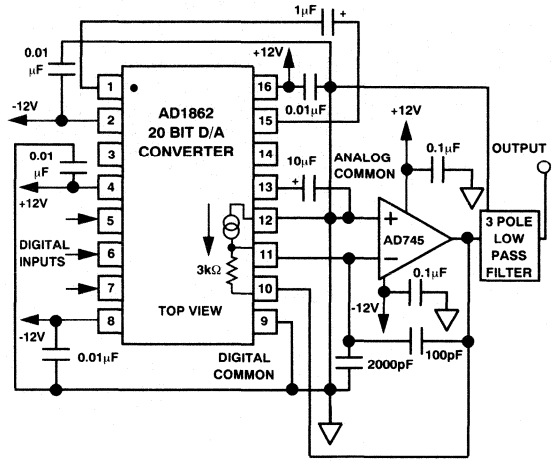


Figure 38. A High Performance Audio DAC Circuit

An important feature of this circuit is that high frequency energy, such as clock feedthrough, is shunted to common via a high quality capacitor and not the output stage of the amplifier, greatly reducing the error signal at the input of the amplifier and subsequent opportunities for intermodulation distortions.

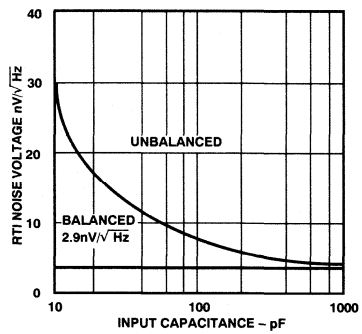


Figure 39. RTI Noise Voltage vs. Input Capacitance

BALANCING SOURCE IMPEDANCES

As mentioned previously, it is good practice to balance the source impedances (both resistive and reactive) as seen by the inputs of the AD745. Balancing the resistive components will optimize dc performance over temperature because balancing will mitigate the effects of any bias current errors. Balancing input capacitance will minimize ac response errors due to the amplifier's input capacitance and, as shown in Figure 39, noise performance will be optimized. Figure 40 shows the required external components for noninverting (A) and inverting (B) configurations.

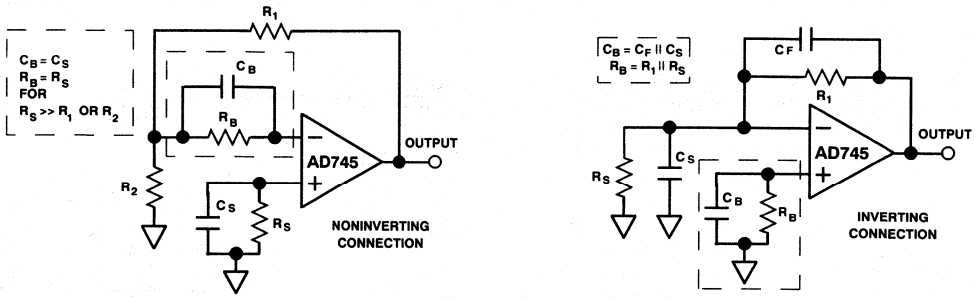


Figure 40. Optional External Components for Balancing Source Impedances

Dual Precision, 500 ns Settling, BiFET Op Amp

AD746

FEATURES

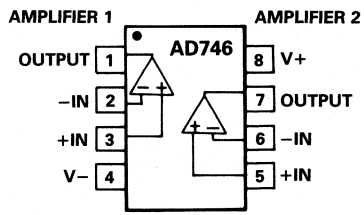
AC PERFORMANCE
- 500 ns Settling to 0.01% for 10 V Step
- 75 V/μs Slew Rate
- 0.0001% Total Harmonic Distortion (THD)
- 13 MHz Gain Bandwidth
- Internal Compensation for Gains of +2 or Greater

DC PERFORMANCE
- 0.5 mV max Offset Voltage (AD746B)
- 10 μV/°C max Drift (AD746B)
- 175 V/mV min Open Loop Gain (AD746B)
- 2 μV p–p Noise, 0.1 Hz to 10 Hz
- Available in Plastic Mini-DIP, Cerdip and Surface Mount Packages
- Available in Tape and Reel in Accordance with EIA-481A Standard
- MIL-STD-883B Processing also Available
- Single Version: AD744

APPLICATIONS
- Dual Output Buffers for 12- and 14-Bit DACs
- Input Buffers for Precision ADCs, Wideband Preamplifiers and Low Distortion Audio Circuitry

CONNECTION DIAGRAM

Plastic Mini-DIP (N)
Cerdip (Q) and
Plastic SOIC (R) Packages



PRODUCT DESCRIPTION

The AD746 is a dual operational amplifier, consisting of two AD744 BiFET op amps on a single chip. These precision monolithic op amps offer excellent dc characteristics plus rapid settling times, high slew rates and ample bandwidths. In addition, the AD746 provides the close matching ac and dc characteristics inherent to amplifiers sharing the same monolithic die.

The single pole response of the AD746 provides fast settling: 500 ns to 0.01%. This feature, combined with its high dc precision, makes it suitable for use as a buffer amplifier for 12- or 14-bit DACs and ADCs. Furthermore, the AD746's low total harmonic distortion (THD) level of 0.0001% and very close matching ac characteristics make it an ideal amplifier for many demanding audio applications.

The AD746 is internally compensated for stable operation as a unity gain inverter or as a noninverting amplifier with a gain of 2 or greater. It is available in four performance grades. The AD746J is rated over the commercial temperature range of 0 to +70°C. The AD746A and AD746B are rated over the industrial temperature range of −40°C to +85°C. The AD746S is rated over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

The AD746 is available in three 8-pin packages: plastic mini-DIP, hermetic cerdip and surface mount (SOIC).

PRODUCT HIGHLIGHTS

1. The AD746 offers exceptional dynamic response for high speed data acquisition systems. It settles to 0.01% in 500 ns and has a 100% tested minimum slew rate of 50 V/μs (AD746B).
2. Outstanding dc precision is provided by a combination of Analog Devices' advanced processing technology, laser wafer drift trimming and well-matched ion-implanted JFETs. Input offset voltage, input bias current and input offset current are specified in the warmed-up condition and are 100% tested.
3. Differential and multichannel systems will benefit from the AD746's very close matching of ac characteristics. Input offset voltage specs are fully tested and guaranteed to a maximum of 0.5 mV (AD746B).
4. The AD746 has very close, guaranteed matching of input bias current between its two amplifiers.
5. Unity gain stable version AD712 also available.

AD746—SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD746J/A Min	AD746J/A Typ	AD746J/A Max	AD746B Min	AD746B Typ	AD746B Max	AD746S Min	AD746S Typ	AD746S Max	Units
INPUT OFFSET VOLTAGE[1]											
Initial Offset			0.3	**1.5**		0.25	**0.5**		0.3	**1.0**	mV
Offset	T_{min} to T_{max}			2.0			**0.7**			**1.5**	mV
vs. Temperature			12	20		5	**10**		12	**20**	μV/°C
vs. Supply[2] (PSRR)		**80**	95		**84**	100		**80**	95		dB
vs. Supply (PSRR)	T_{min} to T_{max}	80			**84**			**80**			dB
Long Term Stability			15			15			15		μV/month
INPUT BIAS CURRENT[3]											
Either Input	V_{CM} = 0 V		110	**250**		110	**150**		110	**250**	pA
Either Input @ T_{max}	V_{CM} = 0 V		2.5/7	5.7/16		7	9.6		113	256	nA
Either Input	V_{CM} = +10 V		145	350		145	**200**		145	**350**	pA
Offset Current	V_{CM} = 0 V		45	**125**		45	**75**		45	**125**	pA
Offset Current @ T_{max}	V_{CM} = 0 V		1.0/3	2.8/8		3	4.8		45	128	nA
MATCHING CHARACTERISTICS											
Input Offset Voltage			0.6	**1.5**		0.3	**0.5**		0.6	**1.0**	mV
Input Offset Voltage	T_{min} to T_{max}			2.0			**0.7**			**1.5**	mV
Input Offset Voltage Drift				20			20			20	μV/°C
Input Bias Current				**125**			**75**			**125**	pA
Crosstalk	@ 1 kHz		120			120			120		dB
	@ 100 kHz		90			90			90		dB
FREQUENCY RESPONSE											
Gain BW, Small Signal	G = −1	8	13		9	13		8	13		MHz
Slew Rate, Unity Gain	G = −1	**45**	75		**50**	75		**45**	75		V/μs
Full Power Response	V_O = 20 V p-p		600			600			600		kHz
Settling Time to 0.01%[4]	G = 1		0.5	0.75		0.5	0.75		0.5	0.75	μs
Total Harmonic Distortion	f = 1 kHz RL≥2 kΩ										
	V_O = 3 V rms		0.0001			0.0001			0.0001		%
INPUT IMPEDANCE											
Differential			$2.5\times10^{11}\|5.5$			$2.5\times10^{11}\|5.5$			$2.5\times10^{11}\|5.5$		Ω|pF
Common Mode			$2.5\times10^{11}\|5.5$			$2.5\times10^{11}\|5.5$			$2.5\times10^{11}\|5.5$		Ω|pF
INPUT VOLTAGE RANGE											
Differential[5]			±20			±20			±20		V
Common-Mode Voltage			+14.5, −11.5			+14.5, −11.5			+14.5, −11.5		V
Over Max Operating Range[6]		**−11**		**+13**	**−11**		**+13**	**−11**		**+13**	V
Common-Mode Rejection Ratio	V_{CM}=±10 V	**78**	88		**82**	88		**78**	88		dB
	T_{min} to T_{max}	76	84		**80**	84		76	84		dB
	V_{CM}=±11 V	**72**	84		**78**	84		**72**	84		dB
	T_{min} to T_{max}	70	80		**74**	80		**70**	80		dB
INPUT VOLTAGE NOISE	0.1 to 10 Hz		2			2			2		μV p-p
	f = 10 Hz		45			45			45		nV/√Hz
	f = 100 Hz		22			22			22		nV/√Hz
	f = 1 kHz		18			18			18		nV/√Hz
	f = 10 kHz		16			16			16		nV/√Hz
INPUT CURRENT NOISE	f = 1 kHz		0.01			0.01			0.01		pA/√Hz
OPEN LOOP GAIN	V_O = ±10 V										
	R_{LOAD}≥2 kΩ	**150**	300		**175**	300		**150**	300		V/mV
	T_{min} to T_{max}	75	200		**75**	200		**65**	175		V/mV
OUTPUT CHARACTERSTICS											
Voltage	R_{LOAD}≥2 kΩ	**+13,−12.5**	+13.9, −13.3		**+13, −12.5**	+13.9, −13.3		**+13,−12.5**	+13.9, −13.3		V
	T_{min} to T_{max}	±12	+13.8, −13.1		**±12**	+13.8, −13.1		**±12**	+13.8, −13.1		V
Current	Short Circuit		25			25			25		mA
Max Capacitive Load	Gain = −1		50			50			50		pF
Driving Capability	Gain= −10		500			500			500		pF
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		**±4.5**		**±18**	**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current			7	**10**		7	**8.0**		7	**10**	mA
TEMPERATURE RANGE											
Rated Performance			0 to +70/−40 to +85			−40 to +85			−55 to +125		°C
PACKAGE OPTIONS[7]											
8-Pin Plastic Mini-DIP (N-8)			AD746JN								
8-Pin Cerdip (Q-8)			AD746AQ			AD746BQ			AD746SQ		
8-Pin Surface Mount (R-8)			AD746JR								
Tape and Reel			AD746JR-REEL								
Chips									AD746SCHIPS		
TRANSISTOR COUNT			54			54			54		

NOTES
[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[2]PSRR test conditions: $+V_S$ = 15 V, $-V_S$ = −12 V to −18 V and $+V_S$ = 12 V to 18 V, $-V_S$ = −15 V.
[3]Bias Current Specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperature, the current doubles every 10°C.
[4]Gain = −1, Rl = 2 k, Cl = 10 pF .
[5]Defined as voltage between inputs, such that neither exceeds ±10 V from ground.
[6]Typically exceeding −14.1 V negative common-mode voltage on either input results in an output phase reversal.
[7]For outline information see Package Information section.

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

2

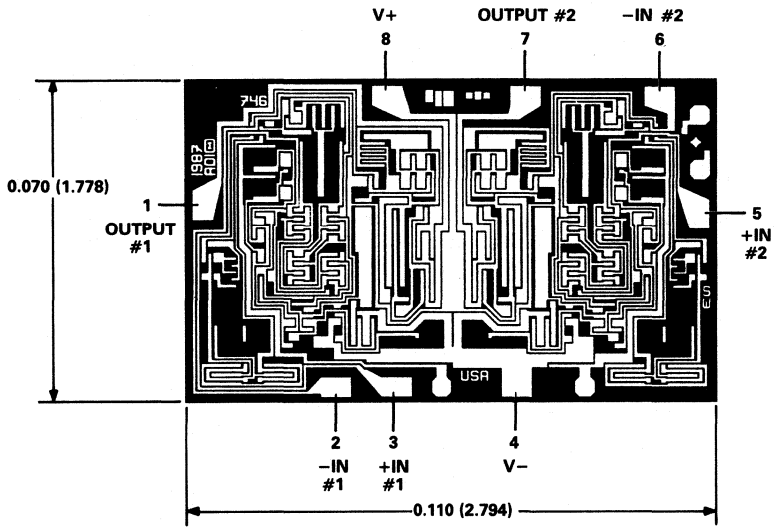
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2] . . . . . 500 mW
Input Voltage . . . . . $\pm V_S$
Output Short Circuit Duration
(For One Amplifier) . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range (Q) . . . . . −65°C to +150°C
Storage Temperature Range (N, R) . . . . . −65°C to +125°C
Operating Temperature Range
AD746J . . . . . 0 to +70°C
AD746A/B . . . . . −40°C to +85°C
AD746S . . . . . −55°C to +125°C
Lead Temperature Range
(Soldering 60 seconds) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Pin Plastic Package: θ_{JA} = 100°C/Watt, θ_{JC} = 50°C/Watt
8-Pin Cerdip Package: θ_{JA} = 110°C/Watt, θ_{JC} = 30°C/Watt
8-Pin Small Outline Package: θ_{JA} = 160°C/Watt, θ_{JC} = 42°C/Watt

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



AD746—Typical Characteristics

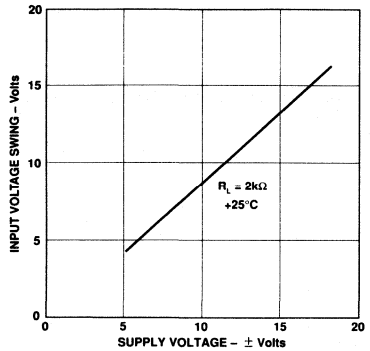


Figure 1. Input Voltage Swing vs. Supply Voltage

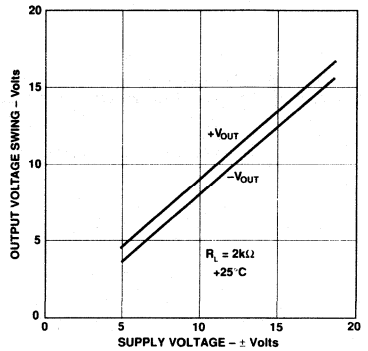


Figure 2. Output Voltage Swing vs. Supply Voltage

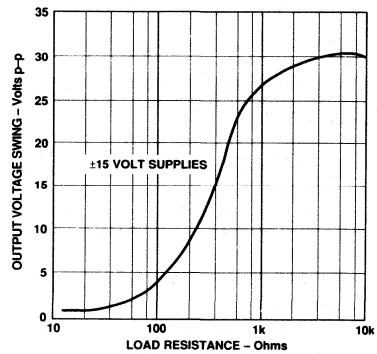


Figure 3. Output Voltage Swing vs. Load Resistance

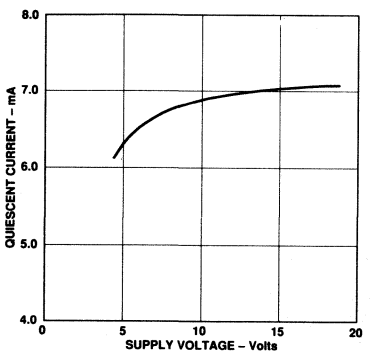


Figure 4. Quiescent Current vs. Supply Voltage

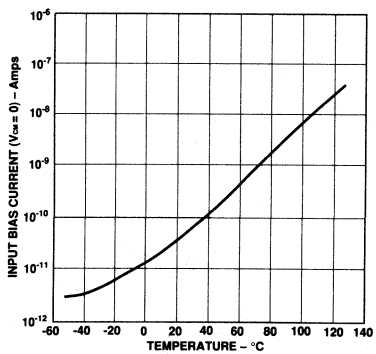


Figure 5. Input Bias Current vs. Temperature

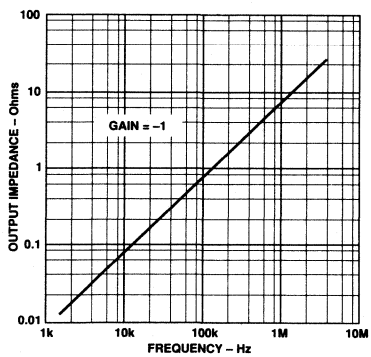


Figure 6. Output Impedance vs. Frequency

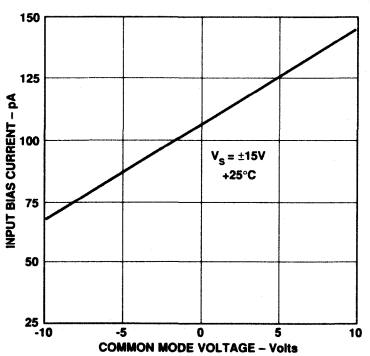


Figure 7. Input Bias Current vs. Common Mode Voltage

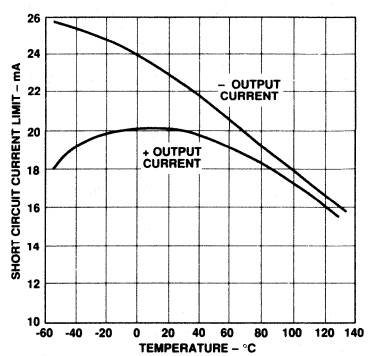


Figure 8. Short Circuit Current Limit vs. Temperature

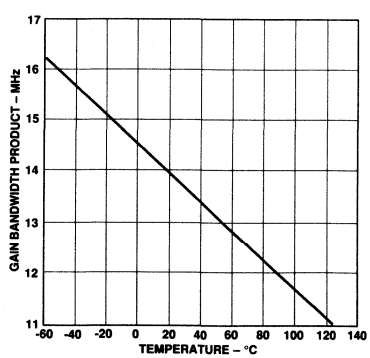


Figure 9. Gain Bandwidth Product vs. Temperature

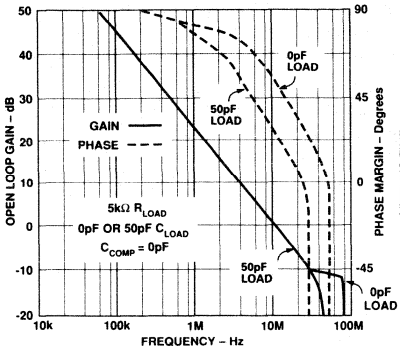


Figure 10. Open Loop Gain and Phase Margin vs. Frequency

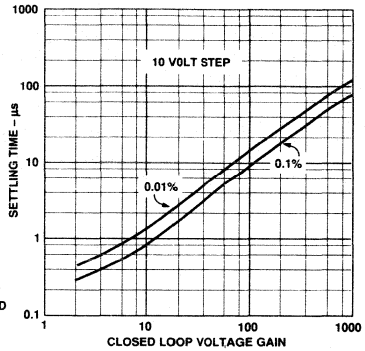


Figure 11. Settling Time vs. Closed Loop Voltage Gain

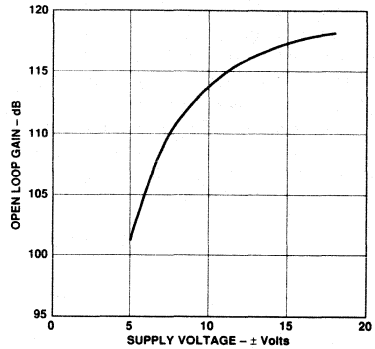


Figure 12. Open Loop Gain vs. Supply Voltage

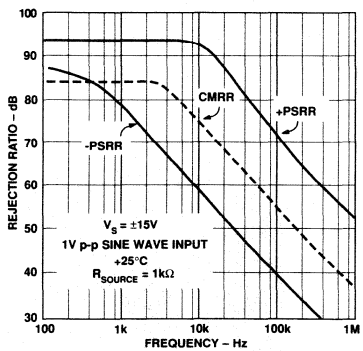


Figure 13. Common-Mode and Power Supply Rejection vs. Frequency

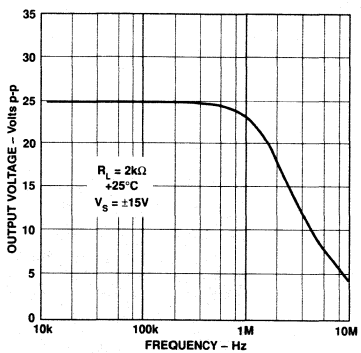


Figure 14. Large Signal Frequency Response

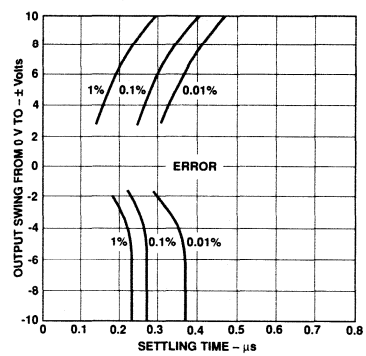


Figure 15. Output Swing and Error vs. Settling Time

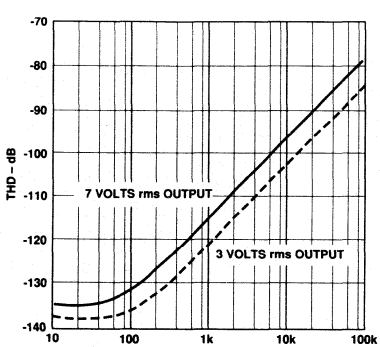


Figure 16. Total Harmonic Distortion vs. Frequency Using Circuit of Figure 19

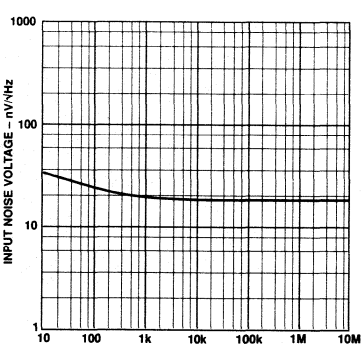


Figure 17. Input Noise Voltage Spectral Density

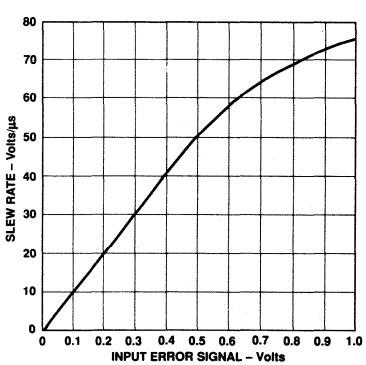


Figure 18. Slew Rate vs. Input Error Signal

Power Supply Bypassing

The power supply connections to the AD746 must maintain a low impedance to ground over a bandwidth of 13 MHz or more. This is especially important when driving a significant resistive or capacitive load, since all current delivered to the load comes from the power supplies. Multiple high quality bypass capacitors are recommended for each power supply line in any critical application. A 0.1 μF ceramic and a 1 μF tantalum capacitor as shown in Figure 20 placed as close as possible to the amplifier (with short lead lengths to power supply common) will assure adequate high frequency bypassing, in most applications. A minimum bypass capacitance of 0.1 μF should be used for any application.

If only one of the two amplifiers inside the AD746 is to be utilized, the unused amplifier should be connected as shown in Figure 21a. Note that the noninverting input should be grounded and that R_L and C_L are not required.

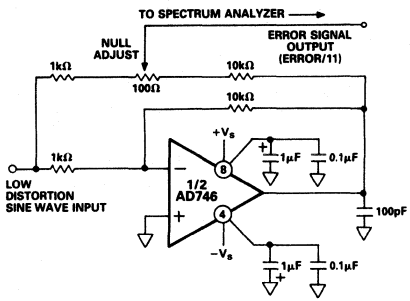


Figure 19. THD Test Circuit

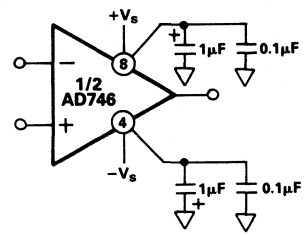


Figure 20. Power Supply Bypassing

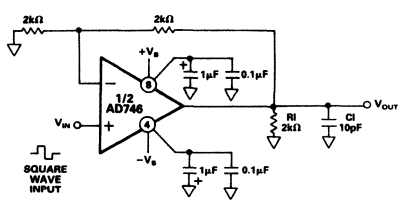


Figure 21a. Gain of 2 Follower

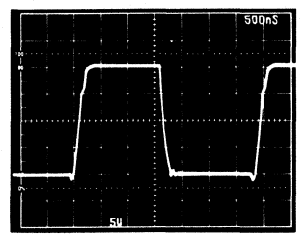


Figure 21b. Gain of 2 Follower Large Signal Pulse Response

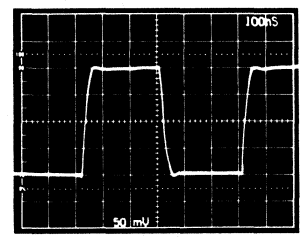


Figure 21c. Gain of 2 Follower Small Signal Pulse Response

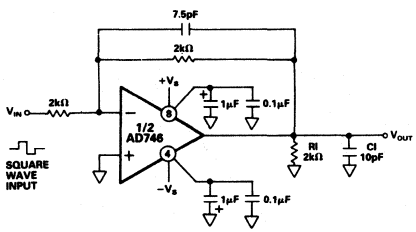


Figure 22a. Unity Gain Inverter

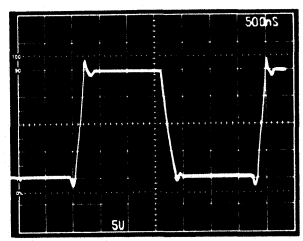


Figure 22b. Unity Gain Inverter Large Signal Pulse Response

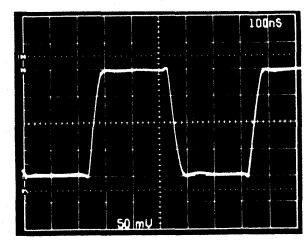


Figure 22c. Unity Gain Inverter Small Signal Pulse Response

A HIGH SPEED 3 OP AMP INSTRUMENTATION AMPLIFIER CIRCUIT

The instrumentation amplifier circuit shown in Figure 23 can provide a range of gains from 2 up to 1000 and higher. The circuit bandwidth is 2.5 MHz at a gain of 2 and 750 kHz at a gain of 10; settling time for the entire circuit is less than 2 μs to within 0.01% for a 10 volt step, (G = 10).

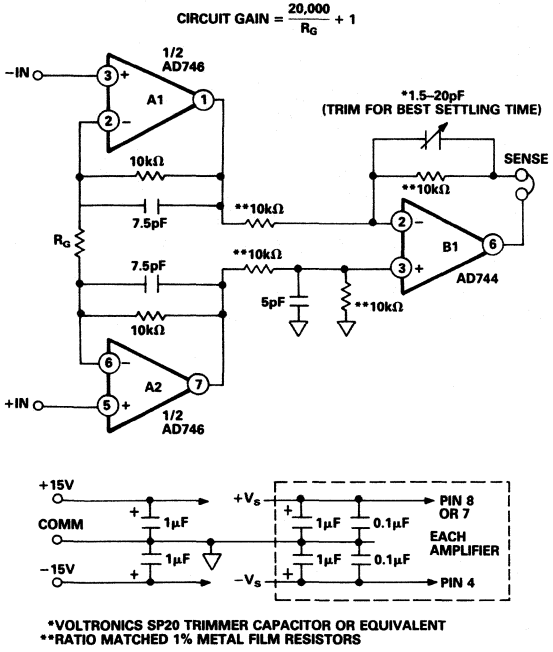


Figure 23. A High Performance, 3 Op Amp, Instrumentation Amplifier Circuit

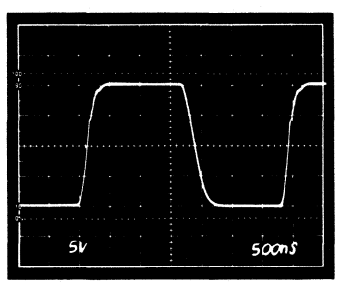


Figure 24. Pulse Response of the 3 Op Amp Instrumentation Amplifier. Gain = 10, Horizontal Scale: 0.5 μs/Div, Vertical Scale: 5 V/Div.

Gain	R_G	Bandwidth	T_{SETTLE} (0.01%)
2	20 kΩ	2.5 MHz	1.0 μs
10	4.04 kΩ	1 MHz	2.0 μs
100	404 Ω	290 kHz	5.0 μs

Table I. Performance Summary for the 3 Op Amp Instrumentation Amplifier Circuit

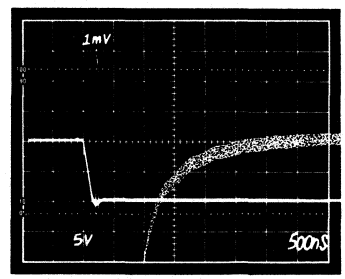


Figure 25. Settling Time of the 3 Op Amp Instrumentation Amplifier. Gain = 10, Horizontal Scale: 0.5 μs/Div, Vertical Scale: 5 V/Div. Error Signal Scale: 0.01%/Div.

THD Performance Considerations

The AD746 was carefully optimized to offer excellent performance in terms of total harmonic distortion (THD) in signal processing applications. The THD level when operating the AD746 in inverting gain applications will show a gradual rise from the distortion floor of 20 dB/decade (see Figure 28). In noninverting applications, care should be taken to balance the source impedances at both the inverting and noninverting inputs, to avoid distortion caused by the modulation of input capacitance inherent in all BiFET op amps.

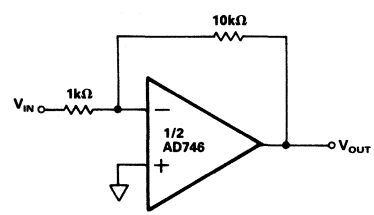


Figure 26. THD Measurement, Inverter Circuit

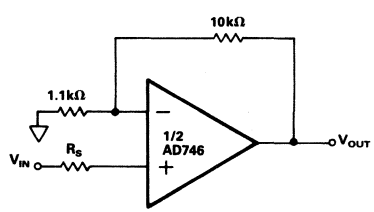


Figure 27. THD Measurement, Follower Circuit

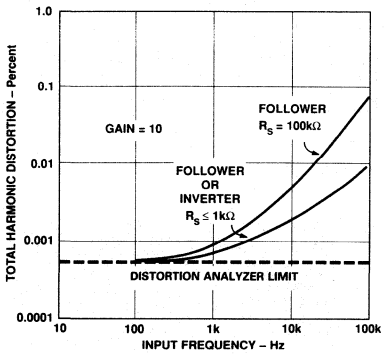


Figure 28. THD vs. Frequency Using Standard Distortion Analyzer

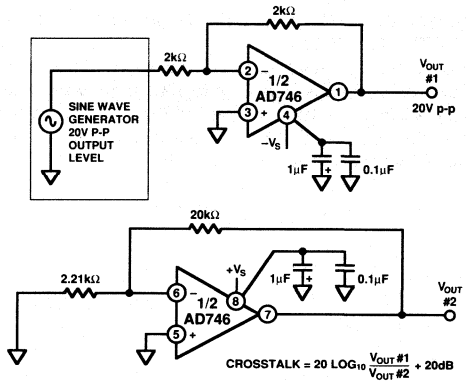


Figure 29. Crosstalk Test Circuit

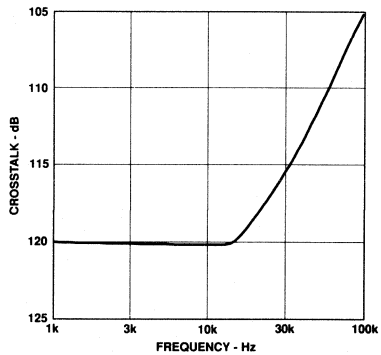


Figure 30. Crosstalk vs. Frequency

ANALOG DEVICES

Low Power, Low Noise Precision FET Op Amp

AD795

FEATURES

Low Power Replacement for Burr-Brown OPA-111, OPA-121 Op Amp and TI TLC 2201
Low Noise
- **2.5 μV p–p max, 0.1 Hz to 10 Hz**
- **10 nV/√Hz max at 10 kHz**
- **0.6 fA/√Hz at 1 kHz**

High DC Accuracy
- **250 μV max Offset Voltage**
- **1 μV/°C max Drift**
- **1 pA max Input Bias Current**
- **114 dB Open-Loop Gain**

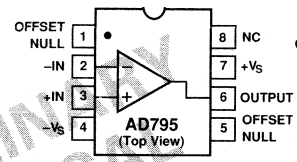
Available in Plastic Mini-DIP, 8-Pin Header and Surface Mount (SOIC) Packages
Dual Version AD796 also Available

APPLICATIONS

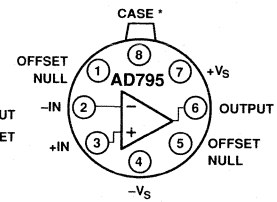
Low Noise Photodiode Preamps
CT Scanners
Precision I-to-V Converters

CONNECTION DIAGRAMS

8-Pin Plastic Mini-DIP (N) Package

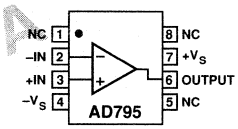


TO-99 (H) Package



* NOTE: CASE CONNECTED TO PIN 8.

8-Pin SOIC (R) Package



PRELIMINARY TECHNICAL DATA

PRODUCT DESCRIPTION

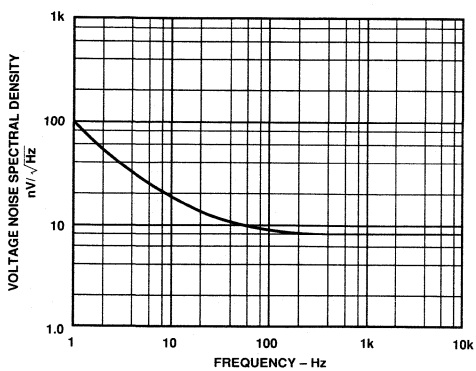
The AD795 is a low noise, precision, FET input operational amplifier. It offers both the low voltage noise and low offset drift of a bipolar input op amp and the very low bias current of a FET-input device. The 10^{14} Ω common-mode impedance insures that input bias current is essentially independent of common-mode voltage variations.

The AD795 has both excellent dc performance and a guaranteed and tested maximum input voltage noise. It features 1 pA maximum input bias current and 250 μV maximum offset voltage, along with low supply current of 1.5 mA max.

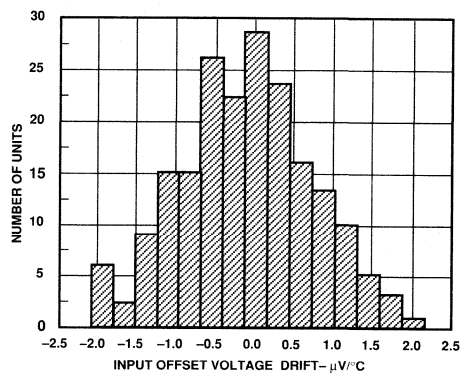
Furthermore, the AD795 features a guaranteed low input noise of 2.5 μV p–p (0.1 Hz to 10 Hz) and a 10 nV/√Hz max noise level at 10 kHz. The AD795 has a fully specified and tested input offset voltage drift of only 1 μV/°C max which is trimmed at the wafer level to keep device cost low.

The AD795 is useful for many high input impedance, low noise applications. It is available in five performance grades. The AD795J and AD795K are rated over the commercial temperature range of 0°C to +70°C. The AD795A and AD795B are rated over the industrial temperature of −40°C to +85°C. The AD795SQ/883B is rated over the military temperature range of −55°C to +125°C and is processed to MIL-STD-883B.

The AD795 is available in 8-pin plastic mini-DIP, 8-pin header, and 8-pin surface mount (SOIC) packages.



AD795 Voltage Noise Spectral Density



Typical Distribution of Average Input Offset

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD795—SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Parameter	Conditions	AD795J/A Min	AD795J/A Typ	AD795J/A Max	AD795K/B Min	AD795K/B Typ	AD795K/B Max	AD795S Min	AD795S Typ	AD795S Max	Units
INPUT OFFSET VOLTAGE[1]											
Initial Offset			100	500		50	250		100	500	μV
Offset	T_{MIN}–T_{MAX}		300	1000		100	400		500	1500	μV
vs. Temperature			3	10/5		2	3/1		4	10	μV/°C
vs. Supply		90	110		94	110		90	110		dB
vs. Supply (PSRR)	T_{MIN}–T_{MAX}		100		90	100		86	95		dB
INPUT BIAS CURRENT[2]											
Either Input	V_{CM} = 0 V		1	2		1	1		1	4	pA
Either Input @ T_{MAX} =	V_{CM} = 0 V		23/64			23/64			1000		pA
Either Input	V_{CM} = +10 V		1			1			1		pA
Offset Current	V_{CM} = 0 V		0.1	1.0		0.1	0.5		0.1	1.0	pA
Offset Current @ T_{MAX} =	V_{CM} = 0 V		2/6			2/6			100		pA
INPUT VOLTAGE NOISE	0.1 Hz to 10 Hz		1.0	3.3		1.0	2.5		1.0	3.3	μV p–p
	f = 10 Hz		20	50		20	40		20	50	nV/√Hz
	f = 100 Hz		10	30		10	20		10	30	nV/√Hz
	f = 1 kHz		9	15		9	10		7	15	nV/√Hz
	f = 10 kHz		8	10		8	10		8	10	nV/√Hz
INPUT CURRENT NOISE	f = 0.1 Hz to 10 Hz		13			13			13		fA p–p
	f = 1 kHz		0.6			0.6			0.6		fA/√Hz
FREQUENCY RESPONSE											
Unity Gain, Small Signal	G = −1		1.6			1.6			1.6		MHz
Full Power Response	V_O = 20 V p–p										
	R_{LOAD} = 2 kΩ		16			16			16		kHz
Slew Rate, Unity Gain	V_{OUT} = 20 V p–p										
	R_{LOAD} = 2 kΩ		1			1			1		V/μs
SETTLING TIME[3]											
To 0.1%			6			6			6		μs
To 0.01%			8			8			8		μs
Overload Recovery[4]	50% Overdrive		5			5			5		μs
Total Harmonic Distortion	f = 1 kHz, R1 ≥ 2 kΩ, V_O = 3 V rms		0.0006			0.0006			0.0006		%
INPUT IMPEDANCE											
Differential	V_{DIFF} = ±1 V		10^{12}‖1			10^{12}‖1			10^{12}‖1		Ω‖pF
Common Mode			10^{14}‖2.2			10^{14}‖2.2			10^{14}‖2.2		Ω‖pF
INPUT VOLTAGE RANGE											
Differential[5]			±20			±20			±20		V
Common-Mode Voltage		±10	±11		±10	±11		±10	±11		V
Over Max Operating Range		±10			±10			±10			V
Common-Mode Rejection Ratio	V_{CM} = ±10 V	90	110		94	110		90	110		dB
	T_{MIN} to T_{MAX}		100		90	100		86	100		dB
OPEN-LOOP GAIN	V_O = ±10 V										
	R_{LOAD} ≥ 10 kΩ		120			120			120		dB
	R_{LOAD} ≥ 2 kΩ	100	108		100	108		100	108		dB
	T_{MIN}–T_{MAX}				114			110			dB
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD} ≥ 2 kΩ	±10	±11		±10	±11		±10	±11		V
	T_{MIN}–T_{MAX}	±10			±10			±10			V
Current	V_{OUT} = ±10 V	±5	±10		±5	±10		±5	±10		mA
	Short Circuit		±15			±15			±15		mA
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		±5		±18	±5		±18	±5		±18	V
Quiescent Current			1.2	1.5		1.2	1.5		1.2	1.5	mA

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

NOTES
[1]Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[2]Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperature, the current doubles every 10°C.
[3]Gain = −1, R1 = 2 kΩ.
[4]Defined as the time required for the amplifier's output to return to normal operation after removal of a 50% overload from the amplifier input.
[5]Defined as the maximum continuous voltage between the inputs such that neither input exceeds ±10 V from ground.
All min and max specifications are guaranteed.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2] (@ T_A = +25°C)
8-Pin Header Package . . . . . 500 mW
8-Pin Mini-DIP Package . . . . . 750 mW
Input Voltage . . . . . $\pm V_S$
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range (H) . . . . . −65°C to +150°C
Storage Temperature Range (N, R) . . . . . −65°C to +125°C
Operating Temperature Range
AD795J/K . . . . . 0°C to +70°C
AD795A/B . . . . . −40°C to +85°C

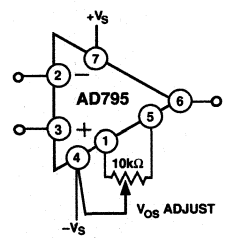
NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Pin Plastic Mini-DIP Package: θ_{JA} = 100°C/Watt
8-Pin Header Package: θ_{JA} = 200°C/Watt
8-Pin Small Outline Package: θ_{JA} = 155°C/Watt

PRELIMINARY TECHNICAL DATA

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD795JN	0°C to +70°C	N-8
AD795KN	0°C to +70°C	N-8
AD795JR	0°C to +70°C	R-8
AD795AH	−40°C to +85°C	H-08A
AD795BH	−40°C to +85°C	H-08A
AD795SH-883B	−55°C to +125°C	H-08A

*N = Plastic mini-DIP; H-08A = Metal can; R = SOIC package. For outline information see Package Information section.



Offset Null Configuration

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AD795—Typical Characteristics

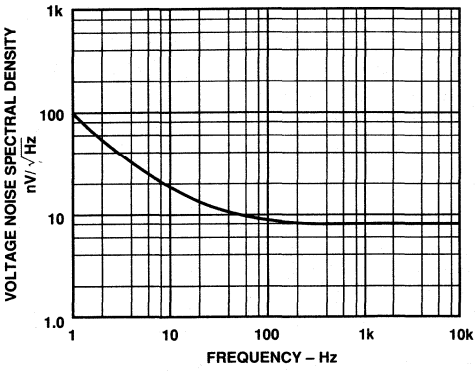

Figure 1. Voltage Noise Spectral Density

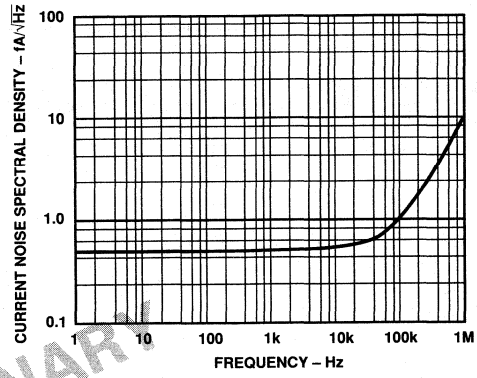

Figure 2. Current Noise Spectral Density

PRELIMINARY TECHNICAL DATA

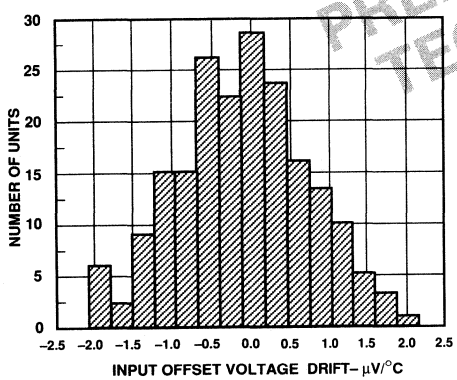

Figure 3. Typical Distribution of Average Input Offset Voltage Drift

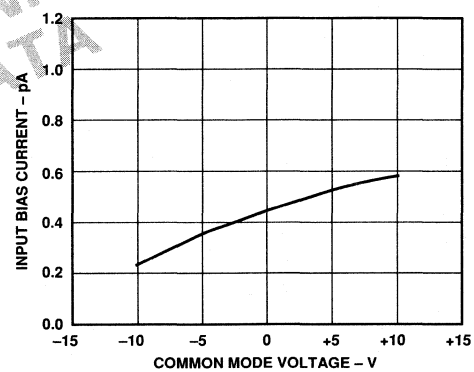

Figure 4. Input Bias Current vs. Common-Mode Voltage

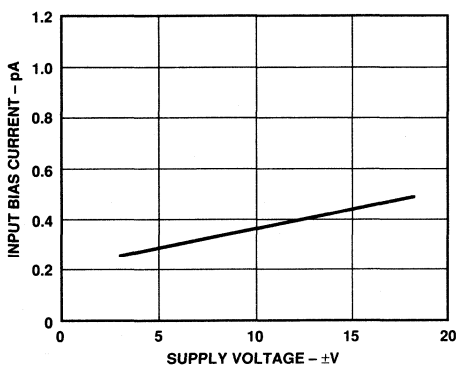

Figure 5. Input Bias Current vs. Supply Voltage

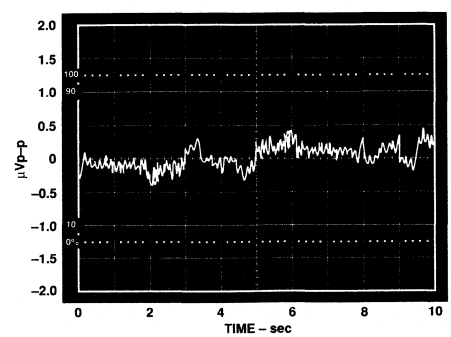

Figure 6. 0.1 Hz to 10 Hz Noise Voltage

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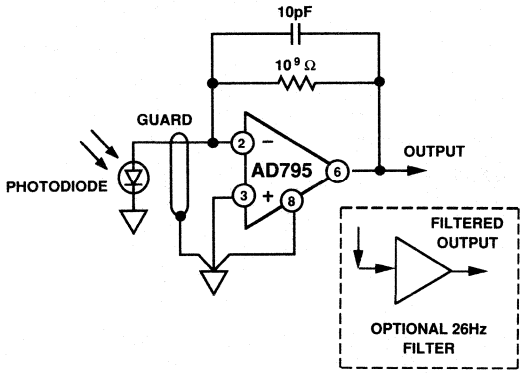

Figure 7. The AD795 Used as a Sensitive Preamplifier

Preamplifier Applications

The low input current and offset voltage levels of the AD795 together with its low voltage noise make this amplifier an excellent choice for preamplifiers used in sensitive photodiode applications. In a typical preamp circuit, shown in Figure 7, the output of the amplifier is equal to:

$$V_{OUT} = I_D\,(Rf) = Rp\,(P)\,Rf$$

where:

I_D = photodiode signal current (Amps)

Rp = photodiode sensitivity (Amp/Watt)

Rf = the value of the feedback resistor, in ohms.

P = light power incident to photodiode surface, in watts.

An equivalent model for a photodiode and its dc error sources is shown in Figure 8. The amplifier's input current, I_B, will contribute an output voltage error which will be proportional to the value of the feedback resistor. The offset voltage error, V_{OS}, will cause a "dark" current error due to the photodiode's finite shunt resistance, Rd. The resulting output voltage error, V_E, is equal to:

$$V_E = (1 + Rf/Rd)\,V_{OS} + Rf\,I_B$$

A shunt resistance on the order of 10^9 ohms is typical for a small photodiode. Resistance Rd is a junction resistance which will typically drop by a factor of two for every 10°C rise in temperature. In the AD795, both the offset voltage and drift are low, this helps minimize these errors.

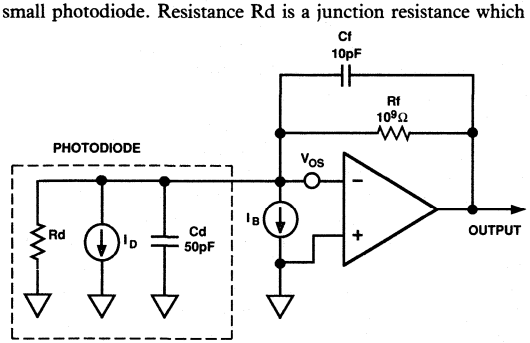

Figure 8. A Photodiode Model Showing DC Error Sources

Minimizing Noise Contributions

The noise level limits the resolution obtainable from any preamplifier. The total output voltage noise divided by the feedback resistance of the op amp defines the minimum detectable signal current. The minimum detectable current divided by the photodiode sensitivity is the minimum detectable light power.

Sources of noise in a typical preamp are shown in Figure 9. The total noise contribution is defined as:

$$\overline{V_{OUT}} = \sqrt{(\overline{i_s^2} + \overline{i_f^2} + \overline{i_r^2})\left(\frac{Rf}{1 + s\,(Cf)\,Rf}\right)^2 + (\overline{en^2})\left(1 + \frac{Rf}{Rd}\left(\frac{1 + s\,(Cd)\,Rd}{1 + s\,(Cf)\,Rf}\right)\right)^2}$$

Figure 10, a spectral density versus frequency plot of each source's noise contribution, shows that the bandwidth of the amplifier's input voltage noise contribution is much greater than its signal bandwidth. In addition, capacitance at the summing junction results in a "peaking" of noise gain in this configuration. This effect can be substantial when large photodiodes with large shunt capacitances are used. Capacitor Cf sets the signal bandwidth and also limits the peak in the noise gain. Each source's rms or root-sum-square contribution to noise is obtained by integrating the sum of the squares of all the noise sources and then by obtaining the square root of this sum. Minimizing the total area under these curves will optimize the preamplifier's overall noise performance.

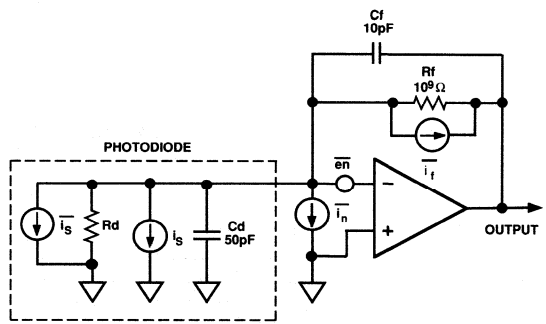

Figure 9. Noise Contributions of Various Sources

An output filter with a passband close to that of the signal can greatly improve the preamplifier's signal to noise ratio. The photodiode preamplifier shown in Figure 9—without a bandpass filter—has a total output noise of 50 μV rms. Using a 26 Hz single pole output filter, the total output noise drops to 23 μV rms, a factor of 2 improvement with no loss in signal bandwidth.

Using a "T" Network

A "T" network, shown in Figure 11, can be used to boost the effective transimpedance of an I to V converter, for a given feedback resistor value. Unfortunately, amplifier noise and offset voltage contributions are also amplified by the "T" network gain. A low noise, low offset voltage amplifier, such as the AD795, is needed for this type of application.

PRELIMINARY TECHNICAL DATA

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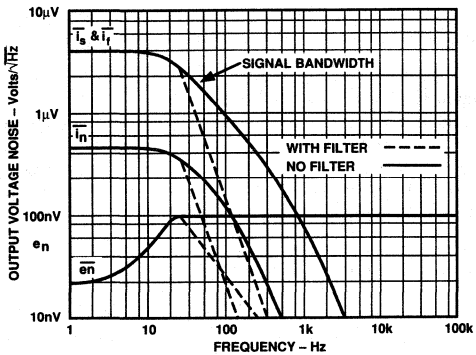

Figure 10. Voltage Noise Spectral Density of the Circuit of Figure 9 with and without an Output Filter

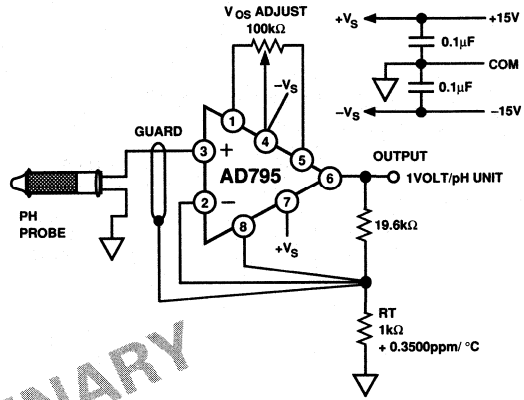

Figure 12. A pH Probe Amplifier

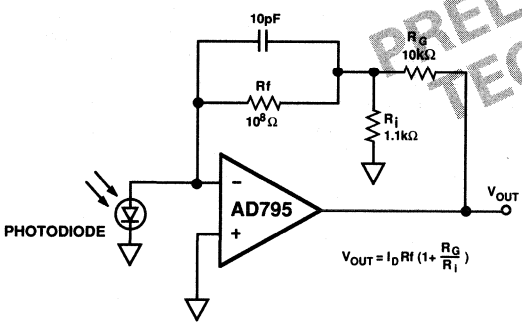

Figure 11. A Photodiode Preamp Employing a "T" Network for Added Gain

A pH Probe Buffer Amplifier

A typical pH probe requires a buffer amplifier to isolate its 10^6 to 10^9 Ω source resistance from external circuitry. Just such an amplifier is shown in Figure 12. The low input current of the AD795 allows the voltage error produced by the bias current and electrode resistance to be minimal. The use of guarding, shielding, high insulation resistance standoffs, and other such standard methods used to minimize leakage are all needed to maintain the accuracy of this circuit.

The slope of the pH probe transfer function, 50 mV per pH unit at room temperature, has a +3300 ppm/°C temperature coefficient. The buffer of Figure 12 provides an output voltage equal to 1 volt/pH unit. Temperature compensation is provided by resistor RT which is a special temperature compensation resistor, part number Q81, 1 kΩ, 1%, +3500 ppm/°C, available from Tel Labs Inc.

PRELIMINARY TECHNICAL DATA

Circuit Board Notes

The AD795 is designed for through hole mount into PC boards. Maintaining picoampere level resolution in that environment requires a lot of care. Since both the printed circuit board and the amplifier's package have a finite resistance, the voltage difference between the amplifier's input pin and other pins (or traces on the PC board) will cause parasitic currents to flow into (or out of) the signal path. These currents can easily exceed the 1 pA input current level of the AD795 unless special precautions are taken. Two successful methods for minimizing leakage are: guarding the AD795's input lines and maintaining adequate insulation resistance.

Guarding the input lines by completely surrounding them with a metal conductor biased near the input lines' potential has two major benefits. First, parasitic leakage from the signal line is reduced, since the voltage between the input line and the guard is very low. Second, stray capacitance at the input terminal is minimized which in turn increases signal bandwidth. In the header or can package, the case of the AD795 is connected to Pin 8 so that it may be tied to the input potential (when operating as a follower) or tied to ground (when operating as an inverter). The AD795's positive input (Pin 3) is located next to the negative supply voltage pin (Pin 4). The negative input (Pin 2) is next to the balance adjust pin (Pin 1) which is biased at a potential close to that of the negative supply voltage. Note that any guard traces should be placed on *both* sides of the board. In addition, the input trace should be guarded along both of its edges, along its entire length.

Contaminants such as solder flux, on the board's surface and on the amplifier's package, can greatly reduce the insulation resistance and also increase the sensitivity to atmospheric humidity. Both the package and the board must be kept clean and dry. An effective cleaning procedure is to: first, swab the surface with high grade isopropyl alcohol, then rinse it with deionized water, and finally, bake it at 80°C for 1 hour. Note that if either polystyrene or polypropylene capacitors are used on the printed circuit board that a baking temperature of 70°C is safer, since both of these plastic compounds begin to melt at approximately +85°C.

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Dual Low Power, Low Cost, Precision FET Op Amp

AD796

FEATURES

Low Noise
- 2.5 μV p–p max, 0.1 Hz to 10 Hz
- 10 nV/√Hz max at 10 kHz
- 14 fA p–p Current Noise 0.1 Hz to 10 Hz

High DC Accuracy
- 300 μV max Offset Voltage
- 3 μV/°C max Drift
- 2 pA max Input Bias Current
- 114 dB Open Loop Gain
- Low Power: 1.5 mA max per Amplifier

Good AC Performance
- 1 V/μs Slew Rate
- 2 MHz Unity Gain Bandwidth

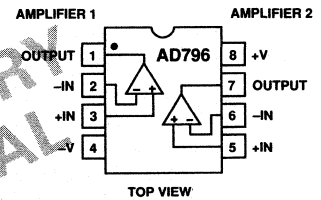
Available in 8-Pin Plastic Mini-DIP, Cerdip and Surface Mount (SOIC) Packages

APPLICATIONS

Low Noise Photodiode Preamps
CT Scanners
Precision I/V Converters

CONNECTION DIAGRAM

Plastic Mini-DIP (N) Package, Cerdip (Q) Package, and SOIC (R) Package



PRELIMINARY TECHNICAL DATA

PRODUCT DESCRIPTION

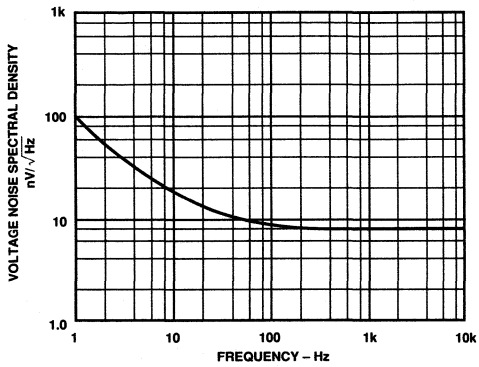
The AD796 is a low noise, precision, FET input, dual monolithic operational amplifier. Each amplifier offers both the low voltage noise and low offset drift of a bipolar input op amp and the very low bias current of a FET input device. The 10^{14} Ω common-mode impedance insures that input bias current is essentially independent of common-mode voltage variations.

The AD796 has both excellent dc performance and a guaranteed and tested maximum input voltage noise. Each amplifier features 2 pA maximum input bias current and 300 μV maximum offset voltage (AD796B) along with 1.5 mA max power supply current.

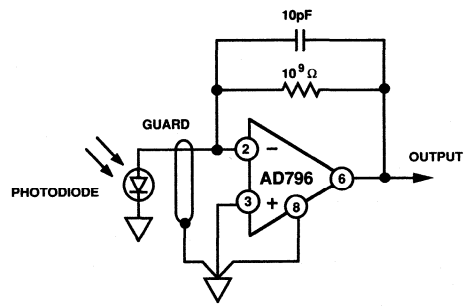
The AD796 features a guaranteed low input noise of 2.5 μV p–p (0.1 Hz to 10 Hz) and a 10 nV/√Hz max noise level at 10 kHz. The AD796 has a fully specified and tested input offset voltage drift of only 3 μV/°C max which is trimmed at the wafer level to keep device cost low.

The AD796 is the ideal choice for many high input impedance, low noise applications. It is available in three performance grades. The AD796A and AD796B are rated over the industrial temperature of −40°C to +85°C. The AD796S is rated over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B.

The AD796 is available in 8-pin plastic mini-DIP, cerdip, and surface mount (SOIC).



Voltage Noise Spectral Density



The AD796 Used as a Sensitive Photodiode Preamplifier

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD796—SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Parameter	Conditions	AD796A Min	AD796A Typ	AD796A Max	AD796B Min	AD796B Typ	AD796B Max	AD796S Min	AD796S Typ	AD796S Max	Units
INPUT OFFSET VOLTAGE[1]											
Initial Offset			100	500		50	300		100	500	μV
Offset	T_{MIN}–T_{MAX}		300	1000		100	400		500	1500	μV
vs. Temperature			3	12		2	3		4	10	μV/°C
vs. Supply		90	110		94	110		90	110		dB
vs. Supply (PSRR)	T_{MIN}–T_{MAX}		100		90	100		86	95		dB
INPUT BIAS CURRENT[2]											
Either Input	V_{CM} = 0 V		1.5	2.5		1.5	2		2	5	pA
Either Input @ T_{MAX} = 70°C	V_{CM} = 0 V		34/96			34/96			2050		pA
Either Input	V_{CM} = +10 V		1.5			1.5			1.5		pA
Offset Current	V_{CM} = 0 V		0.1	1.0		0.1	0.5		0.1	1.0	pA
Offset Current @ T_{MAX} = 70°C	V_{CM} = 0 V		2/6			2/6			100		pA
INPUT VOLTAGE NOISE	0.1 Hz to 10 Hz		1.0	3.3		1.0	2.5		1.0	3.3	μV p–p
	f = 10 Hz		20	50		20	40		20	50	nV/√Hz
	f = 100 Hz		10	30		10	20		10	30	nV/√Hz
	f = 1 kHz		7	15		7	10		7	15	nV/√Hz
	f = 10 kHz		8	10		8	10		8	10	nV/√Hz
INPUT CURRENT NOISE	f = 0.1 Hz to 10 Hz		14			14			18		fA p–p
	f = 0.1 kHz to 20 kHz		0.7			0.7			0.8		fA/√Hz
FREQUENCY RESPONSE											
Unity Gain, Small Signal	G = −1		2			2			2		MHz
Full Power Response	V_O = 20 V p–p										
	R_{LOAD} = 2 kΩ	12.8	16		12.8	16		12.8	16		kHz
Slew Rate, Unity Gain	V_{OUT} = 20 V p–p										
	R_{LOAD} = 2 kΩ		1			1			1		V/μs
SETTLING TIME[3]											
To 0.1%			11			11			11		μs
To 0.01%			12			12			12		μs
Overload Recovery[4]	50% Overdrive		5			5			5		μs
Total Harmonic	f = 1 kHz										
INPUT IMPEDANCE											
Differential	V_{DIFF} = ±1 V		10^{12}‖1			10^{12}‖1			10^{12}‖1		Ω‖pF
Common Mode			10^{14}‖2.2			10^{14}‖2.2			10^{14}‖2.2		Ω‖pF
INPUT VOLTAGE RANGE											
Differential[5]			±20			±20			±20		V
Common-Mode Voltage		±10	±11		±10	±11		±10	±11		V
Over Max Operating Range		±10			±10			±10			V
Common-Mode Rejection Ratio	V_{CM} = ±10 V	90	110		94	110		90	110		dB
	T_{MIN} to T_{MAX}		100		90	100		86	100		dB
OPEN-LOOP GAIN	V_O = ±10 V										
	R_{LOAD} ≥ 2 kΩ	100	110		100	110		114	130		dB
	T_{MIN}–T_{MAX}				100			110			dB
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD} ≥ 2 kΩ	±10	±11		±10	±11		±10	±11		V
	T_{MIN}–T_{MAX}										V
Current	V_{OUT} = ±10 V	±5	±10		±5	±10		±5	±10		mA
	Short Circuit		±15			±15			±15		mA
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		±5		±18	±5		±18	±5		±18	V
Quiescent Current			2.5	3		2.5	3		2.5	3	mA

PRELIMINARY TECHNICAL DATA

NOTES

[1]Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperature, the current doubles every 10°C.

[3]Gain = −1, R_{LOAD} = 2 kΩ.

[4]Defined as the time required for the amplifier's output to return to normal operation after removal of a 50% overload from the amplifier input.

[5]Defined as the maximum continuous voltage between the inputs such that neither input exceeds ±10 V from ground.

All min and max specifications are guaranteed.

Specifications subject to change without notice.

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ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2] (@ T_A = +25°C)
8-Pin Header Package . . . . . 500 mW
8-Pin Mini-DIP Package . . . . . 750 mW
8-Pin SOIC Package . . . . . 650 mW
Input Voltage . . . . . $\pm V_S$
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range (Q) . . . . . −65°C to +150°C
Storage Temperature Range (N) . . . . . −65°C to +125°C
Storage Temperature Range (R) . . . . . −65°C to +125°C
Operating Temperature Range
AD796A/B . . . . . −40°C to +85°C
AD796S . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 secs) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Pin Plastic Mini-DIP Package: θ_{JA} = 100°C/Watt
8-Pin Small Outline Package: θ_{JA} = 155°C/Watt
8-Pin Cerdip Package: θ_{JA} = 110°C/Watt

2

PRELIMINARY TECHNICAL DATA

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD796AN	−40°C to +85°C	N-8
AD796BN	−40°C to +85°C	N-8
AD796AR	−40°C to +85°C	R-8
AD796SQ-883B	−55°C to +125°C	Q-08

*N = Plastic mini-DIP, Q-8 = Cerdip, R = SOIC package. See outline information see Package Information section.

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Ultralow Distortion, Ultralow Noise Op Amp

AD797

FEATURES

Low Noise
- 0.9 nV/$\sqrt{Hz}$ typ (1.2 nV/$\sqrt{Hz}$ max) Input Voltage Noise (@1 kHz)
- 50 nV p–p Input Voltage Noise, 0.1 Hz to 10 Hz

Low Distortion
- −110 dB Total Harmonic Distortion (@ 20 kHz)

Excellent AC Characteristics
- 110 MHz Gain Bandwidth (G = 1000)
- 6 MHz Bandwidth (G = 10)
- 280 kHz Full Power Bandwidth
- 18 V/μs Slew Rate

Good DC Precision
- 80 μV max Input Offset Voltage (40 μV "B" Grade)
- 1.0 μV/°C V_{OS} Drift (0.8 μV/°C "B" Grade)

Flexible Operation
- Specified for ±5 V and ±15 V Power Supplies
- Low Power of 7.5 mA typ

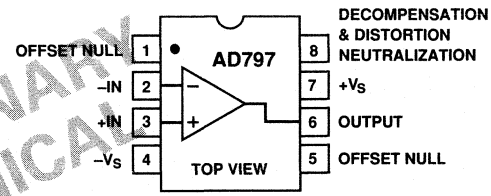
High Output Drive Current of 30 mA min

APPLICATIONS

Professional Audio Preamplifiers
IR, CCD, and Sonar Imaging Systems
Spectrum Analyzers
Ultrasound Preamplifiers
Seismic Detectors
ΣΔ ADC/DAC Buffers

CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP (N), Cerdip (Q) and SOIC (R) Packages



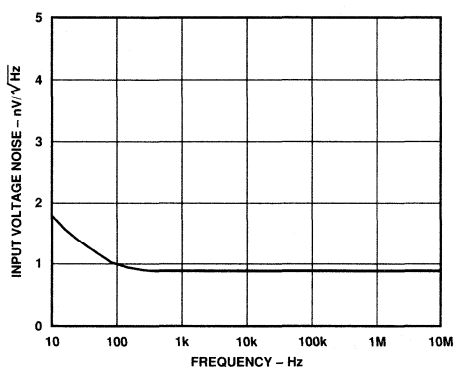
PRELIMINARY TECHNICAL DATA

PRODUCT DESCRIPTION

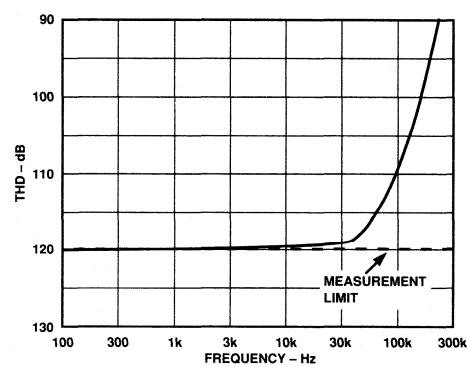
The AD797 is a very low noise, low distortion amplifier ideal for use as a preamplifier. The low noise of 0.9 nV/$\sqrt{Hz}$ and low total harmonic distortion of −110 dB at audio bandwidths gives the AD797 the wide dynamic range necessary for preamps in microphones and mixing consoles. Furthermore, the excellent frequency response of the AD797 of 18 V/μs slew rate and 80 MHz gain bandwidth makes it highly suitable for ultrasound applications.

The AD797 is also useful in IR and sonar imaging applications where the widest dynamic range is necessary along with the operating temperature range of the AD797SQ/883B of −55°C to +125°C.

The low distortion and unity gain stability of the AD797 make it ideal for buffering the inputs to ΣΔ ADCs or the outputs of high resolution DACs especially in critical applications such as seismic detection and spectrum analyzers. Key features such as a 30 mA output current drive and the fully specified power supply voltage range of ±5 volts to ±15 volts help to make the AD797 a good general purpose amplifier.



AD797 Voltage Noise



AD797 Total Harmonic Distortion

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AD797—SPECIFICATIONS (@T_A = +25°C and V_S = ±15 V dc, unless otherwise noted)

Model	Conditions	V_S	AD797A/S Min	AD797A/S Typ	AD797A/S Max	AD797B Min	AD797B Typ	AD797B Max	Units
INPUT OFFSET VOLTAGE		±5 V, ±15 V		25	80		10	40	μV
	T_{MIN} to T_{MAX}			50	125/180		30	80	μV
Offset Voltage Drift		±5 V, ±15 V		0.2	1		0.2	0.8	μV/°C
INPUT BIAS CURRENT		±5 V, ±15 V		0.8	2.0		0.5	0.9	μA
	T_{MIN} to T_{MAX}			2.0	4.0		1.0	2.0	μA
INPUT OFFSET CURRENT		±5 V, ±15 V		100	300		80	150	nA
	T_{MIN} to T_{MAX}			120	500/750		120	250	nA
OPEN-LOOP GAIN	V_{OUT} = ±10 V	±15 V							
	R_{LOAD} = 2 kΩ		4	20		5	20		V/μV
	T_{MIN}–T_{MAX}		2.5/1.5	6		4	10		V/μV
	R_{LOAD} = 600 Ω		2	15		3	15		V/μV
	T_{MIN} to T_{MAX}		1	5		2	7		V/μV
	@ 20 kHz			5500			5500		V/V
DYNAMIC PERFORMANCE									
Gain Bandwidth Product	G = 1000	±15 V		110			110		MHz
	G = 1000[1]	±15 V		450			450		MHz
−3 dB Bandwidth	G = 10	±15 V		6			6		MHz
Full Power Bandwidth[2]	V_O = 10 V p–p,								
	R_{LOAD} = 1 kΩ	±15 V		280			280		kHz
Slew Rate	R_{LOAD} = 1 kΩ	±15 V	12.5	18		12.5	18		V/μs
COMMON-MODE REJECTION	V_{CM} = ±11 V	±15 V	110	130		120	130		dB
	T_{MIN} to T_{MAX}		106	120		110	120		dB
POWER SUPPLY REJECTION	V_S = ±4.75 V to ±18 V		110	130		120	130		dB
	T_{MIN} to T_{MAX}		107	120		114	120		dB
INPUT VOLTAGE NOISE	f = 0.1 Hz to 10 Hz	±15 V		50			50		nV p–p
	f = 10 Hz	±15 V		1.7	2.5		1.7	2.5	nV/√Hz
	f = 1 kHz	±15 V		0.9	1.2		0.9	1.2	nV/√Hz
	f = 1 MHz	±15 V		1.0			1.0		μV rms
INPUT CURRENT NOISE	f = 1 kHz	±15 V		2.0			2.0		pA/√Hz
INPUT COMMON-MODE VOLTAGE RANGE	R_{LOAD} = 2 kΩ	±15 V		±12			±12		V
	R_{LOAD} = 2 kΩ	±5 V		±2.5			±2.5		V
OUTPUT CHARACTERISTICS									
Output Voltage Swing	R_{LOAD} = 2 kΩ	±15 V	±12	±13		±12	±13		V
	R_{LOAD} = 600 Ω	±15 V	±11	±13		±11	±13		V
Short-Circuit Current		±5 V, ±15 V		80			80		mA
Output Current		±5 V, ±15 V	30	50		30	50		mA
TOTAL HARMONIC DISTORTION	R_{LOAD} = 2 kΩ f = 250 kHz, 3 V rms	±15 V		−98			−98		dB
	R_{LOAD} = 600 Ω f = 20 kHz, 7 V rms	±15 V		−110			−110		dB
INPUT CHARACTERISTICS									
Input Resistance (Differential)				7.5			7.5		kΩ
Input Resistance (Common Mode)				100			100		MΩ
Input Capacitance (Differential)[3]				10			10		pF
Input Capacitance (Common Mode)				5			5		pF
OUTPUT RESISTANCE	A_V = +1, f = 1 kHz			3			3		mΩ
POWER SUPPLY									
Operating Range			±4.75		±18	±4.75		±18	V
Quiescent Current		±15		7.5	9.5		7.5	9.5	mA

PRELIMINARY TECHNICAL DATA

NOTES
[1]Specified using external decompensation capacitor, see Applications section.
[2]Full Power Bandwidth = Slew Rate/2 π V_{PEAK}.
[3]Differential input capacitance consists of 1.5 pF package capacitance and 8.5 pF from the input differential pair.
Specifications subject to change without notice.

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ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
  Plastic DIP (N) . . . . . 1.3 W
  Small Outline (R) . . . . . 0.9 W
  Cerdip (Q) . . . . . 1.3 W
Input Voltage . . . . . $\pm V_S$
Differential Input Voltage[3] . . . . . ±0.7 V
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range (Q) . . . . . −65°C to +150°C
Storage Temperature Range (N, R) . . . . . −65°C to +125°C
Operating Temperature Range
  AD797A/B . . . . . −40°C to +85°C
  AD797S . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Thermal Characteristics
8-Pin Plastic Package: θ_{JA} = 95°C/W
8-Pin Cerdip Package: θ_{JA} = 110°C/W
8-Pin Small Outline Package: θ_{JA} = 155°C/W

[3]The AD797's inputs are protected by back-to-back diodes. To achieve low noise, internal current limiting resistors could not be incorporated into the design of this amplifier. If the differential input voltage exceeds 0.7 V, the input current should be limited to less than 25 mA by series protection resistors. Note, however, that this will degrade the low noise performance of the device.

PRELIMINARY TECHNICAL DATA

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD797AN	−40°C to +85°C	8-Pin Plastic DIP	N-8
AD797BN	−40°C to +85°C	8-Pin Plastic DIP	N-8
AD797AR	−40°C to +85°C	8-Pin Plastic SO	R-8
AD797SQ/883B	−55°C to +125°C	8-Pin Cerdip	Q-8

*For outline information see Package Information section.

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AD797—Typical Characteristics

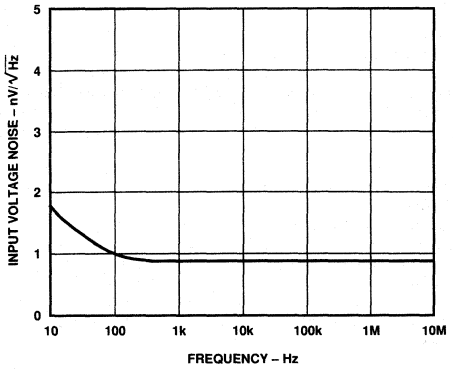


Figure 1. Input Voltage Noise Spectral Density

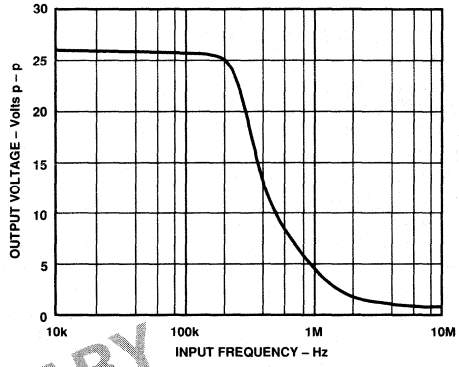


Figure 2. Large Signal Frequency Response

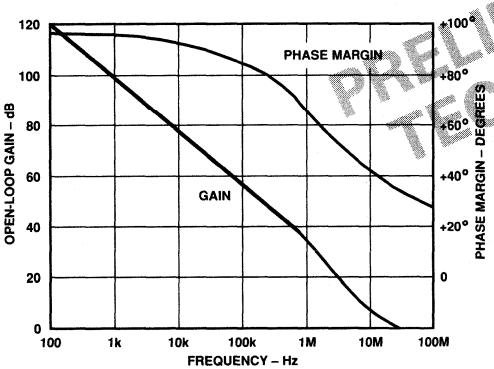


Figure 3. Open Loop Gain & Phase vs. Frequency

PRELIMINARY TECHNICAL DATA

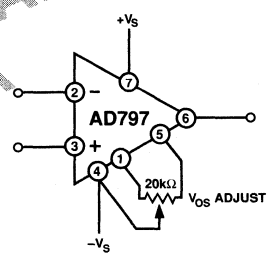


Figure 4. Offset Null Configuration

Amorphous (Photodiode) Detector

Large area photodiodes $C_S \geq 500$ pF and certain image detectors (amorphous Si), have optimum performance when used in conjunction with amplifiers with very low voltage rather than very low current noise. Figure 5 shows the AD797 used with an amorphous Si (C_S = 1000 pF) detector. The response is adjusted for flatness with C_F, while the noise is dominated by voltage noise amplified by the ac noise gain. The 797's excellent input noise performance gives 27 μV rms total noise in 1 MHz bandwidth, as shown by Figure 6.

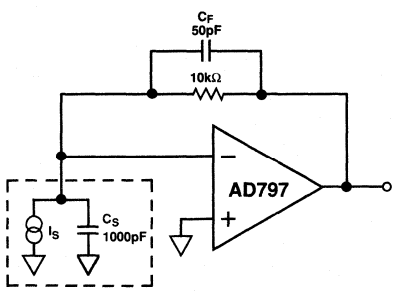


Figure 5. Amorphous Detector Preamp

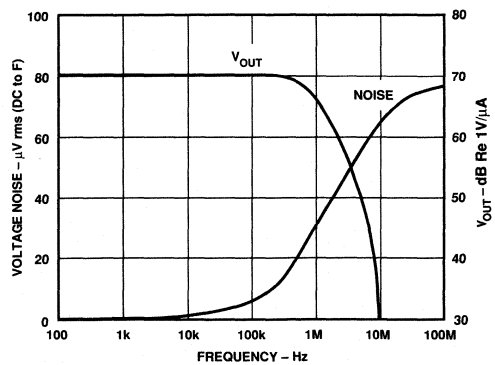


Figure 6. Voltage Noise Spectral Density & V_{OUT} of Amorphous Detector Preamp

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Differential Line Receiver

The differential receiver circuit of Figure 7 is useful for many applications from audio to MRI imaging. It allows extraction of a low level signal in the presence of common-mode noise. As shown in Figure 8, the AD797 provides this function with only 9 nV/$\sqrt{\text{Hz}}$ noise at the output. Figure 9 shows the AD797's 20-bit THD performance over the audio band and 16-bit accuracy to 250 kHz.

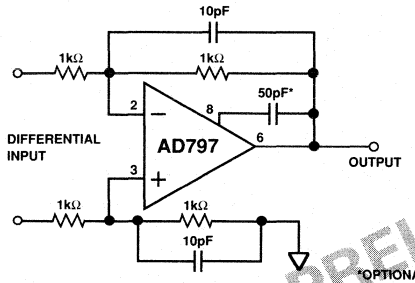


Figure 7. Differential Line Receiver

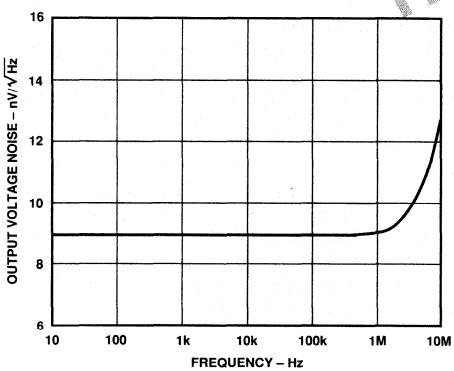


Figure 8. Output Voltage Noise Spectral Density for Differential Line Receiver

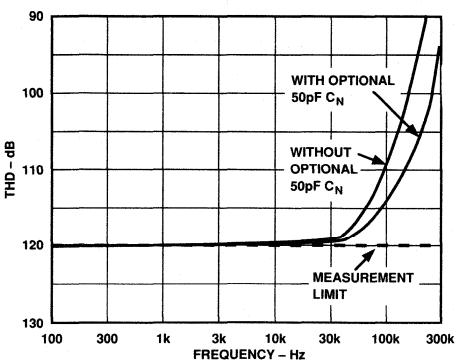


Figure 9. Total Harmonic Distortion (THD) vs. Frequency for Differential Receiver

Low Noise Preamplifier Applications

The AD797 has an input voltage noise specification of 0.9 nV/$\sqrt{\text{Hz}}$. This is less than the Johnson noise of a 50 Ω resistor. The equivalent source resistance of any feedback network should, therefore, be <50 Ω in order to obtain optimum noise performance. This implies that in some applications the amplifier sees a substantial load just in driving its own feedback network. As with all voltage feedback amplifiers, the bandwidth and the distortion reducing benefit of feedback are both reduced in proportion to the closed-loop gain. The design of the AD797 addresses these problems by providing passive (patent pending) distortion cancellation at the output. In addition, the bandwidth is enhanced via decompensation. A single extra pin allows the user to simultaneously decompensate the amplifier and neutralize output distortion. The performance of the AD797 with and without the use of these features is summarized in Figure 10 and Table I. Figure 11 provides THD performance at 3 volts rms.

PRELIMINARY TECHNICAL DATA

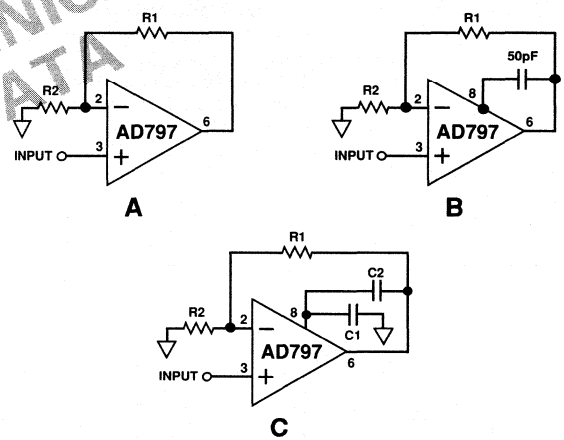


Figure 10. Low Noise Preamp Connections With and Without External Compensation

Table I. Recommended External Compensation

	A/B/C		A			B			C		
	R1	R2	C1 (pF)	C2 (pF)	3 dB BW	C1 (pF)	C2 (pF)	3 dB BW	C1 (pF)	C2 (pF)	3 dB BW
G = 100	990	10	0	0	1 MHz	0	50	1 MHz	12	39	1.5 MHz
G = 1000	9990	10	0	0	96 kHz	0	50	96 kHz	39	12	450 kHz

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

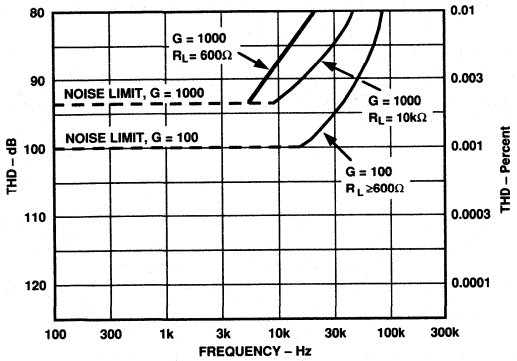


Figure 11. Total Harmonic Distortion (THD) vs. Frequency @ 3 V rms

Professional Audio Signal Processing—DAC Buffers

The low noise and low distortion of the AD797 make it an ideal choice for professional audio signal processing. An ideal I-to-V converter for a current out DAC would simply be a resistor to ground, were it not for the fact that most DACs do not operate linearly with voltage on their output. Standard practice is to operate an op amp as an I-to-V converter creating a virtual ground at its inverting input, Figure 12. In this configuration clock energy and current steps must be absorbed by the op amp's output stage. The unusual configuration, shown in Figure 12, shunts high frequency energy to ground while correctly reproducing the desired output with extremely low THD and IMD distortion.

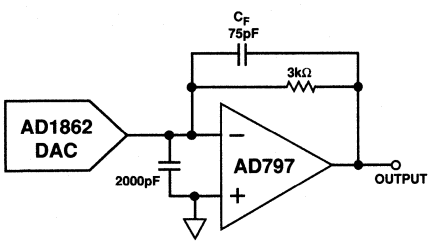


Figure 12. A Professional Audio DAC Buffer

A General Purpose ATE/Instrumentation Input/Output Driver

The ultralow noise and distortion of the AD797 may be combined with the wide bandwidth, slew rate, and load drive of a current feedback amplifier to yield a very wide dynamic range general purpose driver. The circuit of Figure 13 combines the AD797 with the AD811 in just such an application. Using the component values shown, this circuit is capable of better than −90 dB THD with a ±5 V, 500 kHz output signal. The circuit is therefore suitable for driving high resolution A/D converters and as an output driver in automatic test equipment (ATE) systems. Using a 100 kHz sine wave, the circuit will drive a 600 Ω load to a level of 7 V rms with less than −109 dB THD, and a 10 kΩ load at less than −117 dB THD.

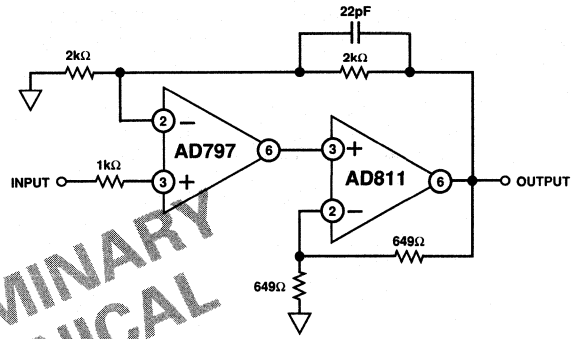


Figure 13. A General Purpose ATE/Instrumentation Input/Output Driver

PRELIMINARY TECHNICAL DATA

Ultrasound/Sonar Preamp

The AD600, variable-gain-amplifier, provides the time controlled gain (TCG) function necessary for very wide dynamic range sonar and ultrasound applications. Under some circumstances, it is necessary to buffer the input of the AD600 and preserve its low noise performance. To optimize dynamic range this buffer should have at most 6 dB of gain. The combination of low noise as well as low gain is difficult to achieve. The input buffer circuit of Figure 14 provides 1 nV$\sqrt{\text{Hz}}$ noise performance at a gain of two (dc to 1 MHz) by using 26.1 Ω resistors in its feedback path. Distortion is only −50 dBc @ 1 MHz at a 2 volt p–p output level and drops rapidly to better than −70 dBc at an output of 200 mV p–p.

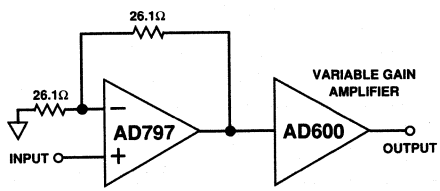


Figure 14. An Ultrasound Preamplifier Circuit

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Low Power Video Op Amp with Disable

AD810

FEATURES

High Speed
- 100 MHz Bandwidth (3 dB, G = +1)
- 65 MHz Bandwidth (3 dB, G = +2)
- 30 MHz Bandwidth (0.1 dB, G = +2)
- 1000 V/μs Slew Rate
- 50 ns Settling Time to 0.1% (V_O = 10 V Step)

Ideal for Video Applications (R_L = 150 Ω)
- 0.05% Differential Gain
- 0.05° Differential Phase

Low Noise
- 2.5 nV/$\sqrt{Hz}$ Input Voltage Noise

Low Power
- 8.0 mA Supply Current
- 2.0 mA Supply Current (Power-Down Mode)

High Performance Disable Function
- Turn-Off Time of 100 ns
- Input to Output Isolation of 60 dB (Off State)

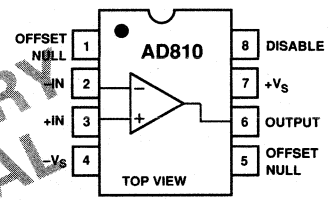
Flexible Operation
- Specified for ±5 V and ±15 V Operation
- ±2.5 V Output Swing into a 150 Ω Load (V_S = ±5 V)

APPLICATIONS

Professional Video Cameras
Multimedia Broadcast Systems
HDTV, NTSC, PAL & SECAM Compatible Systems
Video Line Driver
ADC/DAC Buffer
DC Restoration Circuits

CONNECTION DIAGRAM

8 Pin Plastic Mini-DIP (N), SOIC (R) and Cerdip (Q) Packages



PRELIMINARY TECHNICAL DATA

PRODUCT DESCRIPTION

The AD810 is an HDTV, NTSC, PAL and SECAM compatible video operational amplifier, which is ideal for use in any broadcast quality video system such as multimedia, video cameras and crosspoint switchers. The 65 MHz bandwidth at a gain of +2 is ideal for video applications and the differential gain and phase of 0.05% and 0.05° (NTSC and PAL) make the AD810 ideal for high quality video systems. The AD810 is designed for HDTV, NTSC & PAL compatibility so that the op amp meets a stringent 0.1 dB flatness specification at a bandwidth of 30 MHz (G = +2) and still meets differential gain and phase specs of 0.05% and 0.05°. All these specifications are under load conditions of 150 Ω (one 75 Ω back terminated cable), with low power supply current of 8.0 mA.

The AD810 is ideal for power sensitive applications such as video cameras. The disable feature reduces the power supply current to only 2 mA, while the amplifier is not in use, to conserve power. Furthermore the AD810 is specified over a power supply range of ±5 V to ±15 V for battery powered applications.

The AD810 works well as an ADC or DAC buffer in video systems due to its unity gain bandwidth of 100 MHz; furthermore because the AD810 is a transimpedence amplifier this bandwidth can be maintained over a wide range of gains. Also the AD810 offers low noise of 2.5 nV/$\sqrt{Hz}$ for wide dynamic range applications.

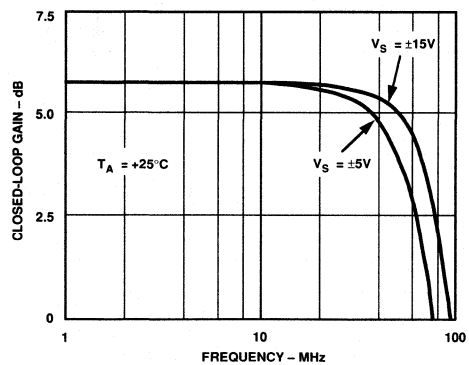


Figure 1. Closed-Loop Gain vs. Frequency for $R_F = R_G$ = 750 Ω, R_L = 150 Ω

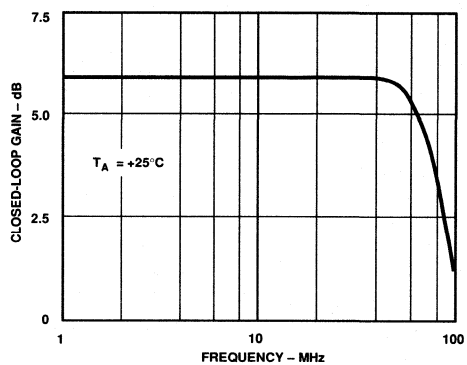


Figure 2. Closed-Loop Gain vs. Frequency for R_F = 649 Ω, R_L = 150 Ω

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD810—SPECIFICATIONS (@ T_A = +25°C and V_S = ±15 V dc, R_L = 150 Ω unless otherwise noted)

Model	Conditions	V_S	AD810A Min	AD810A Typ	AD810A Max	AD810S[1] Min	AD810S[1] Typ	AD810S[1] Max	Units
DYNAMIC PERFORMANCE									
3 dB Bandwidth	(G = +2) R_{FB} = 649	±5 V		65			65		MHz
	(G = +2) R_{FB} = 750	±5 V		55			55		MHz
	(G = +2) R_{FB} = 649	±15 V		85			85		MHz
	(G = +2) R_{FB} = 750	±15 V		70			70		MHz
	(G = +1) R_{FB} = 649	+15 V		100			100		MHz
	(G = +10) R_{FB} = 649	±15 V		50			50		MHz
0.1 dB Bandwidth	(G = +2) R_{FB} = 649	±5 V		20			20		MHz
	(G = +2) R_{FB} = 750	±5 V		10			10		MHz
	(G = +2) R_{FB} = 649	±15 V		30			30		MHz
	(G = +2) R_{FB} = 750	±15 V		15			15		MHz
Full Power Bandwidth	V_O = 20 V p-p,								
	R_{LOAD} = 400 Ω	±15 V		16			16		MHz
Slew Rate	R_{LOAD} = 150 Ω	±15 V		1000			1000		V/μs
		±5 V		400			400		V/μs
Settling Time to 0.1%	10 V Step, A_V = −1	±15 V		50			50		ns
Differential Gain	f = 3.58 MHz	±15 V		0.02			0.02		%
	f = 3.58 MHz	±5 V		0.03			0.03		%
Differential Phase	f = 3.58 MHz	±15 V		0.03			0.03		Degrees
	f = 3.58 MHz	±5 V		0.05			0.05		Degrees
INPUT OFFSET VOLTAGE		±15 V		0.5	3		0.5	3	mV
Offset Voltage Drift				5			5		μV/°C
INPUT BIAS CURRENT	(−Input)	±15 V		2	5		2	5	μA
	(+Input)	±15 V		2	10		2	10	μA
OPEN-LOOP TRANSRESISTANCE	V_O = ±10 V, R_L = 400 Ω	±15 V		1.5			1.5		MΩ
COMMON-MODE REJECTION	V_{CM} = ±12 V,	±15 V							
V_{OS}	V_{CM} = ±2.5 V	±5 V		60			60		dB
Input Current				1			1		μA/V
POWER SUPPLY REJECTION	V_S = ±4 V to ±18 V								
V_{OS}				64			64		dB
Input Current				0.5			0.5		μA/V
INPUT VOLTAGE NOISE	f = 1 kHz	±15 V		2.5			2.5		nV/√Hz
INPUT CURRENT NOISE	$-I_{IN}$, f = 1 kHz	±15 V		20			20		pA/√Hz
	$+I_{IN}$, f = 1 kHz	±15 V		1.5			1.5		pA/√Hz
INPUT COMMON-MODE VOLTAGE RANGE		±5 V		±3.0			±3.0		V
		±15 V		±12.5			±12.5		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 150 Ω	±5 V		±2.9			±2.9		V
	R_{LOAD} = 500 Ω	±15 V		±12.9			±12.9		V
Short-Circuit Current		±15 V		150			150		mA
Output Current				60			60		mA
INPUT CHARACTERISTICS									
Input Resistance	(+Input)			5			5		MΩ
Input Resistance	(−Input)			35			35		Ω
Input Capacitance	(+Input)			2			2		pF
OUTPUT RESISTANCE	Open Loop (5 MHz)			15			15		Ω
DISABLE CHARACTERISTICS									
OFF Isolation	f = 10 MHz			50			50		dB
OFF Output Impedance				$(R_F+R_G)\|\|6$ pF			$(R_F+R_G)\|\|6$ pF		
Turn On Time	(Before Z_{OUT} = Low)			400			400		ns
Turn Off Time	(Before Z_{OUT} = High)			100			100		ns

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Model	Conditions	V_S	AD810A Min	AD810A Typ	AD810A Max	AD810S[1] Min	AD810S[1] Typ	AD810S[1] Max	Units
POWER SUPPLY									
Operating Range			±4.0		±18	±4.0		±18	V
Quiescent Current		±5 V		6.5			6.5		mA
		±15 V		7.0			7.0		mA
Power-Down Current		±5 V		1.8			1.8		mA
		±15 V		2.3			2.3		mA

NOTE
[1]See Analog Devices Military datasheet for 883B tested specifications.
Specifications subject to change without notice.

2

PRELIMINARY TECHNICAL DATA

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
Common-Mode Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±6 V
Storage Temperature Range (Q) . . . . . −65°C to +150°C
Storage Temperature Range (N) . . . . . −65°C to +125°C
Storage Temperature Range (R) . . . . . −65°C to +125°C
Operating Temperature Range
AD810A . . . . . −40°C to +85°C
AD810S . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 seconds) . . . . . 300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Pin Plastic DIP Package: θ_{JA} = 90°C/Watt
8-Pin Cerdip Package: θ_{JA} = 110°C/Watt
8-Pin SOIC Package: θ_{JA} = 150°C/Watt

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD810AN	−40°C to +85°C	8-Pin Plastic DIP	N-8
AD810AR	−40°C to +85°C	8-Pin Plastic SOIC	R-8
AD810SQ/883B	−55°C to +125°C	8-Pin Cerdip	Q-8

*For outline information see Package Information section.

ESD SUSCEPTIBILITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although the AD810 features proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ANALOG DEVICES

High Performance Video Op Amp

AD811

FEATURES

High Speed
- 140 MHz Bandwidth (3 dB, G = +1)
- 120 MHz Bandwidth (3 dB, G = +2)
- 35 MHz Bandwidth (0.1 dB, G = +2)
- 2500 V/μs Slew Rate
- 25 ns Settling Time to 0.1% (For a 2 V Step)
- 65 ns Settling Time to 0.01% (For a 10 V Step)

Excellent Video Performance (R_L = 150 Ω)
- 0.01% Differential Gain, 0.01° Differential Phase
- Voltage Noise of 1.9 nV/√Hz

Low Distortion: THD = −74 dB @ 10 MHz

Excellent DC Precision
- 3 mV max Input Offset Voltage

Flexible Operation
- Specified for ±5 V and ±15 V Operation
- ±2.3 V Output Swing into a 75 Ω Load (V_S = ±5 V)

APPLICATIONS

Video Crosspoint Switchers, Multimedia Broadcast Systems

HDTV Compatible Systems

Video Line Drivers, Distribution Amplifiers

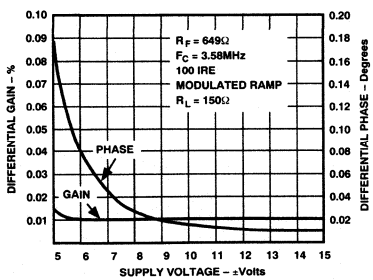
ADC/DAC Buffers

DC Restoration Circuits

Medical—Ultrasound, PET, Gamma & Counter Applications

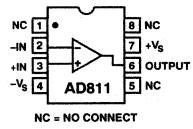
PRODUCT DESCRIPTION

The AD811 is a wideband current-feedback operational amplifier, optimized for broadcast quality video systems. The −3 dB bandwidth of 120 MHz at a gain of +2 and differential gain and phase of 0.01% and 0.01° (R_L = 150 Ω) make the AD811 an excellent choice for all video systems. The AD811 is designed to meet a stringent 0.1 dB gain flatness specification to a bandwidth of 35 MHz (G = +2) in addition to the low differential gain and phase errors. This performance is achieved whether driving one or two back terminated 75 Ω cables, with a low power supply current of 16.5 mA. Furthermore, the AD811 is specified over a power supply range of ±4.5 V to ±18 V.



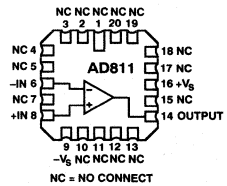
CONNECTION DIAGRAMS

8-Pin Plastic (N-8), Cerdip (Q-8) and SOIC (R-8) Packages



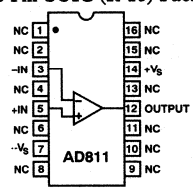
NC = NO CONNECT

20-Pin LCC (E-20A) Package



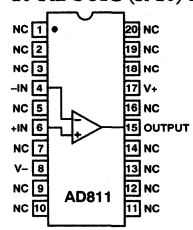
NC = NO CONNECT

16-Pin SOIC (R-16) Package



NC = NO CONNECT

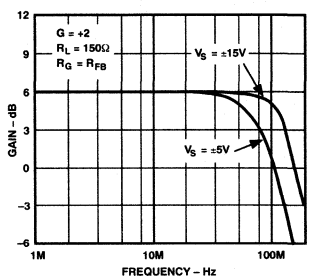
20-Pin SOIC (R-20) Package



NC = NO CONNECT

The AD811 is also excellent for pulsed applications where transient response is critical. It can achieve a maximum slew rate of greater than 2500 V/μs with a settling time of less than 25 ns to 0.1% on a 2 volt step and 65 ns to 0.01% on a 10 volt step.

The AD811 is ideal as an ADC or DAC buffer in data acquisition systems due to its low distortion up to 10 MHz and its wide unity gain bandwidth. Because the AD811 is a current feedback amplifier, this bandwidth can be maintained over a wide range of gains. The AD811 also offers low voltage and current noise of 1.9 nV/√Hz and 20 pA/√Hz, respectively, and excellent dc accuracy for wide dynamic range applications.



AD811—SPECIFICATIONS (@ T_A = +25°C and V_S = ±15 V dc, R_{LOAD} = 150 Ω unless otherwise noted)

Model	Conditions	V_S	AD811J/A[1] Min	AD811J/A[1] Typ	AD811J/A[1] Max	AD811S[2] Min	AD811S[2] Typ	AD811S[2] Max	Units
DYNAMIC PERFORMANCE									
Small Signal Bandwidth (No Peaking)									
−3 dB									
G = +1	R_{FB} = 562 Ω	±15 V		140			140		MHz
G = +2	R_{FB} = 649 Ω	±15 V		120			120		MHz
G = +2	R_{FB} = 562 Ω	±5 V		80			80		MHz
G = +10	R_{FB} = 511 Ω	±15 V		100			100		MHz
0.1 dB Flat									
G = +2	R_{FB} = 562 Ω	±5 V		25			25		MHz
	R_{FB} = 649 Ω	±15 V		35			35		MHz
Full Power Bandwidth[3]	V_{OUT} = 20 V p-p	±15 V		40			40		MHz
Slew Rate	V_{OUT} = 4 V p-p	±5 V		400			400		V/µs
	V_{OUT} = 20 V p-p	±15 V		2500			2500		V/µs
Settling Time to 0.1%	10 V Step, A_V = −1	±15 V		50			50		ns
Settling Time to 0.01%				65			65		ns
Settling Time to 0.1%	2 V Step, A_V = −1	±5 V		25			25		ns
Rise Time, Fall Time	R_{FB} = 649, A_V = +2	±15 V		3.5			3.5		ns
Differential Gain	f = 3.58 MHz	±15 V		0.01			0.01		%
Differential Phase	f = 3.58 MHz	±15 V		0.01			0.01		Degree
THD @ f_C = 10 MHz	V_{OUT} = 2 V p-p, A_V = +2	±15 V		−74			−74		dBc
Third Order Intercept[4]	@ f_C = 10 MHz	±5 V		36			36		dBm
		±15 V		43			43		dBm
INPUT OFFSET VOLTAGE		±5 V, ±15 V		0.5	3		0.5	3	mV
	T_{MIN} to T_{MAX}				5			5	mV
Offset Voltage Drift				5			5		µV/°C
INPUT BIAS CURRENT									
−Input		±5 V, ±15 V		2	5		2	5	µA
	T_{MIN} to T_{MAX}				15			30	µA
+Input		±5 V, ±15 V		2	10		2	10	µA
	T_{MIN} to T_{MAX}				20			25	µA
TRANSRESISTANCE	T_{MIN}–T_{MAX}								
	V_{OUT} = ±10 V								
	R_L = ∞	±15 V	0.75	1.5		0.75	1.5		MΩ
	R_L = 200 Ω	±15 V	0.5	0.75		0.5	0.75		MΩ
	V_{OUT} = ±2.5 V								
	R_L = 150 Ω	±5 V	0.25	0.4		0.125	0.4		MΩ
COMMON-MODE REJECTION									
V_{OS} (vs. Common Mode)									
T_{MIN}–T_{MAX}	V_{CM} = ±2.5	±5 V	56	60		50	60		dB
T_{MIN}–T_{MAX}	V_{CM} = ±10 V	±15 V	60	66		56	66		dB
Input Current (vs. Common Mode)	T_{MIN}–T_{MAX}			1	3		1	3	µA/V
POWER SUPPLY REJECTION	V_S = ±4.5 V to ±18 V								
V_{OS}	T_{MIN}–T_{MAX}		60	70		60	70		dB
+Input Current	T_{MIN}–T_{MAX}			0.3	2		0.3	2	µA/V
−Input Current	T_{MIN}–T_{MAX}			0.4	2		0.4	2	µA/V
INPUT VOLTAGE NOISE	f = 1 kHz			1.9			1.9		nV/√Hz
INPUT CURRENT NOISE	f = 1 kHz			20			20		pA/√Hz
OUTPUT CHARACTERISTICS									
Voltage Swing, Useful Operating Range[5]		±5 V		±2.9			±2.9		V
		±15 V		±12			±12		V
Output Current	T_J = +25°C			100			100		mA
Short-Circuit Current				150			150		mA
Output Resistance	(Open Loop @ 5 MHz)			9			9		Ω
INPUT CHARACTERISTICS									
+Input Resistance				1.5			1.5		MΩ
−Input Resistance				14			14		Ω
Input Capacitance	+Input			7.5			7.5		pF
Common-Mode Voltage Range		±5 V		±3			+3		V
		±15 V		±13			±13		V
POWER SUPPLY									
Operating Range			±4.5		±18	±4.5		±18	V
Quiescent Current		±5 V		14.5	16.0		14.5	16.0	mA
		±15 V		16.5	18.0		16.5	18.0	mA
TRANSISTOR COUNT	# of Transistors			40			40		

NOTES
[1]The AD811JR is specified with ±5 V power supplies only, with operation up to ±12 volts.
[2]See Analog Devices' military data sheet for 883B tested specifications.
[3]FPBW = slew rate/(2 π V_{PEAK})
[4]Output power level, tested at a closed loop gain of two.
[5]Useful operating range is defined as the output voltage at which linearity begins to degrade.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
AD811JR Grade Only . . . . . ±12 V
Internal Power Dissipation[2] . . . . . Observe Derating Curves
Output Short Circuit Duration . . . . . Observe Derating Curves
Common-Mode Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±6 V
Storage Temperature Range (Q, E) . . . . . −65°C to +150°C
Storage Temperature Range (N, R) . . . . . −65°C to +125°C
Operating Temperature Range
AD811J . . . . . 0°C to +70°C
AD811A . . . . . −40°C to +85°C
AD811S . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]8-Pin Plastic Package: θ_{JA} = 90°C/Watt
8-Pin Cerdip Package: θ_{JA} = 110°C/Watt
8-Pin SOIC Package: θ_{JA} = 155°C/Watt
16-Pin SOIC Package: θ_{JA} = 85°C/Watt
20-Pin SOIC Package: θ_{JA} = 80°C/Watt
20-Pin LCC Package: θ_{JA} = 70°C/Watt

ORDERING GUIDE

Model	Temperature Range	Package*
AD811AN	−40°C to +85°C	N-8
AD811AR-16	−40°C to +85°C	R-16
AD811AR-20	−40°C to +85°C	R-20
AD811JR	0°C to +70°C	R-8
AD811SQ/883B	−55°C to +125°C	Q-8
AD811SE/883B	−55°C to +125°C	E-20A
AD811ACHIPS	−40°C to +85°C	Die
AD811SCHIPS	−55°C to +125°C	Die

*E = Ceramic Leadless Chip Carrier; N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD811 is limited by the associated rise in junction temperature. For the plastic packages, the maximum safe junction temperature is 145°C. For the cerdip and LCC packages, the maximum junction temperature is 175°C. If these maximums are exceeded momentarily, proper circuit operation will be restored as soon as the die temperature is reduced. Leaving the device in the "overheated" condition for an extended period can result in device burnout. To ensure proper operation, it is important to observe the derating curves in Figures 17 and 18.

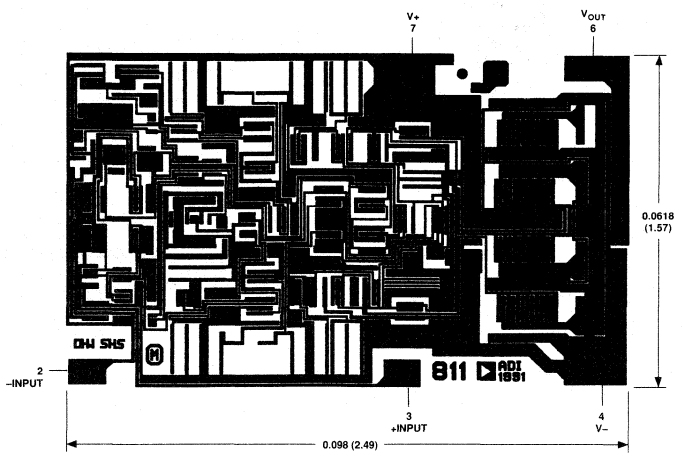
While the AD811 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature is not exceeded under all conditions. One important example is when the amplifier is driving a reverse terminated 75 Ω cable and the cable's far end is shorted to a power supply. With power supplies of ±12 volts (or less) at an ambient temperature of +25°C or less, if the cable is shorted to a supply rail, then the amplifier will not be destroyed, even if this condition persists for an extended period.

ESD SUSCEPTIBILITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although the AD811 features proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

METALIZATION PHOTOGRAPH

Contact Factory for Latest Dimensions.
Dimensions Shown in Inches and (mm).



AD811—Typical Characteristics

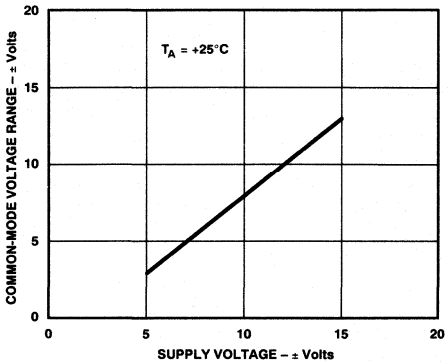


Figure 1. Input Common-Mode Voltage Range vs. Supply

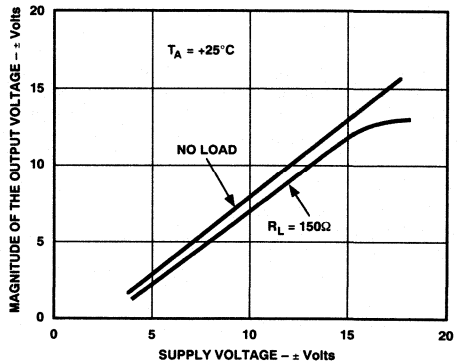


Figure 2. Output Voltage Swing vs. Supply

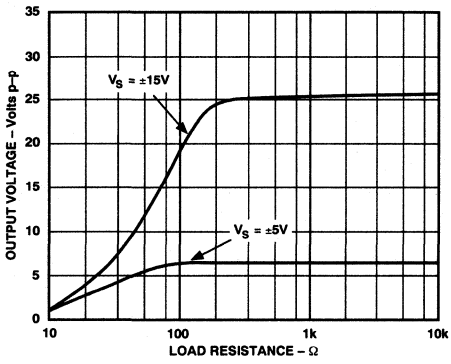


Figure 3. Output Voltage Swing vs. Resistive Load

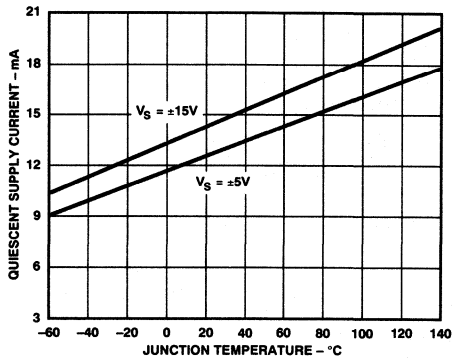


Figure 4. Quiescent Supply Current vs. Junction Temperature

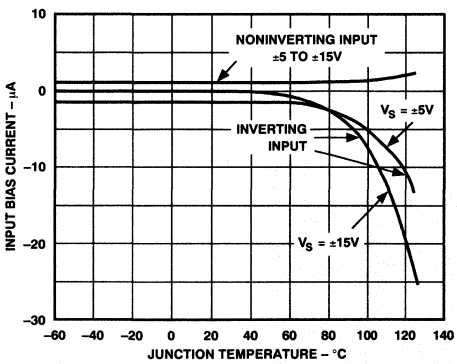


Figure 5. Input Bias Current vs. Junction Temperature

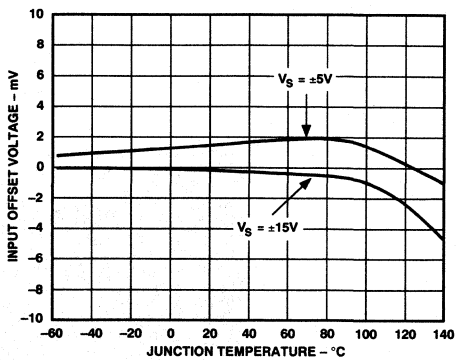


Figure 6. Input Offset Voltage vs. Junction Temperature

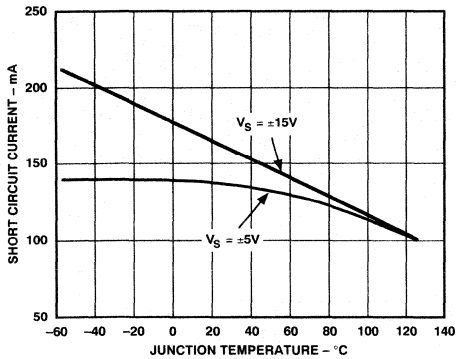


Figure 7. Short Circuit Current vs. Junction Temperature

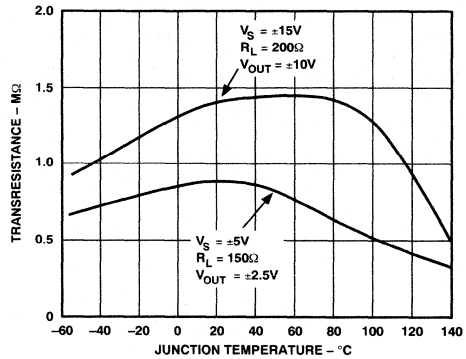


Figure 8. Transresistance vs. Junction Temperature

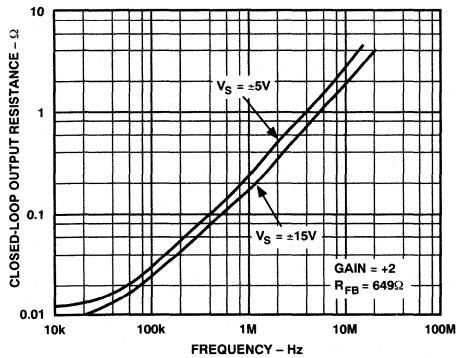


Figure 9. Closed-Loop Output Resistance vs. Frequency

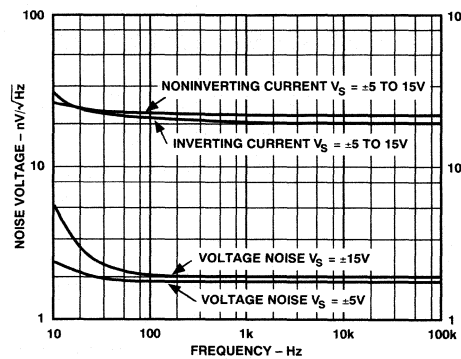


Figure 10. Input Noise vs. Frequency

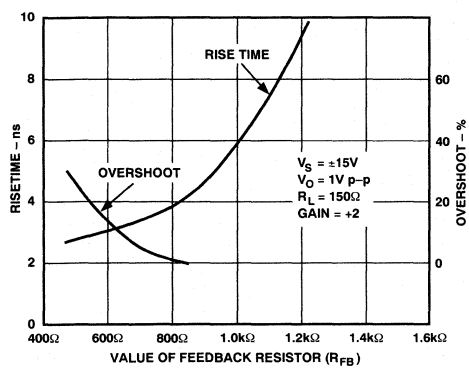


Figure 11. Rise Time & Overshoot vs. Value of Feedback Resistor, R_{FB}

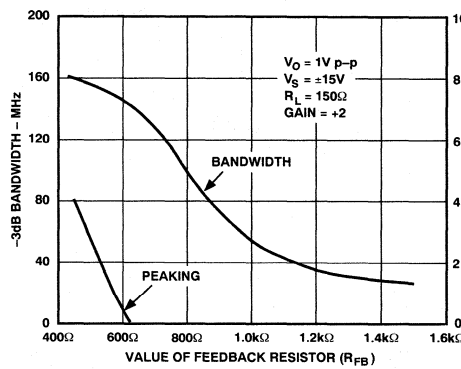


Figure 12. 3 dB Bandwidth & Peaking vs. Value of R_{FB}

AD811—Typical Characteristics

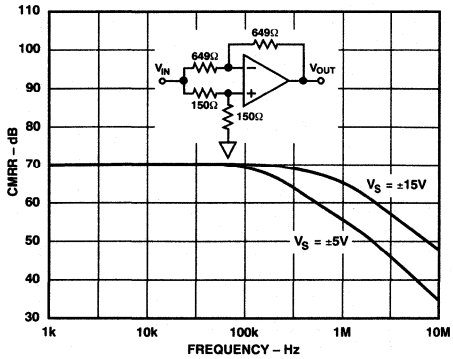


Figure 13. Common-Mode Rejection vs. Frequency

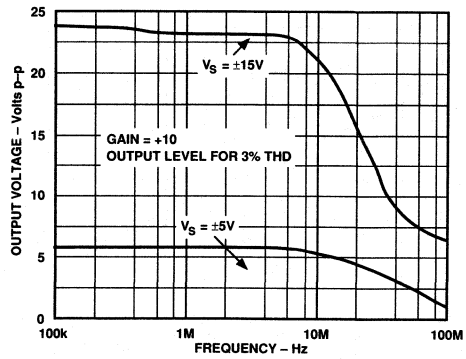


Figure 14. Large Signal Frequency Response

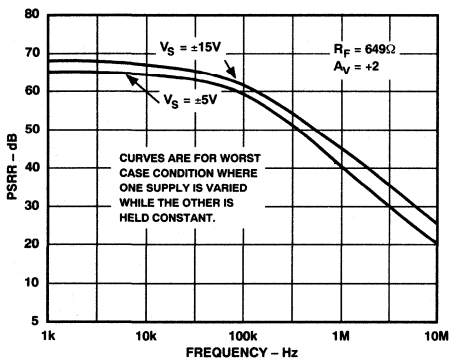


Figure 15. Power Supply Rejection vs. Frequency

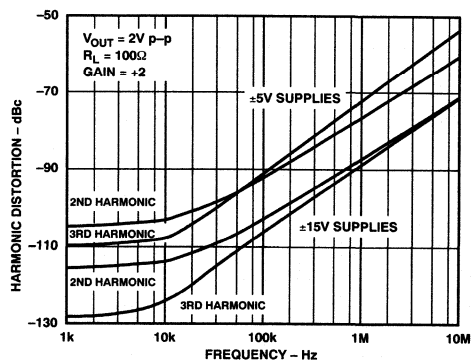


Figure 16. Harmonic Distortion vs. Frequency

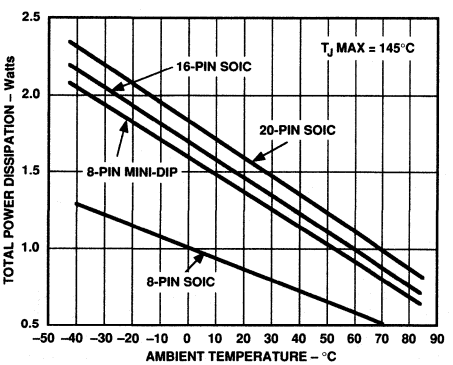


Figure 17. Maximum Power Dissipation vs. Temperature for Plastic Packages

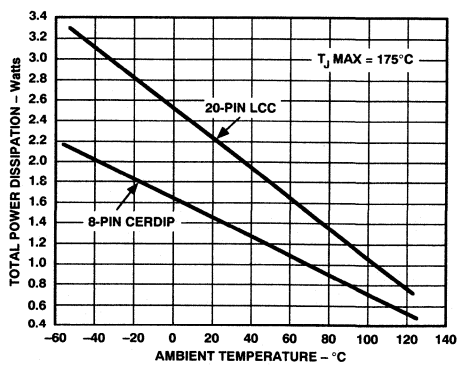


Figure 18. Maximum Power Dissipation vs. Temperature for Hermetic Packages

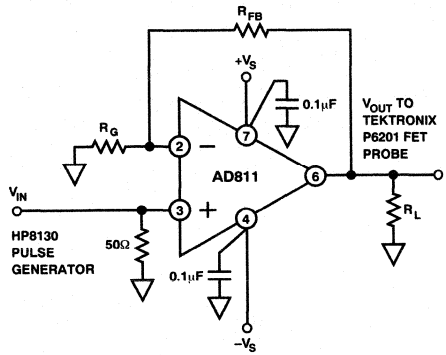


Figure 19. Noninverting Amplifier Connection

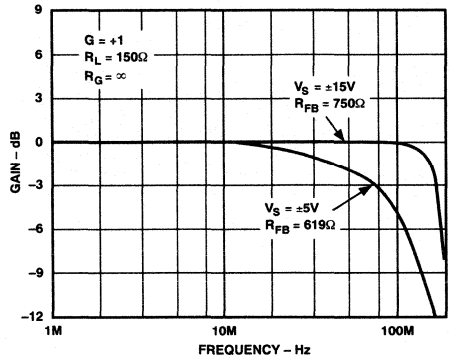


Figure 20. Closed-Loop Gain vs. Frequency, Gain = +1

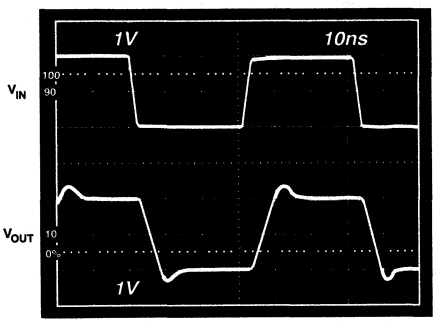


Figure 21. Small Signal Pulse Response, Gain = +1

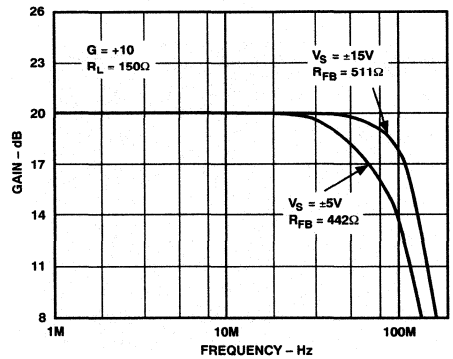


Figure 22. Closed-Loop Gain vs. Frequency, Gain = +10

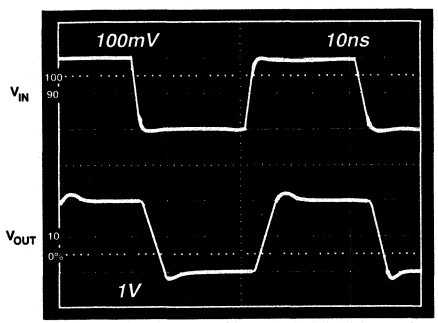


Figure 23. Small Signal Pulse Response, Gain = +10

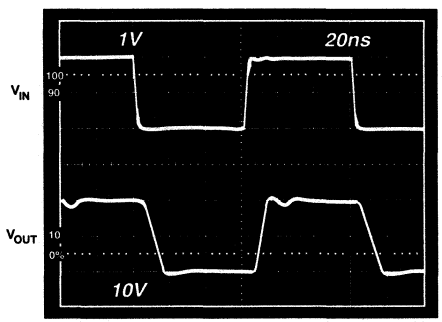


Figure 24. Large Signal Pulse Response, Gain = +10

AD811—Typical Characteristics, Inverting Connection

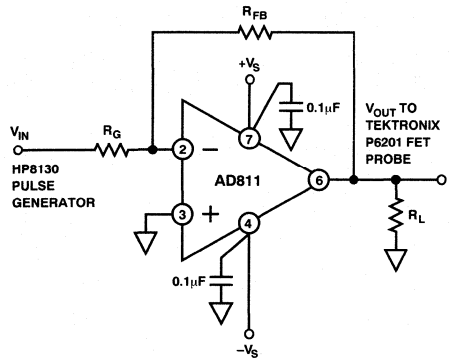


Figure 25. Inverting Amplifier Connection

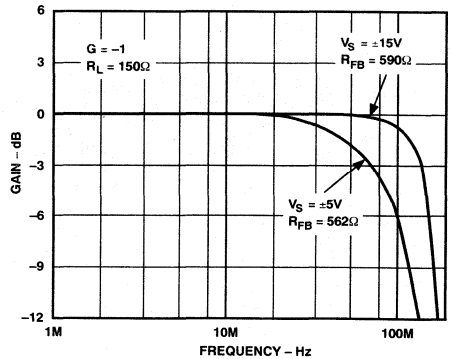


Figure 26. Closed-Loop Gain vs. Frequency, Gain = –1

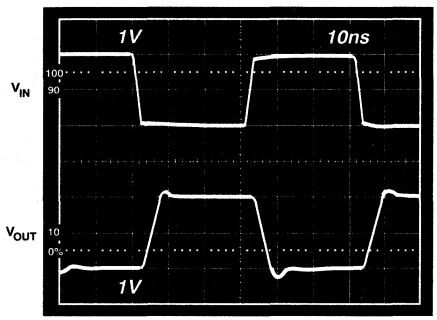


Figure 27. Small Signal Pulse Response, Gain = –1

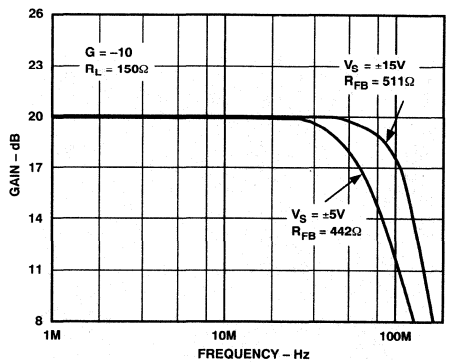


Figure 28. Closed-Loop Gain vs. Frequency, Gain = –10

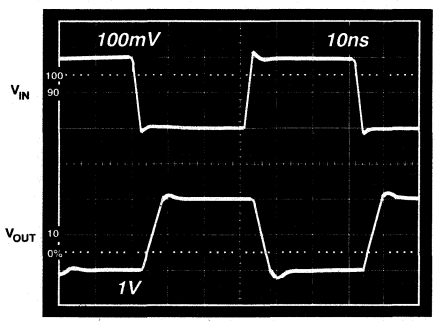


Figure 29. Small Signal Pulse Response, Gain = –10

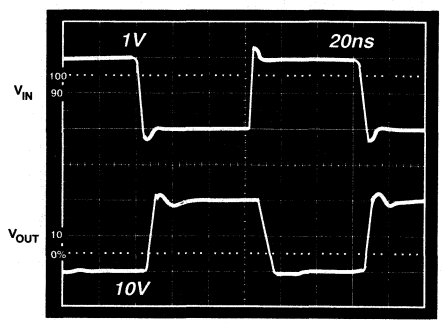


Figure 30. Large Signal Pulse Response, Gain = –10

AD811 APPLICATIONS

General Design Considerations

The AD811 is a current feedback amplifier optimized for use in high performance video and data acquisition applications. Since it uses a current feedback architecture, its closed-loop −3 dB bandwidth is dependent on the magnitude of the feedback resistor. The desired closed-loop gain and bandwidth are obtained by varying the feedback resistor (R_{FB}) to tune the bandwidth, and varying the gain resistor (R_G) to get the correct gain. Table I contains recommended resistor values for a variety of useful closed-loop gains and supply voltages.

Table I. −3 dB Bandwidth vs. Closed-Loop Gain and Resistance Values

V_S = ±15 V Closed-Loop Gain	R_{FB}	R_G	−3 dB BW (MHz)
+1	750 Ω		140
+2	649 Ω	649 Ω	120
+10	511 Ω	56.2 Ω	100
−1	590 Ω	590 Ω	115
−10	511 Ω	51.1 Ω	95
V_S = ±5 V Closed-Loop Gain	**R_{FB}**	**R_G**	**−3 dB BW (MHz)**
+1	619 Ω		80
+2	562 Ω	562 Ω	80
+10	442 Ω	48.7 Ω	65
−1	562 Ω	562 Ω	75
−10	442 Ω	44.2 Ω	65
V_S = ±10 V Closed-Loop Gain	**R_{FB}**	**R_G**	**−3 dB BW (MHz)**
+1	649 Ω		105
+2	590 Ω	590 Ω	105
+10	499 Ω	49.9 Ω	80
−1	590 Ω	590 Ω	105
−10	499 Ω	49.9 Ω	80

Figures 11 and 12 illustrate the relationship between the feedback resistor and the frequency and time domain response characteristics for a closed-loop gain of +2. (The response at other gains will be similar.)

The 3 dB bandwidth is somewhat dependent on the power supply voltage. As the supply voltage is decreased for example, the magnitude of internal junction capacitances is increased, causing a reduction in closed-loop bandwidth. To compensate for this, smaller values of feedback resistor are used at lower supply voltages.

Achieving the Flattest Gain Response at High Frequency

Achieving and maintaining gain flatness of better than 0.1 dB at frequencies above 10 MHz requires careful consideration of several issues.

Choice of Feedback and Gain Resistors

Because of the above-mentioned relationship between the 3 dB bandwidth and the feedback resistor, the fine scale gain flatness will, to some extent, vary with feedback resistor tolerance. It is, therefore, recommended that resistors with a 1% tolerance be used if it is desired to maintain flatness over a wide range of production lots. In addition, resistors of different construction have different associated parasitic capacitance and inductance. Metal-film resistors were used for the bulk of the characterization for this data sheet. It is possible that values other than those indicated will be optimal for other resistor types.

Printed Circuit Board Layout Considerations

As to be expected for a wideband amplifier, PC board parasitics can affect the overall closed loop performance. Of concern are stray capacitances at the output and the inverting input nodes. If a ground plane is to be used on the same side of the board as the signal traces, a space (3/16″ is plenty) should be left around the signal lines to minimize coupling. Additionally, signal lines connecting the feedback and gain resistors should be short enough so that their associated inductance does not cause high frequency gain errors. Line lengths less than 1/4″ are recommended.

Quality of Coaxial Cable

Optimum flatness when driving a coax cable is possible only when the driven cable is terminated at each end with a resistor matching its characteristic impedance. If the coax was ideal, then the resulting flatness would not be affected by the length of the cable. While outstanding results can be achieved using inexpensive cables, it should be noted that some variation in flatness due to varying cable lengths may be experienced.

Power Supply Bypassing

Adequate power supply bypassing can be critical when optimizing the performance of a high frequency circuit. Inductance in the power supply leads can form resonant circuits that produce peaking in the amplifier's response. In addition, if large current transients must be delivered to the load, then bypass capacitors (typically greater than 1 μF) will be required to provide the best settling time and lowest distortion. Although the recommended 0.1 μF power supply bypass capacitors will be sufficient in many applications, more elaborate bypassing (such as using two paralleled capacitors) may be required in some cases.

Driving Capacitive Loads

The feedback and gain resistor values in Table I will result in very flat closed-loop responses in applications where the load capacitances are below 10 pF. Capacitances greater than this will result in increased peaking and overshoot, although not necessarily in a sustained oscillation.

There are at least two very effective ways to compensate for this effect. One way is to increase the magnitude of the feedback resistor, which lowers the 3 dB frequency. The other method is to include a small resistor in series with the output of the amplifier to isolate it from the load capacitance. The results of these two techniques are illustrated in Figure 32. Using a 1.5 kΩ feedback resistor, the output ripple is less than 0.5 dB when driving 100 pF. The main disadvantage of this method is that it sacrifices a little bit of gain flatness for increased capacitive load drive capability. With the second method, using a series resistor, the loss of flatness does not occur.

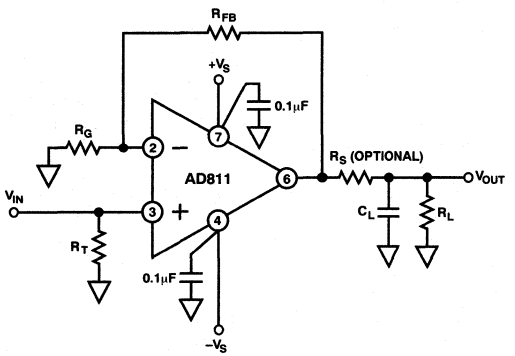


Figure 31. Recommended Connection for Driving a Large Capacitive Load

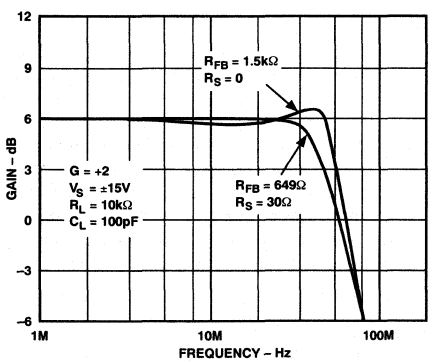


Figure 32. Performance Comparison of Two Methods for Driving a Capacitive Load

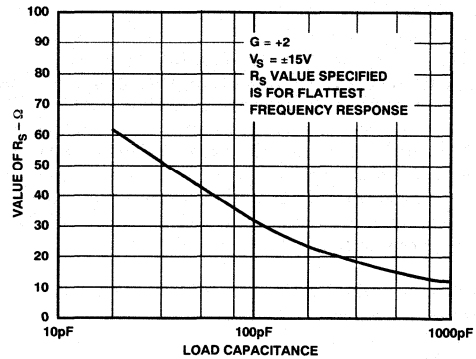


Figure 33. Recommended Value of Series Resistor vs. the Amount of Capacitive Load

Figure 33 shows recommended resistor values for different load capacitances. Refer again to Figure 32 for an example of the results of this method. Note that it may be necessary to adjust the gain setting resistor, R_G, to correct for the attenuation which results due to the divider formed by the series resistor, R_S, and the load resistance.

Applications which require driving a large load capacitance at a high slew rate are often limited by the output current available from the driving amplifier. For example, an amplifier limited to 25 mA output current cannot drive a 500 pF load at a slew rate greater than 50 V/μs. However, because of the AD811's 100 mA output current, a slew rate of 200 V/μs is achievable when driving this same 500 pF capacitor (see Figure 34).

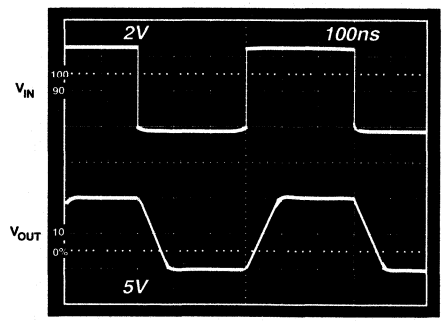


Figure 34. Output Waveform of an AD811 Driving a 500 pF Load. Gain = +2, R_{FB} = 649 Ω, R_S = 15 Ω, R_L = 10 kΩ

Operation as a Video Line Driver

The AD811 has been designed to offer outstanding performance at closed-loop gains of one or greater, while driving multiple reverse-terminated video loads. The lowest differential gain and phase errors will be obtained when using ±15 volt power supplies. With ±12 volt supplies, there will be an insignificant increase in these errors and a slight improvement in gain flatness. Due to power dissipation considerations, ±12 volt supplies are recommended for optimum video performance. Excellent performance can be achieved at much lower supplies as well.

The closed-loop gain vs. frequency at different supply voltages is shown in Figure 36. Figure 37 is an oscilloscope photograph of an AD811 line driver's pulse response with ±15 volt supplies. The differential gain and phase error vs. supply are plotted in Figures 38 and 39, respectively.

Another important consideration when driving multiple cables is the high frequency isolation between the outputs of the cables. Due to its low output impedance, the AD811 achieves better than 40 dB of output to output isolation at 5 MHz driving back terminated 75 Ω cables.

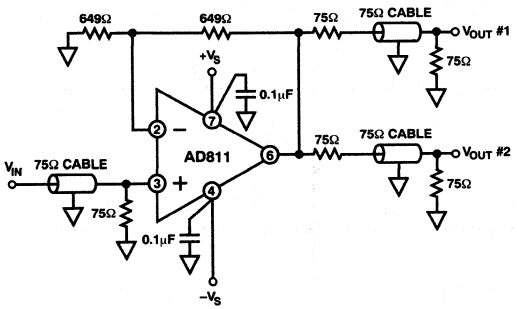


Figure 35. A Video Line Driver Operating at a Gain of +2

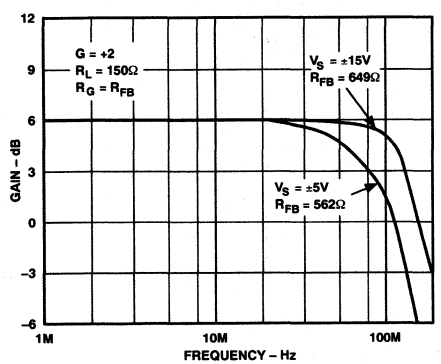


Figure 36. Closed-Loop Gain vs. Frequency, Gain = +2

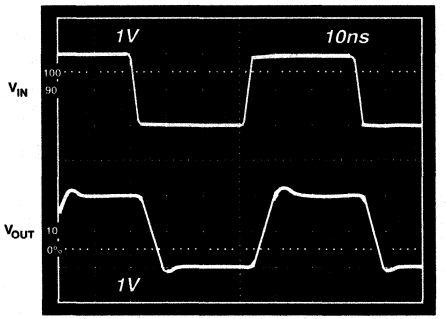


Figure 37. Small Signal Pulse Response, Gain = +2, V_S = ±15 V

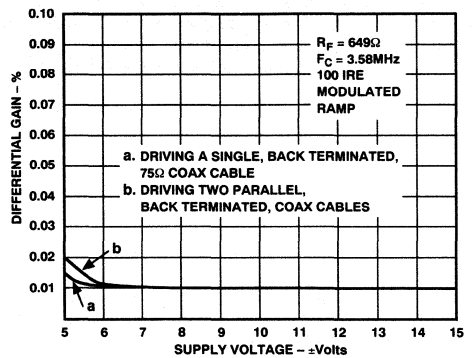


Figure 38. Differential Gain Error vs. Supply Voltage for the Video Line Driver of Figure 35

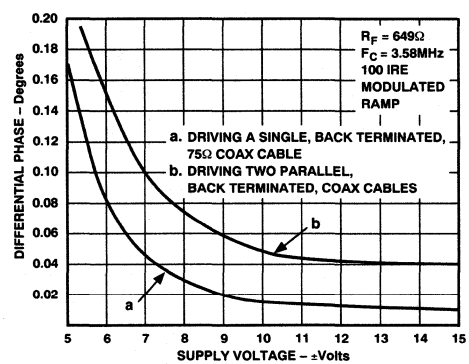


Figure 39. Differential Phase Error vs. Supply Voltage for the Video Line Driver of Figure 35

An 80 MHz Voltage-Controlled Amplifier Circuit

The voltage-controlled amplifier (VCA) circuit of Figure 40 shows the AD811 being used with the AD834, a 500 MHz, 4-quadrant multiplier. The AD834 multiplies the signal input by the dc control voltage, V_G. The AD834 outputs are in the form of differential currents from a pair of open collectors, ensuring that the full bandwidth of the multiplier (which exceeds 500 MHz) is available for certain applications. Here, the AD811 op amp provides a buffered, single-ended ground-referenced output. Using feedback resistors R8 and R9 of 511 Ω, the overall gain ranges from −70 dB, for V_G = 0 to +12 dB, (a numerical gain of four), when V_G = +1 V. The overall transfer function of the VCA is:

$$V_{OUT} = 4(X1 - X2)(Y1 - Y2)$$

which reduces to $V_{OUT} = 4\ V_G\ V_{IN}$ using the labeling conventions shown in Figure 40. The circuit's −3 dB bandwidth of 80 MHz, is maintained essentially constant—independent of gain. The response can be maintained flat to within ±0.1 dB from dc to 40 MHz at full gain with the addition of an optional capacitor of about 0.3 pF across the feedback resistor R8. The circuit produces a full-scale output of ±4 V for a ±1 V input, and can drive a reverse-terminated load of 50 Ω or 75 Ω to ±2 V.

The gain can be increased to 20 dB (×10) by raising R8 and R9 to 1.27 kΩ, with a corresponding decrease in −3 dB bandwidth to about 25 MHz. The maximum output voltage under these conditions will be increased to ±9 V using ±12 V supplies.

The gain-control input voltage, V_G, may be a positive or negative ground-referenced voltage, or fully differential, depending on the user's choice of connections at Pins 7 and 8. A positive value of V_G results in an overall noninverting response. Reversing the sign of V_G simply causes the sign of the overall response to invert. In fact, although this circuit has been classified as a voltage-controlled amplifier, it is also quite useful as a general-purpose four-quadrant multiplier, with good load-driving capabilities and fully-symmetrical responses from X- and Y-inputs.

The AD811 and AD834 can both be operated from power supply voltages of ±5 V. While it is not necessary to power them from the same supplies, the common-mode voltage at W1 and W2 must be biased within the common-mode range of the AD811's input stage. To achieve the lowest differential gain and phase errors, it is recommended that the AD811 be operated from power supply voltages of ±10 volts or greater. This VCA circuit is designed to operate from a ±12 volt dual power supply.

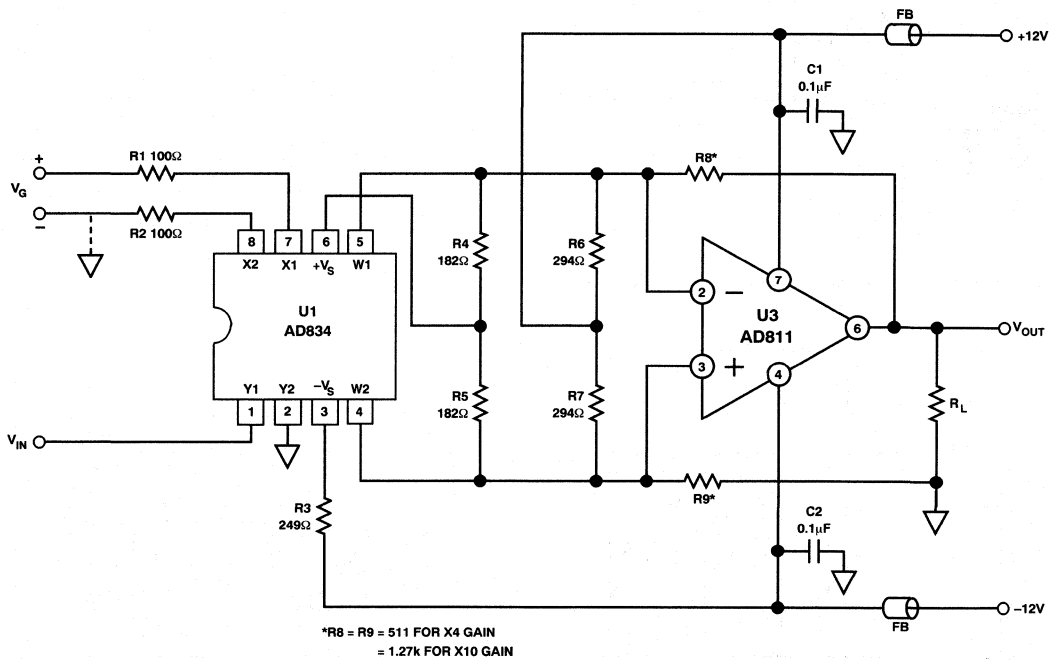


Figure 40. An 80 MHz Voltage-Controlled Amplifier

A Video Keyer Circuit

By using two AD834 multipliers, an AD811, and a 1 V dc source, a special form of a two-input VCA circuit called a video keyer can be assembled. "Keying" is the term used in reference to blending two or more video sources under the control of a third signal or signals to create such special effects as dissolves and overlays. The circuit shown in Figure 41 is a two-input keyer, with video inputs V_A and V_B, and a control input V_G. The transfer function (with V_{OUT} at the load) is given by:

$$V_{OUT} = G\,V_A + (1-G)\,V_B$$

where G is a dimensionless variable (actually, just the gain of the "A" signal path) that ranges from 0 when V_G = 0, to 1 when V_G = +1 V. Thus, V_{OUT} varies continuously between V_A and V_B as G varies from 0 to 1.

Circuit operation is straightforward. Consider first the signal path through U1, which handles video input V_A. Its gain is clearly zero when V_G = 0 and the scaling we have chosen ensures that it is unity when V_G = +1 V; this takes care of the first term of the transfer function. On the other hand, the V_G input to U2 is taken to the inverting input X2 while X1 is biased at an accurate +1 V. Thus, when V_G = 0, the response to video input V_B is already at its full-scale value of unity, whereas when V_G = +1 V, the differential input X1–X2 is zero. This generates the second term.

The bias currents required at the output of the multipliers are provided by R8 and R9. A dc-level-shifting network comprising R10/R12 and R11/R13 ensures that the input nodes of the AD811 are positioned at a voltage within its common-mode range. At high frequencies C1 and C2 bypass R10 and R11 respectively. R14 is included to lower the HF loop gain, and is needed because the voltage-to-current conversion in the AD834s, via the Y2 inputs, results in an effective value of the feedback resistance of 250 Ω; this is only about half the value required for optimum flatness in the AD811's response. (Note that this resistance is unaffected by G: when G = 1, all the feedback is via U1, while when G = 0 it is all via U2). R14 reduces the fractional amount of output current from the multipliers into the current-summing inverting input of the AD811, by sharing it with R8. This resistor can be used to adjust the bandwidth and damping factor to best suit the application.

To generate the 1 V dc needed for the "1–G" term an AD589 reference supplies 1.225 V ± 25 mV to a voltage divider consisting of resistors R2 through R4. Potentiometer R3 should be adjusted to provide exactly +1 V at the X1 input.

In this case, we have shown an arrangement using dual supplies of ±5 V for both the AD834 and the AD811. Also, the overall gain in this case is arranged to be unity at the load, when it is driven from a reverse-terminated 75 Ω line. This means that the "dual VCA" has to operate at a maximum gain of 2, rather

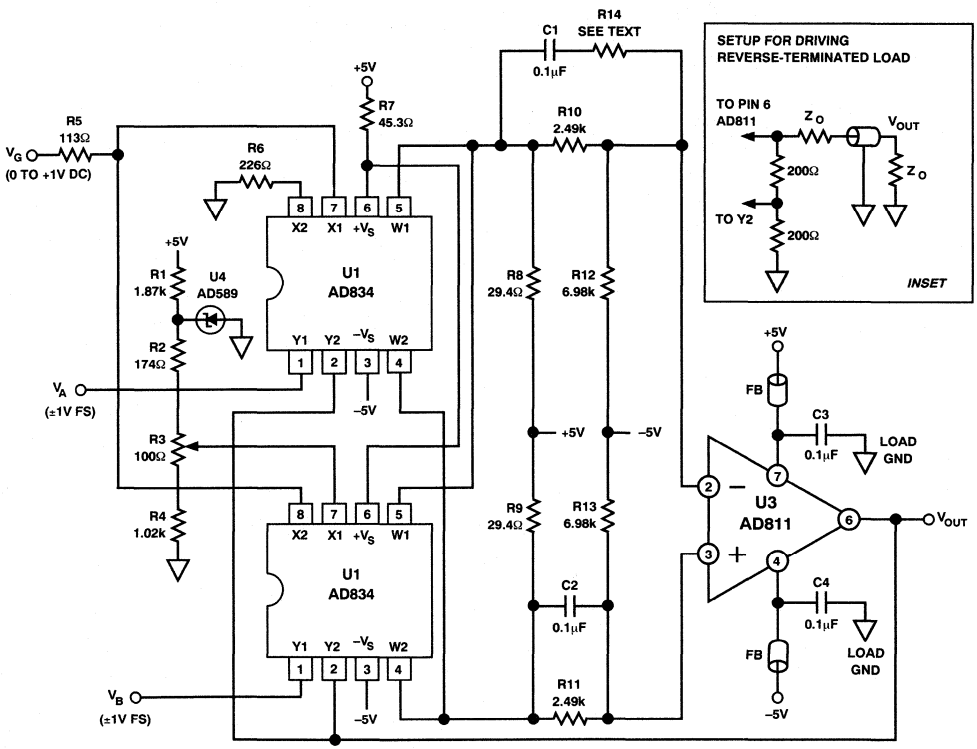


Figure 41. A Practical Video Keyer Circuit

than 4 as in the VCA circuit of Figure 40. However, this cannot be achieved by lowering the feedback resistor, since below a critical value (not much less than 500 Ω) the AD811's peaking may be unacceptable. This is because the dominant pole in the open-loop ac response of a current-feedback amplifier is controlled by this feedback resistor. It would be possible to operate at a gain of X4 and then attenuate the signal at the output. Instead, we have chosen to attenuate the signals by 6 dB at the input to the AD811; this is the function of R8 through R11.

Figure 42 is a plot of the ac response of the feedback keyer, when driving a reverse terminated 50 Ω cable. Output noise and adjacent channel feedthrough, with either channel fully off and the other fully on, is about −50 dB to 10 MHz. The feedthrough at 100 MHz is limited primarily by board layout. For V_G = +1 V, the −3 dB bandwidth is 15 MHz when using a 137 Ω resistor for R14 and 70 MHz with R14 = 49.9 Ω. For further information regarding the design and operation of the VCA and video keyer circuits, refer to the application note "Video VCA's and Keyers Using the AD834 & AD811" by Brunner, Clarke, and Gilbert, available FREE from Analog Devices.

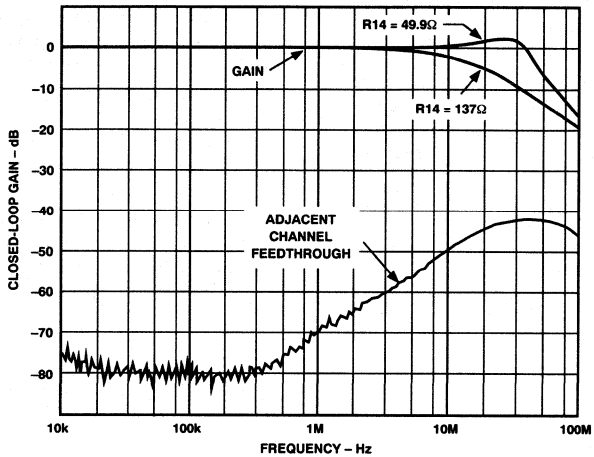


Figure 42. A Plot of the AC Response of the Video Keyer

High Speed, Low Power General Purpose Amplifier

AD817

FEATURES

High Speed
- 50 MHz Unity Gain Bandwidth
- 300 V/μs Slew Rate
- 120 ns Settling Time to 0.1% (V_O = 10 V Step)

Low Power
- 7.5 mA max Power Supply Current

Easy to Use
- Drives Heavy Capacitive Loads
- 50 mA Output Current
- Specified for ±5 V and ±15 V Operation
- ±3.0 V Output Swing into a 150 Ω Load (V_S = ±5 V)

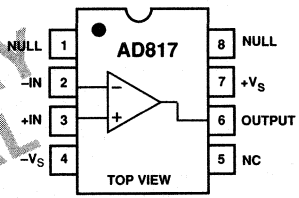
Excellent DC Performance
- 1.0 mV Input Offset Voltage

APPLICATIONS

Unity Gain ADC/DAC Buffer
Cable Drivers
Copiers, Fax, Scanners and Cameras
Video Line Driver
Active Filters

CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP (N)
and SOIC (R) Packages

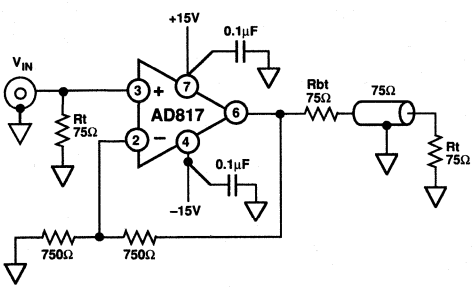


PRELIMINARY TECHNICAL DATA

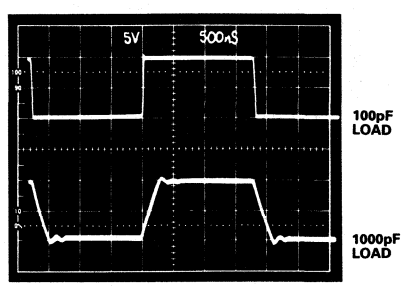
PRODUCT DESCRIPTION

The AD817 is a general purpose, high speed voltage feedback op amp. It is ideal for use in applications which require unity gain stability and high output drive capability, such as buffering and cable driving. The 50 MHz bandwidth and 300 V/μs slew rate make the AD817 useful in many high speed applications including: video, CATV, copiers, scanners and fax machines. The AD817 features high output current drive capability of 50 mA, and is able to drive heavy capacitive loads. With a low power supply current of 7.5 mA max, the AD817 is a true general purpose operational amplifier. The AD817 is ideal for power sensitive applications such as video cameras and portable instrumentation. The AD817 can operate from ±5 V supplies while still achieving 35 MHz of bandwidth. Furthermore, the AD817 is fully specified from ±5 V to ±15 V power supplies.

The AD817 excels as an ADC/DAC buffer or active filter in data acquisition systems and achieves a settling time of 120 ns to 0.1%, with a low input offset voltage of 1 mV max. The AD817 is available in small 8-pin plastic mini-DIP and SOIC packages.



The AD817 as a Video Line Driver



The AD817 Driving Capacitive Loads

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD817—SPECIFICATIONS (@ T_A = + 25°C, unless otherwise noted)

Parameter	Conditions	V_S	AD817A Min	AD817A Typ	AD817A Max	Units
DYNAMIC PERFORMANCE						
Unity Gain Bandwidth		±5 V		35		MHz
		±15 V		50		MHz
Full Power Bandwidth[1]	V_O = 5 V p–p					
	R_L = 500 Ω	±5 V		12.7		MHz
	V_O = 20 V p–p					
	R_L = 1 kΩ	±15 V		4.7		MHz
Slew Rate[2]	R_{LOAD} = 1 kΩ	±5 V		200		V/μs
		±15 V	225	300		V/μs
Settling Time						
to 0.1%	−2.5 V to +2.5 V	±5 V		65		ns
	10 V Step, A_V = −1	±15 V		65		ns
to 0.01%	−2.5 V to +2.5 V	±5 V		120		ns
	10 V Step, A_V = −1	±15 V		140		ns
Phase Margin	C_{LOAD} = 10 pF	±15 V				
	R_{LOAD} = 1 kΩ			50		Degree
Differential Gain (Rl = 150 Ω)	f ≈ 4.4 MHz	±15 V		0.06		%
Differential Phase (Rl = 150 Ω)	f ≈ 4.4 MHz	±15 V		0.11		Degrees
INPUT OFFSET VOLTAGE[3]						
		±5 V, ±15 V		0.5	1	mV
	T_{MIN} to T_{MAX}				4	mV
Offset Drift				15		μV/°C
INPUT BIAS CURRENT		±5 V, ±15 V		3.3	6.6	μA
	T_{MIN} to T_{MAX}				10	μA
INPUT OFFSET CURRENT		±5 V, ±15 V		50	300	nA
	T_{MIN} to T_{MAX}				500	nA
Offset Current Drift				0.3		nA/°C
OPEN-LOOP GAIN	V_O = ±2.5 V	±5 V				
	R_{LOAD} = 500 Ω		2	3.5		V/mV
	T_{MIN} to T_{MAX}		1			V/mV
	R_{LOAD} = 150 Ω			2.0		V/mV
	V_{OUT} = ±10 V	±15 V				
	R_{LOAD} = 1 kΩ		3	5.5		V/mV
	T_{MIN} to T_{MAX}		1.5			V/mV
COMMON-MODE REJECTION	V_{CM} = ±2.5 V	±5	78	95		dB
	V_{CM} = ±12 V	±15 V	78	95		dB
POWER SUPPLY REJECTION	V_S = ±5 V to ±15 V		75	86		dB
	T_{MIN} to T_{MAX}		72			dB
INPUT VOLTAGE NOISE	f = 10 kHz	±15 V		15		nV/√Hz
INPUT CURRENT NOISE	f = 10 kHz	±15 V		1.5		pA/√Hz
INPUT COMMON-MODE VOLTAGE RANGE		±5 V		+4.3		V
				−3.4		V
		±15 V		+14.3		V
				−13.4		V
OUTPUT VOLTAGE SWING						
	R_{LOAD} = 500 Ω	±5 V	3.0			±V
	R_{LOAD} = 150 Ω	±5 V	3.0			±V
	R_{LOAD} = 1 kΩ	±15 V	12			±V
	R_{LOAD} = 500 Ω	±15 V	10			±V
Output Current		±15 V	30			mA
Short Circuit Current		±15 V		60		mA
INPUT RESISTANCE				300		kΩ

PRELIMINARY TECHNICAL DATA

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Parameter	Conditions	V_S	AD817A Min	AD817A Typ	AD817A Max	Units
INPUT CAPACITANCE				1.5		pF
OUTPUT RESISTANCE	Open Loop			10		Ω
POWER SUPPLY						
Operating Range			±4.5		±18	V
Quiescent Current		±5 V		4.8	6.5	mA
	T_{MIN} to T_{MAX}				7.5	mA
		±15 V		6.0	7.5	mA
	T_{MIN} to T_{MAX}				8.0	mA

NOTES
[1]Full power bandwidth = slew rate/2π V_{PEAK}.
[2]Slew rate is measured on rising edge.
[3]Input offset voltage specifications are guaranteed after 5 minutes @ T_A = +25°C.
Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
Plastic DIP (N) . . . . . 1.3 Watts
Small Outline (R) . . . . . 0.9 Watts
Input Voltage (Common Mode) . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±6
Storage Temperature Range (N, R) . . . . . −65°C to +125°C
Operating Temperature Range
AD817A . . . . . −40°C to +85°C
Lead Temperature Range (Soldering 10 seconds) . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Pin Plastic DIP Package: θ_{JA} = 95°C/Watt
8-Pin SOIC Package: θ_{JA} = 155°C/Watt

ORDERING GUIDE

Model	Temperature Range	Package Description*
AD817AN	−40°C to +85°C	8-Pin Plastic DIP
AD817AR	−40°C to +85°C	8-Pin Plastic SOIC

*For outline information see Package Information section.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Single Supply, Precision, Low Power FET-Input Op Amps

AD820/AD822

FEATURES

TRUE SINGLE SUPPLY OPERATION
- Output Swings "Rail to Rail"
- Input Voltage Range Includes Ground

EASY TO USE
- Drives Heavy Capacitive and Resistive Loads (Output Current of 20 mA min)
- Low Power of 700 μA max per Amplifier
- Wide Unity Gain Bandwidth: 2 MHz
- High Slew Rate of 3.5 V/μs
- Single and Dual Supply Capability

EXCELLENT DC PERFORMANCE
- 250 μV max Input Offset Voltage
- 5.0 V/°C, max Offset Voltage Drift
- 5 pA, max Input Bias Current

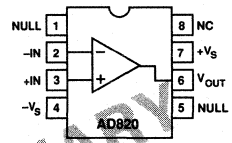
Low Noise
- 12.5 nV/$\sqrt{Hz}$ @ 1 kHz

APPLICATIONS

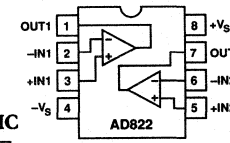
Battery Powered Precision Instrumentation
Strain Gage Signal Conditioners
Thermocouple Amplifiers
Instrumentation Amplifiers
4–20mA Current Transmitters
12- and 14-Bit Data Acquisition Systems
I-to-V Converters and Preamps
Medical Instrumentation – Patient Monitors

FUNCTIONAL BLOCK DIAGRAMS

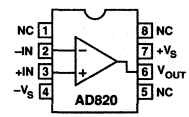
8-Pin Plastic Mini-DIP & Cerdip



8-Pin Plastic, Cerdip & SOIC Packages



8-Pin SOIC



PRELIMINARY TECHNICAL DATA

Low input offset voltage (250 μV max), low offset voltage drift (2 μV/°C), low input bias currents (<10 pA) and low supply currents (700 μA max) provide true DC precision at low power operating conditions. Coupled with a unity gain bandwidth of 2 MHz and 3.75 V/μs, the AD820 and AD822 offer the best combination of AC and DC specifications to the single supply op amp user. Performance in 12- to 14-bit applications is ensured with the low noise (12.5 nV/$\sqrt{Hz}$ @ 1 kHz), high open-loop gain (10^3 V/mV) and 4 μs settling time to 0.01% of final value.

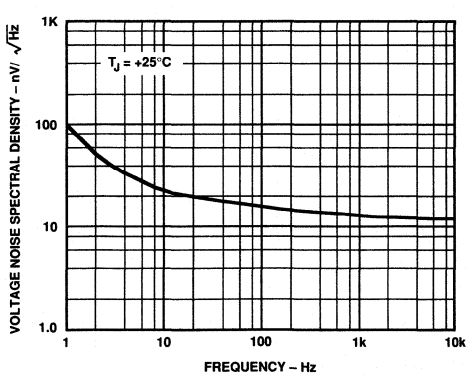
The AD820 and AD822 are an excellent choice for battery-powered precision instrumentation applications—wherein the extended input and output ranges and low power consumption along with output drive of 20 mA minimum and 500 pF cap load dive afford versatility in these applications.

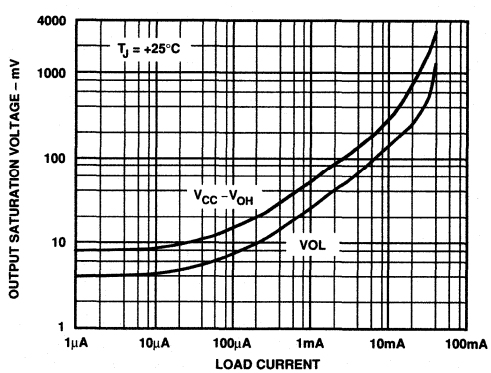
The AD820 and AD822 are available in three performance grades. The A and B grades are rated over the industrial temperature range of −40°C to +85°C. The S grade is rated over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

The AD820 and AD822 are offered in three varieties of 8-pin package: plastic DIP, hermetic cerdip and surface mount (SOIC).

PRODUCT DESCRIPTION

The AD820 and AD822 are precision, low power FET input monolithic op amps that can operate from a single supply of +4.0 V to +36 V, or dual supplies of ±2.0 V to ±18 V with no tradeoffs. They have true single supply capability with input voltage range including the negative rail, allowing the AD820 and AD822 to accommodate input signals down to ground in the single supply mode. Their output voltage swing extends to within 10 mV of each rail providing the maximum output dynamic range to the user.





This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD820/AD822—SPECIFICATIONS (@ T_A = +25°C, V_{CM} = 2.5 V, V_S = +5 V and V_{CM} = 0 V, V_S = ±15 V dc, unless otherwise noted)

Model	Conditions	AD820A/AD822A Min	Typ	Max	AD820B/AD822B Min	Typ	Max	AD820S/AD822S Min	Typ	Max	Unit
Input Offset Voltage											
Initial Offset			0.3	1		0.2	0.5		0.3	1	mV
Offset Drift			2	10		2	5		2	10	μV/°C
Input Bias Current			2	10		2	5		2	10	pA
Offset Current			0.4			0.4			0.4		pA
Open Loop Gain	V_O = +10 V, R_L = ∞		10000			10000			10000		V/mV
	V_O = +10 V, R_L = 10k		1000			1000			1000		V/mV
	V_O = +10 V, R_L = 1k		100			100			100		V/mV
Input Impedance											
Differential			3×10^{12}‖4			3×10^{12}‖4			3×10^{12}‖4		Ω‖pF
Common Mode			3×10^{12}‖4			3×10^{12}‖4			3×10^{12}‖4		Ω‖pF
Input Voltage Range											
Differential	V_S = +5 V		+3.5			+3.5			+3.5		V
Differential	V_S = ±15 V		±20			±20			±20		V
Common-Mode Voltage	V_S = +5 V		0, 4			0, 4			0, 4		V
Common-Mode Voltage	V_S = ±15 V		−15, +14			−15, +14			−15, +14		V
Common-Mode Rejection Ratio	V_{CM} = V_{CC}−2 V		80			80			80		dB
	V_{CM} = V_{CC}−3 V		90			90			90		dB
Output Characteristics											
Output Voltage Swing[1]											
No Load	V_{OL} − V_{EE}		4			4			4		mV
	V_{CC} − V_{OH}		8			8			8		mV
I_{SINK} = 2 mA	V_{OL} − V_{EE}		40			40			40		mV
I_{SOURCE} = 2 mA	V_{CC} − V_{OH}		80			80			80		mV
I_{SINK} = 20 mA	V_{OL} − V_{EE}		210			210			210		mV
I_{SOURCE} = 20 mA	V_{CC} − V_{OH}		800			800			800		mV
Output Current		20	30		20	30		20	30		mV
Short Circuit Current			50			50			50		mA
Cap. Load Drive Capability			500			500			500		pF
Input Voltage Noise	0.1 Hz to 10 Hz		2			2			2		μV p–p
	f = 10 Hz		25			25			25		nV/√Hz
	f = 100 Hz		18			18			18		nV/√Hz
	f = 1 kHz		12.5			12.5			12.5		nV/√Hz
	f = 10 kHz		12			12			12		nV/√Hz
Input Current Noise	0.1 Hz to 10 Hz		15			15			15		fA p–p
	f = 1 kHz		0.8			0.8			0.8		fA/√Hz
Frequency Response											
Unity Gain, Small Signal			2			2			2		MHz
Full Power Response	V_S = +5 V, V_{IN} p–p = 3 V		60			60			60		kHz
Full Power Response	V_S = ±15 V, V_{IN} p–p = 20 V		60			60			60		kHz
Slew Rate, Unity Gain			3.5			3.5			3.5		V/μs

PRELIMINARY TECHNICAL DATA

SPECIFICATIONS (@ T_A = +25°C, V_{CM} = 0 V, +5 V and ±15 V dc, unless otherwise noted)

Model	Conditions	AD820A/AD822A Min	Typ	Max	AD820B/AD822B Min	Typ	Max	AD820S/AD822S Min	Typ	Max	Units
Settling Time to 0.01%	V_S = +5 V, V_{IN} p–p = 3 V		2			2			2		μs
Settling Time to 0.01%	V_S = ±15 V, V_{IN} p–p = 10 V		5			5			5		μs
Power Supply	V_S = +5 V										
Rated Performance			+5			+5			+5		V
Operating Range		+4		+36	+4		+36	+4		+36	V
Quiescent Current			670	700		670	700		670	700	μA
Power Supply Rejection			90			90			90		dB
Power Supply	V_S = ±15 V										
Rated Performance			±15			±15			±15		V
Operating Range		±2		±18	±2		±18	±2		±18	V
Quiescent Current			710	750		710	750		710	750	μA
Power Supply Rejection			90			90			90		dB

NOTE

[1]V_{OL}–V_{EE} is defined as the voltage difference the output node (V_{OUT}) and the amplifier's **negative** supply rail (V_{EE}). This specification defines the minimum attainable output voltage swing for the different loading conditions indicated. V_{CC} − V_{OH} is defined as the voltage difference between the output node (V_{OUT}) and the amplifier's **positive** supply rail (V_{CC}). This specification also defines the minimum attainable output voltage swing for the different loading conditions indicated.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

High Speed, Low Power Dual Op Amp

AD827

FEATURES

HIGH SPEED
50 MHz Unity Gain Stable Operation
300 V/μs Slew Rate
120 ns Settling Time
Drives Unlimited Capacitive Loads

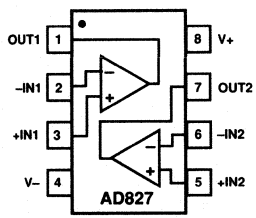
EXCELLENT VIDEO PERFORMANCE
0.04% Differential Gain @ 4.4 MHz
0.19° Differential Phase @ 4.4 MHz

GOOD DC PERFORMANCE
2 mV max Input Offset Voltage
15 μV/°C Input Offset Voltage Drift
Available in Tape and Reel in Accordance with EIA-481A Standard

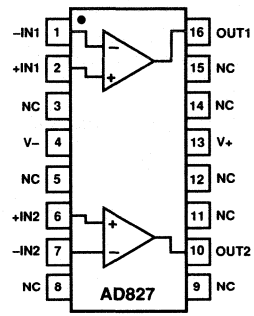
LOW POWER
Only 10 mA Total Supply Current for Both Amplifiers ±5 V to ±15 V Supplies

CONNECTION DIAGRAMS

8-Pin Plastic (N) and Cerdip (Q) Packages

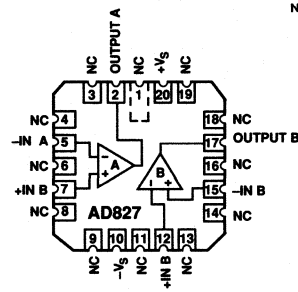


16-Pin Small Outline (R) Package



NC = NO CONNECT

20-Pin LCC (E) Package



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD827 is a dual version of Analog Devices' industry-standard AD847 op amp. Like the AD847, it provides high speed, low power performance at low cost. The AD827 achieves a 300 V/μs slew rate and 50 MHz unity-gain bandwidth while consuming only 100 mW when operating from ±5 volt power supplies. Performance is specified for operation using ±5 V to ±15 V power supplies.

The AD827 offers an open-loop gain of 3,500 V/V into 500 Ω loads. It also features a low input voltage noise of 15 nV/$\sqrt{\text{Hz}}$, and a low input offset voltage of 2 mV maximum. Common-mode rejection ratio is a minimum of 80 dB. Power supply rejection ratio is maintained at better than 20 dB with input frequencies as high as 1 MHz, thus minimizing noise feedthrough from switching power supplies.

The AD827 is also ideal for use in demanding video applications, driving coaxial cables with less than 0.04% differential gain and 0.19° differential phase errors for 643 mV p–p into a 75 Ω reverse terminated cable.

The AD827 is also useful in multichannel, high speed data conversion systems where its fast (120 ns to 0.1%) settling time is of importance. In such applications, the AD827 serves as an input buffer for 8-bit to 10-bit A/D converters and as an output amplifier for high speed D/A converters.

APPLICATION HIGHLIGHTS

1. Performance is fully specified for operation using ±5 V to ±15 V supplies.
2. A 0.04% differential gain and 0.19° differential phase error at the 4.4 MHz color subcarrier frequency, together with its low cost, make it ideal for many video applications.
3. The AD827 can drive unlimited capacitive loads, while its 30 mA output current allows 50 Ω and 75 Ω reverse-terminated loads to be driven.
4. The AD827's 50 MHz unity-gain bandwidth makes it an ideal candidate for multistage active filters.
5. The AD827 is available in 8-pin plastic mini-DIP and cerdip, 20-pin LCC, and 16-pin SOIC packages. Chips and MIL-STD-883B processing are also available.

AD827—SPECIFICATIONS (@ T_A = +25°C, unless otherwise noted)

Model	Conditions	V_S	AD827J Min	AD827J Typ	AD827J Max	AD827A/S Min	AD827A/S Typ	AD827A/S Max	Units
DC PERFORMANCE									
Input Offset Voltage[1]		±5 V		0.5	2		0.3	2	mV
	T_{min} to T_{max}				3.5			4	mV
		±15 V			4			4	mV
	T_{min} to T_{max}				6			6	mV
Offset Voltage Drift		±5 V to ±15 V		15			15		µV/°C
Input Bias Current		±5 V to ±15 V		3.3	7		3.3	7	µA
	T_{min} to T_{max}				8.2			9.5	µA
Input Offset Current		±5 V to ±15 V		50	300		50	300	nA
	T_{min} to T_{max}				400			400	nA
Offset Current Drift		±5 V to ±15 V		0.5			0.5		nA/°C
Common-Mode Rejection Ratio	V_{CM} = ±2.5 V	±5 V	78	95		80	95		dB
	V_{CM} = ±12 V	±15 V	78	95		80	95		dB
	T_{min} to T_{max}	±5 V to ±15 V	75			75			dB
Power Supply Rejection Ratio		±5 V to ±15 V	75	86		75	86		dB
	T_{min} to T_{max}		72			72			dB
Open-Loop Gain									
	V_O = ±2.5 V	±5 V							
	R_{LOAD} = 500 Ω		2	3.5		2	3.5		V/mV
	T_{min} to T_{max}		1			1			V/mV
	R_{LOAD} = 150 Ω			1.6			1.6		V/mV
	V_{OUT} = ±10 V	±15 V							
	R_{LOAD} = 1 kΩ		3	5.5		3	5.5		V/mV
	T_{min} to T_{max}		1.5			1.5			V/mV
MATCHING CHARACTERISTICS									
Input Offset Voltage		±5 V		0.4			0.2		mV
Crosstalk	f = 5 MHz	±5 V		85			85		dB
DYNAMIC PERFORMANCE									
Unity-Gain Bandwidth		±5 V		35			35		MHz
		±15 V		50			50		MHz
Full Power Bandwidth[2]	V_O = 5 V p-p,								
	R_{LOAD} = 500 Ω	±5 V		12.7			12.7		MHz
	V_O = 20 V p-p,								
	R_{LOAD} = 1 kΩ	±15 V		4.7			4.7		MHz
Slew Rate[3]	R_{LOAD} = 500 Ω	±5 V		200			200		V/µs
	R_{LOAD} = 1 kΩ	±15 V		300			300		V/µs
Settling Time to 0.1%	A_V = −1								
	−2.5 V to +2.5 V	±5 V		65			65		ns
	−5 V to +5 V	±15 V		120			120		ns
Phase Margin	C_{LOAD} = 10 pF	±15 V							
	R_{LOAD} = 1 kΩ			50			50		Degrees
Differential Gain Error	f = 4.4 MHz	±15 V		0.04			0.04		%
Differential Phase Error	f = 4.4 MHz	±15 V		0.19			0.19		Degrees
Input Voltage Noise	f = 10 kHz	±15 V		15			15		nV/√Hz
Input Current Noise	f = 10 kHz	±15 V		1.5			1.5		pA/√Hz
Input Common-Mode Voltage Range		±5 V		+4.3			+4.3		V
				−3.4			−3.4		V
		±15 V		+14.3			+14.3		V
				−13.4			−13.4		V
Output Voltage Swing	R_{LOAD} = 500 Ω	±5 V	3.0	3.6		3.0	3.6		±V
	R_{LOAD} = 150 Ω	±5 V	2.5	3.0		2.5	3.0		±V
	R_{LOAD} = 1 kΩ	±15 V	12	13.3		12	13.3		±V
	R_{LOAD} = 500 Ω	±15 V	10	12.2		10	12.2		±V
Short-Circuit Current Limit		±5 V to ±15 V		32			32		mA
INPUT CHARACTERISTICS									
Input Resistance				300			300		kΩ
Input Capacitance				1.5			1.5		pF
OUTPUT RESISTANCE	Open Loop			15			15		Ω

Model	Conditions	V_S	AD827J Min	AD827J Typ	AD827J Max	AD827A/S Min	AD827A/S Typ	AD827A/S Max	Units
POWER SUPPLY									
Operating Range			±4.5		±18	±4.5		±18	V
Quiescent Current		±5 V		10	13		10	13	mA
	T_{min} to T_{max}				16			16.5/17.5	mA
		±15 V		10.5	13.5		10.5	13.5	mA
	T_{min} to T_{max}				16.5			17/18	mA
TRANSISTOR COUNT				92			92		

NOTES
[1]Offset voltage for the AD827 is guaranteed after power is applied and the device is fully warmed up. All other specifications are measured using high speed test equipment, approximately 1 second after power is applied.
[2]Full Power Bandwidth = Slew Rate/2π V_{PEAK}.
[3]Gain = +1, rising edge.
All min and max specifications are guaranteed.
Specifications subject to change without notice.

2

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
Plastic (N) Package (Derate at 10 mW/°C) . . . . . 1.5 W
Cerdip (Q) Package (Derate at 8.7 mW/°C) . . . . . 1.3 W
Small Outline (R) Package (Derate at 10 mW/°C) . . . . 1.5 W
LCC (E) Package (Derate at 6.7 mW/°C) . . . . . 1.0 W
Input Common Mode Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . 6 V
Output Short Circuit Duration[3] . . . . . Indefinite
Storage Temperature Range (N, R) . . . . . −65°C to +125°C
Storage Temperature Range (Q) . . . . . −65°C to +150°C
Operating Temperature Range
AD827J . . . . . 0 to +70°C
AD827A . . . . . −40°C to +85°C
AD827S . . . . . −55°C to +125°C
Lead Temperature Range
(Soldering to 60 sec) . . . . . 300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.
[2]Maximum internal power dissipation is specified so that T_j does not exceed +175°C at an ambient temperature of +25°C.
Thermal Characteristics:
Mini-DIP: θ_{JA} = 100°C/Watt; θ_{JC} = 33°C/Watt
Cerdip: θ_{JA} = 110°C/Watt; θ_{JC} = 30°C/Watt
16-Pin Small Outline Package: θ_{JA} = 100°C/Watt
20-Pin LCC: θ_{JA} = 150°C/Watt; θ_{JC} = 35°C/Watt
[3]Indefinite short circuit duration is only permissible as long as the absolute maximum power rating is not exceeded.

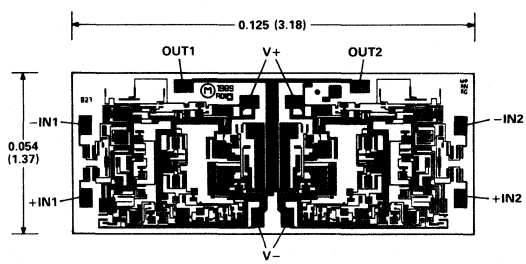
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD827JN	0 to +70°C	8-Pin Plastic DIP	N-8
AD827JR	0 to +70°C	16-Pin Plastic SO	R-16
AD827AQ	−40°C to +85°C	8-Pin Cerdip	Q-8
AD827SQ	−55°C to +125°C	8-Pin Cerdip	Q-8
AD827SQ/883B	−55°C to +125°C	8-Pin Cerdip	Q-8
AD827SE/883B	−55°C to +125°C	20-Pin LCC	E-20A
AD827JR-REEL	0 to +70°C	Tape & Reel	
AD827JChips	0 to +70°C	Die	
AD827SChips	−55°C to +125°C	Die	

*For outline information see Package Information section.

METALIZATION PHOTOGRAPHY

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).
Substrate is connected to V+.



AD827—Typical Characteristics (@ +25°C & ±15 V, unless otherwise noted)

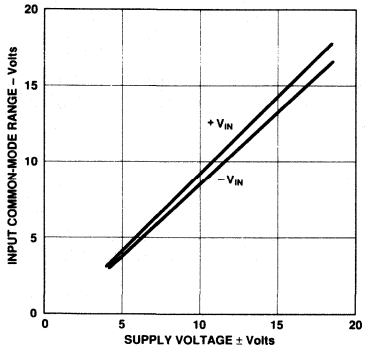


Figure 1. Input Common-Mode Range vs. Supply Voltage

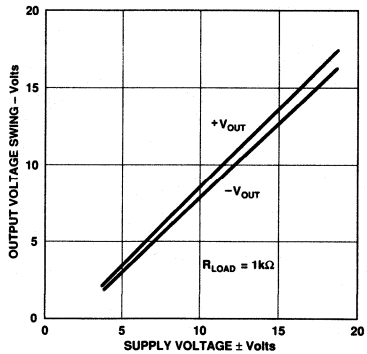


Figure 2. Output Voltage Swing vs. Supply Voltage

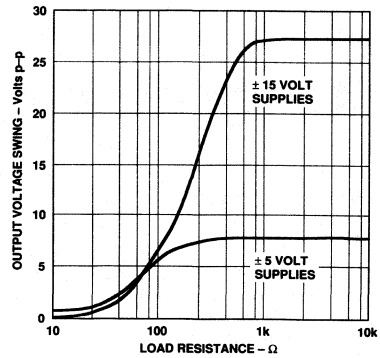


Figure 3. Output Voltage Swing vs. Load Resistance

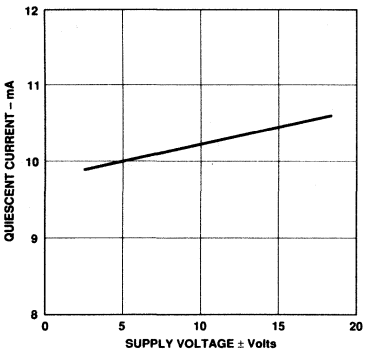


Figure 4. Quiescent Current vs. Supply Voltage

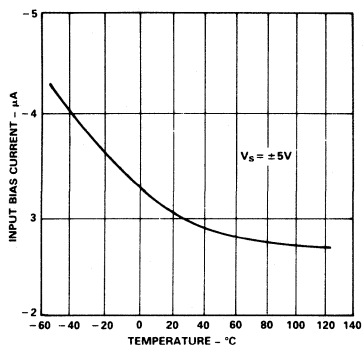


Figure 5. Input Bias Current vs. Temperature

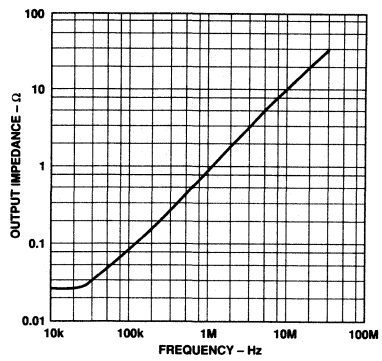


Figure 6. Closed-Loop Output Impedance vs. Frequency, Gain = +1

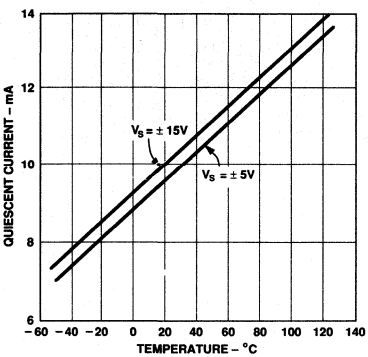


Figure 7. Quiescent Current vs. Temperature

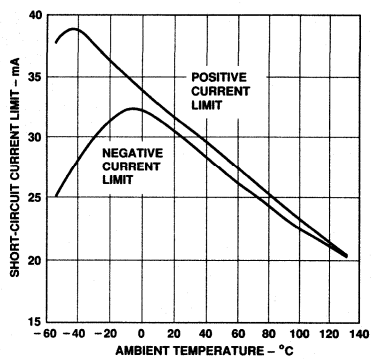


Figure 8. Short-Circuit Current Limit vs. Temperature

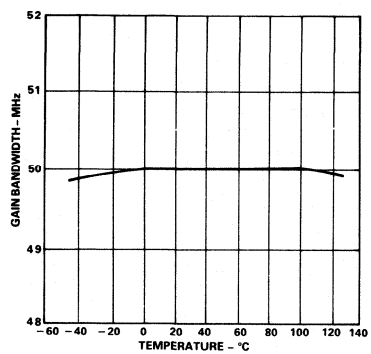


Figure 9. Gain Bandwidth vs. Temperature

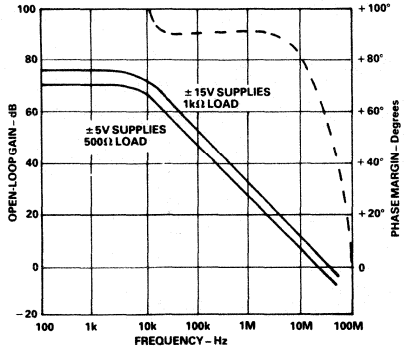


Figure 10. Open-Loop Gain and Phase Margin vs. Frequency

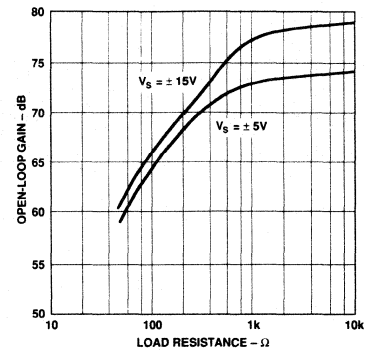


Figure 11. Open-Loop Gain vs. Load Resistance

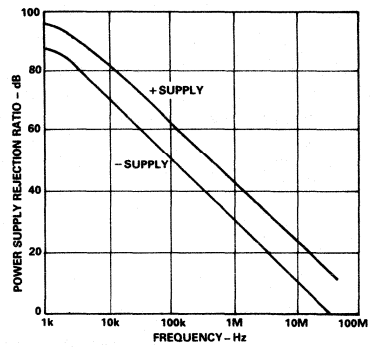


Figure 12. Power Supply Rejection Ratio vs. Frequency

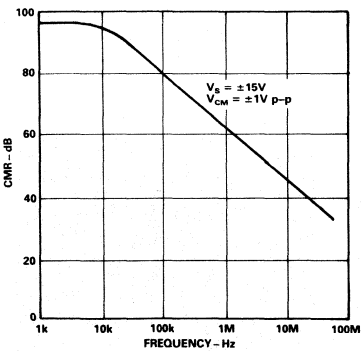


Figure 13. Common-Mode Rejection Ratio vs. Frequency

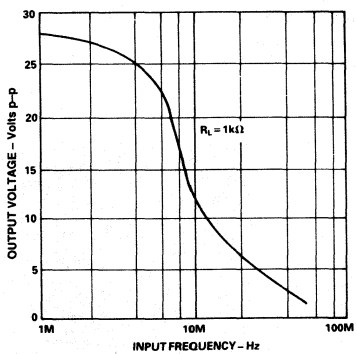


Figure 14. Large Signal Frequency Response

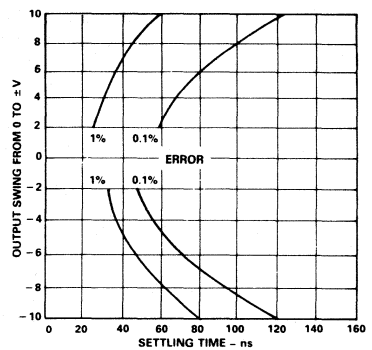


Figure 15. Output Swing and Error vs. Settling Time

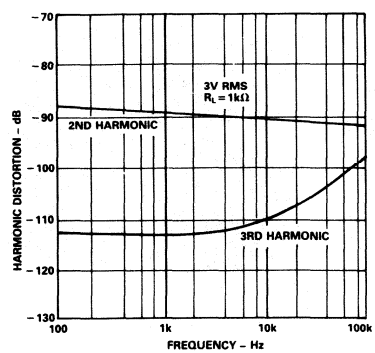


Figure 16. Harmonic Distortion vs. Frequency

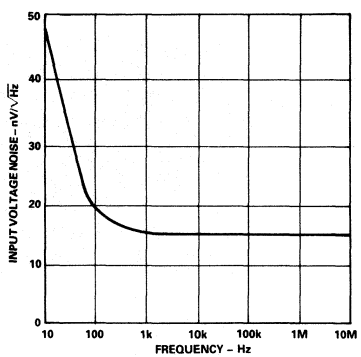


Figure 17. Input Voltage Noise Spectral Density

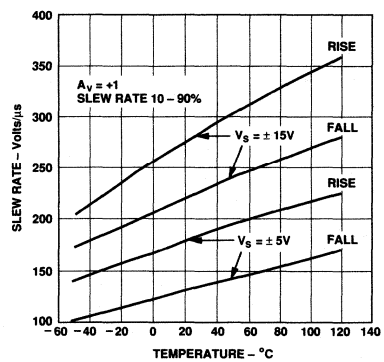


Figure 18. Slew Rate vs. Temperature

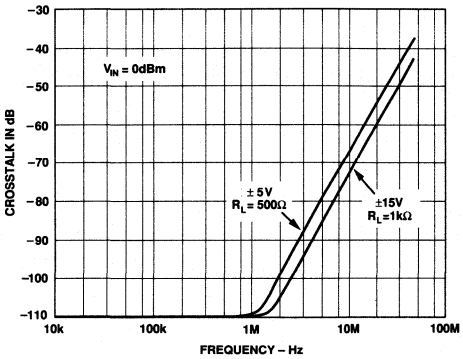


Figure 19. Crosstalk vs. Frequency

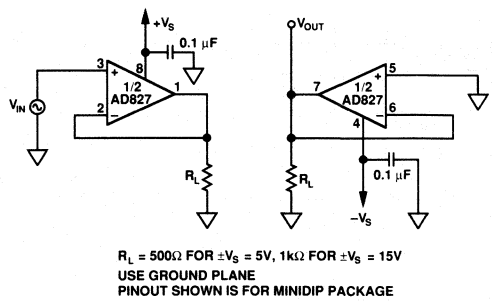


Figure 20. Crosstalk Test Circuit

INPUT PROTECTION PRECAUTIONS

An input resistor (resistor R_{IN} of Figure 21a) is recommended in circuits where the input common-mode voltage to the AD827 may exceed (on a transient basis) the positive supply voltage. This resistor provides protection for the input transistors by limiting the maximum current that can be forced into their bases.

For high performance circuits, it is recommended that a second resistor (R_B in Figures 21a and 22a) be used to reduce bias-current errors by matching the impedance at each input. This resistor reduces the error caused by offset voltages by more than an order of magnitude.

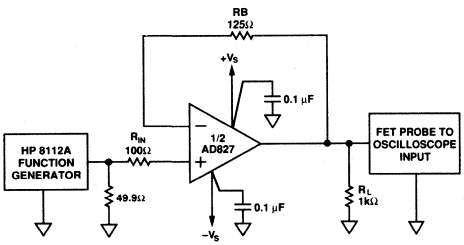


Figure 21a. Follower Connection

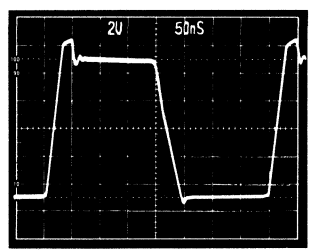


Figure 21b. Follower Large Signal Pulse Response

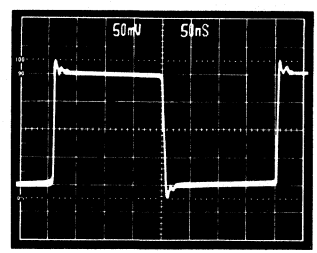


Figure 21c. Follower Small Signal Pulse Response

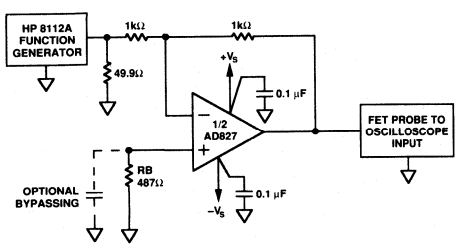


Figure 22a. Inverter Connection

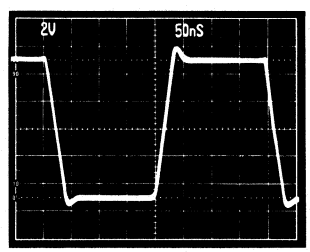


Figure 22b. Inverter Large Signal Pulse Response

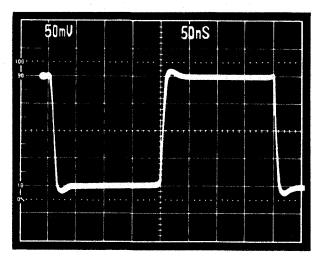


Figure 22c. Inverter Small Signal Pulse Response

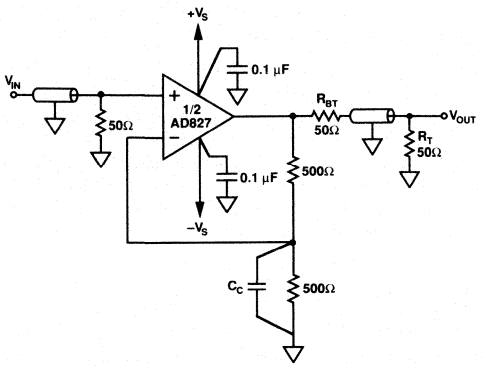


Figure 23. A Video Line Driver

VIDEO LINE DRIVER

The AD827 functions very well as a low cost, high speed line driver for either terminated or unterminated cables. Figure 23 shows the AD827 driving a doubly terminated cable in a follower configuration.

The termination resistor, R_T, (when equal to the cable's characteristic impedance) minimizes reflections from the far end of the cable. While operating from ±5 V supplies, the AD827 maintains a typical slew rate of 200 V/µs, which means it can drive a ±1 V, 30 MHz signal into a terminated cable.

Video Line Driver Performance Summary

V_{IN}*	V_{SUPPLY}	C_C	−3 dB B_W	Overshoot
0 dB or ±500 mV Step	±15	20 pF	23 MHz	4%
0 dB or ±500 mV Step	±15	15 pF	21 MHz	0%
0 dB or ±500 mV Step	±15	0 pF	13 MHz	0%
0 dB or ±500 mV Step	±5	20 pF	18 MHz	2%
0 dB or ±500 mV Step	±5	15 pF	16 MHz	0%
0 dB or ±500 mV Step	±5	0 pF	11 MHz	0%

NOTE
*−3 dB bandwidth numbers are for the 0 dBm signal input. Overshoot numbers are the percent overshoot of the 1 Volt step input.

Table I. Video Line Driver Performance Chart

A back-termination resistor (R_{BT}, also equal to the characteristic impedance of the cable) may be placed between the AD827 output and the cable input, in order to damp any reflected signals caused by a mismatch between R_T and the cable's characteristic impedance. This will result in a flatter frequency response, although this requires that the op amp supply ±2 V to the output in order to achieve a ±1 V swing at resistor R_T.

A HIGH SPEED 3 OP AMP INSTRUMENTATION AMPLIFIER CIRCUIT

The instrumentation amplifier circuit shown in Figure 24 can provide a range of gains. The chart of Table II details performance.

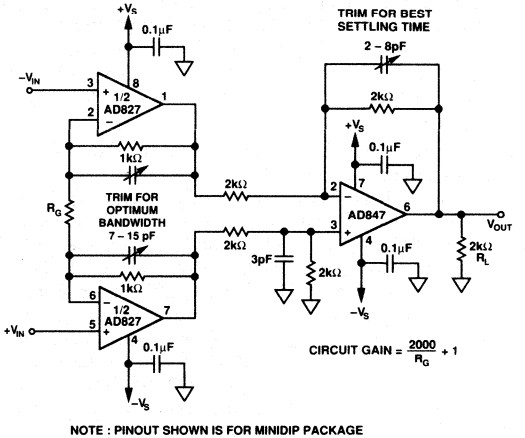


Figure 24. A High Bandwidth Three Op Amp Instrumentation Amplifier

Gain	R_G	Small Signal Bandwidth @ 1 V p–p Output
1	Open	16.1 MHz
2	2 k	14.7 MHz
10	226 Ω	4.9 MHz
100	20 Ω	660 kHz

Table II. Performance Specifications for the Three Op Amp Instrumentation Amplifier

A TWO-CHIP VOLTAGE-CONTROLLED AMPLIFIER (VCA) WITH EXPONENTIAL RESPONSE

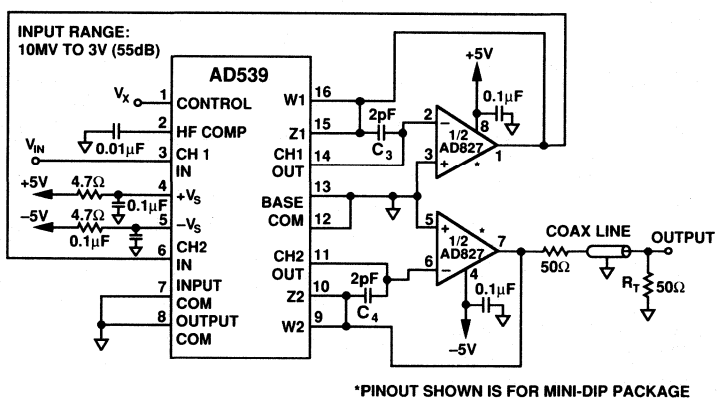
Voltage-controlled amplifiers are often used as building blocks in automatic gain control systems. Figure 25 shows a two-chip VCA built using the AD827 and the AD539, a dual, current-output multiplier. As configured, the circuit has its two multipliers connected in series. They could also be placed in parallel with an increase in bandwidth and a reduction in gain. The gain of the circuit is controlled by V_X, which can range from 0 to 3 V dc. Measurements show that this circuit easily supplies 2 V p–p into a 100 Ω load while operating from ±5 V supplies. The overall bandwidth of the circuit is approximately 7 MHz with 0.5 dB of peaking.

Each half of the AD827 serves as an I/V converter and converts the output current of one of the two multipliers in the AD539 into an output voltage. Each of the AD539's two multipliers contains two internal 6 kΩ feedback resistors; one is connected between the CH1 output and Z1, the other between the CH1 output and W1. Likewise, in the CH2 multiplier, one of the feedback resistors is connected between CH2 and Z2 and the other is connected between CH2 and Z2. In Figure 25, Z1 and W1 are tied together, as are Z2 and W2, providing a 3 kΩ feedback resistor for the op amp. The 2 pF capacitors connected between the AD539's W1 and CH1 and W2 and CH2 pins are in parallel with the feedback resistors and thus reduce peaking in the VCA's frequency response. Increasing the values of C3 and C4 can further reduce the peaking at the expense of reduced bandwidth. The 1.25 mA full-scale output current of the AD539 and the 3 kΩ feedback resistor set the full-scale output voltage of each multiplier at 3.25 V p–p.

Current limiting in the AD827 (typically 30 mA) limits the output voltage in this application to about 3 V p–p across a 100 Ω load. Driving a 50 Ω reverse-terminated load divides this value by two, limiting the maximum signal delivered to a 50 Ω load to about 1.5 V p–p, which suffices for video signal levels. The dynamic range of this circuit is approximately 55 dB and is primarily limited by feedthrough at low input levels and by the maximum output voltage at high levels.

Guidelines for Grounding and Bypassing

When designing practical high frequency circuits using the AD827, some special precautions are in order. Both short interconnection leads and a large ground plane are needed whenever possible to provide low resistance, low inductance circuit paths. One should remember to minimize the effects of capacitive coupling between circuits. Furthermore, IC sockets should be avoided. Feedback resistors should be of a low enough value that the time constant formed with stray circuit capacitances at the amplifier summing junction will not limit circuit performance. As a rule of thumb, use feedback resistor values that are less than 5 kΩ. If a larger resistor value is necessary, a small (<10 pF) feedback capacitor in parallel with the feedback resistor may be used. The use of 0.1 μF ceramic disc capacitors is recommended for bypassing the op amp's power supply leads.



$$V_{OUT} \text{ AT TERMINATION RESISTOR, } R_T = \frac{V_X^2 V_{IN}}{8V_2}$$

$$V_{OUT} \text{ AT PIN 8 OF AD827} = \frac{V_X^2 V_{IN}}{4V^2}$$

Figure 25. A Wide Range Voltage-Controlled Amplifier Circuit

ANALOG DEVICES

High Speed, Low Noise Video Op Amp

AD829

FEATURES

High Speed
- 120 MHz Bandwidth, Gain = −1
- 230 V/μs Slew Rate
- 90 ns Settling Time to 0.1%

Ideal for Video Applications
- 0.02% Differential Gain
- 0.04° Differential Phase

Low Noise
- 1.7 nV/$\sqrt{\text{Hz}}$ Input Voltage Noise
- 1.5 pA/$\sqrt{\text{Hz}}$ Input Current Noise

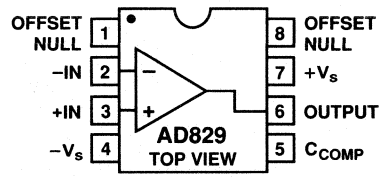
Excellent DC Precision
- 1 mV max Input Offset Voltage (Over Temp)
- 0.3 μV/°C Input Offset Drift

Flexible Operation
- Specified for ±5 V to ±15 V Operation
- ±3 V Output Swing into a 150 Ω Load
- External Compensation for Gains 1 to 20
- 5 mA Supply Current

Available in Tape and Reel in Accordance with EIA-481A Standard

CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP (N), Cerdip (Q) and SOIC (R) Packages



PRODUCT DESCRIPTION

The AD829 is a low noise (1.7 nV/$\sqrt{\text{Hz}}$), high speed op amp with custom compensation that provides the user with gains from ±1 to ±20 while maintaining a bandwidth greater than 50 MHz. The AD829's 0.04° differential phase and 0.02% differential gain performance at 3.58 MHz and 4.43 MHz, driving reverse-terminated 50 Ω or 75 Ω cables, makes it ideally suited for professional video applications. The AD829 achieves its 230 V/μs uncompensated slew rate and 750 MHz gain bandwidth product while requiring only 5 mA of current from the power supplies.

The AD829's external compensation pin gives it exceptional versatility. For example, compensation can be selected to optimize the bandwidth for a given load and power supply voltage. As a gain-of-two line driver, the −3 dB bandwidth can be increased to 95 MHz at the expense of 1 dB of peaking. In addition, the AD829's output can also be clamped at its external compensation pin.

The AD829 has excellent dc performance. It offers a minimum open-loop gain of 30 V/mV into loads as low as 500 Ω, low input voltage noise of 1.7 nV/$\sqrt{\text{Hz}}$, and a low input offset voltage of 1 mV maximum. Common-mode rejection and power supply rejection ratios are both 120 dB.

The AD829 is also useful in multichannel, high speed data conversion where its fast (90 ns to 0.1%) settling time is of importance. In such applications, the AD829 serves as an input buffer for 8-to-10-bit A/D converters and as an output I/V converter for high speed D/A converters.

The AD829 provides many of the same advantages that a transimpedance amplifier offers, while operating as a traditional voltage feedback amplifier. A bandwidth greater than 50 MHz can be maintained for a range of gains by changing the external compensation capacitor. The AD829 and the transimpedance amplifier are both unity gain stable and provide similar voltage noise performance (1.7 nV/$\sqrt{\text{Hz}}$). However, the current noise of the AD829 (1.5 pA/$\sqrt{\text{Hz}}$) is less than 10% of the noise of transimpedance amps. Furthermore, the inputs of the AD829 are symmetrical.

PRODUCT HIGHLIGHTS

1. Input voltage noise of 2 nV/$\sqrt{\text{Hz}}$, current noise of 1.5 pA/$\sqrt{\text{Hz}}$ and 50 MHz bandwidth, for gains of 1 to 20, make the AD829 an ideal preamp.
2. Differential phase error of 0.04° and a 0.02% differential gain error, at the 3.58 MHz NTSC and 4.43 MHz PAL and SECAM color subcarrier frequencies, make it an outstanding video performer for driving reverse-terminated 50 Ω and 75 Ω cables to ±1 V (at their terminated end).
3. The AD829 can drive heavy capacitive loads.
4. Performance is fully specified for operation from ±5 V to ±15 V supplies.
5. Available in plastic, cerdip, and small outline packages. Chips and MIL-STD-883B parts are also available.

AD829—SPECIFICATIONS (@ T_A = +25°C and V_S = ±15 V dc, unless otherwise noted)

Model	Conditions	V_S	AD829J Min	AD829J Typ	AD829J Max	AD829 A/S Min	AD829 A/S Typ	AD829 A/S Max	Units
INPUT OFFSET VOLTAGE		±5 V, ±15 V		0.2	1		0.1	0.5	mV
	T_{min} to T_{max}				1			0.5	mV
Offset Voltage Drift		±5 V, ±15 V		0.3			0.3		µV/°C
INPUT BIAS CURRENT		±5 V, ±15 V		3.3	7		3.3	7	µA
	T_{min} to T_{max}				8.2			9.5	µA
INPUT OFFSET CURRENT		±5 V, ±15 V		50	500		50	500	nA
	T_{min} to T_{max}				500			500	nA
Offset Current Drift		±5 V, ±15 V		0.5			0.5		nA/°C
OPEN-LOOP GAIN	V_O = ±2.5 V	±5 V							
	R_{LOAD} = 500 Ω		30	65		30	65		V/mV
	T_{min} to T_{max}		20			20			V/mV
	R_{LOAD} = 150 Ω			40			40		V/mV
	V_{OUT} = ±10 V	±15 V							
	R_{LOAD} = 1 kΩ		50	100		50	100		V/mV
	T_{min} to T_{max}		20			20			V/mV
	R_{LOAD} = 500 Ω			85			85		V/mV
DYNAMIC PERFORMANCE									
Gain Bandwidth Product		±5 V		600			600		MHz
		±15 V		750			750		MHz
Full Power Bandwidth[1, 2]	V_O = 2 V p-p								
	R_{LOAD} = 500 Ω	±5 V		25			25		MHz
	V_O = 20 V p-p								
	R_{LOAD} = 1 kΩ	±15 V		3.6			3.6		MHz
Slew Rate[2]	R_{LOAD} = 500 Ω	±5 V		150			150		V/µs
	R_{LOAD} = 1 kΩ	±15 V		230			230		V/µs
Settling Time to 0.1%	A_V = −19								
	−2.5 V to +2.5 V	±5 V		65			65		ns
	10 V Step	±15 V		90			90		ns
Phase Margin[2]	C_{LOAD} = 10 pF	±15 V							
	R_{LOAD} = 1 kΩ			60			60		Degrees
DIFFERENTIAL GAIN ERROR[3]	R_{LOAD} = 100 Ω	±15 V							
	C_{COMP} = 30 pF			0.02			0.02		%
DIFFERENTIAL PHASE ERROR[3]	R_{LOAD} = 100 Ω	±15 V							
	C_{COMP} = 30 pF			0.04			0.04		Degrees
COMMON-MODE REJECTION	V_{CM} = ±2.5 V	±5 V	100	120		100	120		dB
	V_{CM} = ±12 V	±15 V	100	120		100	120		dB
	T_{min} to T_{max}		96			96			dB
POWER SUPPLY REJECTION	V_S = ±4.5 V to ±18 V		98	120		98	120		dB
	T_{min} to T_{max}		94			94			dB
INPUT VOLTAGE NOISE	f = 1 kHz	±15 V		1.7	2		1.7	2	nV/$\sqrt{Hz}$
INPUT CURRENT NOISE	f = 1 kHz	±15 V		1.5			1.5		pA/$\sqrt{Hz}$
INPUT COMMON-MODE VOLTAGE RANGE		±5 V		+4.3			+4.3		V
				−3.8			−3.8		V
		±15 V		+14.3			+14.3		V
				−13.8			−13.8		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 500 Ω	±5 V	3.0	3.6		3.0	3.6		±V
	R_{LOAD} = 150 Ω	±5 V	2.5	3.0		2.5	3.0		±V
	R_{LOAD} = 50 Ω	±5 V		1.4			1.4		±V
	R_{LOAD} = 1 kΩ	±15 V	12	13.3		12	13.3		±V
	R_{LOAD} = 500 Ω	±15 V	10	12.2		10	12.2		±V
Short Circuit Current		±5 V, ±15 V		32			32		mA
INPUT CHARACTERISTICS									
Input Resistance (Differential)				13			13		kΩ
Input Capacitance (Differential)[4]				5			5		pF
Input Capacitance (Common Mode)				1.5			1.5		pF
CLOSED-LOOP OUTPUT RESISTANCE	A_V = +1, f = 1 kHz			2			2		mΩ

Model	Conditions	V_S	AD829J Min	AD829J Typ	AD829J Max	AD829 A/S Min	AD829 A/S Typ	AD829 A/S Max	Units
POWER SUPPLY									
Operating Range			±4.5		±18		±4.5	±18	V
Quiescent Current		±5 V		5	6.5		5	6.5	mA
	T_{min} to T_{max}				8.0			8.2/8.7	mA
		±15 V		5.3	6.8		5.3	6.8	mA
	T_{min} to T_{max}				8.3			8.5/9.0	mA
TRANSISTOR COUNT	Number of Transistors			46			46		

NOTES
[1]Full Power Bandwidth = Slew Rate/2 π V_{PEAK}.
[2]Tested at Gain = +20, C_{COMP} = 0 pF.
[3]3.58 MHz (NTSC) and 4.43 MHz (PAL & SECAM).
[4]Differential input capacitance consists of 1.5 pF package capacitance plus 3.5 pF from the input differential pair.
Specifications subject to change without notice.

2

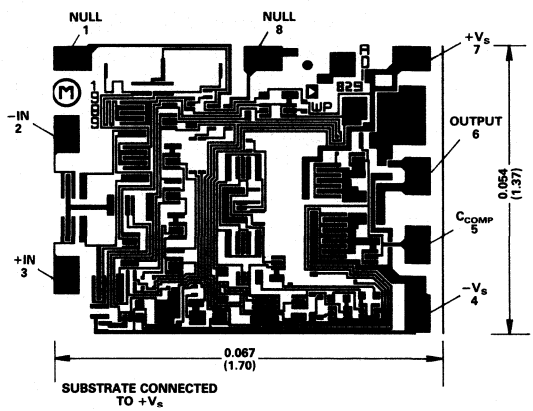
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
Plastic (N) . . . . . 1.3 Watts
Small Outline (R) . . . . . 0.9 Watts
Cerdip (Q) . . . . . 1.3 Watts
Input Voltage . . . . . $\pm V_S$
Differential Input Voltage[3] . . . . . ±6 Volts
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range (Q) . . . . . −65°C to +150°C
Storage Temperature Range (N, R) . . . . . −65°C to +125°C
Operating Temperature Range
AD829J . . . . . 0 to +70°C
AD829A . . . . . −40°C to +85°C
AD829S . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Maximum internal power dissipation is specified so that T_J does not exceed +175°C at an ambient temperature of +25°C.
Thermal characteristics:
8-pin plastic package: θ_{JA} = 100°C/watt (derate at 8.7 mW/°C)
8-pin cerdip package: θ_{JA} = 110°C/watt (derate at 8.7 mW/°C)
8-pin small outline package: θ_{JA} = 155°C/watt (derate at 6 mW/°C).
[3]If the differential voltage exceeds 6 volts, external series protection resistors should be added to limit the input current.

METALIZATION PHOTO

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD829JN	0 to +70°C	8-Pin Plastic Mini-DIP	N-8
AD829JR	0 to +70°C	8-Pin Plastic SOIC	R-8
AD829JR-REEL	0 to +70°C	Tape & Reel	
AD829AQ	−40°C to +85°C	8-Pin Cerdip	Q-8
AD829SQ	−55°C to +125°C	8-Pin Cerdip	Q-8
AD829SQ/883B	−55°C to +125°C	8-Pin Cerdip	Q-8
AD829JChips	0 to +70°C	Die	
AD829SChips	−55°C to +125°C	Die	

*N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.

AD829—Typical Performance Characteristics

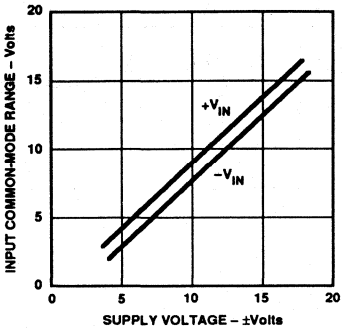


Figure 1. Input Common-Mode Range vs. Supply Voltage

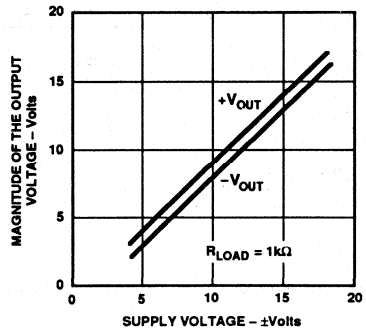


Figure 2. Output Voltage Swing vs. Supply Voltage

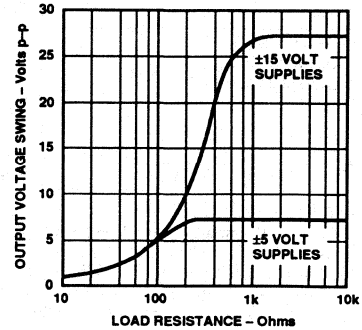


Figure 3. Output Voltage Swing vs. Resistive Load

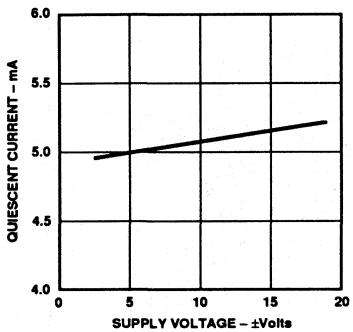


Figure 4. Quiescent Current vs. Supply Voltage

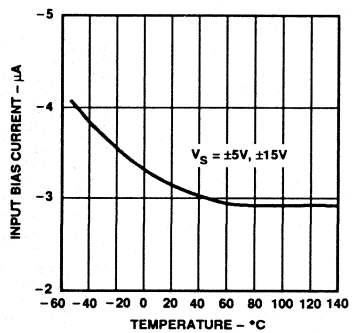


Figure 5. Input Bias Current vs. Temperature

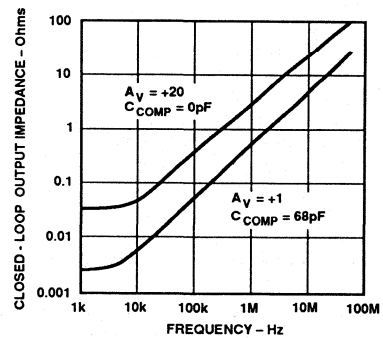


Figure 6. Closed-Loop Output Impedance vs. Frequency

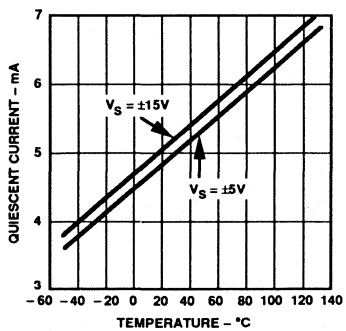


Figure 7. Quiescent Current vs. Temperature

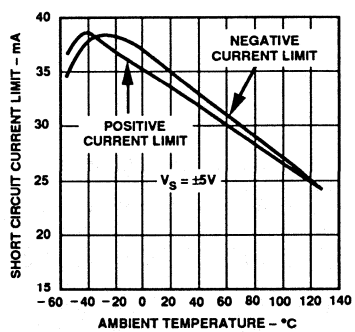


Figure 8. Short Circuit Current Limit vs. Temperature

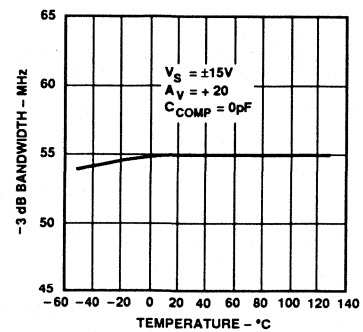


Figure 9. –3 dB Bandwidth vs. Temperature

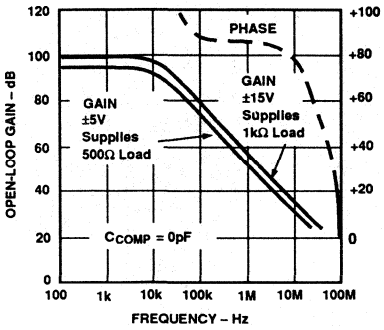


Figure 10. Open-Loop Gain & Phase Margin vs. Frequency

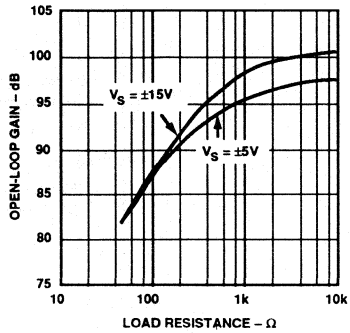


Figure 11. Open-Loop Gain vs. Resistive Load

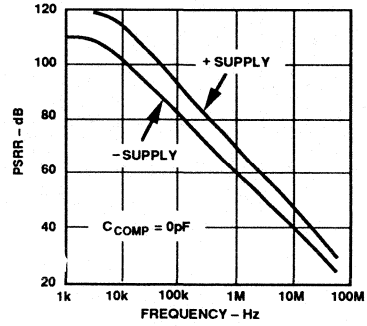


Figure 12. Power Supply Rejection Ratio (PSRR) vs. Frequency

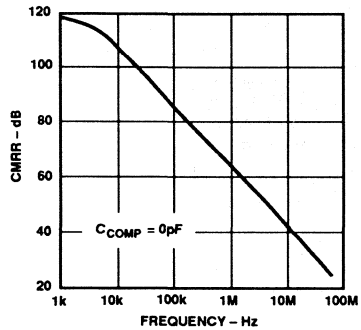


Figure 13. Common-Mode Rejection Ratio vs. Frequency

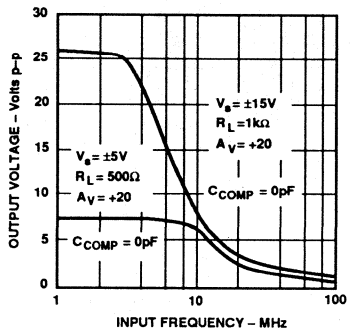


Figure 14. Large Signal Frequency Response

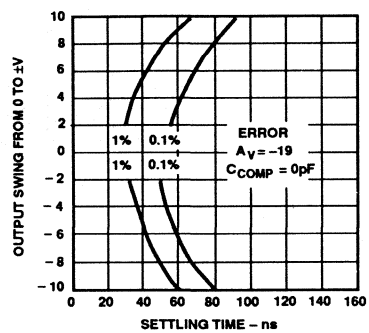


Figure 15. Output Swing & Error vs. Settling Time

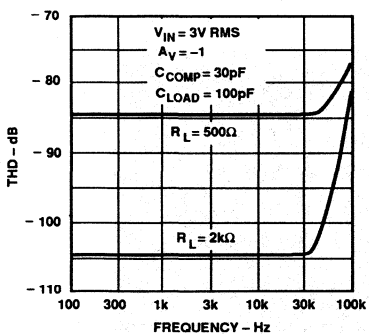


Figure 16. Total Harmonic Distortion (THD) vs. Frequency

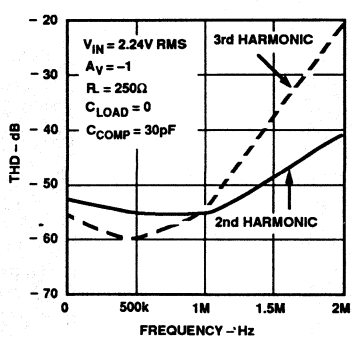


Figure 17. 2nd & 3rd Harmonic Distortion vs. Frequency

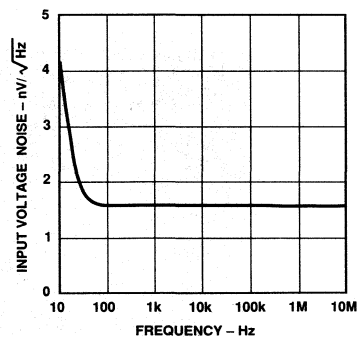


Figure 18. Input Voltage Noise Spectral Density

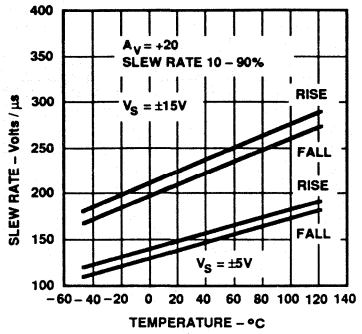


Figure 19. Slew Rate vs. Temperature

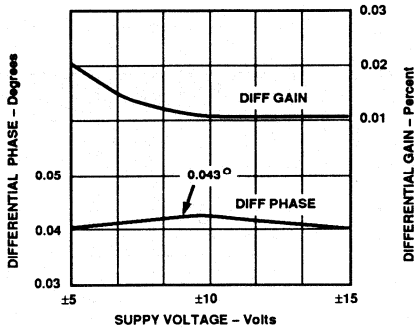


Figure 20. Differential Gain & Phase vs. Supply

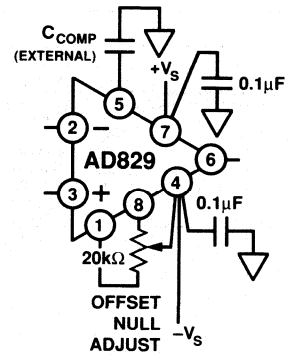


Figure 21. Offset Null and External Shunt Compensation Connections

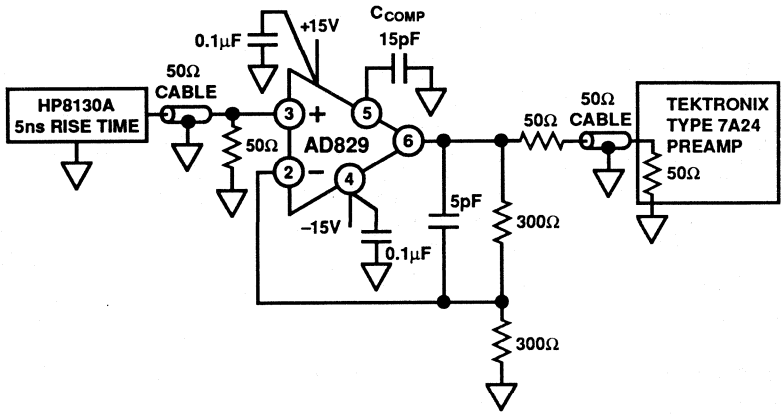


Figure 22a. Follower Connection. Gain = +2

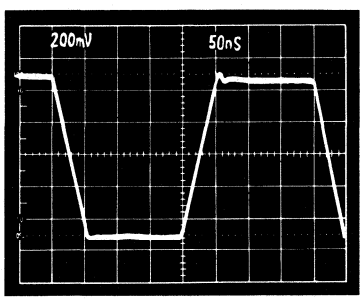


Figure 22b. Gain of 2 Follower Large Signal Pulse Response

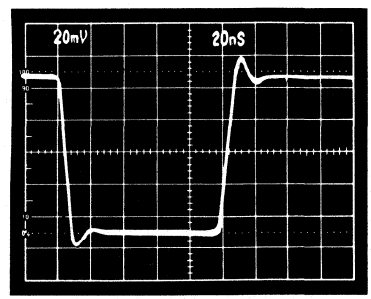


Figure 22c. Gain of 2 Follower Small Signal Pulse Response

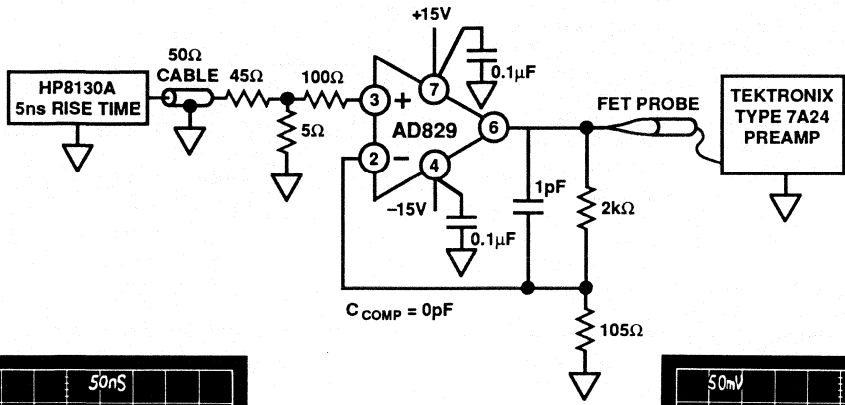


Figure 23a. Follower Connection. Gain = +20

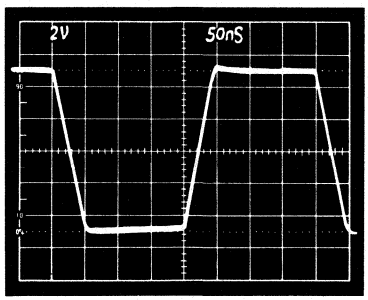


Figure 23b. Gain of 20 Follower Large Signal Pulse Response

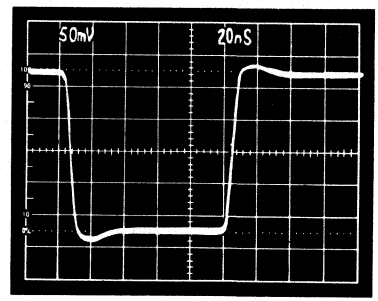


Figure 23c. Gain of 20 Follower Small Signal Pulse Response

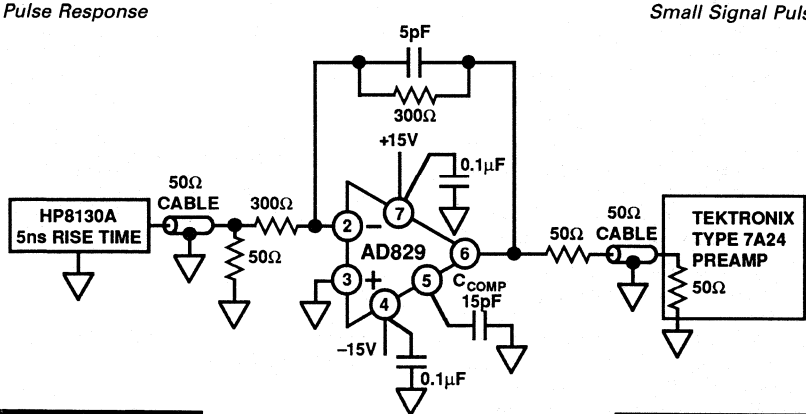


Figure 24a. Unity Gain Inverter Connection

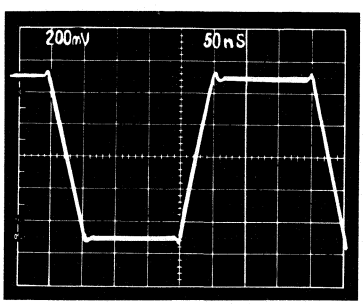


Figure 24b. Unity Gain Inverter Large Signal Pulse Response

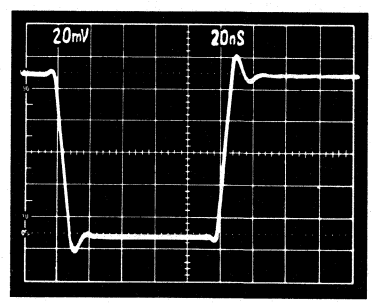


Figure 24c. Unity Gain Inverter Small Signal Pulse Response

THEORY OF OPERATION

The AD829 is fabricated on Analog Devices' proprietary complementary bipolar (CB) process which provides PNP and NPN transistors with similar f_Ts of 600 MHz. As shown in Figure 25, the AD829 input stage consists of an NPN differential pair in which each transistor operates at 600 μA collector current. This gives the input devices a high transconductance and hence gives the AD829 a low noise figure of 2 nV/$\sqrt{Hz}$ @ 1 kHz.

The input stage drives a folded cascode which consists of a fast pair of PNP transistors. These PNPs then drive a current mirror which provides a differential-input to single-ended-output conversion. The high speed PNPs are also used in the current-amplifying output stage which provides high current gain of 40,000. Even under conditions of heavy loading, the high f_Ts of the NPN & PNPs, produced using the CB process, permit cascading two stages of emitter followers while still maintaining 60° of phase margin at closed-loop bandwidths greater than 50 MHz.

Two stages of complementary emitter followers also effectively buffer the high impedance compensation node (at the C_{COMP} pin) from the output so that the AD829 can maintain a high dc open-loop gain, even into low load impedances: 92 dB into a 150 Ω load, 100 dB into a 1 kΩ load. Laser trimming and PTAT biasing assure low offset voltage and low offset voltage drift enabling the user to eliminate ac coupling in many applications.

For added flexibility, the AD829 provides access to the internal frequency compensation node. This allows the user to customize frequency response characteristics for a particular application.

Unity gain stability requires a compensation capacitance of 68 pF (Pin 5 to ground) which will yield a small signal bandwidth of 66 MHz and slew rate of 16 V/μs. The slew rate and gain bandwidth product will vary inversely with compensation capacitance. Table I and the graph of Figure 28 show the optimum compensation capacitance and the resulting slew rate for a desired noise gain. For gains between 1 and 20, C_{COMP} can be chosen to keep the small signal bandwidth relatively constant. The minimum gain which will still provide stability also depends on the value of external compensation capacitance.

An RC network in the output stage (Figure 25) completely removes the effect of capacitive loading when the amplifier is compensated for closed-loop gains of 10 or higher. At low frequencies, and with low capacitive loads, the gain from the compensation node to the output is very close to unity. In this case, C is bootstrapped and does not contribute to the compensation capacitance of the device. As the capacitive load is increased, a pole is formed with the output impedance of the output stage– this reduces the gain, and subsequently, C is incompletely bootstrapped. Therefore, some fraction of C contributes to the compensation capacitance, and the unity gain bandwidth falls. As the load capacitance is further increased, the bandwidth continues to fall, and the amplifier remains stable.

Externally Compensating the AD829

The AD829 is stable with no external compensation for noise gains greater than 20. For lower gains, there are two methods of frequency compensating the amplifier to achieve closed-loop stability; these are the shunt and current feedback compensation methods.

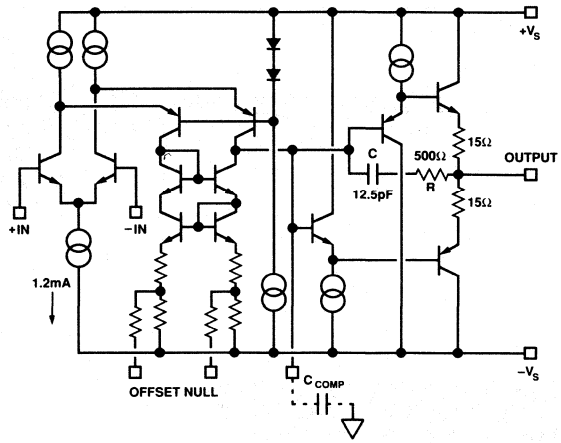


Figure 25. AD829 Simplified Schematic

Shunt Compensation

Figures 26 & 27 show that the first method, shunt compensation, has an external compensation capacitor, C_{COMP}, connected between the compensation pin and ground. This external capacitor is tied in parallel with approximately 3 pF of internal capacitance at the compensation node. In addition, a small capacitance, C_{LEAD}, in parallel with resistor R_2, compensates for the capacitance at the amplifier's inverting input.

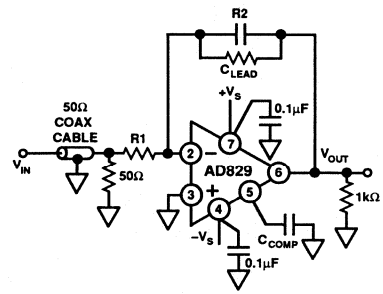


Figure 26. Inverting Amplifier Connection Using External Shunt Compensation

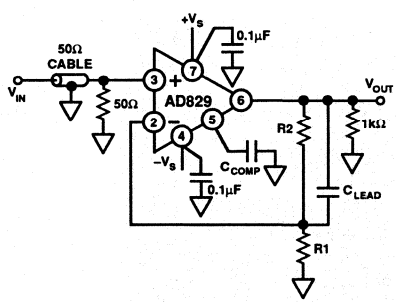


Figure 27. Noninverting Amplifier Connection Using External Shunt Compensation

Table I. Component Selection for Shunt Compensation

Follower Gain	Inverter Gain	R1 Ω	R2 Ω	C_L pF	C_{COMP} pF	Slew Rate V/μs	−3 dB Small Signal Bandwidth – MHz
1		Open	100	0	68	16	66
2	−1	1k	1k	5	25	38	71
5	−4	511	2.0k	1	7	90	76
10	−9	226	2.05k	0	3	130	65
20	−19	105	2k	0	0	230	55
25	−24	105	2.49	0	0	230	39
100	−99	20	2k	0	0	230	7.5

Table I gives recommended C_{COMP} and C_{LEAD} values along with the corresponding slew rates and bandwidth. The capacitor values given were selected to provide a small signal frequency response with less than 1 dB of peaking and less than 10% overshoot. For this table, supply voltages of ±15 volts should be used. Figure 28 is a graphical extension of the table which shows the slew rate/gain trade-off for lower closed-loop gains, when using the shunt compensation scheme.

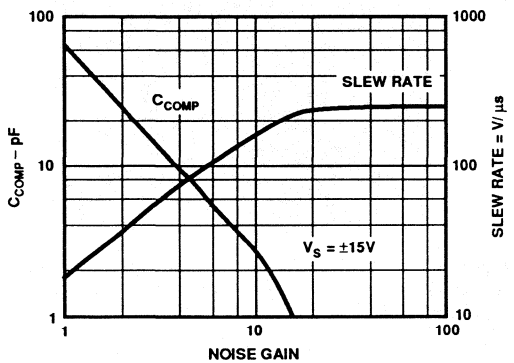


Figure 28. Value of C_{COMP} & Slew Rate vs. Noise Gain

Current Feedback Compensation

Bipolar nondegenerated amplifiers which are single pole and internally compensated have their bandwidths defined as:

$$f_T = \frac{1}{2\pi r_e C_{COMP}} = \frac{I}{2\pi \frac{kT}{q} C_{COMP}}$$

where:

f_T is the unity gain bandwidth of the amplifier
I is the collector current of the input transistor
C_{COMP} is the compensation capacitance
r_e is the inverse of the transconductance of the input transistors
kT/q is approximately equal to 26 mV @ 27°C.

Since both f_T and slew rate are functions of the same variables, the dynamic behavior of an amplifier is limited. Since:

$$Slew\ Rate = \frac{2I}{C_{COMP}}$$

then:

$$\frac{Slew\ Rate}{f_T} = 4\pi \frac{kT}{q}$$

This shows that the slew rate will be only 0.314 V/μs for every MHz of bandwidth. The only way to increase slew rate is to increase the f_T and that is difficult, due to process limitations. Unfortunately, an amplifier with a bandwidth of 10 MHz can only slew at 3.1 V/μs, which is barely enough to provide a full power bandwidth of 50 kHz.

The AD829 is especially suited to a new form of compensation which allows for the enhancement of both the full power bandwidth and slew rate of the amplifier. The voltage gain from the inverting input pin to the compensation pin is large; therefore, if a capacitance is inserted between these pins, the amplifier's bandwidth becomes a function of its feedback resistor and this capacitance. The slew rate of the amplifier is now a function of its internal bias (2I) and this compensation capacitance.

Since the closed-loop bandwidth is a function of R_F and C_{COMP} (Figure 29), it is independent of the amplifier closed-loop gain, as shown in Figure 31. To preserve stability, the time constant of R_F and C_{COMP} needs to provide a bandwidth of less than 65 MHz. For example, with C_{COMP} = 15 pF and R_F = 1 kΩ, the small signal bandwidth of the AD829 is 10 MHz, while Figure 30 shows that the slew rate is in excess of 60 V/μs. As can be seen in Figure 31, the closed-loop bandwidth is constant for gains of −1 to −4, a property of current feedback amplifiers.

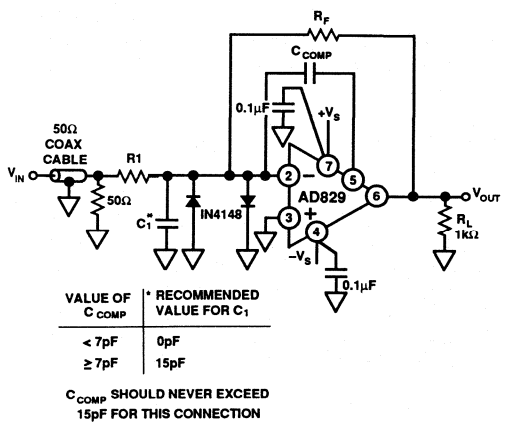


Figure 29. Inverting Amplifier Connection Using Current Feedback Compensation

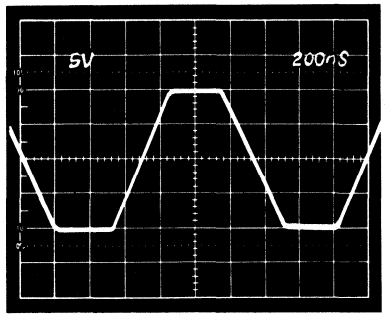


Figure 30. Large Signal Pulse Response of Inverting Amplifier Using Current Feedback Compensation. C_{COMP} = 15 pF, C_1 = 15 pF, R_F = 1 kΩ, R_1 = 1 kΩ

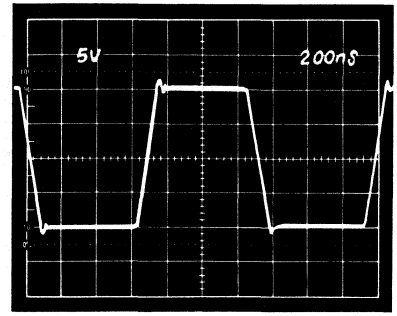


Figure 32. Large Signal Pulse Response of the Inverting Amplifier Using Current Feedback Compensation. C_{COMP} = 1 pF, R_F = 3 kΩ, R_1 = 3 kΩ

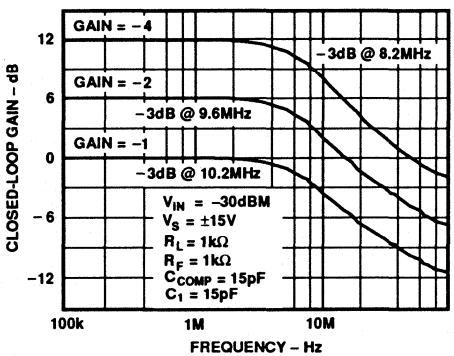


Figure 31. Closed-Loop Gain vs. Frequency for the Circuit of Figure 29

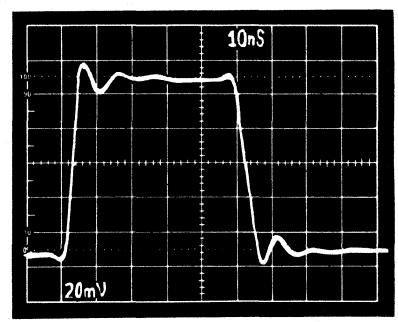


Figure 33. Small Signal Pulse Response of Inverting Amplifier Using Current Feedback Compensation. C_{COMP} = 4 pF, R_F = 1 kΩ, R_1 = 1 kΩ

Figure 32 is an oscilloscope photo of the pulse response of a unity gain inverter which has been configured to provide a small signal bandwidth of 53 MHz and a subsequent slew rate of 180 V/μs; resistor R_F = 3 kΩ, capacitor C_{COMP} = 1 pF. Figure 33 shows the excellent pulse response as a unity gain inverter, this time using component values of: R_F = 1 kΩ and C_{COMP} = 4 pF.

Figures 34 and 35 show the closed-loop frequency response of the AD829 for different closed-loop gains and for different supply voltages.

If a noninverting amplifier configuration using current feedback compensation is desired, the circuit of Figure 36 is recommended. This circuit doubles the slew rate compared to the shunt compensated noninverting amplifier of Figure 27 at the expense of gain flatness. Nonetheless, this circuit delivers 95 MHz bandwidth with ±1 dB flatness into a back terminated cable, with a differential gain error of only 0.01%, and a differential phase error of only 0.015° at 4.43 MHz.

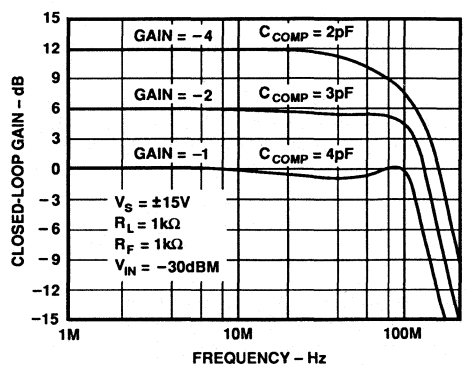


Figure 34. Closed-Loop Frequency Response for the Inverting Amplifier Using Current Feedback Compensation

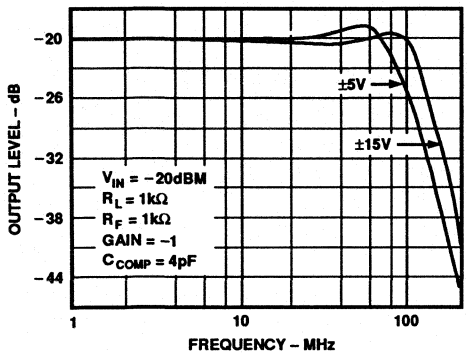


Figure 35. Closed-Loop Frequency Response vs. Supply for the Inverting Amplifier Using Current Feedback Compensation

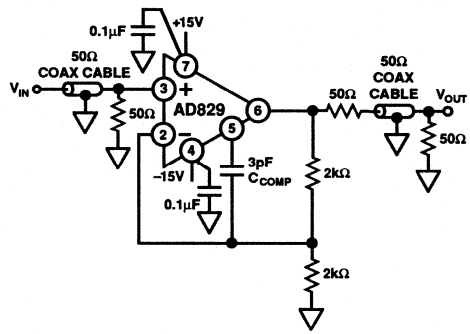


Figure 36. Noninverting Amplifier Connection Using Current Feedback Compensation

A Low Error Video Line Driver

The buffer circuit shown in Figure 37 will drive a back-terminated 75 Ω video line to standard video levels (1 V p–p) with 0.1 dB gain flatness to 30 MHz with only 0.04° and 0.02% differential phase and gain at the 4.43 MHz PAL color subcarrier frequency. This level of performance, which meets the requirements for high definition video displays and test equipment, is achieved using only 5 mA quiescent current.

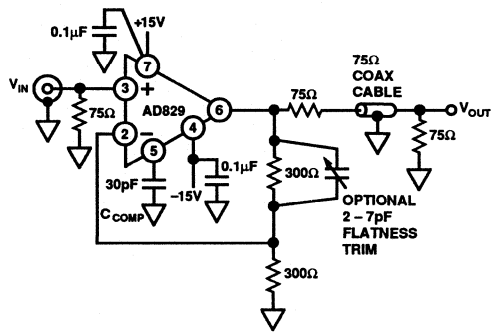
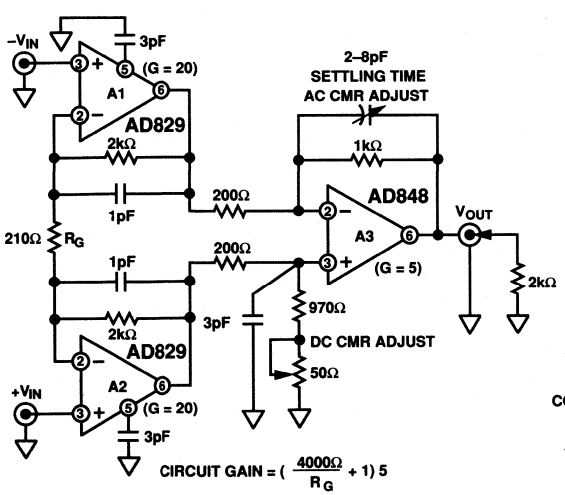


Figure 37. A Video Line Driver with a Flatness over Frequency Adjustment

A High Gain, Video Bandwidth Three Op-Amp In-Amp

Figure 38 shows a three op-amp instrumentation amplifier circuit which provides a gain of 100 at video bandwidths. At a circuit gain of 100 the small signal bandwidth equals 18 MHz into an FET probe. Small signal bandwidth equals 6.6 MHz with a 50 Ω load. 0.1% settling time is 300 ns.

The input amplifiers operate at a gain of 20, while the output op amp runs at a gain of 5. In this circuit the main bandwidth limitation is the gain/bandwidth product of the output amplifier. Extra care needs to be taken while breadboarding this circuit, since even a couple of extra picofarads of stray capacitance at the compensation pins of A1 and A2 will degrade circuit bandwidth.



INPUT FREQUENCY	CMRR
100 Hz	64.6 dB
1 MHz	44.7 dB
10 MHz	23.9 dB

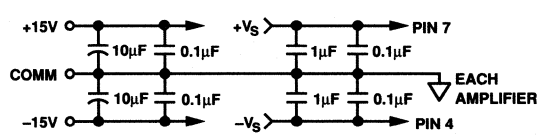


Figure 38. A High Gain, Video Bandwidth Three Op-Amp In-Amp Circuit

High Speed, Video Difference Amplifier

AD830

FEATURES

Differential Amplification
- Wide Common-Mode Voltage Range: +13 V, −11.5 V
- Differential Voltage Range: ±2 V
- High CMRR: 60 dB @ 4 MHz
- Built-in Differential Clipping Level: ±2.4 V

Fast Dynamic Performance
- 60 MHz Unity Gain Bandwidth
- 10 MHz (0.1 dB) Bandwidth
- 530 V/μs Slew Rate
- 35 ns Settling Time to 0.1%

Excellent Video Specifications
- Differential Gain Error: 0.05%
- Differential Phase Error: 0.08%

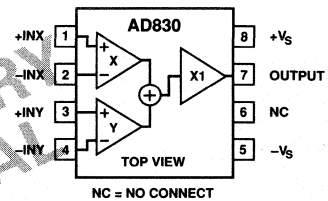
Flexible Operation
- High Output Drive of ±30 mA
- Specified with Both ±5 V and ±15 V Supplies

Low Distortion: THD = −72 dB @ 4 MHz

Excellent DC Performance: 1 mV max Input Offset Voltage

CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP (N), Cerdip (Q) and SOIC (R) Packages



PRELIMINARY TECHNICAL DATA

APPLICATIONS

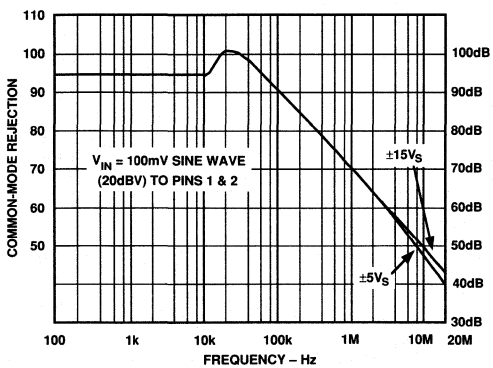
Differential Line Receiver
High Speed Level Translation
High Speed In-Amp
Differential to Single Ended Conversion
Resistorless Summation and Subtraction

PRODUCT DESCRIPTION

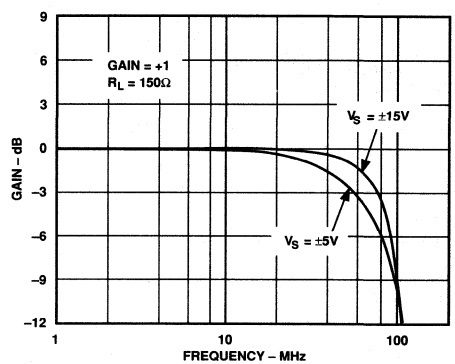
The AD830 is a wideband, differencing amplifier designed for use at video frequencies. It accurately amplifies a fully differential signal at the input and produces an output voltage referred to a user-chosen level. The undesired common-mode signal is rejected, even at high frequencies. High impedance inputs ease interfacing to finite source impedances and thus preserve the good common-mode rejection. In this respect, it offers significant improvements over discrete difference amplifier approaches.

The wide common-mode and differential-voltage range of the AD830 also make it particularly useful and flexible in level shifting applications, but at lower power dissipation than discrete solutions with resistors. Low distortion is preserved over the many possible differential and common-mode voltages at the input and output.

Wide bandwidth, with excellent differential gain of 0.05% and phase of 0.08° makes the AD830 suitable for many video system applications. Furthermore, the AD830 is suited for general purpose signal processing from 100 kHz to 10 MHz.



Common-Mode Rejection Ratio vs. Frequency



Closed-Loop Gain vs. Frequency, Gain = +1

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD830—SPECIFICATIONS (V_S = ±5 V to ±15 V, R_{LOAD} = 1 kΩ, C_{LOAD} = 5 pF, T_A = +25°C unless otherwise noted)

Parameter	Conditions	V_S	AD830J/A Min	AD830J/A Typ	AD830J/A Max	AD830S[1] Min	AD830S[1] Typ	AD830S[1] Max	Units
INPUT CHARACTERISTICS									
Differential Voltage Range	V_{CM} = 0	All		±2.0			±2.0		V
Differential Clipping Level[2]		±5		±2.2			±2.2		V
		±15	±2.1	±2.4		±2.1	±2.4		V
Common-Mode Voltage Range	V_{DM} = ±1 V	±5	−1.7		+3.0	−1.7		+3.0	V
		±15	−11.5		+13.0	−11.5		+13.0	V
Offset Voltage	Gain = 1	±5, ±15		±1	±3		±1	±3	mV
		±10		±0.4	±1		±0.4	±1	mV
CMRR	DC	All		95			95		dB
	Freq = 4 MHz	All		60			60		dB
Input Bias Current		All		5	10		5	10	μA
Input Resistance		All		370			370		kΩ
Input Capacitance		All		2			2		pF
Input Voltage Noise		All		27			27		nV/√Hz
Input Current Noise		All		1.4			1.4		pA/√Hz
Open Loop Gain (DC)		±5		63			63		dB
		±15		67			67		dB
Peak Nonlinearity	−1 V ≤ X ≤ +1 V	All		0.01			0.01		% FS
	−1.5 V ≤ X ≤ +1.5 V	All		0.04			0.04		% FS
	−2 V ≤ X ≤ +2 V	±5		0.2			0.2		% FS
DYNAMIC CHARACTERISTICS									
3 dB Small Signal Bandwidth	Gain = 1, R_L = 150 Ω	±5		40			40		MHz
	V_{OUT} = 100 mV rms	±15		60			60		MHz
0.1 dB Gain Flatness Frequency	Gain = 1, R_L = 150 Ω	±5		5			5		MHz
	V_{OUT} = 100 mV rms	±15		10			10		MHz
Differential Gain Error	0 to +0.7 V,	±5		0.15			0.15		%
	Freq = 4.5 MHz	±15		0.05			0.05		%
Differential Phase Error	0 to +0.7 V,	±5		0.4			0.4		Degree
	Freq = 4.5 MHz	±15		0.08			0.08		Degree
Harmonic Distortion	2 V p–p, Freq = 1 MHz,	±5		−69			−69		dBc
	R_L = 150 Ω	±15		−82			−82		dBc
	2 V p–p, Freq = 4 MHz,	±5		−56			−56		dBc
	R_L = 150 Ω	±15		−72			−72		dBc
Slew Rate	2 V Step	±5		240			240		V/μs
		±15		340			340		V/μs
	4 V Step	±5		364			364		V/μs
		±15		530			530		V/μs
3 dB Full Power Bandwidth	Gain = 1, R_L = 150 Ω	±5		45			45		MHz
	V_{OUT} = 1 V rms	±15		50			50		MHz
Settling Time	V_{OUT} = 2 V Step,	±5		35			35		ns
	to 0.1%	±15		25			25		ns
	V_{OUT} = 4 V Step,	±5		48			48		ns
	to 0.1%	±15		35			35		ns
OUTPUT CHARACTERISTICS									
Output Voltage Swing	R_L ≥ 1 kΩ	±5		±3.5			±3.5		V
		±15		±13.2			±13.2		V
Output Current	Nonlinearity ≤ 1%	All		±30			±30		mA
Short-Circuit Current	Short to Ground	±5	−55		+70	−55		+70	mA
		±15	−85		+80	−85		+80	mA
POWER SUPPLIES									
Operating Range			±4		±16.5	±4		±16.5	V
Quiescent Current		±5		13.6			13.6		mA
		±15		14.4			14.4		mA
+ PSRR (to V_P)	DC, G = 1			86			86		dB
− PSRR (to V_N)	DC, G = 1			68			68		dB
PSRR	DC, G = 1								
	±5 V to ±15 V			70			70		dB

PRELIMINARY TECHNICAL DATA

NOTES
[1]See Analog Devices' military data sheet for 883B specifications.
[2]Clipping level function on X channel only.

Specifications subject to change without notice.

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ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2] . . . . . Observe Derating Curves
Output Short Circuit Duration . . . . Observe Derating Curves
Common-Mode Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . $\pm V_S$
Storage Temperature Range (Q) . . . . . −65°C to +150°C
Storage Temperature Range (N) . . . . . −65°C to +125°C
Storage Temperature Range (R) . . . . . −65°C to +125°C
Operating Temperature Range
AD830A . . . . . −40°C to +85°C
AD830S . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 seconds) . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Pin Plastic Package: θ_{JA} = 90°C/Watt
8-Pin SOIC Package: θ_{JA} = 155°C/Watt
8-Pin Cerdip Package: θ_{JA} = 110°C/Watt

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD830 is limited by the associated rise in junction temperature. For the plastic packages, the maximum safe junction temperature is 145°C. For the cerdip, the maximum junction temperature is 175°C. If these maximums are exceeded momentarily, proper circuit operation will be restored as soon as the die temperature is reduced. Leaving the AD830 in the "overheated" condition for an extended period can result in permanent damage to the device. To ensure proper operation, it is important to observe the derating curves: Figures 1 and 2.

While the AD830 output is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature is not exceeded under all conditions. If the output is shorted to a supply rail for an extended period, then the amplifier may be destroyed.

PRELIMINARY TECHNICAL DATA

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD830AN	−40°C to +85°C	8-Pin Plastic Mini-DIP	N-8
AD830JR	0°C to +70°C	8-Pin SOIC	R-8
AD830SQ/883B	−55°C to +125°C	8-Pin Cerdip	Q-8

*For outline information see Package Information section.

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AD830—Typical Characteristics

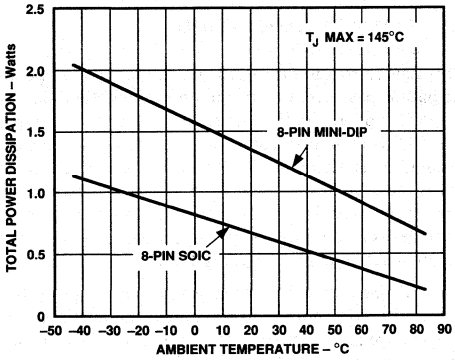


Figure 1. Maximum Power Dissipation vs. Temperature, Mini-DIP and SOIC Packages

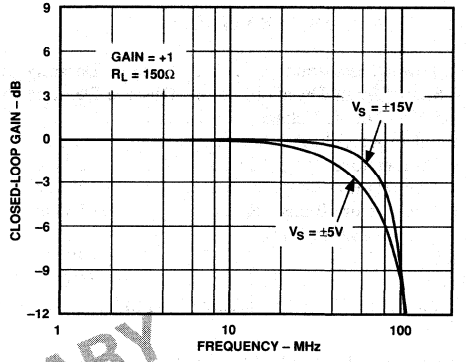


Figure 4. Closed-Loop Gain vs. Frequency, G = +1

PRELIMINARY TECHNICAL DATA

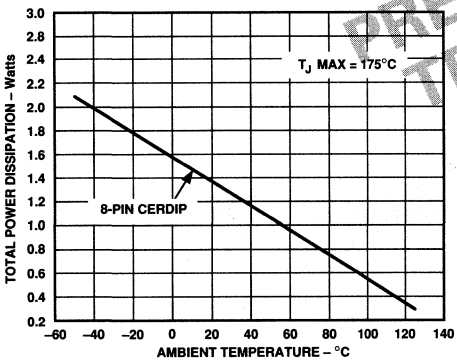


Figure 2. Maximum Power Dissipation vs. Temperature, Cerdip Package

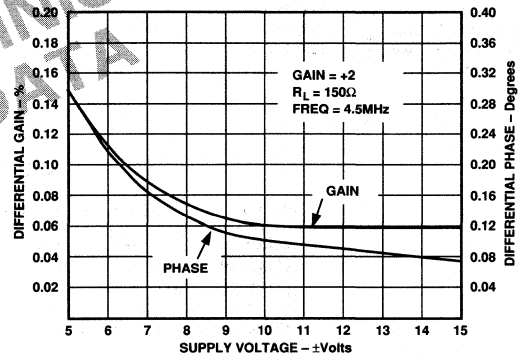


Figure 5. Differential Gain vs. Supply Voltage

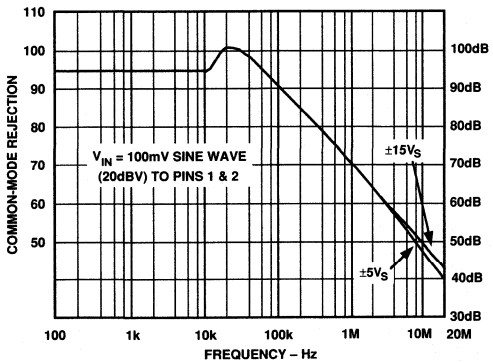


Figure 3. Common-Mode Rejection vs. Frequency

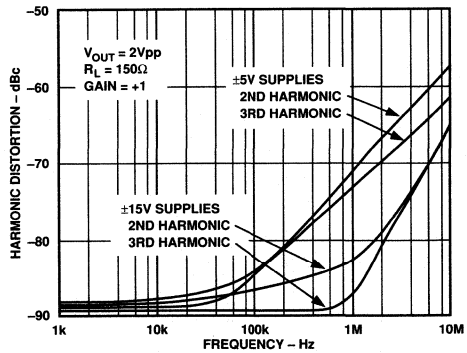


Figure 6. Harmonic Distortion vs. Frequency

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Differential Line Receiver

The AD830 is specifically designed to perform as a differential line receiver. The circuit of Figure 7 shows how simply the AD830 is configured for this function. The signal from system "A" is received differentially relative to A's ground, and that voltage is exactly reproduced relative to the ground in system B. Any common-mode noise due to ground noise, interference, etc., or mismatch in system grounds is rejected by the AD830.

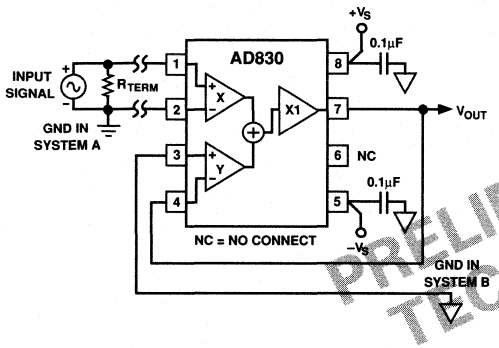


Figure 7. Differential Line Receiver

Wide Range Level Shifter

The wide common-mode voltage range and accuracy of the AD830 allows easy level shifting of signals referred to large voltages. The inputs may be referenced to levels as high as 10 V at the inputs with a ±2 V swing around 10 V. It is possible then to level shift the signal to any new level defined at the output. In the circuit of Figure 8, the output voltage V_{OUT} is defined by the simple equation shown below. The voltages do not need to be of low impedance, since the high input resistance and modest input bias current of the AD830 V-to-I converters permit the use of resistive voltage dividers as reference voltages. The excellent linearity and low distortion are preserved over the full input and output common-mode range.

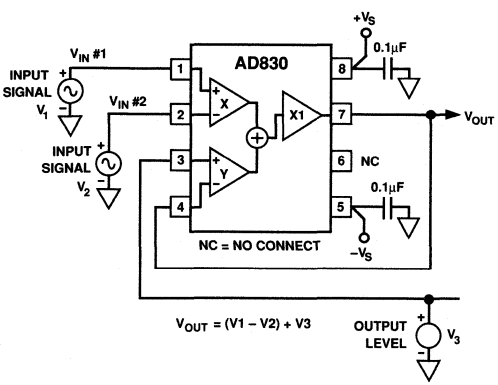


Figure 8. Level Shifter

Gain of N Instrumentation Amplifier

The AD830 may be configured for gains greater than 1 and provide instrumentation amplifier (in amp) style amplification. The input signal is connected differentially to the internal V–I converter X. The gain is set via the feedback resistors R2 and R1 in the same manner as a noninverting op amp circuit. The gain function is:

$$Gain\ N = (R2+R1)/R1$$

The polarity of the gain is established by the connection at the input. Inverting gain is set by reversing the shown connections to the input. As in a conventional voltage feedback op amp, the bandwidth decreases with increasing gain.

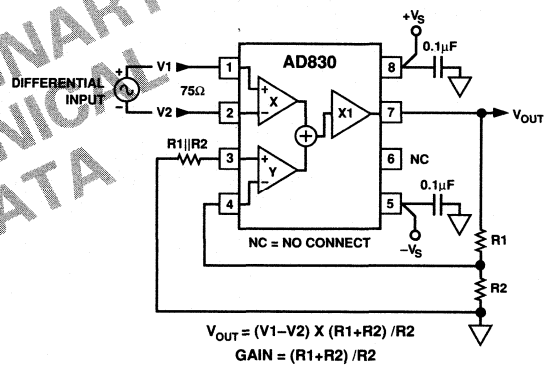


Figure 9. Gain of N Instrumentation Amplifier

Cable Receiver

The AD830 is ideally suited for the video cable receiver circuit shown in Figure 10. Here the cable is terminated at its own shield. The input signal is taken differentially from the conductor to shield and then amplified relative to the *board ground*. The 499 Ω resistors set the gain at ×2, with the 249 Ω included in series with the input to ground to cancel input bias current induced offsets. A 75 Ω resistor connected at the output serves as the standard back termination impedance. Therefore, the net gain to the load resistor is unity.

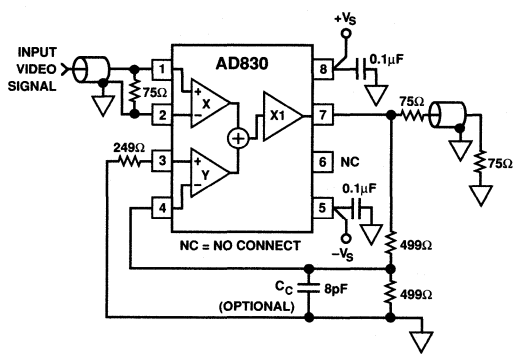


Figure 10. Video Cable Receiver/Driver

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ANALOG DEVICES

Wideband, Fast Settling Op Amp

AD840

FEATURES

Wideband AC Performance
- Gain Bandwidth Product: 400 MHz (Gain ≥ 10)
- Fast Settling: 100 ns to 0.01% for a 10 V Step
- Slew Rate: 400 V/μs
- Stable at Gains of 10 or Greater
- Full Power Bandwidth: 6.4 MHz for 20 V p–p into a 500 Ω Load

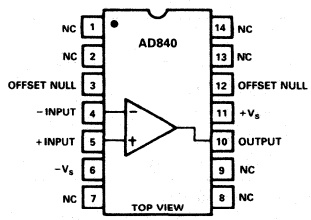
Precision DC Performance
- Input Offset Voltage: 0.3 mV max
- Input Offset Drift: 3 μV/°C typ
- Input Voltage Noise: 4 nV/$\sqrt{Hz}$
- Open-Loop Gain: 130 V/mV into a 1 kΩ Load
- Output Current: 50 mA min
- Supply Current: 12 mA max

APPLICATIONS

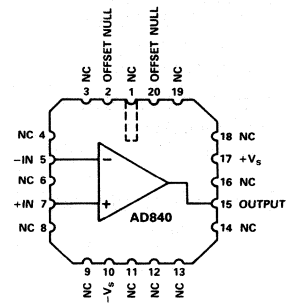
- Video and Pulse Amplifiers
- DAC and ADC Buffers
- Line Drivers
- Available in 14-Pin Plastic DIP, Hermetic Cerdip and 20-Pin LCC Packages and in Chip Form
- MIL-STD-883B Processing Available

CONNECTION DIAGRAMS

Plastic DIP (N) Package and Cerdip (Q) Package



LCC (E) Package



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD840 is a member of the Analog Devices' family of wide bandwidth operational amplifiers. This high speed/high precision family includes, among others, the AD841, which is unity-gain stable, and the AD842, which is stable at a gain of two or greater and has 100 mA minimum output current drive. These devices are fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. This process permits a combination of dc precision and wideband ac performance previously unobtainable in a monolithic op amp. In addition to its 400 MHz gain bandwidth product, the AD840 offers extremely fast settling characteristics, typically settling to within 0.01% of final value in 100 ns for a 10 volt step.

The AD840 remains stable over its full operating temperature range at closed-loop gains of 10 or greater. It also offers a low quiescent current of 12 mA maximum, a minimum output current drive capability of 50 mA, a low input voltage noise of 4 nV/$\sqrt{Hz}$ and a low input offset voltage of 0.3 mV maximum (AD840K).

The 400 V/μs slew rate of the AD840, along with its 400 MHz gain bandwidth, ensures excellent performance in video and pulse amplifier applications. This amplifier is ideally suited for use in high frequency signal conditioning circuits and wide bandwidth active filters. The extremely rapid settling time of the AD840 makes it the preferred choice for data acquisition applications which require 12-bit accuracy. The AD840 is also appropriate for other applications such as high speed DAC and ADC buffer amplifiers and other wide bandwidth circuitry.

APPLICATION HIGHLIGHTS

1. The high slew rate and fast settling time of the AD840 make it ideal for DAC and ADC buffers, line drivers and all types of video instrumentation circuitry.
2. The AD840 is truly a precision amplifier. It offers 12-bit accuracy to 0.01% or better and wide bandwidth, performance previously available only in hybrids.
3. The AD840's thermally balanced layout and the high speed of the CB process allow the AD840 to settle to 0.01% in 100 ns without the long "tails" that occur with other fast op amps.
4. Laser wafer trimming reduces the input offset voltage to 0.3 mV max on the K grade, thus eliminating the need for external offset nulling in many applications. Offset null pins are provided for additional versatility.
5. Full differential inputs provide outstanding performance in all standard high frequency op amp applications where circuit gain will be 10 or greater.
6. The AD840 is an enhanced replacement for the HA2540.

AD840—SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD840J Min	AD840J Typ	AD840J Max	AD840K Min	AD840K Typ	AD840K Max	AD840S Min	AD840S Typ	AD840S Max	Units
INPUT OFFSET VOLTAGE[1]			0.2	**1**		0.1	**0.3**		0.2	**1**	mV
	$T_{min} - T_{max}$			1.5			**0.7**			2	mV
Offset Drift			5			3			5		μV/°C
INPUT BIAS CURRENT			3.5	**8**		3.5	**5**		3.5	**8**	μA
	$T_{min} - T_{max}$			10			**6**			12	μA
INPUT OFFSET CURRENT			0.1	**0.4**		0.1	**0.2**		0.1	**0.4**	μA
	$T_{min} - T_{max}$			0.5			**0.3**			0.6	μA
INPUT CHARACTERISTICS	Differential Mode										
Input Resistance			30			30			30		kΩ
Input Capacitance			2			2			2		pF
INPUT VOLTAGE RANGE											
Common Mode		**±10**	12		**±10**	12		±10	12		V
Common-Mode Rejection	$V_{CM} = \pm 10$ V	**90**	110		**106**	115		**90**	110		dB
	$T_{min} - T_{max}$	85			**90**			85			dB
INPUT VOLTAGE NOISE	f = 1 kHz		4			4			4		nV/√Hz
Wideband Noise	10 Hz to 10 MHz		10			10			10		μV rms
OPEN LOOP GAIN	$V_O = \pm 10$ V										
	$R_{LOAD} = 1$ kΩ	**100**	130		**100**	130		**100**	130		V/mV
	$T_{min} - T_{max}$	50	80		**75**	100		**50**	80		V/mV
	$R_{LOAD} = 500$ Ω	**75**			**100**			75			V/mV
	$T_{min} - T_{max}$	50			**75**			50			V/mV
OUTPUT CHARACTERISTICS											
Voltage	$R_{LOAD} \geq 500$ Ω										
	$T_{min} - T_{max}$	**±10**			**±10**			**±10**			V
Current	$V_{OUT} = \pm 10$ V	**50**			**50**			**50**			mA
Output Resistance	Open Loop		15			15			15		Ω
FREQUENCY RESPONSE											
Gain Bandwidth Product	$V_{OUT} = 90$ mV p–p										
	$A_V = -10$		400			400			400		MHz
Full Power Bandwidth[2]	$V_O = 20$ V p–p										
	$R_{LOAD} \geq 500$ Ω	5.5	6.4		5.5	6.4		5.5	6.4		MHz
Rise Time	$A_V = -10$		10			10			10		ns
Overshoot[3]	$A_V = -10$		20			20			20		%
Slew Rate[3]	$A_V = -10$	350	400		350	400		350	400		V/μs
Settling Time[3] −10 V Step	$A_V = -10$										
	to 0.1%		80			80			80		ns
	to 0.01%		100			100			100		ns
OVERDRIVE RECOVERY	−Overdrive		190			190			190		ns
	+Overdrive		350			350			350		ns
DIFFERENTIAL GAIN	f = 4.4 MHz		0.025			0.025			0.025		%
DIFFERENTIAL PHASE	f = 4.4 MHz		0.04			0.04			0.04		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		±5		**±18**	±5		**±18**	±5		**±18**	V
Quiescent Current			12	**14**		12	**14**		12	**14**	mA
	$T_{min} - T_{max}$			16			**16**			**18**	mA
Power Supply Rejection Ratio	$V_S = \pm 5$ V to ±18 V	**90**	100		**94**	100		**90**	100		dB
	$T_{min} - T_{max}$	80			**86**			**80**			dB
TEMPERATURE RANGE											
Rated Performance[4]		**0**		**+75**	0		**+75**	−55		**+125**	°C
TRANSISTOR COUNT	# of Transistors		72			72			72		

NOTES
[1]Input offset voltage specifications are guaranteed after 5 minutes at T_A = +25°C.
[2]Full power bandwidth = slew rate/2π V_{PEAK}.
[3]Refer to Figures 22 and 23.
[4]"S" grade T_{min}–T_{max} specifications are tested with automatic test equipment at T_A = −55°C and T_A = +125°C.
All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
Plastic (N) . . . . . 1.5 W
Cerdip (Q) . . . . . 1.3 W
LCC (E) . . . . . 1.0 W
Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±6 V
Storage Temperature Range
Q, E . . . . . −65°C to +150°C
N . . . . . −65°C to +125°C
Junction Temperature (T_J) . . . . . +175°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

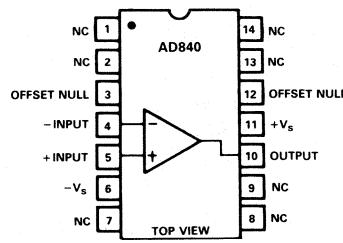
NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Maximum internal power dissipation is specified so that T_J does not exceed +175°C at an ambient temperature of +25°C.

Thermal Characteristics:

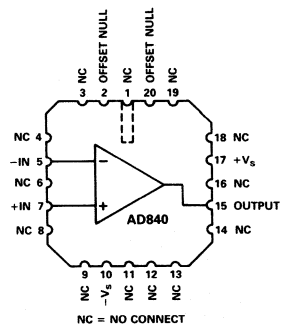
	θ_{JC}	θ_{JA}	Derate at
Cerdip Package	30°C/W	110°C/W	8.7 mW/°C
Plastic Package	30°C/W	100°C/W	10 mW/°C
LCC Package	35°C/W	150°C/W	6.7 mW/°C

Recommended Heat Sink:
Aavid Engineering© #602B

Plastic DIP (N) Package and Cerdip (Q) Package



LCC (E) Package



AD840 Connection Diagrams

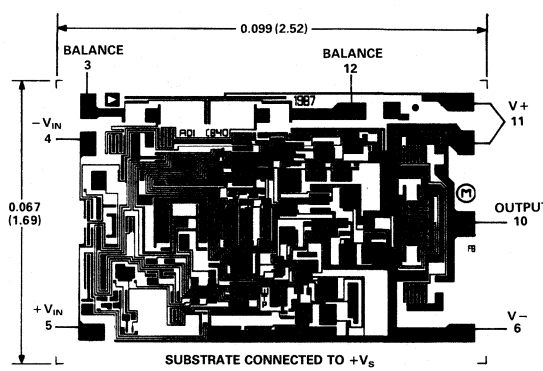
ORDERING GUIDE

Model[1]	Package Options[2]
AD840JN	N-14
AD840KN	N-14
AD840JQ	Q-14
AD840KQ	Q-14
AD840SQ	Q-14
AD840SQ-883B	Q-14
AD840SE-883B	E-20A

NOTES
[1]J and S Grade Chips also available.
[2]N = Plastic DIP; Q = Cerdip; E = LCC (Leadless Ceramic Chip Carrier). For outline information see Package Information section.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



AD840—Typical Characteristics (at +25°C and V_S = ±15 V, unless otherwise noted)

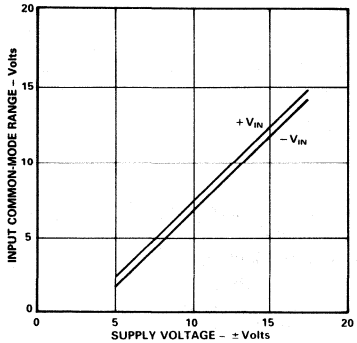


Figure 1. Input Common-Mode Range vs. Supply Voltage

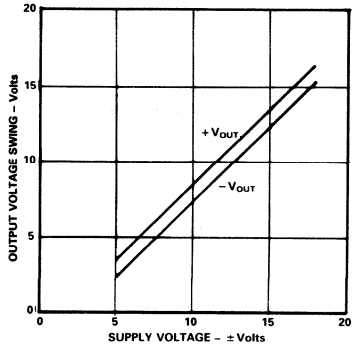


Figure 2. Output Voltage Swing vs. Supply Voltage

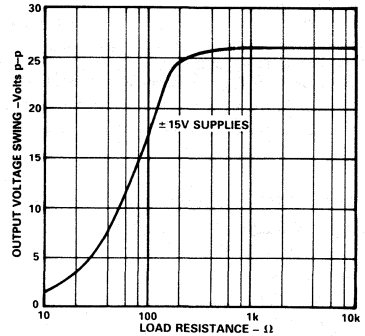


Figure 3. Output Voltage Swing vs. Load Resistance

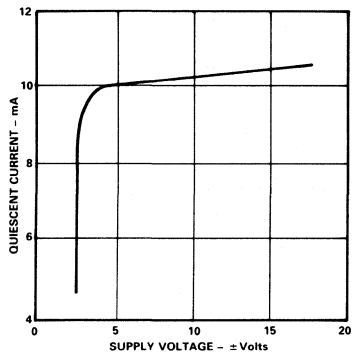


Figure 4. Quiescent Current vs. Supply Voltage

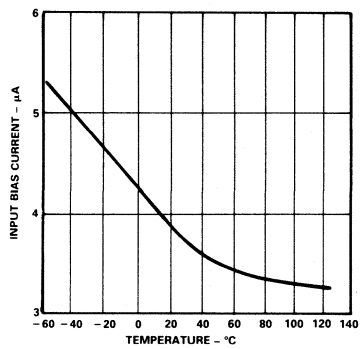


Figure 5. Input Bias Current vs. Temperature

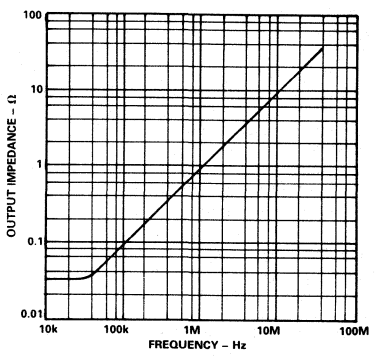


Figure 6. Output Impedance vs. Frequency

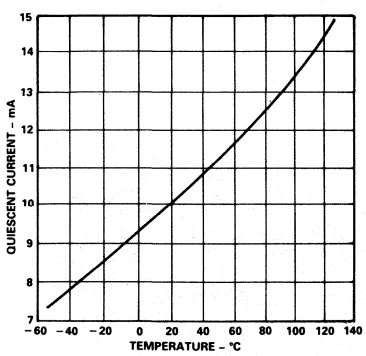


Figure 7. Quiescent Current vs. Temperature

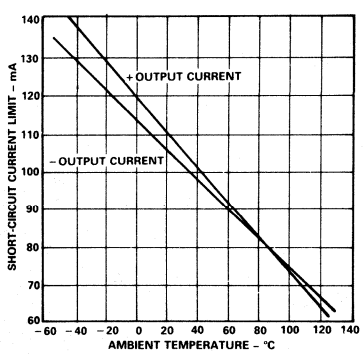


Figure 8. Short-Circuit Current Limit vs. Temperature

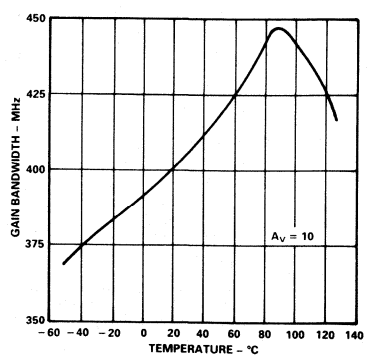


Figure 9. Gain Bandwidth Product vs. Temperature

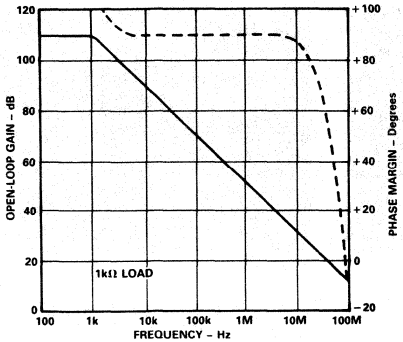


Figure 10. Open-Loop Gain and Phase Margin Phase vs. Frequency

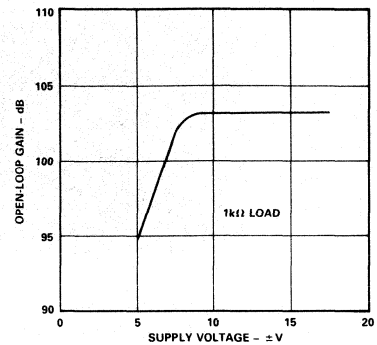


Figure 11. Open-Loop Gain vs. Supply Voltage

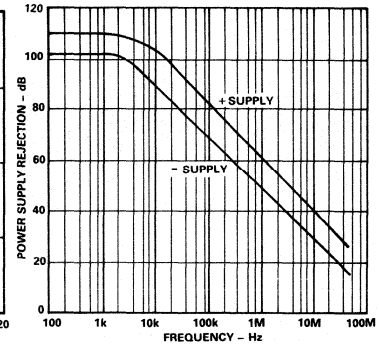


Figure 12. Power Supply Rejection vs. Frequency

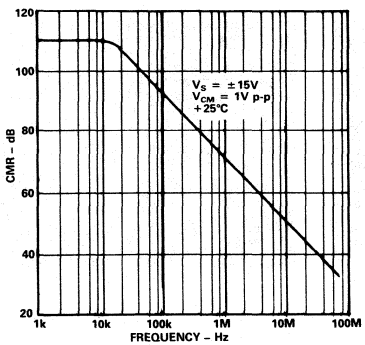


Figure 13. Common-Mode Rejection vs. Frequency

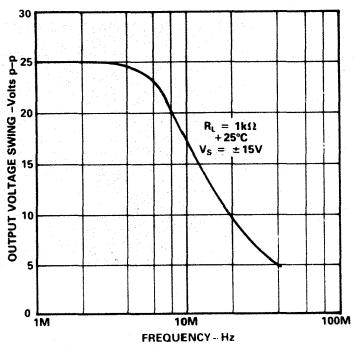


Figure 14. Large Signal Frequency Response

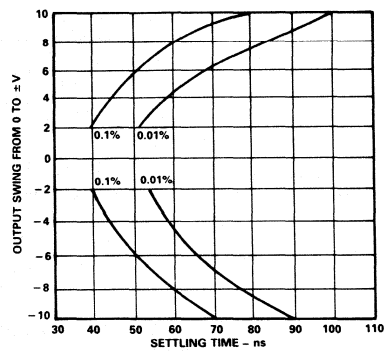


Figure 15. Output Swing and Error vs. Settling Time

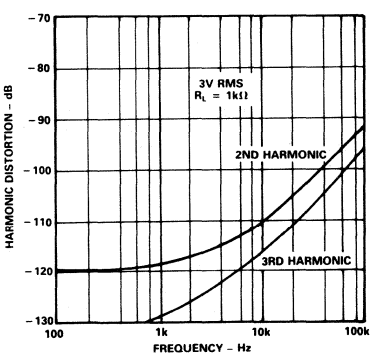


Figure 16. Harmonic Distortion vs. Frequency

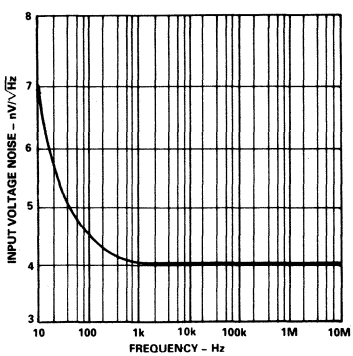


Figure 17. Input Voltage Noise Spectral Density

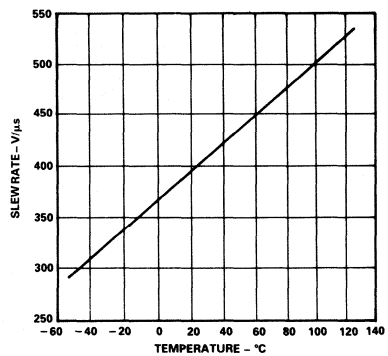


Figure 18. Slew Rate vs. Temperature

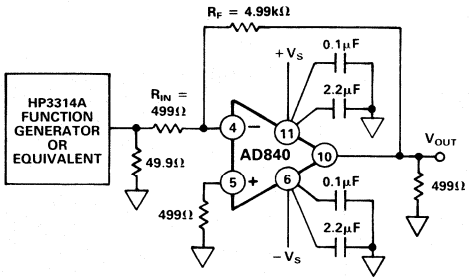


Figure 19a. Inverting Amplifier Configuration (DIP Pinout)

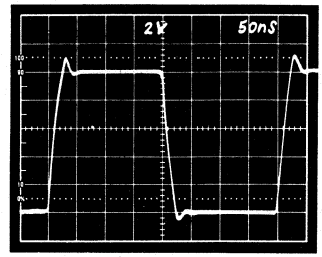


Figure 19b. Inverter Large Signal Pulse Response

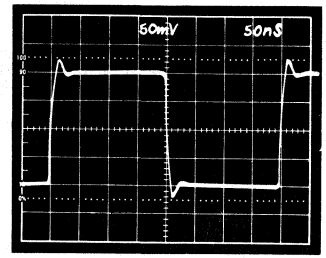


Figure 19c. Inverter Small Signal Pulse Response

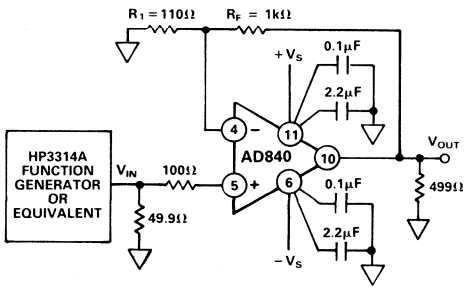


Figure 20a. Noninverting Amplifier Configuration (DIP Pinout)

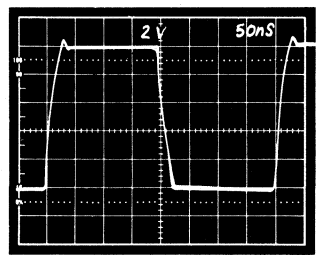


Figure 20b. Noninverting Large Signal Pulse Response

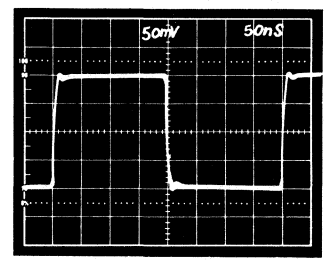


Figure 20c. Noninverting Small Signal Pulse Response

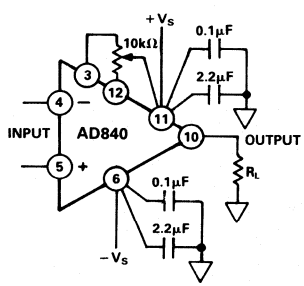


Figure 21. Offset Nulling (DIP Pinout)

OFFSET NULLING

The input offset voltage of the AD840 is very low for a high speed op amp, but if additional nulling is required, the circuit shown in Figure 21 can be used.

AD840 SETTLING TIME

Figures 22 and 24 show the settling performance of the AD840 in the test circuit shown in Figure 23.

Settling time is defined as:

> The interval of time from the application of an ideal step function input until the closed-loop amplifier output has entered and remains within a specified error band.

This definition encompasses the major components which comprise settling time. They include (1) propagation delay through the amplifier; (2) slewing time to approach the final output value; (3) the time of recovery from the overload associated with slewing; and (4) linear settling to within the specified error band.

Expressed in these terms, the measurement of settling time is obviously a challenge and needs to be done accurately to assure the user that the amplifier is worth consideration for the application.

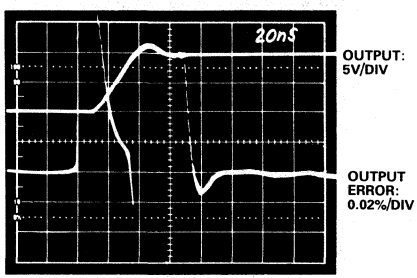


Figure 22. AD840 0.01% Settling Time

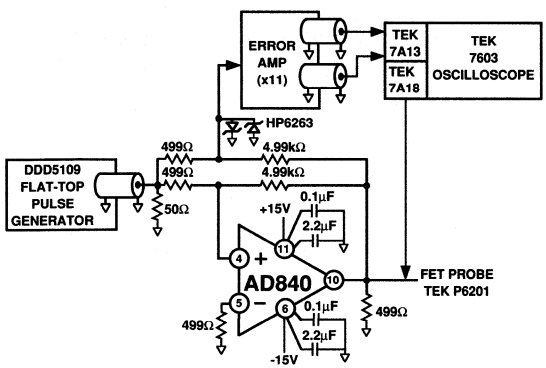


Figure 23. Settling Time Test Circuit

Figure 23 shows how measurement of the AD840's 0.01% settling in 100 ns was accomplished by amplifying the error signal from a false summing junction with a very high speed proprietary hybrid error amplifier specially designed to enable testing of small settling errors. The device under test was driving a 420 Ω load. The input to the error amp is clamped in order to avoid possible problems associated with the overdrive recovery of the oscilloscope input amplifier. The error amp amplifies the error from the false summing junction by 11, and it contains a gain vernier to fine trim the gain.

Figure 24 shows the "long-term" stability of the settling characteristics of the AD840 output after a 10 V step. There is no evidence of settling tails after the initial transient recovery time. The use of a junction isolated process, together with careful layout, avoids these problems by minimizing the effects of transistor isolation capacitance discharge and thermally induced shifts in circuit operating points. These problems do not occur even under high output current conditions.

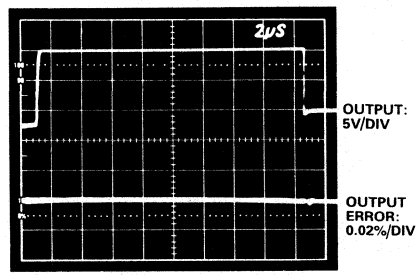


Figure 24. AD840 Settling Demonstrating No Settling Tails

GROUNDING AND BYPASSING

In designing practical circuits with the AD840, the user must remember that whenever high frequencies are involved, some special precautions are in order. Circuits must be built with short interconnect leads. Large ground planes should be used whenever possible to provide a low resistance, low inductance circuit path, as well as minimizing the effects of high frequency coupling. Sockets should be avoided, because the increased inter-lead capacitance can degrade bandwidth.

Feedback resistors should be of low enough value to assure that the time constant formed with the circuit capacitances will not limit the amplifier performance. Resistor values of less than 5 kΩ are recommended. If a larger resistor must be used, a small (±10 pF) feedback capacitor in connected parallel with the feedback resistor, R_F, may be used to compensate for these stray capacitances and optimize the dynamic performance of the amplifier in the particular application.

Power supply leads should be bypassed to ground as close as possible to the amplifier pins. A 2.2 μF capacitor in parallel with a 0.1 μF ceramic disk capacitor is recommended.

CAPACITIVE LOAD DRIVING ABILITY

Like all wideband amplifiers, the AD840 is sensitive to capacitive loading. The AD840 is designed to drive capacitive loads of up to 20 pF without degradation of its rated performance. Capacitive loads of greater than 20 pF will decrease the dynamic performance of the part although instability should not occur unless the load exceeds 100 pF. A resistor in series with the output can be used to decouple larger capacitive loads.

USING A HEAT SINK

The AD840 draws less quiescent power than most high speed amplifiers and is specified for operation without a heat sink. However, when driving low impedance loads the current to the load can be 4 to 5 times the quiescent current. This will create a noticeable temperature rise. Improved performance can be achieved by using a small heat sink such as the Aavid Engineering #602B.

HIGH SPEED DAC BUFFER CIRCUIT

The AD840's 100 ns settling time to 0.01% for a 10 V step makes it well suited as an output buffer for high speed D/A converters. Figure 25 shows the connections for producing a 0 to +10.24 V output swing from the AD568 35 ns DAC. With the AD568 in unbuffered voltage output mode, the AD840 is placed in noninverting configuration. As a result of the 1 kΩ span resistor provided internally in the AD568, the noise gain of this topology is 10. Only 5 pF is required across the feedback (span) resistor to optimize settling.

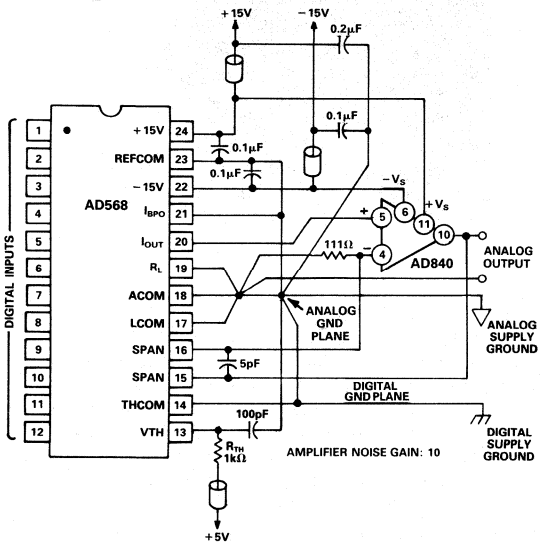


Figure 25. 0 to +10.24 V DAC Output Buffer

OVERDRIVE RECOVERY

Figure 26 shows the overdrive recovery capability of the AD840. Typical recovery time is 190 ns from negative overdrive and 350 ns from positive overdrive.

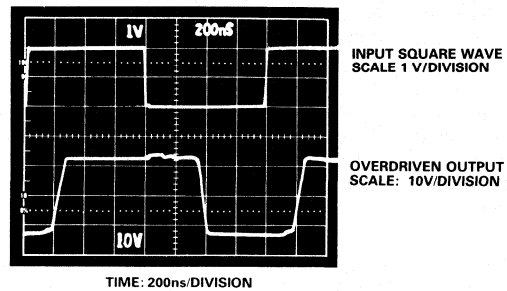


Figure 26. Overdrive Recovery

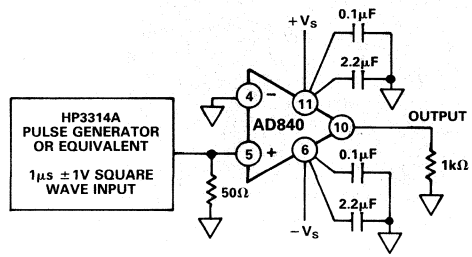


Figure 27. Overdrive Recovery Test Circuit

ANALOG DEVICES

Wideband, Unity-Gain Stable, Fast Settling Op Amp

AD841

FEATURES

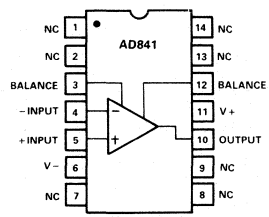
AC PERFORMANCE
- Unity-Gain Bandwidth: 40 MHz
- Fast Settling: 110 ns to 0.01%
- Slew Rate: 300 V/μs
- Full Power Bandwidth: 4.7 MHz for 20 V p–p into a 500 Ω Load

DC PERFORMANCE
- Input Offset Voltage: 1 mV max
- Input Voltage Noise: 13 nV/$\sqrt{Hz}$ typ
- Open-Loop Gain: 45 V/mV into a 1 kΩ Load
- Output Current: 50 mA min
- Supply Current: 12 mA max

APPLICATIONS
- High Speed Signal Conditioning
- Video and Pulse Amplifiers
- Data Acquisition Systems
- Line Drivers
- Active Filters
- Available in 14-Pin Plastic DIP, Hermetic Cerdip, 12-Pin TO-8 Metal Can and 20-Pin LCC Packages
- Chips and MIL-STD-883B Parts Available

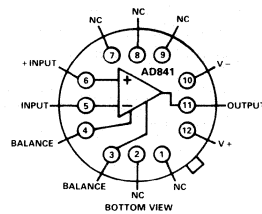
CONNECTION DIAGRAMS

Plastic DIP (N) Package and Cerdip (Q) Package



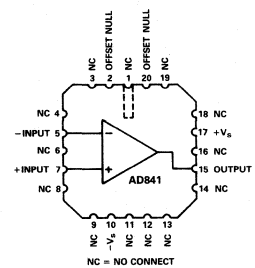
TOP VIEW
NC = NO CONNECT

TO-8 (H) Package



BOTTOM VIEW
NOTE: CAN TIED TO V+
NC = NO CONNECT

LCC (E) Package



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD841 is a member of the Analog Devices family of wide bandwidth operational amplifiers. This high speed/high precision family includes, among others, the AD840, which is stable at a gain of 10 or greater, and the AD842, which is stable at a gain of two or greater and has 100 mA minimum output current drive. These devices are fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. This process permits a combination of dc precision and wideband ac performance previously unobtainable in a monolithic op amp. In addition to its 40 MHz unity-gain bandwidth product, the AD841 offers extremely fast settling characteristics, typically settling to within 0.01% of final value in 110 ns for a 10 volt step.

Unlike many high frequency amplifiers, the AD841 requires no external compensation. It remains stable over its full operating temperature range. It also offers a low quiescent current of 12 mA maximum, a minimum output current drive capablity of 50 mA, a low input voltage noise of 13 nV/$\sqrt{Hz}$ and low input offset voltage of 1 mV maximum.

The 300 V/μs slew rate of the AD841, along with its 40 MHz gain bandwidth, ensures excellent performance in video and pulse amplifier applications. This amplifier is well suited for use in high frequency signal conditioning circuits and wide bandwidth active filters. The extremely rapid settling time of the AD841 makes it the preferred choice for data acquisition applications which require 12-bit accuracy. The AD841 is also appropriate for other applications such as high speed DAC and ADC buffer amplifiers and other wide bandwidth circuitry.

APPLICATION HIGHLIGHTS

1. The high slew rate and fast settling time of the AD841 make it ideal for DAC and ADC buffers, and all types of video instrumentation circuitry.
2. The AD841 is a precision amplifier. It offers accuracy to 0.01% or better and wide bandwidth performance previously available only in hybrids.
3. The AD841's thermally balanced layout and the speed of the CB process allow the AD841 to settle to 0.01% in 110 ns without the long "tails" that occur with other fast op amps.
4. Laser wafer trimming reduces the input offset voltage to 1 mV max on the K grade, thus eliminating the need for external offset nulling in many applications. Offset null pins are provided for additional versatility.
5. The AD841 is an enhanced replacement for the HA2541.

AD841—SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD841J Min	AD841J Typ	AD841J Max	AD841K Min	AD841K Typ	AD841K Max	AD841S Min	AD841S Typ	AD841S Max	Units
INPUT OFFSET VOLTAGE[1]			0.8	**2.0**		0.5	**1.0**		0.5	**2.0**	mV
	T_{min}–T_{max}			5.0			**3.3**			5.5	mV
Offset Drift			35			35			35		μV/°C
INPUT BIAS CURRENT			3.5	**8**		3.5	**5**		3.5	**8**	μA
	T_{min}–T_{max}			10			**6**			**12**	μA
Input Offset Current			0.1	**0.4**		0.1	**0.2**		0.1	**0.4**	μA
	T_{min}–T_{max}			0.5			**0.3**			**0.6**	μA
INPUT CHARACTERISTICS	Differential Mode										
Input Resistance			200			200			200		kΩ
Input Capacitance			2			2			2		pF
INPUT VOLTAGE RANGE											
Common Mode		**±10**	12		**±10**	12		**±10**	12		V
Common Mode Rejection	V_{CM} = ±10 V	**86**	100		**103**	109		**86**	100		dB
	T_{min}–T_{max}	80			**100**			80			dB
INPUT VOLTAGE NOISE	f = 1 kHz		15			15			15		nV/√Hz
Wideband Noise	10 Hz to 10 MHz		47			47			47		μV rms
OPEN-LOOP GAIN	V_O = ±10 V										
	R_{LOAD}≥500 Ω	**25**	45		**25**	45		**25**	45		V/mV
	T_{min}–T_{max}	12			**20**			**12**			V/mV
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD}≥500 Ω										
	T_{min}–T_{max}	±10			**±10**			**±10**			V
Current	V_{OUT} = ±10 V	**50**			**50**			**50**			mA
OUTPUT RESISTANCE	Open Loop		5			5			5		Ω
FREQUENCY RESPONSE											
Unity Gain Bandwidth	V_{OUT} = 90 mV p-p		40			40			40		MHz
Full Power Bandwidth[2]	V_O = 20 V p-p										
	R_{LOAD}≥500 Ω	3.1	4.7		3.1	4.7		3.1	4.7		MHz
Rise Time[3]	A_V = −1		10			10			10		ns
Overshoot[3]	A_V = −1		10			10			10		%
Slew Rate[3]	A_V = −1	200	300		200	300		200	300		V/μs
Settling Time – 10 V Step	A_V = −1										
	to 0.1%		90			90			90		ns
	to 0.01%		110			110			110		ns
OVERDRIVE RECOVERY	−Overdrive		200			200			200		ns
	+Overdrive		700			700			700		ns
DIFFERENTIAL GAIN	f = 4.4 MHz		0.03			0.03			0.03		%
Differential Phase	f = 4.4 MHz		0.022			0.022			0.022		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		**±5**		**±18**	**±5**		**±18**	**±5**		**±18**	V
Quiescent Current			11	**12**		11	**12**		11	**12**	mA
	T_{min}–T_{max}			14			**14**			**16**	mA
Power Supply Rejection Ratio	V_S = ±5 V to ±18 V	**86**	100		**90**	100		**86**	100		dB
	T_{min}–T_{max}	80			**86**			**80**			dB
TEMPERATURE RANGE											
Rated Performance[4]		0		+75	0		+75	−55		+125	°C
PACKAGE OPTIONS[5]											
LCC (E-20A)								AD841SE, AD841SE/883B			
Cerdip (Q-14)		AD841JQ			AD841KQ			AD841SQ, AD841SQ/883B			
Plastic (N-14)		AD841JN			AD841KN						
TO-8 (H-12)		AD841JH			AD841KH			AD841SH, AD841SH/883B			
Chips		AD841J CHIPS						AD841S CHIPS			

NOTES
[1]Input offset voltage specifications are guaranteed after 5 minutes at T_A = +25°C.
[2]Full power bandwidth = Slew Rate/2π V_{PEAK}.
[3]Refer to Figure 19.
[4]"S" grade T_{min} and T_{max} specifications are tested with automatic test equipment at T_A = −55°C and T_A = +125°C.
[5]For outline information see Package Information section.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
TO-8 (H) . . . . . 1.4 W
Plastic (N) . . . . . 1.5 W
Cerdip (Q) . . . . . 1.3 W
Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±6 V
Storage Temperature Range
Q, H, E . . . . . −65°C to +150°C
N . . . . . −65°C to +125°C
Junction Temperature . . . . . +175°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Maximum internal power dissipation is specified so that T_J does not exceed +175°C at an ambient temperature of +25°C.

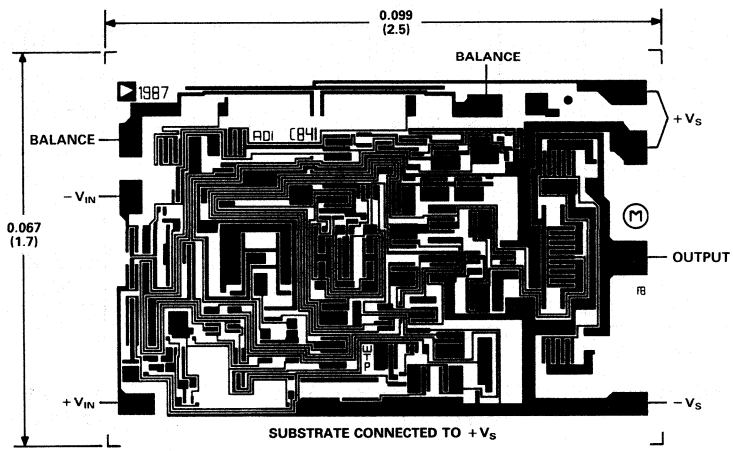
Thermal Characteristics:

	θ_{JC}	θ_{JA}	θ_{SA}	
Cerdip Package	35°C/W	110°C/W	38°C/W	Recommended Heat Sink:
TO-8 Package	30°C/W	100°C/W	37°C/W	Aavid Engineering ©#602B
Plastic Package	30°C/W	100°C/W		
LCC Package	35°C/W	150°C/W		

2

METALIZATION PHOTOGRAPHY

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



AD841—Typical Characteristics (at +25°C and V_S = ±15 V, unless otherwise noted)

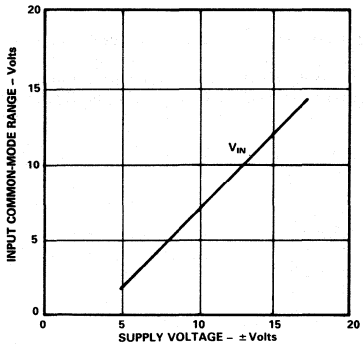


Figure 1. Input Common-Mode Range vs. Supply Voltage

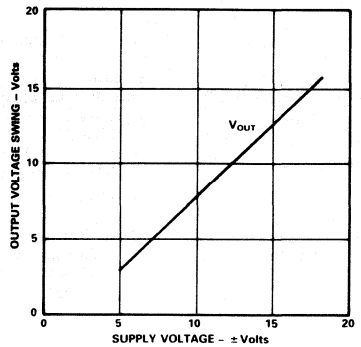


Figure 2. Output Voltage Swing vs. Supply Voltage

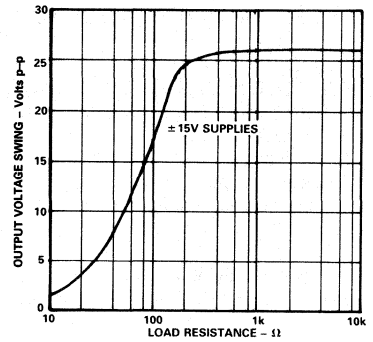


Figure 3. Output Voltage Swing vs. Load Resistance

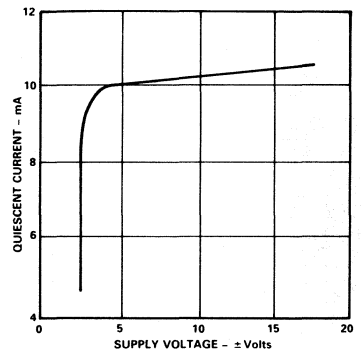


Figure 4. Quiescent Current vs. Supply Voltage

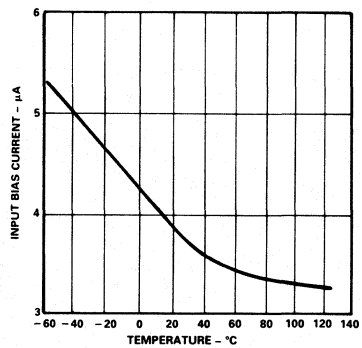


Figure 5. Input Bias Current vs. Temperature

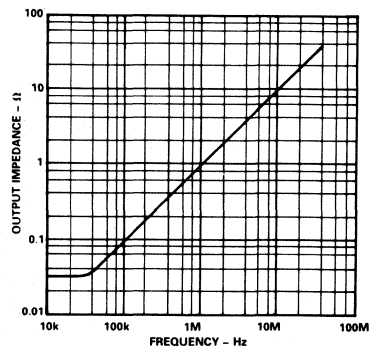


Figure 6. Output Impedance vs. Frequency

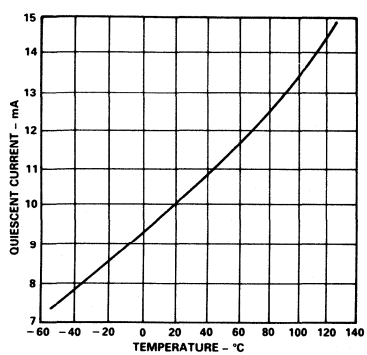


Figure 7. Quiescent Current vs. Temperature

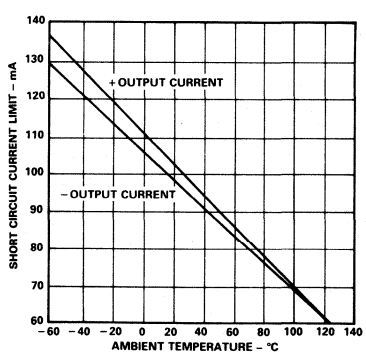


Figure 8. Short-Circuit Current Limit vs. Temperature

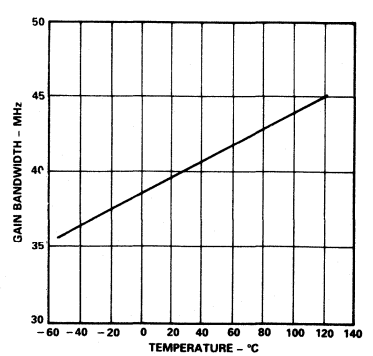


Figure 9. Gain Bandwidth Product vs. Temperature

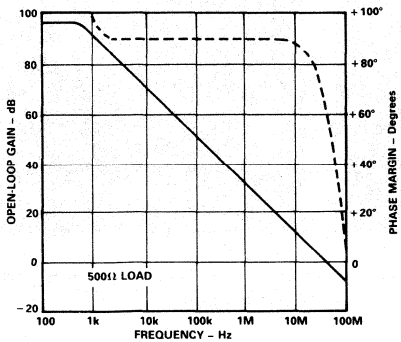


Figure 10. Open-Loop Gain and Phase Margin vs. Frequency

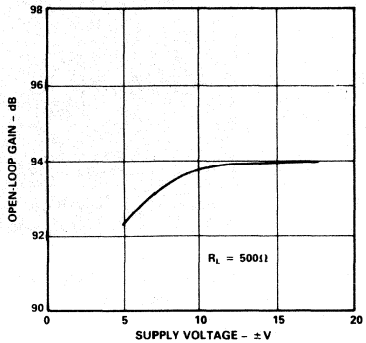


Figure 11. Open-Loop Gain vs. Supply Voltage

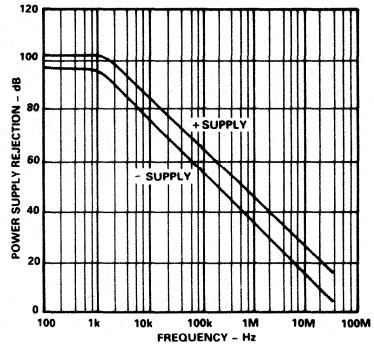


Figure 12. Power Supply Rejection vs. Frequency

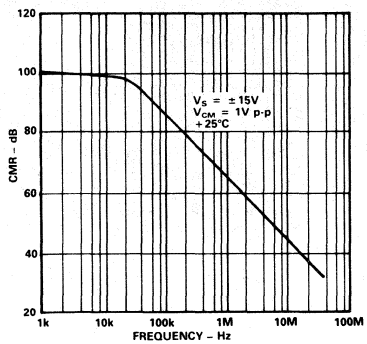


Figure 13. Common-Mode Rejection vs. Frequency

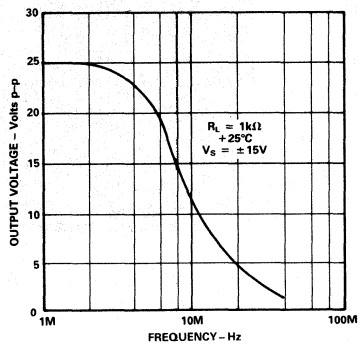


Figure 14. Large Signal Frequency Response

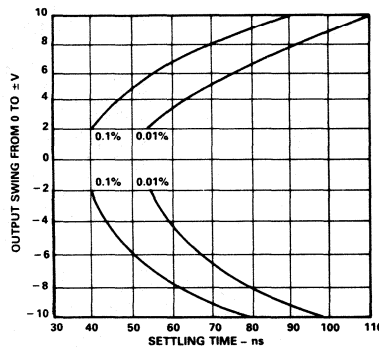


Figure 15. Output Swing and Error vs. Settling Time

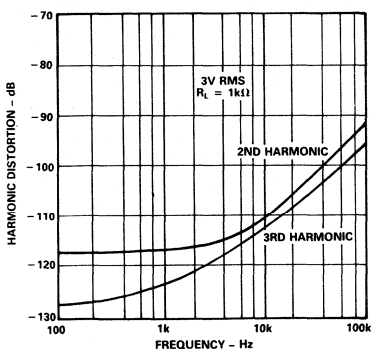


Figure 16. Harmonic Distortion vs. Frequency

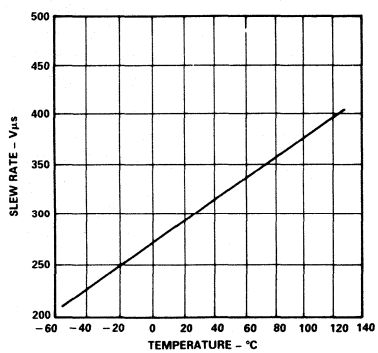


Figure 17. Slew Rate vs. Temperature

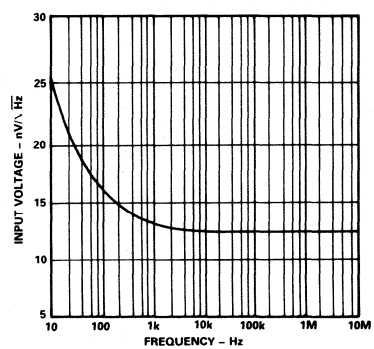


Figure 18. Input Noise Voltage Spectral Density

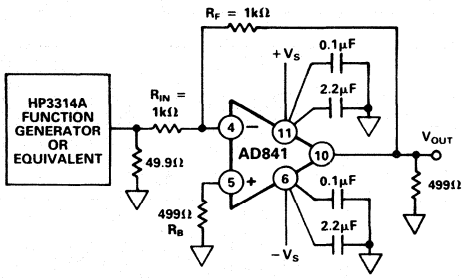


Figure 19a. Inverting Amplifier Configuration (DIP Pinout)

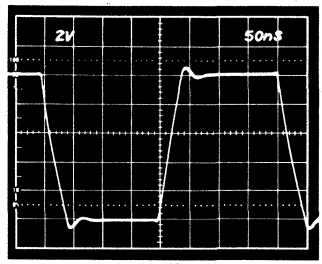


Figure 19b. Inverter Large Signal Pulse Response

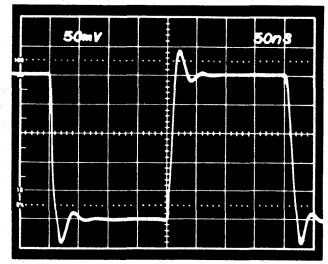


Figure 19c. Inverter Small Signal Pulse Response

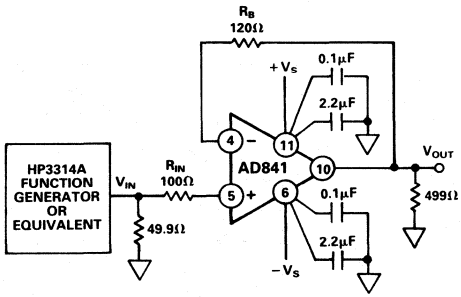


Figure 20a. Unity-Gain Buffer Amplifier Configuration (DIP Pinout)

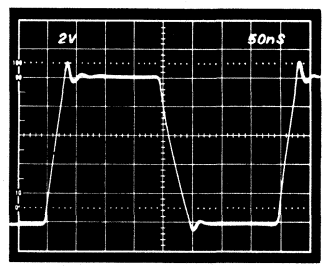


Figure 20b. Buffer Large Signal Pulse Response

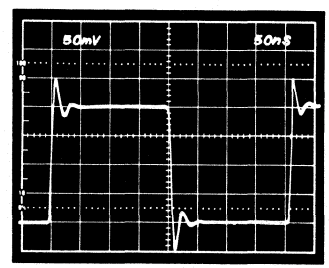


Figure 20c. Buffer Small Signal Pulse Response

OFFSET NULLING

The input offset voltage of the AD841 is very low for a high speed op amp, but if additional nulling is required, the circuit shown in Figure 21 can be used.

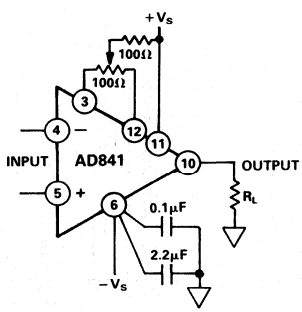


Figure 21. Offset Nulling (DIP Pinout)

INPUT CONSIDERATIONS

An input resistor (R_{IN} in Figure 20) is recommended in circuits where the input to the AD841 will be subjected to transient or continuous overload voltages exceeding the ±6 V maximum differential limit. This resistor provides protection for the input transistors by limiting the maximum current that can be forced into the input.

For high performance circuits it is recommended that a resistor (R_B in Figures 19 and 20) be used to reduce bias current errors by matching the impedance at each input. The output voltage error caused by the offset current is more than an order of magnitude less than the error present if the bias current error is not removed.

AD841 SETTLING TIME

Figures 22 and 24 show the settling performance of the AD841 in the test circuit shown in Figure 23.

Settling time is defined as:

> The interval of time from the application of an ideal step function input until the closed-loop amplifier output has entered and remains within a specified error band.

This definition encompasses the major components which comprise settling time. They include (1) propagation delay through the amplifier; (2) slewing time to approach the final output value; (3) the time of recovery from the overload associated with slewing and (4) linear settling to within the specified error band.

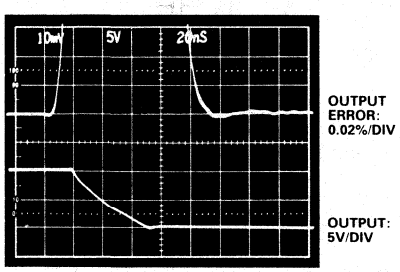


Figure 22. AD841 0.01% Settling Time

Expressed in these terms, the measurement of settling time is obviously a challenge and needs to be done accurately to assure the user that the amplifier is worth consideration for the application.

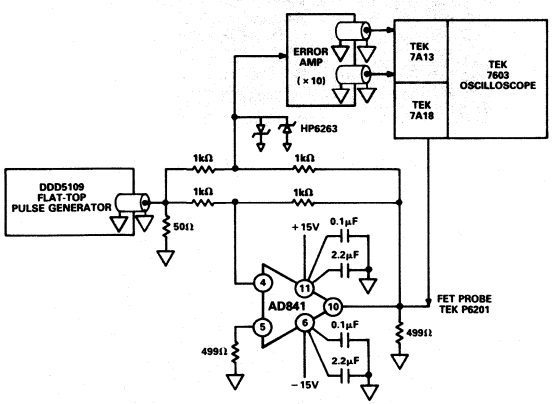


Figure 23. Settling Time Test Circuit

Measurement of the AD841's 0.01% settling in 110 ns was accomplished by amplifying the error signal from a false summing junction with a very high speed proprietary hybrid error amplifier specially designed to enable testing of small settling errors. The device under test was driving a 500 Ω load. The input to the error amp is clamped in order to avoid possible problems associated with the overdrive recovery of the oscilloscope input amplifier. The error amp gains the error from the false summing junction by 10, and it contains a gain vernier to fine trim the gain.

Figure 24 shows the "long term" stability of the settling characteristics of the AD841 output after a 10 V step. There is no evidence of settling tails after the initial transient recovery time. The use of a junction isolated process, together with careful layout, avoids these problems by minimizing the effects of transistor isolation capacitance discharge and thermally induced shifts in circuit operating points. These problems do not occur even under high output current conditions.

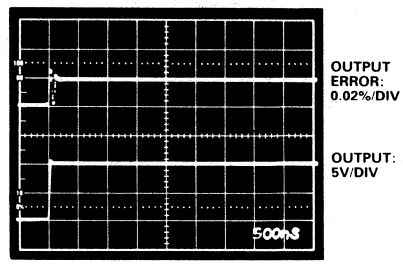


Figure 24. AD841 Settling Demonstrating No Settling Tails

GROUNDING AND BYPASSING

In designing practical circuits with the AD841, the user must remember that whenever high frequencies are involved, some special precautions are in order. Circuits must be built with short interconnect leads. Large ground planes should be used whenever possible to provide a low resistance, low inductance circuit path, as well as minimizing the effects of high frequency coupling. Sockets should be avoided because the increased interlead capacitance can degrade bandwidth.

Feedback resistors should be of low enough value to assure that the time constant formed with the circuit capacitances will not limit the amplifier performance. Resistor values of less than 5 kΩ are recommended. If a larger resistor must be used, a small (<10 pF) feedback capacitor in parallel with the feedback resistor, R_F, may be used to compensate for these stray capacitances and optimize the dynamic performance of the amplifier in the particular application.

Power supply leads should be bypassed to ground as close as possible to the amplifier pins. A 2.2 μF capacitor in parallel with a 0.1 μF ceramic disk capacitor is recommended.

CAPACITIVE LOAD DRIVING ABILITY

Like all wideband amplifiers, the AD841 is sensitive to capacitive loading. The AD841 is designed to drive capacitive loads of up to 20 pF without degradation of its rated performance. Capacitive loads of greater than 20 pF will decrease the dynamic performance of the part although instability should not occur unless the load exceeds 100 pF (for a unity-gain follower). A resistor in series with the output can be used to decouple larger capacitive loads.

Figure 25 shows a typical configuration for driving a large capacitive load. The 51 Ω output resistor effectively isolates the high frequency feedback from the load and stabilizes the circuit. Low frequency feedback is returned to the amplifier summing junction via the low pass filter formed by the 51 Ω resistor and the load capacitance, C_L.

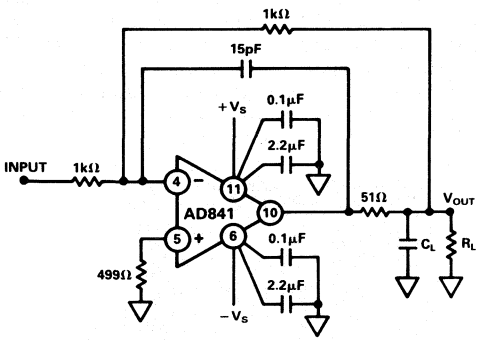


Figure 25. Circuit for Driving a Large Capacitive Load

USING A HEAT SINK

The AD841 draws less quiescent power than most precision high speed amplifiers and is specified for operation without a heat sink. However, when driving low impedance loads, the current to the load can be 4 to 5 times the quiescent current. This will create a noticeable temperature rise. Improved performance can be achieved by using a small heat sink such as the Aavid Engineering #602B.

TERMINATED LINE DRIVER

The AD841 functions very well as a high speed line driver of either terminated or unterminated cables. Figure 26 shows the AD841 driving a doubly terminated cable in a follower configuration. The AD841 maintains a typical slew rate of 300 V/μs, which means it can drive a ±10 V, 4.7 MHz signal or a ±3 V, 15.9 MHz signal.

The termination resistor, R_T, (when equal to the characteristic impedance of the cable) minimizes reflections from the far end of the cable. A back-termination resistor (R_{BT}, also equal to the characteristic impedance of the cable) may be placed between the AD841 output and the cable in order to damp any stray signals caused by a mismatch between R_T and the cable's characteristic impedance.This will result in a "cleaner" signal, but since 1/2 the output voltage will be dropped across R_{BT}, the op amp must supply double the output signal required if there is no back termination. Therefore the full power bandwidth is cut in half.

If termination is not used, cables appear as capacitive loads. If this capacitive load is large, it should be decoupled from the AD841 by a resistor in series with the output (see above: Driving a Capacitive Load).

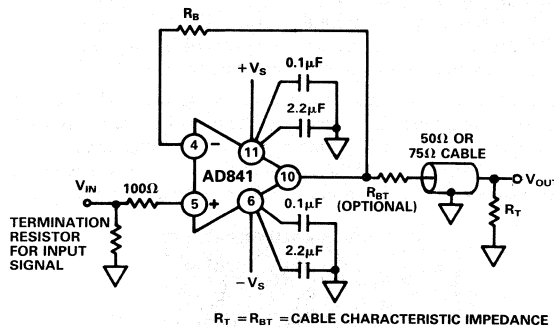


Figure 26. Line Driver Configuration

OVERDRIVE RECOVERY

Figure 27 shows the overdrive recovery capability of the AD841. Typical recovery time is 200 ns from negative overdrive and 700 ns from positive overdrive.

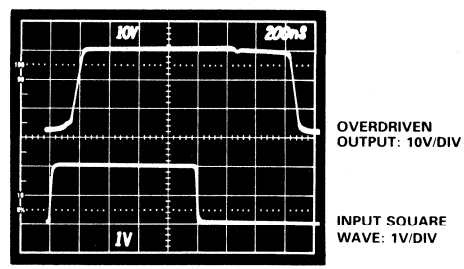


Figure 27. Overdrive Recovery

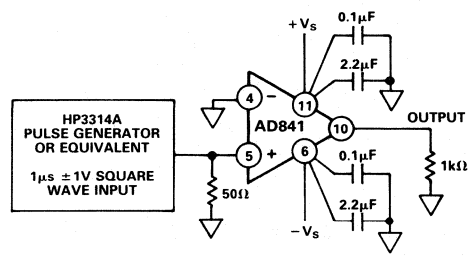


Figure 28. Overdrive Recovery Test Circuit

Wideband, High Output Current, Fast Settling Op Amp

AD842

FEATURES

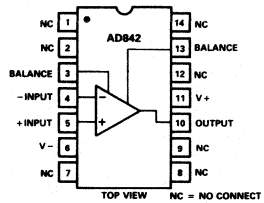
AC PERFORMANCE
- Gain Bandwidth Product: 80 MHz (Gain = 2)
- Fast Settling: 100 ns to 0.01% for a 10 V Step
- Slew Rate: 375 V/μs
- Stable at Gains of 2 or Greater
- Full Power Bandwidth: 6.0 MHz for 2

DC PERFORMANCE
- Input Offset Voltage: 1 mV max
- Input Offset Drift: 14 μV/°C
- Input Voltage Noise: 9 nV/$\sqrt{Hz}$ typ
- Open-Loop Gain: 90 V/mV into a 500 Ω Load
- Output Current: 100 mA min
- Quiescent Supply Current: 14 mA max

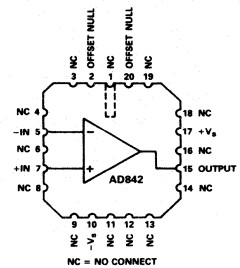
APPLICATIONS
- Line Drivers
- DAC and ADC Buffers
- Video and Pulse Amplifiers
- Available in Plastic DIP, Hermetic Metal Can, Hermetic Cerdip, SOIC and LCC Packages and in Chip Form
- MIL-STD-883B Parts Available
- Available in Tape and Reel in Accordance with EIA-481A Standard

CONNECTION DIAGRAMS

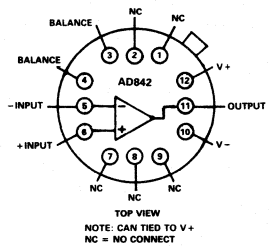
Plastic DIP (N) Package and Cerdip (Q) Package



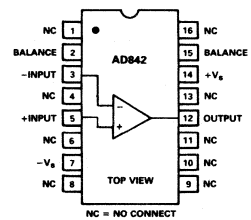
LCC (E) Package



TO-8 (H) Package



SOIC (R-16) Package



PRODUCT DESCRIPTION

The AD842 is a member of the Analog Devices family of wide bandwidth operational amplifiers. This family includes, among others, the AD840 which is stable at a gain of 10 or greater and the AD841 which is unity-gain stable. These devices are fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. This process permits a combination of dc precision and wideband ac performance previously unobtainable in a monolithic op amp. In addition to its 80 MHz gain bandwidth, the AD842 offers extremely fast settling characteristics, typically settling to within 0.01% of final value in less than 100 ns for a 10 volt step.

The AD842 also offers a low quiescent current of 13 mA, a high output current drive capability (100 mA minimum), a low input voltage noise of 9 nV$\sqrt{Hz}$ and a low input offset voltage (1 mV maximum).

The 375 V/μs slew rate of the AD842, along with its 80 MHz gain bandwidth, ensures excellent performance in video and pulse amplifier applications. This amplifier is ideally suited for use in high frequency signal conditioning circuits and wide bandwidth active filters. The extremely rapid settling time of the AD842 makes this amplifier the preferred choice for data acquisition applications which require 12-bit accuracy. The AD842 is also appropriate for other applications such as high speed DAC and ADC buffer amplifiers and other wide bandwidth circuitry.

APPLICATION HIGHLIGHTS

1. The high slew rate and fast settling time of the AD842 make it ideal for DAC and ADC buffers amplifiers, lines drivers and all types of video instrumentation circuitry.
2. The AD842 is a precision amplifier. It offers accuracy to 0.01% or better and wide bandwidth; performance previously available only in hybrids.
3. Laser-wafer trimming reduces the input offset voltage of 1 mV max, thus eliminating the need for external offset nulling in many applications.
4. Full differential inputs provide outstanding performance in all standard high frequency op amp applications where the circuit gain will be 2 or greater.
5. The AD842 is an enhanced replacement for the HA2542.

AD842—SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD842J/JR[1] Min	AD842J/JR[1] Typ	AD842J/JR[1] Max	AD842K Min	AD842K Typ	AD842K Max	AD842S Min	AD842S Typ	AD842S Max	Units
INPUT OFFSET VOLTAGE[2]			0.5	1.5		0.3	1.0		0.5	1.5	mV
	T_{min}–T_{max}			2.5/3			1.5			3.5	mV
Offset Drift			14			14			14		µV/°C
INPUT BIAS CURRENT			4.2	8		3.5	5		4.2	8	µA
	T_{min}–T_{max}			10			6			12	µA
Input Offset Current			0.1	0.4		0.05	0.2		0.1	0.4	µA
	T_{min}–T_{max}			0.5			0.3			0.6	µA
INPUT CHARACTERISTICS											
Input Resistance	Differential Mode		100			100			100		kΩ
Input Capacitance			2.0			2.0			2.0		pF
INPUT VOLTAGE RANGE											
Common Mode		±10			±10			±10			V
Common-Mode Rejection	V_{CM} = ±10 V	86	115		90	115		86	115		dB
	T_{min}–T_{max}	80			86			80			dB
INPUT VOLTAGE NOISE	f = 1 kHz		9			9			9		nV/√Hz
Wideband Noise	10 Hz to 10 MHz		28			28			28		µV rms
OPEN-LOOP GAIN	V_O = ±10 V										
	R_{LOAD}≥500 Ω	40/30	90		50	90		40	90		V/mV
	T_{min}–T_{max}	20/15			25			20			V/mV
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD}≥500 Ω	±10			±10			±10			V
Current	V_{OUT} = ±10 V	100			100			100			mA
	Open Loop		5			5			5		Ω
FREQUENCY RESPONSE											
Gain Bandwidth Product	V_{OUT} = 90 mV		80			80			80		MHz
Full Power Bandwidth[3]	V_O = 20 V p-p										
	R_{LOAD}≥500 Ω	4.7	6		4.7	6		4.7	6		MHz
Rise Time[4]	A_{VCL} = −2		10			10			10		ns
Overshoot[4]	A_{VCL} = −2		20			20			20		%
Slew Rate[4]	A_{VCL} = −2	300	375		300	375		300	375		V/µs
Settling Time[4]	10 V Step										
	to 0.1%		80			80			80		ns
	to 0.01%		100			100			100		ns
Differential Gain	f = 4.4 MHz		0.015			0.015			0.015		%
Differential Phase	f = 4.4 MHz		0.035			0.035			0.035		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		±5		±18	±5		±18	±5		±18	V
Quiescent Current			13/14	14/16		13	14		13	14	mA
	T_{min}–T_{max}			16/19.5			16			19	mA
Power Supply Rejection Ratio	V_S = ±5 V to ±15 V	86	100		90	105		86	100		dB
	T_{min}–T_{max}	80			86			80			dB
TEMPERATURE RANGE											
Rated Performance[5]		0		+75	0		+75	−55		+125	°C
PACKAGE OPTIONS[6]											
Plastic (N-14)			AD842JN			AD842KN					
Cerdip (Q-14)			AD842JQ			AD842KQ			AD842SQ, AD842SQ/883B		
SOIC (R-16)			AD842JR								
Tape and REEL			AD842JR-REEL								
TO-8 (H-12A)			AD842JH			AD842KH			AD842SH		
LCC (E-20A)									AD842SE/883B		
Chips			AD842J Chips						AD842S Chips		

NOTES

[1]AD842JR specifications differ from those of the AD842JN, JQ and JH due to the thermal characteristics of the SOIC package.

[2]Input offset voltage specifications are guaranteed after 5 minutes at T_A = +25°C.

[3]FPBW Slew Rate/2π V_{PEAK}.

[4]Refer to Figures 22 and 23.

[5]"S" grade T_{min} and T_{max} specifications are tested with automatic test equipment at T_A = −55°C and T_A = +125°C.

[6]For outline information see Package Information section.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
Plastic (N) . . . . . 1.5 W
Cerdip (Q) . . . . . 1.1 W
TO-8 (H) . . . . . 1.3 W
SOIC (R) . . . . . 1.3 W
Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±6 V
Storage Temperature Range
(Q, H) . . . . . −65°C to +150°C
(N, R) . . . . . −65°C to +125°C
Junction Temperature . . . . . +175°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Maximum internal power dissipation is specified so that T_J does not exceed +150°C at an ambient temperature of +25°C.

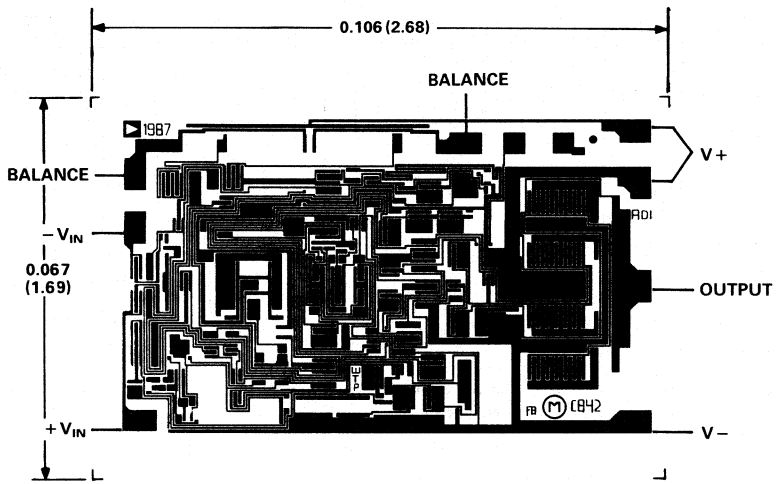
Thermal Characteristics:

	θ_{JC}	θ_{JA}	θ_{SA}
Plastic Package	30°C/W	100°C/W	
Cerdip Package	30°C/W	110°C/W	38°C/W
TO-8 Package	30°C/W	100°C/W	27°C/W
16-Pin SOIC Package	30°C/W	100°C/W	
20-Pin LCC Package	35°C/W	150°C/W	

Recommended heat sink: Aavid Engineering© #602B

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



AD842—Typical Characteristics (at +25°C and V_S = ±15 V, unless otherwise noted.)

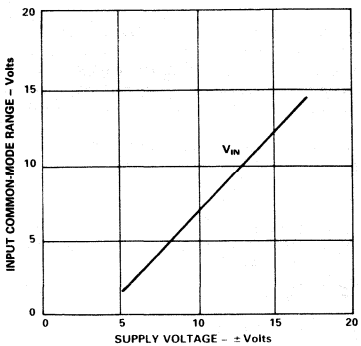


Figure 1. Input Common-Mode Range vs. Supply Voltage

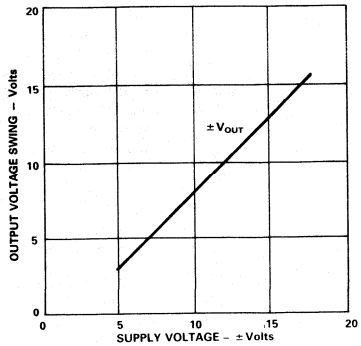


Figure 2. Output Voltage Swing vs. Supply Voltage

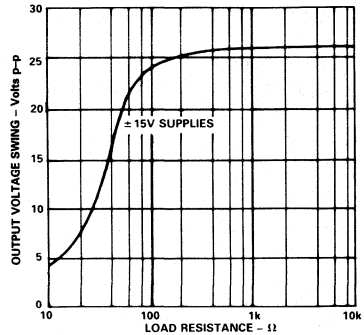


Figure 3. Output Voltage Swing vs. Load Resistance

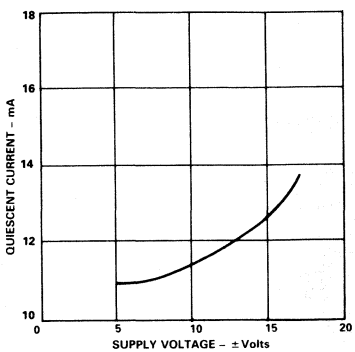


Figure 4. Quiescent Current vs. Supply Voltage

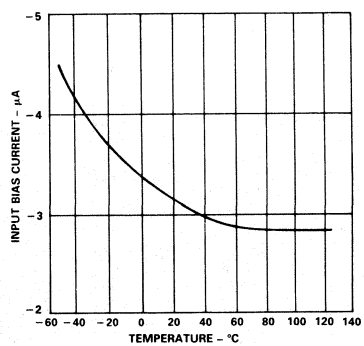


Figure 5. Input Bias Current vs. Temperature

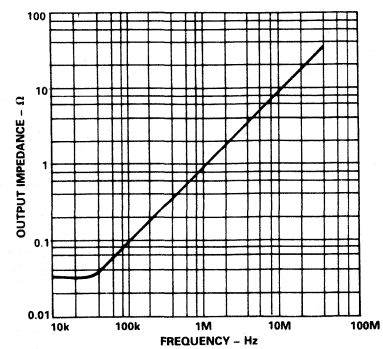


Figure 6. Output Impedance vs. Frequency

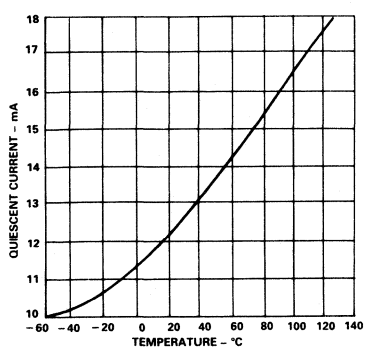


Figure 7. Quiescent Current vs. Temperature

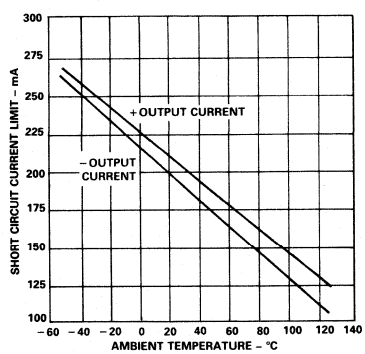


Figure 8. Short-Circuit Current Limit vs. Temperature

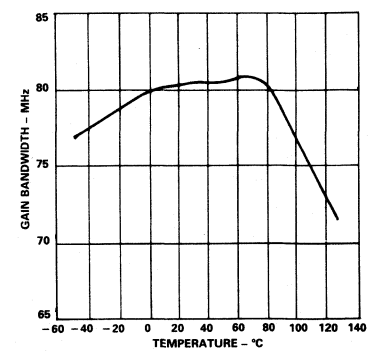


Figure 9. Gain Bandwidth Product vs. Temperature

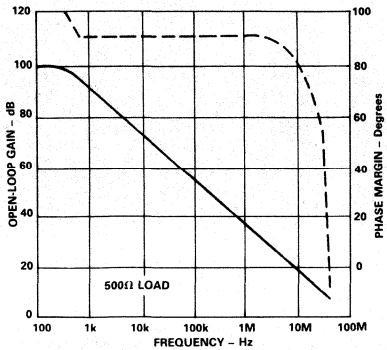


Figure 10. Open-Loop Gain and Phase Margin vs. Frequency

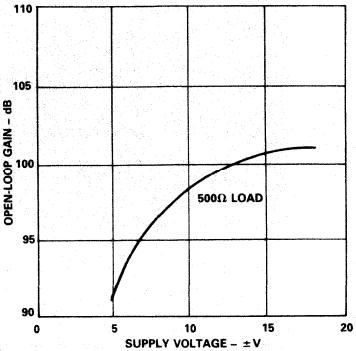


Figure 11. Open-Loop Gain vs. Supply Voltage

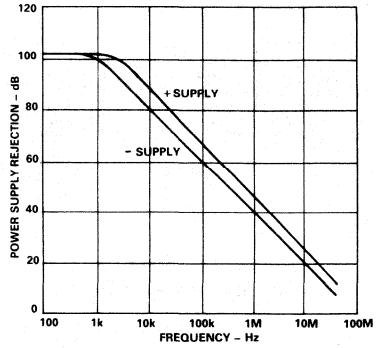


Figure 12. Power Supply Rejection vs. Frequency

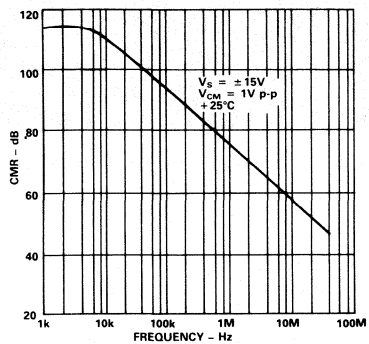


Figure 13. Common-Mode Rejection vs. Frequency

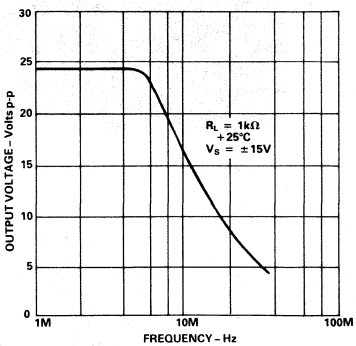


Figure 14. Large Signal Frequency Response

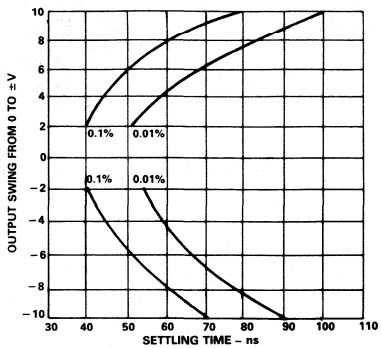


Figure 15. Output Swing and Error vs. Settling Time

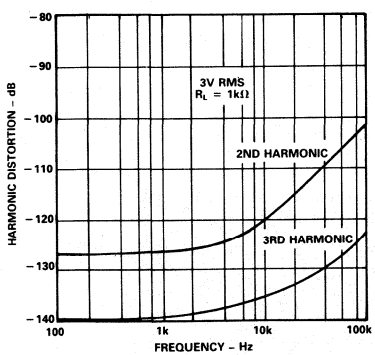


Figure 16. Harmonic Distortion vs. Frequency

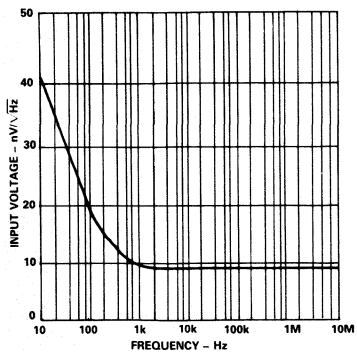


Figure 17. Input Voltage vs. Frequency

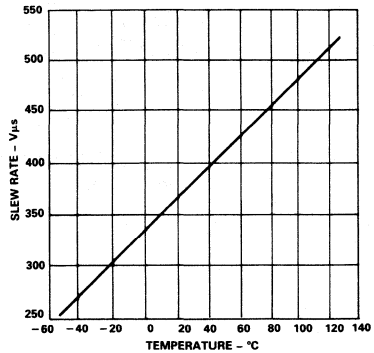


Figure 18. Slew Rate vs. Temperature

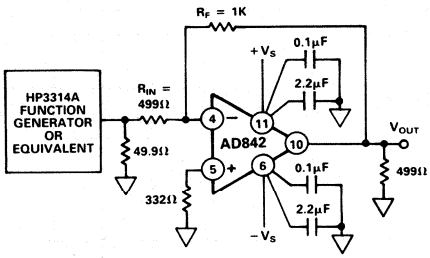


Figure 19a. Inverting Amplifier Configuration (DIP Pinout)

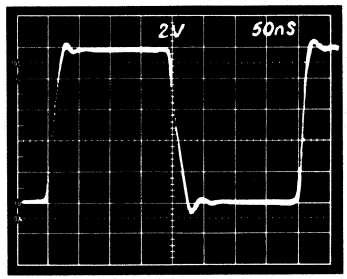


Figure 19b. Inverter Large Signal Pulse Response

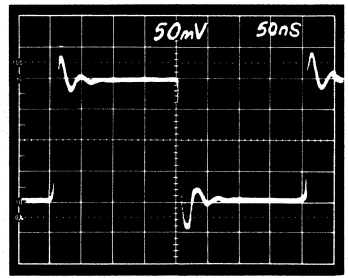


Figure 19c. Inverter Small Signal Pulse Response

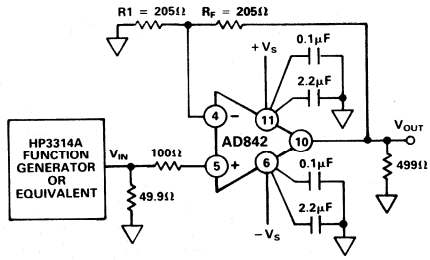


Figure 20a. Noninverting Amplifier Configuration (DIP Pinout)

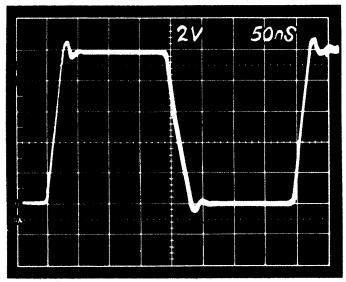


Figure 20b. Noninverting Large Signal Pulse Response

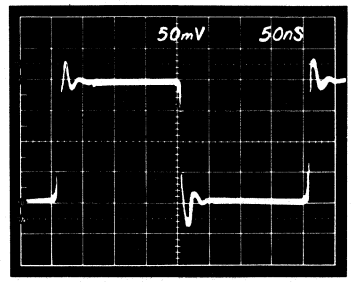


Figure 20c. Noninverting Small Signal Pulse Response

OFFSET NULLING

The input offset voltage of the AD842 is very low for a high speed op amp, but if additional nulling is required, the circuit shown in Figure 21 can be used.

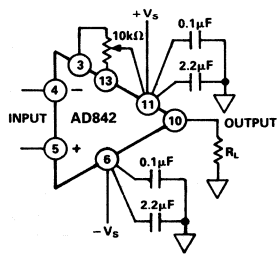


Figure 21. Offset Nulling (DIP Pinout)

AD842 SETTLING TIME

Figures 22 and 24 show the settling performance of the AD842 in the test circuit shown in Figure 23.

Settling time is defined as:

> The interval of time from the application of an ideal step function input until the closed-loop amplifier output has entered and remains within a specified error band.

This definition encompasses the major components which comprise settling time. They include: (1) propagation delay through the amplifier; (2) slewing time to approach the final output value; (3) the time of recovery from the overload associated with slewing; and (4) linear settling to within the specified error band.

Expressed in these terms, the measurement of settling time is obviously a challenge and needs to be done accurately to assure the user that the amplifier is worth consideration for the application.

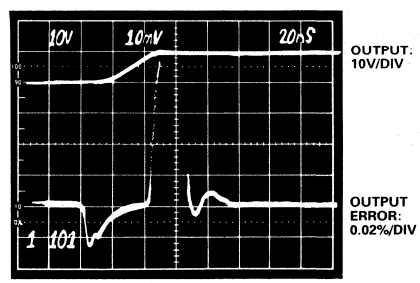


Figure 22. AD842 0.01% Settling Time

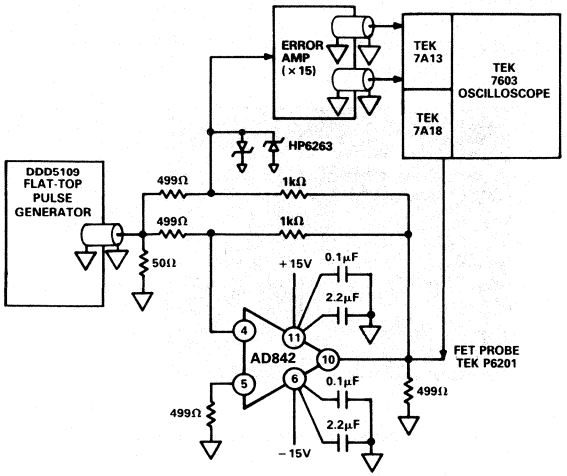


Figure 23. Settling Time Test Circuit

Figure 23 shows how measurement of the AD842's 0.01% settling in 100 ns was accomplished by amplifying the error signal from a false summing junction with a very high-speed proprietary hybrid error amplifier specially designed to enable testing of small settling errors. The device under test was driving a 300 Ω load. The input to the error amp is clamped in order to avoid possible problems associated with the overdrive recovery of the oscilloscope input amplifier. The error amp gains the error from the false summing junction by 15, and it contains a gain vernier to fine trim the gain.

Figure 24 shows the "long term" stability of the settling characteristics of the AD842 output after a 10 V step. There is no evidence of settling tails after the initial transient recovery time. The use of a junction isolated process, together with careful layout, avoids these problems by minimizing the effects of transistor isolation capacitance discharge and thermally induced shifts in circuit operating points. These problems do not occur even under high output current conditions.

GROUNDING AND BYPASSING

In designing practical circuits with the AD842, the user must remember that whenever high frequencies are involved, some special precautions are in order. Circuits must be built with short interconnect leads. Large ground planes should be used whenever possible to provide a low resistance, low inductance circuit path, as well as minimizing the effects of high frequency coupling. Sockets should be avoided because the increased interlead capacitance can degrade bandwidth.

Feedback resistors should be of low enough value to assure that the time constant formed with the circuit capacitances will not limit the amplifier performance. Resistor values of less than 5 kΩ are recommended. If a larger resistor must be used, a small (<10 pF) feedback capacitor connected in parallel with the feedback resistor, R_F, may be used to compensate for these stray capacitances and optimize the dynamic performance of the amplifier in the particular application.

Power supply leads should be bypassed to ground as close as possible to the amplifier pins. A 2.2 μF capacitor in parallel with a 0.1 μF ceramic disk capacitor is recommended.

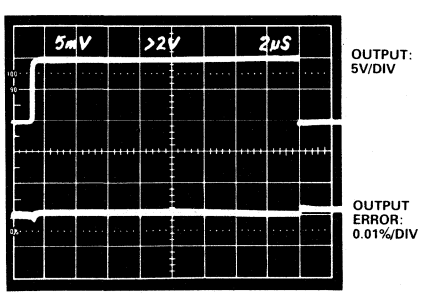


Figure 24. AD842 Settling Demonstrating No Settling Tails

CAPACITIVE LOAD DRIVING ABILITY

Like all wideband amplifiers, the AD842 is sensitive to capacitive loading. The AD842 is designed to drive capacitive loads of up to 20 pF without degradation of its rated performance. Capacitive loads of greater than 20 pF will decrease the dynamic performance of the part although instability should not occur unless the load exceeds 100 pF.

USING A HEAT SINK

The AD842 draws less quiescent power than most precision high speed amplifiers and is specified for operation without a heat sink. However, when driving low impedance loads, the current to the load can be 10 times the quiescent current. This will create a noticeable temperature rise. Improved performance can be achieved by using a small heat sink such as the Aavid Engineering #602B.

TERMINATED LINE DRIVER

The AD842 is optimized for high speed line driver applications. Figure 25 shows the AD842 driving a doubly terminated cable in a gain-of-2 follower configuration. The AD842 maintains a typical slew rate of 375 V/μs, which means it can drive a ±10 V, 6.0 MHz signal or a ±3 V, 19.9 MHz signal.

The termination resistor, R_T, (when equal to the characteristic impedance of the cable) minimizes reflections from the far end of the cable. A back-termination resistor (R_{BT}, also equal to the characteristic impedance of the cable) may be placed between the AD842 output and the cable in order to damp any stray signals caused by a mismatch between R_T and the cable's characteristic impedance. This will result in a "cleaner" signal. With this circuit, the voltage on the line equals V_{IN} because one half of V_{OUT} is dropped across R_{BT}.

The AD842 has ±100 mA minimum output current and, therefore, can drive ±5 V into a 50 Ω cable.

The feedback resistors, R_1 and R_2, must be chosen carefully. Large value resistors are desirable in order to limit the amount of current drawn from the amplifier output. But large resistors can cause amplifier instability because the parallel resistance $R_1 \| R_2$ combines with the input capacitance (typically 2–5 pF) to create an additional pole. Also, the voltage noise of the AD842 is equivalent to a 5 kΩ resistor, so large resistors can significantly increase the system noise. Resistor values of 1 kΩ or 2 kΩ are recommended.

If termination is not used, cables appear as capacitive loads and can be decoupled from the AD842 by a resistor in series with the output.

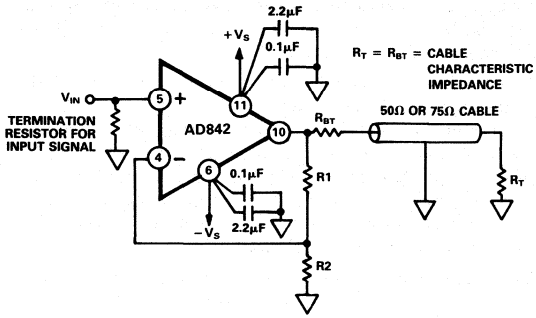


Figure 25. Line Driver Configuration

OVERDRIVE RECOVERY

Figure 26 shows the overdrive recovery capability of the AD842. Typical recovery time is 80 ns from negative overdrive and 400 ns from positive overdrive.

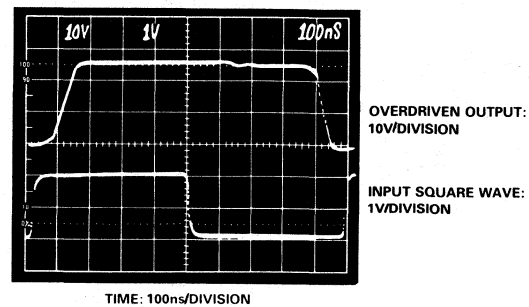


Figure 26. Overdrive Recovery

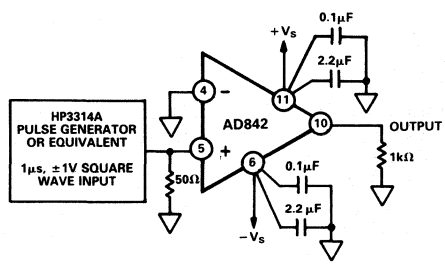


Figure 27. Overdrive Recovery Test Circuit

34 MHz, CBFET Fast Settling Op Amp

AD843

FEATURES

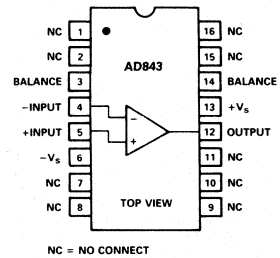
AC PERFORMANCE
- Unity Gain Bandwidth: 34 MHz
- Fast Settling: 135 ns to 0.01%
- Slew Rate: 250 V/μs
- Stable at Gains of 1 or Greater
- Full Power Bandwidth: 3.9 MHz

DC PERFORMANCE
- Input Offset Voltage: 1 mV max (AD843K/B)
- Input Bias Current: 0.6 nA typ
- Input Voltage Noise: 19 nV/$\sqrt{Hz}$
- Open Loop Gain: 30 V/mV into a 500 Ω Load
- Output Current: 50 mA min
- Supply Current: 13 mA max
- Available in 8-Pin Plastic Mini-DIP & Cerdip, 16-Pin SOIC, 20-Pin LCC and 12-Pin Hermetic Metal Can Packages
- Available in Tape and Reel in Accordance with EIA-481A Standard
- Chips and MIL-STD-883B Parts Also Available

APPLICATIONS
- High Speed Sample-and-Hold Amplifiers
- High Bandwidth Active Filters
- High Speed Integrators
- High Frequency Signal Conditioning

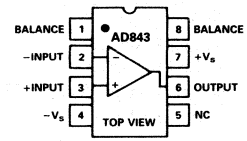
CONNECTION DIAGRAMS

16-Pin SOIC (R-16) Package



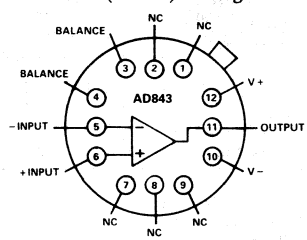
NC = NO CONNECT

Plastic (N-8) and Cerdip (Q-8) Package



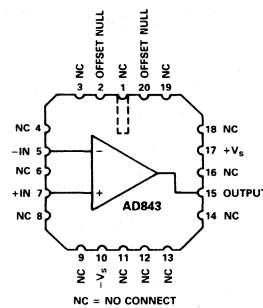
NC = NO CONNECT

T0–8 (H-12A) Package



NOTE: CAN TIED TO V+
NC = NO CONNECT

LCC (E-20A) Package



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD843 is a fast settling, 34 MHz, CBFET input op amp. The AD843 combines the low (0.6 nA) input bias currents characteristic of a FET input amplifier while still providing a 34 MHz bandwidth and a 135 ns settling time (to within 0.01% of final value for a 10 volt step). The AD843 is a member of the Analog Devices' family of wide bandwidth operational amplifiers. These devices are fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. This process permits a combination of dc precision and wideband ac performance previously unobtainable in a monolithic op amp.

The 250 V/μs slew rate and 0.6 nA input bias current of the AD843 ensure excellent performance in high speed sample-and-hold applications and in high speed integrators. This amplifier is also ideally suited for high bandwidth active filters and high frequency signal conditioning circuits.

Unlike many high frequency amplifiers, the AD843 requires no external compensation and it remains stable over its full operating temperature range. It is available in five performance grades: the AD843J and AD843K are rated over the commercial temperature range of 0°C to +70°C. The AD843A and AD843B are rated over the industrial temperature range of −40°C to +85°C. The AD843S is rated over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

The AD843 is offered in either 8-pin plastic DIP or hermetic cerdip packages, in 16-pin SOIC, 20-Pin LCC, or in a 12-pin metal can. Chips are also available.

PRODUCT HIGHLIGHTS

1. The high slew rate, fast settling time and low input bias current of the AD843 make it the ideal amplifier for 12-bit D/A and A/D buffers, for high speed sample-and-hold amplifiers and for high speed integrator circuits. The AD843 can replace many FET input hybrid amplifiers such as the LH0032, LH4104 and OPA600.
2. Fully differential inputs provide outstanding performance in all standard high frequency op amp applications such as signal conditioning and active filters.
3. Laser wafer trimming reduces the input offset voltage to 1 mV max (AD843K and AD843B).
4. Although external offset nulling is unnecessary in many applications, offset null pins are provided.
5. The AD843 does not require external compensation at closed loop gains of 1 or greater.

AD843—SPECIFICATIONS (@ T_A +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD843J/A Min	AD843J/A Typ	AD843J/A Max	AD843K/B Min	AD843K/B Typ	AD843K/B Max	AD843S Min	AD843S Typ	AD843S Max	Units
INPUT OFFSET VOLTAGE[1]			1.0	**2.0**		0.5	**1.0**		1.0	**2.0**	mV
	T_{min}–T_{max}		1.7	4.0		1.2	**2.0**		3.0	**4.5**	mV
Offset Drift			12			12	35		12		µV/°C
INPUT BIAS CURRENT	Initial (T_J = +25°C)		50			40			50		pA
	Warmed-Up[1]		0.8	**2.5**		0.6	**1.0**		0.8	**2.5**	nA
	T_{min}–T_{max}			60/160			23/65			2600	nA
INPUT OFFSET CURRENT	Initial (T_J = +25°C)		30			20			30		pA
	Warmed-Up[1]		0.25	**1.0**		0.2	**0.4**		0.25	**1.0**	nA
	T_{min}–T_{max}			23/64			9/26			1025	nA
INPUT CHARACTERISTICS											
Input Resistance			10^{10}			10^{10}			10^{10}		Ω
Input Capacitance			6			6			6		pF
INPUT VOLTAGE RANGE											
Common Mode		**±10**	+12, −13		**±10**	+12, −13		**±10**	+12, −13		V
COMMON MODE REJECTION	V_{CM} = ±10 V	**60**	72		**70**	76		**60**	72		dB
	T_{min}–T_{max}	60	72		**68**	76		**60**	72		dB
INPUT VOLTAGE NOISE	f = 10 kHz		19			19			19		nV/√Hz
Wideband Noise	10 Hz to 10 MHz		60			60			60		µV rms
OPEN LOOP GAIN	V_O = ±10 V										
	R_{LOAD}≥500 Ω	**15**	25		**20**	30		**15**	30		V/mV
	T_{min}–T_{max}	10	20		**10**	25		**10**	25		V/mV
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD}≥500 Ω	**±10**	+11.5, −12.6		**±10**	+11.5, −12.6		**±10**	+11.5, −12.6		V
Current	V_{OUT} = ±10 V	**50**			**50**			**50**			mA
Output Resistance	Open Loop		12			12			12		Ω
FREQUENCY RESPONSE											
Unity Gain Bandwidth	V_{OUT} = 90 mV p-p		34			34			34		MHz
Full Power Bandwidth[2]	V_O = 20 V p-p										
	Rl≥500 Ω	2.5	3.9		2.5	3.9		2.5	3.9		MHz
Rise Time	A_{VCL} = −1		10			10			10		ns
Overshoot	A_{VCL} = −1		15			15			15		%
Slew Rate	A_{VCL} = −1	160	250		160	250		160	250		V/µs
Settling Time	10 V Step										
	A_{VCL} = −1										
	to 0.1%		95			95			95		ns
	to 0.01%		135			135			135		ns
Overdrive Recovery	−Overdrive		200			200			200		ns
	+Overdrive		700			700			700		ns
Differential Gain	f = 4.4 MHz		0.025			0.025			0.025		%
Differential Phase	f = 4.4 MHz		0.025			0.025			0.025		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		**±4.5**		**±18**	**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current			12	**13**		12	**13**		12	**13**	mA
	T_{min}–T_{max}		12.3	14		12.3	**14**		12.5	**16**	mA
Rejection Ratio	±5 V to ±18 V	**65**	76		**70**	80		**65**	76		dB
Rejection Ratio	T_{min}–T_{max}	62	76		**68**	80		**62**	76		dB
TEMPERATURE RANGE											
Operating, Rated Performance											
Commercial (0 to +70°C)			AD843J			AD843K					
Industrial (−40°C to +85°C)			AD843A			AD843B					
Military (−55°C to +125°C)[3]									AD843S		
PACKAGE OPTIONS[4]											
Plastic (N-8)			AD843JN			AD843KN					
Cerdip (Q-8)			AD843AQ			AD843BQ			AD843SQ, AD843SQ/883B		
Metal Can (H-12A)						AD843BH			AD843SH		
LCC (E-20A)									AD843SE, AD843SE/883B		
SOIC (R-16)			AD843JR								
Tape & Reel			AD843JR-REEL								
Chips			AD843JChips						AD843SChips		

NOTES
[1]Specifications are guaranteed after 5 minutes at T_A = +25°C.
[2]Full power bandwidth = Slew Rate/2 πV peak.
[3]All "S" grade T_{min}–T_{max} specifications are tested with automatic test equipment at T_A = −55°C and T_A = +125°C.
[4]For outline information see Package Information section.

Specifications subject to change without notice.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed although only those shown in **boldface** are tested on all production units.

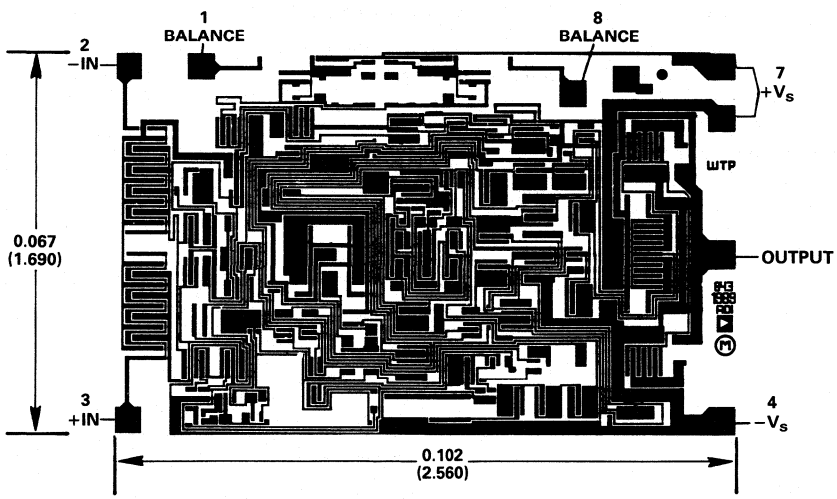
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
Plastic Package . . . . . 1.50 Watts
Cerdip Package . . . . . 1.35 Watts
12-Pin Header Package . . . . . 1.80 Watts
16-Pin SOIC Package . . . . . 1.50 Watts
20-Pin LCC Package . . . . . 1.00 Watt
Input Voltage . . . . . $\pm V_S$
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range (N, R) . . . . . −65°C to +125°C
Storage Temperature Range (Q, H, E) . . . . . −65°C to +150°C
Operating Temperature Range
AD843J/K . . . . . 0 to +70°C
AD843A/B . . . . . −40°C to +85°C
AD843S . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Pin Plastic Package: θ_{JA} = 100°C/Watt
8-Pin Cerdip Package: θ_{JA} = 110°C/Watt
12-Pin Header Package: θ_{JA} = 80°C/Watt
16-Pin SOIC Package: θ_{JA} = 100°C/Watt
20-Pin LCC Package: θ_{JA} = 150°C/Watt

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



AD843—Typical Characteristics

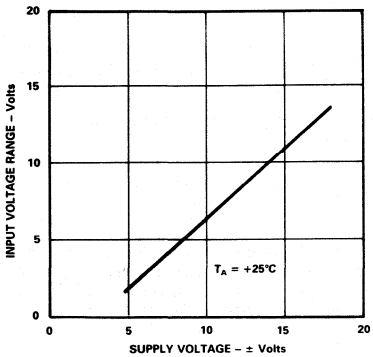


Figure 1. Input Voltage Range vs. Supply Voltage

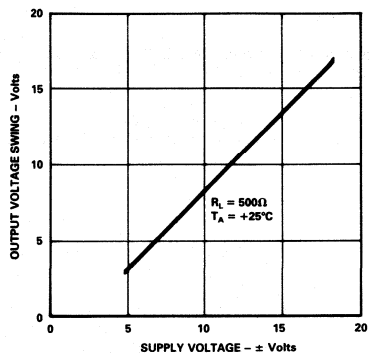


Figure 2. Output Voltage Swing vs. Supply Voltage

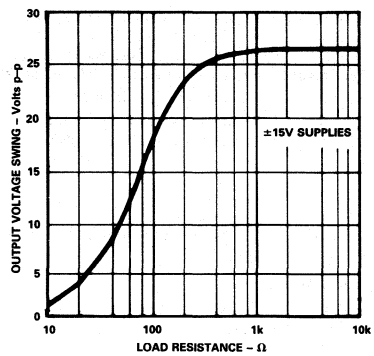


Figure 3. Output Voltage Swing vs. Load Resistance

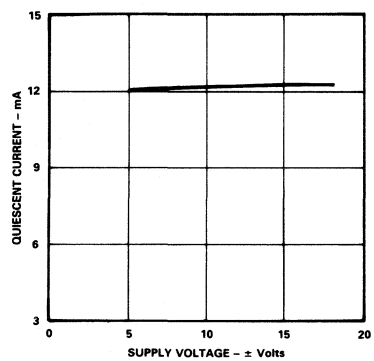


Figure 4. Quiescent Current vs. Supply Voltage

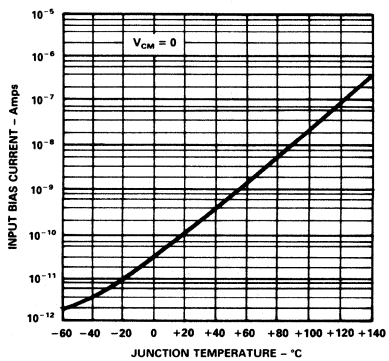


Figure 5. Input Bias Current vs. Junction Temperature

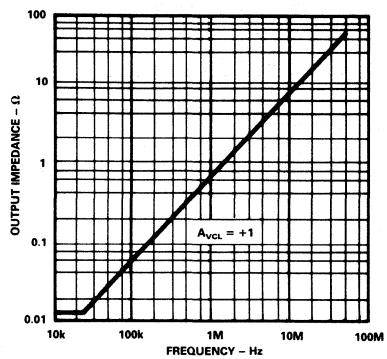


Figure 6. Output Impedance vs. Frequency

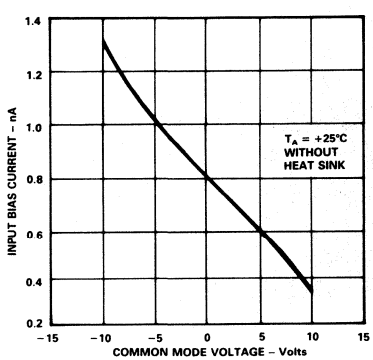


Figure 7. Input Bias Current vs. Common Mode Voltage

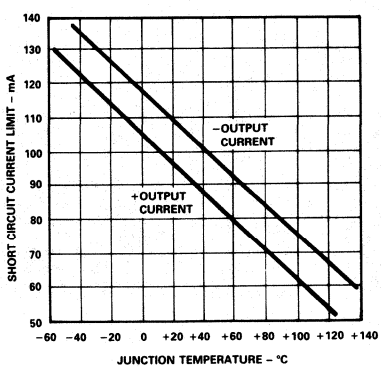


Figure 8. Short Circuit Current Limit vs. Junction Temperature (T_J)

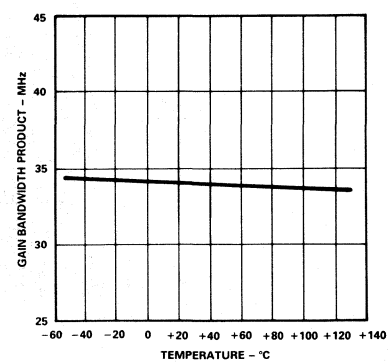


Figure 9. Gain Bandwidth Product vs. Temperature

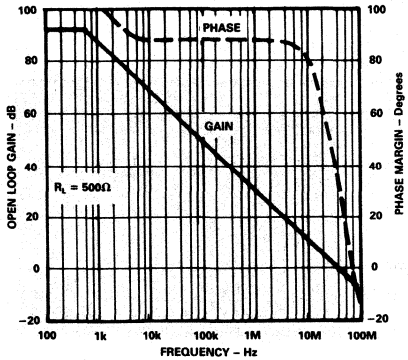


Figure 10. Open Loop Gain and Phase Margin vs. Frequency

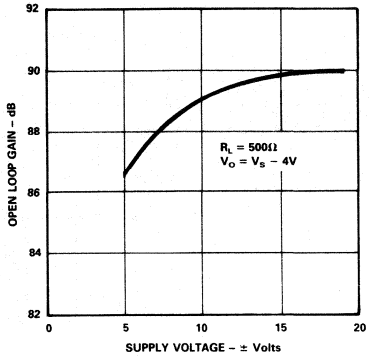


Figure 11. Open Loop Gain vs. Supply Voltage

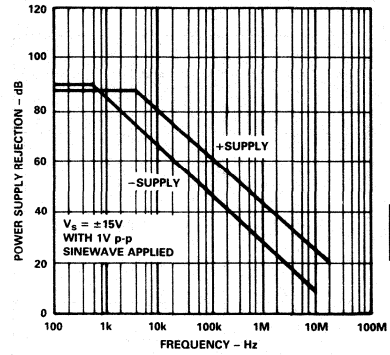


Figure 12. Power Supply Rejection vs. Frequency

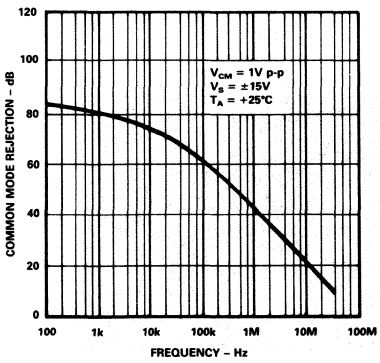


Figure 13. Common Mode Rejection vs. Frequency

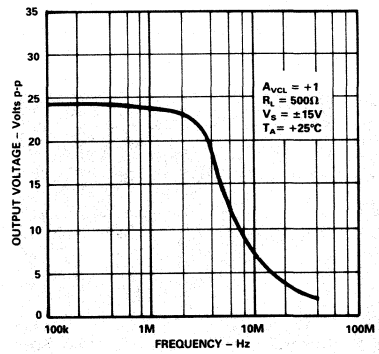


Figure 14. Large Signal Frequency Response

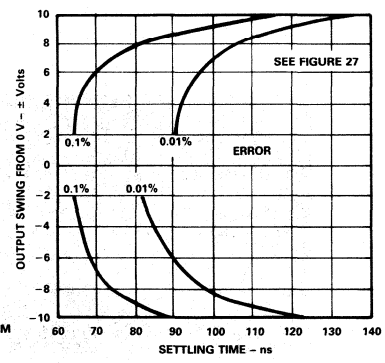


Figure 15. Output Swing and Error vs. Settling Time

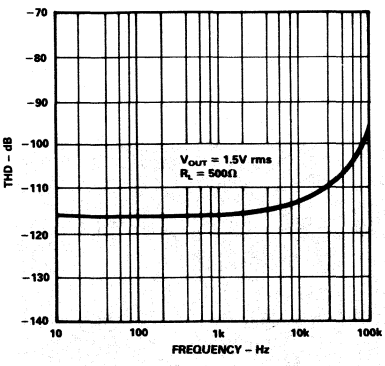


Figure 16. Harmonic Distortion vs. Frequency

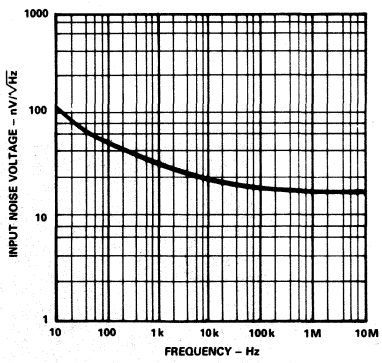


Figure 17. Input Noise Voltage Spectral Density

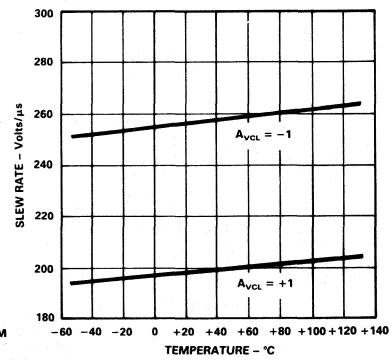


Figure 18. Slew Rate vs. Temperature

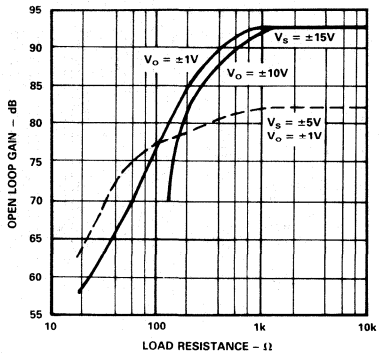


Figure 19. Open Loop Gain vs. Resistive Load

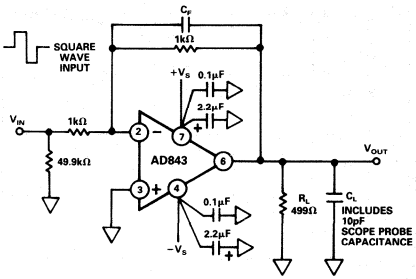


Figure 20a. Inverting Amplifier Connection

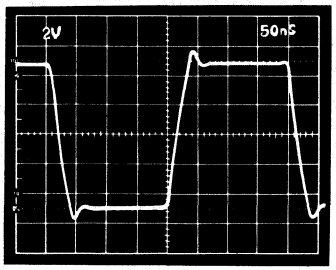


Figure 20b. Inverter Large Signal Pulse Response. C_F = 0, C_L = 10 pF

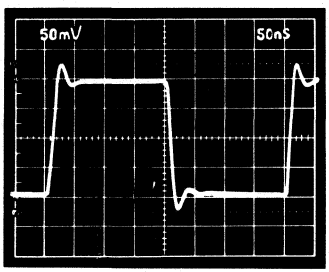


Figure 20c. Inverter Small Signal Pulse Response. C_F = 0, C_L = 10 pF

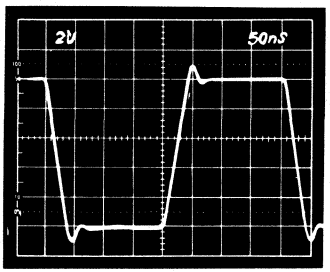


Figure 20d. Inverter Large Signal Pulse Response. C_F = 5 pF, C_L = 110 pF

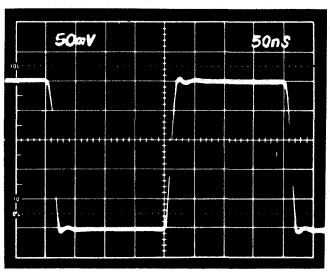


Figure 20e. Inverter Small Signal Pulse Response. C_F = 5 pF, C_L = 110 pF

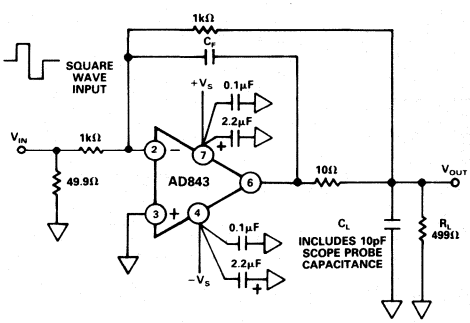


Figure 21a. Unity Gain Inverter Circuit for Driving Capacitive Loads

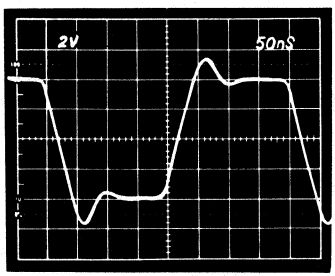


Figure 21b. Inverter Cap Load Large Signal Pulse Response. C_F = 15 pF, C_L = 410 pF

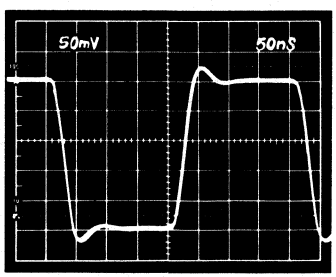


Figure 21c. Inverter Cap Load Small Signal Pulse Response. C_F = 15 pF, C_L = 410 pF

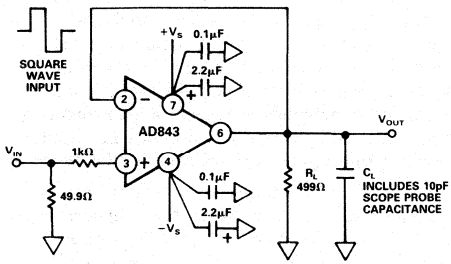


Figure 22a. Unity Gain Buffer Amplifier

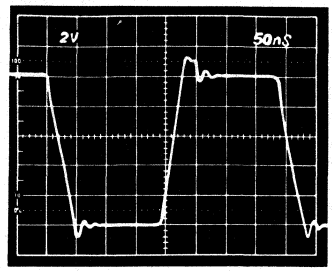


Figure 22b. Buffer Large Signal Pulse Response. C_L = 10 pF

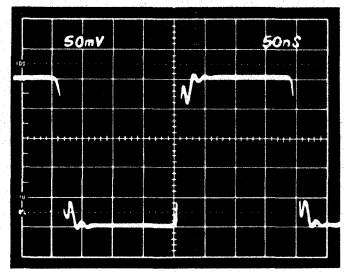


Figure 22c. Buffer Small Signal Pulse Response. C_L = 10 pF

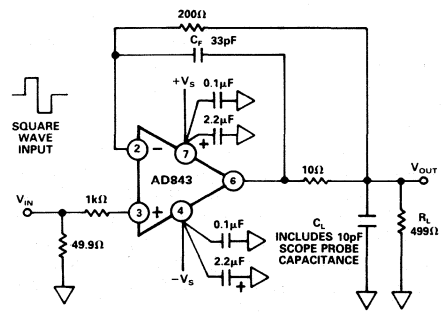


Figure 23a. Unity Gain Buffer Circuit for Driving Capacitive Loads

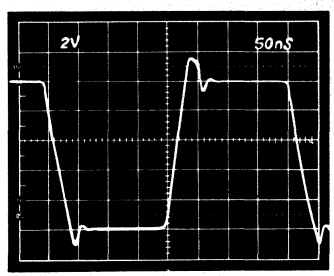


Figure 23b. Buffer Cap Load Large Signal Pulse Response. C_F = 33 pF, C_L = 10 pF

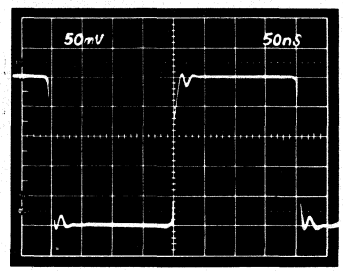


Figure 23c. Buffer Cap Load Small Signal Pulse Response. C_F = 33 pF, C_L = 10 pF

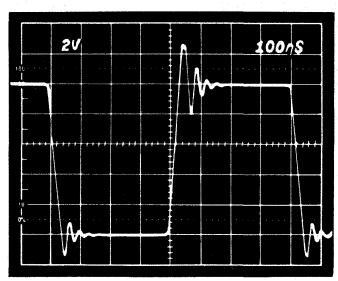


Figure 23d. Buffer Cap Load Large Signal Pulse Response. C_F = 33 pF, C_L = 110 pF

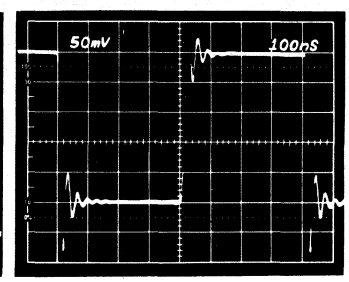


Figure 23e. Buffer Cap Load Small Signal Pulse Response. C_F = 33 pF, C_L = 110 pF

DRIVING CAPACITIVE LOADS

Like most high bandwidth amplifiers, the AD843 is sensitive to capacitive loading. Although it will drive capacitive loads up to 20 pF without degradation of its rated performance, both an increased capacitive load drive capability and a "cleaner" (non-ringing) pulse response can be obtained from the AD843 by using the circuits illustrated in Figures 20 to 23. The addition of a 5 pF feedback capacitor to the unity gain inverter connection (Figure 20a) substantially reduces the circuit's overshoot, even when it is driving a 110 pF load. This can be seen by comparing the waveforms of Figures 20b through 20e. To drive capacitive loads greater than 100 pF, the load should be decoupled from the amplifier's output by a 10 Ω resistor and the feedback capacitor, C_F, should be connected directly between the amplifier's output and its inverting input (Figure 21a). When using a 15 pF feedback capacitor, this circuit can drive 400 pF with less than 20% overshoot, as illustrated in Figures 21b and 21c. Increasing capacitor C_F to 47 pF also increases the capacitance drive capability to 1000 pF, at the expense of a 10:1 reduction in bandwidth compared with the simple unity gain inverter circuit of Figure 20a.

Unity gain voltage followers (buffers) are more sensitive to capacitive loads than are inverting amplifiers because there is no attenuation of the feedback signal. The AD843 can drive 10 pF to 20 pF when connected in the basic unity gain buffer circuit of Figure 22a.

The 1 kΩ resistor in series with the AD843's noninverting input serves two functions: first, together with the amplifier's input capacitance, it forms a low pass filter which slows down the actual signal seen by the AD843. This helps reduce ringing on the amplifier's output voltage. The resistor's second function is to limit the current into the amplifier when the differential input voltage exceeds the total supply voltage.

The AD843 will deliver a much "cleaner" pulse response when connected in the somewhat more elaborate follower circuit of Figure 23a. Note the reduced overshoot in Figure 23b and 23c as compared to Figure 22b and 22c.

For maximum bandwidth, in most applications, input and feedback resistors used with the AD843 should have resistance values equal to or less than 1.5 kΩ. Even with these low resistance values, the resultant RC time constant formed between them and stray circuit capacitances is large enough to cause peaking in the amplifier's response. Adding a small capacitor, C_F, as shown in Figures 20a to 23a will reduce this peaking and flatten the overall frequency response. C_F will normally be less than 10 pF in value.

The AD843 can drive resistive loads over the range of 500 Ω to ∞ with no change in dynamic response. While a 499 Ω load was used in the circuits of Figures 20–23, the performance of these circuits will be essentially the same even if this load is removed or changed to some other value, such as 2 kΩ.

To obtain the "cleanest" possible transient response when driving heavy capacitive loads, be sure to connect bypass capacitors directly between the power supply pins of the AD843 and ground as outlined in "grounding and bypassing."

GROUNDING AND BYPASSING

In designing practical circuits using the AD843, the user must keep in mind that some special precautions are needed when dealing with high frequency signals. Circuits must be wired using short interconnect leads. Ground planes should be used whenever possible to provide both a low resistance, low inductance circuit path and to minimize the effects of high frequency coupling. IC sockets should be avoided, since their increased interlead capacitance can degrade the bandwidth of the device.

Power supply leads should be bypassed to ground as close as possible to the pins of the amplifier. Again, the component leads should be kept very short. As shown in Figure 24, a parallel combination of a 2.2 μF tantalum and a 0.1 μF ceramic disc capacitor is recommended.

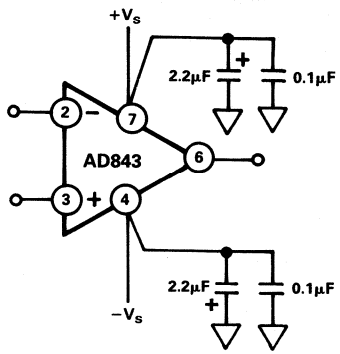
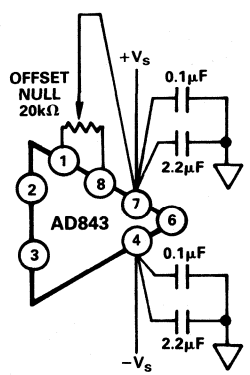


Figure 24. Recommended Power Supply Bypassing for the AD843 (DIP Pinout)

USING A HEAT SINK

The AD843 consumes less quiescent power than most precision high speed amplifiers and is specified to operate without using a heat sink. However, when driving low impedance loads, the current applied to the load can be 4 to 5 times greater than the quiescent current. This will produce a noticeable temperature rise, which will increase input bias currents. The use of a small heat sink, such as the Mouser Electronics #33HS008 is recommended.



Offset Null Configuration (DIP Pinout)

SAMPLE-AND-HOLD AMPLIFIER CIRCUITS

A Fast Switching Sample & Hold Circuit

A sample-and-hold circuit possessing short acquisition time and low aperture delay can be built using an AD843 and discrete JFET switches. The circuit of Figure 25 employs five n-channel JFETs (with turn-on times of 35 ns) and an AD843 op amp (which can settle to 0.01% in 135 ns). The circuit has an aperture delay time of 50 ns and an acquisition time of 1 μs or less.

This circuit is based on a noninverting open loop architecture, using a differential hold capacitor to reduce the effects of pedestal error. The charge that is removed from CH1 by Q2 and Q3 is offset by the charge removed from CH2 by Q4 and Q5. This circuit can tolerate low hold capacitor values (approximately 100 pF), which improve acquisition time, due to the small gate-to-drain capacitance of the discrete JFETs. Although pedestal error will vary with input signal level, making trimming more difficult, the circuit has the advantages of high bandwidth and short acquisition times. In addition, it will exhibit some nonlinearity because both amplifiers are operating with a common mode input. Amplifier A2, however, contributes less than 0.025% linearity error, due to its 72 dB common mode rejection ratio.

To make sure the circuit accommodates a wide ±10 V input range, the gates of the JFETs must be connected to a potential near the −15 V supply. The level-shift circuitry (diode D3, PNP transistor Q7, and NPN transistor Q6) shifts the TTL-level S/H command to provide for an adequate pinch-off voltage for the JFET switches over the full input voltage range.

The JFETs Q2, Q3, Q4 and Q5 across the two hold capacitors ensure signal acquisition for all conditions of V_{IN} and V_{OUT} when the circuit switches from the sample to the hold mode. Transistor Q1 provides an extra stage of isolation between the output of amplifier A1 and the hold capacitor CH1.

When selecting capacitors for use in a sample-and-hold circuit, the designer should choose those types with low dielectric absorption and low temperature coefficients. Silvered-mica capacitors exhibit low (0 to 100 ppm/°C) temperature coefficients and will still work in temperatures exceeding 200°C. It is also recommend that the user test the chosen capacitor to insure that its value closely matches that printed on it since not all capacitors are fully tested by their manufacturers for absolute tolerance.

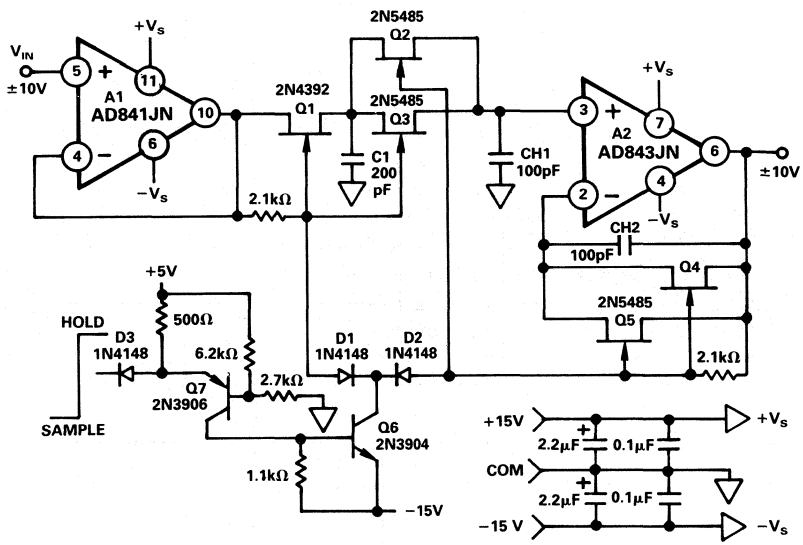


Figure 25. A Fast Switching Sample-and-Hold Amplifier

A PING-PONG S/H AMPLIFIER

For improved throughput over the circuit of Figure 25, a "ping-pong" architecture may be used. A ping-pong circuit overcomes some of the problems associated with high speed S/H amplifiers by allowing the use of a larger hold capacitor for a given sample rate: this will reduce the associated feedthrough, droop and pedestal errors.

Figure 26 illustrates a simple, four-chip ping-pong sample-and-hold amplifier circuit. This design increases throughput by using one channel to acquire a new sample while another channel holds the previous sample. Instead of having to reacquire the signal when switching from hold to sample mode, it alternately connects the outputs from Channel 1 or from Channel 2 to the A/D converter. In this case, the throughput is the slew rate and settling time of the output amplifiers, A2 and A3.

A high speed CB amplifier, A1, follows the input signal. U1, a dual wide-band "T" switch, connects the input buffer amp to one of the two output amplifiers while selecting the complementary amplifier to drive the A/D input. For example, when "select" is at logic high, A1 drives CH1, A2 tracks the input signal and the output of A3 is connected to the input of the A/D converter. At the same time, A3 holds an analog value and its output is connected to the input of the A/D converter. When the select command goes to logic LOW, the two output amplifiers alternate functions.

Since the input to the A/D converter is the alternated "held" outputs from A1 and A2, the offset voltage mismatch of the two amplifiers will show up as nonlinearity and, therefore, distortion in the output signal. To minimize this, potentiometers can be used to adjust the offsets of the output amplifiers until they are equal. Alternatively, an autocalibration circuit using two D/A converters can be employed. This can also be used to calibrate-out the effects of offset voltage drift over temperature.

The switch choice, for U1, is critical in this type of design. The DG542 utilizes "T" switching techniques on each channel for exceptionally low crosstalk and for high isolation. The part further improves these specifications by using ground pins between the signal pins. With an input frequency of 5 MHz, crosstalk and isolation are −85 dB and −75 dB, respectively. A limitation of this switch is that it operates from a maximum −5 V negative supply, making bipolar operation more difficult. It is recommended that amplifiers A1, A2 and A3 operate from the same −5 V supply to minimize any potential latch-up problems.

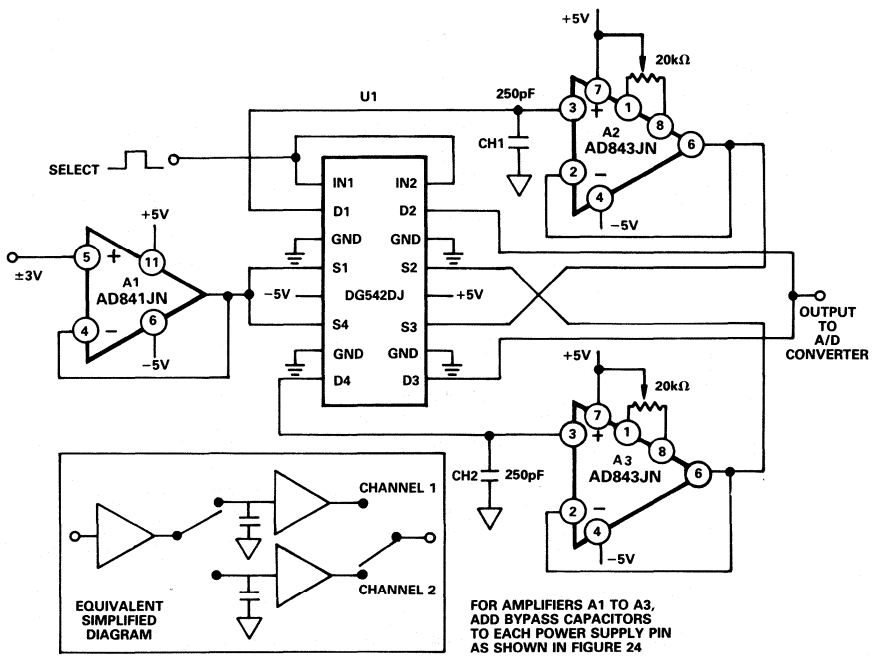


Figure 26. A Ping-Pong Sample-and-Hold Amplifier

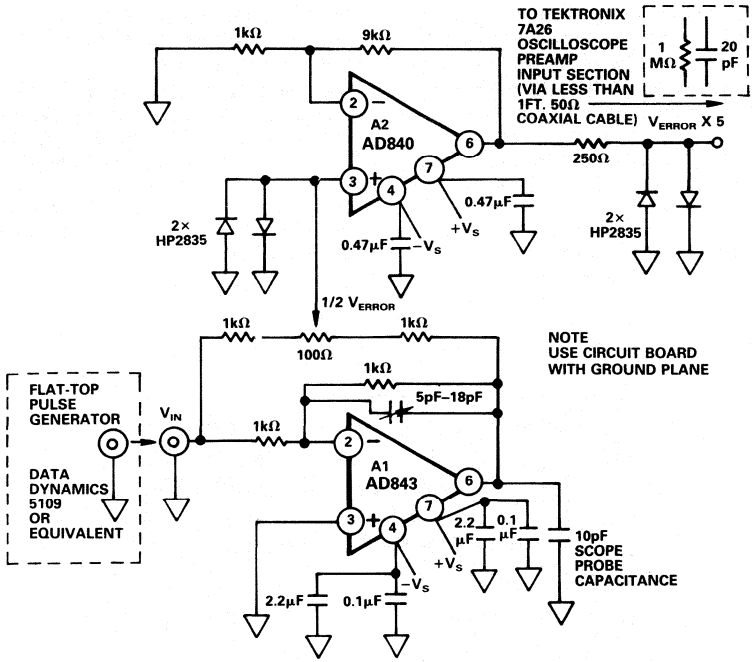


Figure 27. Settling Time Test Circuit

MEASURING AD843 SETTLING TIME

Figure 28 shows the dynamic response of the AD843 while operating in the settling time test circuit of Figure 27. The input of the settling time fixture is driven by a flat-top pulse generator. The error signal output from A1, the AD843 under test, is amplified by op amp A2 and then clamped by two high speed Schottky diodes.

The error signal is clamped to prevent it from greatly overloading the oscilloscope preamp. A Tektronix oscilloscope preamp type 7A26 was chosen because it will recover from the approximately 0.4 volt overload, quickly enough to allow accurate measurement of the AD843's 135 ns settling time. Amplifier A2 is a very high speed op amp; it provides a voltage gain of 10, providing a total gain of 5 from the error signal to the oscilloscope input.

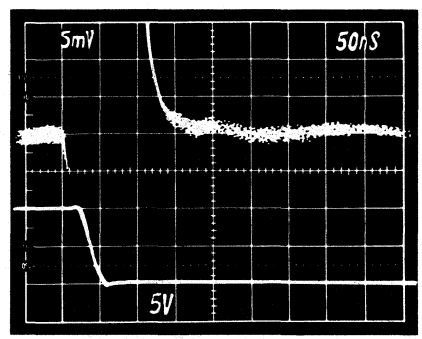


Figure 28. Settling Characteristics: +10 V to 0 V Step.
Upper Trace: Amplified Error Voltage (0.01%/Div)
Lower Trace: Output of AD843 Under Test (5 V/Div)

AD843—Applications Circuit

A FAST PEAK DETECTOR CIRCUIT

The peak detector circuit of Figure 29, can accurately capture the amplitude of input pulses as narrow as 200 ns and can hold their value with a droop rate of less than 20 μV/μs. This circuit will capture the peak value of positive polarity waveforms; to detect negative peaks, simply reverse the polarity of the two diodes.

The high bandwidth and 200 V/μs slew rate of amplifier A2, an AD843, allows the detector's output to "keep up" with its input thus minimizing overshoot. The low (<1 nA) input current of the AD843 ensures that the droop rate is limited only by the reverse leakage of diode D2, which is typically <10 nA for the type shown. The low droop rate is apparent in Figure 30. The detector's output (top trace) loses slightly over a volt of the 8 volt peak input value (bottom trace) in 75 ms, or a rate of approximately 16 μV/μs

Amplifier A1, an AD847, can drive 680 pF hold capacitor, C_P, fast enough to "catch-up" with the next peak in 100 ns and still settle to the new value in 250 ns, as illustrated in Figure 31. *Reducing* the value of capacitor C_P to 100 pF will maximize the speed of this circuit at the expense of increased overshoot and droop. Since the AD847 can drive an arbitrarily large value of capacitance, C_P can be *increased* to reduce droop, at the expense of response time.

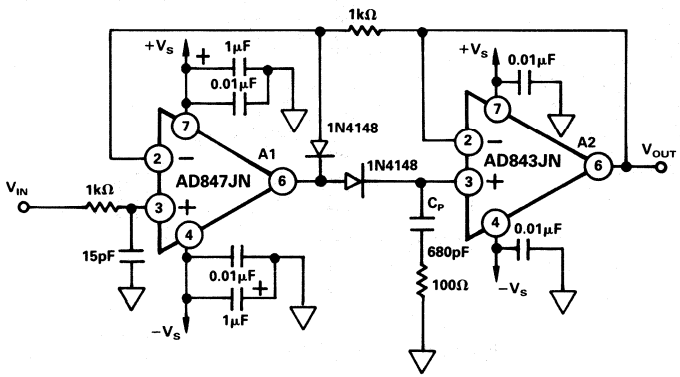
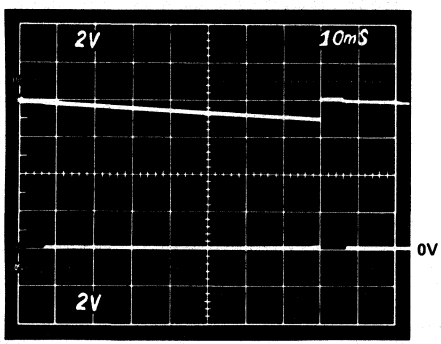


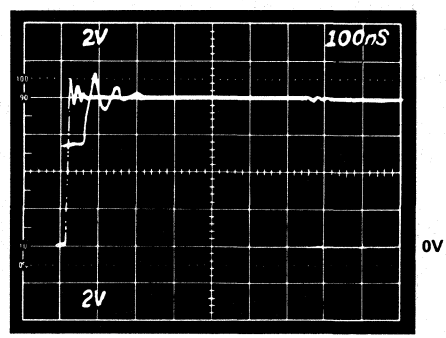
Figure 29. A Fast Peak Detector Circuit



TOP TRACE: PEAK DETECTOR OUTPUT

BOTTOM TRACE: INPUT, 8V PEAK @ 125Hz

Figure 30. Peak Detector Response to 125 Hz Pulse Train



TOP TRACE: PEAK DETECTOR OUTPUT, 8V

BOTTOM TRACE: INPUT VOLTAGE, 8V PEAK, 650ns PULSE WIDTH

Figure 31. Peak Capture Time

ANALOG DEVICES

60MHz, 2000V/μs Monolithic Op Amp

AD844

FEATURES

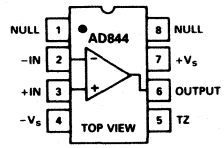
Wide Bandwidth: 60MHz at Gain of −1
33MHz at Gain of −10
Very High Output Slew Rate: Up to 2000V/μs
20MHz Full Power Bandwidth, 20V pk-pk, R_L=500Ω
Fast Settling: 100ns to 0.1% (10V Step)
Differential Gain Error: 0.03% at 4.4MHz
Differential Phase Error: 0.15° at 4.4MHz
High Output Drive: ±50mA into 50Ω Load
Low Offset Voltage: 150μV max (B Grade)
Low Quiescent Current: 6.5mA
Available in Tape and Reel in Accordance with EIA-481A Standard

APPLICATIONS

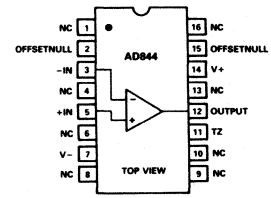
Flash ADC Input Amplifiers
High Speed Current DAC Interfaces
Video Buffers and Cable Drivers
Pulse Amplifiers

CONNECTION DIAGRAM

8-Pin Plastic (N), and Cerdip (Q) Packages



16-Pin SOIC (R) Package



PRODUCT DESCRIPTION

The AD844 is a high speed monolithic operational amplifier fabricated using Analog Devices' junction isolated complementary bipolar (CB) process. It combines high bandwidth and very fast large signal response with excellent dc performance. Although optimized for use in current to voltage applications and as an inverting mode amplifier, it is also suitable for use in many non-inverting applications.

The AD844 can be used in place of traditional op amps, but its current feedback architecture results in much better ac performance, high linearity and an exceptionally clean pulse response.

This type of op amp provides a closed-loop bandwidth which is determined primarily by the feedback resistor and is almost independent of the closed-loop gain. The AD844 is free from the slew rate limitations inherent in traditional op amps and other current-feedback op amps. Peak output rate of change can be over 2000V/μs for a full 20V output step. Settling time is typically 100ns to 0.1%, and essentially independent of gain. The AD844 can drive 50Ω loads to ±2.5V with low distortion and is short circuit protected to 80mA.

The AD844 is available in four performance grades and three package options. In the 16-pin SOIC (R) package, the AD844J is specified for the commercial temperature range of 0 to +70°C. The AD844A and AD844B are specified for the industrial temperature range of −40°C to +85°C and are available in the cerdip (Q) package. The AD844A is also available in an 8-pin plastic mini-DIP (N). The AD844S is specified over the military temperature range of −55°C to +125°C. It is available in the 8-pin cerdip (Q) package. "A" and "S" grade chips and devices processed to MIL-STD-883B, REV. C are also available.

PRODUCT HIGHLIGHTS

1. The AD844 is a versatile, low cost component providing an excellent combination of ac and dc performance. It may be used as an alternative to the EL2020 and CLC400/1.
2. It is essentially free from slew rate limitations. Rise and fall times are essentially independent of output level.
3. The AD844 can be operated from ±4.5V to ±18V power supplies and is capable of driving loads down to 50Ω, as well as driving very large capacitive loads using an external network.
4. The offset voltage and input bias currents of the AD844 are laser trimmed to minimize dc errors; V_{OS} drift is typically 1μV/°C and bias current drift is typically 9nA/°C.
5. The AD844 exhibits excellent differential gain and differential phase characteristics, making it suitable for a variety of video applications with bandwidths up to 60MHz.
6. The AD844 combines low distortion, low noise and low drift with wide bandwidth, making it outstanding as an input amplifier for flash A/D converters.

AD844—SPECIFICATIONS (@ T_A+25°C and V_S=±15V dc, unless otherwise noted)

Model	Conditions	AD844J/A Min	AD844J/A Typ	AD844J/A Max	AD844B Min	AD844B Typ	AD844B Max	AD844S Min	AD844S Typ	AD844S Max	Units
INPUT OFFSET VOLTAGE[1]			50	**300**		50	**150**		50	**300**	μV
T_{min}–T_{max}			75	500		75	**200**		125	**500**	μV
vs. Temperature			1			1	5		1	5	μV/°C
vs. Supply	5V–18V										
Initial			4	**20**		4	**10**		4	**20**	μV/V
T_{min}–T_{max}			4			4	**10**		4	**20**	μV/V
vs. Common Mode	V_{CM}=±10V										
Initial			10	**35**		10	**20**		10	**35**	μV/V
T_{min}–T_{max}			10			10	**20**		10	**35**	μV/V
INPUT BIAS CURRENT											
–Input Bias Current[1]			200	**450**		150	**250**		200	**450**	nA
T_{min}–T_{max}			800	1500		750	**1100**		1900	**2500**	nA
vs. Temperature			9			9	15		20	30	nA/°C
vs. Supply	5V–18V										
Initial			175	**250**		175	**200**		175	**250**	nA/V
T_{min}–T_{max}			220			220	**240**		220	**300**	nA/V
vs. Common Mode	V_{CM}=±10V										
Initial			90	**160**		90	**110**		90	**160**	nA/V
T_{min}–T_{max}			110			110	**150**		120	**200**	nA/V
+Input Bias Current[1]			150	**400**		100	**200**		100	**400**	nA
T_{min}–T_{max}			350	700		300	**500**		800	**1300**	nA
vs. Temperature			3			3	7		7	15	nA/°C
vs. Supply	5V–18V										
Initial			80	**150**		80	**100**		80	**150**	nA/V
T_{min}–T_{max}			100			100	**120**		120	**200**	nA/V
vs. Common Mode	V_{CM}=±10V										
Initial			90	**150**		90	**120**		90	**150**	nA/V
T_{min}–T_{max}			130			130	**190**		140	**200**	nA/V
INPUT CHARACTERISTICS											
Input Resistance											
–Input			50	65		50	65		50	65	Ω
+Input		7	10		7	10		7	10		MΩ
Input Capacitance											
–Input			2			2			2		pF
+Input			2			2			2		pF
Input Voltage Range											
Common Mode		±10			±10			±10			V
INPUT VOLTAGE NOISE	f≥1kHz		2			2			2		nV/√Hz
INPUT CURRENT NOISE											
–Input	f≥1kHz		10			10			10		pA/√Hz
+Input	f≥1kHz		12			12			12		pA/√Hz
OPEN LOOP TRANSRESISTANCE	V_{OUT}=±10V										
	R_{LOAD}=500Ω	**2.2**	3.0		**2.8**	3.0		**2.2**	3.0		MΩ
T_{min}–T_{max}		1.3	2.0		**1.6**	2.0		**1.3**	1.6		MΩ
Transcapacitance			4.5			4.5			4.5		pF
DIFFERENTIAL GAIN ERROR[2]	f=4.4MHz		0.03			0.03			0.03		%
DIFFERENTIAL PHASE ERROR[2]	f=4.4MHz		0.15			0.15			0.15		Degree
FREQUENCY RESPONSE											
Small Signal Bandwidth											
[3]Gain=–1			60			60			60		MHz
[4]Gain=–10			33			33			33		MHz
TOTAL HARMOMIC DISTORTION	f=100kHz, 2V rms[5]		0.005			0.005			0.005		%
SETTLING TIME											
10V Output Step	±15V Supplies										
Gain=–1, to 0.1%[5]			100			100			100		ns
Gain=–10, to 0.1%[6]			100			100			100		ns
2V Output Step	±5V Supplies										
Gain=–1, to 0.1%[5]			110			110			110		ns
Gain=–10, to 0.1%[6]			100			100			100		ns

Model	Conditions	AD844J/A Min	AD844J/A Typ	AD844J/A Max	AD844B Min	AD844B Typ	AD844B Max	AD844S Min	AD844S Typ	AD844S Max	Units
OUTPUT SLEW RATE	Overdriven Input	1200	2000		1200	2000		1200	2000		V/μs
FULL POWER BANDWIDTH											
V_{OUT}=20V p-p[5]	V_S=±15V		20			20			20		MHz
V_{OUT}=2V p-p[5]	V_S=±5V THD=3%		20			20			20		MHz
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD}=500Ω	**10**	11		**10**	11		**10**	11		±V
Short Circuit Current			80			80			80		mA
T_{min}–T_{max}			60			60			60		mA
Output Resistance	Open Loop		15			15			15		Ω
POWER SUPPLY											
Operating Range		±4.5		±18	±4.5		±18	±4.5		±18	V
Quiescent Current			6.5	7.5		6.5	7.5		6.5	7.5	mA
T_{min}–T_{max}			7.5	8.5		7.5	8.5		8.5	9.5	mA

NOTES
[1]Rated performance after a 5 minute warmup at T_A=25°C.
[2]Input signal 285mV p-p carrier (40 IRE) riding on 0 to 642mV (90 IRE) ramp. R_L=100Ω; R1, R2=300Ω.
[3]Input signal 0dBm, C_L=10pF, R_L=500Ω, R1=500Ω, R2=500Ω in Figure 26.
[4]Input signal 0dBm, C_L=10pF, R_L=500Ω, R1=500Ω, R2=50Ω in Figure 26.
[5]C_L=10pF, R_L=500Ω, R1=1kΩ, R2=1kΩ in Figure 26.
[6]C_L=10pF, R_L=500Ω, R1=500Ω, R2=50Ω in Figure 26.

Specifications subject to change without notice. All min and max specifications are guaranteed.
Specifications shown in **boldface** are tested on all production units at final electrical test.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18V
Power Dissipation[2] 1.1W
Output Short Circuit Duration . . . . . Indefinite
Common Mode Input Voltage . . . . . $\pm V_S$
Differential Input Voltage 6V
Inverting Input Current
Continuous 5mA
Transient 10mA
Storage Temperature Range (Q) . . . . . −65°C to +150°C
(N, R) . . . . . −65°C to +125°C
Lead Temperature Range (Soldering 60sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Pin Plastic Package: θ_{JA}=100°C/Watt
8-Pin Cerdip Package: θ_{JA}=110°C/Watt
16-Pin SOIC Package: θ_{JA}=100°C/Watt

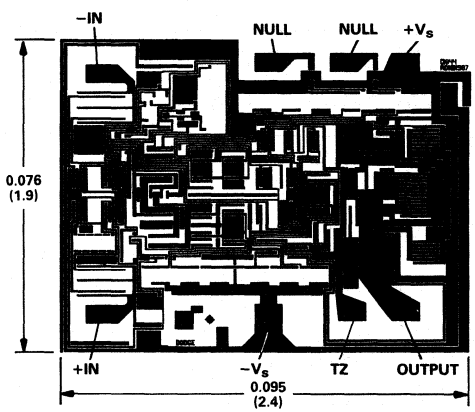
ORDERING GUIDE

Model	Temperature Range	Package Option*
AD844JR	0°C to +70°C	R-16
AD844JR-REEL	0°C to +70°C	Tape and Reel
AD844AN	−40°C to +85°C	N-8
AD844AQ	−40°C to +85°C	Q-8
AD844BQ	−40°C to +85°C	Q-8
AD844SQ	−55°C to +125°C	Q-8
AD844SQ/883B	−55°C to +125°C	Q-8
AD844A Chips	−40°C to +85°C	Die
AD844S Chips	−55°C to +125°C	Die

*N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



SUBTRATE CONNECTED TO +V_S

AD844—Typical Characteristics (T_A = +25°C and V_S = ±15V, unless otherwise noted)

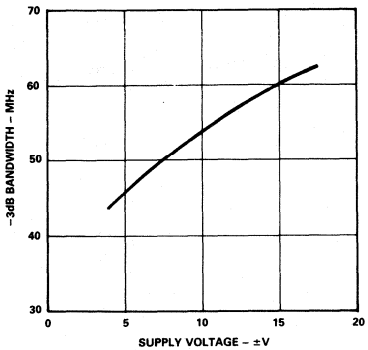


Figure 1. −3dB Bandwidth vs. Supply Voltage R1 = R2 = 500Ω

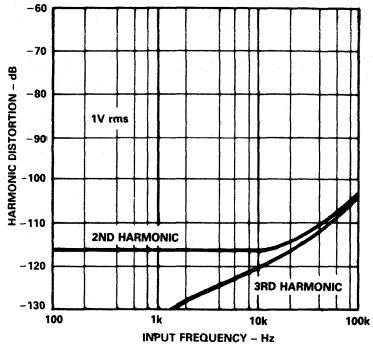


Figure 2. Harmonic Distortion vs. Frequency, R1 = R2 = 1kΩ

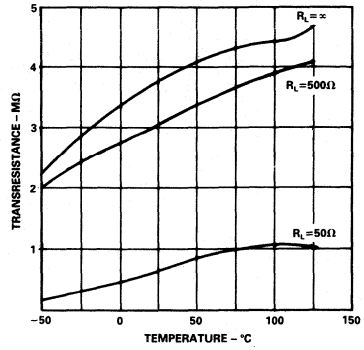


Figure 3. Transresistance vs. Temperature

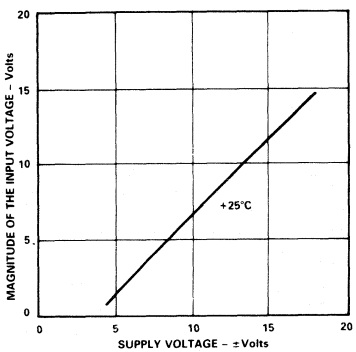


Figure 4. Noninverting Input Voltage Swing vs. Supply Voltage

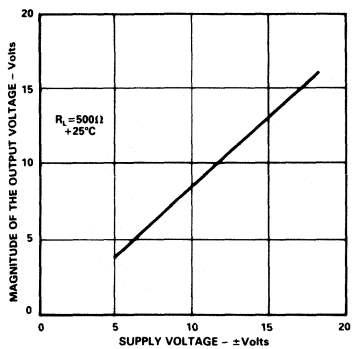


Figure 5. Output Voltage Swing vs. Supply Voltage

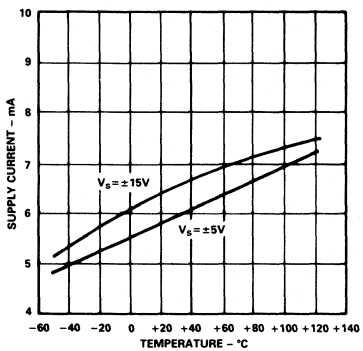


Figure 6. Quiescent Supply Current vs. Temperature and Supply Voltage

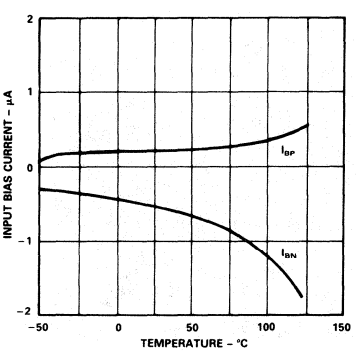


Figure 7. Inverting Input Bias Current (I_{BN}) and Noninverting Input Bias Current (I_{BP}) vs. Temperature

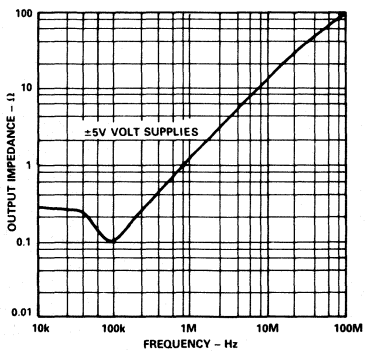


Figure 8. Output Impedance vs. Frequency, Gain = −1, R1 = R2 = 1kΩ

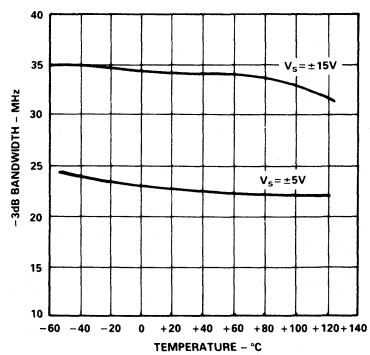


Figure 9. −3dB Bandwidth vs. Temperature, Gain = −1, R1 = R2 = 1kΩ

Inverting Gain of 1 AC Characteristics

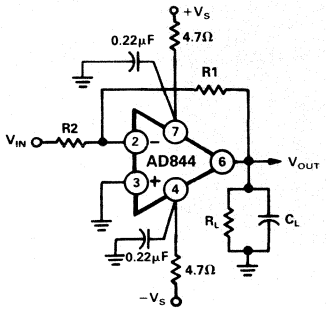


Figure 10. Inverting Amplifier, Gain of −1 (R1=R2)

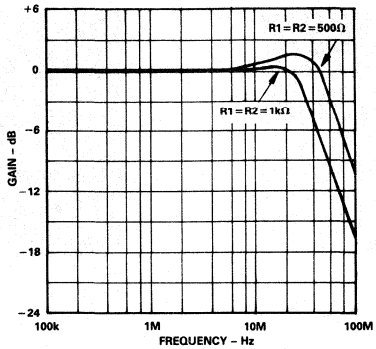


Figure 11. Gain vs. Frequency for Gain = −1, R_L = 500Ω, C_L = 0pF

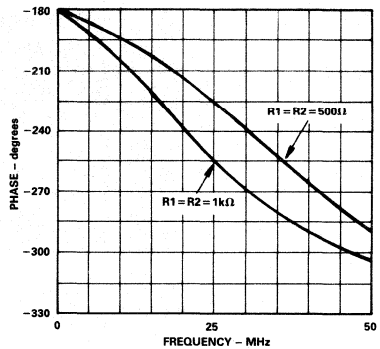


Figure 12. Phase vs. Frequency Gain = −1, R_L = 500Ω, C_L = 0pF

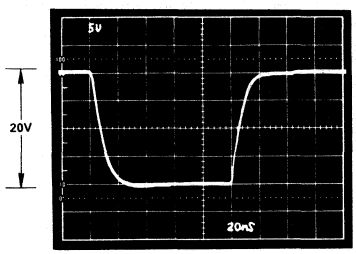


Figure 13. Large Signal Pulse Response, Gain = −1, R1 = R2 = 1kΩ

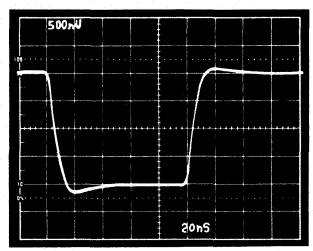


Figure 14. Small Signal Pulse Response, Gain = −1, R1 = R2 = 1kΩ

Inverting Gain of 10 AC Characteristics

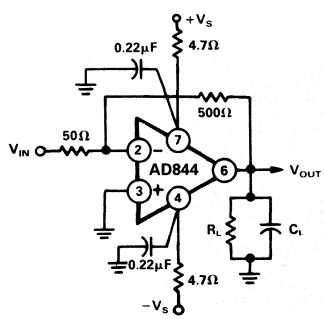


Figure 15. Gain of −10 Amplifier

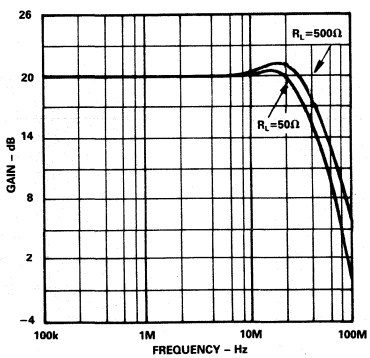


Figure 16. Gain vs. Frequency, Gain = −10

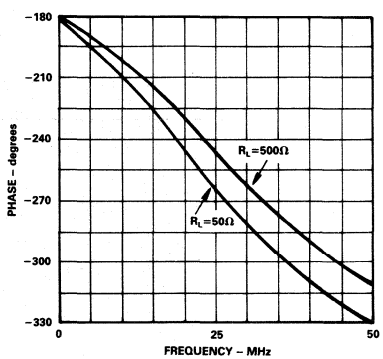


Figure 17. Phase vs. Frequency, Gain = −10

Inverting Gain of 10 Pulse Response

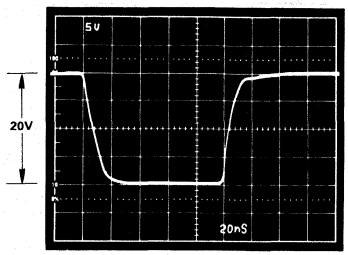


Figure 18. Large Signal Pulse Response, Gain=−10, R_L=500Ω

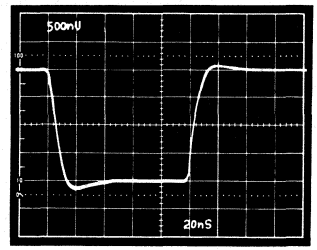


Figure 19. Small Signal Pulse Response, Gain=−10, R_L=500Ω

Noninverting Gain of 10 AC Characteristics

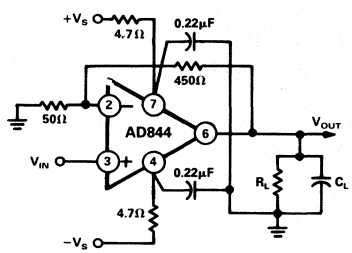


Figure 20. Noninverting Gain of +10 Amplifier

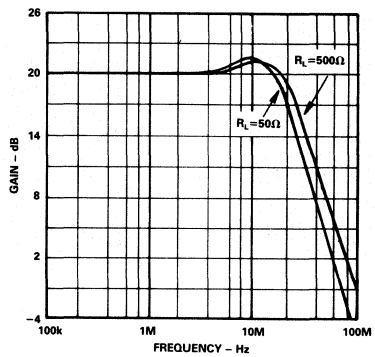


Figure 21. Gain vs. Frequency, Gain=+10

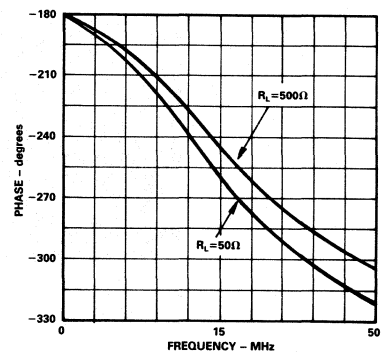


Figure 22. Phase vs. Frequency, Gain=+10

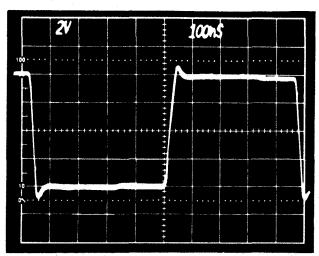


Figure 23. Noninverting Amplifier Large Signal Pulse Response, Gain=+10, R_L=500Ω

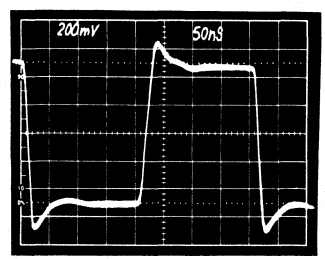


Figure 24. Small Signal Pulse Response, Gain=+10, R_L=500Ω

UNDERSTANDING THE AD844

The AD844 can be used in ways similar to a conventional op amp while providing performance advantages in wideband applications. However, there are important differences in the internal structure which need to be understood in order to optimize the performance of the AD844 op amp.

Open Loop Behavior

Figure 25 shows a current feedback amplifier reduced to essentials. Sources of fixed dc errors such as the inverting node bias current and the offset voltage are excluded from this model and are discussed later. The most important parameter limiting the dc gain is the transresistance, Rt, which is ideally infinite. A finite value of Rt is analogous to the finite open loop voltage gain in a conventional op amp.

The current applied to the inverting input node is replicated by the current conveyor so as to flow in resistor Rt. The voltage developed across Rt is buffered by the unity gain voltage follower. Voltage gain is the ratio Rt/ R_{IN}. With typical values of Rt=3MΩ and R_{IN}=50Ω, the voltage gain is about 60,000. The open loop current gain is another measure of gain and is determined by the beta product of the transistors in the voltage follower stage (see Figure 28); it is typically 40,000.

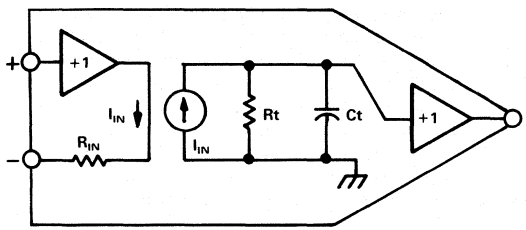


Figure 25. Equivalent Schematic

The important parameters defining ac behavior are the transcapacitance, Ct, and the external feedback resistor (not shown). The time constant formed by these components is analogous to the dominant pole of a conventional op amp, and thus cannot be reduced below a critical value if the closed loop system is to be stable. In practice, Ct is held to as low a value as possible (typically 4.5pF) so that the feedback resistor can be maximized while maintaining a fast response. The finite R_{IN} also affects the closed loop response in some applications as will be shown.

The open loop ac gain is also best understood in terms of the transimpedance rather than as an open loop voltage gain. The open loop pole is formed by Rt in parallel with Ct. Since Ct is typically 4.5pF, the open loop corner frequency occurs at about 12kHz. However, this parameter is of little value in determining the closed loop response.

Response as an Inverting Amplifier

Figure 26 shows the connections for an inverting amplifier. Unlike a conventional amplifier the transient response and the small signal bandwidth are determined primarily by the value of the external feedback resistor, R1, rather than by the ratio of R1/R2 as is customarily the case in an op amp application. This is a direct result of the low impedance at the inverting input. As with conventional op amps, the closed loop gain is −R1/R2.

The closed loop transresistance is simply the parallel sum of R1 and Rt. Since R1 will generally be in the range 500Ω to 2kΩ and Rt is about 3MΩ the closed loop transresistance will be only 0.02% to 0.07% lower than R1. This small error will often be less than the resistor tolerance.

When R1 is fairly large (above 5kΩ) but still much less than Rt, the closed loop HF response is dominated by the time constant R1Ct. Under such conditions the AD844 is over-damped and will provide only a fraction of its bandwidth potential. Because of the absence of slew rate limitations under these conditions, the circuit will exhibit a simple single pole response even under large signal conditions.

In Figure 26, R3 is used to properly terminate the input if desired. R3 in parallel with R2 gives the terminated resistance. As R1 is lowered, the signal bandwidth increases, but the time constant R1Ct becomes comparable to higher order poles in the closed loop response. Therefore, the closed loop response becomes complex, and the pulse response shows overshoot. When R2 is much larger than the input resistance, R_{IN}, at Pin 2, most of the feedback current in R1 is delivered to this input; but as R2 becomes comparable to R_{IN}, less of the feedback is absorbed at Pin 2, resulting in a more heavily damped response. Consequently, for low values of R2 it is possible to lower R1 without causing instability in the closed loop response. Table I lists combinations of R1 and R2 and the resulting frequency response for the circuit of Figure 26. Figure 13 shows the very clean and fast ±10V pulse response of the AD844.

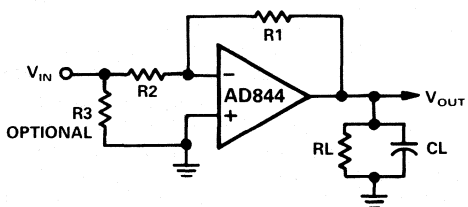


Figure 26. Inverting Amplifier

Gain	R1	R2	BW (MHz)	GBW (MHz)
−1	1kΩ	1kΩ	35	35
−1	500Ω	500Ω	60	60
−2	2kΩ	1kΩ	15	30
−2	1kΩ	500Ω	30	60
−5	5kΩ	1kΩ	5.2	26
−5	500Ω	100Ω	49	245
−10	1kΩ	100Ω	23	230
−10	500Ω	50Ω	33	330
−20	1kΩ	50Ω	21	420
−100	5kΩ	50Ω	3.2	320
+100	5kΩ	50Ω	9	900

Table I.

Response as an I-V Converter

The AD844 works well as the active element in an operational current to voltage converter, used in conjunction with an external scaling resistor, R1, in Figure 27. This analysis includes the stray capacitance, C_S, of the current source, which might be a high speed DAC. Using a conventional op amp, this capacitance forms a "nuisance pole" with R1 which destabilizes the closed loop response of the system. Most op amps are internally compensated for the fastest response at unity gain, so the pole due to R1 and C_S reduces the already narrow phase margin of the system. For example, if R1 were 2.5kΩ a C_S of 15pF would place this pole at a frequency of about 4MHz, well within the response range of even a medium speed operational amplifier. In a current feedback amp this nuisance pole is no longer determined by R1 but by the input resistance, R_{IN}. Since this is about 50Ω for the AD844, the same 15pF forms a pole 212MHz and causes little trouble. It can be shown that the response of this system is:

$$V_{OUT} = -Isig \frac{K\,R1}{(1+sTd)(1+sTn)}$$

where K is a factor very close to unity and represents the finite dc gain of the amplifier, Td is the dominant pole and Tn is the nuisance pole:

$$K = \frac{Rt}{Rt+R1}$$

$$Td = KR1Ct$$

$$Tn = R_{IN}C_S \qquad \text{(assuming } R_{IN} << R1\text{)}$$

Using typical values of R1=1kΩ and Rt=3MΩ, K is 0.9997; in other words, the "gain error" is only 0.03%. This is much less than the scaling error of virtually all DACs and can be absorbed, if necessary, by the trim needed in a precise system.

In the AD844, Rt is fairly stable with temperature and supply voltages, and consequently the effect of finite "gain" is negligible unless high value feedback resistors are used. Since that would result in slower response times than are possible, the relatively low value of Rt in the AD844 will rarely be a significant source of error.

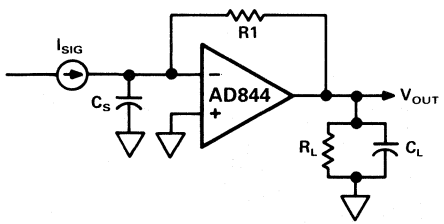


Figure 27. Current to Voltage Converter

Circuit Description of the AD844

A simplified schematic is shown in Figure 28. The AD844 differs from a conventional op amp in that the signal inputs have radically different impedance. The noninverting input (Pin 3) presents the usual high impedance. The voltage on this input is transferred to the inverting input (Pin 2) with a low offset voltage, ensured by the close matching of like polarity transistors

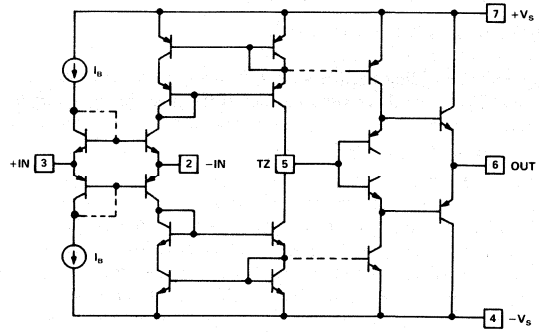


Figure 28. Simplified Schematic

operating under essentially identical bias conditions. Laser trimming nulls the residual offset voltage, down to a few tens of microvolts. The inverting input is the common emitter node of a complementary pair of grounded base stages and behaves as a current summing node. In an ideal current feedback op amp the input resistance would be zero. In the AD844 it is about 50Ω.

A current applied to the inverting input is transferred to a complementary pair of unity-gain current mirrors which deliver the same current to an internal node (Pin 5) at which the full output voltage is generated. The unity-gain complementary voltage follower then buffers this voltage and provides the load driving power. This buffer is designed to drive low impedance loads such as terminated cables, and can deliver ±50mA into a 50Ω load while maintaining low distortion, even when operating at supply voltages of only ±6V. Current limiting (not shown) ensures safe operation under short circuited conditions.

It is important to understand that the low input impedance at the inverting input is locally generated, and does not depend on feedback. This is very different from the "virtual ground" of a conventional operational amplifier used in the current summing mode which is essentially an open circuit until the loop settles. In the AD844, transient current at the input does not cause voltage spikes at the summing node while the amplifier is settling. Furthermore, all of the transient current is delivered to the slewing (TZ) node (Pin 5) via a short signal path (the grounded base stages and the wideband current mirrors).

The current available to charge the capacitance (about 4.5pF) at TZ node, *is always proportional to the input error current*, and the slew rate limitations associated with the large signal response of op amps do not occur. For this reason, the rise and fall times are almost independent of signal level. In practice, the input current will eventually cause the mirrors to saturate. When using ±15V supplies, this occurs at about 10mA (or ±2200V/μs). Since signal currents are rarely this large, classical "slew rate" limitations are absent.

This inherent advantage would be lost if the voltage follower used to buffer the output were to have slew rate limitations. The AD844 has been designed to avoid this problem, and as a result the output buffer exhibits a clean large signal transient response, free from anomalous effects arising from internal saturation.

Response as a Noninverting Amplifier

Since current feedback amplifiers are asymmetrical with regard to their two inputs, performance will differ markedly in noninverting and inverting modes. In noninverting modes, the large signal high speed behavior of the AD844 deteriorates at low gains because the biasing circuitry for the input system (not shown in Figure 28) is not designed to provide high input voltage slew rates.

However, good results can be obtained with some care. The noninverting input will not tolerate a large transient input; it must be kept below ±1V for best results. Consequently this mode is better suited to high gain applications (greater than ×10). Figure 20 shows a noninverting amplifier with a gain of 10 and a bandwidth of 30MHz. The transient response is shown in Figures 23 and 24. To increase the bandwidth at higher gains, a capacitor can be added across R2 whose value is approximately the ratio of R1 and R2 times Ct.

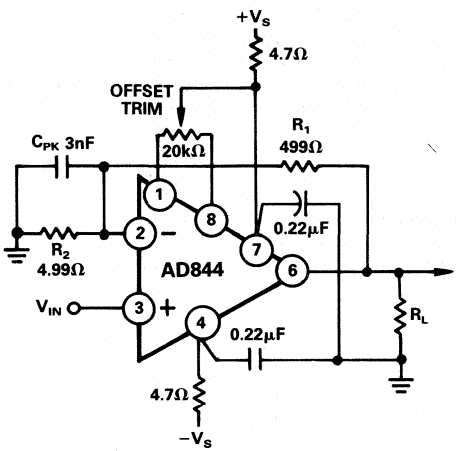


Figure 29. Noninverting Amplifier Gain=100, Optional Offset Trim Is Shown

Noninverting Gain of 100

The AD844 provides very clean pulse response at high noninverting gains. Figure 29 shows a typical configuration providing a gain of 100 with high input resistance. The feedback resistor is kept as low as practicable to maximize bandwidth, and a peaking capacitor (C_{PK}) can optionally be added to further extend the bandwidth. Figure 30 shows the small signal response with C_{PK}=3nF, R_L=500Ω and supply voltages of either ±5V or ±15V. *Gain bandwidth products of up to 900MHz can be achieved in this way.*

The offset voltage of the AD844 is laser trimmed to the 50μV level and exhibits very low drift. In practice, there is an additional offset term due to the bias current at the inverting input (I_{BN}) which flows in the feedback resistor (R1). This can optionally be nulled by the trimming potentiometer shown in Figure 29.

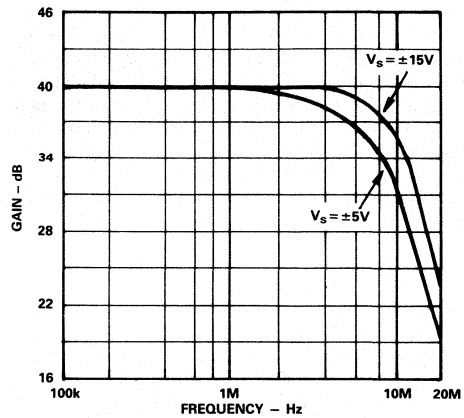


Figure 30. AC Response for Gain=100, Configuration Shown in Figure 29

USING THE AD844

Board Layout

As with all high frequency circuits considerable care must be used in the layout of the components surrounding the AD844. A ground plane, to which the power supply decoupling capacitors are connected by the shortest possible leads, is essential to achieving clean pulse response. Even a continuous ground plane will exhibit finite voltage drops between points on the plane, and this must be kept in mind in selecting the grounding points. Generally speaking, decoupling capacitors should be taken to a point close to the load (or output connector) since the load currents flow in these capacitors at high frequencies. The +In and −In circuits (for example, a termination resistor and Pin 3) must be taken to a common point on the ground plane close to the amplifier package.

Use low impedance capacitors (AVX SR305C224KAA or equivalent) of 0.22μF wherever ac coupling is required. Include either ferrite beads and/or a small series resistance (approximately 4.7Ω) in each supply line.

Input Impedance

At low frequencies, negative feedback keeps the resistance at the inverting input close to zero. As the frequency increases, the impedance looking into this input will increase from near zero to the open loop input resistance, due to bandwidth limitations, making the input seem inductive. If it is desired to keep the input impedance flatter, a series RC network can be inserted across the input. The resistor is chosen so that the parallel sum of it and R2 equals the desired termination resistance. The capacitance is set so that the pole determined by this RC network is about half the bandwidth of the op amp. This network is not important if the input resistor is much larger than the termination used, or if frequencies are relatively low. In some cases, the small peaking that occurs without the network can be of use in extending the −3dB bandwidth.

Driving Large Capacitive Loads

Capacitive drive capability is 100pF without an external network. With the addition of the network shown in Figure 31, the capacitive drive can be extended to over 10,000pF, limited by internal power dissipation. With capacitive loads, the output speed becomes a function of the overdriven output current limit. Since this is roughly ±100mA, under these conditions, the maximum slew rate into a 1000pF load is ±100V/μs. Figure 32 shows the transient response of an inverting amplifier (R1=R2=1kΩ) using the feed forward network shown in Figure 31, driving a load of 1000pF.

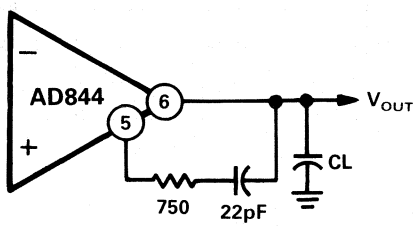


Figure 31. Feed Forward Network for Large Capacitive Loads

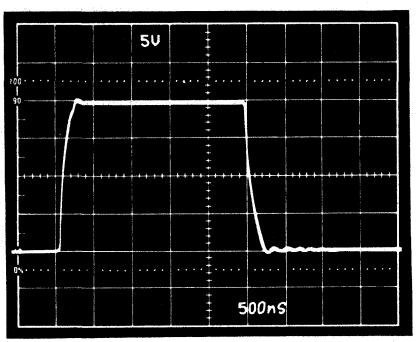


Figure 32. Driving 1000pF CL with Feed Forward Network of Figure 31

Settling Time

Settling time is measured with the circuit of Figure 33. This circuit employs a false summing node, clamped by the two Schottky diodes, to create the error signal and limit the input signal to the oscilloscope. For measuring settling time, the ratio of R6/R5 is equal to R1/R2. For unity gain, R6=R5=1kΩ, and R_L=500Ω. For the gain of −10, R5=50Ω, R6=500Ω and R_L was not used since the summing network loads the output with approximately 275Ω. Using this network in a unity-gain configuration, settling time is 100ns to 0.1% for a −5V to +5V step with C_L=10pF.

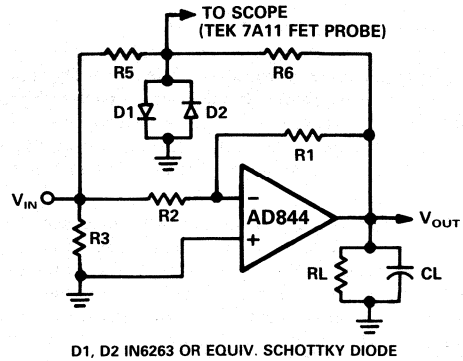


Figure 33. Settling Time Test Fixture

DC Error Calculation

Figure 34 shows a model of the dc error and noise sources for the AD844. The inverting input bias current, I_{BN}, flows in the feedback resistor. I_{BP}, the noninverting input bias current, flows in the resistance at Pin 3 (R_P), and the resulting voltage (plus any offset voltage) will appear at the inverting input. The total error, V_O, at the output is:

$$V_O=(I_{BP}\,R_P+V_{OS}+I_{BN}\,R_{IN})\left(1+\frac{R1}{R2}\right)+I_{BN}\,R1$$

Since I_{BN} and I_{BP} are unrelated both in sign and magnitude, inserting a resistor in series with the noninverting input will not necessarily reduce dc error and may actually increase it.

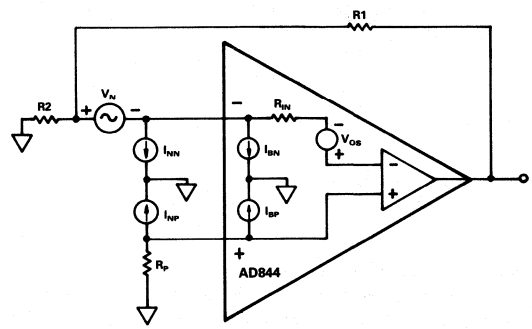


Figure 34. Offset Voltage and Noise Model for the AD844

Noise

Noise sources can be modeled in a manner similar to the dc bias currents, but the noise sources are Inn, Inp, Vn, and the amplifier-induced noise at the output, V_{ON}, is:

$$V_{ON}=\sqrt{((Inp\,R_P)^2+Vn^2)\left(1+\frac{R1}{R2}\right)^2+(Inn\,R1)^2}$$

Overall noise can be reduced by keeping all resistor values to a minimum. With typical numbers, R1=R2=1k, R_P=0, Vn=2nV/√Hz, Inp=10pA/√Hz, Inn=12pA/√Hz, V_{ON} calculates to 12nV/√Hz. The current noise is dominant in this case, as it will be in most low gain applications.

Video Cable Driver Using ±5 Volt Supplies

The AD844 can be used to drive low impedance cables. Using ±5V supplies, a 100Ω load can be driven to ±2.5V with low distortion. Figure 35a shows an illustrative application which provides a noninverting gain of 2, allowing the cable to be reverse-terminated while delivering an overall gain of +1 to the load. The −3dB bandwidth of this circuit is typically 30MHz. Figure 35b shows a differential gain and phase test setup. In video applications, differential-phase and differential-gain characteristics are often important. Figure 35c shows the variation in phase as the load voltage varies. Figure 35d shows the gain variation.

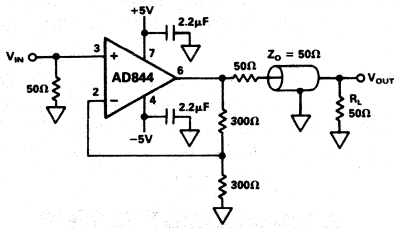


Figure 35a. The AD844 as a Cable Driver

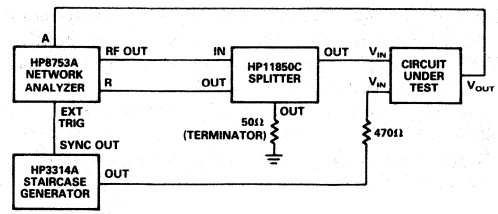


Figure 35b. Differential Gain/Phase Test Setup

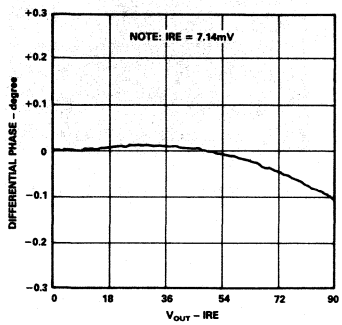


Figure 35c. Differential Phase for the Circuit of Figure 35a

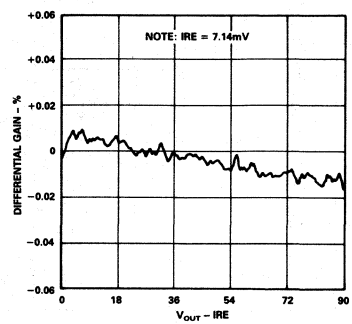


Figure 35d. Differential Gain for the Circuit of Figure 35a

High Speed DAC Buffer

The AD844 performs very well in applications requiring current-to-voltage conversion. Figure 36 shows connections for use with the AD568 current output DAC. In this application the bipolar offset is used so that the full scale current is ±5.12mA, which generates an output of ±5.12V using the 1kΩ application resistor on the AD568. Figure 37 shows the full scale transient response. Care is needed in power supply decoupling and grounding techniques to achieve the full 12-bit accuracy and realize the fast settling capabilities of the system. The unmarked capacitors in this figure are 0.1µF ceramic (for example, AVX Type SR305C104KAA), and the ferrite inductors should be about 2.5µH (for example, Fair-Rite Type 2743002122). The AD568 data sheet should be consulted for more complete details about its use.

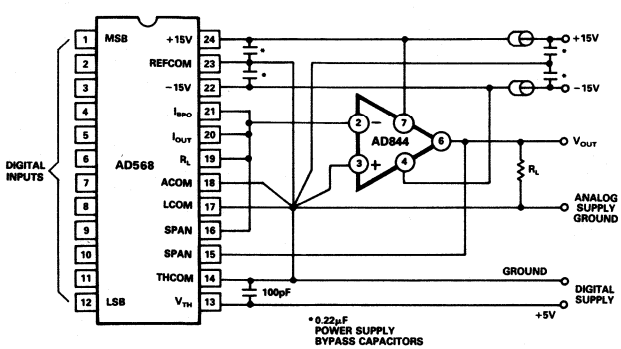


Figure 36. High Speed DAC Amplifier

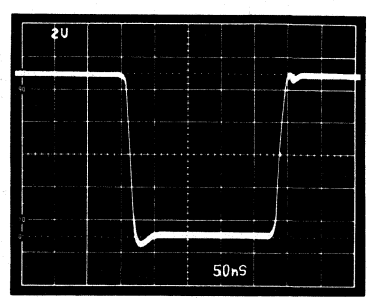


Figure 37. DAC Amplifier Full-Scale Transient Response

20MHz Variable Gain Amplifier

The AD844 is an excellent choice as an output amplifier for the AD539 multiplier, in all of its connection modes. (See AD539 data sheet for full details.) Figure 38 shows a simple multiplier providing the output:

$$V_W = -\frac{V_X V_Y}{2V}$$

where V_X is the "gain control" input, a positive voltage of from 0 to +3.2V (max) and V_Y is the "signal voltage", nominally ±2V FS but capable of operation up to ±4.2V. The peak output in this configuration is thus ±6.7V. Using all four of the internal application resistors provided on the AD539 in parallel results in a feedback resistance of 1.5kΩ, at which value the bandwidth of the AD844 is about 22MHz, and is essentially independent of V_X. The gain at V_X=3.16V is +4dB.

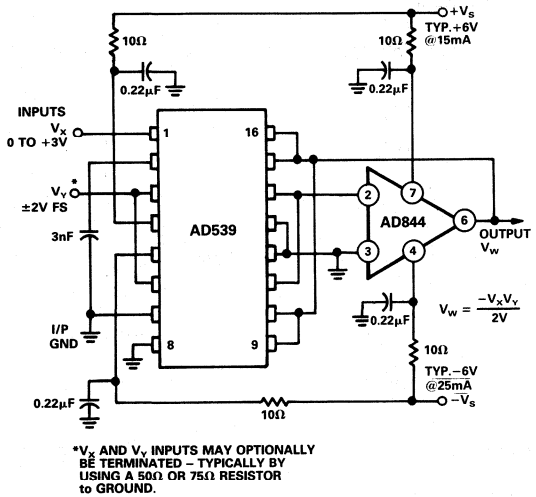


Figure 38. 20MHz VGA Using the AD539

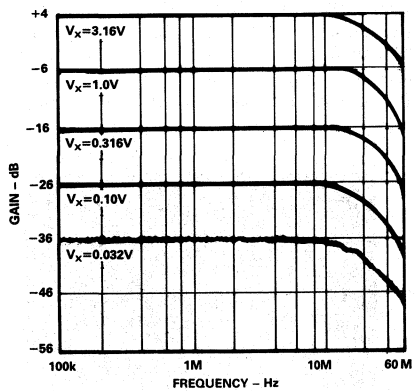


Figure 39. VGA AC Response

Figure 39 shows the small signal response for a 50dB gain control range (V_X=+10mV to +3.16V). At small values of V_X, capacitive feedthrough on the PC board becomes troublesome, and very careful layout techniques are needed to minimize this problem. A ground strip between the pins of the AD539 will be helpful in this regard. Figure 40 shows the response to a 2V pulse on V_Y for V_X=+1V, +2V and +3V. For these results, a load resistor of 500Ω was used and the supplies were ±9V. The multiplier will operate from supplies between ±4.5V and ±16.5V.

Disconnecting Pins 9 and 16 on the AD539 alters the denominator in the above expression to 1V, and the bandwidth will be approximately 10MHz, with a maximum gain of 10dB. Using only Pin 9 or Pin 16 results in a denominator of 0.5V, a bandwidth of 5MHz and a maximum gain of 16dB.

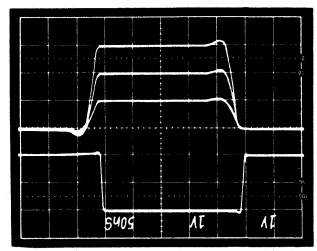


Figure 40. VGA Transient Response with V_X=1V, 2V, and 3V

Precision, 16 MHz CBFET Op Amp

AD845

FEATURES

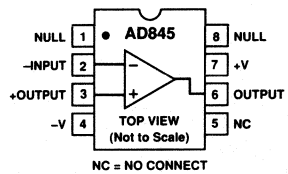
Replaces Hybrid Amplifiers in Many Applications

AC PERFORMANCE:
Settles to 0.01% in 350 ns
100 V/μs Slew Rate
12.8 MHz min Unity-Gain Bandwidth
1.75 MHz Full-Power Bandwidth at 20 V p–p

DC PERFORMANCE:
0.25 mV max Input Offset Voltage
5 μV/°C max Offset Voltage Drift
0.5 nA Input Bias Current
250 V/mV min Open-Loop Gain
4 μV p–p max Voltage Noise, 0.1 Hz to 10 Hz
94 dB min CMRR
Available in Plastic Mini-DIP, Hermetic Cerdip and SOIC Packages. Also Available in Tape and Reel in Accordance with EIA-481A Standard

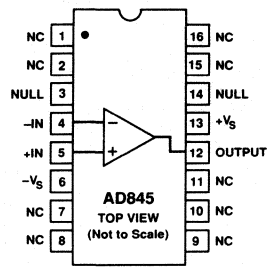
CONNECTION DIAGRAMS

Plastic Mini-DIP (N) Package and Cerdip (Q) Package



NC = NO CONNECT

16-Pin SOIC (R-16) Package



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD845 is a fast, precise, N channel JFET input, monolithic operational amplifier. It is fabricated using Analog Devices' complementary bipolar (CB) process. Advanced laser-wafer trimming technology enables the very low input offset voltage and offset voltage drift performance to be realized. This precision, when coupled with a slew rate of 100 V/μs, a stable unity-gain bandwidth of 16 MHz, and a settling time of 350 ns 0.01%—while driving a parallel load of 100 pF and 500 Ω—represents a combination of features unmatched by any FET input IC amplifier. The AD845 can easily be used to upgrade many existing designs which use BiFET or FET input hybrid amplifiers and, in some cases, those which use bipolar input op amps.

The AD845 is ideal for use in applications such as active filters, high speed integrators, photo diode preamps, sample-and-hold amplifiers, log amplifiers, and in buffering A/D and D/A converters. The 250 μV max input offset voltage makes offset nulling unnecessary in many applications. The common-mode rejection ratio of 110 dB over a ±10 V input voltage range represents exceptional performance for a JFET input high speed op amp. This, together with a minimum open-loop gain of 250 V/mV ensures that 12-bit performance is achieved, even in unity-gain buffer circuits.

The AD845 conforms to the standard op amp pinout except that offset nulling is to V+. The AD845J and AD845K grade devices are available specified to operate over the commercial 0 to +70°C temperature range. AD845A and AD845B devices are specified for operation over the −40°C to +85°C industrial temperature range. The AD845S is specified to operate over the full military temperature range of −55°C to +125°C. Both the industrial and military versions are available in 8-pin cerdip packages. The commercial version is available in an 8-pin plastic mini-DIP and 16-pin SOIC; "J" and "S" grade chips are also available.

PRODUCT HIGHLIGHTS

1. The high slew rate, fast settling time, and dc precision of the AD845 make it ideal for high speed applications requiring 12-bit accuracy.
2. The performance of circuits using the LF400, HA2520/2/5, HA2620/2/5, 3550, OPA605, and LH0062 can be upgraded in most cases.
3. The AD845 is unity-gain stable and internally compensated.
4. The AD845 is specified while driving 100 pF/500 Ω loads.

AD845—SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD845J/A Min	AD845J/A Typ	AD845J/A Max	AD845K/B Min	AD845K/B Typ	AD845K/B Max	AD845S Min	AD845S Typ	AD845S Max	Units
INPUT OFFSET VOLTAGE[1]											
Initial Offset			0.7	**1.5**		0.1	**0.25**		0.25	**1.0**	mV
	T_{min}–T_{max}			2.5			**0.4**			2.0	mV
Offset Drift				20		1.5	**5.0**			**10**	μV/°C
INPUT BIAS CURRENT[2]											
Initial	V_{CM} = 0 V		0.75	**2**		0.5	**1**		0.75	**2**	nA
	T_{min}–T_{max}			45/75			**18/38**			**500**	nA
INPUT OFFSET CURRENT											
Initial	V_{CM} = 0 V		25	**300**		15	**100**		25	**300**	pA
	T_{min}–T_{max}			3/6.5			**1.2/2.6**			**20**	nA
INPUT CHARACTERISTICS											
Input Resistance			10^{11}			10^{11}			10^{11}		kΩ
Input Capacitance			4.0			4.0			4.0		pF
INPUT VOLTAGE RANGE											
Differential			±20			±20			±20		V
Common Mode		**±10**	+ 10.5/−13		**+10**	+10.5/−13		**±10**	+10.5/−13		V
Common-Mode Rejection	V_{CM} = ±10 V	**86**	110		**94**	113		**86**	110		dB
INPUT VOLTAGE NOISE	0.1 to 10 Hz		4			4			4		μV p–p
	f = 10 Hz		80			80			80		nV/√Hz
	f = 100 Hz		60			60			60		nV/√Hz
	f = 1 kHz		25			25			25		nV/√Hz
	f = 10 kHz		18			18			18		nV/√Hz
	f = 100 kHz		12			12			12		nV/√Hz
INPUT CURRENT NOISE	f = 1 kHz		0.1			0.1			0.1		pA/√Hz
OPEN-LOOP GAIN	V_O = ±10 V										
	R_{LOAD}≥2 kΩ	**200**	500		**250**	500		**200**	500		V/mV
	R_{LOAD}≥500 Ω	**100**	250		**125**	250		**100**	250		V/mV
	T_{min}–T_{max}	70			75			50			V/mV
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD}≥500 Ω	**±12.5**			**±12.5**			**±12.5**			V
Current	Short Circuit		50			50			50		mA
Output Resistance	Open Loop		5			5			5		Ω
FREQUENCY RESPONSE											
Small Signal	Unity Gain	12.8	16		13.6	16		13.6	16		MHz
Full Power Bandwidth[3]	V_O = ±10 V										
	R_{LOAD} = 500 Ω		1.75			1.75			1.75		MHz
Rise Time			20			20			20		ns
Overshoot			20			20			20		%
Slew Rate		**80**	100		**94**	100		**94**	100		V/μs
Settling Time	10 V Step										
	C_{LOAD} = 100 pF										ns
	R_{LOAD} = 500 Ω										ns
	to 0.01%		350			350	500		350	500	ns
	to 0.1%		250			250			250		ns
DIFFERENTIAL GAIN	f = 4.4 MHz		0.04			0.04			0.04		%
DIFFERENTIAL PHASE	f = 4.4 MHz		0.02			0.02			0.02		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		**±4.75**		**±18**	**±4.75**		**±18**	**±4.75**		**±18**	V
Rejection Ratio	V_S = ±5 to ±15 V	**88**	110		**95**	113		**88**	110		dB
Quiescent Current	T_{min} to T_{max}		10	12		10	**12**		10	**12**	mA

NOTES

[1]Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C.

[3]FPBW=slew rate/2π V peak.

[4]"S" grade T_{min}-T_{max} are tested with automatic test equipment at T_A = −55°C and T_A = +125°C.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final electrical test. Results from these tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

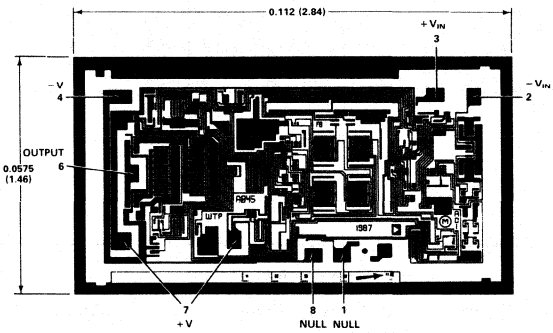
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
  Plastic Mini-DIP . . . . . 1.6 Watts
  Cerdip . . . . . 1.4 Watts
  16-Pin SOIC . . . . . 1.5 Watts
Input Voltage . . . . . $\pm V_S$
Output Short-Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range
  Q . . . . . −65°C to +150°C
  N, R . . . . . −65°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Mini-DIP package: θ_{JA} = 100°C/W; cerdip package: θ_{JA} = 110°C/W; SOIC package: θ_{JA} = 100°C/W.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option[1]
AD845JN	0°C to +70°C	8-Pin Plastic Mini-DIP	N-8
AD845KN	0°C to +70°C	8-Pin Plastic Mini-DIP	N-8
AD845JR	0°C to +70°C	16-Pin SOIC	R-16
AD845AQ	−40°C to +85°C	8-Pin Cerdip	Q-8
AD845BQ	−40°C to +85°C	8-Pin Cerdip	Q-8
AD845SQ	−55°C to +125°C	8-Pin Cerdip	Q-8
AD845SQ/883B	−55°C to +125°C	8-Pin Cerdip	Q-8
AD845J Chips	0°C to +70°C	Die	
AD845S Chips	−55°C to +125°C	Die	
AD845JR-Reel	0°C to +70°C	Tape & Reel	

NOTE
[1]N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.

AD845—Typical Characteristics

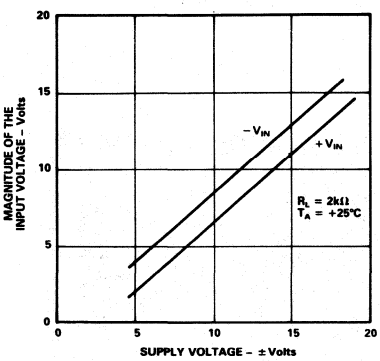


Figure 1. Input Voltage Swing vs. Supply Voltage

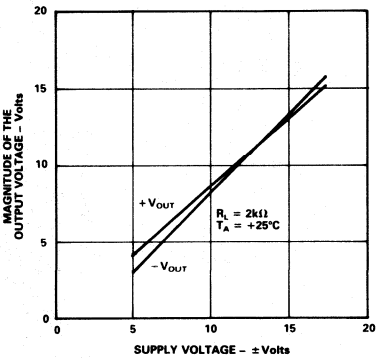


Figure 2. Output Voltage Swing vs. Supply Voltage

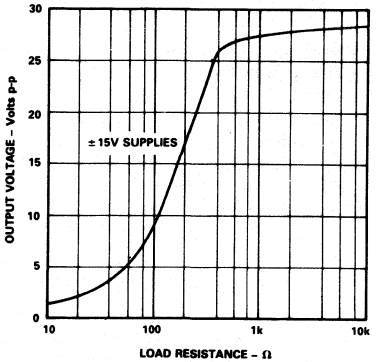


Figure 3. Output Voltage Swing vs. Resistive Load

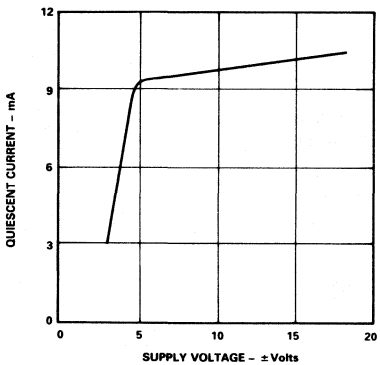


Figure 4. Quiescent Current vs. Supply Voltage

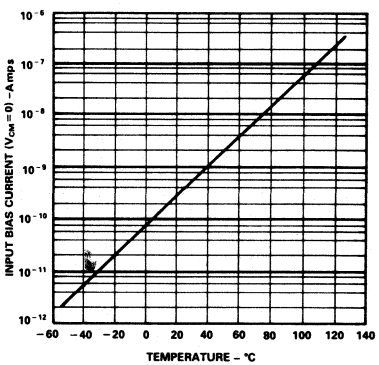


Figure 5. Input Bias Current vs. Temperature

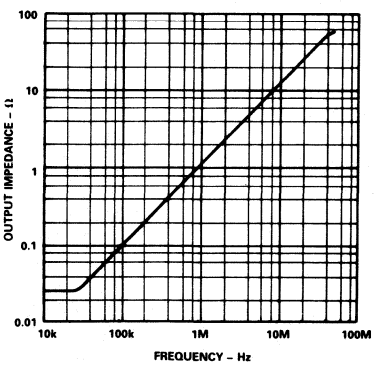


Figure 6. Magnitude of Output Impedance vs. Frequency

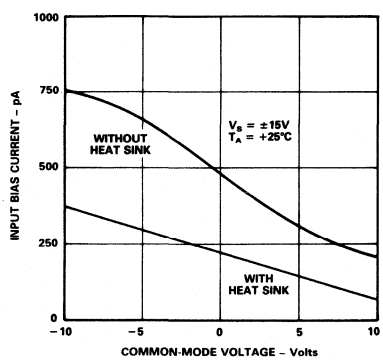


Figure 7. Input Bias Current vs. Common-Mode Voltage

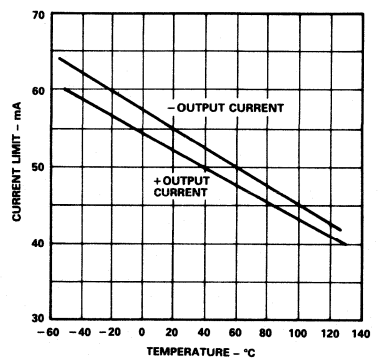


Figure 8. Short-Circuit Current Limit vs. Temperature

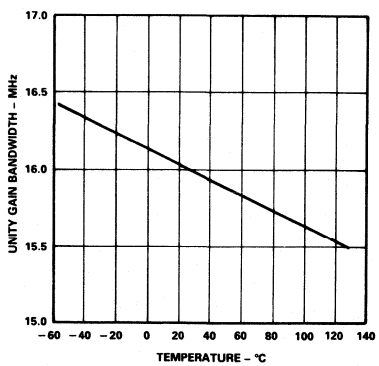


Figure 9. Unity-Gain Bandwidth vs.Temperature

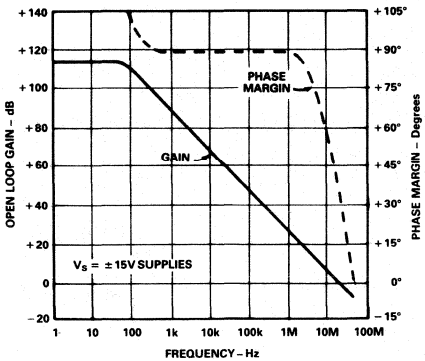


Figure 10. Open-Loop Gain and Phase Margin vs. Frequency

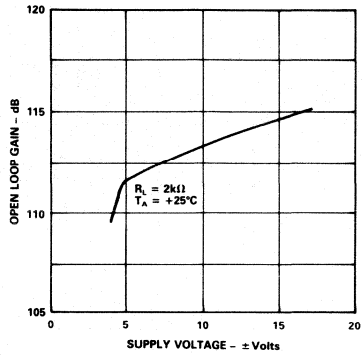


Figure 11. Open-Loop Gain vs. Supply Voltage

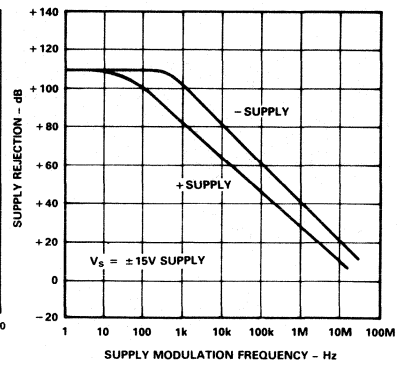


Figure 12. Power Supply Rejection vs. Frequency

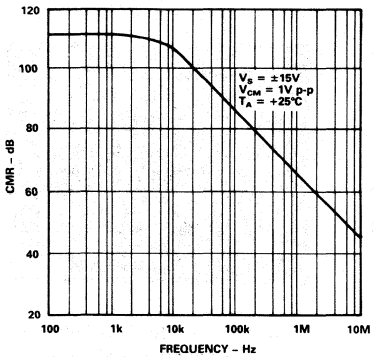


Figure 13. Common-Mode Rejection vs. Frequency

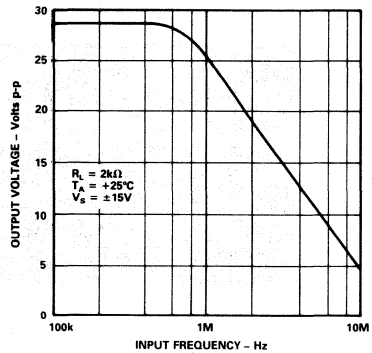


Figure 14. Large Signal Frequency Response

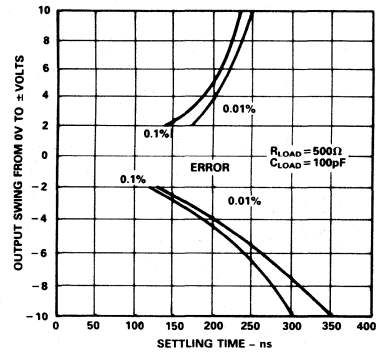


Figure 15. Output Swing and Error vs. Settling Time

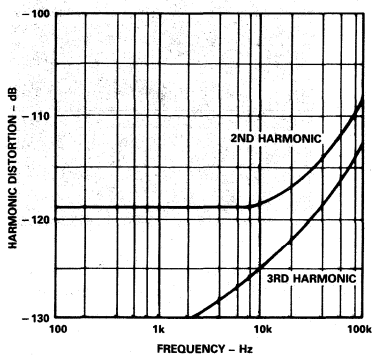


Figure 16. Harmonic Distortion vs. Frequency

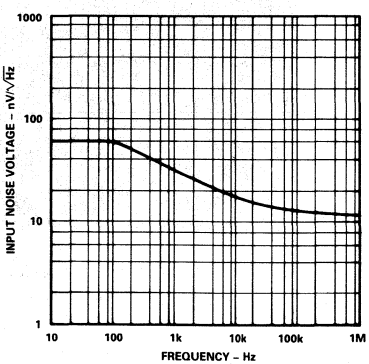


Figure 17. Input Noise Voltage Spectral Density

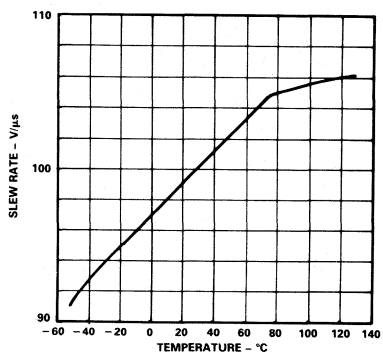


Figure 18. Slew Rate vs. Temperature

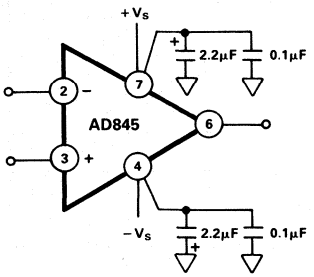


Figure 19. Recommended Power Supply Bypassing

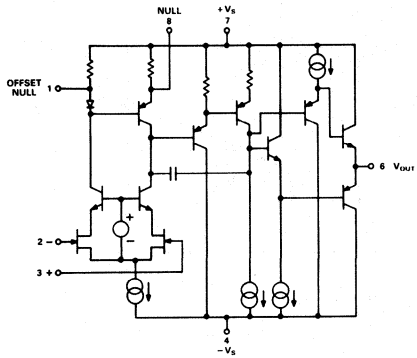


Figure 20. AD845 Simplified Schematic

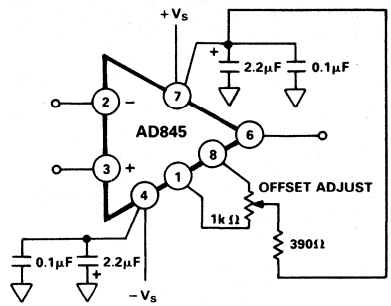


Figure 21. Offset Null Configuration

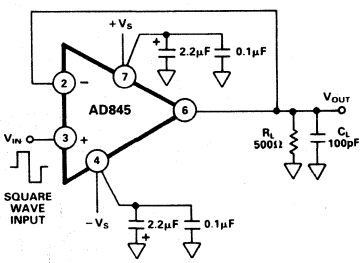


Figure 22a. Unity-Gain Follower

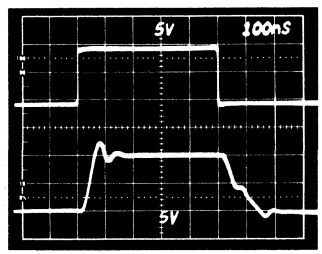


Figure 22b. Unity-Gain Follower Large Signal Pulse Response

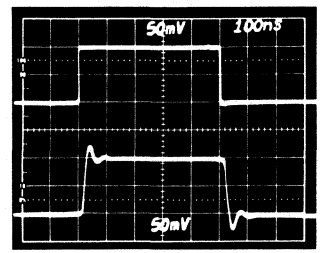


Figure 22c. Unity-Gain Follower Small Signal Pulse Response

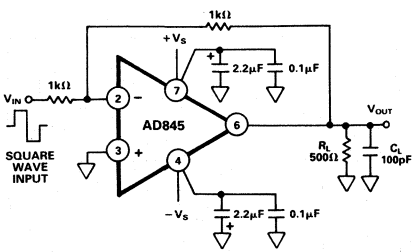


Figure 23a. Unity-Gain Inverter

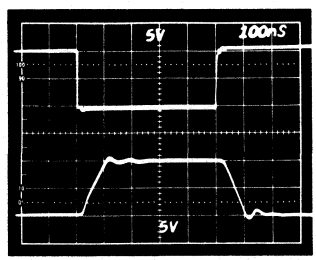


Figure 23b. Unity-Gain Inverter Large Signal Pulse Response

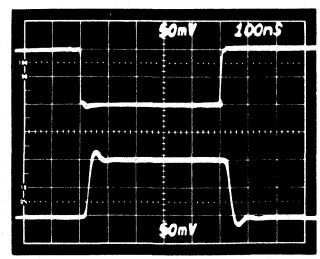


Figure 23c. Unity-Gain Inverter Small Signal Pulse Response

MEASURING AD845 SETTLING TIME

The Figure 24 shows the AD845 settling time performance. This measurement was accomplished by driving the amplifier in the unity-gain inverting mode with a fast pulse generator. The input summing junction was measured using false nulling techniques.

Settling time is defined as:

> The interval of time from the application of an ideal step function input until the closed-loop amplifier output has entered and remains within a specified error band.

Components of settling time include:

1. Propagation time through the amplifier
2. Slewing time to approach the final output value
3. Recovery time from overload associated with the slewing
4. Linear settling to within a specified error band.

These individual components can easily be seen in Figure 24. Settling time is extremely important in high speed applications where the current output of a DAC must be converted to a voltage. When driving a 500 Ω load in parallel with a 100 pF capacitor, the AD845 settles to 0.1% in 250 ns and to 0.01% in 310 ns.

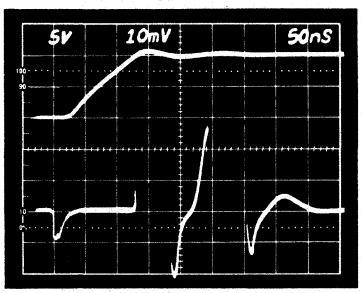


Figure 24. Settling Characteristics 0 to 10 V Step
Upper Trace: Output of AD845 Under Test (5 V/Div)
Lower Trace: Error Voltage (1 mV/Div)

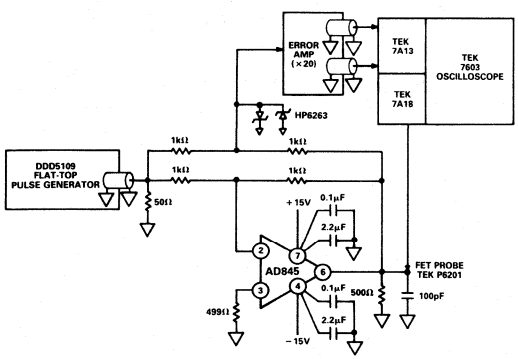


Figure 25. Settling Time Test Circuit

A HIGH SPEED INSTRUMENTATION AMP

The three op amp instrumentation amplifier circuit shown in Figure 26 can provide a range of gains from unity up to 1000 and higher. The instrumentation amplifier configuration features high common-mode rejection, balanced differential inputs and stable, accurately defined gain. Low input bias currents and fast settling are achieved with the FET input AD845.

Most monolithic instrumentation amplifiers do not have the high frequency performance of the circuit in Figure 26. The circuit bandwidth is 10.9 MHz at a gain of 1 and 2.6 MHz at a gain of 10; settling time for the entire circuit is 900 ns to 0.01% for a 10 V step (Gain = 10).

The capacitors employed in this circuit greatly improve the amplifier's settling time and phase margin.

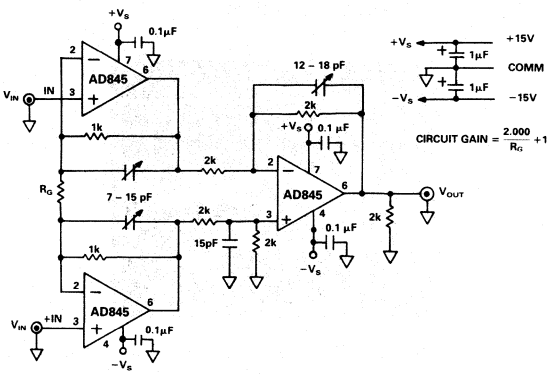


Figure 26. High Performance, High Speed Instrumentation Amplifier

3 OP-AMP IN-AMP

Gain	RG	Small Signal Bandwidth	Settling Time to 0.01%
1	Open	10.9 MHz	500 ns
2	2k	8.8 MHz	500 ns
10	226Ω	2.6 MHz	900 ns
100	20Ω	290 kHz	7.5 μs

Note: Resistors around the amplifiers' input pins need to be small enough in value so that the RC time constant they form, with stray circuit capacitance, does not reduce circuit bandwidth.

Table I. Performance Summary for the Three Op Amp Instrumentation Amplifier Circuit

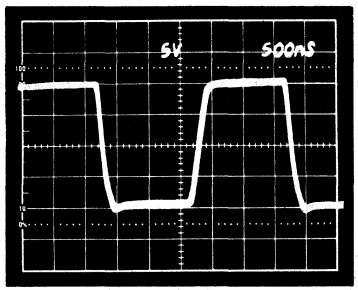


Figure 27. The Pulse Response of the Three Op Amp Instrumentation Amplifier. Gain = 1, Horizontal Scale: 0.5 ms/Div; Vertical Scale: 5 V/Div

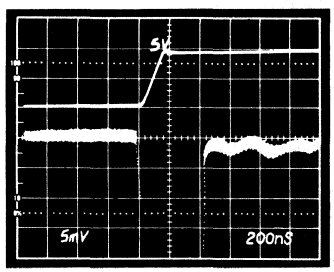


Figure 28a. Settling Time of the Three Op Amp Instrumentation Amplifier. Horizontal Scale:200 ns/Div; Vertical Scale, Positive Pulse Input: 5 V/Div; Output Settling: 1 mV/Div

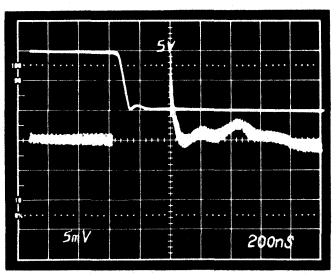


Figure 28b. Settling Time of the Three Op Amp Instrumentation Amplifier. Horizontal Scale: 200 ns/Div; Vertical Scale, Negative Pulse Input: 5 V/Div; Output Settling: 1 mV/Div

DRIVING THE ANALOG INPUT OF AN A/D CONVERTER

An op amp driving the analog input of an A/D converter, such as that shown in Figure 29, must be capable of maintaining a constant output voltage under dynamically changing load conditions. In successive-approximation converters, the input current is compared to a series of switched trial currents. The comparison point is diode clamped but may deviate several hundred millivolts resulting in high frequency modulation of A/D input current. The output impedance of a feedback amplifier is made artificially low by the loop gain. At high frequencies, where the loop gain is low, the amplifier output impedance can approach its open-loop value. Most IC amplifiers exhibit a minimum open-loop output impedance of 25 Ω due to current limiting resistors. A few hundred microamps reflected from the change in converter loading can introduce errors in instantaneous input voltage. If the A/D conversion speed is not excessive and the bandwidth of the amplifier is sufficient, the amplifier's output will return to the nominal value before the converter makes its comparison. However, many amplifiers have relatively narrow bandwidth yielding slow recovery from output transients. The AD845 is ideally suited to drive high resolution A/D converters with 5 μs on longer conversion times since it offers both wide bandwidth and high open-loop gain.

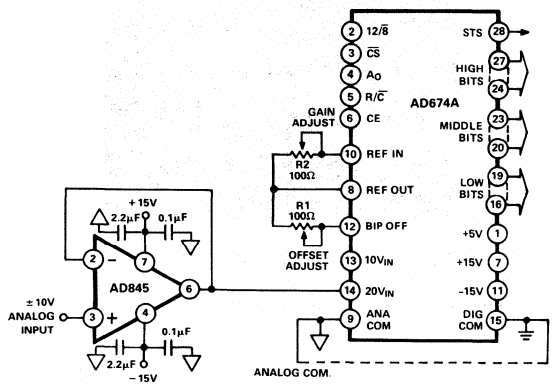


Figure 29. AD845 As ADC Unity Gain Buffer

450 V/μs, Precision, Current-Feedback Op Amp

AD846

FEATURES

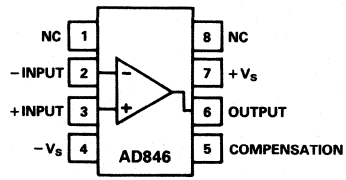
AC PERFORMANCE
- Small Signal Bandwidth: 80 MHz (A_V = −1)
- Slew Rate: 450 V/μs
- Full Power Bandwidth: 6.8 MHz at 20 V p-p, R_L = 500 Ω
- Fast Settling: for 10 V Step: 110 ns to 0.01%, 80 ns to 0.1%
- Differential Gain: <0.01% @ 4.4 MHz
- Differential Phase: <0.028° @ 4.4 MHz
- Total Harmonic Distortion (THD): 0.0005% @ 100 kHz
- Open-Loop Transimpedance: 200 MΩ
- Input Voltage Noise: 2 nV/√Hz

DC PERFORMANCE
- Input Offset Voltage: 75 μV max (B Grade)
- Input Offset Drift: 3.5 μV/°C max (B Grade)
- Quiescent Supply Current: 6.5 mA max

APPLICATIONS
- High Speed DAC Buffers
- Multiflash ADC Error Amplifiers
- Flash ADC Buffers
- Coaxial Cable Drivers
- High Performance Audio Circuitry
- Available in Plastic Mini-DIP, Hermetic Cerdip, and Hermetic Metal Can Packages
- MIL-STD-883B Parts Available

CONNECTION DIAGRAM

Plastic Mini-DIP (N) Package
and
Cerdip (Q) Package



NC = NO CONNECT
TOP VIEW

PRODUCT DESCRIPTION

The AD846 is a monolithic, very high speed operational amplifier offering high performance. Although technically classed as a current-feedback or transimpedance amplifier, it may be used in much the same way as traditional op amps while providing significant performance benefits. Employing Analog Devices' junction isolated complementary bipolar (CB) process, the AD846 achieves true "12-bit" (0.01%) precision on critical ac and dc parameters, a level of performance unmatched by amplifiers fabricated using either the dielectrically isolated (DI) or other bipolar processes.

The AD846 offers significant advantages over conventional high speed operational amplifiers. It maintains a nearly constant bandwidth and settling time to 0.01% over a wide range of closed-loop gains. This makes the AD846 ideal for amplifying the residue in multiple-pass analog-to-digital converters.

Other advantages include: low input errors and high open-loop transresistance (200 MΩ) into a 500 Ω load, ensuring true 12-bit dc accuracy for closed-loop gains from −1 to gains greater than −100. This combination of ac and dc performance makes the AD846 an excellent choice for buffering precision high speed DACs and flash ADCs.

The AD846 is available in three performance grades. The AD846A and AD846B are rated over the industrial temperature range of −40°C to +85°C. The AD846S is rated over the full military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev C.

Extended reliability PLUS screening is available specified over the commercial temperature range. PLUS screening includes 168 hour burn-in as well as other environmental and physical tests. The AD846 is available in two types of 8-pin package: plastic mini-DIP and hermetic cerdip. "A" and "S" grade chips are also available.

PRODUCT HIGHLIGHTS

1. The AD846 achieves settling times of 110 ns to 0.01% for gains of −1 to −10, with a 450 V/μs slew rate, while consuming only 5 mA of supply current.
2. For closed-loop gains of −1 to −100, the high speed performance of the AD846 is achieved without sacrificing full 12-bit dc precision.
3. The AD846 is well suited to line driver and video buffer applications where the properties of low distortion and high slew rate are required.

AD846—SPECIFICATIONS (@ +25°C and ±15 V dc, unless otherwise noted)

Model	Conditions	AD846A Min	AD846A Typ	AD846A Max	AD846B Min	AD846B Typ	AD846B Max	AD846S Min	AD846S Typ	AD846S Max	Units
INPUT OFFSET VOLTAGE[1]											
Initial			25	**200**		25	**75**		25	**200**	μV
T_{min}–T_{max}			50	350		50	**125**		100	**350**	μV
vs. Temperature			0.8	5		0.8	3.5		1	5.5	μV/°C
vs. Supply (PSRR)	5 V–18 V[2]										
Initial		**110**	125		**120**	125		**110**	125		dB
T_{min}–T_{max}		110	120		**116**	120		**94**	116		dB
vs. Common Mode (CMRR)	V_{CM} = ±10 V										
Initial		**110**	125		**120**	125		**110**	125		dB
T_{min}–T_{max}		110	120		**116**	120		**94**	116		dB
INPUT BIAS CURRENT[3]											
–Input Bias Current											
Initial			150	**450**		100	**250**		150	**450**	nA
T_{min}–T_{max}			450	1200		400	**750**		1000	**1500**	nA
vs. Temperature			6	20		6	**17**		9	20	nA/°C
vs. Supply	5 V–18 V[2]										
Initial			9	**15**		9	**10**		9	**15**	nA/V
T_{min}–T_{max}			11	20		11	**15**		11	**25**	nA/V
vs. Common Mode	V_{CM} = ±10 V										
Initial			5	**10**		3	**5**		5	**10**	nA/V
T_{min}–T_{max}			5	15		3	**7**		5	**20**	nA/V
+Input Bias Current											
Initial			3	**15**		3	**5**		3	**15**	μA
T_{min}–T_{max}			4	20		4	**7**		5	**20**	μA
vs. Temperature			15	80		15	45		15	80	nA/°C
vs. Supply	5 V–18 V[2]										
Initial			5	**15**		5	**10**		5	**15**	nA/V
T_{min}–T_{max}			5	20		5	**15**		5	**20**	nA/V
vs. Common Mode	V_{CM} = ±10 V										
Initial			5	**15**		3	**10**		5	**15**	nA/V
T_{min}–T_{max}			5	15		3	**10**		5	**20**	nA/V
INPUT CHARACTERISTICS											
Input Resistance											
–Input			50			50			50		Ω
+Input			10			10			10		kΩ
Input Capacitance											
–Input			2			2			2		pF
+Input			2			2			2		pF
INPUT VOLTAGE RANGE											
Common Mode		±10			±10			±10			V
INPUT VOLTAGE NOISE	F = 1 kHz		2			2			2		nV/√Hz
Input Current Noise											
–Input	1 kHz		20			20			20		pA/√Hz
+Input	1 kHz		6			6			6		pA/√Hz
OPEN LOOP TRANSRESISTANCE	V_{OUT} = ±10 V										
	R_{LOAD} = 500 Ω	**100**	200		**150**	200		**100**	200		MΩ
	T_{min}–T_{max}	50			**75**			**50**			MΩ
OUTPUT CHARACTERISTICS											
Voltage	R_{LOAD} = 500 Ω	**±10**			**±10**			**±10**			V
Current	Short Circuit		65			65			65		mA
Output Resistance	Open Loop		16			16			16		Ω
FREQUENCY RESPONSE											
Small Signal Bandwidth	A_V = −1 R_F = 1k		80			80			80		MHz
(−3dB)	A_V = −10 R_F = 875 Ω		31			31			31		MHz
	A_V = −30 R_F = 875 Ω		15			15			15		MHz
Full Power Bandwidth[4]	V_{OUT} = 20 V p–p										
	R_L = 500 Ω		6.8			6.8			6.8		MHz
Rise Time	A_V = −1		10			10			10		ns
Overshoot	A_V = −1		20			20			20		%
Slew Rate	A_V = −1		450			450			450		V/μs
Settling Time											
10 V Step, A_V = −1	to 0.1%		80			80			80		ns
	to 0.01%		110			110			110		ns
TOTAL HARMONIC DISTORTION[5]	F = 100 kHz		0.0005			0.0005			0.0005		%

Model	Conditions	AD846A Min	AD846A Typ	AD846A Max	AD846B Min	AD846B Typ	AD846B Max	AD846S Min	AD846S Typ	AD846S Max	Units
DIFFERENTIAL GAIN	F = 4.4 MHz, R_L = 100 Ω		0.01			0.01			0.01		%
DIFFERENTIAL PHASE	F = 4.4 MHz, R_L = 100 Ω		0.028			0.028			0.028		Degree
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		±5		±18	±5		±18	±5		±18	V
Quiescent Current	T_{min}–T_{max}		5	6.5		5	6.5		5	7	mA
TRANSISTOR COUNT			72			72			72		

NOTES
[1]Input Offset Voltage Specifications are guaranteed after 5 minutes at T_A = +25°C.
[2]Test Conditions: $+V_S$ = 15 V, $-V_S$ = 5 V to 18 V and $+V_S$ = 5 V to 18 V, $-V_S$ = 15 V.
[3]Bias Current Specifications are guaranteed maximum after 5 minutes at T_A = +25°C.
[4]FPBW = Slew Rate/2 π V_{PEAK}.
[5]Total Harmonic Distortion.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
  Plastic Package . . . . . 1.5 W
  Cerdip Package . . . . . 1.3 W
Common-Mode Input Voltage, Max Safe . . . . . $|V_S|$ −3 V
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . ±1 V
Continuous Input Current
  Inverting or Noninverting . . . . . 2.0 mA
Storage Temperature Range (Q) . . . . . −65°C to +150°C
Storage Temperature Range (N) . . . . . −65°C to +125°C
Operating Temperature Range
  AD846A/B . . . . . −40°C to +85°C
  AD846S . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Maximum internal power dissipation is specified so that T_J does not exceed +175°C at an ambient temperature of +25°C, derate cerdip (Q) package at 8.7 mW/°C and plastic (N) package at 10 mW/°C.
Plastic Package: θ_{JA} = 100°C/Watt, θ_{JC} =33°C/W.
Cerdip Package: θ_{JA} = 110°C/Watt, θ_{JC} = 30°C/W.

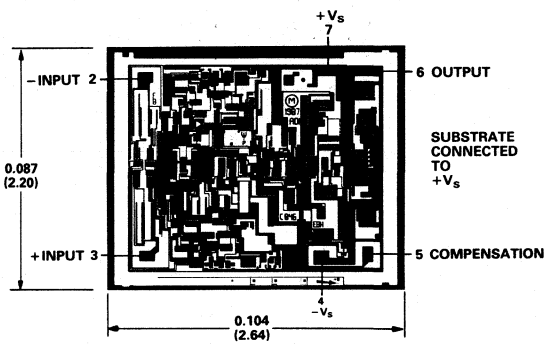
ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
AD846AN	−40°C to +85°C	N-8
AD846BN	−40°C to +85°C	N-8
AD846AQ	−40°C to +85°C	Q-8
AD846BQ	−40°C to +85°C	Q-8
AD846SQ	−55°C to +125°C	Q-8
AD846SQ/883B	−55°C to +125°C	Q-8

NOTES
[1]"A" and "S" grade chips are also available.
[2]N = Plastic DIP Package; Q = Cerdip Package. For outline information see Package Information section.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Consult factory for latest dimensions.



AD846 — Typical Characteristics

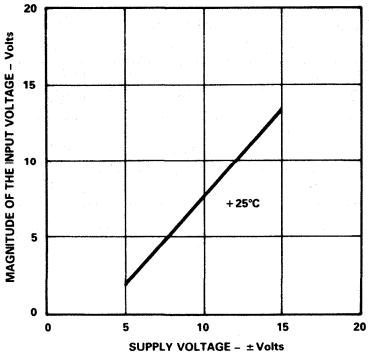


Figure 1. Input Voltage Swing vs. Supply

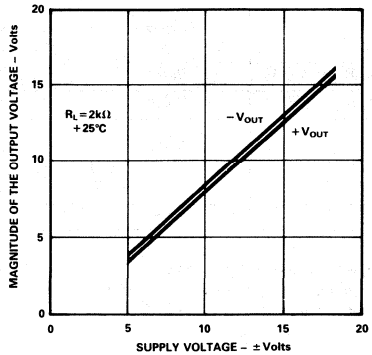


Figure 2. Output Voltage Swing vs. Supply

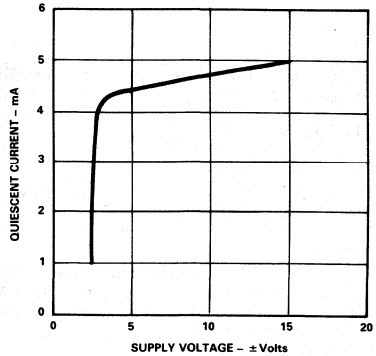


Figure 3. Quiescent Current vs. Supply Voltage

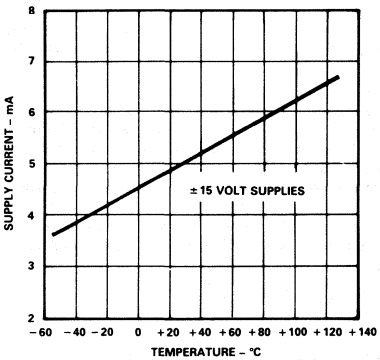


Figure 4. Quiescent Supply Current vs. Temperature

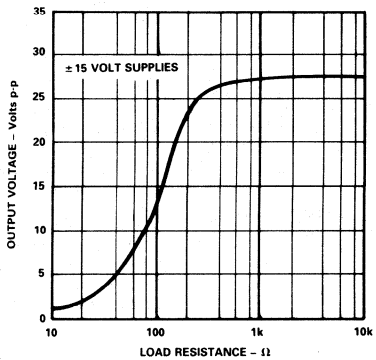


Figure 5. Output Voltage Swing vs. Resistive Load

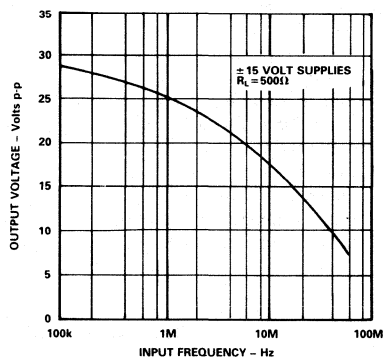


Figure 6. Large Signal Frequency Response

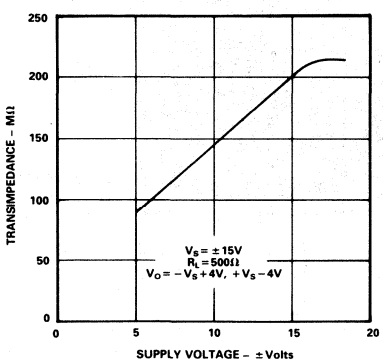


Figure 7. Open-Loop Trans-impedance vs. Supply

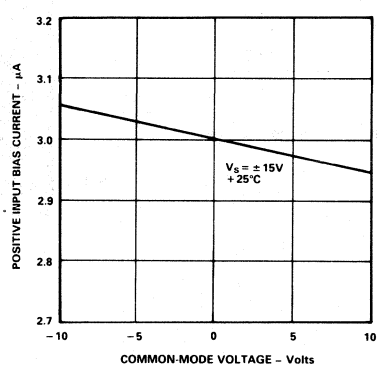


Figure 8. Positive Input Bias Current vs. Common-Mode Voltage

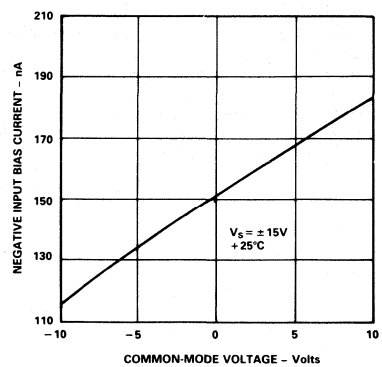


Figure 9. Negative Input Bias Current vs. Common-Mode Voltage

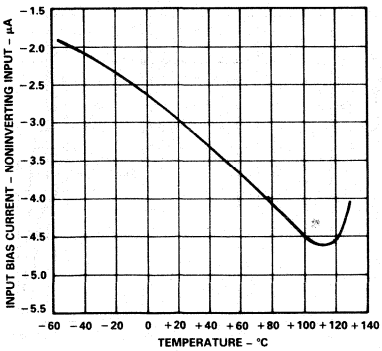


Figure 10. Positive Input Bias Current vs. Temperature

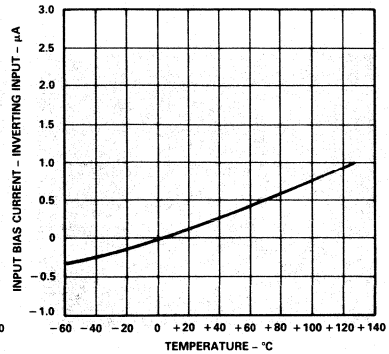


Figure 11. Negative Input Bias Current vs. Temperature

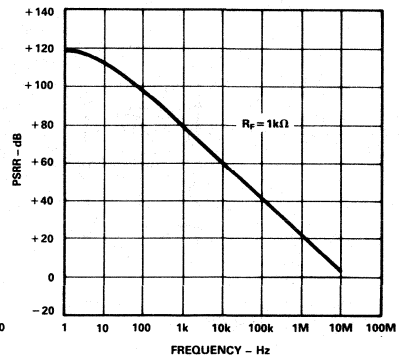


Figure 12. Power Supply Rejection vs. Frequency

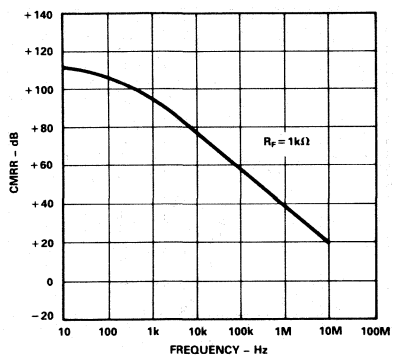


Figure 13. Common-Mode Rejection vs. Frequency

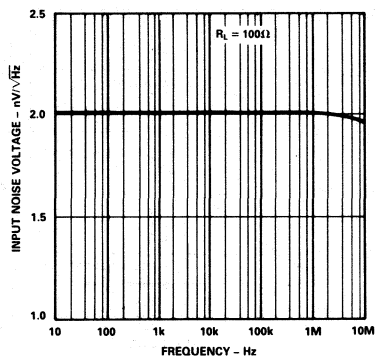


Figure 14. Input Noise Voltage Spectral Density

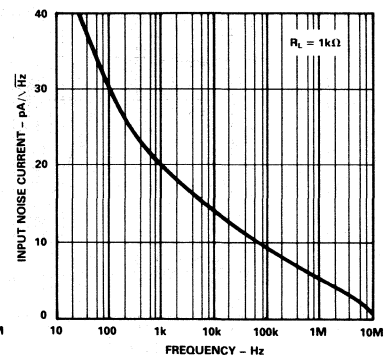


Figure 15. Inverting Input Noise Current Spectral Density

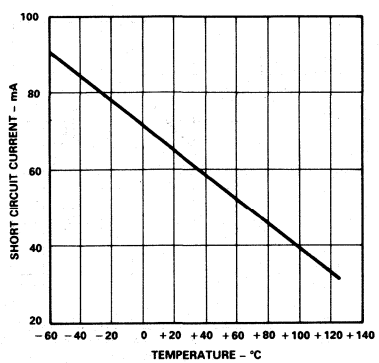


Figure 16. Short Circuit Current Limit vs. Temperature

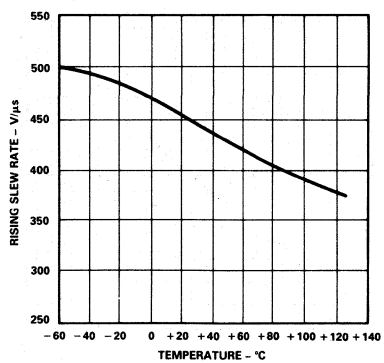


Figure 17. Slew Rate vs. Temperature

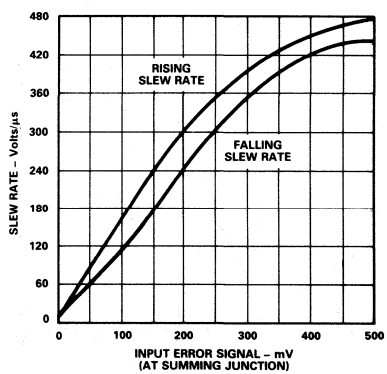


Figure 18. Slew Rate vs. Input Error Signal

AD846—Typical Characteristics, Inverting Gain of 1

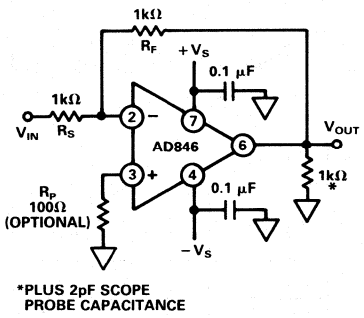


Figure 19a. Inverting Amplifier, Gain of 1

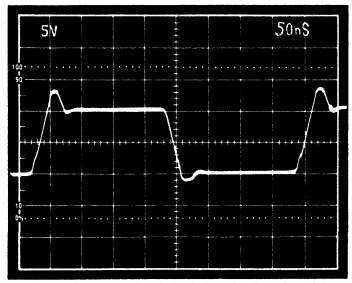


Figure 19b. Large Signal Pulse Response, Gain of −1

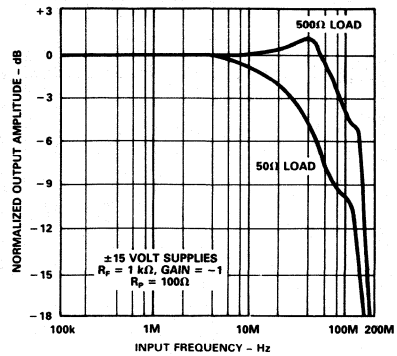


Figure 20. Normalized Output Amplitude vs. Frequency vs. Load

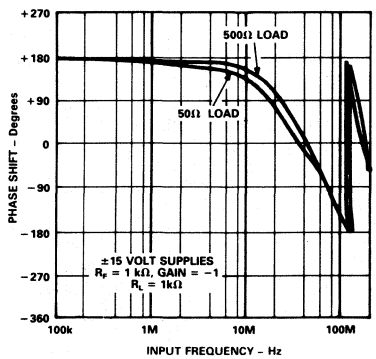


Figure 21. Phase Shift vs. Frequency

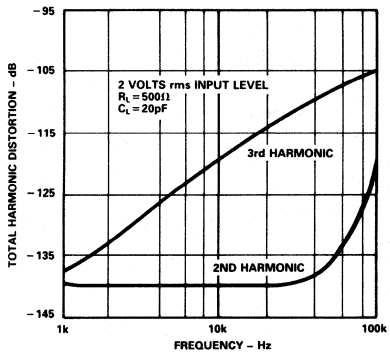


Figure 22. Total Harmonic Distortion vs. Frequency

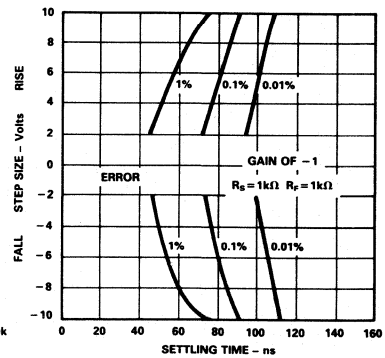


Figure 23. Settling Time vs. Step Size

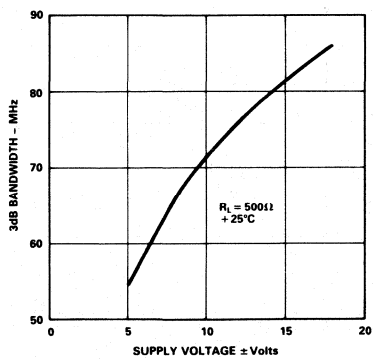


Figure 24. 3 dB Bandwidth vs. Supply Voltage

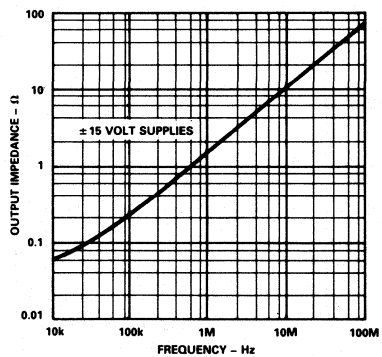


Figure 25. Output Impedance vs. Frequency

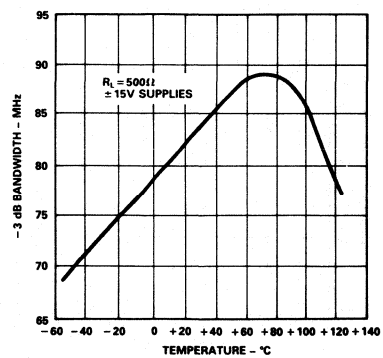


Figure 26. 3 dB Bandwidth vs. Temperature

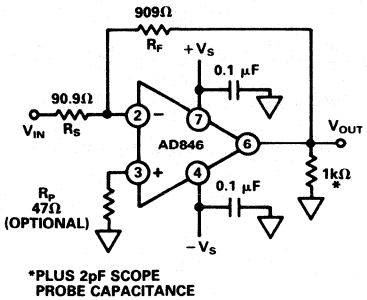


Figure 27a. Inverting Amplifier, Gain of 10

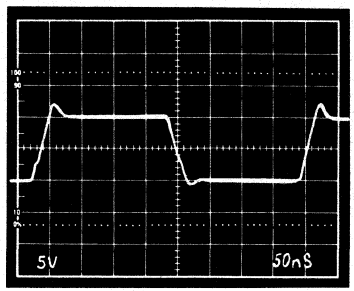


Figure 27b. Large Signal Pulse Response, Gain of 10

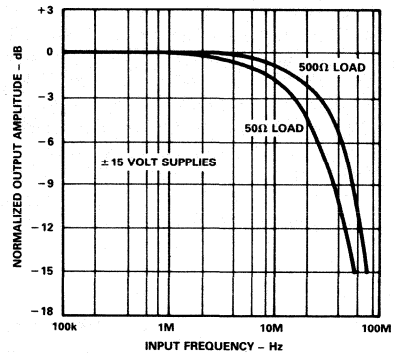


Figure 28. Normalized Output Amplitude vs. Frequency vs. Load

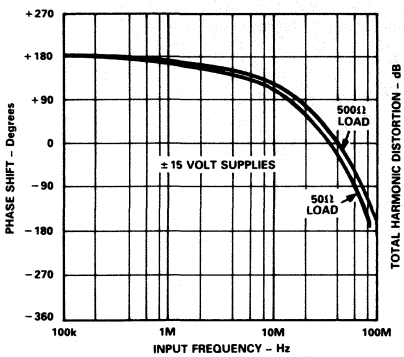


Figure 29. Phase vs. Frequency vs. Load

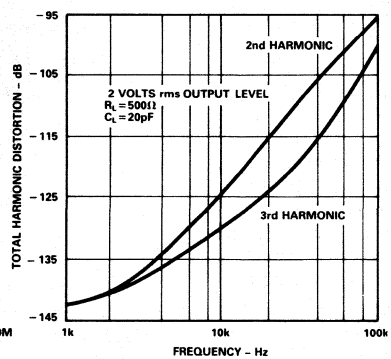


Figure 30. Harmonic Distortion vs. Frequency

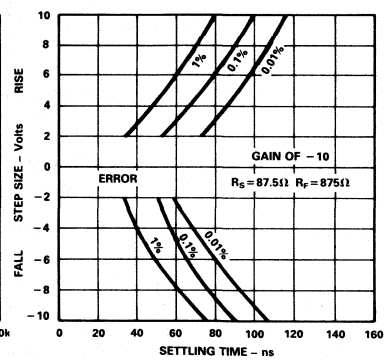


Figure 31. Settling Time vs. Step Size

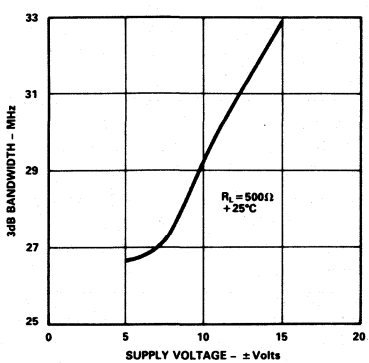


Figure 32. 3 dB Bandwidth vs. Supply Voltage

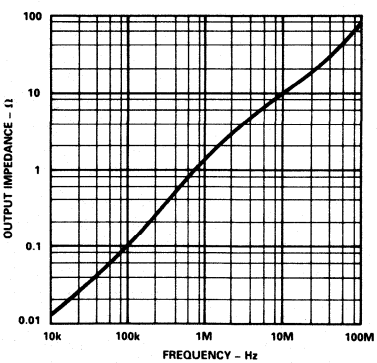


Figure 33. Output Impedance vs. Frequency

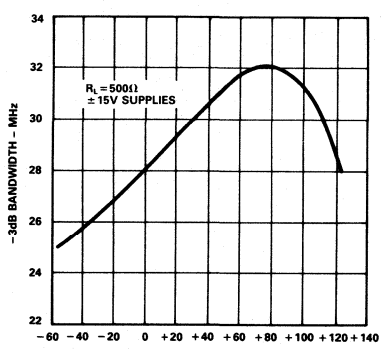


Figure 34. 3 dB Bandwidth vs. Temperature

POWER SUPPLY CONSIDERATIONS

The power supply connections to the AD846 must maintain a low impedance to ground over a bandwidth of 40 MHz or more. This is especially important when driving a significant resistive or capacitive load, since all current delivered to the load comes from the power supplies. Multiple high quality bypass capacitors are recommended for each power supply line in any critical application. A 0.1 μF ceramic and a 2.2 μF electrolytic capacitor as shown in Figure 35 placed as close as possible to the amplifier (with short lead lengths to power supply common) will assure adequate high frequency bypassing, in most applications. A minimum bypass capacitance of 0.1 μF should be used for any application.

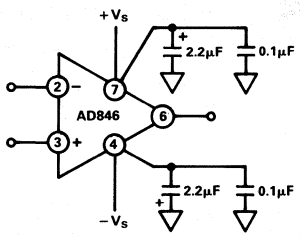


Figure 35. Recommended Power Supply Bypassing

THEORY OF OPERATION

The AD846 differs from conventional operational amplifiers in that it is a transimpedance device rather than a conventional voltage amplifier. Figure 36 is a simplified schematic of the AD846. The input stage consists of a pair of transistors, Q1 and Q2, which are biased by two diode-connected transistors, Q3 and Q4. Transistors Q1 and Q2 have their emitters connected together, and this common point functions as the inverting input of the amplifier. Correspondingly, the common connection of the two biasing diodes acts as the noninverting input.

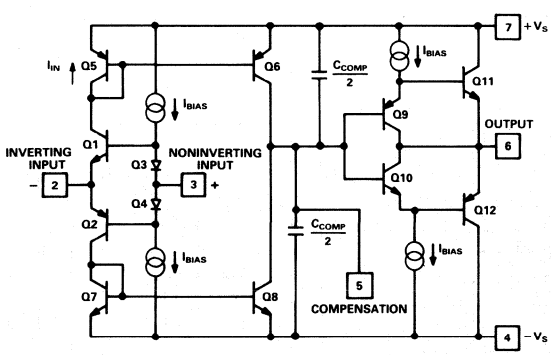


Figure 36. AD846 Simplified Schematic

When operated as a closed-loop amplifier, feedback error current, I_{IN}, flows into the inverting input terminal and is conveyed via current mirrors (transistors Q5, Q6, Q7, and Q8) to the compensation capacitor, C_{COMP}. The voltage developed across C_{COMP} is buffered by the output stage, consisting of transistors Q9–Q12.

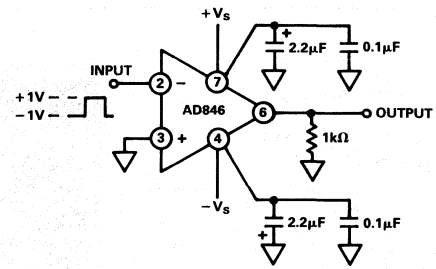


Figure 37. Overload Recovery Test Circuit

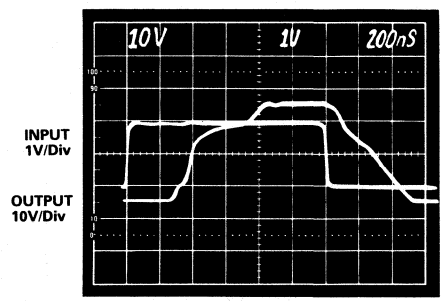


Figure 38. Overload Recovery Time Photo

Because the input error signal developed is in the form of a current, not a voltage, the AD846 differs from conventional operational amplifiers. This also means that, unlike most operational amplifiers which rely on negative feedback to produce a "virtual ground" at the inverting input terminal, this terminal explicitly has a low impedance.

A unique circuit approach allows the AD846 to realize an open-loop transimpedance of close to 200 MΩ. This is nearly three orders of magnitude greater than that of any other operational transimpedance amplifier and results in extremely high levels of dc precision.

As an example, the output voltage gain error is approximately equal to the value of the feedback resistor divided by the value of the open-loop transimpedance of the amplifier. That is, when using a 1 kΩ feedback resistor, this error is one part in 200,000. For a transimpedance amplifier with 1 MΩ transimpedance, this error is only one part in 1000; such an amplifier would barely be able to achieve 10-bit precision.

Figure 39 is a simplified three-terminal model for the AD846. Figure 40 is a simplified three-terminal model for a conventional voltage op amp. The action of current feedback serves to modify the behavior of the amplifier under closed-loop conditions. The feedback resistor, R_F, is somewhat analogous to the input stage transconductance of a conventional voltage amplifier; and therefore, if the value of R_F is held constant, the closed-loop bandwidth also remains virtually constant, independent of closed-loop voltage gain.

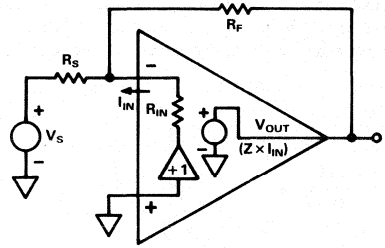


Figure 39. AD846 Three-Terminal Model

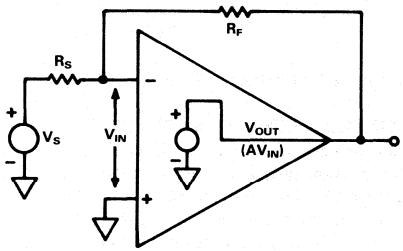


Figure 40. Op Amp Three-Terminal Model

A more detailed examination of the closed-loop transfer function of the AD846 results in the following equation:

$$\text{Closed-Loop Gain } G(s) = \frac{\frac{-R_F}{R_S}}{\left(1 + C_{COMP}\left[R_F + \left(1 + \frac{R_F}{R_S}\right)R_{IN}\right]s\right)}$$

Compare this to the equation for a conventional op amp:

$$\text{Closed-Loop Gain } G(s) = \frac{\frac{-R_F}{R_S}}{\left(1 + \frac{C_{COMP}}{g_M}\left(1 + \frac{R_F}{R_S}\right)s\right)}$$

where: C_{COMP} is the internal compensation capacitor of the amplifier; g_M is the input stage transconductance of the amplifier.

In the case of the voltage amplifier, the closed-loop bandwidth decreases directly with increasing values of $(1 + R_F/R_S)$, the closed-loop gain. However, for the transimpedance amplifier, the situation is different. At low gains, where $(1 + R_F/R_S)\ R_{IN}$ is small compared to R_F, the closed-loop bandwidth is controlled by the internal compensation capacitance of 7 pF and the value of R_F, and not by the closed-loop gain. At higher gains, where $(1 + R_F/R_S)\ R_{IN}$ is much larger than R_F, the behavior is that of a conventional operational amplifier in which the input stage transconductance is equal to the inverting terminal input impedance of the transimpedance amplifier (R_{IN} = 50 Ω).

A simple equation can, therefore, be used to determine the bandwidth of an amplifier employing the AD846 in the inverting configuration.

$$3\ dB\ Bandwidth = \frac{23}{R_F + 0.05\ (1 + G)}$$

where: The 3 dB bandwidth is in MHz
G is the closed-loop inverting gain of the AD846
R_F is the feedback resistance in kΩ.

NOTE: This equation applies only for values of R_F between 10 kΩ and 100 kΩ, and for R_{LOAD} greater than 500 Ω. For R_F = 1 kΩ the bandwidth should be estimated from Figure 41.

Figure 41 illustrates the closed-loop voltage gain vs. frequency of the AD846 for various values of feedback resistor. For comparison purposes, the characteristic of a conventional amplifier having an 80 MHz unity gain bandwidth is also shown.

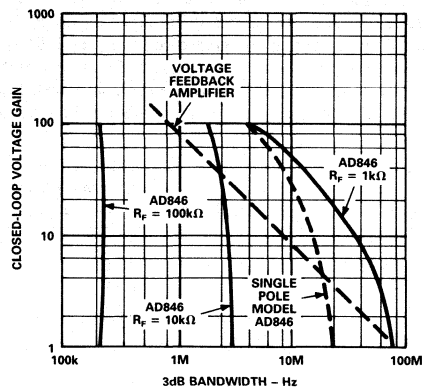


Figure 41. Closed-Loop Voltage Gain vs. Bandwidth for Various Values of R_F

For the case where R_F = 1 kΩ and R_S = 100 Ω (closed-loop gain of −10), the closed-loop bandwidth is approximately 28 MHz. It should also be noted that the use of a capacitor to shunt R_F, a normal practice for stabilizing conventional op amps, will cause this amplifier to become unstable because the closed-loop bandwidth will increase beyond the stable operating frequency.

A similar approach can be taken to calculate the noise performance of the amplifier. A simplified noise model is shown in Figure 42.

The equivalent mean-square output noise voltage spectral density will equal:

$$V_{ON}^2 = (R_F\ I_{NN})^2 + \left(1 + \frac{R_F}{R_S}\right)^2 [V_N^2 + (R_P\ I_{NP})^2 + 4\ kT\ R_P] + 4\ kT\ R_F\left(\frac{R_F}{R_S} + 1\right)$$

Where:

R_P is the external resistance placed in series with the noninverting input
R_F is the feedback resistor
R_S is the source resistor
I_{NN} is the noise current in the inverting input
I_{NP} is the noise current in the noninverting input
V_N is the input noise voltage.

Typical values for these parameters (@ 1 kHz) in pA/$\sqrt{Hz}$ are: I_{NN} = 20, I_{PN} = 6, V_N = 2.

Or, referring to the signal input, the equivalent mean-square input voltage noise is:

$$V_{IN}^2 = (R_F I_{NN})^2 + \left(1 + \frac{R_S}{R_F}\right)^2 [V_N^2 + (R_P I_{NP})^2 + 4kT R_P] + 4kT R_S \left(1 + \frac{R_S}{R_F}\right)$$

Resistor R_P is required for both inverting and noninverting (follower) operation, to insure stable operation. The amplifier's noninverting input current (flowing through R_P of 100 Ω) will typically add less than 300 μV to the AD846's input offset voltage. This can be trimmed-out using the optional network shown in Figure 44. The following table gives recommended values for R_P.

Supply Voltage	Gain (R_F/R_S)	Recommended Value for R_P
6 V to 15 V	1–10	100 Ω
6 V to 15 V	10–20	47 Ω
6 V to 15 V	20–200	0 Ω
5 V	1–10	47 Ω
5 V	10–200	0 Ω

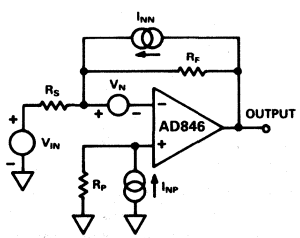


Figure 42. Op Amp Simplified Noise Model

NONINVERTING GAIN OPERATION

The AD846 can be used as a noninverting amplifier or voltage follower, operating at gains between 1 and 200. A minimum value of R_F equal to 1 kΩ should be employed. For low gains (1 to 2), the input signal should be applied to the AD846's noninverting input through a 100 Ω series resistor; this will help reduce peaking. The best transient response will occur when the amplifier's output level is below 5 V peak to peak.

At closed-loop gains of 3 or more, the input resistor is not required unless peak signals greater than 3 V will be applied. The amplifier's bandwidth can be determined by using the inverting amplifier's bandwidth equation or from Figure 41. For example, at a gain of +10 (R_F = 1 kΩ, R_S = 100 Ω) the bandwidth of the AD846 will be approximately 33 MHz; at a gain of +100, (R_F = 1 kΩ, R_S = 10 Ω) it will be 4 MHz. At gains of 3 or greater, a small capacitor (2 pF–5 pF) connected across the feedback resistor will help reduce overshoot; but when operating at noninverting gains below 3, this same capacitance will cause instability.

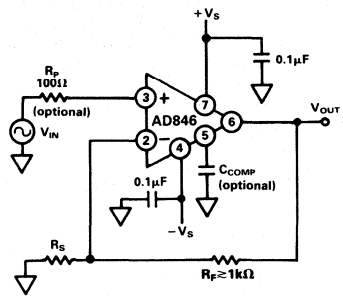


Figure 43. AD846 Noninverting Amplifier Configuration

USING THE COMPENSATION PIN OF THE AD846

Additional compensation may be provided for the AD846 by applying an external capacitance between Pin 5 and analog ground (Figure 44). The nominal value of the AD846's internal compensation capacitor is 7 pF. For a given value of feedback resistance (R_F), any added external capacitance reduces the amplifier's slew rate and bandwidth proportionally.

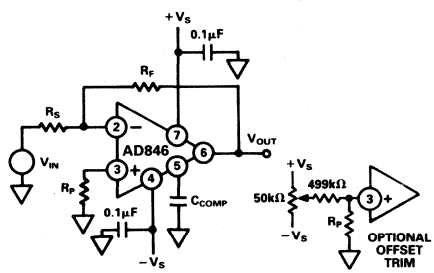


Figure 44. AD846 Inverting Amplifier Showing External Compensation Connection, R_P and Optional V_{OS} Trim

In addition to providing for external compensation, Pin 5 may be used to clamp the output of the amplifier, as shown in Figure 45. The output can be clamped anywhere within the output range (approximately ±10 V) of the amplifier. The input should also be clamped as a precaution against damaging the amplifier's input transistors.

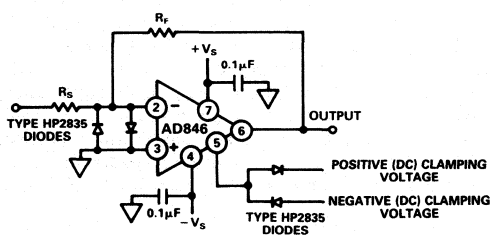


Figure 45. AD846 Used as a Clamped Amplifier

This compensation node may also be used as an additional output terminal as in the precision transconductance amplifier application of Figure 46.

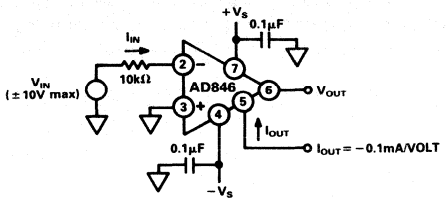


Figure 46. A Precision Transconductance Amplifier

The AD846 can be used in either the inverting transconductance mode as shown in Figure 46, or in a noninverting mode with R_S grounded and V_{IN} applied to the noninverting terminal. The current output is essentially constant over a compliance range of ±10 V at the compensation node. The output current (from Pin 5) is limited to about ±1 mA due to internal saturation. Under these circumstances the normal output pin provides a buffered version of the compensation node output voltage. Output load impedance of 500 Ω or greater will not affect the accuracy of the transconductance conversion.

THE AD846 IN A 2 MHz, 12-BIT SUBRANGING A/D CONVERTER CIRCUIT

The combination of fast settling times at high gains and low dc errors make the AD846 ideal for use as an error amplifier in high speed, 12-bit subranging A-D applications. In the circuit of Figure 47, an AD842 serves as an input amplifier. First pass conversion is accomplished, in a straightforward manner, determining the top 7 bits. The latch then holds these top 7 bits which are applied to a 7 bit, 12-bit accurate DAC and also to the highest 7 bits of the adder (note that a sample-and-hold should be used ahead of this converter to minimize errors due to its 500 ns acquisition time). In the second pass, the input switches S1 and S2 and S3 are set to state 2. The DAC output is then subtracted from the input signal and the resulting difference is then amplified by an AD846 gain of 32 follower. This gain, together with a 1/64th scale offset, insures a unipolar residue which can be converted by the flash A-D. Conversion is accomplished via switches S1, S2 and S3 in state 1. Switch S1 connects the input signal of the AD846 residue amplifier to ground which minimized overload recovery time.

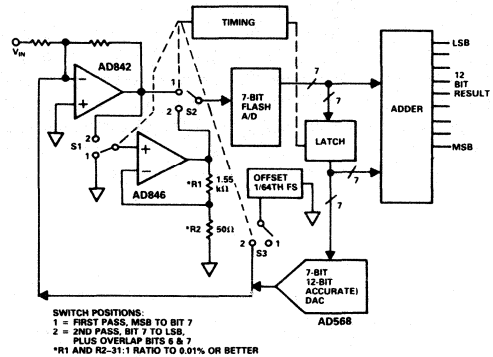


Figure 47. Block Diagram of a 2 MHz, 12-Bit Subranging A/D Converter

THE AD846 AS AN OPEN-LOOP LEVEL SHIFTER

The AD846 can also be used for open-loop level shifting. As shown in Figure 48, resistor R_S is used to develop an input current which is proportional to the input voltage, V_{IN}. This current flows from the compensation node (Pin 5) developing a voltage across resistor R_C (R_C is equal in value to resistor R_S) which, rather than being grounded, has one end tied to reference voltage V2. The voltage appearing at Pin 5 is, therefore, voltage V_{IN} plus voltage V2 and will directly follow changes in V_{IN}. By scaling resistor R_C, a level shift with voltage gain can be produced.

In addition, the normal voltage output at Pin 6 is approximately equal to the voltage at Pin 5 thus providing a low impedance, buffered output for the level shifter.

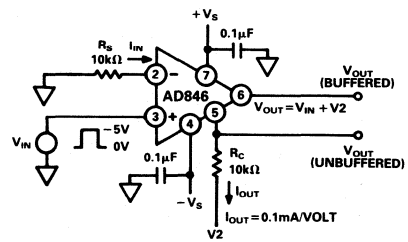


Figure 48. AD846 Connected as a Level Shift Amplifier

THE AD846 AS A HIGH SPEED DAC BUFFER

The AD846 will enable the AD568 12-bit DAC to develop a 10 V output step which settles to within 0.025 percent of its final value in about 100 ns. This AD846/AD568 combination is shown in the circuit of Figure 49. Correct power supply decoupling is essential: a 2.2 μF tantalum capacitor connected in parallel with a 0.1 μF to 0.01 μF ceramic disc capacitor is usually sufficient. These should be placed as close to the power supply pins as possible. Also, a ground plane should be employed; this ensure that there is a low impedance signal path to ground which allows the fastest possible output settling. In 12-bit systems with the AD846 operating at gains of 10 or less, inadequate supply decoupling can cause the output settling to degrade from 100 ns to as much as 300 ns, with a 10 V output step applied.

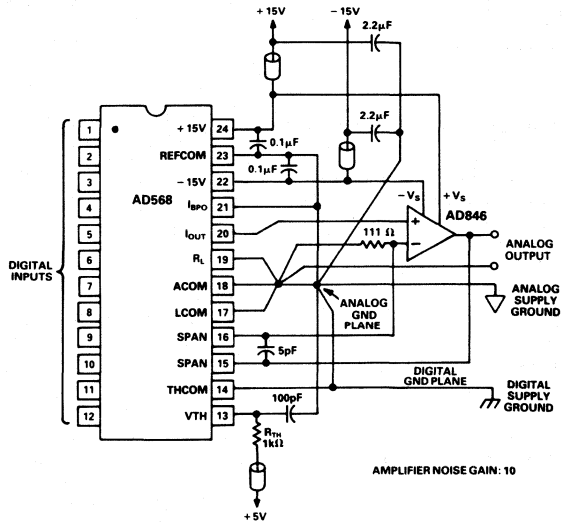


Figure 49. The AD846 Serving as a DAC Buffer

ANALOG DEVICES

High Speed, Low Power Monolithic Op Amp

AD847

FEATURES

Superior Performance
- High Unity Gain BW: 50 MHz
- Low Supply Current: 5.3 mA
- High Slew Rate: 300 V/μs
- Excellent Video Specifications
  - 0.04% Differential Gain (NTSC and PAL)
  - 0.19° Differential Phase (NTSC and PAL)
- Drives Any Capacitive Load
- Fast Settling Time to 0.1% (10 V Step): 65 ns

Excellent DC Performance
- High Open-Loop Gain 5.5 V/mV (R_{LOAD} = 1 kΩ)
- Low Input Offset Voltage: 0.5 mV

Specified for ±5 V and ±15 V Operation

Available in a Wide Variety of Options
- Plastic DIP and SOIC Packages
- Cerdip Package
- Die Form
- MIL-STD-883B Processing
- Tape & Reel (EIA-481A Standard)

Dual Version Available: AD827 (8 Lead)

Enhanced Replacement for LM6361

Replacement for HA2544, HA2520/2/5 and EL2020

APPLICATIONS

Video Instrumentation

Imaging Equipment

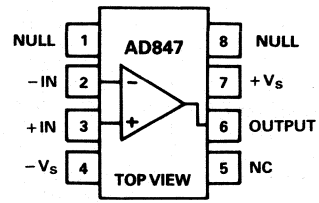
Copiers, Fax, Scanners, Cameras

High Speed Cable Driver

High Speed DAC and Flash ADC Buffers

CONNECTION DIAGRAM

Plastic DIP (N), Small Outline (R) and Cerdip (Q) Packages



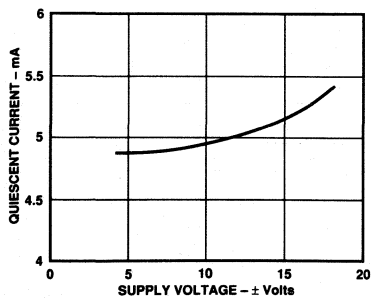
NC = NO CONNECT

PRODUCT DESCRIPTION

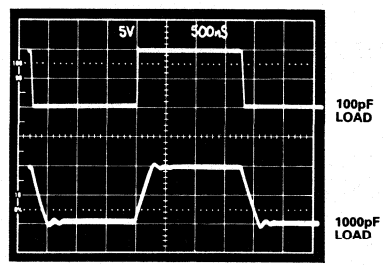
The AD847 represents a breakthrough in high speed amplifiers offering superior ac & dc performance and low power, all at low cost. The excellent dc performance is demonstrated by its ±5 V specifications which include an open-loop gain of 3500 V/V (500 Ω load) and low input offset voltage of 0.5 mV. Common-mode rejection is a minimum of 78 dB. Output voltage swing is ±3 V into loads as low as 150 Ω. Analog Devices also offers over 30 other high speed amplifiers from the low noise AD829 (1.7 nV/$\sqrt{\text{Hz}}$) to the ultimate video amplifier, the AD811, which features 0.01% differential gain and 0.01° differential phase.

APPLICATION HIGHLIGHTS

1. As a buffer the AD847 offers a full-power bandwidth of 12.7 MHz (5 V p–p with ±5 V supplies) making it outstanding as an input buffer for flash A/D converters.
2. The low power and small outline package of the AD847 make it very well suited for high density applications such as multiple pole active filters.
3. The AD847 is internally compensated for unity gain operation and remains stable when driving any capacitive load.



Quiescent Current vs. Supply Voltage



AD847 Driving Capacitive Loads

AD847—SPECIFICATIONS (@ T_A = +25°C, unless otherwise noted)

Model	Conditions	V_S	AD847J Min	AD847J Typ	AD847J Max	AD847AR Min	AD847AR Typ	AD847AR Max	Units
INPUT OFFSET VOLTAGE[1]		±5 V		0.5	**1**		0.5	**1**	mV
	T_{MIN} to T_{MAX}				3.5			4	mV
Offset Drift				15			15		µV/°C
INPUT BIAS CURRENT		±5 V, ±15 V		3.3	**6.6**		3.3	**6.6**	µA
	T_{MIN} to T_{MAX}				7.2			10	µA
INPUT OFFSET CURRENT		±5 V, ±15 V		50	**300**		50	**300**	nA
	T_{MIN} to T_{MAX}				400			500	nA
Offset Current Drift				0.3			0.3		nA/°C
OPEN-LOOP GAIN	V_{OUT} = ±2.5 V	±5 V							
	R_{LOAD} = 500 Ω		**2**	3.5		**2**	3.5		V/mV
	T_{MIN} to T_{MAX}		1			1			V/mV
	R_{LOAD} = 150 Ω			1.6			1.6		V/mV
	V_{OUT} = ±10 V	±15 V							
	R_{LOAD} = 1 kΩ		**3**	5.5		**3**	5.5		V/mV
	T_{MIN} to T_{MAX}		1.5			1.5			V/mV
DYNAMIC PERFORMANCE									
Unity Gain Bandwidth		±5 V		35			35		MHz
		±15 V		50			50		MHz
Full Power Bandwidth[2]	V_{OUT} = 5 V p-p								
	R_{LOAD} = 500 Ω,	±5 V		12.7			12.7		MHz
	V_{OUT} = 20 V p-p,								
	R_{LOAD} = 1 kΩ	±15 V		4.7			4.7		MHz
Slew Rate[3]	R_{LOAD} = 1 kΩ	±5 V		200			200		V/µs
		±15 V	225	300		225	300		V/µs
Settling Time									
to 0.1%, R_{LOAD} = 250 Ω	−2.5 V to +2.5 V	±5 V		65			65		ns
	10 V Step, A_V = −1	±15 V		65			65		ns
to 0.01%, R_{LOAD} = 250 Ω	−2.5 V to +2.5 V	±5 V		140			140		ns
	10 V Step, A_V = −1	±15 V		120			120		ns
Phase Margin	C_{LOAD} = 10 pF	±15 V							
	R_{LOAD} = 1 kΩ			50			50		Degree
Differential Gain	f ≈ 4.4 MHz, R_{LOAD} = 1 kΩ	±15 V		0.04			0.04		%
Differential Phase	f ≈ 4.4 MHz, R_{LOAD} = 1 kΩ	±15 V		0.19			0.19		Degree
COMMON-MODE REJECTION	V_{CM} = ±2.5 V	±5 V	**78**	95		**78**	95		dB
	V_{CM} = ±12 V	±15 V	**78**	95		**78**	95		dB
	T_{MIN} to T_{MAX}		75			75			dB
POWER SUPPLY REJECTION	V_S = ±5 V to ±15 V		**75**	86		**75**	86		dB
	T_{MIN} to T_{MAX}		72			72			dB
INPUT VOLTAGE NOISE	f = 10 kHz	±15 V		15			15		nV/√Hz
INPUT CURRENT NOISE	f = 10 kHz	±15 V		1.5			1.5		pA/√Hz
INPUT COMMON-MODE VOLTAGE RANGE		±5 V		+4.3			+4.3		V
				−3.4			−3.4		V
		±15 V		+14.3			+14.3		V
				−13.4			−13.4		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 500 Ω	±5 V	**3.0**	3.6		**3.0**	3.6		±V
	R_{LOAD} = 150 Ω	±5 V	**2.5**	3		**2.5**	3		±V
	R_{LOAD} = 1 kΩ	±15 V	**12**			**12**			±V
	R_{LOAD} = 500 Ω	±15 V	**10**			**10**			±V
Short-Circuit Current		±15 V		32			32		mA
INPUT RESISTANCE				300			300		kΩ
INPUT CAPACITANCE				1.5			1.5		pF
OUTPUT RESISTANCE	Open Loop			15			15		Ω
POWER SUPPLY									
Operating Range			**± 4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current		±5 V		4.8	**6.0**		4.8	**6.0**	mA
	T_{MIN} to T_{MAX}				7.3			7.3	mA
		±15 V		5.3	**6.3**		5.3	**6.3**	mA
	T_{MIN} to T_{MAX}				7.6			7.6	mA

NOTES
[1]Input Offset Voltage Specifications are guaranteed after 5 minutes at T_A = +25°C.
[2]Full Power Bandwidth = Slew Rate/2π V_{PEAK}.
[3]Slew Rate is measured on rising edge.

All min and max specifications are guaranteed. Specifications in **boldface** are 100% tested at final electrical test.
Specifications subject to change without notice.

Model	Conditions	V_S	AD847AQ Min	AD847AQ Typ	AD847AQ Max	AD847S Min	AD847S Typ	AD847S Max	Units
INPUT OFFSET VOLTAGE[1]		±5 V		0.5	1		0.5	1	mV
	T_{MIN} to T_{MAX}				4			4	mV
Offset Drift				15			15		µV/°C
INPUT BIAS CURRENT		±5 V, ±15 V		3.3	5		3.3	5	µA
	T_{MIN} to T_{MAX}				7.5			7.5	µA
INPUT OFFSET CURRENT		±5 V, ±15 V		50	300		50	300	nA
	T_{MIN} to T_{MAX}				400			400	nA
Offset Current Drift				0.3			0.3		nA/°C
OPEN LOOP GAIN	V_{OUT} = ±2.5 V	±5 V							
	R_{LOAD}= 500 Ω		2	3.5		2	3.5		V/mV
	T_{MIN} to T_{MAX}		1			1			V/mV
	R_{LOAD} = 150 Ω			1.6			1.6		V/mV
	V_{OUT} = ±10 V	±15 V							
	R_{LOAD} = 1 kΩ		3	5.5		3	5.5		V/mV
	T_{MIN} to T_{MAX}		1.5			1.5			V/mV
DYNAMIC PERFORMANCE									
Unity Gain Bandwidth		±5 V		35			35		MHz
		±15 V		50			50		MHz
Full Power Bandwidth[2]	V_{OUT} = 5 V p-p								
	R_{LOAD} = 500 Ω,	±5 V		12.7			12.7		MHz
	V_{OUT} = 20 V p-p,								
	R_{LOAD} = 1 kΩ	±15 V		4.7			4.7		MHz
Slew Rate[3]	R_{LOAD} = 1 kΩ	±5 V		200			200		V/µs
		±15 V	225	300		225	300		V/µs
Settling Time									
to 0.1%, R_{LOAD} = 250 Ω	−2.5 V to +2.5 V	±5 V		65			65		ns
	10 V Step, A_V = −1	±15 V		65			65		ns
to 0.01%, R_{LOAD} = 250 Ω	−2.5 V to +2.5 V	±5 V		140			140		ns
	10 V Step, A_V = −1	±15 V		120			120		ns
Phase Margin	C_{LOAD} = 10 pF	±15 V							
	R_{LOAD} = 1 kΩ			50			50		Degree
Differential Gain	f ≈ 4.4 MHz, R_{LOAD} = 1 kΩ	±15 V		0.04			0.04		%
Differential Phase	f ≈ 4.4 MHz, R_{LOAD} = 1 kΩ	±15 V		0.19			0.19		Degree
COMMON-MODE REJECTION	V_{CM} = ±2.5 V	±5 V	80	95		80	95		dB
	V_{CM} = ±12 V	±15 V	80	95		80	95		dB
	T_{MIN} to T_{MAX}		75			75			dB
POWER SUPPLY REJECTION	V_S = ±5 V to ±15 V		75	86		75	86		dB
	T_{MIN} to T_{MAX}		72			72			dB
INPUT VOLTAGE NOISE	f = 10 kHz	±15 V		15			15		nV/√Hz
INPUT CURRENT NOISE	f = 10 kHz	±15 V		1.5			1.5		pA/√Hz
INPUT COMMON-MODE VOLTAGE RANGE		±5 V		+4.3			+4.3		V
				−3.4			−3.4		V
		±15 V		+14.3			+14.3		V
				−13.4			−13.4		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 500 Ω	±5 V	3.0	3.6		3.0	3.6		±V
	R_{LOAD} = 150 Ω	±5 V	2.5	3		2.5	3		±V
	R_{LOAD} = 1 kΩ	±15 V	12			12			±V
	R_{LOAD} = 500 Ω	±15 V	10			10			±V
Short-Circuit Current		±15 V		32			32		mA
INPUT RESISTANCE				300			300		kΩ
INPUT CAPACITANCE				1.5			1.5		pF
OUTPUT RESISTANCE	Open Loop			15			15		Ω
POWER SUPPLY									
Operating Range			± 4.5		±18	±4.5		±18	V
Quiescent Current		±5 V		4.8	5.7		4.8	5.7	mA
	T_{MIN} to T_{MAX}				7.0			7.8	mA
		±15 V		5.3	6.3		5.3	6.3	mA
	T_{MIN} to T_{MAX}				7.6			8.4	mA

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
Plastic (N) . . . . . 1.2 Watts
Small Outline (R) . . . . . 0.8 Watts
Cerdip (Q) . . . . . 1.1 Watts
Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±6 V
Storage Temperature Range (Q) . . . . . −65°C to +150°C
(N, R) . . . . . −65°C to +125°C
Junction Temperature . . . . . 175°C
Lead Temperature Range (Soldering 60 sec) . . . . . 300°C

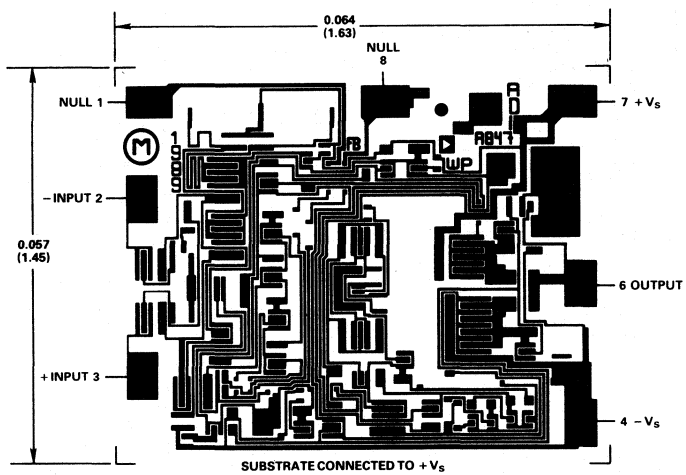
NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Mini-DIP Package: θ_{JA} = 100°C/Watt; θ_{JC} = 33°C/Watt
Cerdip Package: θ_{JA} = 110°C/Watt; θ_{JC} = 30°C/Watt
Small Outline Package: θ_{JA} = 155°C/Watt; θ_{JC} = 33°C/Watt

ESD SUSCEPTIBILITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although the AD847 features proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



ORDERING GUIDE

Model[1]	Temperature Range − °C	Package Description	Package Option[2]
AD847JN	0 to +70	Plastic	N-8
AD847JR	0 to +70	SOIC	R-8
AD847AQ	−40 to +85	Cerdip	Q-8
AD847AR	−40 to +85	SOIC	R-8
AD847SQ	−55 to +125	Cerdip	Q-8
AD847SQ/883B	−55 to +125	Cerdip	Q-8

NOTES
[1]AD847 also available in J and S grade chips, and AD847JR and AD847AR are available in tape and reel.
[2]For outline information see Package Information section.

Typical Characteristics (@ +25°C and V_S = ±15 V, unless otherwise noted)

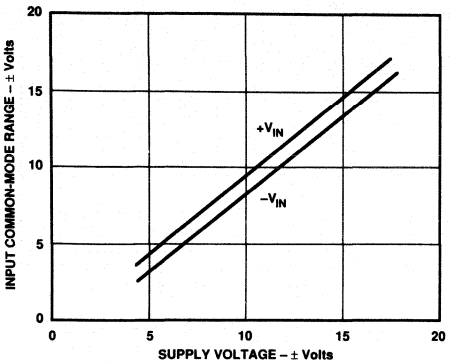


Figure 1. Input Common-Mode Range vs. Supply Voltage

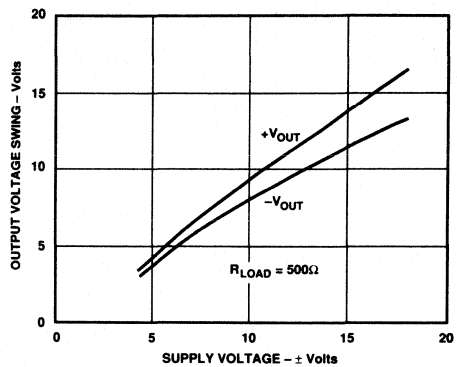


Figure 2. Output Voltage Swing vs. Supply Voltage

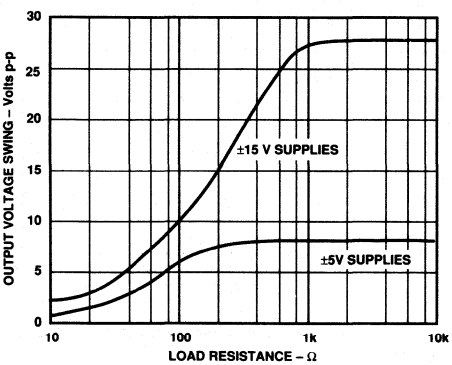


Figure 3. Output Voltage Swing vs. Load Resistance

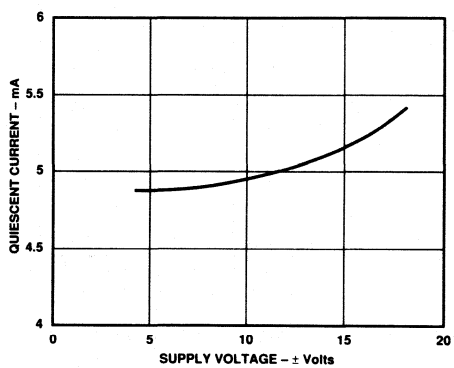


Figure 4. Quiescent Current vs. Supply Voltage

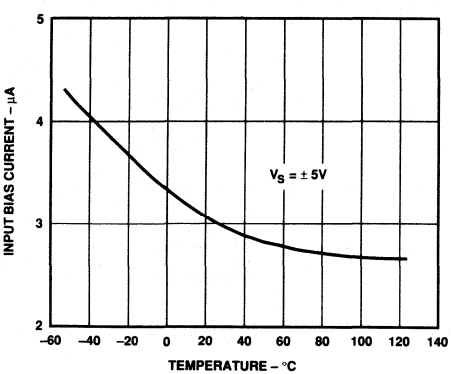


Figure 5. Input Bias Current vs. Temperature

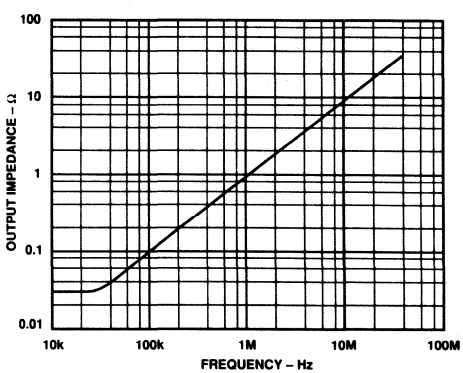


Figure 6. Output Impedance vs. Frequency

AD847—Typical Characteristics (@ +25°C and V_S = ±15 V, unless otherwise noted)

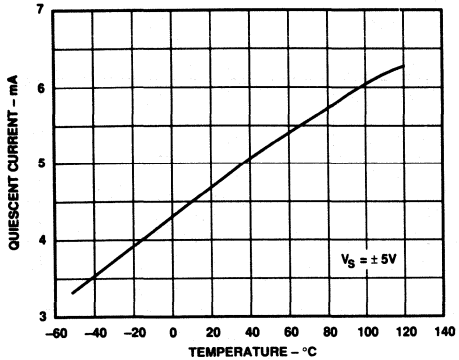


Figure 7. Quiescent Current vs. Temperature

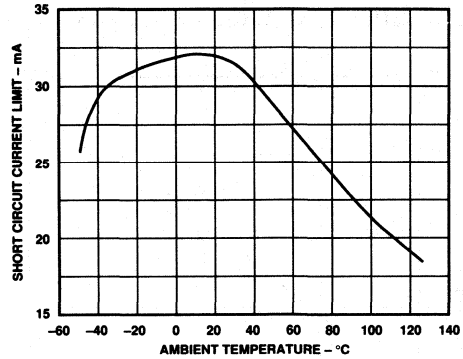


Figure 8. Short-Circuit Current Limit vs. Temperature

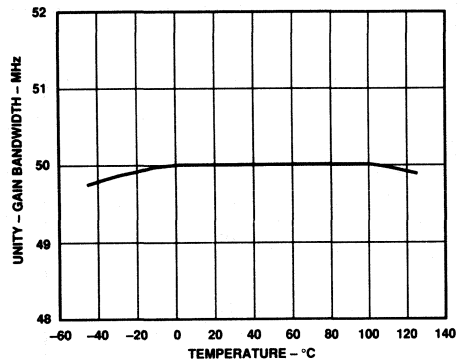


Figure 9. Gain Bandwidth Product vs. Temperature

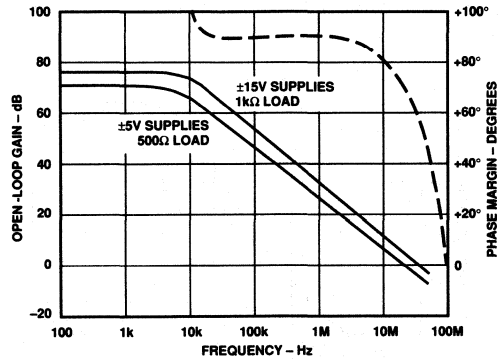


Figure 10. Open-Loop Gain and Phase Margin vs. Frequency

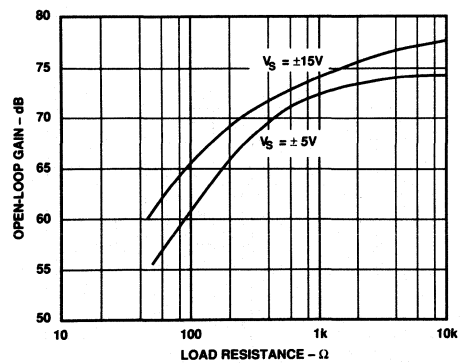


Figure 11. Open-Loop Gain vs. Load Resistance

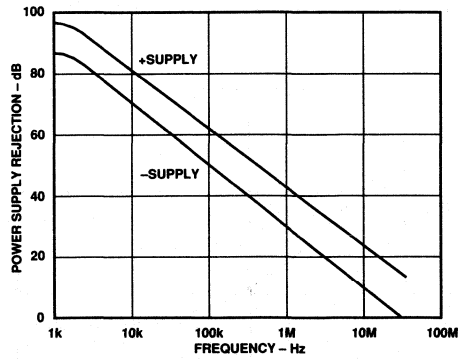


Figure 12. Power Supply Rejection vs. Frequency

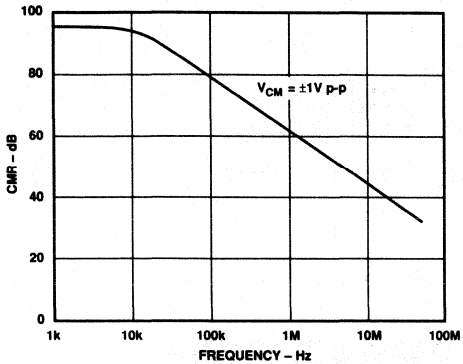


Figure 13. Common-Mode Rejection vs. Frequency

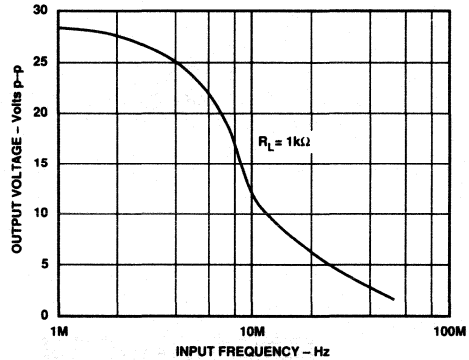


Figure 14. Large Signal Frequency Response

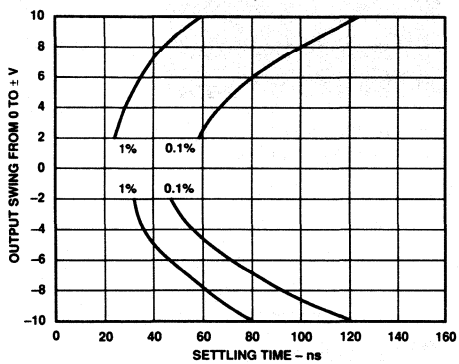


Figure 15. Output Swing and Error vs. Settling Time

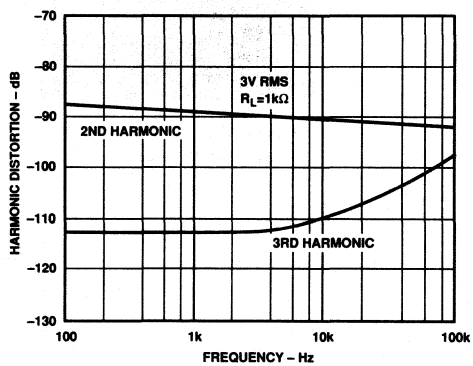


Figure 16. Harmonic Distortion vs. Frequency

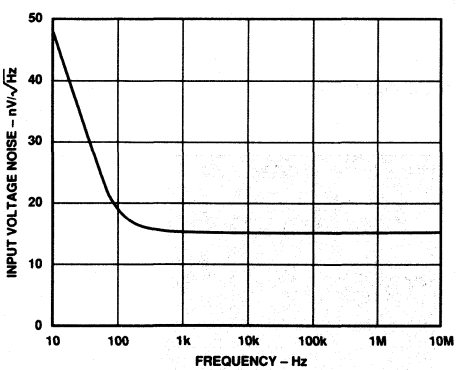


Figure 17. Input Voltage Noise Spectral Density

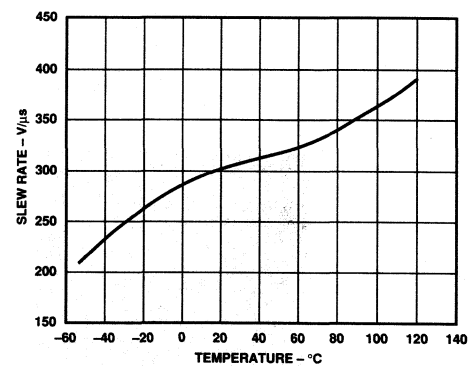


Figure 18. Slew Rate vs. Temperature

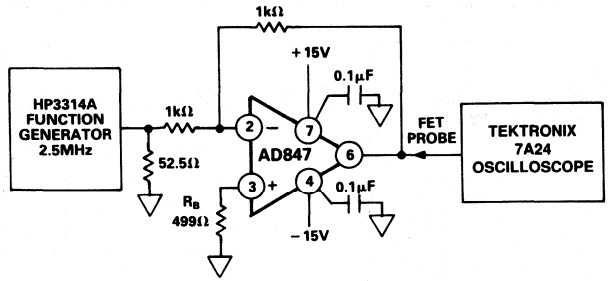


Figure 19. Inverting Amplifier Configuration

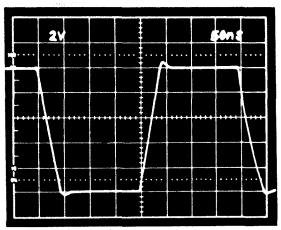


Figure 19a. Inverter Large Signal Pulse Response

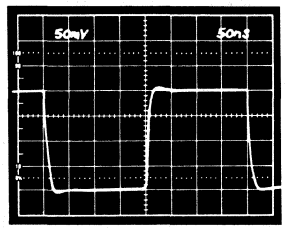


Figure 19b. Inverter Small Signal Pulse Response

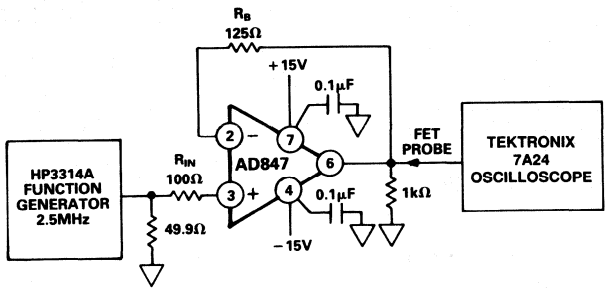


Figure 20. Noninverting Amplifier Configuration

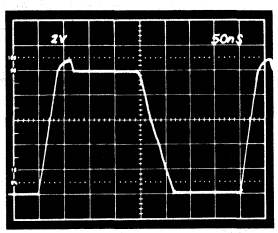


Figure 20a. Noninverting Large Signal Pulse Response

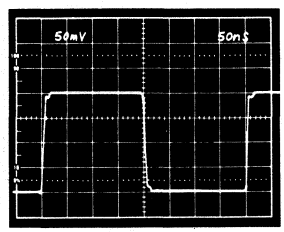


Figure 20b. Noninverting Small Signal Pulse Response

OFFSET NULLING

The input offset voltage of the AD847 is very low for a high speed op amp, but if additional nulling is required, the circuit shown in Figure 21 can be used.

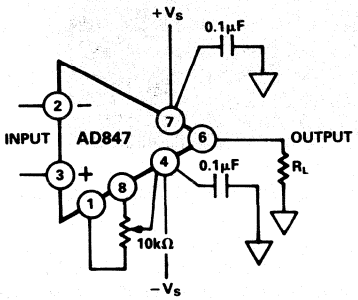


Figure 21. Offset Nulling

INPUT CONSIDERATIONS

An input resistor (R_{IN} in Figure 20) is required in circuits where the input to the AD847 will be subjected to transient or continuous overload voltages exceeding the ±6 V maximum differential limit. This resistor provides protection for the input transistors by limiting the maximum current that can be forced into their bases.

For high performance circuits it is recommended that a resistor (R_B in Figures 19 and 20) be used to reduce bias current errors by matching the impedance at each input. The offset voltage error will be reduced by more than an order of magnitude.

THEORY OF OPERATION

The AD847 is fabricated on Analog Devices' proprietary complementary bipolar (CB) process which enables the construction of pnp and npn transistors with similar f_Ts in the 600 MHz to 800 MHz region. The AD847 circuit (Figure 22) includes an npn input stage followed by fast pnps in the folded cascode intermediate gain stage. The CB pnps are also used in the current amplifying output stage. The internal compensation capacitance that makes the AD847 unity gain stable is provided by the junction capacitances of transistors in the gain stage.

The capacitor, C_F, in the output stage mitigates the effect of capacitive loads. At low frequencies and with low capacitive loads, the gain from the compensation node to the output is very close to unity. In this case C_F is bootstrapped and does not contribute to the compensation capacitance of the part. As the capacitive load is increased, a pole is formed with the output impedance of the output stage. This reduces the gain, and therefore, C_F is incompletely bootstrapped. Some fraction of C_F contributes to the compensation capacitance, and the unity gain bandwidth falls. As the load capacitance is increased, the bandwidth continues to fall, and the amplifier remains stable.

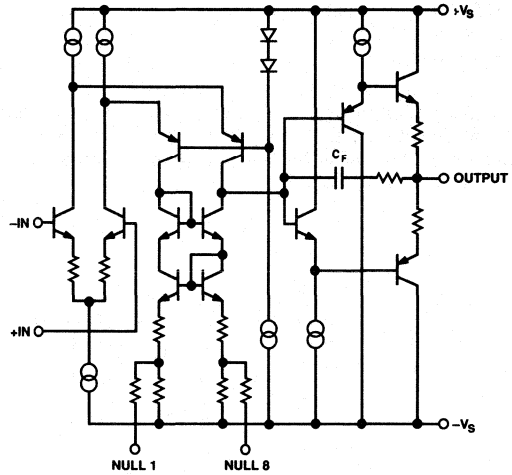


Figure 22. AD847 Simplified Schematic

GROUNDING AND BYPASSING

In designing practical circuits with the AD847, the user must remember that whenever high frequencies are involved, some special precautions are in order. Circuits must be built with short interconnect leads. A large ground plane should be used whenever possible to provide a low resistance, low inductance circuit path, as well as minimizing the effects of high frequency coupling. Sockets should be avoided because the increased interlead capacitance can degrade bandwidth.

Feedback resistors should be of low enough value to assure that the time constant formed with the capacitance at the amplifier summing junction will not limit the amplifier performance. Resistor values of less than 5 kΩ are recommended. If a larger resistor must be used, a small (<10 pF) feedback capacitor in parallel with the feedback resistor, R_F, may be used to compensate for the input capacitances and optimize the dynamic performance of the amplifier.

Power supply leads should be bypassed to ground as close as possible to the amplifier pins. Ceramic disc capacitors of 0.1 μF are recommended.

VIDEO LINE DRIVER

The AD847 functions very well as a low cost, high speed line driver for either terminated or unterminated cables. Figure 23 shows the AD847 driving a doubly terminated cable in a follower configuration.

The termination resistor, R_T, (when equal to the cable's characteristic impedance) minimizes reflections from the far end of the cable. While operating from ±5 V supplies, the AD847 maintains a typical slew rate of 200 V/μs, which means it can drive a ±1 V, 30 MHz signal into a terminated cable.

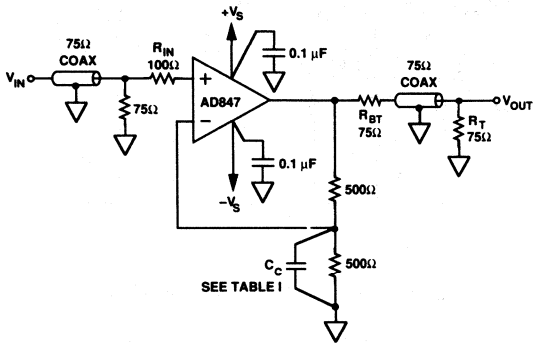


Figure 23. Video Line Driver

Table I. Video Line Driver Performance Chart

V_{IN}*	V_{SUPPLY}	C_C	−3 dB B_W	Overshoot
0 dB or ±500 mV Step	±15	20 pF	23 MHz	4%
0 dB or ±500 mV Step	±15	15 pF	21 MHz	0%
0 dB or ±500 mV Step	±15	0 pF	13 MHz	0%
0 dB or ±500 mV Step	±5	20 pF	18 MHz	2%
0 dB or ±500 mV Step	±5	15 pF	16 MHz	0%
0 dB or ±500 mV Step	±5	0 pF	11 MHz	0%

NOTE
*−3 dB bandwidth numbers are for the 0 dBm signal input. Overshoot numbers are the percent overshoot of the 1 volt step input.

A back-termination resistor (R_{BT}, also equal to the characteristic impedance of the cable) may be placed between the AD847 output and the cable input, in order to damp any reflected signals caused by a mismatch between R_T and the cable's characteristic impedance. This will result in a flatter frequency response, although this requires that the op amp supply ±2 V to the output in order to achieve a ±1 V swing at resistor R_T.

Figure 24 shows the AD847 driving 100 pF and 1000 pF loads.

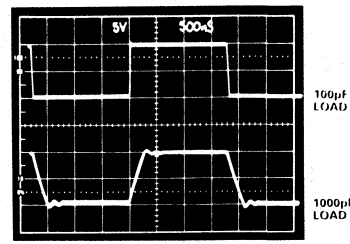


Figure 24. AD847 Driving Capacitive Loads

FLASH ADC INPUT BUFFER

The 35 MHz unity gain bandwidth of the AD847 makes it an excellent choice for buffering the input of high speed flash A/D converters, such as the AD9048.

Figure 25 shows the AD847 as a unity inverter for the input to the AD9048.

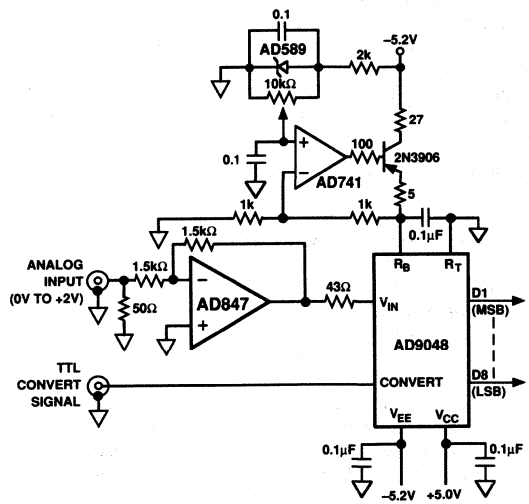
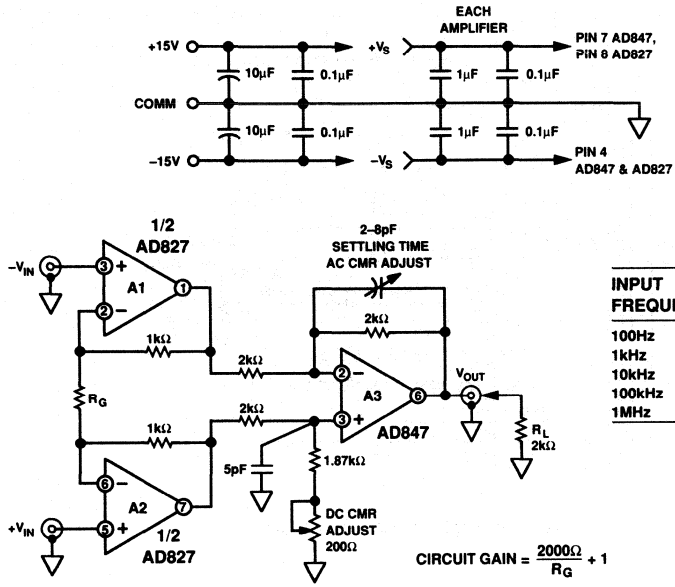


Figure 25. Flash ADC Input Buffer

A High Speed, Three Op-Amp In-Amp

The circuit of Figure 26 lends itself well to CCD imaging and other video speed applications. It uses two high speed CB process op-amps: Amplifier A3, the output amplifier, is an AD847. The input amplifier (A1 and A2) is an AD827, which is a dual version of the AD847. This circuit has the optional flexibility of both dc and ac trims for common-mode rejection, plus the ability to adjust for minimum settling time.



INPUT FREQUENCY	CMRR
100Hz	88.3dB
1kHz	87.4dB
10kHz	86.2dB
100kHz	67.4dB
1MHz	47.1dB

BANDWIDTH, SETTLING TIME AND TOTAL HARMONIC DISTORTION VS. GAIN

GAIN	R_G	C_{ADJ} (pF)	SMALL SIGNAL BANDWIDTH	SETTLING TIME TO 0.1%	THD + NOISE BELOW INPUT LEVEL @ 10kHz
1	OPEN	2–8	16.1MHz	200ns	82dB
2	2kΩ	2–8	14.7MHz	200ns	82dB
10	226Ω	2–8	4.5MHz	370ns	81dB
100	20Ω	2–8	660kHz	2.5µs	71dB

Figure 26. A High Speed In-Amp Circuit for Data Acquisition

HIGH SPEED DAC BUFFER

The wide bandwidth and fast settling time of the AD847 makes it a very good output buffer for high speed current-output D/A converters like the AD668. As shown in Figure 27, the op amp establishes a summing node at ground for the DAC output. The output voltage is determined by the amplifier's feedback resistor (10.24 V for a 1 kΩ resistor). Note that since the DAC generates a positive current to ground, the voltage at the amplifier output will be negative. A 100 Ω series resistor between the noninverting amplifier input and ground minimizes the offset effects of op amp input bias currents.

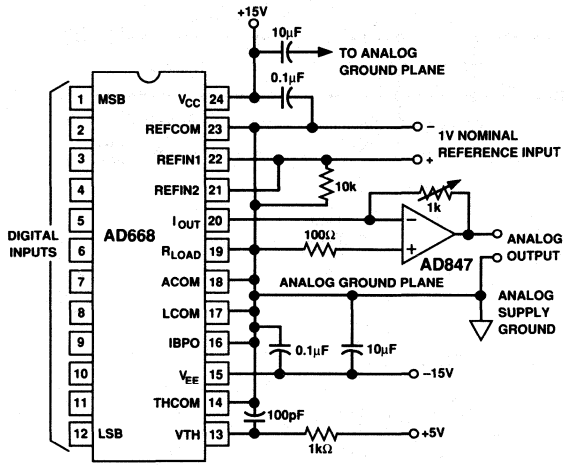


Figure 27. High Speed DAC Buffer

ANALOG DEVICES

High Speed, Low Power Monolithic Op Amps

AD848/AD849

FEATURES

725MHz Gain Bandwidth – AD849
175MHz Gain Bandwidth – AD848
4.8mA Supply Current
300V/μs Slew Rate
80ns Settling Time to 0.1% for a 10V Step – AD849
Differential Gain: AD848 = 0.07%, AD849 = 0.08%
Differential Phase: AD848 = 0.08°, AD849 = 0.04°
Drives Capacitive Loads

DC PERFORMANCE

3nV/√Hz Input Voltage Noise – AD849
85V/mV Open Loop Gain into a 1kΩ Load – AD849
1mV max Input Offset Voltage
Performance Specified for ±5V and ±15V Operation
Available in Plastic, Hermetic Cerdip and Small Outline Packages. Chips and MIL-STD-883B Parts Available.
Available in Tape and Reel in Accordance with EIA-481A Standard

APPLICATIONS

Cable Drivers
8- and 10-Bit Data Acquisition Systems
Video and R_F Amplification
Signal Generators

PRODUCT DESCRIPTION

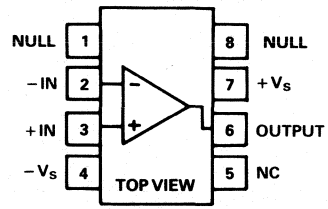
The AD848 and AD849 are high speed, low power monolithic operational amplifiers. The AD848 is internally compensated so that it is stable for closed loop gains of 5 or greater. The AD849 is fully decompensated and is stable at gains greater than 24. The AD848 and AD849 achieve their combination of fast ac and good dc performance by utilizing Analog Devices' junction isolated complementary bipolar (CB) process. This process enables these op amps to achieve their high speed while only requiring 4.8mA of current from the power supplies.

The AD848 and AD849 are members of Analog Devices' family of high speed op amps. This family includes, among others, the AD847 which is unity gain stable, with a gain bandwidth of 50MHz. For more demanding applications, the AD840, AD841 and AD842 offer even greater precision and greater output current drive.

The AD848 and AD849 have good dc performance. When operating with ±5V supplies, they offer open loop gains of 13V/mV (AD848 with a 500Ω load) and low input offset voltage of 1mV maximum. Common-mode rejection is a minimum of 92dB. Output voltage swing is ±3V even into loads as low as 150Ω.

CONNECTION DIAGRAM

Plastic (N), Small Outline (R) and Cerdip (Q) Packages



NC = NO CONNECT

APPLICATIONS HIGHLIGHTS

1. The high slew rate and fast settling time of the AD848 and AD849 make them ideal for video instrumentation circuitry, low noise pre-amps and line drivers.
2. In order to meet the needs of both video and data acquisition applications, the AD848 and AD849 are optimized and tested for ±5V and ±15V power supply operation.
3. Both amplifiers offer full power bandwidth greater than 20MHz (for 2V p-p with ±5V supplies).
4. The AD848 and AD849 remain stable when driving any capacitive load.
5. Laser wafer trimming reduces the input offset voltage to 1mV maximum on all grades, thus eliminating the need for external offset nulling in many applications.
6. The AD848 is an enhanced replacement for the LM6164 series and can function as a pin-for-pin replacement for many high speed amplifiers such as the HA2520/2/5 and EL2020 in applications where the gain is 5 or greater.

AD848/AD849—SPECIFICATIONS ($@T_A$ = +25°C, unless otherwise noted)

Model	Conditions	V_S	AD848J Min	AD848J Typ	AD848J Max	AD848A/S Min	AD848A/S Typ	AD848A/S Max	Units
INPUT OFFSET VOLTAGE[1]		±5V		0.2	**1**		0.2	**1**	mV
		±15V		0.5	**2.3**		0.5	**2.3**	mV
	T_{min} to T_{max}	±5V			1.5			**2**	mV
		±15V			3.0			**3.5**	mV
Offset Drift		±5V, ±15V		7			7		µV/°C
INPUT BIAS CURRENT		±5V, ±15V		3.3	**6.6**		3.3	**6.6/5**	µA
	T_{min} to T_{max}	±5V, ±15V			7.2			**7.5**	µA
INPUT OFFSET CURRENT		±5V, ±15V		50	**300**		50	**300**	nA
	T_{min} to T_{max}	±5V, ±15V			400			**400**	nA
Offset Current Drift		±5V, ±15V		0.3			0.3		nA/°C
OPEN LOOP GAIN	V_O = ±2.5V	±5V							
	R_{LOAD} = 500Ω		**9**	13		**9**	13		V/mV
	T_{min} to T_{max}		7			**7/5**			V/mV
	R_{LOAD} = 150Ω			8			8		V/mV
	V_{OUT} = ±10V	±15V							
	R_{LOAD} = 1kΩ		**12**	20		**12**	20		V/mV
	T_{min} to T_{max}		8			**8/6**			V/mV
DYNAMIC PERFORMANCE									
Gain Bandwidth	A_{VCL}≥5	±5V		125			125		MHz
		±15V		175			175		MHz
Full Power Bandwidth[2]	V_O = 2V p-p,								
	R_L = 500Ω	±5V		24			24		MHz
	V_O = 20V p-p,								
	R_L = 1kΩ	±15V		4.7			4.7		MHz
Slew Rate		±5V		200			200		V/µs
	R_{LOAD} = 1kΩ	±15V	225	300		225	300		V/µs
Settling Time to 0.1%	−2.5V to +2.5V	±5V		65			65		ns
	10V Step, A_V = −4	±15V		100			100		ns
Phase Margin	C_{LOAD} = 10pF	±15V							
	R_{LOAD} = 1kΩ			60			60		Degrees
DIFFERENTIAL GAIN	f = 4.4MHz	±15V		0.07			0.07		%
DIFFERENTIAL PHASE	f = 4.4MHz	±15V		0.08			0.08		Degree
COMMON-MODE REJECTION	V_{CM} = ±2.5V	±5V	**92**	105		**92**	105		dB
	V_{CM} = ±12V	±15V	**92**	105		**92**	105		dB
	T_{min} to T_{max}		88			**88**			dB
POWER SUPPLY REJECTION	V_S = ±4.5V to ±18V		**85**	98		**85**	98		dB
	T_{min} to T_{max}		80			**80**			dB
INPUT VOLTAGE NOISE	f = 10kHz	±15V		5			5		nV/√Hz
INPUT CURRENT NOISE	f = 10kHz	±15V		1.5			1.5		pA/√Hz
INPUT COMMON-MODE VOLTAGE RANGE		±5V		+4.3			+4.3		V
				−3.4			−3.4		V
		±15V		+14.3			+14.3		V
				−13.4			−13.4		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 500Ω	±5V	**3.0**	3.6		**3.0**	3.6		±V
	R_{LOAD} = 150Ω	±5V	**2.5**	3		**2.5**	3		±V
	R_{LOAD} = 50Ω	±5V		1.4			1.4		±V
	R_{LOAD} = 1kΩ	±15V	**12**			**12**			±V
	R_{LOAD} = 500Ω	±15V	**10**			**10**			±V
SHORT CIRCUIT CURRENT		±15V		32			32		mA
INPUT RESISTANCE				70			70		kΩ
INPUT CAPACITANCE				1.5			1.5		pF
OUTPUT RESISTANCE	Open Loop			15			15		Ω
POWER SUPPLY									
Operating Range			**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current		±5V		4.8	**6.0**		4.8	**6.0**	mA
	T_{min} to T_{max}				7.4			**7.4/8.3**	mA
		±15V		5.1	**6.8**		5.1	**6.8**	mA
	T_{min} to T_{max}				8.0			**8.0/9.0**	mA

NOTES

[1]Input offset voltage specifications are guaranteed after 5 minutes at T_A = +25°C.

[2]Full power bandwidth = slew rate/2π V_{PEAK}. Refer to Figure 1.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. All others are guaranteed but not necessarily tested.

Specifications subject to change without notice.

Model	Conditions	V_S	AD849J Min	AD849J Typ	AD849J Max	AD849A/S Min	AD849A/S Typ	AD849A/S Max	Units
INPUT OFFSET VOLTAGE[1]		±5V		0.3	**1**		0.1	**0.75**	mV
		±15V		0.3	**1**		0.1	**0.75**	mV
	T_{min} to T_{max}	±5V			1.3			**1.0**	mV
		±15V			1.3			**1.0**	mV
Offset Drift		±5V, ±15V		2			2		µV/°C
INPUT BIAS CURRENT		±5V, ±15V		3.3	**6.6**		3.3	**6.6/5**	µA
	T_{min} to T_{max}	±5V, ±15V			7.2			**7.5**	µA
INPUT OFFSET CURRENT		±5V, ±15V		50	**300**		50	**300**	nA
	T_{min} to T_{max}	±5V, ±15V			400			**400**	nA
Offset Current Drift		±5V, ±15V		0.3			0.3		nA/°C
OPEN LOOP GAIN	V_O = ±2.5V	±5V							
	R_{LOAD} = 500Ω		**30**	50		**30**	50		V/mV
	T_{min} to T_{max}		20			**20/15**			V/mV
	R_{LOAD} = 150Ω			32			32		V/mV
	V_{OUT} = ±10V	±15V							
	R_{LOAD} = 1kΩ		**45**	85		**45**	85		V/mV
	T_{min} to T_{max}		30			**30/25**			V/mV
DYNAMIC PERFORMANCE									
Gain Bandwidth	A_{VCL}≥25	±5V		520			520		MHz
		±15V		725			725		MHz
Full Power Bandwidth[2]	V_O = 2V p-p,								
	R_L = 500Ω	±5V		20			20		MHz
	V_O = 20V p-p,								
	R_L = 1kΩ	±15V		4.7			4.7		MHz
Slew Rate		±5V		200			200		V/µs
	R_{LOAD} = 1kΩ	±15V	225	300		225	300		V/µs
Settling Time to 0.1%	−2.5V to +2.5V	±5V,		65			65		ns
	10V Step, A_V = −24	±15V		80			80		ns
Phase Margin	C_{LOAD} = 10pF	±15V							
	R_{LOAD} = 1kΩ			60			60		Degrees
DIFFERENTIAL GAIN	f = 4.4MHz	±15V		0.08			0.08		%
DIFFERENTIAL PHASE	f = 4.4MHz	±15V		0.04			0.04		Degree
COMMON-MODE REJECTION	V_{CM} = ±2.5V	±5V	**100**	115		**100**	115		dB
	V_{CM} = ±12V	±15V	**100**	115		**100**	115		dB
	T_{min} to T_{max}		96			**96**			dB
POWER SUPPLY REJECTION	V_S = ±4.5V to ±18V		**98**	120		**98**	120		dB
	T_{min} to T_{max}		94			**94**			dB
INPUT VOLTAGE NOISE	f = 10kHz	±15V		3			3		nV/$\sqrt{Hz}$
INPUT CURRENT NOISE	f = 10kHz	±15V		1.5			1.5		pA/$\sqrt{Hz}$
INPUT COMMON-MODE VOLTAGE RANGE		±5V		+4.3			+4.3		V
				−3.4			−3.4		V
		±15V		+14.3			+14.3		V
				−13.4			−13.4		V
OUTPUT VOLTAGE SWING	R_{LOAD} = 500Ω	±5V	**3.0**	3.6		**3.0**	3.6		±V
	R_{LOAD} = 150Ω	±5V	**2.5**	3		**2.5**	3		±V
	R_{LOAD} = 50Ω	±5V		1.4			1.4		±V
	R_{LOAD} = 1kΩ	±15V	**12**			**12**			±V
	R_{LOAD} = 500Ω	±15V	**10**			**10**			±V
SHORT CIRCUIT CURRENT		±15V		32			32		mA
INPUT RESISTANCE				25			25		kΩ
INPUT CAPACITANCE				1.5			1.5		pF
OUTPUT RESISTANCE	Open Loop			15			15		Ω
POWER SUPPLY									
Operating Range			±4.5		±18	±4.5		±18	V
Quiescent Current		±5V		4.8	**6.0**		4.8	**6.0**	mA
	T_{min} to T_{max}				7.4			**7.4/8.3**	mA
		±15V		5.1	**6.8**		5.1	**6.8**	mA
	T_{min} to T_{max}				8.0			**8.0/9.0**	mA

NOTES

[1]Input offset voltage specifications are guaranteed after 5 minutes at T_A = +25°C.

[2]Full power bandwidth = slew rate/2π V_{PEAK}. Refer to Figure 1.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. All others are guaranteed but not necessarily tested.

Specifications subject to change without notice.

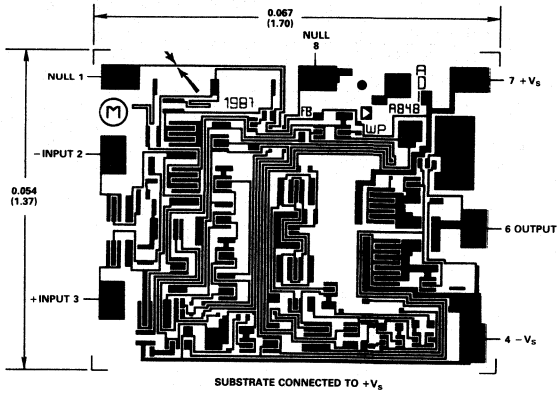
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18V
Internal Power Dissipation[2]
Plastic (N) . . . . . 1.1 Watts
Small Outline (R) . . . . . 0.9 Watts
Cerdip (Q) . . . . . 1.1 Watts
Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . +6V
Storage Temperature Range (Q) . . . . . −65°C to +150°C
(N, R) . . . . . −65°C to +125°C
Junction Temperature . . . . . +175°C
Lead Temperature Range (Soldering 60sec) . . . . . +300°C

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Mini-DIP Package: θ_{JA} = 110°C/Watt
Cerdip Package: θ_{JA} = 110°C/Watt
Small Outline Package: θ_{JA} = 155°C/Watt.

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions. (AD848 and AD849 are identical except for the part number in the upper right.)
Dimensions shown in inches and (mm).



ORDERING GUIDE

Model	Gain Bandwidth MHz	Min Stable Gain	Max Offset Voltage mV	Temperature Range – °C	Package Option[1]
AD848JN	175	5	1	0 to +70	N-8
AD848JR[2]	175	5	1	0 to +70	R-8
AD848AQ	175	5	1	−40 to +85	Q-8
AD848SQ	175	5	1	−55 to +125	Q-8
AD848SQ/883B	175	5	1	−55 to +125	Q-8
AD849JN	725	25	1	0 to +70	N-8
AD849JR[2]	725	25	1	0 to +70	R-8
AD849AQ	725	25	0.75	−40 to +85	Q-8
AD849SQ	725	25	0.75	−55 to +125	Q-8
AD849SQ/883B	725	25	0.75	−55 to +125	Q-8
AD847J/A/S	50	1	1	See AD847 Data Sheet	

NOTES
[1]N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.
[2]Plastic SOIC (R) available in tape and reel. AD848 available in S grade chips. AD849 available in J and S grade chips.

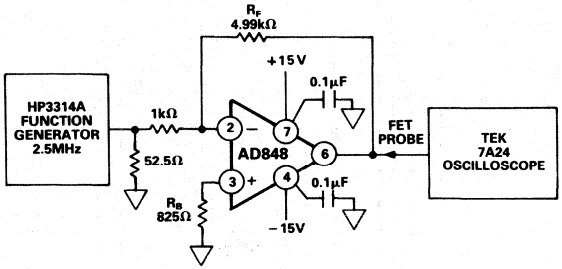


Figure 1. AD848 Inverting Amplifier Configuration

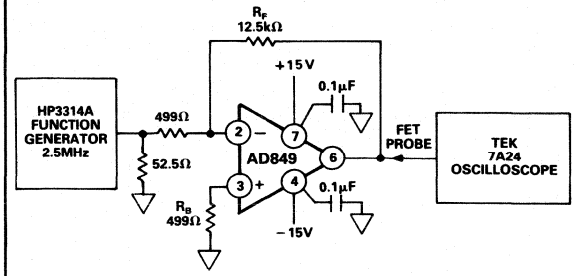


Figure 2. AD849 Inverting Amplifier Configuration

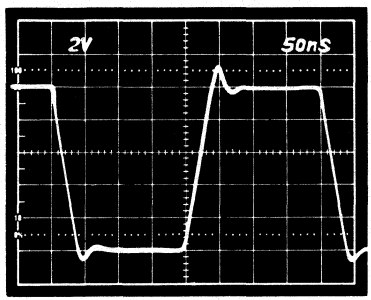


Figure 1a. AD848 Large Signal Pulse Response

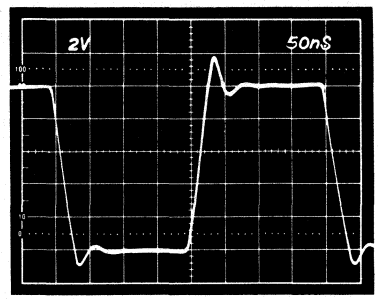


Figure 2a. AD849 Large Signal Pulse Response

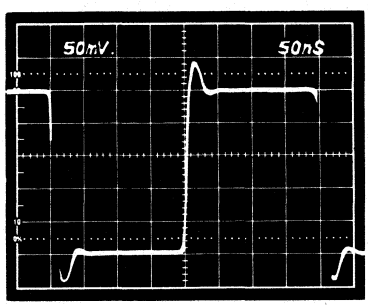


Figure 1b. AD848 Small Signal Pulse Response

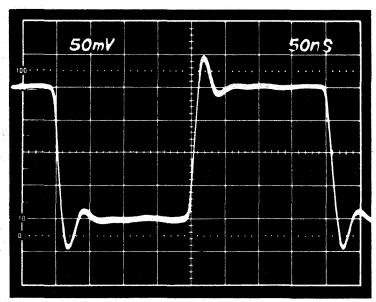


Figure 2b. AD849 Small Signal Pulse Response

OFFSET NULLING

The input voltage of the AD848 and AD849 are very low for high speed op amps, but if additional nulling is required, the circuit shown in Figure 3 can be used.

For high performance circuits it is recommended that a resistor (R_B in Figures 1 and 2) be used to reduce bias current errors by matching the impedance at each input. The offset voltage error caused by the input currents is decreased by more than an order of magnitude.

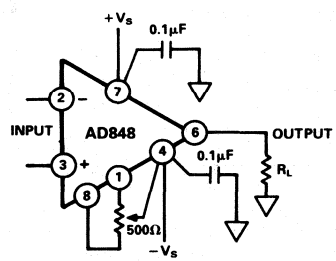


Figure 3. Offset Nulling

AD848/AD849—Typical Characteristics (@ +25°C and $V_S = \pm 15V$, unless otherwise noted)

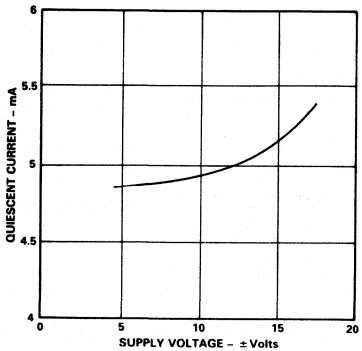


Figure 4. Quiescent Current vs. Supply Voltage (AD848 and AD849)

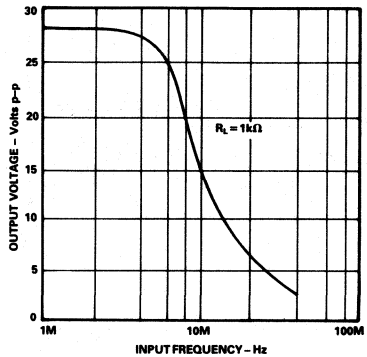


Figure 5. Large Signal Frequency Response (AD848 and AD849)

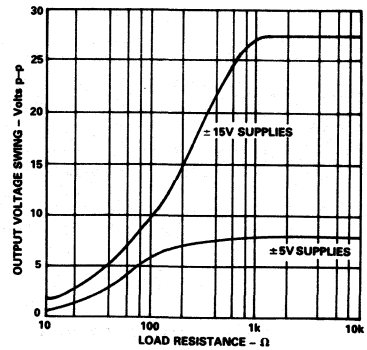


Figure 6. Output Voltage Swing vs. Load Resistance (AD848 and AD849)

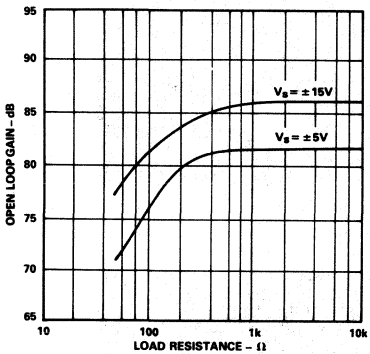


Figure 7. Open Loop Gain vs. Load Resistance (AD848)

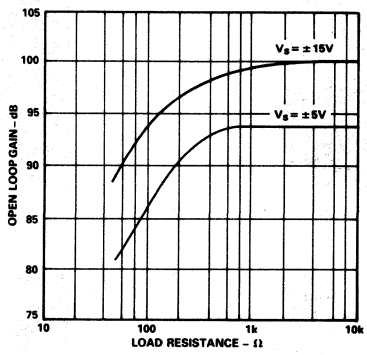


Figure 8. Open Loop Gain vs. Load Resistance (AD849)

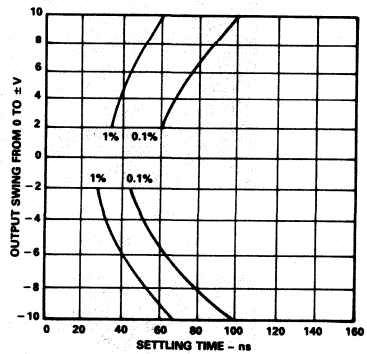


Figure 9. Output Swing and Error vs. Settling Time (AD848)

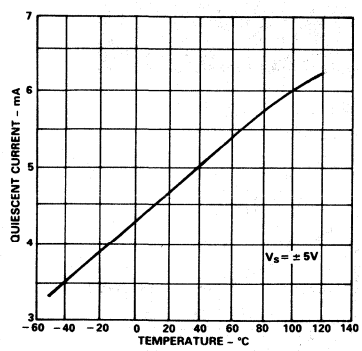


Figure 10. Quiescent Current vs. Temperature (AD848 and AD849)

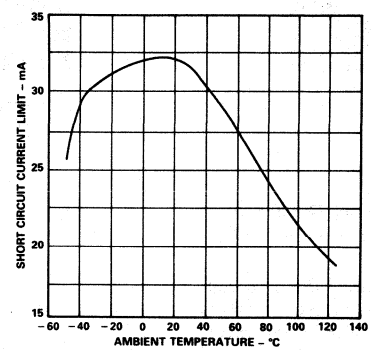


Figure 11. Short Circuit Current Limit vs. Temperature (AD848 and AD849)

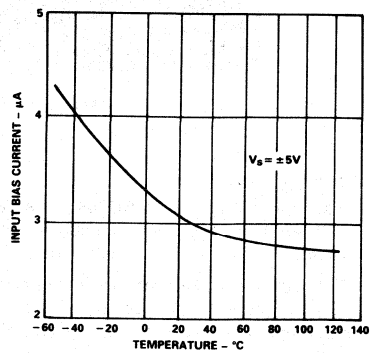


Figure 12. Input Bias Current vs. Temperature (AD848 and AD849)

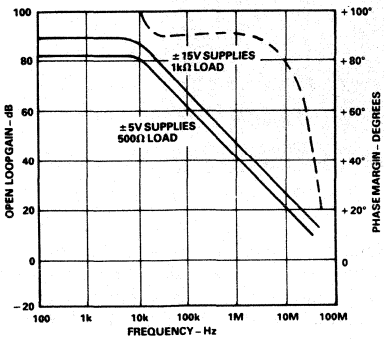


Figure 13. Open Loop Gain and Phase Margin vs. Frequency (AD848)

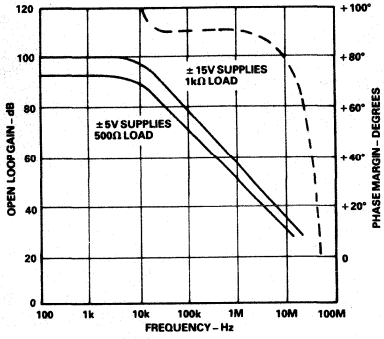


Figure 14. Open Loop Gain and Phase Margin vs. Frequency (AD849)

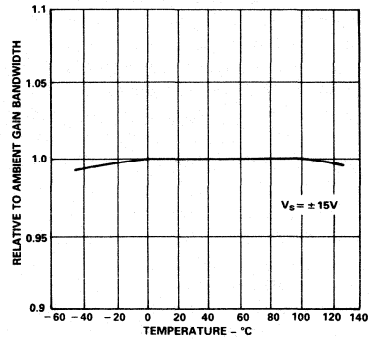


Figure 15. Normalized Gain Bandwidth Product vs. Temperature (AD848 and AD849)

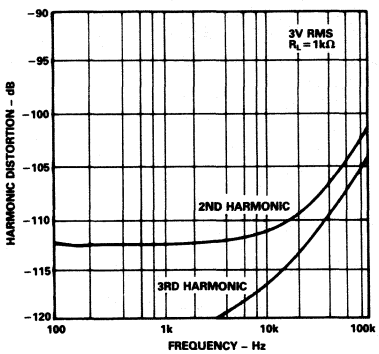


Figure 16. Harmonic Distortion vs. Frequency (AD848)

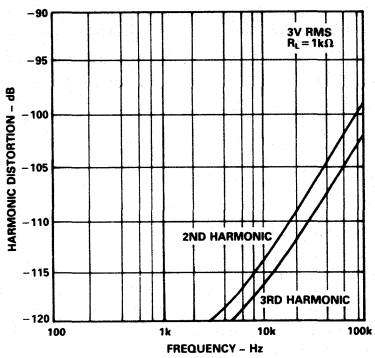


Figure 17. Harmonic Distortion vs. Frequency (AD849)

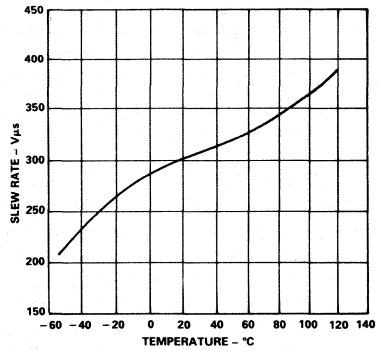


Figure 18. Slew Rate vs. Temperature (AD848 and AD849)

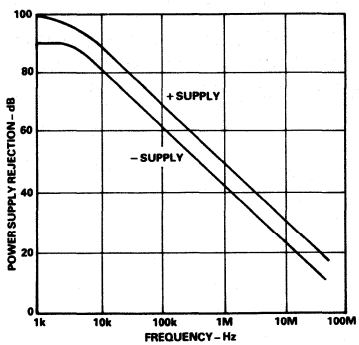


Figure 19. Power Supply Rejection vs. Frequency (AD848)

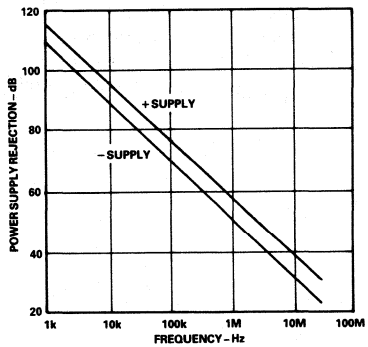


Figure 20. Power Supply Rejection vs. Frequency (AD849)

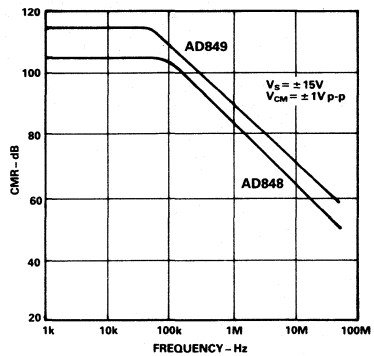


Figure 21. Common-Mode Rejection vs. Frequency

GROUNDING AND BYPASSING

In designing practical circuits with the AD848 or AD849, the user must remember that whenever high frequencies are involved, some special precautions are in order. Circuits must be built with short interconnect leads. A large ground plane should be used whenever possible to provide a low resistance, low inductance circuit path, as well as minimizing the effects of high frequency coupling. Sockets should be avoided because the increased interlead capacitance can degrade bandwidth.

Feedback resistors should be of low enough value to assure that the time constant formed with the capacitances at the amplifier summing junction will not limit the amplifier performance. Resistor values of less than 5kΩ are recommended. If a larger resistor must be used, a small (<10pF) feedback capacitor in parallel with the feedback resistor, R_F, may be used to compensate for the input capacitances and optimize the dynamic performance of the amplifier.

Power supply leads should be bypassed to ground as close as possible to the amplifier pins. 0.1μF ceramic disc capacitors are recommended.

VIDEO LINE DRIVER

The AD848 functions very well as a low cost, high speed line driver of either terminated or unterminated cables. Figure 22 shows the AD848 driving a doubly terminated cable.

The termination resistor, R_T, (when equal to the characteristic impedance of the cable) minimizes reflections from the far end of the cable. While operating off ±5V supplies, the AD848 maintains a typical slew rate of 200V/μs, which means it can drive a ±1V, 24MHz signal on the terminated cable.

A back-termination resistor (R_{BT}, also equal to the characteristic impedance of the cable) may be placed between the AD848 output and the cable in order to damp any reflected signals caused by a mismatch between R_T and the cable's characteristic impedance. This will result in a "cleaner" signal, although it requires that the op amp supply ±2V to the output in order to achieve a ±1V swing at the line.

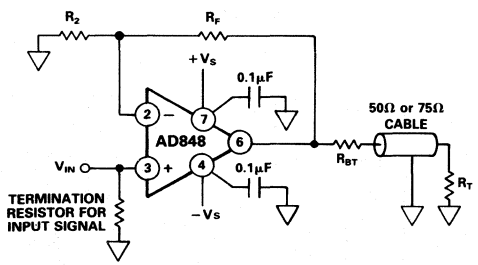


Figure 22. Video Line Driver

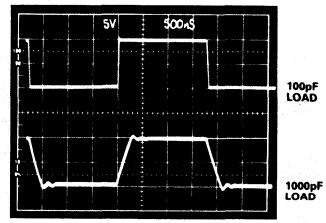


Figure 23. AD848 Driving a Capacitive Load

Often termination is not used, either because signal integrity requirements are low or because too many high frequency signals returned to ground contaminate the ground plane. Unterminated cables appear as capacitive loads. Since the AD848 and AD849 are stable into any capacitive load, the op amp will not oscillate if the cable is not terminated; however pulse integrity will be degraded. Figure 23 shows the AD848 driving both 100pF and 1000pF loads.

LOW NOISE PRE-AMP

The input voltage noise spectral densities of the AD848 and the AD849 are shown in Figure 24. The low wideband noise and high gain bandwidths of these devices makes them well suited as pre-amps for high frequency systems.

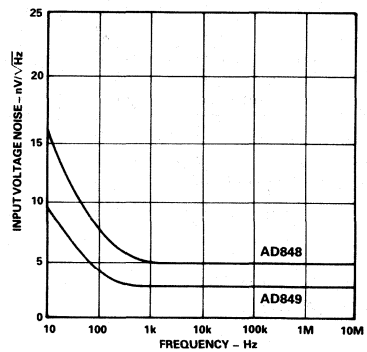


Figure 24. Input Voltage Noise Spectral Density

Input voltage noise will be the dominant source of noise at the output in most applications. Other noise sources can be minimized by keeping resistor values as small as possible.

ANALOG DEVICES

Ultrahigh Frequency Operational Amplifier

AD5539

FEATURES

Improved Replacement for Signetics SE/NE5539

AC PERFORMANCE

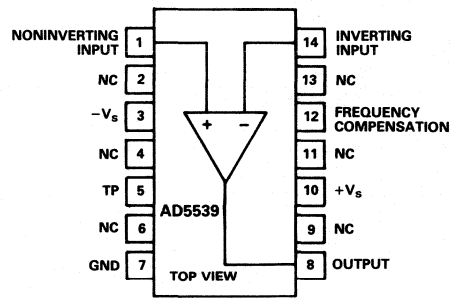
- **Gain Bandwidth Product: 1.4 GHz typ**
- **Unity Gain Bandwidth: 220 MHz typ**
- **High Slew Rate: 600 V/μs typ**
- **Full Power Response: 82 MHz typ**
- **Open-Loop Gain: 47 dB min, 52 dB typ**

DC PERFORMANCE

- **All Guaranteed DC Specifications Are 100% Tested For Each Device Over Its Full Temperature Range – For All Grades and Packages**
- **V_{OS}: 5 mV max Over Full Temperature Range (AD5539S)**
- **I_B: 20 μA max (AD5539J)**
- **CMRR: 70 dB min, 85 dB typ**
- **PSRR: 100 μV/V typ**
- **MIL-STD-883B Parts Available**

CONNECTION DIAGRAM

Plastic DIP (N) Package
or Cedip (Q) Package



PRODUCT DESCRIPTION

The AD5539 is an ultrahigh frequency operational amplifier designed specifically for use in video circuits and RF amplifiers. Requiring no external compensation for gains greater than 5, it may be operated at lower gains with the addition of external compensation.

As a superior replacement for the Signetics NE/SE5539, each AD5539 is 100% dc tested to meet all of its guaranteed dc specifications over the full temperature range of the device.

The high slew rate and wide bandwidth of the AD5539 provide low cost solutions to many otherwise complex and expensive high frequency circuit design problems.

The AD5539 is available specified to operate over either the commercial (AD5539JN/JQ) or military (AD5539SQ) temperature range. The commercial grade is available either in 14-pin plastic or cerdip packages. The military version is supplied in the cerdip package. Chip versions are also available.

PRODUCT HIGHLIGHTS

1. All guaranteed dc specifications are 100% tested.
2. The AD5539 drives 50 Ω and 75 Ω loads directly.
3. Input voltage noise is less than 4 $nV\sqrt{Hz}$.
4. Low cost RF and video speed performance.
5. ±2 volt output range into a 150 Ω load.
6. Low cost.
7. Chips available.

AD5539—SPECIFICATIONS (@ +25°C and V_S = ±8 V dc, unless otherwise noted)

Parameter	AD5539J Min	AD5539J Typ	AD5539J Max	AD5539S Min	AD5539S Typ	AD5539S Max	Units
INPUT OFFSET VOLTAGE							
Initial Offset[1]		2	5		2	3	mV
T_{min} to T_{max}			6			5	mV
INPUT OFFSET CURRENT							
Initial Offset[2]		0.1	2		0.1	1	μA
T_{min} to T_{max}			5			3	μA
INPUT BIAS CURRENT							
Initial[2]							
V_{CM} = 0		6	20		6	13	μA
Either Input							
T_{min} to T_{max}			40			25	μA
FREQUENCY RESPONSE							
R_L = 150 Ω[3]							
Small Signal Bandwidth		220			220		MHz
A_{CL} = 2[4]							
Gain Bandwidth Product		1400			1400		MHz
A_{CL} = 26 dB							
Full Power Response							
A_{CL} = 2[4]		68			68		MHz
A_{CL} = 7		82			82		MHz
A_{CL} = 20		65			65		MHz
Settling Time (1%)		12			12		ns
Slew Rate		600			600		V/μs
Large Signal Propagation Delay		4			4		ns
Total Harmonic Distortion							
R_L = ∞		0.010			0.010		%
R_L = 100 Ω[3]		0.016			0.016		%
V_{OUT} = 2 V p–p							
A_{CL} = 7, f = 1 kHz							
INPUT IMPEDANCE		100			100		kΩ
OUTPUT IMPEDANCE (f <10 MHz)		2			2		Ω
INPUT VOLTAGE RANGE							
Differential[5]							
(Max Nondestructive)		250			250		mV
Common-Mode Voltage							
(Max Nondestructive)		2.5			2.5		V
Common-Mode Rejection Ratio							
ΔV_{CM} = 1.7 V							
R_S = 100 Ω	70	85		70	85		dB
T_{min} to T_{max}	60			60			dB
INPUT VOLTAGE NOISE							
Wideband RMS Noise (RTI)		5			5		μV
BW = 5 MHz; R_S = 50 Ω							
Spot Noise		4			4		nV$\sqrt{Hz}$
F = 1 kHz; R_S = 50 Ω							
OPEN-LOOP GAIN							
V_O = +2.3 V, −1.7 V							
R_L = 150 Ω[3]	47	52	58	47	52	58	dB
R_L = 2 kΩ	47		58	48		57	dB
T_{min} to T_{max} $-R_L$ = 2 kΩ	43		63	46		60	dB

Parameter	AD5539J Min	AD5539J Typ	AD5539J Max	AD5539S Min	AD5539S Typ	AD5539S Max	Units
OUTPUT CHARACTERISTICS							
Positive Output Swing							
R_L = 150 Ω[3]	+2.3	+2.8		+2.3	+2.8		V
R_L = 2 kΩ	+2.3	+3.3		+2.5	+3.3		V
T_{min} to T_{max} with							
R_L = 2 kΩ	+2.3			+2.3			V
Negative Output Swing							
R_L = 150 Ω[3]		−2.2	**−1.7**		−2.2	**−1.7**	V
R_L = 2 kΩ		−2.9	**−1.7**		−2.9	**−2.0**	V
T_{min} to T_{max} with							
R_L = 2 kΩ			**−1.5**			**−1.5**	V
POWER SUPPLY (No Load, No Resistor to $-V_S$)							
Rated Performance		±8			±8		V
Operating Range	**±4.5**		**±10**	**±4.5**		**±10**	V
Quiescent Current							
Initial I_{CC}+		14	**18**		14	**17**	mA
T_{min} to T_{max}			**20**			**18**	mA
Initial I_{CC}−		11	**15**		11	**14**	mA
T_{min} to T_{max}			**17**			**15**	mA
PSRR							
Initial		100	**1000**		100	**1000**	μV/V
T_{min} to T_{max}			**2000**			**2000**	μV/V
TEMPERATURE RANGE							
Operating,							
Rated Performance							
Commercial (0 to +70°C)	AD5539JN, AD5539JQ						
Military (−55°C to +125°C)				AD5539SQ			
PACKAGE OPTIONS[6]							
Plastic (N-14)	AD5539JN						
Cerdip (Q-14)	AD5539JQ			AD5539SQ, AD5539SQ/883B			
J and S Grade Chips Available							

NOTES
[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[2]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C.
[3]R_X = 470 Ω to $-V_S$.
[4]Externally compensated.
[5]Defined as voltage between inputs, such that neither exceeds +2.5 V, −5.0 V from ground.
[6]For outline information see Package Information section.

Specifications subject to change without notice.

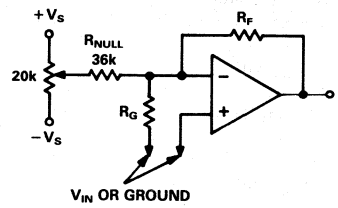
Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±10 V
Internal Power Dissipation . . . . . 550 mW
Input Voltage . . . . . +2.5 V, −5.0 V
Differential Input Voltage . . . . . 0.25 V
Storage Temperature Range (Q) . . . . . −65°C to +150°C
Storage Temperature Range (N) . . . . . −65°C to +125°C
Operating Temperature Range
AD5539JN . . . . . 0 to +70°C
AD5539JQ . . . . . 0 to +70°C
AD5539SQ . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 Seconds) . . . . . 300°C

NOTE
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OFFSET NULL CONFIGURATION

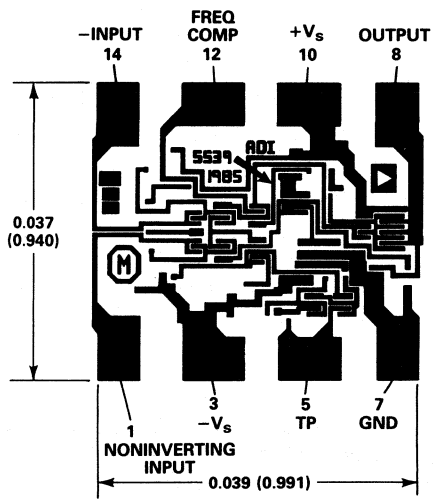


$$\text{OUTPUT NULL RANGE} \cong +V_S\left(\frac{R_F}{R_{NULL}}\right) \text{ TO } -V_S\left(\frac{R_F}{R_{NULL}}\right)$$

OFFSET NULL CONFIGURATION

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



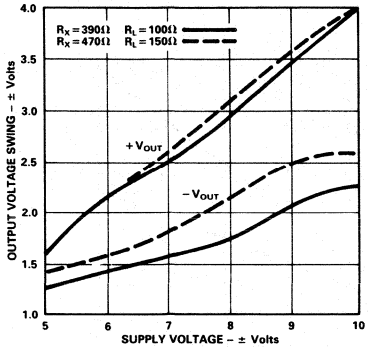


Figure 1. Output Voltage Swing vs. Supply Voltage

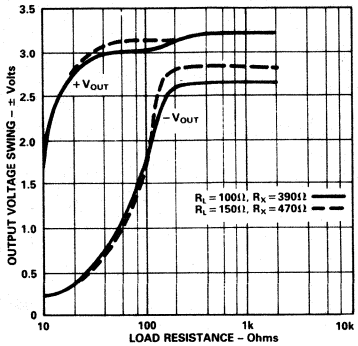


Figure 2. Output Voltage Swing vs. Load Resistance

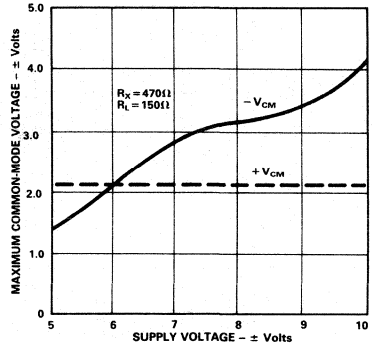


Figure 3. Maximum Common-Mode Voltage vs. Supply Voltage

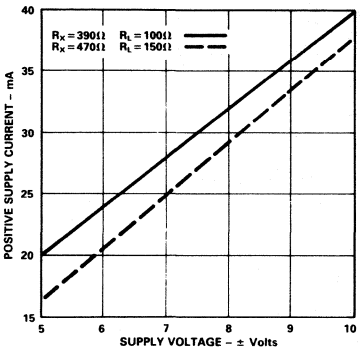


Figure 4. Positive Supply Current vs. Supply Voltage

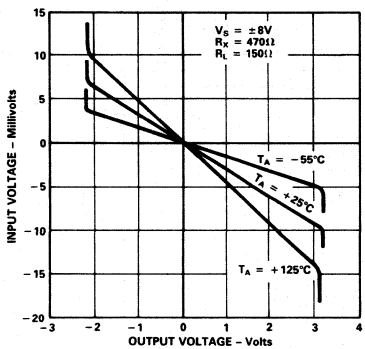


Figure 5. Input Voltage vs. Output Voltage for Various Temperatures

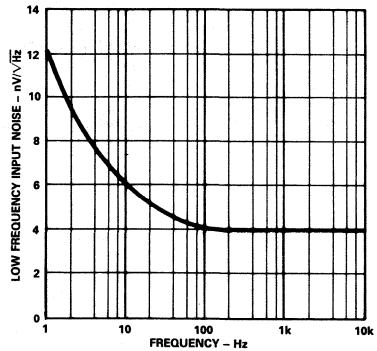


Figure 6. Low Frequency Input Noise vs. Frequency

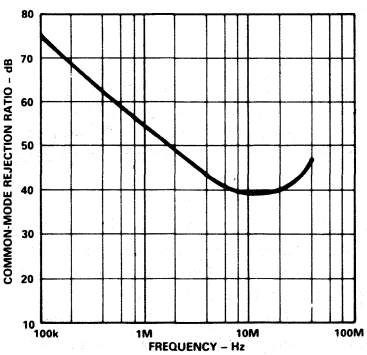


Figure 7. Common-Mode Rejection Ratio vs. Frequency

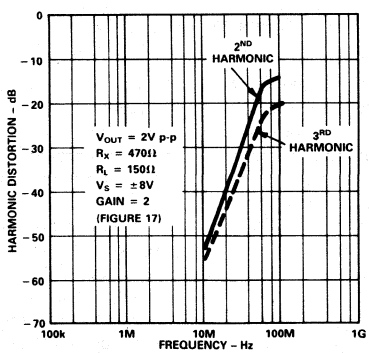


Figure 8. Harmonic Distortion vs. Frequency – Low Gain

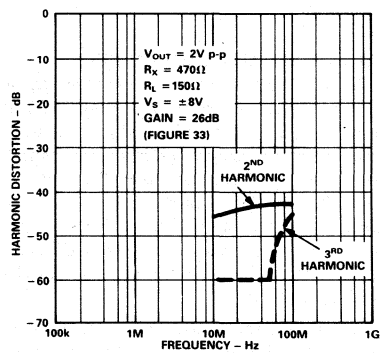


Figure 9. Harmonic Distortion vs. Frequency – High Gain

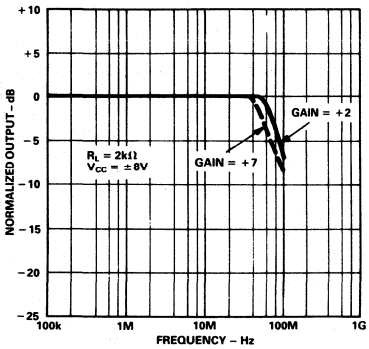


Figure 10. Full Power Response

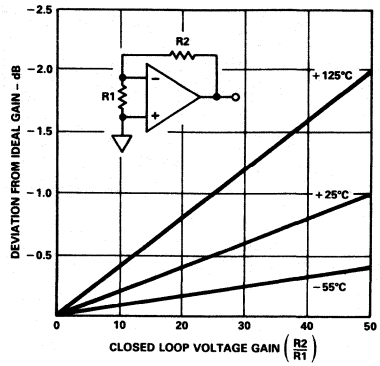


Figure 11. Deviation from Ideal Gain vs. Closed-Loop Voltage Gain

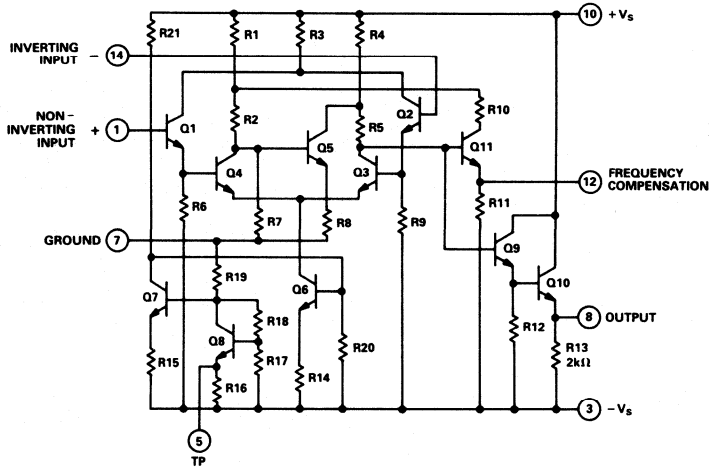


Figure 12. AD5539 Circuit

FUNCTIONAL DESCRIPTION

The AD5539 is a two-stage, very high frequency amplifier. Darlington input transistors Q1, Q4 –Q2, Q3 form the first stage — a differential gain amplifier with a voltage gain of approximately 50. The second stage, Q5, is a single-ended amplifier whose input is derived from one phase of the differential amplifier output; the other phase of the differential output is then summed with the output of Q5. The all NPN design of the AD5539 is configured such that the emitter of Q5 is returned, via a small resistor to ground; this eliminates the need for separate level shifting circuitry.

The output stage, consisting of transistors Q9 and Q10, is a Darlington voltage follower with a resistive pull-down. The bias section, consisting of transistors Q6, Q7 and Q8, provides a stable emitter current for the input section, compensating for temperature and power supply variations.

SOME GENERAL PRINCIPLES OF HIGH FREQUENCY CIRCUIT DESIGN

In designing practical circuits with the AD5539, the user must remember that whenever very high frequencies are involved, some special precautions are in order. All real-world applications circuits must be built using proper RF techniques: the use of short interconnect leads, adequate shielding, groundplanes, and very low profile IC sockets. In addition, very careful bypassing of power supply leads is a must.

Low-impedance transmission line is frequently used to carry signals at RF frequencies: 50 Ω line for telecommunications purposes and 75 Ω for video applications. The AD5539 offers a relatively low output impedance; therefore, some consideration must be given to impedance matching. A common matching technique involves simply placing a resistor in series with the amplifier output that is equal to the characteristic impedance of the transmission line. This provides a good match (although at a loss of 6 dB), adequate for many applications.

All of the circuits here were built and tested in a 50 Ω system. Care should be taken in adapting these circuits for each particular use. Any system which has been properly matched and terminated in its characteristic impedance should have the same small signal frequency response as those shown in this data sheet.

APPLYING THE AD5539

The AD5539 is stable for closed-loop gains of 4 or more as an inverter and at (noise) gains of 5 or greater as a voltage follower. This means that whenever the AD5539 is operated at noise gains below 5, external frequency compensation must be used to insure stable operation.

The following sections outline specific compensation circuits which permit stable operation of the AD5539 down to follower (noise) gains of 3 (inverting gains of 2) with corresponding −3 dB bandwidths up to 390 MHz. External compensation is achieved by modifying the frequency response to the AD5539's external feedback network (i.e., by adding lead-lag compensation) so that the amplifier operates at a noise gain of 5 (or more) at frequencies over 44 MHz, independent of signal gain.

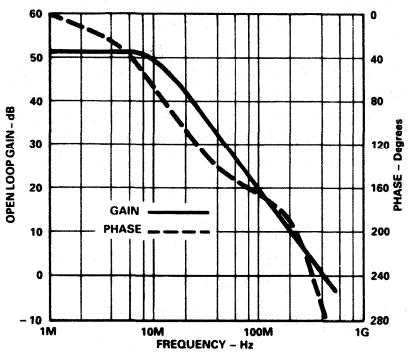


Figure 13. Small Signal Open-Loop Gain and Phase vs. Frequency

GENERAL PRINCIPLES OF LEAD AND LAG COMPENSATION

The AD5539 has its first pole or breakpoint in its open-loop frequency response at about 10 MHz (see Figure 13). At frequencies beyond 100 MHz, phase shift increases such that the output lags the input by 180° — well before the unity gain crossover frequency. Therefore, severe peaking (and possible oscillation) will result if the AD5539 is operated at noise gains below 5, unless external compensation is employed. Figure 14 shows the uncompensated closed-loop frequency response of the AD5539 when operating at a noise gain of 7. Under these conditions, excess phase shift causes nearly 10 dB of peaking at 150 MHz.

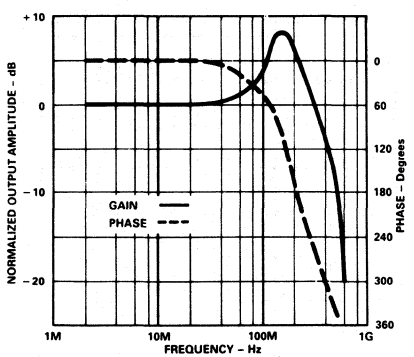


Figure 14. AD5539 Uncompensated Response, Closed-Loop Gain = 7

Figure 15 illustrates the use of both lead and lag compensation to permit stable low-gain operation. The AD5539 is shown connected as an inverting amplifier with the required external components added to provide stability and improve high frequency response. The stray capacitance between the amplifier summing junction and ground, C_X, represents whatever capacitance is associated with the particular type of op amp package used plus the stray wiring capacitance at the summing junction.

Evaluating the lead capacitance first (ignoring R_{LAG} and C_{LAG} for now): the feedback network, consisting of R2 and C_{LEAD}, has a pole frequency equal to:

$$F_A = \frac{1}{2\pi\,(C_{LEAD} + C_X)\,(R1 \parallel R2)} \quad (1)$$

and a zero frequency equal to:

$$F_B = \frac{1}{2\pi\,(R1 \times C_{LEAD})} \quad (2)$$

Usually, frequency F_A is made equal to F_B; that is, $(R1C_X) = (R2\,C_{LEAD})$, in a manner similar to the compensation used for an attenuator or scope probe. However, if the pole frequency, F_A, will lie above the unity gain crossover frequency (440 MHz), then the optimum location of F_B will be near the

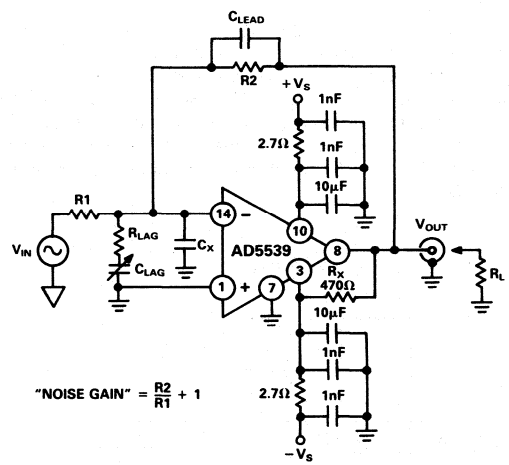


Figure 15. Inverting Amplifier Model Showing Both Lead and Lag Compensation

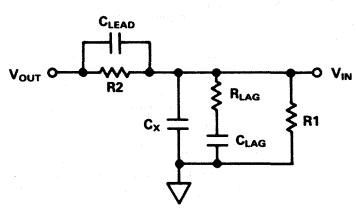


Figure 16. A Model of the Feedback Network of the Inverting Amplifier

crossover frequency. Both of these circuit techniques add a large amount of leading phase shift at the crossover frequency, greatly aiding stability.

The lag network (R_{LAG}, C_{LAG}) increases the feedback attenuation, i.e., the amplifier operates at a higher noise gain, above some frequency, typically one-tenth of the crossover frequency. As an example, to achieve a noise gain of 5 at frequencies above 44 MHz, for the circuit of Figure 15, would require a network of:

$$R_{LAG} = \frac{R1}{(4R1/R2) - 1} \quad (3)$$

and . . .

$$C_{LAG} = \frac{1}{2\pi R_{LAG} (44 \times 10^6)} \quad (4)$$

It is worth noting that an R_{LAG} resistor may be used alone, to increase the noise gain above 5 at all frequencies. However, this approach has the disadvantage of also increasing the dc offset and low frequency noise errors by an amount equal to the increase in gain, in this case, by a factor of 5.

SOME PRACTICAL CIRCUITS

The preceding general principles may now be applied to some actual circuits.

A General Purpose Inverter Circuit

Figure 17 is a general purpose inverter circuit operating at a gain of −2.

For this circuit, the total capacitance at the inverting input is approximately 3 pF; therefore, C_{LEAD} from Equations 1 and 2 needs to be approximately 1.5 pF. As shown in Figure 17, a small trimmer is used to optimize the frequency response of this circuit. Without a lag compensation network, the noise gain of the circuit is 3.0 and, as shown in Figure 18, the output amplitude remains within ±0.5 dB to 170 MHz and the −3 dB bandwidth is 200 MHz.

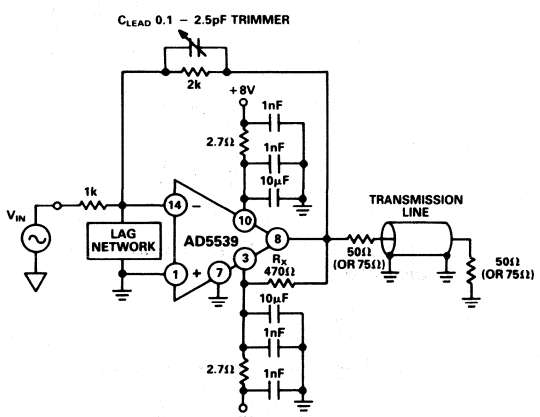


Figure 17. A General Purpose Inverter Circuit

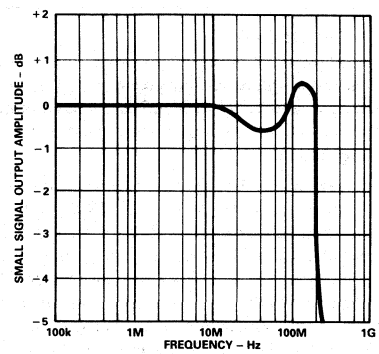


Figure 18. Response of the (Figure 17) Inverter Circuit without a Lag Compensation Network

A lag network (Figure 15) can be added to improve the response of this circuit even further as shown in Figures 19 and 20. In almost all cases, it is imperative to make capacitor C_{LEAD} adjustable; in some cases, C_{LAG} must also be variable. Otherwise, component and circuit capacitance variations will dominate circuit performance.

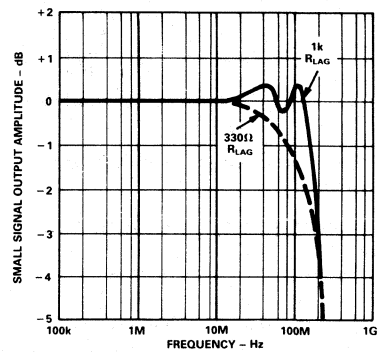


Figure 19. Response of the (Figure 17) Inverter Circuit with an R_{LAG} Compensation Network Employed

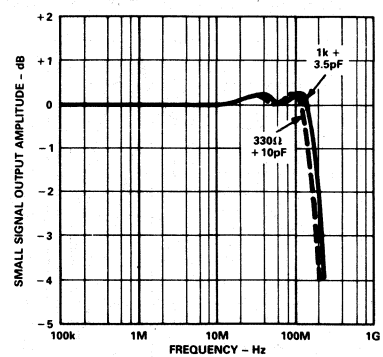


Figure 20. Response of the (Figure 17) Inverter Circuit with an R_{LAG} and a C_{LAG} Compensation Network Employed

Figures 21 and 22 show the small and large signal pulse responses of the general purpose inverter circuit of Figure 17, with C_{LEAD}=1.5 pF, R_{LAG}=330 Ω and C_{LAG}=3.5 pF.

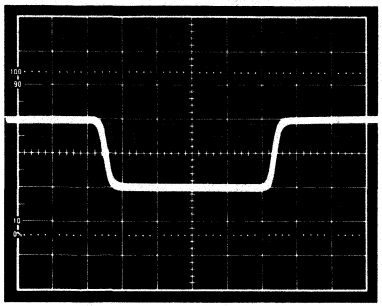


Figure 21. Small Signal Pulse Response of the (Figure 17) Inverter Circuit; Vertical Scale: 50 mV/div; Horizontal Scale: 5 ns/div

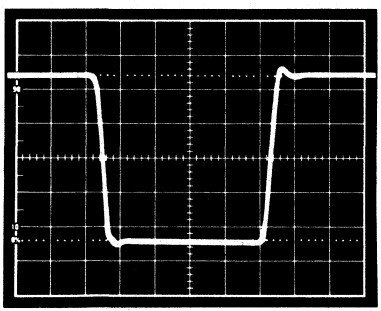


Figure 22. Large Signal Response of the (Figure 17) Inverter Circuit; Vertical Scale: 200 mV/div, Horizontal Scale: 5 ns/div

A C_{LEAD} capacitor may be used to limit the circuit bandwidth and to achieve a single pole response free of overshoot

$$\left(-3\ dB\ frequency = \frac{1}{2\pi\ R2\ C_{LEAD}}\right)$$

If this option is selected, it is recommended that a C_{LEAD} be connected between Pin 12 and the summing junction, as shown in Figure 23. Pin 12 provides a separately buffered version of the output signal. Connecting the lead capacitor here avoids the excess output-stage phase shift and subsequent oscillation problems (at approx. 350 MHz) which would otherwise occur when using the circuit of Figure 17 with a C_{LEAD} of more than about 2 pF.

Figure 24 shows the response of the circuit of Figure 23 for each connection of C_{LEAD}. Lag components may also be added to this circuit to further tailor its response, but, in this case, the results will be slightly less satisfactory than connecting C_{LEAD} directly to the output, as was done in Figure 17.

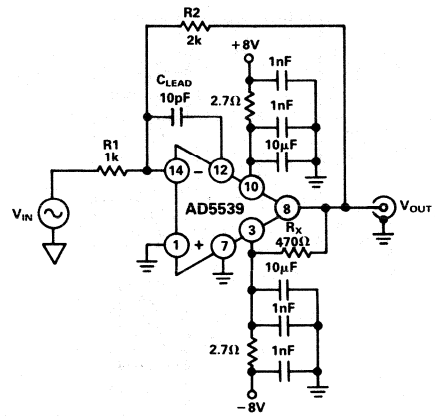


Figure 23. A Gain of 2 Inverter Circuit with the C_{LEAD} Capacitor Connected to Pin 12

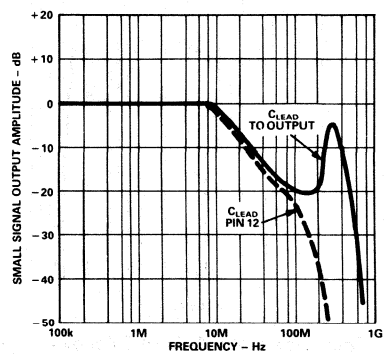


Figure 24. Response of the Circuit of Figure 23 with C_{LEAD} = 10 pF

A General Purpose Voltage Follower Circuit

Noninverting (voltage follower) circuits pose an additional complication, in that when a lag network is used, the source impedance will affect the noise gain. In addition, the slightly greater bandwidth of the noninverting configuration makes any excess phase shift due to the output stage more of a problem.

For example, a gain of 3 noninverting circuit with C_{LEAD} connected normally (across the feedback resistor — Figure 25) will require a source resistance of 200 Ω or greater to prevent UHF oscillation; the extra source resistance provides some damping as well as increasing the noise gain. The frequency response plot of Figure 26 shows that the highest −3 dB frequency of all the applications circuits can be achieved using this connection, unfortunately, at the expense of a noise gain of 14.2.

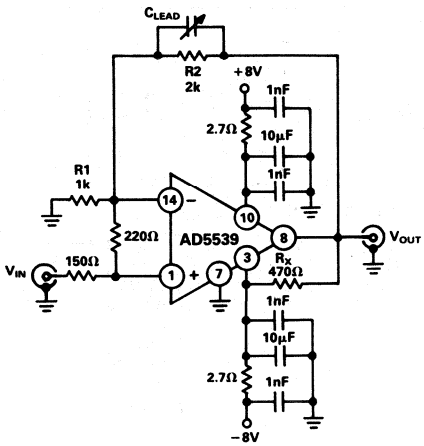


Figure 25. A Gain of 3 Follower with Both Lead and Lag Compensation

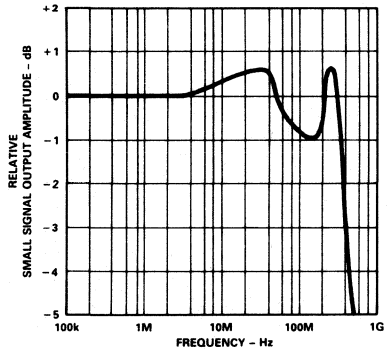


Figure 26. Response of the Gain of 3 Follower Circuit

Adding a lag capacitor (Figure 27) will greatly reduce the mid-band and low frequency noise gain of the circuit while sacrificing only a small amount of bandwidth as shown in Figure 28.

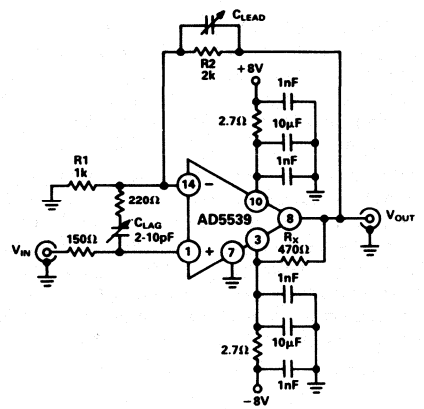


Figure 27. A Gain of 3 Follower Circuit with Both C_{LEAD} and R_{LAG} Compensation

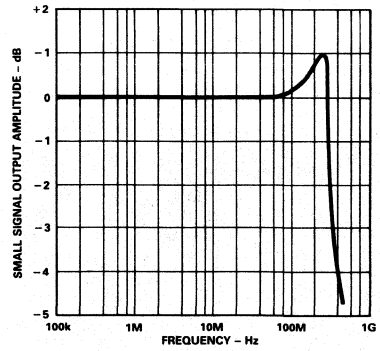


Figure 28. Response of the Gain of 3 Follower with C_{LEAD}, C_{LAG} and R_{LAG}

These same principles may be applied when capacitor C_{LEAD} is connected to Pin 12 (Figure 29). Figure 30 shows the bandwidth of the gain of 3 amplifier for various values of R_{LAG}. It can be seen from these response plots that a high noise gain is still needed to achieve a reasonably flat response (the smaller the

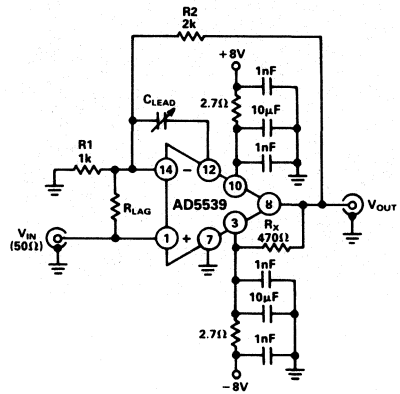


Figure 29. A Gain of 3 Follower Circuit with C_{LEAD} Compensation Connected to Pin 12

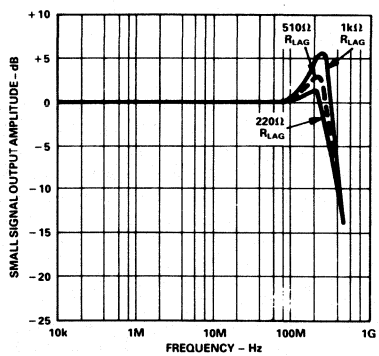


Figure 30. Response of the Gain of 3 Follower Circuit with C_{LEAD} Connected to Pin 12

value of R_{LAG}, the higher the noise gain). For example, with a 220 Ω R_{LAG} and a 50 Ω source resistance, the noise gain will be 12.8, because the source resistance affects the noise gain.

Figures 31 and 32 show the small and large signal responses of the circuit of Figure 29.

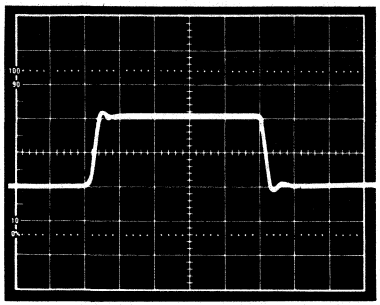


Figure 31. The Small-Signal Pulse Response of the Gain of 3 Follower Circuit with R_{LAG} and C_{LEAD} Compensation to Pin 12; Vertical Scale: 50 mV/div; Horizontal Scale: 5 ns/div

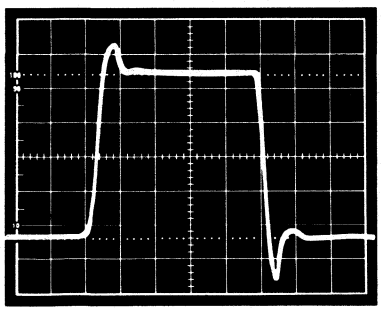


Figure 32. The Large-Signal Pulse Response of the Gain of 3 Follower Circuit with R_{LAG} and C_{LEAD} Compensation to Pin 12; Vertical Scale: 200 mV/div; Horizontal Scale: 5 ns/div

A Video Amplifier Circuit with 20 dB Gain (Terminated)
High gain applications (14 dB and up) require only a small lead capacitance to obtain flat response. The 26 dB (20 dB terminated) video amplifier circuit of Figure 33 has the response shown in Figure 34 using only approximately 0.5–1 pF lead capacitance. Again, a small C_{LEAD} can be connected, either to the output or to Pin 12 with very little difference in response.

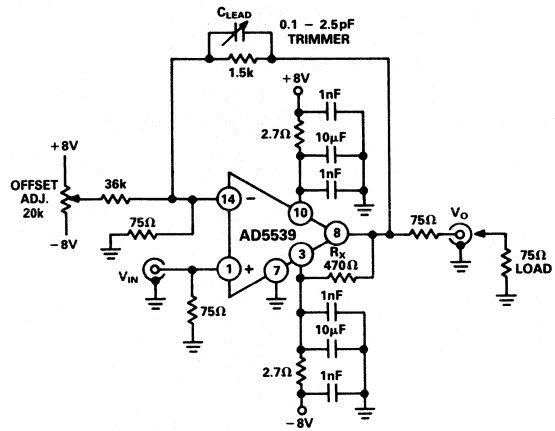


Figure 33. A 20 dB Gain Video Amplifier for 75 Ω Systems

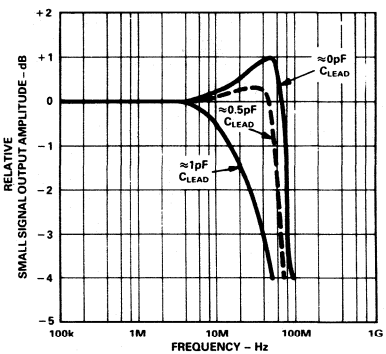


Figure 34. Response of the 20 dB Video Amplifier

In color video applications, the quality of differential gain and differential phase response is very important. Figures 35 and 36 show a circuit and test setup to measure the AD5539's response to a modulated ramp signal (0–90 IRE p–p ramp, 40 IRE p–p modulation, 4.4 MHz).

Figures 37 and 38 show the differential gain and phase response.

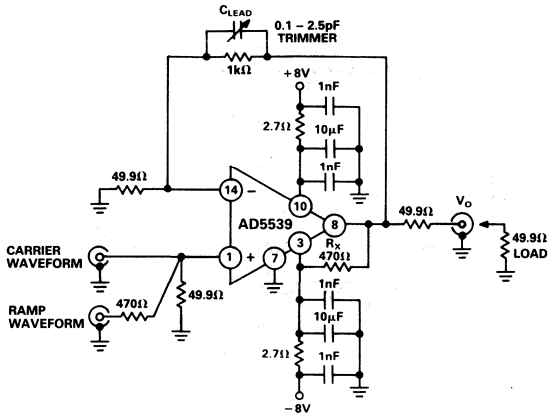


Figure 35. Differential Gain and Phase Measurement Circuit

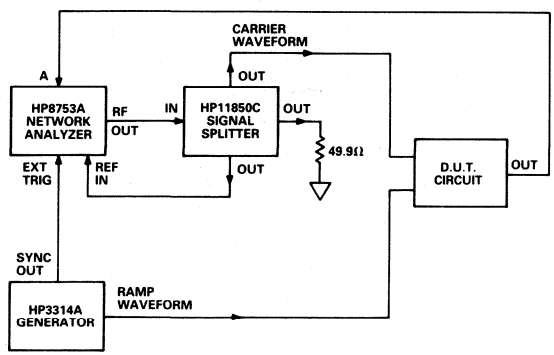


Figure 36. Differential Gain and Phase Test Setup

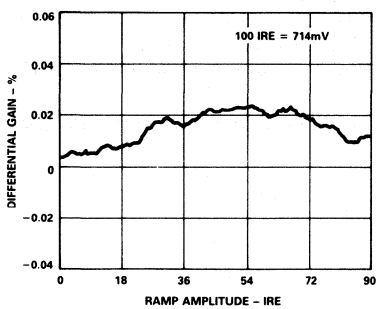


Figure 37. Differential Gain vs. Ramp Amplitude

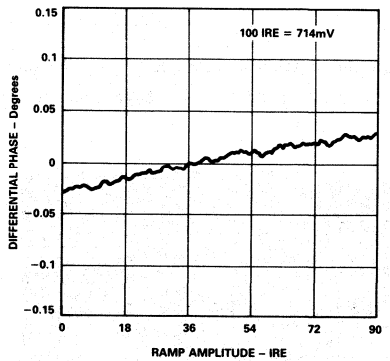


Figure 38. Differential Phase vs. Ramp Amplitude

MEASURING AD5539 SETTLING TIME

Measuring the very rapid settling times associated with AD5539 can be a real problem for the designer; proper component layout must be used and appropriate test equipment selected. In addition, both cable dispersion (a function of cable losses) and the quality of termination (SWR) directly affect the measurement. The circuit of Figure 39 was used to make a "brute force" AD5539 settling time measurement. The fixture containing the circuit was connected directly — using a male BNC connector (but no cable) — onto the front of a 50 Ω input oscilloscope preamp. A digital mainframe was then used to capture, average, and expand the error signal. Most of the small-scale waveform aberrations shown on the figure were caused by the oscilloscope itself, especially the glitch at 15 ns. The pulse source used for this measurement was an EH-SPG2000 pulse generator set for a 1 ns rise-time; it was coupled directly to the circuit using 18" of microwave 50 Ω hard line.

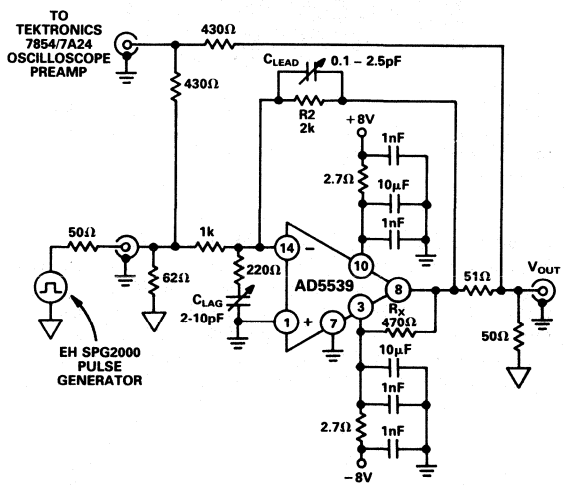


Figure 39. AD5539 Settling Time Test Circuit

APPLICATIONS SUMMARY CHART

	R1	R2[1]	R_{LAG}	C_{LAG}[2]	C_{LEAD}[2]	GAIN	GAIN FLATNESS (TRIMMED)	3 dB BANDWIDTH
Gain = −1 to −5 Circuit of Fig. 17	$\frac{R2}{G}$	2 k	$\leq \frac{R1}{4\frac{R1}{R2} - 1}$	$\geq \frac{1}{2\pi (44 \times 10^6) R_{LAG}}$	$\approx \frac{3\text{ pF}}{G}$	−2	±0.2 dB	200 MHz
Gain = −1 to −5 Circuit of Fig. 23	$\frac{R2}{G}$	2 k	$\leq \frac{R1}{4\frac{R1}{R2} - 1}$	$\geq \frac{1}{2\pi (44 \times 10^6) R_{LAG}}$	$\approx \frac{3\text{ pF}}{G}$	−2	±1 dB	180 MHz
Gain = −2 to +5[3] Circuit of Fig. 27	$\frac{R2}{G-1}$	2 k	$\leq \frac{R1}{10\frac{R1}{R2} - 1}$	$\geq \frac{1}{2\pi (44 \times 10^6) R_{LAG}}$	$\approx \frac{3\text{ pF}}{G-1}$	+3	±1 dB	390 MHz
Gain = +2 to +5[4] Circuit of Fig. 29	$\frac{R2}{G-1}$	2 k	$\leq \frac{R1}{10\frac{R1}{R2} - 1}$	NA	$\approx \frac{3\text{ pF}}{G-1}$	+3	±0.5 dB	340 MHz
Gain < −5	$\frac{R2}{G}$	1.5 k	NA	NA	Trimmer[5]	−20	±0.2 dB	80 MHz
Gain >+5	$\frac{R}{G-1}$	1.5 k	NA	NA	Trimmer[5]	+20	±0.2 dB	80 MHz

NOTES
G=Gain NA=Not Applicable
[1]Values given for specific results summarized here—applications can be adapted for values different than those specified.
[2]It is recommended that C_{LEAD} and C_{LAG} be trimmers covering a range that includes the computed value above.
[3]$R_{SOURCE} \geq 200\ \Omega$.
[4]$R_{SOURCE} \geq 50\ \Omega$.
[5]Use Voltronics CPA2 0.1–2.5 pF Teflon Trimmer Capacitor (or equivalent).

The photos of Figures 40 and 41 demonstrate how the AD5539 easily settles to 1% (1 mV) in less than 12 ns; settling to 0.1% (100 μV) requires less than 25 ns.

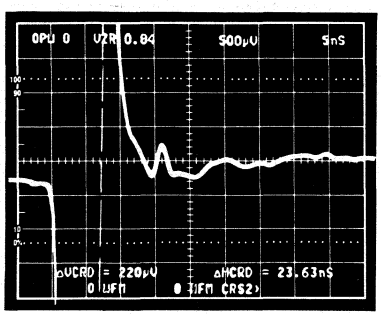


Figure 40. Error Signal from AD5539 Settling Time Test Circuit – Falling Edge. Vertical Scale: 5 ns/div.; Horizontal Scale: 500 μV/div

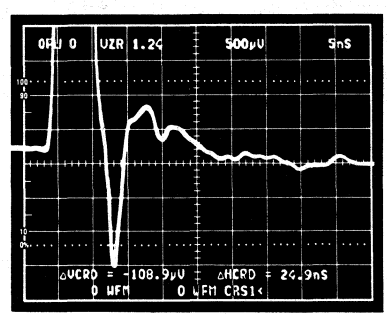


Figure 41. Error Signal from AD5539 Settling Time Test Circuit – Rising Edge. Vertical Scale: 5 ns/div.; Horizontal Scale: 500 μV/div

Figure 42 shows the oscilloscope response of the generator alone, set up to simulate the ideal test circuit error signal (Figure 43).

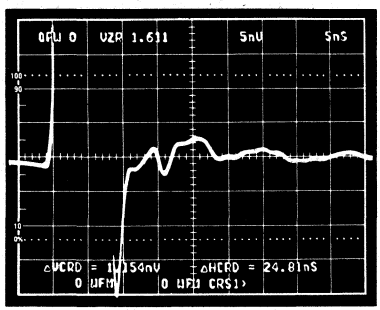


Figure 42. The Oscilloscope Response Alone Directly Driven by the Test Generator. Vertical Scale: 5 ns/div.; Horizontal Scale: 500 μV/div

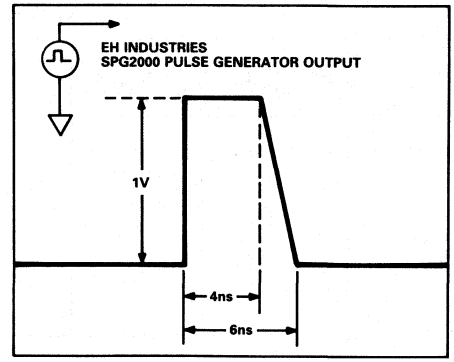


Figure 43. A Simulated Ideal Test Circuit Error Signal

A 50 MHz VOLTAGE-CONTROLLED AMPLIFIER

Figure 44 is a circuit for a 50 MHz voltage-controlled amplifier (VCA) suitable for use in high quality video-speed applications. This circuit uses the AD5539 as an output amplifier for the AD539, a high bandwidth multiplier. The outputs from the two signal channels of the AD539 are applied to the op amp in a subtracting configuration. This connection has two main advantages: first, it results in better rejection of the control voltage, particularly when over-driven (V_X<0 or V_X>3.3 V). Secondly, it provides a choice of either noninverting or inverting responses, using either input V_{Y1} or V_{Y2}, respectively. In this circuit, the output of the op amp will equal:

$$V_{OUT} = \frac{V_X\,(V_{Y1} - V_{Y2})}{2V} \text{ for } V_X > 0$$

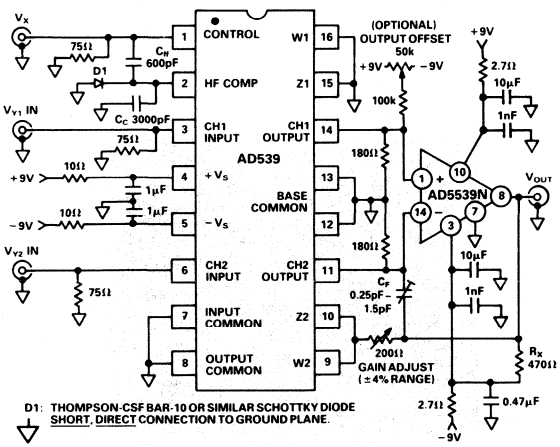


Figure 44. A Wide Bandwidth Voltage-Controlled Amplifier

Hence, the gain is unity at V_X = +2 V. Since V_X can overrange to +3.3 V, the maximum gain in this configuration is about 4.3 dB. (Note: If Pin 9 of the AD539 is grounded, rather than connected to the output of the 5539N, the maximum gain becomes 10 dB.)

The bandwidth of this circuit is over 50 MHz at full gain, and is not substantially affected at lower gains. Of course, when V_X is zero (or slightly negative, to override the residual input offset) there is still a small amount of capacitive feedthrough at high frequencies; therefore, extreme care is needed in laying out the PC board to minimize this effect. Also, for small values of V_X, the combination of this feedthrough with the multiplier output can cause a dip in the response where they are out of phase. Figure 45 shows the ac response from the noninverting input, with the response from the inverting input, V_{Y2}, essentially identical. Test conditions: V_{Y1} = 0.5 V rms for values of V_X from +10 mV to +3.16 V; this is with a 75 Ω load on the output. The feedthrough at V_X = −10 mV is also shown.

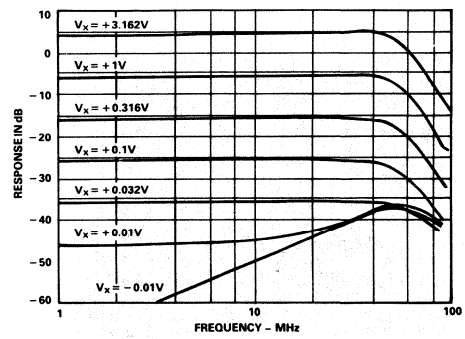


Figure 45. AC Response of the VCA at Different Gains V_Y = 0.5 V RMS

The transient response of the signal channel at $V_X = +2$ V, $V_Y = V_{OUT} = +$ or -1 V is shown in Figure 46; with the VCA driving a 75 Ω load. The rise and fall times are both approximately 7 ns.

A few final circuit details: in general, the control amplifier compensation capacitor for Pin 2, C_C, must have a minimum value of 3000 pF (3 nF) to provide both circuit stability and maximum control bandwidth. However, if the *maximum* control bandwidth is not needed, then it is advisable to use a larger value of C_C, with typical values between 0.01 and 0.1 μF. Like many aspects of design, the value of C_C will be a tradeoff: higher values of C_C will lower the high frequency distortion, reduce the high frequency crosstalk and improve the signal channel phase response. Conversely, lower values of C_C will provide a higher control channel bandwidth at the expense of degraded linearity in the output response when amplitude modulating a carrier signal.

The control channel bandwidth will vary in inverse proportion to the value of C_C, providing a typical bandwidth of 2 MHz with a C_C of 0.01 μF and a V_X voltage of +1.7 volts.

Both the bandwidth and pulse response of the control channel can be further increased by using a feedforward capacitor, C_{ff}, with a value between 5 and 20 percent of C_C. C_{ff} should be carefully adjusted to give the best pulse response for a particular step input applied to the control channel. Note that since C_{ff} is connected between a linear control input (Pin 1) and a logarithmic node, the settling time of the control channel with a pulse input will vary with different control input step levels.

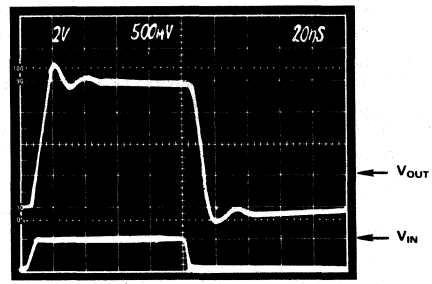


Figure 46. Transient Response of the Voltage-Controlled Amplifier $V_X = +2$ Volts, $V_Y = \pm 1$ Volt

Diode D1 clamps the logarithmic control node at Pin 2 of the AD539, (preventing this point from going too negative); this diode helps decrease the circuit recovery time when the control input goes below ground potential.

THE AD539/5539 COMBINATION AS A FAST, LOW FEEDTHROUGH, VIDEO SWITCH

Figure 47 shows how the AD539/5539 combination can be used to create a fast video speed switch suitable for many high fre-

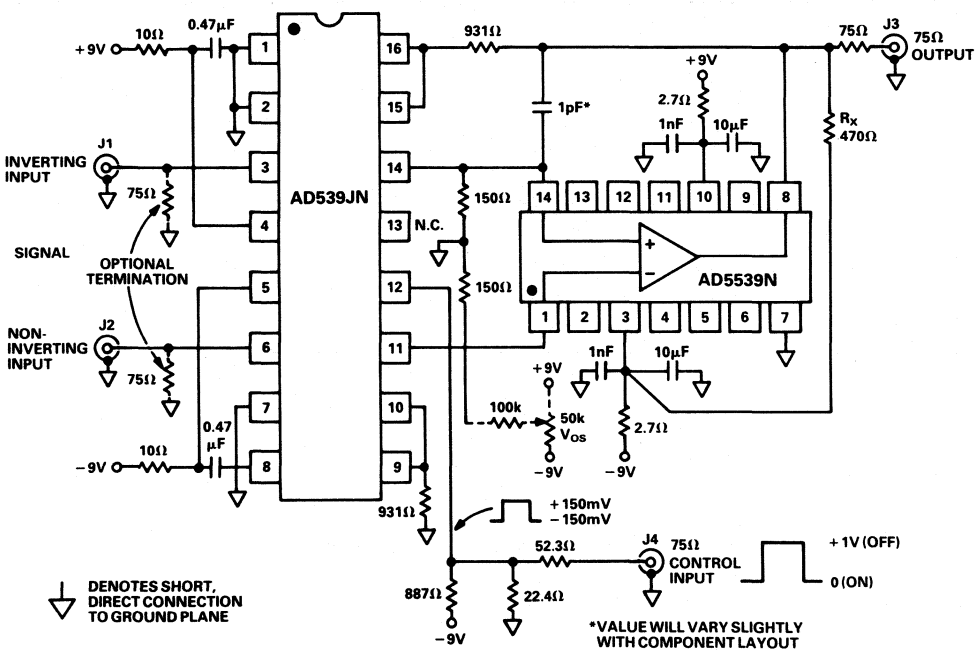


Figure 47. An Analog Multiplier Video Switch

quency applications including color key switching. It features both inverting and noninverting inputs and can provide an output of ±1 V into a reverse-terminated 75 Ω load (or ±2 V into 150 Ω). An optional output offset adjustment is provided. The input range of the video switch is the same as the output range: ±1 V at either input generates ±1 V (noninverting) or ∓1 V (inverting) across the 75 Ω load. The circuit provides a gain of about 1, when "ON," or zero when "OFF."

The differential configuration uses both channels of the AD539 not only to provide alternative input phases, but also to eliminate the switching pedestal due to step changes in the output current as the AD539 is gated on or off.

Figure 49 shows the response to a pulse of 0 to +1 V on the signal channel. With the control input held at zero, the rise time is under 10 ns. The response from the inverting input is similar.

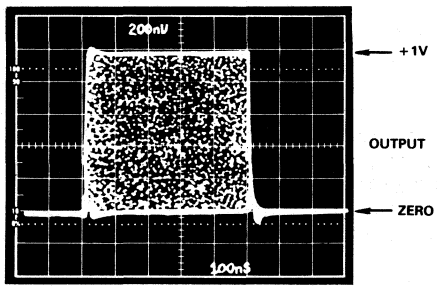


Figure 48. The Control Response of the Video Switcher

The differential-gain and differential-phase characteristics of this switch are compatible with video applications. The incremental gain changes less than 0.05 dB over a signal window of 0 to +1 V, with a phase variation of less than 0.5 degree at the subcarrier frequency of 3.58 MHz. The noise level of this circuit measured at the 75 Ω load is typically 200 μV in a 0 to 5 MHz bandwidth or approximately 100 nV per root hertz. The noise spectral density is essentially flat to 40 MHz.

The waveforms shown in Figures 48 and 49 were taken across a 75 Ω termination; in both photos, the signal of 0 to +1 V (in this case, an offset sine wave at 1 MHz) was applied to the noninverting input. In Figure 48, the envelope response shows the output being fully switched in about 50 ns. Note that the output is ON when the control input is zero (or more negative) and OFF for a control input of +1 V or more. There is very little control-signal breakthrough.

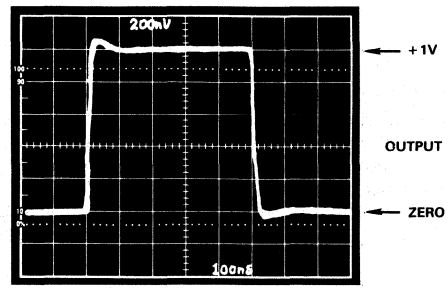


Figure 49. The Signal Response of the Video Switcher

Wide Bandwidth, Fast Settling Operational Amplifier

AD9610

FEATURES

Ultrastable Unity Gain Bandwidth (100MHz)
Bandwidth Is Independent of Gain Settings
18ns Settling to 0.1%
Low Power Dissipation (630mW)
Complete Overdrive Protection
Low Distortion (THD: −59dBc @ 20MHz, −78dBc @ 5MHz, −100dBc @ 10kHz)
Excellent DC Specifications
Available Processed to MIL-STD 883

APPLICATIONS

Driving Flash Converters
High Speed DAC I/V Converters
Radar, IF Processors
Broadband, Digital Radio
Photodiode Preamps (FLIR)
ATE/Pulse Generators
Imaging/Display Drivers

GENERAL DESCRIPTION

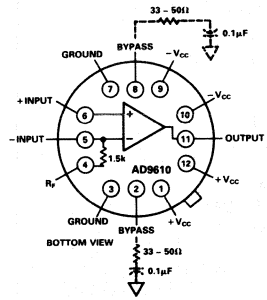
The AD9610 is a fast settling, wide bandwidth, dc coupled, operational amplifier which combines superior dc specifications and exceptional dynamic performance with impeccable spectral purity (harmonic distortion, intermodulation distortion, noise, etc.) over the full bandwidth. This combination provides remarkable versatility and utility for high speed designers.

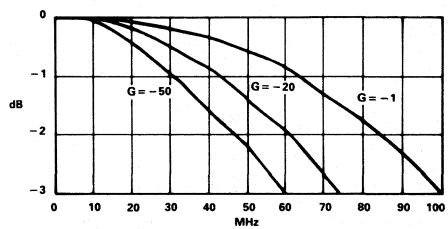
Thin-film technology and innovative design techniques help assure stable operation over the complete operating temperature range. Input offset voltage is ±0.3mV, with 5μV/°C drift; input bias currents are ±15μA with ±30nA/°C drift.

Unique internal architecture employing current feedback keeps the AD9610 inherently stable over its complete gain range and assures wide bandwidth at all gain settings. With G = −1, −3dB bandwidth is 120MHz; with G = −10, −3dB bandwidth is 100MHz. When G = −50, the −3dB bandwidth is 60MHz. Slew rate, fall time and settling time are also independent of gain.

Frequency domain performance for the AD9610 is unmatched. The part can be used in applications requiring wide spurious free dynamic range. At 10kHz total harmonic distortion (THD) is −100dBc; at 1MHz the THD is −85dBc; at 20MHz the THD is −59dBc. Third order intermodulation distortion is similarly impressive, which is often required in communications applications.

FUNCTIONAL BLOCK DIAGRAM





AD9610 Inverting Gain

The design of the AD9610 makes it easy to apply. The unit requires no external compensation. An internal 1.5kΩ feedback resistor is available to the user by connecting Pin 4 to Pin 11. This resistor is trimmed for gain accuracy and should be used when the full bandwidth of the amplifier is required. To achieve higher gains, and for lower bandwidth applications, an external resistor can be used. Pins 2 and 8 are bypass pins and should be connected to ground through 33 – 50Ω resistors and 0.1μF ceramic capacitors; effective decoupling of the power supplies is also important to obtain optimum high frequency performance.

Two temperature ranges are available. The AD9610BH is guaranteed over a case temperature range of −25°C to +85°C; the AD9610TH is for a range of −55°C to +125°C. The AD9610 is available in versions compliant with MIL-STD-883. Refer to the *Analog Devices Military Products Databook* or current AD9610/883B data sheet for detailed specifications.

AD9610—SPECIFICATIONS

DC ELECTRICAL CHARACTERISTICS ($\pm V = \pm 15V$; $A_V = -10$; $R_{IN} = 150\Omega$; $R_F = 1.5k\Omega$; No R_{LOAD})

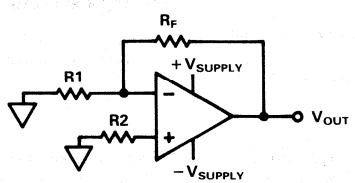
	Parameter (Conditions)	AD9610BH/TH Typical @ +25°C	AD9610BH[1] Min/Max @ −25°C	AD9610BH[1] Min/Max @ +25°C	AD9610BH[1] Min/Max @ +85°C	AD9610TH[2] Min/Max @ −55°C	AD9610TH[2] Min/Max @ +25°C	AD9610TH[2] Min/Max @ +125°C	Units
✓	Offset Voltage	±0.3	±4.0	±1.0	±2.5	±4.0	±1.0	±2.5	mV
✓	Offset Voltage T_C[3]	±5				±25		±25	μV/°C
✓	Input Bias Current								
	Inverting	±5	±56	±15	±35	±56	±15	±35	μA
	Noninverting	±15	±75	±50	±62	±75	±50	±62	μA
✓	Input Bias Current T_C[3]								
	Inverting	±70				±330		±330	nA/°C
	Noninverting	±30				±200		±200	nA/°C
#	Noninverting								
	Impedance	200k							Ω
	Capacitance	2							pF
#	Common-Mode Input	±5	±5	±5	±5	±5	±5	±5	V
✓	Internal Feedback Resistor (R_F)	1500		1490/ 1510			1490/ 1510		Ω
#	R_F Temperature Coefficient		±25		±25	±25		±25	ppm/°C
✓	Common-Mode Rejection Ratio (CMRR)[4]	>50	≥35	≥35	≥35	≥35	≥35	≥35	dB
	CMRR ($R_F = 1500\Omega$; $R_{IN} = 150\Omega$; $\Delta V_S = 5V$)	>60							dB
✓	Common-Mode Sensitivity (CMS),[5]								
	Referred to Input ($\Delta V_S = 5V$)								
	−CMS	3	8	8	8	8	8	8	μA/V
	+CMS	3	8	8	8	8	8	8	μA/V
	$CMS_{VOLTAGE}$	62	≥50	≥50	≥50	≥50	≥50	≥50	dB
#	Output Impedance (dc to 100kHz)	0.05							Ω
✓	Output Voltage Swing ($R_{LOAD} = 200\Omega$)	±10	≥±9	≥±9	≥±9	≥±9	≥±9	≥±9	V
#	Output Current (Continuous)	±50	≥±50	≥±50	≥±50	≥±50	≥±50	≥±50	mA
✓	Open Loop Transimpedance Gain (200Ω Load)	>1.5	≥0.7	≥0.9	≥0.7	≥0.7	≥0.9	≥0.7	MΩ
✓	Supply Current[6]	21	≤27	≤25	≤27	≤27	≤25	≤27	mA
	Power Consumption[6]	630	≤810	≤750	≤810	≤810	≤750	≤810	mW
✓	Power Supply Rejection Ratio (PSRR)[4]	>50	≥35	≥35	≥35	≥35	≥35	≥35	dB
	PSRR ($R_F = 1500\Omega$; $R_{IN} = 150\Omega$; $\Delta V_S = 10V$)	>60							dB
✓	Power Supply Sensitivity (PSS),[7]								
	Referred to Input ($\Delta V_S = 10V$)								
	$PSS_{VOLTAGE}$	65	50	50	50	50	50	50	dB
	−PSS	3	8	8	8	8	8	8	μA/V
	+PSS	3	8	8	8	8	8	8	μA/V

AC ELECTRICAL CHARACTERISTICS ($\pm V = \pm 15V$; $A_V = -10$; $R_{IN} = 150\Omega$; $R_F = 1.5k\Omega$; $R_{LOAD} = 200\Omega$)

	Bandwidth (−3dB) (V_{OUT} = 100mV p-p)								
✓	G = −10	>100	≥80	≥80	≥80	≥80	≥80	≥80	MHz
	Amplitude of Peaking:								
✓	DC to 60MHz	0	≤0.4	≤0.2	≤1.0	≤0.4	≤0.2	≤1.0	dB
#	>60MHz	0	≤0.6	≤0.3	≤1.8	≤0.6	≤0.3	≤1.8	dB
#	Phase Nonlinearity (dc to 45MHz)	1							°
#	Rise (Fall) Time (V_{OUT} = 5V Step)	<3.5	≤4	≤4	≤4.3	≤4	≤4	≤4.3	ns
#	Slew Rate (V_{OUT} = 18V Step)	>3.5	≥3	≥3	≥2.4	≥3	≥3	≥2.4	kV/μs
#	Settling Time to 0.1% (G = −10; 5V Output Step)	18	≤29	≤25	≤29	≤29	≤25	≤29	ns
#	Settling Time to 0.02% (G = −10; 5V Output Step)	30							ns
#	Overshoot Amplitude (V_{OUT} = 5V Output Step)	<4	≤14	≤8	≤18	≤14	≤8	≤18	%
#	Propagation Delay	3.3	≤4.0	≤4.0	≤4.0	≤4.0	≤4.0	≤4.0	ns
✓	Total Harmonic Distortion (Freq. = 20 MHz; Output Voltage = 2V p-p)	55	50	50	50	50	50	50	dB
#	Input Noise ($R_{LOAD} = 100\Omega$)								
	Voltage (5MHz to 150MHz)	0.7	≤1.2	≤1.5	≤2.0	≤1.2	≤1.5	≤2.0	nV/√Hz
	Current (5MHz to 150MHz)	23	≤29	≤30	≤35	≤29	≤30	≤35	pA/√Hz

Parameter	Sub-Group	AD9610BH/TH Typical @ +25°C	AD9610BH Min/Max @ −25°C	AD9610BH Min/Max @ +25°C	AD9610BH Min/Max @ +85°C	AD9610TH Min/Max @ −55°C	AD9610TH Min/Max @ +25°C	AD9610TH Min/Max @ +125°C	Units
OTHER INFORMATION									
Case to Ambient, θ_{CA}[8] (Still Air; No Heat Sink)		65	*	*	*	*	*	*	°C/W
Case to Ambient, θ_{CA}[8] (500 LFPM Air; No Heat Sink)		38	*	*	*	*	*	*	°C/W
MTBF[9]		$\geq 1.48 \times 10^6$	*	*	*	*	*	*	hours

NOTES
√ 100% tested (See Notes 1 and 2).
Specifications guaranteed by design; not tested.
*Specification same as AD9610BH/TH typical specification.
[1]AD9610BH parameters preceded by a check (√) are tested at +25°C ambient temperature; performance is guaranteed over the industrial temperature range (−25°C to +85°C) case temperature.
[2]AD9610TH parameters preceded by a check (√) are tested at −55°C case, +25°C ambient, and +125°C case temperatures. Mil-processed versions are available.
[3]Offset voltage T_C and bias current T_C are guaranteed over the respective temperature ranges.
[4]CMRR and PSRR apply only for stated conditions.
[5]CMS values can be used to determine the CMRR for specific gain settings according to the following worst case relationships:



$$\Delta V_{OUT} = [-CMS]\,[R_F]\,[\Delta V_{SUPPLY}] + [+CMS]\,[R2]\left[1+\frac{R_F}{R1}\right][\Delta V_{SUPPLY}] + [CMS_{VOLT}]\left[1+\frac{R_F}{R1}\right][\Delta V_{SUPPLY}]$$

$$\text{WHERE } \Delta V_{SUPPLY} = \Delta -V_{SUPPLY} \text{ AND } \Delta +V_{SUPPLY}$$

$$CMRR = -20\,LOG\left[\left(\frac{\Delta V_{OUT}}{1+\frac{R_F}{R1}\times \Delta V_{SUPPLY}}\right)\right]$$

[6]Supply current and power dissipation numbers are for quiescent operation (input is grounded). Values increase with higher frequency operation.
[7]PSS values can be used to determine the PSRR for specific gain settings according to the following worst case relationships (See diagram in 5 above):

$$\Delta V_{OUT} = [-PSS]\,[R_F]\,[\Delta V_{SUPPLY}] + [+PSS]\,[R2]\left[1+\frac{R_F}{R1}\right][\Delta V_{SUPPLY}] + [PSS_{VOLT}]\left[1+\frac{R_F}{R1}\right][\Delta V_{SUPPLY}]$$

$$\text{WHERE } \Delta V_{SUPPLY} = \Delta -V_{SUPPLY} \text{ OR } \Delta +V_{SUPPLY}$$

$$PSRR = -20\,LOG\left[\left(\frac{\Delta V_{OUT}}{1+\frac{R_F}{R1}\times \Delta V_{SUPPLY}}\right)\right]$$

[8]Recommended maximum junction temperature is +165°C. See Thermal Model.
[9]MTBF calculated using MIL-HNBK 217D; Ground Fixed; Temperature (case) = +70°C.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

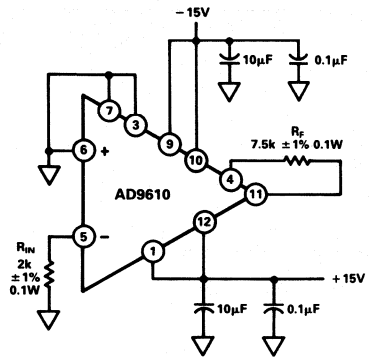
Supply Voltages ($\pm V_S$) . . . . . ±18V
Operating Temperature Range (case)
AD9610BH . . . . . −25°C to +85°C
AD9610TH/TH/883B . . . . . −55°C to +125°C
Power Dissipation . . . . . See Thermal Model
Junction Temperature . . . . . +165°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (soldering, 10 sec) . . . . . +300°C

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD9610BH	−25°C to +85°C	TO-8 Style Metal Can	H-12A
AD9610TH	−55°C to +125°C	TO-8 Style Metal Can	H-12A
AD9610TH/883B	−55°C to +125°C	TO-8 Style Metal Can	H-12A

*For outline information see Package Information section.

LIFE TEST/BURN-IN CIRCUIT



R_{IN} = RNC55H2001F
R_F = RN55C7501F
10µF = M39003101-2302
0.1µF = M39014101-1553

THIS MICROCIRCUIT IS COVERED BY TECHNOLOGY GROUP (I.) PER MIL-M-38510

THEORY OF OPERATION

The advantages of the transimpedance AD9610 Operational Amplifier become easier to understand when its operation is compared to the operation of conventional high-speed op amps.

The operation of the AD9610 Operational Amplifier is similar to a standard voltage-input differential amplifier in terms of setting gain and calculating noise. The primary difference between the two types is a low-impedance inverting input on the AD9610; this causes the unit to use current feedback, rather than voltage feedback, to achieve signal amplification.

Figure 1 and the discussion which follows help make a comparison between the AD9610 and "conventional" devices.

Two equations are necessary to describe the amplifier shown in Figure 1.

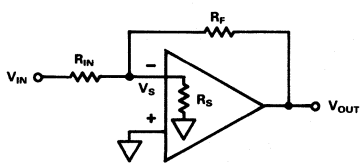


Figure 1.

One equation is a rudimentary amplifier transfer function:

$$-V_{OUT} = A(\omega)\, V_S \qquad \textit{(Equation A)}$$

and the other sums the currents at the inverting input:

$$\frac{V_S - V_{IN}}{R_{IN}} + \frac{V_S}{R_S} + \frac{V_S - V_{OUT}}{R_F} = 0 \qquad \textit{(Equation B)}$$

Rearranging and reducing Equation B; and substituting from Equation A results in a third equation:

$$\frac{V_{OUT}}{V_{IN}} = \frac{-A(\omega)R_SR_F/(R_SR_F + R_{IN}R_F + R_{IN}R_S)}{1 + A(\omega)R_{IN}R_S/(R_SR_F + R_{IN}R_F + R_{IN}R_S)} \qquad \textit{(Equation C)}$$

For purposes of discussion, assume the amplifier shown in Figure 1 exhibits a single-pole frequency response. When it does, $A(\omega) = A_O/(1 + j\omega\tau)$ where A_O = open loop gain; and $1/\tau$ = the roll-off frequency. When these terms are substituted into Equation C, the result is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{-A_OR_SR_F/(R_SR_F + R_{IN}R_F + R_{IN}R_S)}{1 + j\omega\tau + \left[A_OR_{IN}R_S/(R_SR_F + R_{IN}R_F + R_{IN}R_S)\right]}$$

Based on the idea that

$$1 + \left[A_OR_{IN}R_S/(R_SR_F + R_{IN}R_F + R_{IN}R_S)\right]$$

is approximately equal to

$$A_OR_{IN}R_S/(R_SR_F + R_{IN}R_F + R_{IN}R_S)$$

and G (closed loop gain) = R_F/R_{IN}, it becomes possible to simplify and substitute terms in the above equation to obtain:

$$\frac{V_{OUT}}{V_{IN}} = \frac{-G}{1 + \frac{j\omega\tau R_F}{A_O}\left[\frac{1}{R_{IN}} + \frac{1}{R_S} + \frac{1}{R_F}\right]}$$

The fundamental difference between the AD9610 and traditional amplifiers becomes apparent at this point.

In traditional voltage-imput amplifiers, the input resistance (R_S) approaches infinity. Consequently, $1/R_S$ approaches zero; and the term $R_F\,(1/R_{IN} + 1/R_S + 1/R_F)$ simplifies to the term $R_F\,(1/R_{IN} + 1/R_F)$. The latter can be reduced further to (G + 1). When substitutions are made, the gain/frequency relationship for a traditional amplifier design is expressed as:

$$\frac{V_{OUT}}{V_{IN}} = \frac{-G}{1 + \frac{j\omega\tau}{A_O}[G+1]}$$

There is a dramatically different result for the AD9610.

This difference is because the value of R_S in the transimpedance amplifier is only 20Ω. This is important when one realizes $R_S \parallel R_{IN} \parallel R_F$; and $R_S << R_{IN}$ and/or R_F. In this case, $(1/R_S + 1/R_{IN} + 1/R_F) \approx 1/R_S$. Substituting terms, a direct comparison with traditional amplifer relationships can be made:

$$\frac{V_{OUT}}{V_{IN}} = \frac{-G}{1 + \frac{j\omega\tau}{A_O}\left[\frac{R_F}{R_S}\right]}$$

Both amplifier types yield similar algebraic results, but there is one critical difference in how they are obtained.

As shown above, the closed loop gain (G) of the traditional amplifier is multiplied by the frequency-dependent term of the denominator; **this means increasing frequencies or closed loop gain accelerates the gain roll-off.**

In the AD9610, however, the constant R_F/R_S is multiplied by the frequency-dependent term; **this means bandwidth remains relatively constant for any given value of gain.**

Inside the AD9610, the design includes a 1.5kΩ feedback resistor to help reduce the effect of stray capacitances and make it easier to apply the amplifier. This internal R_F means *the gain of the AD9610 is set by varying R_{IN}.*

The differences in the architecture of the AD9610 vis-a-vis a traditional op amp cause its closed-loop frequency response to be considerably different from conventional units.

Figure 2 pictures a typical plot for a traditional single-pole amplifier.

As shown, increasing the closed loop gain of a traditional op amp decreases the bandwidth of the amplifier; the precise amount of change will be determined by the actual roll-off characteristics of the op amp.

By contrast, the frequency response of the AD9610 changes very little when the gain is changed. Refer to Figure 3.

Variations in gain (established by varying values of R_{IN}) have only a negligible effect on the bandwidth of the amplifier.

(NOTE: For a more complete explanation of the mathematics involved in comparing conventional op amps and the AD9610, refer to the Analog Devices application note entitled "Using the AD9610 Transimpedance Amplifier.")

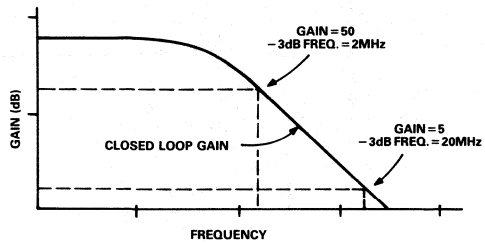


Figure 2.

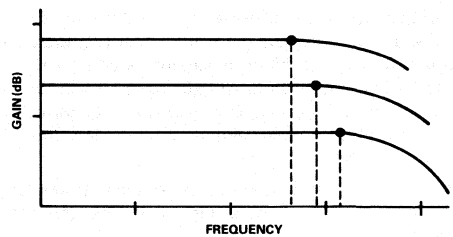


Figure 3.

AD9610 FUNCTIONAL DESCRIPTION

Refer to Figure 4, AD9610 Functional Circuit.

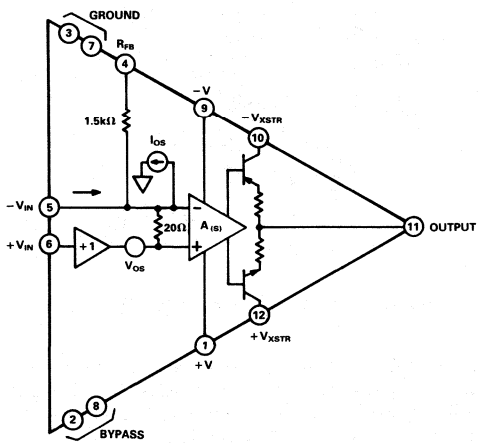


Figure 4. AD9610 Functional Circuit

The most prominent characteristic illustrated in this model of the unit is the combination of a high-impedance noninverting terminal and a low-impedance inverting terminal. This is achieved by buffering the noninverting terminal to create a high-impedance input; while maintaining a low impedance through the 20Ω characteristic of the inverting input.

Because of the low input impedance of the inverting input, all of the input signal voltage is impressed across the input resistor (R_{IN} in Figure 6); this causes a direct voltage-to-current conversion to take place.

Conventional op amps use a volts/volts transfer function, while the transfer function of the AD9610 is volts/μA (or resistance).

Signal current flowing in the inverting terminal (Pin 5) will flow through the 20Ω resistor. The voltage developed across this input impedance becomes the input signal for the internal amplifier.

As a result of this action, the input current is converted to an output voltage; this is the reason for the open loop transfer function being expressed in ohms.

To compensate for variations in offset voltage and current in the AD9610, both a voltage source and a current source are included in the unit. Input offset voltage (V_{OS}) is a dc error which appears at the output as $[V_{OS}\ (1+R_F/R_{IN})]$. In a similar fashion, the input bias current (I_{OS}) reflects as a dc error which appears at the output as $[I_{OS}\ (R_F)]$.

The current source connected to the inverting terminal effectively models the input offset current; and although bias currents flow in both terminals, the inverting input bias current is dominant. The combined actions of the internal voltage and current sources effectively compensate for discrepancies in offset voltage and current.

Power supply voltages applied to the AD9610 are separated, with one set of terminals designated for the output transistors (Pins 10 and 12) and another set for the internal amplifier (Pins 1 and 9). This splitting of the voltages makes it possible to limit voltage swings and current at the output, and helps regulate the junction temperatures of the output transistors.

APPLYING THE AD9610 OP AMP

In applying the AD9610 op amp, there are certain precautions which **must** be observed to protect the unit from damage:

1. Shorting either power supply input pin (Pin 10 or Pin 12) to the output (Pin 11) will destroy the device.
2. Shorting the output (Pin 11) to ground will destroy the device; no internal protection is provided.

As explained earlier, the noninverting input of the AD9610 Operational Amplifier is a high impedance. This requires that it be driven from a low-impedance source, or connected to ground. Driving this input from a high impedance detracts from the wide bandwidth performance; connecting it to ground avoids the possibility of closed-loop ac peaking.

Because the internal biasing network of the AD9610 is connected to the +V and −V supply pins, it is important that these pins have adequate decoupling. Nominal supply voltages for the AD9610 are ±15V, but this can be reduced to a lower limit of ±12V without serious degradation of high-speed performance. When ±12V supplies are used, output voltage swings from the amplifier must be reduced.

Bypass Pins 2 and 8 should be decoupled to ground through 33 – 50Ω resistors and 0.1μF capacitors to maintain stability on the bias network.

Feedback resistor R_F is internal to the AD9610 and has been precisely adjusted to allow the widest possible range of operating conditions. While it is possible to use an external feedback resistor for the device, the user is urged to avoid the temptation to "tune" performance with this technique because it will inevitably detract from ac performance.

A massive low-impedance ground plane is essential for optimum performance from the AD9610 because it provides a moderate level of shielding and helps reduce the effects of distributed capacitance.

But the benefits of a large ground plane can be diminished if components are grounded at multiple points on the ground plane. Single-point grounding is *always* preferred for high-speed circuits to avoid the possibility of voltage differentials which might result from multiple grounds.

The best high-frequency performance is obtained from the AD9610 when total output capacitance is minimized. Realistically, this is not always possible; but performance can be improved with a 5 – 30Ω resistor in series with the output as shown in Figure 5.

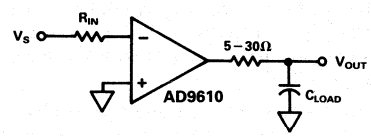


Figure 5.

Isolation provided by the series resistor makes it possible for the AD9610 to drive loads well outside its design limits, but at some loss of speed. Isolating the capacitive load from the output of the amplifier is particularly useful when driving flash A/D converters.

The power supplies for the AD9610 must be decoupled effectively to obtain maximum performance from the device. Recommended choices are a 0.1μF ceramic capacitor and a 10μF tantalum capacitor in parallel on each supply. These connections show up in Figures 6 and 7 which illustrate the connections for inverting and noninvertering operation, respectively. Decoupling components should always be connected as closely as possible to the amplifier's voltage supply pins.

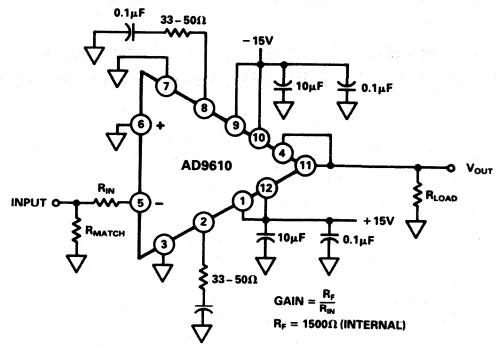


Figure 6. AD9610 Inverting Operation

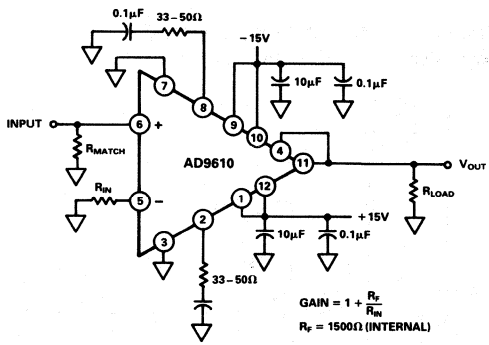


Figure 7. AD9610 Noninverting Operation

If the expected output voltage swings are small, it is possible to operate the ouput stages from ±5V supplies; this will reduce power dissipation and junction temperatures on the output transistors. For this, the ±5V and ±15V supplies must be decoupled separately.

As shown in Figures 6 and 7, bypass Pins 2 and 8 should be decoupled individually with a 33 – 50Ω resistor and 0.1μF capacitor in series to ground. Without this decoupling, power supply and common-mode rejection ratios (PSRR and CMRR) may be degraded. In some applications, the lack of this decoupling may show up as very high-frequency "ringing" on the output. R_{MATCH} in Figures 6 and 7 is used to match the output impedance of the driving source.

AD9610 POWER DISSIPATION

Quiescent power supply currents for the AD9610 are ±21mA. Supply currents this low allow the unit to be operated over a wide temperature range without damage. For high-temperature operation and long-term stability, however, the user is urged to use a heat sink. Two acceptable models for TO-8 packages are the Thermalloy 2240 and the IERC Up-TO8-48CB.

Refer to Figure 8.

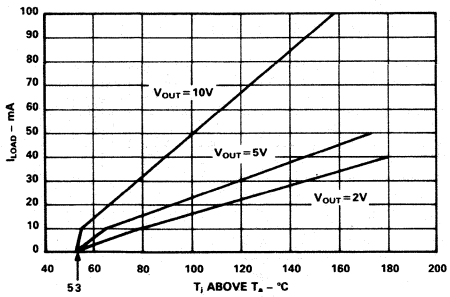
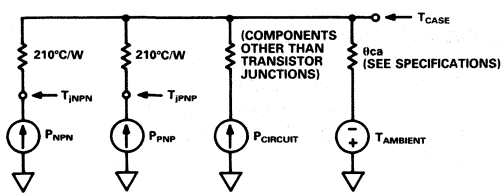


Figure 8. Junction Temp. Rise vs. Load Current

The data in this illustration are typical characteristics when the AD9610 is operated from ±15V supplies. Assume the desired output from the op amp is ±10V swings at ±50mA currents. For this combination, maximum junction temperature will be 100°C above the ambient temperature.

Since maximum allowable junction temperature is +165°C, the maximum ambient temperature which can be tolerated is +65°C. If there is a possibility the ambient may exceed this limit, heat sinking and/or heat removal is required. Additional details on the thermal characteristics of the unit are included in the AD9610 Thermal Model. *(For more information on thermal protection, consult the Analog Devices application note "Using the AD9610 Transimpedance Amplifier".)*



$P_{CIRCUIT} = I_{CC}[+V_{CC} - (-V_{CC})]$ WHERE I_{CC} = 21mA @ ±15V

$P_{XXX} = [(\pm V_{CC}) - V_{OUT} - I_{COL}(8)]$ (I_{COL}) (% DUTY CYCLE)

NOTE: XXX = NPN OR PNP

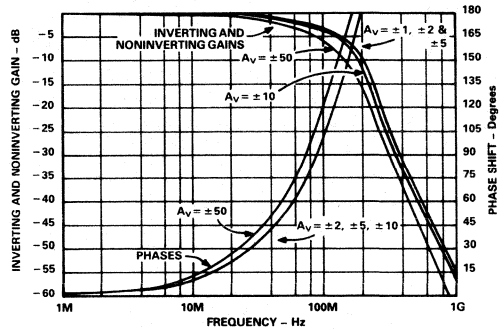
(FOR POSITIVE V_{OUT} AND V_{CC}, THIS IS POWER IN NPN OUTPUT STAGE: FOR NEGATIVE V_{OUT} AND V_{CC}, THIS IS POWER IN PNP OUTPUT STAGE. $I_{COL} = V_{OUT}/R_{LOAD}$ or 3.0mA, WHICHEVER IS GREATER. FEEDBACK RESISTOR R_F IS INCLUDED IN R_{LOAD}.)

$T_{J(PNP)} = P_{PNP}$ (210 + θca) + ($P_{CIRCUIT}$ + P_{NPN}) (θ ca) + T_a. SIMILAR FOR $T_{J(NPN)}$

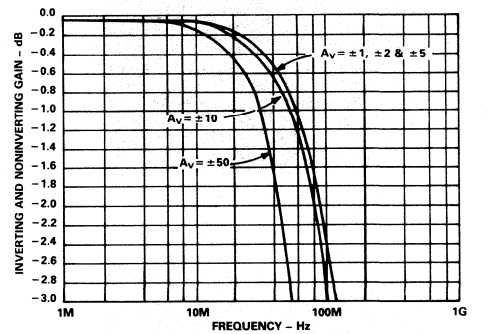
AD9610 Thermal Model

AD9610 PERFORMANCE

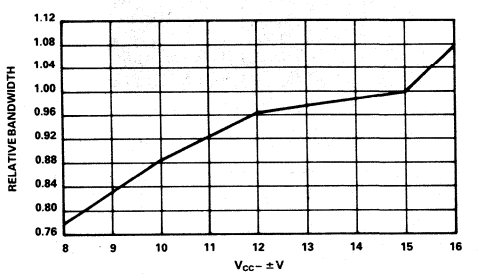
In the following section, graphs and photographs depict typical performance of the AD9610 for various characteristics.



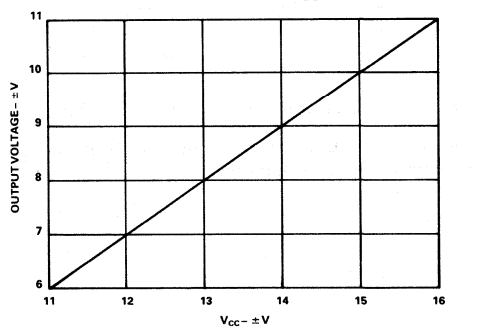
AD9610 Frequency Response (A_V = ±1, ±2, ±5, ±10, ±50)



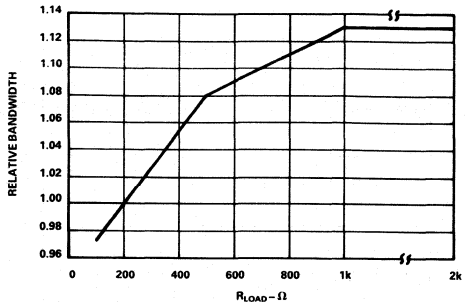
AD9610 Frequency Response (A_V = ±1, ±2, ±5, ±10, ±50)



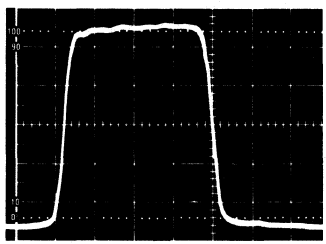
Bandwidth vs. V_{CC}



Output Voltage vs. V_{CC}

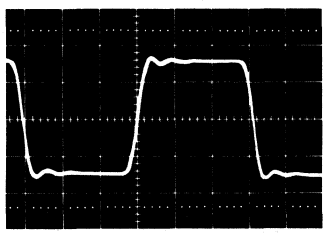


Bandwidth vs. Load



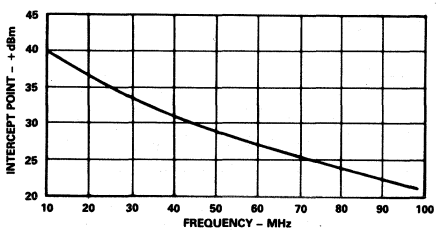
GAIN = –10; 136mV/DIV; 10ns/DIV

AD9610 Small-Signal Pulse Response



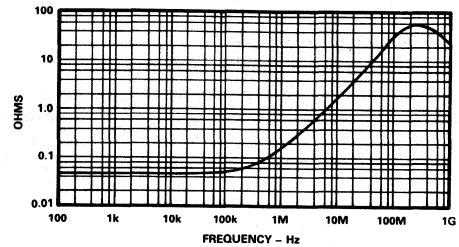
GAIN = –10; 3.4V/DIV; 10ns/DIV

AD9610 Large-Signal Pulse Response

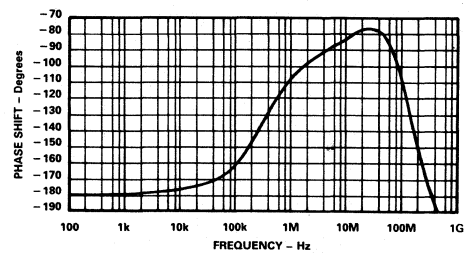


Two-Tone, 3rd Order IMD Intercept (G = –5; R_L = 50Ω)

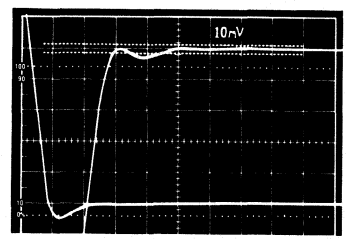
Information in graphs above can be used to obtain effective output impedance versus frequency.



Small-Signal Output Resistance vs. Frequency (G = –10)



Small-Signal Output Phase Shift vs. Frequency (G = –10)



GAIN = –10; 5V OUTPUT; ERROR WINDOW (±5mV) = 0.1%; 5ns/DIV

AD9610 Settling Time

ORDERING INFORMATION

The AD9610BH is specified for operation over a case temperature range of –25°C to +85°C; the AD9610TH is intended for applications in which case temperature may be between –55°C and +125°C. The AD9610TH/883B is processed per MIL-STD-883B.

ANALOG DEVICES

Low Distortion, Precision, Wide Bandwidth Op Amp

AD9617*

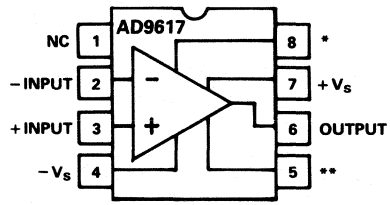
FEATURES

Usable Closed-Loop Gain Range: ±1 to ±40
Low Distortion: −67 dBc (2nd) at 20 MHz
Small Signal Bandwidth: 190 MHz (A_V = +3)
Large Signal Bandwidth: 150 MHz at 4 V p-p
Settling Time: 10 ns to 0.1%; 14 ns to 0.02%
Overdrive and Output Short Circuit Protected
Fast Overdrive Recovery
DC Nonlinearity 10 ppm

APPLICATIONS

Driving Flash Converters
D/A Current-to-Voltage Converters
IF, Radar Processors
Baseband and Video Communications
Photodiode, CCD Preamps

PIN CONFIGURATION



*OPTIONAL $+V_S$ **OPTIONAL $-V_S$

NOTE: FOR BEST SETTLING TIME AND DISTORTION PERFORMANCE, USE OPTIONAL SUPPLY CONNECTIONS. PERFORMANCE INDICATED IN SPECIFICATIONS IS BASED ON SUPPLY CONNECTIONS TO THESE PINS.

GENERAL DESCRIPTION

The AD9617 is a current feedback amplifier which utilizes a proprietary architecture to produce superior distortion and dc precision. It achieves this along with fast settling, very fast slew rate, wide bandwidth (both small signal and large signal) and exceptional signal fidelity. The device achieves −67 dBc 2nd harmonic distortion at 20 MHz while maintaining 190 MHz small signal and 150 MHz large signal bandwidths.

These attributes position the AD9617 as an ideal choice for driving flash ADCs and buffering the latest generation of DACs. Optimized for applications requiring gain between ±1 to ±15, the AD9617 is unity gain stable without external compensation.

Additional benefits of the AD9617B and T grades include input offset voltage of 500 μV and temperature coefficient (TC) of 3 μV/°C. These accuracy performance levels make the AD9617 an excellent choice for driving emerging high resolution (12–16 bits), high speed analog-to-digital converters and flash converters.

The AD9617 offers outstanding performance in high fidelity, wide bandwidth applications in instrumentation ranging from network and spectrum analyzers to oscilloscopes and in military systems such as radar, SIGINT, and ESM systems. The superior slew rate, low overshoot and fast settling of the AD9617 allow the device to be used in pulse applications such as communications receivers and high speed ATE. Most monolithic op amps suffer in these precision pulse applications due to slew rate limiting.

The AD9617J operates over the range of 0 to +70°C and is available in either an 8-pin plastic mini-DIP or an 8-lead plastic small outline package (SOIC). The AD9617A and B versions are rated over the industrial temperature range of −40°C to +85°C. The AD9617S and T versions are rated over the military temperature range of −55°C to +125°C and are available processed to MIL-STD-883B.

*Patent pending.

AD9617—SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltages ($\pm V_S$) . . . . . ±7 V
Common Mode Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . 3 V
Continuous Output Current[2] . . . . . 70 mA
Operating Temperature Ranges
AD9617JN/JR . . . . . 0 to +70°C
AD9617AQ/BQ . . . . . −40°C to +85°C
AD9617SQ/TQ . . . . . −55°C to +125°C
Storage Temperature
AD9617JN/JR . . . . . −65°C to +125°C
AD9617AQ/BQ/SQ/TQ . . . . . −65°C to +150°C
Junction Temperature[3]
AD9617JN/JR . . . . . +150°C
AD9617AQ/BQ/SQ/TQ . . . . . +175°C
Lead Soldering Temperature (10 Seconds) . . . . . +300°C

DC ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $A_V = +3$; $\pm V_S = \pm 5$ V; $R_F = 400\ \Omega$; $R_{LOAD} = 100\ \Omega$)

Parameter	Conditions	Temp	Test Level	AD9617JN/JR Min	AD9617JN/JR Typ	AD9617JN/JR Max	AD9617AQ/SQ Min	AD9617AQ/SQ Typ	AD9617AQ/SQ Max	AD9617BQ/TQ Min	AD9617BQ/TQ Typ	AD9617BQ/TQ Max	Units
Input Offset Voltage[4, 5]		+25°C	I	−1.1	+0.5	+2.2	−1.1	+0.5	+2.2	+0.0	+0.5	+1.1	mV
Input Offset Voltage TC[5]		Full	IV	−4	+3	+25	−4	+3	+25	−4	+3	+25	µV/°C
Input Bias Current[5]													
Inverting		+25°C	I	−50	0	+50	−50	0	+50	−25	0	+25	µA
Noninverting		+25°C	I	−25	+5	+35	−25	+5	+35	−15	+5	+20	µA
Input Bias Current TC[5]													
Noninverting		Full	IV	−50	+30	+125	−50	+30	+125	−50	+30	+125	nA/°C
Inverting		Full	IV	−50	+50	+150	−50	+50	+150	−50	+50	+150	nA/°C
Input Resistance													
Noninverting		+25°C	V		60			60			60		kΩ
Input Capacitance													
Noninverting		+25°C	V		1.5			1.5			1.5		pF
Common-Mode Input Range[6]	$T = T_{max}$	←	II	±1.4	±1.5		±1.4	±1.5		±1.4	±1.5		V
	$T = T_{min}$ to +25°C	←	II	±1.7	±1.8		±1.7	±1.8		±1.7	±1.8		V
Common-Mode Rejection Ratio[7]	$T = T_{max}$	←	II	44	48		44	48		44	48		dB
	$T = T_{min}$ to +25°C	←	II	50	53		50	53		50	53		dB
Power Supply Rejection Ratio	$\Delta V_S = \pm 5\%$	Full	II	50	60		50	60		50	60		dB
Open Loop Gain													
T_O	At dc	+25°C	V		500			500			500		kΩ
Nonlinearity	At dc	+25°C	IV		10			10			10		ppm
Output Voltage Range		+25°C	II	±3.4	±3.8		±3.4	±3.8		±3.4	±3.8		V
Output Impedance	At dc	+25°C	V		0.07			0.07			0.07		Ω
Output Current (50 Ω Load)	$T = +25°C$ to T_{max}	←	II	60			60			60			mA
	$T = T_{min}$	←	II	50			50			50			mA

AC ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $A_V = +3$; $\pm V_S = \pm 5$ V; $R_F = 400\ \Omega$; $R_{LOAD} = 100\ \Omega$)

Parameter	Conditions	Temp	Test Level	AD9617JN/JR Min	AD9617JN/JR Typ	AD9617JN/JR Max	AD9617AQ/SQ Min	AD9617AQ/SQ Typ	AD9617AQ/SQ Max	AD9617BQ/TQ Min	AD9617BQ/TQ Typ	AD9617BQ/TQ Max	Units
FREQUENCY DOMAIN													
Bandwidth (−3 dB)													
Small Signal	$V_{OUT} \leq 2$ V p-p	Full	II	145	190		145	190		145	190		MHz
Large Signal	$V_{OUT} = 4$ V p-p	Full	IV		150		115	150		115	150		MHz
Bandwidth Variation vs. A_V	$A_V = -1$ to ±15	+25°C	V		40			40			40		MHz
Amplitude of Peaking (<50 MHz)	$T = T_{min}$ to +25°C	←	II		0			0	0.3		0	0.3	dB
	$T = T_{max}$	←	II		0			0	0.6		0	0.6	dB
Amplitude of Peaking (>50 MHz)	$T = T_{min}$ to +25°C	←	II		0			0	0.8		0	0.8	dB
	$T = T_{max}$	←	II		0			0	1.0		0	1.0	dB
Amplitude of Roll-Off (<75 MHz)		Full	II		0.1			0.1	0.6		0.1	0.6	dB
Phase Nonlinearity	dc to 75 MHz	+25°C	V		0.5			0.5			0.5		Degree
2nd Harmonic Distortion	2 V p-p; 4.3 MHz	Full	IV		−86	−78		−86	−78		−86	−78	dBc
	2 V p-p; 20 MHz	Full	IV		−67	−59		−67	−59		−67	−59	dBc
	2 V p-p; 60 MHz	Full	II		−51	−43		−51	−43		−51	−43	dBc
3rd Harmonic Distortion	2 V p-p; 4.3 MHz	Full	IV		−83	−75		−83	−75		−83	−75	dBc
	2 V p-p; 20 MHz	Full	IV		−69	−61		−69	−61		−69	−61	dBc
	2 V p-p; 60 MHz	Full	II		−54	−46		−54	−46		−54	−46	dBc
Input Noise Voltage	10 MHz	+25°C	V		1.2			1.2			1.2		nV/√(Hz)
Inverting-Input Noise Current	10 MHz	+25°C	V		29			29			29		pA/√(Hz)
Average Equivalent Integrated Input Noise Voltage	0.1 to 200 MHz	+25°C	V		55			55			55		µV, rms

Parameter	Conditions	Temp	Test Level	AD9617JN/JR Min	AD9617JN/JR Typ	AD9617JN/JR Max	AD9617AQ/SQ Min	AD9617AQ/SQ Typ	AD9617AQ/SQ Max	AD9617BQ/TQ Min	AD9617BQ/TQ Typ	AD9617BQ/TQ Max	Units
TIME DOMAIN													
Slew Rate	V_{OUT} = 4 V Step	Full	IV		1400		1100	1400		1100	1400		V/μs
Rise/Fall Time													
V_{OUT} = 2 V Step		Full	IV		2.0			2.0	2.5		2.0	2.5	ns
V_{OUT} = 4 V Step	T = +25°C to T_{max}	←	IV		2.4			2.4	3.3		2.4	3.3	ns
V_{OUT} = 4 V Step	T = T_{min}	←	IV		2.4			2.4	3.5		2.4	3.5	ns
Overshoot	V_{OUT} = 2 V Step	Full	IV		3			3	14		3	14	%
Settling Time													
To 0.1%	V_{OUT} = 2 V Step	Full	IV		10			10	15		10	15	ns
To 0.02%	V_{OUT} = 2 V Step	Full	IV		14			14	23		14	23	ns
To 0.1%	V_{OUT} = 4 V Step	Full	IV		11			11	16		11	16	ns
To 0.02%	V_{OUT} = 4 V Step	Full	IV		16			16	24		16	24	ns
2×Overdrive Recovery to ±2 mV of Final Value	V_{IN} = 1.7 V Step	+25°C	V		50			50			50		ns
Propagation Delay		+25°C	V		2			2			2		ns
Differential Gain[8]		Full	V		<0.01			<0.01			<0.01		%
Differential Phase[8]		Full	V		0.01			0.01			0.01		Degree
POWER SUPPLY REQUIREMENTS													
Quiescent Current													
$+I_S$		Full	II		34	48		34	48		34	48	mA
$-I_S$		Full	II		34	48		34	48		34	48	mA

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Output is short circuit protected to ground, but not to supplies. Continuous short circuit to ground may affect device reliability.

[3]Typical thermal impedances (part soldered onto board):
Mini-DIP: θ_{JA} = 140°C/W; θ_{JC} = 30°C/W. Side Brazed/Cerdip: θ_{JA} = 110°C/W; θ_{JC} = 20°C/W. SOIC Package: θ_{JA} = 150°C/W; θ_{JC} = 30°C/W.

[4]Measured with respect to the inverting input.

[5]Typical is defined as the mean of the distribution.

[6]Measured in voltage follower configuration.

[7]Measured with V_{IN} = ±0.25 V.

[8]Frequency = 4.3 MHz; R_L = 150 Ω; A_V = +3.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

II – 100% production tested at +25°C and sample tested at specified temperatures. AC testing of J grade devices done on sample basis.

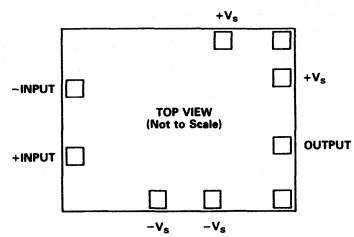
III – Sample tested only.

IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

Die Connections



DIE SIZE = 53 × 67 × 15 mils

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD9617JN	0 to +70°C	Plastic DIP	N-8
AD9617JR	0 to +70°C	SOIC	R-8
AD9617AQ	−40°C to +85°C	Cerdip	Q-8
AD9617BQ	−40°C to +85°C	Cerdip	Q-8
AD9617SQ	−55°C to +125°C	Cerdip	Q-8
AD9617TQ	−55°C to +125°C	Cerdip	Q-8

*For outline information see Package Information section.

THEORY OF OPERATION

The AD9617 has been designed to combine the key attributes of traditional "low frequency" precision amplifiers with exceptional high frequency characteristics that are independent of closed-loop gain. Previous "high frequency" closed-loop amplifiers have low open loop gain relative to precision amplifiers. This results in relatively poor dc nonlinearity and precision, as well as excessive high frequency distortion due to open loop gain roll-off.

Operational amplifiers use two basic types of feedback correction, each with advantages and disadvantages. Voltage feedback topologies exhibit an essentially constant gain bandwidth product. This forces the closed-loop bandwidth to vary inversely with closed-loop gain. Moreover, this type design typically slew rate limits in a way that causes the large signal bandwidth to be much lower than its small signal characteristics.

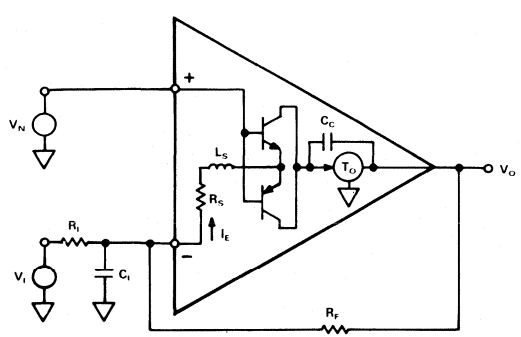
A newer approach is to use current feedback to realize better dynamic performance. This architecture provides two key attributes over voltage feedback configurations: (1) avoids slew rate limiting and therefore large signal bandwidth can approach small signal performance; and (2) low bandwidth variation versus gain settings, due to the inherently low open loop inverting input resistance (R_S).

The AD9617 uses a new current feedback topology that overcomes these limitations and combines the positive attributes of both current feedback and voltage feedback designs. These devices achieve excellent high frequency dynamics (slew, BW and distortion) along with excellent low frequency linearity and good dc precision.

DC GAIN CHARACTERISTICS

A simplified equivalent schematic is shown below. When operating the device in the inverting mode, the input signal error current (I_E) is amplified by the open loop transimpedance gain (T_O). The output signal generated is equal to $T_O \times I_E$. Negative feedback is applied through R_F such that the device operates at a gain (G) equal to $-R_F/R_I$.

Noninverting operation is similar, with the input signal applied to the high impedance buffer (noninverting) input. As before,



Equivalent Circuit

an output (buffer) error current (I_E) is generated at the low impedance inverting input. The signal generated at the output is fed back to the inverting input such that the external gain is $(1+R_F/R_I)$. The feedback mechanics are identical to the voltage feedback topology when exact equations are used.

The major difference lies in the front end architecture. A voltage feedback amplifier has symmetrical high resistance (buffered) inputs. A current feedback amplifier has a high noninverting resistance (buffered) input and a low inverting (buffer output) input resistance. The feedback mechanics can be easily developed using current feedback and transresistance open loop gain T(s) to describe the I/O relationship. (See typical specification chart.)

DC closed-loop gain for the AD9617 can be calculated using the following equations:

$$G = \frac{V_O}{V_I} \approx \frac{-R_F/R_I}{1 + 1/LG} \qquad \text{inverting} \qquad (1)$$

$$G = \frac{V_O}{V_N} \approx \frac{1 + R_F/R_I}{1 + 1/LG} \qquad \text{noninverting} \qquad (2)$$

$$\text{where: } \frac{1}{LG} \approx \frac{R_S(R_F + R_S \| R_I)}{T(s)(R_S \| R_I)} \qquad (3)$$

Because the noninverting input buffer is not ideal, input resistance R_S (at dc) is gain dependent and is typically higher for noninverting operation than for inverting operation. R_S will approach the same value (≈7 Ω) for both at input frequencies above 50 MHz. Below the open loop corner frequency, the noninverting R_S can be approximated as:

$$R_S \text{ (noninverting)} \approx 7 + \frac{T(s)}{A_O} = 7 + \left.\frac{T_O}{A_O}\right|_{dc} \qquad (4)$$

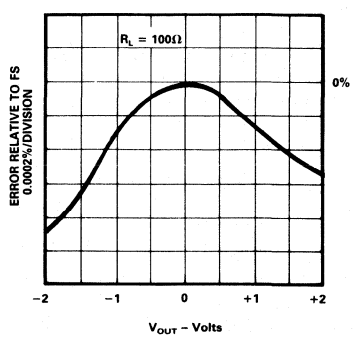
where: A_O = *Open Loop Voltage Gain* ≈ $G \times 600$

Inverting R_S below the open loop corner frequency can be approximated as:

$$R_S \text{ (inverting)} \approx 7 + \frac{T(s)}{A_O} = 7 + \left.\frac{T_O}{A_O}\right|_{dc} \qquad (5)$$

where: A_O = 40,000.

The AD9617 approaches this condition. With $T_O = 1 \times 10^6$ Ω, R_L = 500 Ω and R_S = 25 Ω (dc), a gain error no greater than 0.05% typically results for G = −1 and 0.15% for G = −40. Moreover, the architecture linearizes the open loop gain over its operating voltage range and temperature resulting in ≥16 bits of linearity.



DC Nonlinearity vs. V_{OUT}

AC GAIN CHARACTERISTICS

Closed-loop bandwidth at high frequencies is determined primarily by the roll-off of T(s). But circuit layout is critical to minimize external parasitics which can degrade performance by causing premature peaking and/or reduced bandwidth.

The inverting and noninverting dynamic characteristics are similar. When driving the noninverting input, the inverting input capacitance (C_I) will cause the noninverting closed-loop bandwidth to be higher than the inverting bandwidth for gains less than two (2). In the remaining cases, inverting and noninverting responses are nearly identical.

For best overall dynamic performance, the value of the feedback resistor (R_F) should be 400 ohms. Although bandwidth reduces as closed-loop gain increases, the change is relatively small due to low equivalent series input impedance, Z_S. (See typical performance charts.) The simplified equations governing the device's dynamic performance are shown below.

Closed-Loop Gain vs. Frequency:
(noninverting operation)

$$\frac{V_O}{V_S} \approx \frac{1 + \frac{R_F}{R_I}}{s\tau\left(1 + \frac{R_S}{R_I}\right) + 1} \qquad (6)$$

where: $\tau = R_F \times C_C = 0.9\ ns | R_F = 400\ \Omega$

$$Slew\ Rate \approx \frac{\Delta V_O}{R_F K C_C} \times e^{-\tau R_I K C_C} \qquad (7)$$

where: $K = 1 + \frac{R_S}{R_I}$

Increasing Bandwidth at Low Gains

By reducing R_F, wider bandwidth and faster pulse response can be attained beyond the specified values, although increased overshoot, settling time and possible ac peaking may result. As a rule of thumb, overshoot and bandwidth will increase by 1% and 8%, respectively, for a 5% reduction in R_F at gains of ±10. Lower gains will increase these sensitivities.

Equations 6 and 7 are simplified and do not accurately model the second order (open loop) frequency response term which is the primary contributor to overshoot, peaking and nonlinear bandwidth expansion. (See Open Loop Bode Plots.) The user should exercise caution when selecting R_F values much lower than 400 Ω. Note that a feedback resistor must be used in all situations, including those in which the amplifier is used in a noninverting unity gain configuration.

Increasing Bandwidth at High Gains

Closed loop bandwidth can be extended at high closed loop gain by reducing R_F. Bandwidth reduction is a result of the feedback current being split between R_S and R_I. As the gain increases (for a given R_F), more feedback current is shunted through R_I, which reduces closed loop bandwidth (see Equation 6). To maintain specified BW, the following equations can be used to approximate R_F and R_I for any gain from ±1 to ±15.

$$R_F = 424 \pm 8G \qquad (8)$$

(+ for inverting and − for noninverting)

$$R_I \approx \frac{424 - 8G}{G - 1} \quad \text{(noninverting)} \qquad (9)$$

$$R_I \approx \frac{424 + 8G}{G} \quad \text{(inverting)} \qquad (10)$$

G = *Closed Loop Gain.*

Bandwidth Reduction

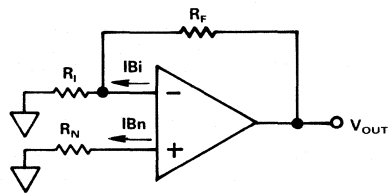
The closed loop bandwidth can be reduced by increasing R_F. Equations 6 and 7 can be used to determine the closed loop bandwidth for any value R_F. Do not connect a feedback capacitor across R_F, as this will degrade dynamic performance and possibly induce oscillation.

DC Precision and Noise

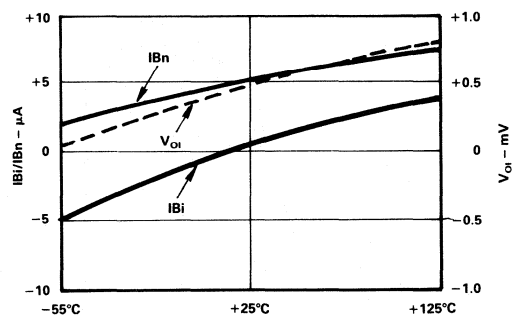
Output offset voltage results from both input bias currents and input offset voltage. These input errors are multiplied by the noise gain term ($1 + R_F/R_I$) and algebraically summed at the output as shown below.

$$V_O = V_{IO} \times \left(1 + \frac{R_F}{R_I}\right) \pm IBn \times R_N \times \left(1 + \frac{R_F}{R_I}\right) \pm IBi \times R_F \qquad (11)$$

Since the inputs are asymmetrical, IBi and IBn do not correlate. Canceling their output effects by making $R_N = R_F \| R_I$ will not reduce output offset errors, as it would for voltage feedback



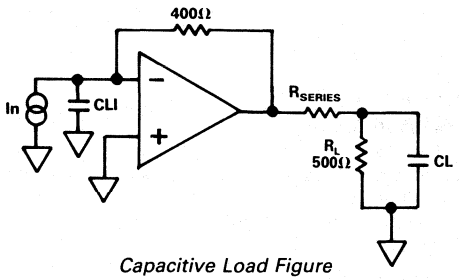
Output Offset Voltage



DC Accuracy

amplifiers. Typically, IBn is 5 µA and V_{IO} is +0.5 mV (1 sigma = 0.3 mV), which means that the dc output error can be reduced by making $R_N \approx 100\ \Omega$. Note that the offset drift will not change significantly because the IBn TC is relatively small. (See specification table.)

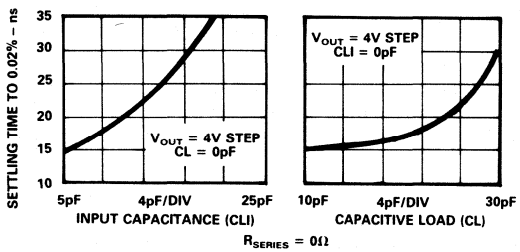
The effective noise at the output of the amplifier can be determined by taking the root sum of the squares of Equation 11 and applying the spectral noise values found in the typical graph section. This applies to noise from the op amp only. Note that both the noise figure and equivalent input offset voltages improve as the closed loop gain is increased (by keeping R_F fixed and reducing R_I with $R_N = 0\ \Omega$).



Capacitive Load Figure

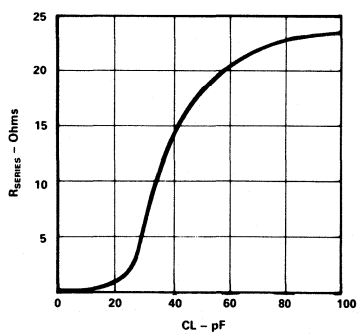
Capacitive Load Considerations

Due to the low inverting input resistance (R_S) and output buffer design, the AD9617 can directly handle input and/or output load capacitances of up to 20 pF. See the chart below.



Input/Output Capacitance Comparisons

A small series resistor can be used at the output of the amplifier and outside of the feedback loop to facilitate driving larger capacitive loads or for obtaining faster settling time. For capacitive loads above 20 pF, R_{SERIES} should be considered.



Recommended R_{SERIES} vs. CL

APPLYING THE AD9617

The superior frequency and time domain specifications of the AD9617 make it an obvious choice for driving flash converters and buffering the outputs of high speed DACs. Its outstanding distortion and noise performance make it well suited as a driver for analog to digital converters (ADCs) with resolutions as high as 16 bits.

Typical circuits for inverting and noninverting applications are shown in Figures 1 and 2.

Closed-loop gain for noninverting configurations is determined by the value of R_I according to the equation:

$$G = 1 + \frac{R_F}{R_I} \qquad (12)$$

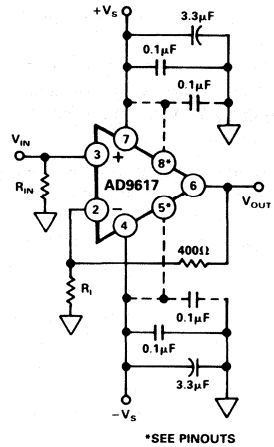


Figure 1. Noninverting Operation

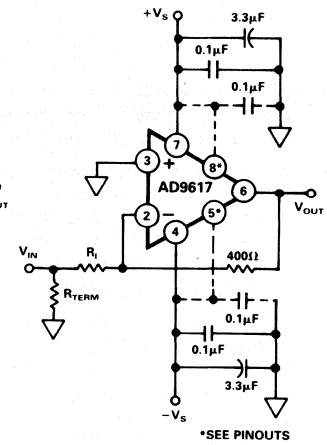


Figure 2. Inverting Operation

LAYOUT CONSIDERATIONS

As with all high performance amplifiers, printed circuit layout is critical in obtaining optimum results with the AD9617. The ground plane in the area of the amplifier should cover as much of the component side of the board as possible. Each power supply trace should be decoupled close to the package with at least a 3.3 µF tantalum and a low inductance, 0.1 µF ceramic capacitor.

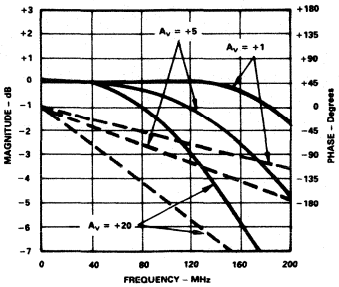
All lead lengths for input, output and the feedback resistor should be kept as short as possible. All gain setting resistors should be chosen for low values of parasitic capacitance and inductance, i.e., microwave resistors and/or carbon resistors.

Stripline techniques should be used for lead lengths in excess of one inch. Sockets should be avoided if possible because of their stray inductance and capacitance. If sockets are necessary, individual pin sockets such as AMP p/n 6–330808–3 should be used. These contribute far less stray reactance than molded socket assemblies.

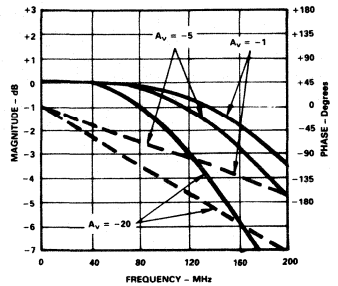
An evaluation board is available from Analog Devices at nominal cost.

*Consult factory regarding MIL-883 parts in "Z" packages.

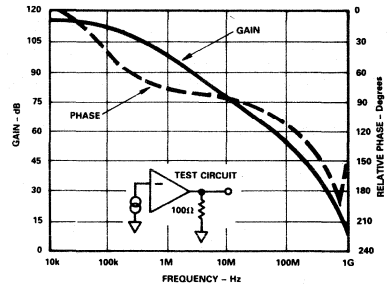
Typical Performance (A_V = +3; $\pm V_S$ = ±5 V; R_F = 400 Ω, unless otherwise noted)



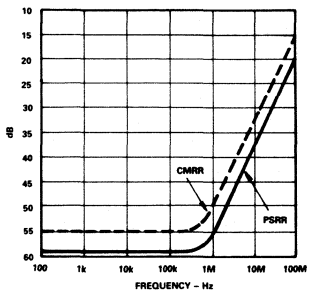
Noninverting Frequency Response



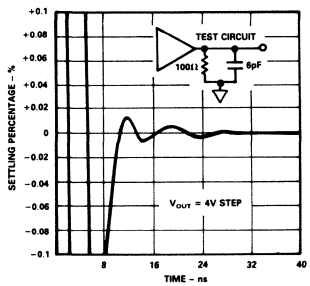
Inverting Frequency Response



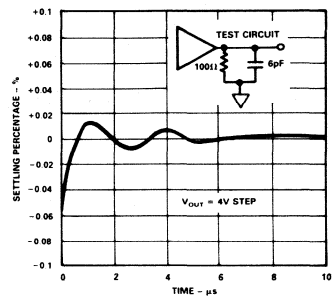
Open Loop Transimpedance Gain [T(s) Relative to 1Ω]



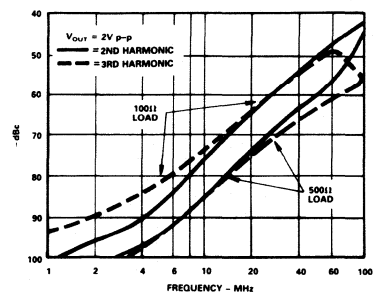
CMRR and PSRR



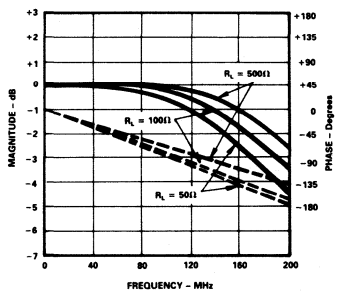
Settling Time



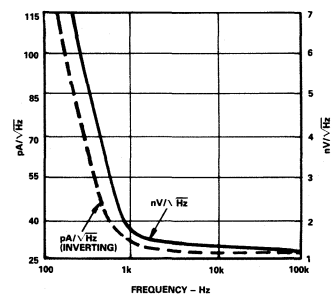
Long Term Settling Time



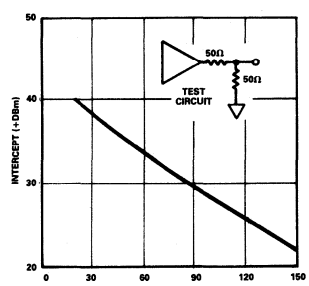
Harmonic Distortion



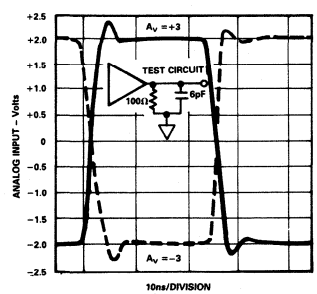
Frequency Response vs. R_{LOAD}



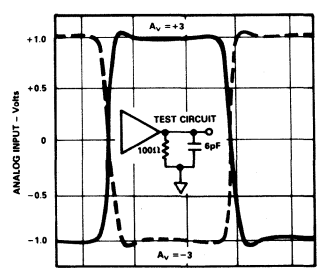
Equivalent Input Noise



Intermodulation Distortion (IMD)



Large Signal Pulse Response



Small Signal Pulse Response

ANALOG DEVICES

Low Distortion, Precision, Wide Bandwidth Op Amp

AD9618*

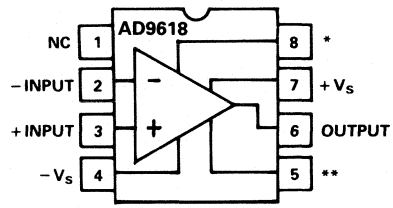
FEATURES

Usable Closed-Loop Gain Range: +5/−1 to ±100
Low Distortion: −63 dBc (2nd) at 20 MHz
Small Signal Bandwidth: 160 MHz (A_V = +10)
Large Signal Bandwidth: 150 MHz at 5 V p–p
Settling Time: 10 ns to 0.1%; 14 ns to 0.02%
Overdrive and Output Short Circuit Protected
Fast Overdrive Recovery
DC Nonlinearity 5 ppm

APPLICATIONS

Driving Flash Converters
D/A Current to Voltage Converters
IF, Radar Processors
Baseband and Video Communications
Photodiode, CCD Preamps

PIN CONFIGURATION



NOTE: FOR BEST SETTLING TIME AND DISTORTION PERFORMANCE, USE OPTIONAL SUPPLY CONNECTIONS. PERFORMANCE INDICATED IN SPECIFICATIONS IS BASED ON SUPPLY CONNECTIONS TO THESE PINS.

GENERAL DESCRIPTION

The AD9618 is a current feedback amplifier which utilizes a proprietary architecture to produce superior distortion and dc precision. It achieves this along with fast settling, very fast slew rate, wide bandwidth (both small signal and large signal), and exceptional signal fidelity. The device achieves −63 dBc 2nd harmonic distortion at 20 MHz while maintaining 160 MHz small signal and 150 MHz large signal bandwidths.

These attributes position the AD9618 as an ideal choice for driving flash ADCs and buffering the latest generation of DACs. Optimized for applications requiring gain between +5/−1 to ±40, the AD9618 is unity gain stable without external compensation.

Additional benefits of the AD9618B and T grades include input offset voltage of 500 μV and temperature coefficient (TC) of 3 μV/°C. These accuracy performance levels make the AD9618 an excellent choice for driving emerging high resolution (12–16 bits), high speed analog to digital converters and flash converters.

The AD9618 offers outstanding performance in high fidelity, wide bandwidth applications in instrumentation ranging from network and spectrum analyzers to oscilloscopes, and in military systems such as radar, SIGINT, and ESM systems. The superior slew rate, low overshoot, and fast settling of the AD9618 allow the device to be used in pulse applications such as communications receivers and high speed ATE. Most monolithic op amps suffer in these precision pulse applications due to slew rate limiting.

***Patent pending.**

The AD9618J operates over the range of 0 to +70°C and is available in either an 8-pin plastic mini-DIP or an 8 lead plastic small outline package (SOIC). The AD9618A and B versions are rated over the industrial temperature range of −40°C to +85°C. The AD9618S and T versions are rated over the military temperature range of −55°C to +125°C; and are available processed to MIL-STD-883B.

AD9618—SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltages ($\pm V_S$) . . . . . ±7 V
Common Mode Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . 3 V
Continuous Output Current[2] . . . . . 70 mA
Operating Temperature Ranges
AD9618JN/JR . . . . . 0 to +70°C
AD9618AQ/BQ . . . . . −40°C to +85°C
AD9618SQ/TQ . . . . . −55°C to +125°C
Storage Temperature
AD9618JN/JR . . . . . −65°C to +125°C
AD9618AQ/BQ/SQ/TQ . . . . . −65°C to +150°C
Junction Temperature[3]
AD9618JN/JR . . . . . 150°C
AD9618AQ/BQ/SQ/TQ . . . . . 175°C
Lead Soldering Temperature (10 Seconds) . . . . . +300°C

DC ELECTRICAL CHARACTERISTICS

(unless otherwise noted, $A_V = +10$; $\pm V_S = \pm 5$ V; $R_F = 1000\ \Omega$; $R_{LOAD} = 100\ \Omega$)

Parameter	Conditions	Temp	Test Level	AD9618JN/JR Min	AD9618JN/JR Typ	AD9618JN/JR Max	AD9618AQ/SQ Min	AD9618AQ/SQ Typ	AD9618AQ/SQ Max	AD9618BQ/TQ Min	AD9618BQ/TQ Typ	AD9618BQ/TQ Max	Units
Input Offset Voltage[4, 5]		+25°C	I	−1.1	+0.5	+2.2	−1.1	+0.5	+2.2	0.0	+0.5	+1.1	mV
Input Offset Voltage TC[5]		Full	IV	−4	+3	+25	−4	+3	+25	−4	+3	+25	µV/°C
Input Bias Current[5]													
Inverting		+25°C	I	−45	0	+45	−45	0	+45	−20	0	+20	µA
Noninverting		+25°C	I	−25	+5	+35	−25	+5	+35	−13	+5	+18	µA
Input Bias Current TC[5]													
Noninverting		Full	IV	−50	+30	+125	−50	+30	+125	−50	+30	+125	nA/°C
Inverting		Full	IV	−50	+40	+130	−50	+40	+130	−50	+40	+130	nA/°C
Input Resistance													
Noninverting		+25°C	V		75			75			75		kΩ
Input Capacitance													
Noninverting		+25°C	V		1.5			1.5			1.5		pF
Common Mode Input Range[6]	$T = T_{max}$	←	II	±1.0	±1.2		±1.0	±1.2		±1.0	±1.2		V
	$T = T_{min}$ to +25°C	←	II	±1.4	±1.5		±1.4	±1.5		±1.4	±1.5		V
Common Mode Rejection Ratio[7]	$T = T_{max}$	←	II	44	48		44	48		44	48		dB
	T = +25°C	←	II	48	52		48	52		48	52		dB
	$T = T_{min}$	←	II	50	54		50	54		50	54		dB
Power Supply Rejection Ratio	$\Delta V_S = \pm 5\%$	Full	II	50	60		50	60		50	60		dB
Open Loop Gain													
T_O	At dc	+25°C	V		3			3			3		MΩ
Nonlinearity	At dc	+25°C	V		5			5			5		ppm
Output Voltage Range		+25°C	II	±3.3	±3.7		±3.3	±3.7		±3.3	±3.7		V
Output Impedance	At dc	+25°C	V		0.08			0.08			0.08		Ω
Output Current (50 Ω Load)	$T = +25°C$ to T_{max}	←	II	60			60			60			mA
	$T = T_{min}$	←	II	50			50			50			mA

AC ELECTRICAL CHARACTERISTICS

(unless otherwise noted, $A_V = +10$; $\pm V_S = \pm 5$ V; $R_F = 1$ kΩ; $R_{LOAD} = 100\ \Omega$)

Parameter	Conditions	Temp	Test Level	AD9618JN/JR Min	AD9618JN/JR Typ	AD9618JN/JR Max	AD9618AQ/SQ Min	AD9618AQ/SQ Typ	AD9618AQ/SQ Max	AD9618BQ/TQ Min	AD9618BQ/TQ Typ	AD9618BQ/TQ Max	Units
FREQUENCY DOMAIN													
Bandwidth (−3 dB)													
Small Signal	$V_{OUT} \le 2$ V p–p	Full	II	130	160		130	160		130	160		MHz
Large Signal	$V_{OUT} \le 5$ V p–p	Full	IV		150		120	150		120	150		MHz
Bandwidth Variation vs. A_V	$A_V = -1$ to ±40	+25°C	V		35			35			35		MHz
Amplitude of Peaking (<50 MHz)	$T = T_{min}$ to +25°C	←	II		0			0	0.4		0	0.4	dB
	$T = T_{max}$	←	II		0			0	0.7		0	0.7	dB
Amplitude of Peaking (>50 MHz)	$T = T_{min}$ to +25°C	←	II		0			0	0.6		0	0.6	dB
	$T = T_{max}$	←	II		0			0	1.2		0	1.2	dB
Amplitude of Roll-Off (<75 MHz)		Full	II		0.5			0.5	1.2		0.5	1.2	dB
Phase Nonlinearity	dc to 75 MHz	+25°C	V		0.5			0.5			0.5		Degree
2nd Harmonic Distortion	2 V p–p; 4.3 MHz	Full	IV		−83	−75		−83	−75		−83	−75	dBc
	2 V p–p; 20 MHz	Full	IV		−63	−55		−63	−55		−63	−55	dBc
	2 V p–p; 60 MHz	Full	II		−51	−43		−51	−43		−51	−43	dBc
3rd Harmonic Distortion	2 V p–p; 4.3 MHz	Full	IV		−85	−77		−85	−77		−85	−77	dBc
	2 V p–p; 20 MHz	Full	IV		−70	−62		−70	−62		−70	−62	dBc
	2 V p–p; 60 MHz	Full	II		−62	−54		−62	−54		−62	−54	dBc
Input Noise Voltage	10 MHz	+25°C	V		1.2			1.2			1.2		nV/√(Hz)
Inverting Input Noise Current	10 MHz	+25°C	V		24			24			24		pA/√(Hz)

Parameter	Conditions	Temp	Test Level	AD9618JN/JR Min	AD9618JN/JR Typ	AD9618JN/JR Max	AD9618AQ/SQ Min	AD9618AQ/SQ Typ	AD9618AQ/SQ Max	AD9618BQ/TQ Min	AD9618BQ/TQ Typ	AD9618BQ/TQ Max	Units
Average Equivalent Integrated Input Noise Voltage	0.1 to 200 MHz	+25°C	V		38			38			38		μV, rms
TIME DOMAIN													
Slew Rate	V_{OUT} = 4 V Step	Full	IV		1800		1400	1800		1400	1800		V/μs
Rise/Fall Time													
V_{OUT} = 2 V Step		Full	IV		2.2			2.2	2.6		2.2	2.6	ns
V_{OUT} = 5 V Step	T = +25°C to	←	IV		2.3			2.3	2.8		2.3	2.8	ns
	T = T_{min}	←	IV		2.3			2.3	3.1		2.3	3.1	ns
Overshoot	V_{OUT} = 2 V Step	Full	IV		2			2	10		2	10	%
Settling Time													
To 0.1%	V_{OUT} = 2 V Step	Full	IV		9			9	15		9	15	ns
To 0.02%	V_{OUT} = 2 V Step	Full	IV		14			14	23		14	23	ns
To 0.1%	V_{OUT} = 4 V Step	Full	IV		10			10	16		10	16	ns
To 0.02%	V_{OUT} = 4 V Step	Full	IV		16			16	24		16	24	ns
2×Overdrive Recovery to ±2 mV of Final Value	V_{IN} = 0.6 V Step	+25°C	V		50			50			50		ns
Propagation Delay		+25°C	V		2			2			2		ns
Differential Gain[8]		Full	V		0.01			0.01			0.01		%
Differential Phase[8]		Full	V		0.02			0.02			0.02		Degree
POWER SUPPLY REQUIREMENTS													
Quiescent Current													
$+I_S$		Full	II		31	43		31	43		31	43	mA
$-I_S$		Full	II		31	43		31	43		31	43	mA

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Output is short circuit protected to ground, but not to supplies. Continuous short circuit to ground may affect device reliability.

[3]Typical thermal impedances (part soldered onto board):
Mini-DIP: θ_{JA} = 140°C/W; θ_{JC} = 30°C/W.
Side Brazed/Cerdip: θ_{JA} = 110°C/W; θ_{JC} = 20°C/W.
SOIC Package: θ_{JA} = 150°C/W; θ_{JC} = 30°C/W.

[4]Measured with respect to the inverting input.

[5]Typical is defined as the mean of the distribution.

[6]Measured in voltage follower configuration.

[7]Measured with V_{IN} = ±0.25 V.

[8]Frequency = 4.3 MHz; R_L = 150 Ω; A_V = +10.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

II – 100% production tested at +25°C and sample tested at specified temperatures. AC testing of J grade devices done on sample basis.

III – Sample tested only.

IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

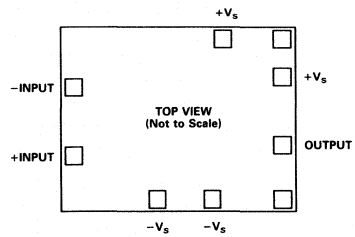
VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD9618JN	0 to +70°C	Plastic DIP	N-8
AD9618JR	0 to +70°C	SOIC	R-8
AD9618AQ	−40°C to +85°C	Cerdip	Q-8
AD9618BQ	−40°C to +85°C	Cerdip	Q-8
AD9618SQ	−55°C to +125°C	Cerdip	Q-8
AD9618TQ	−55°C to +125°C	Cerdip	Q-8

*For outline information see Package Information section.

DIE CONNECTIONS



DIE SIZE = 53 × 67 × 15 mils

THEORY OF OPERATION

The AD9618 has been designed to combine the key attributes of traditional "low frequency" precision amplifiers with exceptional high frequency characteristics that are independent of closed-loop gain. Previous "high frequency" closed-loop amplifiers have low open loop gain relative to precision amplifiers. This results in relatively poor dc nonlinearity and precision, as well as excessive high frequency distortion due to open loop gain roll-off.

Operational amplifiers use two basic types of feedback correction, each with advantages and disadvantages. Voltage feedback topologies exhibit an essentially constant gain bandwidth product. This forces the closed-loop bandwidth to vary inversely with closed-loop gain. Moreover, this type design typically slew rate limits in a way that causes the large signal bandwidth to be much lower than its small signal characteristics.

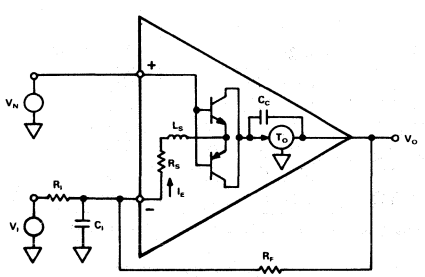
A newer approach is to use current feedback to realize better dynamic performance. This architecture provides two key attributes over voltage feedback configurations: (1) avoids slew rate limiting and therefore large signal bandwidth can approach small signal performance; and (2) low bandwidth variation versus gain settings, due to the inherently low open loop inverting input resistance (R_S).

The AD9618 uses a new current feedback topology that overcomes these limitations and combines the positive attributes of both current feedback and voltage feedback designs. These devices achieve excellent high frequency dynamics (slew, BW and distortion) along with excellent low frequency linearity and good dc precision.

DC GAIN CHARACTERISTICS

A simplified equivalent schematic is shown below. When operating the device in the inverting mode, the input signal error current (I_E) is amplified by the open loop transimpedance gain (T_O). The output signal generated is equal to $T_O \times I_E$. Negative feedback is applied through R_F such that the device operates at a gain (G) equal to $-R_F/R_I$.

Noninverting operation is similar, with the input signal applied to the high impedance buffer (noninverting) input. As before,



Equivalent Circuit

an output (buffer) error current (I_E) is generated at the low impedance inverting input. The signal generated at the output is fed back to the inverting input such that the external gain is $(1+ R_F/R_I)$. The feedback mechanics are identical to the voltage feedback topology when exact equations are used.

The major difference lies in the front end architecture. A voltage feedback amplifier has symmetrical high resistance (buffered) inputs. A current feedback amplifier has a high noninverting resistance (buffered) input and a low inverting (buffer output) input resistance. The feedback mechanics can be easily developed using current feedback and transresistance open loop gain T(s) to describe the I/O relationship. (See typical specification chart.)

DC closed-loop gain for the AD9618 can be calculated using the following equations:

$$G = \frac{V_O}{V_I} \approx \frac{-R_F/R_I}{1 + 1/LG} \quad \text{inverting} \qquad (1)$$

$$G = \frac{V_O}{V_N} \approx \frac{1 + R_F/R_I}{1 + 1/LG} \quad \text{noninverting} \qquad (2)$$

$$\text{where: } \frac{1}{LG} \approx \frac{R_S(R_F + R_S \| R_I)}{T(s)(R_S \| R_I)} \qquad (3)$$

Because the noninverting input buffer is not ideal, input resistance R_S (at dc) is gain dependent and is typically higher for noninverting operation than for inverting operation. R_S will approach the same value ($\approx 9\ \Omega$) for both at input frequencies above 50 MHz. Below the open loop corner frequency, the noninverting R_S can be approximated as:

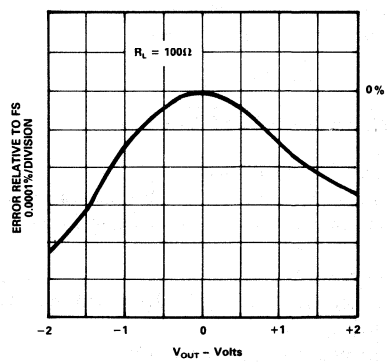
$$R_S\ (noninverting) \approx 9 + \frac{T(s)}{A_O} = 9 + \left.\frac{T_O}{A_O}\right|_{dc} \qquad (4)$$

where: A_O=*Open Loop Voltage Gain* $\approx G \times 350$

Inverting R_S below the open loop corner frequency can be approximated as:

$$R_S\ (inverting) \approx 9 + \frac{T(s)}{A_O} = 9 + \left.\frac{T_O}{A_O}\right|_{dc} \qquad (5)$$

where: A_O = *140,000*



DC Nonlinearity vs. V_{OUT}

The AD9618 approaches this condition. With $T_O = 3 \times 10^6\ \Omega$ and $R_S = 32\ \Omega$ (dc), a gain error of 0.04% typically results for $G = -1$ and 0.11% for $G = -100$. Moreover, the architecture linearizes the open loop gain over its operating voltage range and temperature resulting in >16 bits of linearity.

AC GAIN CHARACTERISTICS

Closed-loop bandwidth at high frequencies is determined primarily by the roll-off of T(s). But circuit layout is critical to minimize external parasitics which can degrade performance by causing premature peaking and/or reduced bandwidth.

The inverting and noninverting dynamic characteristics are similar. When driving the noninverting input, the inverting input capacitance (C_I) will cause the noninverting closed-loop bandwidth to be higher than the inverting bandwidth for gains less than five (5). In the remaining cases, inverting and noninverting responses are nearly identical.

For best overall dynamic performance, the value of the feedback resistor (R_F) should be 1000 Ω. Although bandwidth reduces as closed-loop gain increases, the change is relatively small due to low equivalent series input impedance, Z_S. (See typical performance charts.) The simplified equations governing the device's dynamic performance are shown below.

Closed-Loop Gain vs. Frequency:
(noninverting operation)

$$\frac{V_O}{V_S} \approx \frac{1 + \frac{R_F}{R_I}}{s\tau\left(1 + \frac{R_S}{R_I}\right) + 1} \qquad (6)$$

where: $\tau = R_F \times C_C = 1.0\ ns\ (R_F = 1\ k\Omega)$

$$Slew\ Rate \approx \frac{\Delta V_O}{R_F K C_C} \times e^{-\tau/R_F K C_C} \qquad (7)$$

where: $K = 1 + \frac{R_S}{R_I}$

Increasing Bandwidth at Low Gains

By reducing R_F, wider bandwidth and faster pulse response can be attained beyond the specified values, although increased overshoot, settling time, and possible ac peaking may result. As a rule of thumb, overshoot and bandwidth will increase by 1% and 8%, respectively, for a 5% reduction in R_F at gains of ±10.

Equations 6 and 7 are simplified and do not accurately model the second order (open loop) frequency response term which is the primary contributor to overshoot, peaking, and nonlinear bandwidth expansion. (See Open Loop Bode Plots.) The user should exercise caution when selecting R_F values much lower than 1000 Ω. Note that a feedback resistor must be used in all situations.

Increasing Bandwidth at High Gains

Closed-loop bandwidth can be extended at high closed-loop gain by reducing R_F. Bandwidth reduction is a result of the feedback current being split between R_S and R_I. As the gain increases (for a given R_F), more feedback current is shunted through R_I, which reduces closed-loop bandwidth (see Equation 6). To maintain specified BW, the following equations can be used to approximate R_F and R_I for any gain from = +5/−1 to ±40.

$$R_F = 1100 \pm 8\,G \qquad (8)$$

(+ for inverting and − for noninverting)

$$R_I \approx \frac{1100 - 10\,G}{G - 1} \quad \text{(noninverting)} \qquad (9)$$

$$R_I \approx \frac{1100 + 10\,G}{G} \quad \text{(inverting)} \qquad (10)$$

G = *Closed-Loop Gain.*

Bandwidth Reduction

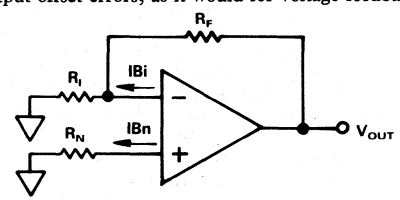
The closed-loop bandwidth can be reduced by increasing R_F. Equations 6 and 7 can be used to determine the closed-loop bandwidth for any value R_F. Do not connect a feedback capacitor across R_F, as this will degrade dynamic performance and possibly induce oscillation.

DC Precision and Noise

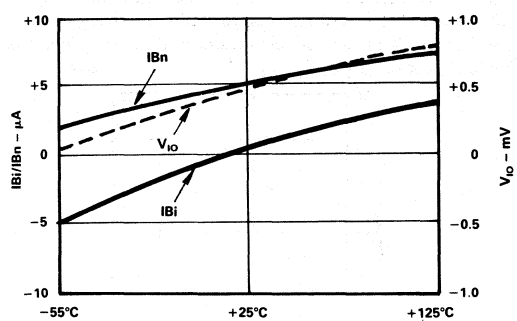
Output offset voltage results from both input bias currents and input offset voltage. These input errors are multiplied by the noise gain term ($1 + R_F/R_I$) and algebraically summed at the output as shown below.

$$V_O = V_{IO} \times \left(1 + \frac{R_F}{R_I}\right) \pm IBn \times R_N \times \left(1 + \frac{R_F}{R_I}\right) \pm IBi \times R_F \qquad (11)$$

Since the inputs are asymmetrical, IBi and IBn do not correlate. Canceling their output effects by making $R_N = R_F \| R_I$ will not reduce output offset errors, as it would for voltage feedback amplifiers. Typically, IBn is 5 μA and V_{IO} is +0.5 mV (1 sigma = 0.3 mV), which means that the dc output error can be reduced by making $R_N \approx 100\ \Omega$. Note that the offset drift will not change significantly because the IBn TC is relatively small. (See specification table.)

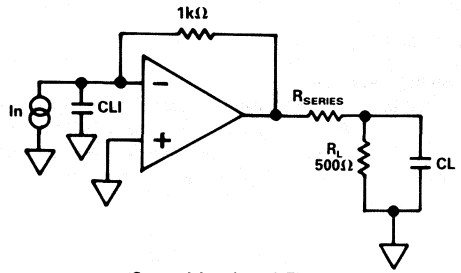


Output Offset Voltage



DC Accuracy

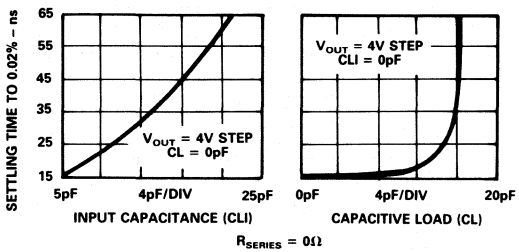
The effective noise at the output of the amplifier can be determined by taking the root sum of the squares of Equation 11 and applying the spectral noise values found in the typical graph section. This applies to noise from the op amp only. Note that both the noise figure and equivalent input offset voltage improve as the closed-loop gain is increased (by keeping R_F fixed and reducing R_I with $R_N = 0\ \Omega$).



Capacitive Load Figure

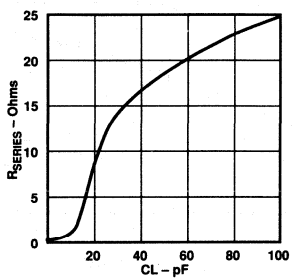
Capacitive Load Considerations

Due to the low inverting input resistance (R_S) and output buffer design, the AD9618 can directly handle input and/or output load capacitances of up to 10 pF. See the chart below.



Input/Output Capacitance Comparisons

A small series resistor can be used at the output of the amplifier and outside of the feedback loop to facilitate driving larger capacitive loads or for obtaining faster settling time. For capacitive loads above 10 pF, R_{SERIES} should be considered.



Recommended R_{SERIES} vs. CL

APPLYING THE AD9618

The superior frequency and time domain specifications of the AD9618 make it an obvious choice for driving flash converters and buffering the outputs of high speed DACs. Its outstanding distortion and noise performance make it well suited as a driver for analog-to-digital converters (ADCs) with resolutions as high as 16 bits.

Typical circuits for inverting and noninverting applications are shown in Figures 1 and 2.

Closed-loop gain for noninverting configurations is determined by the value of R_I according to the equation:

$$G = 1 + \frac{R_F}{R_I} \tag{12}$$

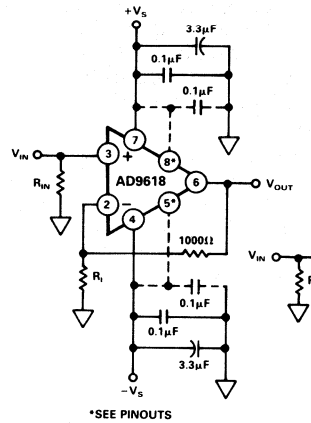


Figure 1. Noninverting Operation

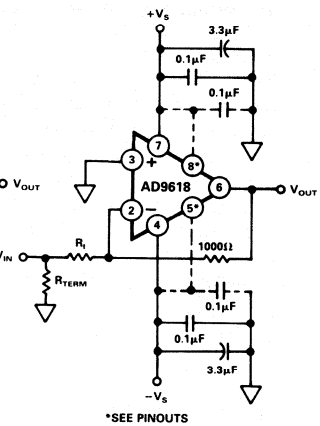


Figure 2. Inverting Operation

To preserve the amplifier's full bandwidth, the noninverting input should be driven from a low impedance source.

A recommended circuit for an inverting amplification is shown in Figure 2.

Closed-loop gain for inverting configurations is determined by the value of R_I per the following equation:

$$G = -\frac{R_F}{R_I} \tag{13}$$

LAYOUT CONSIDERATIONS

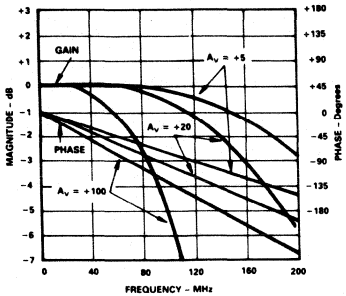
As with all high performance amplifiers, printed circuit layout is critical in obtaining optimum results with the AD9618. The ground plane in the area of the amplifier should cover as much of the component side of the board as possible. Each power supply trace should be decoupled close to the package with at least a 3.3 µF tantalum and a low inductance, 0.1 µF ceramic capacitor.

All lead lengths for input, output, and the feedback resistor should be kept as short as possible. All gain setting resistors should be chosen for low values of parasitic capacitance and inductance, i.e., microwave resistors and/or carbon resistors.

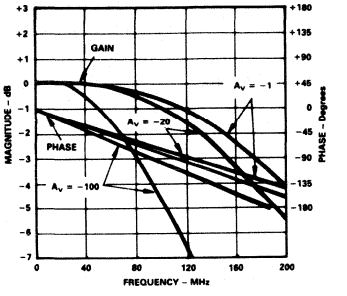
Stripline techniques should be used for lead lengths in excess of one inch. Sockets should be avoided if possible because of their stray inductance and capacitance. If sockets are necessary, individual pin sockets such as AMP p/n 6-330808-3 should be used. These contribute far less stray reactance than molded socket assemblies.

An evaluation board is available from Analog Devices for a nominal charge.

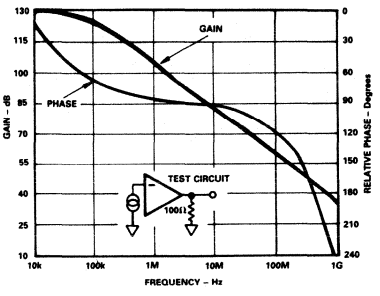
Typical Performance (A_V = +10; $\pm V_S$ = ±5V; R_F = 1 kΩ, unless otherwise noted)



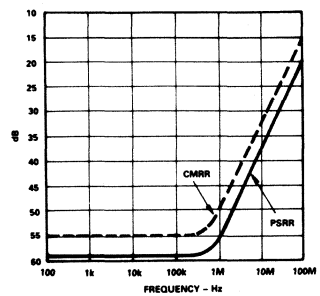
Noninverting Frequency Response



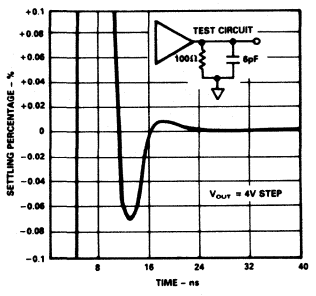
Inverting Frequency Response



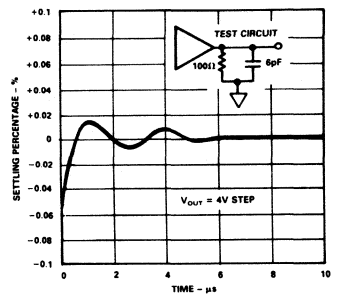
Open Loop Transimpedance Gain [T(s) Relative to 1 Ω]



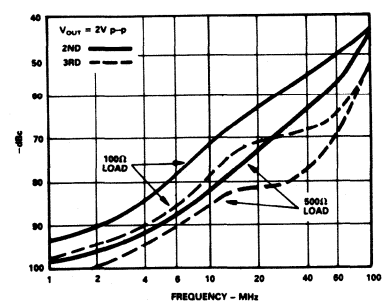
CMRR and PSRR



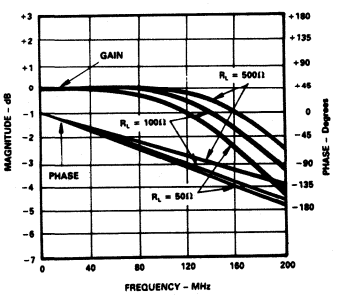
Settling Time



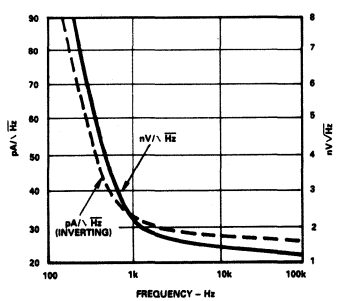
Long Term Settling Time



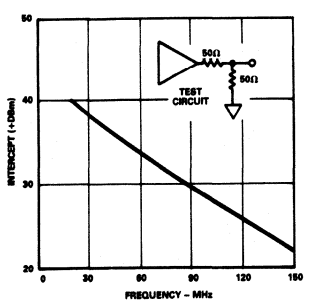
Harmonic Distortion



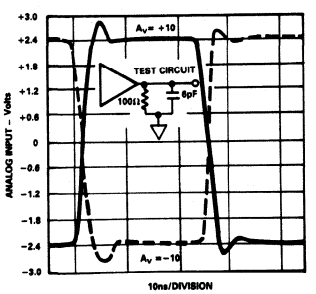
Frequency Response vs. R_{LOAD}



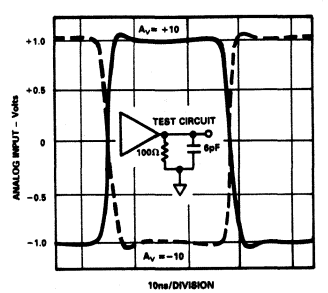
Equivalent Input Noise



Intermodulation Distortion (IMD)



Large Signal Pulse Response



Small Signal Pulse Response

ANALOG DEVICES

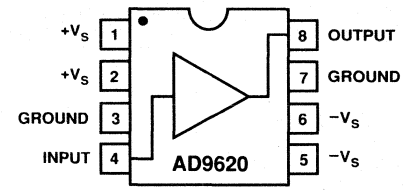
Ultralow Distortion, 600 MHz Buffer

AD9620*

FEATURES
Excellent Gain Accuracy: 0.994 V/V
Wide Bandwidth: 600 MHz
Slew Rate: 2200 V/μs
Ultralow Distortion:
−73 dBc @ 20 MHz
−91 dBc @ 2.3 MHz
Fast Settling Time: 8 ns to 0.02%
Low Noise: 2.0 nV/$\sqrt{Hz}$

APPLICATIONS
IF/Communications
Impedance Transformations
Drives Flash ADCs
Line Driving

DIP CONFIGURATION



NC = NO CONNECT

GENERAL DESCRIPTION

The AD9620 is a monolithic, unity gain buffer amplifier that sets new standards in gain accuracy, wide bandwidth and low distortion. Its large signal bandwidth, ultralow distortion over frequency, and drive capabilities of the AD9620 make this buffer an ideal driver for flash ADCs. Other applications which require increased current drive at unity voltage gain, such as cable driving, also benefit from the AD9620's performance.

In addition to innovative (patent pending) feedback architecture, special packaging techniques improve dynamic performance by minimizing the reactive effects associated with standard packages. The result is −73 dBc harmonic suppression at 20 MHz, and −91 dBc at 2.3 MHz. The AD9620 also outperforms other amplifiers, including its predecessor AD9630, in terms of small-signal pulse response and dc linearity. These features make the AD9620 the premier driver for high speed, high resolution ADCs.

Available in side-brazed ceramic DIP packages, the "A" suffix unit is guaranteed for −40°C to +85°C operating temperatures; the "S" suffix device is guaranteed from −55°C to +125°C. AD9620 die are dc tested at +25°C.

*Patent(s) Pending.

AD9620—SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltages ($\pm V_S$) . . . . . ±7 V
Input Voltage Range . . . . . $\pm V_S$
Continuous Output Current[2] . . . . . 70 mA
Operating Temperature Ranges
AD9620AD . . . . . −40°C to +85°C
AD9620SD . . . . . −55°C to +125°C
Storage Temperature
AD9620AD . . . . . −65°C to +150°C
AD9620SD . . . . . −65°C to +150°C
Junction Temperature[3] . . . . . +175°C
Lead Soldering Temperature (10 seconds)[4] . . . . . +300°C

DC ELECTRICAL CHARACTERISTICS (unless otherwise noted, $\pm V_S = \pm 5$ V; $R_{IN} = 50\ \Omega$, $R_{LOAD} = 100\ \Omega$)

Parameter	Conditions	Temp	Test Level	AD9620AD Min	AD9620AD Typ	AD9620AD Max	AD9620SD Min	AD9620SD Typ	AD9620SD Max	Units
DC SPECIFICATIONS										
Output Offset Voltage		+25°C	I	−8	±2	+8	−8	±2	+8	mV
Offset Voltage TC		Full	IV	−25	±5	+25	−25	±5	+25	µV/°C
Input Bias Current		+25°C	I	−35	±6	+35	−35	±6	+35	µA
Bias Current TC		Full	IV	−150	±50	+150	−150	±50	+150	nA/°C
Input Resistance		+25°C to T_{max}	VI	400	800		400	800		kΩ
Input Resistance		T_{min}	VI	190			190			kΩ
Input Capacitance		+25°C	V		1.0			1.0		pF
Gain	V_{OUT} = 2 V p–p	Full	VI	0.989	0.994		0.989	0.994		V/V
Output Voltage Range		Full	VI	+2.8		−2.8	+2.8		−2.8	V
Output Current (50 Ω Load)		Full	VI	40			40			mA
Output Impedance	At DC	+25°C	V		0.4			0.4		Ω
Power Supply Rejection Ratio	$\Delta V_S = \pm 5\%$	Full	VI	52	60		52	60		dB
DC Nonlinearity	±2 V Full Scale	+25°C	VI		0.005			0.005		%
FREQUENCY DOMAIN										
Bandwidth (−3 dB)										
Small Signal	V_{OUT} = ≤0.7 V p–p	T_{min} to +25°C	II	320	600		320	600		MHz
Small Signal	V_{OUT} = ≤0.7 V p–p	T_{max}	II	260			260			MHz
Large Signal	V_{OUT} = 4 V p–p	T_{min} to +25°C	IV	60	80		60	80		MHz
Large Signal	V_{OUT} = 4 V p–p	T_{max}	IV	45			45			MHz
Amplitude of Peaking	≤150 MHz	T_{min} to +25°C	II		0.8	1.5		0.8	1.5	dB
Amplitude of Peaking	≤150 MHz	T_{max}	II		1.5	2.2		1.5	2.2	dB
Amplitude of Rolloff	≤150 MHz	Full	II		0	0.3		0	0.3	dB
Group Delay	DC to 150 MHz	+25°C	V		0.75			0.75		ns
Phase Nonlinearity	DC to 150 MHz	+25°C	V		1.4			1.4		Degrees
2nd Harmonic Distortion	2 V p–p; 2.3 MHz	+25°C to T_{max}	IV		−91	−82		−91	−82	dBc
	2 V p–p; 2.3 MHz	T_{min}	IV		−81	−73		−81	−73	dBc
	2 V p–p; 20 MHz	Full	IV		−71	−63		−71	−63	dBc
	2 V p–p; 60 MHz	+25	I		−69	−60		−69	−60	dBc
	2 V p–p; 60 MHz	T_{min} and T_{max}	V		−62			−62		dBc
3rd Harmonic Distortion	2 V p–p; 2.3 MHz	Full	IV		−94	−86		−94	−86	dBc
	2 V p–p; 20 MHz	Full	IV		−81	−71		−81	−71	dBc
	2 V p–p; 60 MHz	+25°C	I		−60	−52		−60	−52	dBc
Spectral Input Noise Voltage	10 MHz	+25°C	V		2.0			2.0		nV/$\sqrt{\text{Hz}}$
Average Equivalent Integrated Output Noise Voltage	0.1 to 200 MHz	+25°C	V		28			28		µV
TIME DOMAIN										
Slew Rate	V_{OUT} = 4 V Step	+25°C	IV	1500	2200		1500	2200		V/µs
Rise/Fall Time	V_{OUT} = 1 V Step	T_{min} to +25°C	IV		0.8	1.2		0.8	1.2	ns
	V_{OUT} = 1 V Step	T_{max}	IV		1.1	1.5		1.1	1.5	ns
	V_{OUT} = 4 V Step	T_{min} to +25°C	IV		1.7	2.5		1.7	2.5	ns
	V_{OUT} = 4 V Step	T_{max}	IV		2.3	3.4		2.3	3.4	ns
Overshoot	V_{OUT} = 2 V Step	Full	IV		3	12		3	12	%
Settling Time										
To 0.1%	V_{OUT} = 2 V Step	Full	IV		6	10		6	10	ns
To 0.02%	V_{OUT} = 2 V Step	Full	IV		8	16		8	16	ns
Differential Gain	4.4 MHz	+25°C	V		0.02			0.02		%
Differential Phase	4.4 MHz	+25°C	V		0.02			0.02		Degrees

Parameter	Conditions	Temp	Test Level	AD9620AD Min	AD9620AD Typ	AD9620AD Max	AD9620SD Min	AD9620SD Typ	AD9620SD Max	Units
POWER SUPPLY REQUIREMENTS										
Quiescent Current										
$+I_S$	$+V_S$ = +5 V	Full	VI		40	48		40	48	mA
$-I_S$	$-V_S$ = −5 V	Full	VI		40	48		40	48	mA

NOTES
[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Output is short-circuit protected to ground, but not to supplies. Continuous short circuit to ground may affect device reliability.
[3]Typical side-brazed thermal impedances (part soldered onto board): θ_{JA} = 110°C/W; θ_{JC} = 20°C/W.
[4]External capacitor of AD9620 is attached with 62 Sn/36 Pb/2 Ag solder. Board attachment temperatures should be reviewed to insure the capacitor does not reflow during board mounting.

Specifications subject to change without notice.

2

EXPLANATION OF TEST LEVELS

Test Level
I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures.
III – Sample tested only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

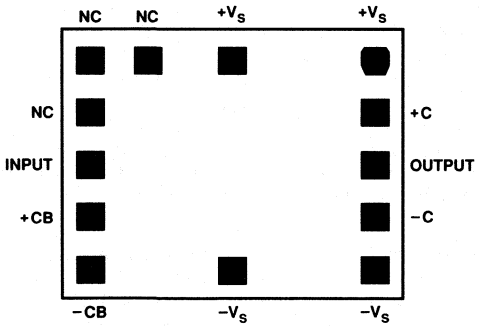
ORDERING GUIDE

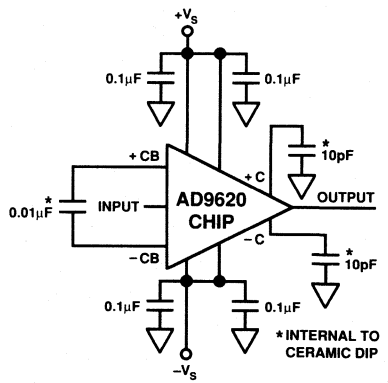
Model	Temperature Range	Package Description	Package Option*
AD9620AD	−40°C to +85°C	8-Pin DIP	D-8
AD9620SD	−55°C to +125°C	8-Pin DIP	D-8
AD9620 Chips	+25°C	Dice	

*For outline information see Package Information section.

AD9620 DIE LAYOUT

60 (length) × 50 (width) × 15 (height) mils





AD9620 Bonding Diagram

THEORY OF OPERATION

The AD9620 is a wide bandwidth, unity gain buffer amplifier that utilizes innovative (patent pending) voltage feedback architecture. Large loop gain and high slew rate significantly improve dc linearity and large signal bandwidth when compared with that achieved with more conventional designs.

Its large-signal bandwidth compares favorably with competitive devices of open-loop design without their limitations. Open-loop devices often sacrifice dc linearity and introduce frequency distortion when driving low load impedances; the AD9620 does not. Its design yields low distortion products that are relatively constant for any resistive load greater than 50 ohms.

The AD9620 will satisfy any high performance analog signal processing application requiring isolation or current boosting between the signal source and load. Its combination of high input resistance and low capacitance, dc precision, and exceptional dynamic characteristics sets a new standard in performance that has no equal.

Excessive peaking may occur when using the AD9620 to directly drive loads with more than 3 pF of capacitance. To prevent this, a small value of resistance (R_S) should be placed in series with

the buffer output. The following figure shows various values of R_S as a function of capacitive load.

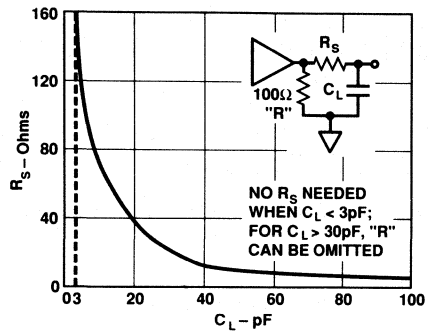


Figure 1. Recommended R_S vs. C_L

When the recommended series resistor is used, the AD9620 will have optimum frequency response, as shown in Figure 2.

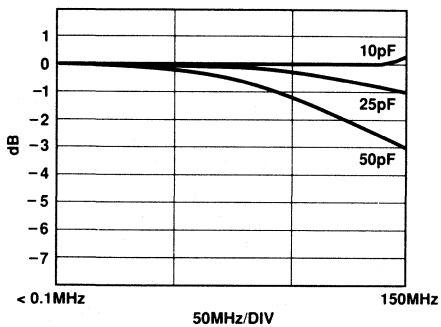


Figure 2. Frequency Response vs. C_L with Recommended R_S

Capacitive loads up to 50 pF can be driven with minimal degradation in pulse response with R_S equal to approximately 12 ohms.

The output stage has short-circuit protection to ground, but average load currents greater than 70 mA may reduce device reliability. The output driver will shut down if more than approximately 130 mA of instantaneous sink or source current is flowing. This ensures that output clipping will not occur during high slew conditions when driving capacitive loads.

LAYOUT CONSIDERATIONS

Although the AD9620AD/SD is housed in a specially designed package with built-in decoupling capacitors, the layout of the circuit containing the buffer requires careful attention. Without it, dynamic performance may be less than desired.

Optimum performance depends on connecting all of the supply pins and ground pins of the AD9620. If they are not connected, the inherent benefits of the buffer's special package will not be realized.

A two-ounce copper ground plane on the component side of the board is recommended. It should cover as much of the board as possible with appropriate openings for supply decoupling capacitors and for load and source resistors.

Settling time and ac performance will be optimized with surface mount 0.1 μF supply decoupling capacitors. These should be located within 50 mils of their corresponding device pins, with the opposite side of the capacitor soldered directly to the ground plane.

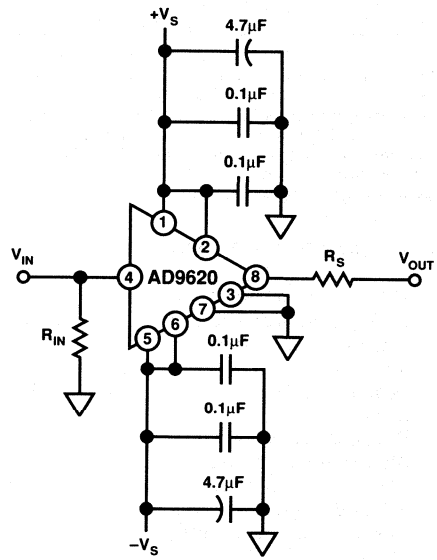


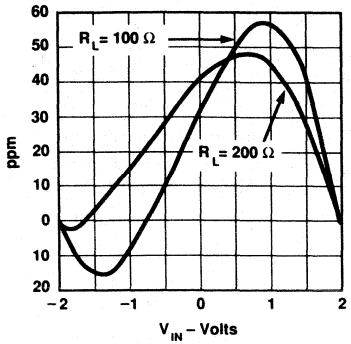
Figure 3. AD9620 Application Circuit (Ceramic DIP)

If surface mount capacitors cannot be used, radial lead ceramic capacitors with lead lengths less than 30 mils are recommended. Low frequency power supply decoupling is also necessary and can be accomplished with 4.7 μF tantalum capacitors mounted within 0.5 inch of the voltage supply pins. The interaction of the series inductance of the tantalum capacitor with the 0.1 μF decoupling capacitor and the supply leads may cause high frequency oscillations at the output. These can be eliminated with a ferrite bead mounted between the tantalum and ceramic capacitors.

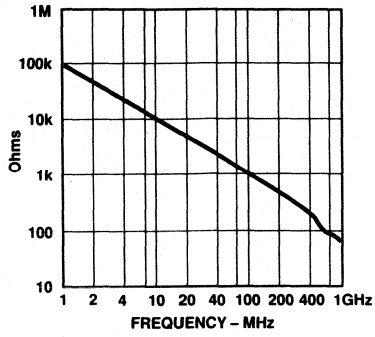
Connections to the AD9620 should be as short as possible. If either the source circuit or the driven circuit is further than one inch from the buffer, the printed circuit board (PCB) line impedances should be matched to the buffer input and output resistances. Basic microstrip techniques should be observed. The input termination resistor (R_{IN}) and R_S should both be connected as close to the AD9620 as possible.

Its performance characteristics allow the AD9620 to drive terminated cables directly without the use of an output termination resistor for many applications. When used, termination resistors (R_S and R_{IN}) can be either carbon composition or microwave types. When matching characteristic impedances, precision microwave resistors with tolerance of 1% or better are recommended.

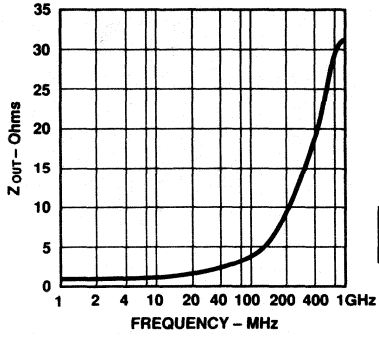
The AD9620 should be soldered directly to the PCB with minimum vertical clearance. The use of zero-insertion sockets is discouraged because of their high pin reactances. Use of this type socket will result in peaking and possibly induce oscillation. If sockets must be used for test or prototyping purposes, individual pin sockets such as the AMP 6-330808 series are recommended.



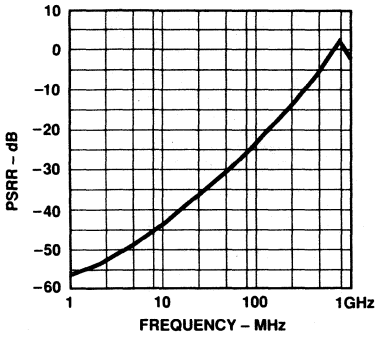
Endpoint DC Linearity Error



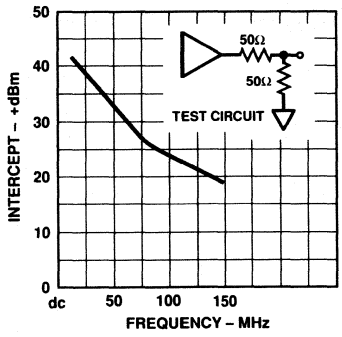
Input Impedance



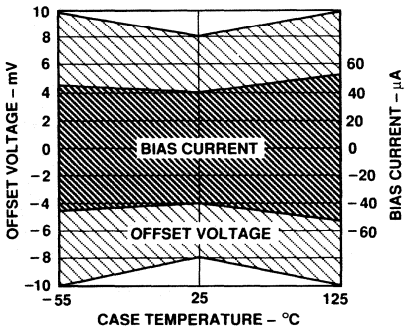
Output Impedance



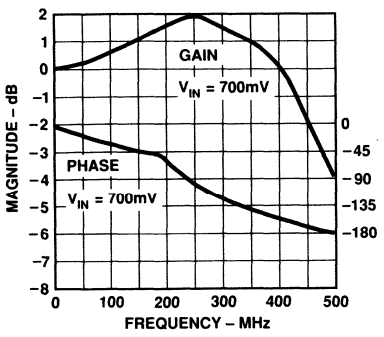
PSRR vs. Frequency



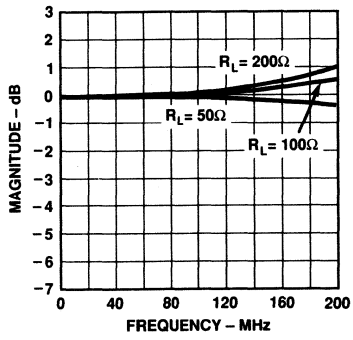
Two-Tone Intermodulation Distortion



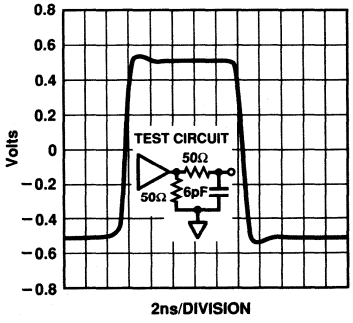
Offset Voltage and Bias Current vs. Temperature (Worst Case)



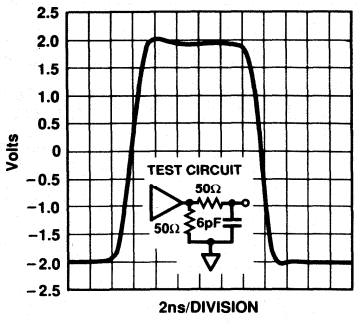
Forward Gain and Phase



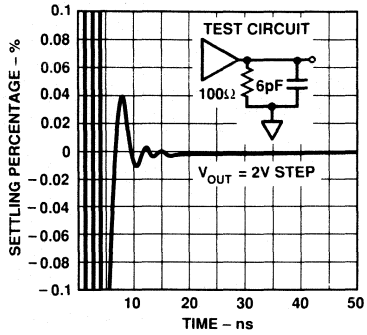
Frequency Response vs. R_{LOAD}



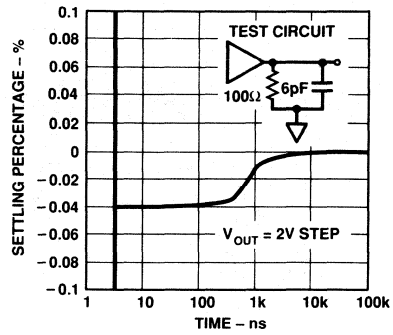
Small-Signal Pulse Response



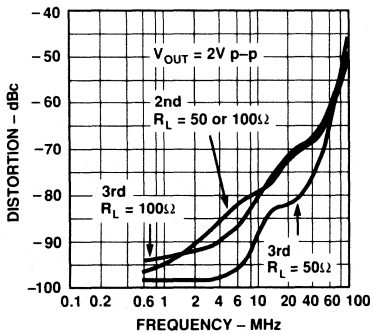
Large-Signal Pulse Response



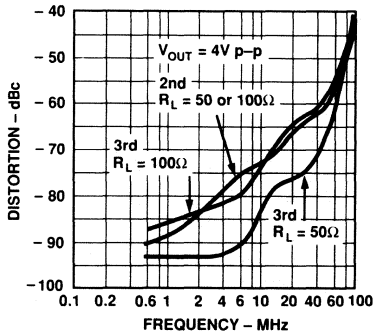
Short-Term Settling Time



Long-Term Settling Time



Harmonic Distortion vs. Frequency



Harmonic Distortion vs. Frequency

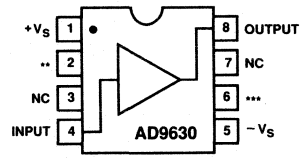
Low Distortion, 750 MHz Closed-Loop Buffer Amp

AD9630*

FEATURES
Excellent Gain Accuracy: 0.99 V/V
Wide Bandwidth: 750 MHz
Slew Rate: 1200 V/μs
Low Distortion
−65 dBc @ 20 MHz
−80 dBc @ 4.3 MHz
Settling Time
6 ns to 0.1%
8 ns to 0.02%
Low Noise: 2.4 nV/√Hz
Improved Source for CLC-110

APPLICATIONS
IF/Communications
Impedance Transformations
Drives Flash ADCs
Line Driving

PIN CONFIGURATION



**OPTIONAL $+V_S$ ***OPTIONAL $-V_S$
NC = NO CONNECT

NOTE: FOR BEST SETTLING TIME PERFORMANCE USE OPTIONAL POWER SUPPLIES. ALL SPECIFICATIONS ARE BASED ON USING SINGLE $\pm V_S$ CONNECTIONS EXCEPT FOR SETTLING TIME TO 0.02% AND SMALL SIGNAL S21. CONSULT THE FACTORY FOR VERSIONS WITH OPTIONAL POWER SUPPLY PINS DISCONNECTED INTERNAL TO THE PACKAGE.

General Description

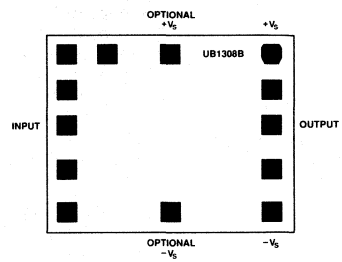
The AD9630 is a monolithic buffer amplifier that utilizes innovative (patent pending) closed-loop design techniques to achieve exceptional gain accuracy, wide bandwidth, and low distortion. Slew rate limiting has been overcome as indicated by the 1200 V/μs slew rate; this improvement allows the user greater flexibility in wideband and pulse applications. The second harmonic distortion terms for an analog input tone of 4.3 MHz and 20 MHz are −80 dBc and −66 dBc, respectively. Clearly, the AD9630 establishes a new standard by combining in one part outstanding dc and dynamic performance.

The large signal bandwidth, low distortion over frequency, and drive capabilities of the AD9630 make the buffer an ideal flash ADC driver. The AD9630 provides better signal fidelity than many of the flash ADCs that it has been designed to drive.

Other applications which require increased current drive at unity voltage gain such as cable driving benefit from the AD9630's performance.

The AD9630 is available in Plastic DIP (N), Ceramic DIP (Q), and SOIC (R). Consult with the factory concerning availability of MIL-STD-883 parts. Die are dc tested at +25°C.

DIE LAYOUT
Die Dimensions 60×50×15 mils



*Patent(s) Pending

AD9630—SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltages ($\pm V_S$) . . . . . ±7 V
Continuous Output Current[2] . . . . . 70 mA
Temperature Range over Which Specifications Apply
AD9630AN/AR/AQ . . . . . −40°C to +85°C
Lead Soldering Temperature (10 sec) . . . . . +300°C
Storage Temperature
AD9630AN/AR/AQ . . . . . −65°C to +150°C
Junction Temperature[3]
AD9630AN/AR/AQ . . . . . +150°C

ELECTRICAL CHARACTERISTICS (unless otherwise noted, $\pm V_S = \pm 5$ V; $R_{IN} = 50\ \Omega$, $R_{LOAD} = 100\ \Omega$)

Parameter	Conditions	Temp	Test Level	AD9630A/N/R/Q Min	Typ	Max	Units
DC SPECIFICATIONS							
Output Offset Voltage		+25°C	I	−8	±3	+8	mV
Offset Voltage TC		Full	IV	−40	±8	+40	µV/°C
Input Bias Current		+25°C	I	−25	±2	+25	µA
Bias Current TC		Full	IV	−100	±20	+100	nA/°C
Input Resistance		+25 to T_{max}	II	300	450		kΩ
Input Resistance		T_{min}	VI	150	250		kΩ
Input Capacitance		+25°C	V		1.0		pF
Gain	V_{OUT} = 2 V p-p	+25 to T_{max}	II	0.983	0.990		V/V
Gain	V_{OUT} = 2 V p-p	T_{min}	VI	0.980	0.985		V/V
Output Voltage Range		Full	VI	+3.2	±3.6	−3.2	V
Output Current (50 Ω Load)		+25 to T_{max}	II	50			mA
Output Current (50 Ω Load)		T_{min}	VI	40			mA
Output Impedance	At dc	+25°C	V		0.6		Ω
PSRR	$\Delta V_S = \pm 5\%$	Full	VI	44	55		dB
DC Nonlinearity	±2 V Full Scale	+25°C	V		0.03		%
FREQUENCY DOMAIN							
Bandwidth (−3 dB)							
Small Signal	$V_O \leq 0.7$ V p-p	T_{min} to 25	II	400	750		MHz
Small Signal	$V_O \leq 0.7$ V p-p	T_{max}	II	330	550		MHz
Large Signal	V_O = 5 V p-p	T_{min} to 25	V		120		MHz
Large Signal	V_O = 5 V p-p	T_{max}	V		105		MHz
Output Peaking	≤200 MHz	Full	II		0.4	1.2	dB
Output Rolloff	≤200 MHz	Full	II		0	0.3	dB
Group Delay	dc to 150 MHz	+25°C	V		0.7		ns
Linear Phase Deviation	dc to 150 MHz	+25°C	V		0.7		Degrees
2nd Harmonic Distortion	2 V p-p; 4.3 MHz	Full	IV		−80	−73	dBc
	2 V p-p; 20 MHz	Full	IV		−66	−58	dBc
	2 V p-p; 50 MHz	Full	II		−52	−43	dBc
3rd Harmonic Distortion	2 V p-p; 4.3 MHz	Full	IV		−86	−79	dBc
	2 V p-p; 20 MHz	Full	IV		−75	−68	dBc
	2 V p-p; 50 MHz	T_{min} to +25	II		−47	−41	dBc
	2 V p-p; 50 MHz	T_{max}	II		−46	−40	dBc
Spectral Input Noise Voltage	10 MHz	+25°C	V		2.4		nV/$\sqrt{\text{Hz}}$
Integrated Output Noise	100 kHz – 200 MHz	+25°C	V		32		µV
TIME DOMAIN							
Slew Rate	V_{OUT} = 5 V Step	+25°C	IV	700	1200		V/µs
Rise/Fall Time	V_{OUT} = 1 V Step	+25°C	IV		1.1	1.7	ns
	V_{OUT} = 1 V Step	T_{min} to T_{max}	IV		1.3	1.9	ns
	V_{OUT} = 5 V Step	+25°C	IV		4.2	5.7	ns
	V_{OUT} = 5 V Step	T_{min} to T_{max}	IV		5.0	6.5	ns
Overshoot Amplitude	V_{OUT} = 2 V Step	Full	IV		2	12	%
Settling Time							
To 0.1%	V_{OUT} = 2 V Step	T_{min} to +25	IV		6	10	ns
To 0.1%	V_{OUT} = 2 V Step	T_{max}	IV		7	12	ns
To 0.02%[4]	V_{OUT} = 2 V Step	T_{min} to +25	V		8		ns
To 0.02%[4]	V_{OUT} = 2 V Step	T_{max}	V		12		ns
Differential Gain	4.4 MHz	+25°C	V		0.015		%
Differential Phase	4.4 MHz	+25°C	V		0.025		Degree
SUPPLY CURRENTS							
V_{CC} ($+I_S$)	V_{CC} = +5 V	Full	II		19	26	mA
V_{EE} ($-I_S$)	V_{EE} = −5 V	Full	II		19	26	mA

NOTES
[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Output is short-circuit protected to ground, but not to supplies. Prolonged short circuit to ground may affect device reliability.
[3]Typical thermal impedances (part soldered onto board): Mini-DIP (N): θ_{JA} = 110°C/W; θ_{JC} = 30°C/W; SOIC (R): θ_{JA} = 150°C/W; θ_{JC} = 50°C/W; Cerdip (Q): θ_{JA} = 110°C/W; θ_{JC} = 20°C/W.
[4]Short-term settling with 50 Ω source impedance.

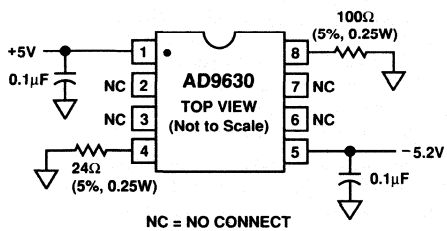
EXPLANATION OF TEST LEVELS

Test Level
I 100% Production tested.
II 100% Production tested at +25°C and sample tested at specified temperatures. AC testing of AN and AR grades done on sample basis only.
III Sample tested only.
IV Parameter is guaranteed by design and characterization testing.
V Typical value.
VI S versions are 100% production tested at temperature extremes. Other grades are sample tested at extremes.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options*
AD9630AN	−40°C to +85°C	8-Pin Plastic DIP	N-8
AD9630AR	−40°C to +85°C	8-Pin SOIC	R-8
AD9630AQ	−40°C to +85°C	8-Pin Cerdip	Q-8
AD9630 Chips	+25°C	Dice	

*For outline information see Package Information section.



AD9630 Burn-In Circuit

THEORY OF OPERATION

The AD9630 is a wide-bandwidth, closed-loop, unity-gain buffer which makes use of a new voltage-feedback architecture (Patent Pending). This architecture brings together wide bandwidth and high slew rate along with exceptional dc linearity. Most previous wide bandwidth buffers achieved their bandwidth by utilizing an open-loop topology which sacrificed both dc linearity and frequency distortion when driven into low load impedances. The design's high loop correction factor radically improves dc linearity and distortion characteristics without diminishing bandwidth. This, in combination with high slew rate, results in exceptionally low distortion over a wide frequency range.

The AD9630 is an excellent choice to drive high speed and high resolution analog-to-digital Converters. Its output stage is designed to drive high speed flash converters with minimal or no series resistance. A current booster built into the output driver helps to maintain low distortion.

Parasitic or load capacitance (>7 pF) connected directly to the AD9630 output will result in frequency peaking. A small series resistor (R_S) connected between the buffer output and capacitive load will negate this effect. Figure 1 shows the optimal value of R_S as a function of C_L to obtain the flattest frequency response. Figure 2 illustrates frequency response for various capacitive loads utilizing the recommended R_S.

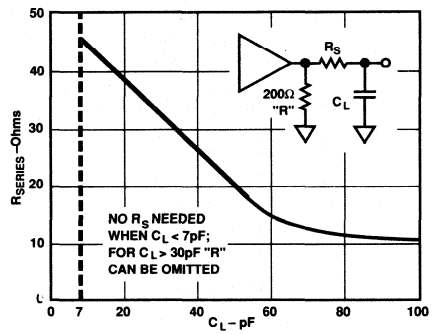


Figure 1. Recommended R_S vs. C_L

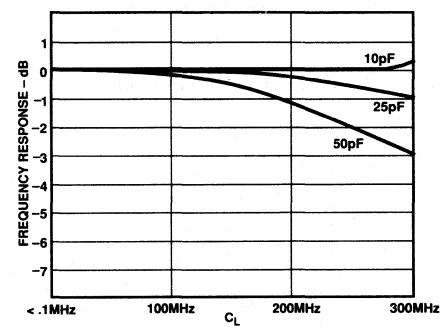


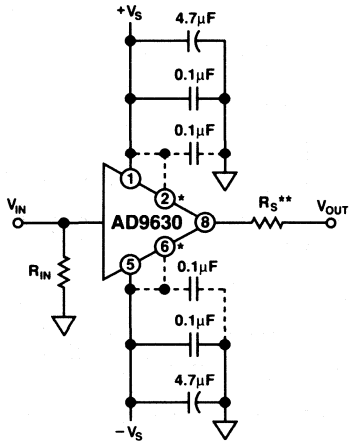
Figure 2. Frequency Response vs. C_L with Recommended R_S

In pulse mode applications, with R_S equal to approximately 12 ohms, capacitive loads of up to 50 pF can be driven with minimal settling time degradation.

The output stage has short circuit protection to ground. The output driver will shut down if more than approximately 130 mA of instantaneous sink or source current is reached. This level of current ensures that output clipping will not result when driving heavy capacitive loads during high slew conditions. Though average load currents above 70 mA may reduce device reliability.

LAYOUT CONSIDERATIONS

Due to the high frequency operation of the AD9630 attention to board layout is necessary to achieve optimum dynamic performance. A two ounce copper ground plane on the top side of the board is recommended; it should cover as much of the board as possible with appropriate openings for supply decoupling capacitors as well as for load and source termination resistors. (See Figure 3.)



*SEE PINOUTS **SEE FIGURE 1

Figure 3. AD9630 Application Circuit

Optimum settling time and ac performance results will be achieved with surface mount 0.1 µF supply decoupling ceramic chip capacitors mounted within 50 mils of the corresponding device pins with the other side soldered directly to the ground plane. For best high resolution (<0.02%) settling times, the optional power supply pins should be decoupled as shown above. If the optional power supply pins are not used, they should be left open.

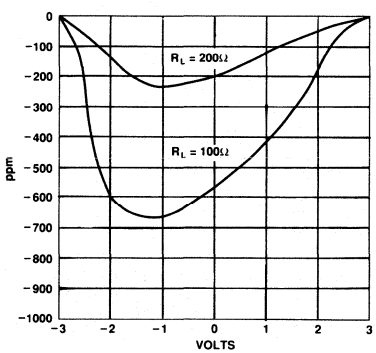
If surface mount capacitors cannot be used, radial lead ceramic capacitors with leads less than 30 mils long are recommended. Low frequency power supply decoupling is necessary and can be accomplished with 4.7 µF tantalum capacitors mounted within 0.5 inches of the supply pins. Due to the series inductance of these capacitors interacting with the 0.1 µF capacitors and power supply leads, high frequency oscillations might appear on the device output. To avoid this occurrence, the power supply leads should be tightly twisted (if appropriate). Ferrite beads mounted between the tantalum and ceramic capacitors will serve the same purpose.

All unused pins (except the optional power supply pins) should be connected to ground to reduce pin-to-pin capacitive coupling and prevent external RF interference. If the source and drive electronics require "remote" operation (> 1 inch from the AD9630), the PC board line impedances should be matched with the buffer input and output resistances. Basic micro strip techniques should be observed. R_{IN} and R_S should be connected as close to the AD9630 as possible.

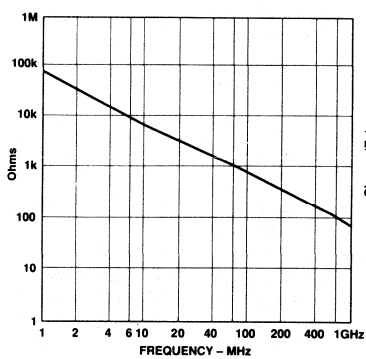
With only minimal pulse overshoot and ringing, the AD9630 can drive terminated cables directly without the use of an output termination resistor (R_S). Termination resistors (R_S and R_{IN}) can be either standard carbon composition or microwave type. For matching characteristic impedances, precision microwave resistor of 1% or better tolerance are preferred.

The AD9630 should be soldered directly to the PC board with as little vertical clearance as possible. The use of zero insertion sockets is strongly discouraged because of the high effective pin inductances. Use of this type socket will result in peaking and possibly induce oscillation. Consult the factory about the availability of an evaluation board, AD9630/PCB.

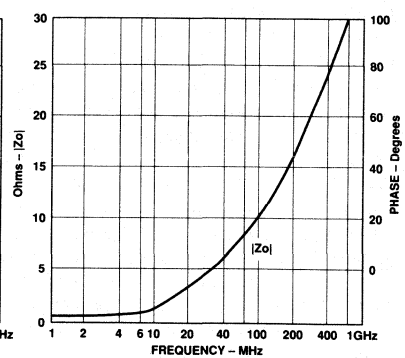
Typical Performance Curves



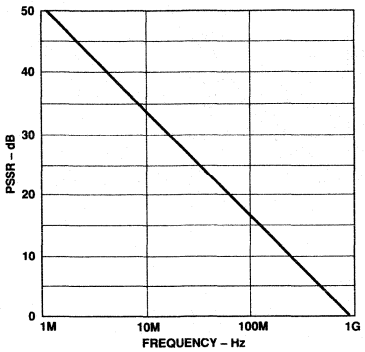
Endpoint DC Linearity Error



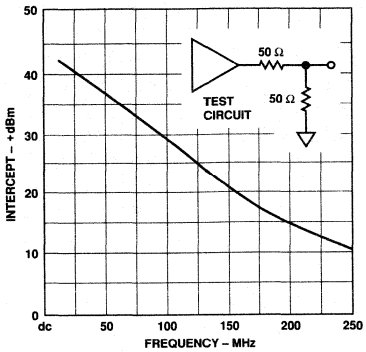
Input Impedance



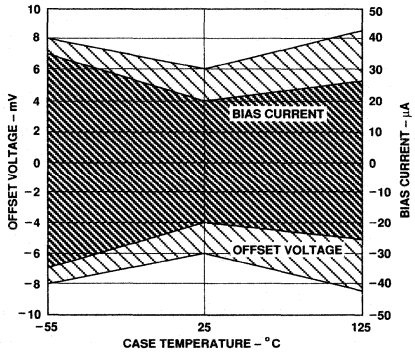
Output Impedance



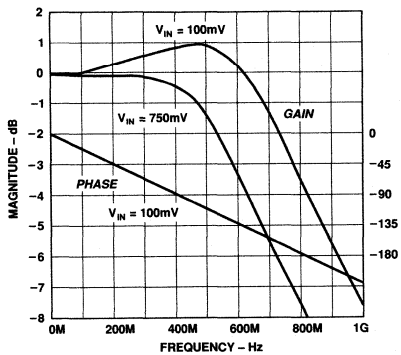
PSRR vs. Frequency



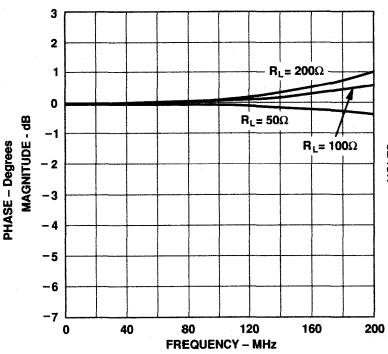
2-Tone Intermodulation Distortion



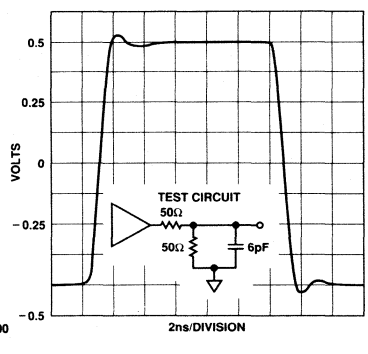
Offset Voltage and Bias Current vs. Temperature



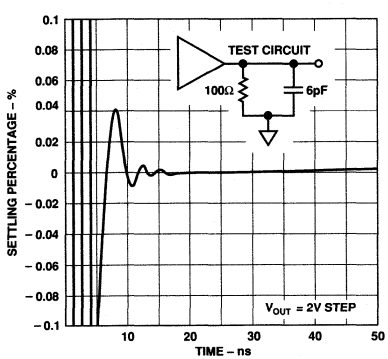
Forward Gain and Phase



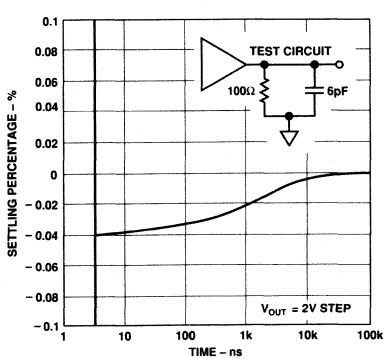
Frequency Response vs. R_{LOAD}



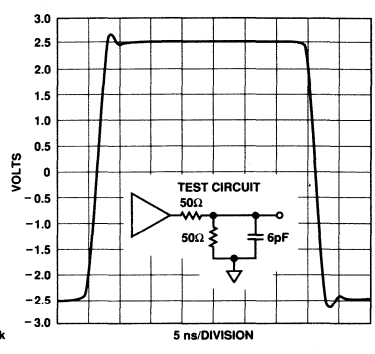
Small-Signal Pulse Response



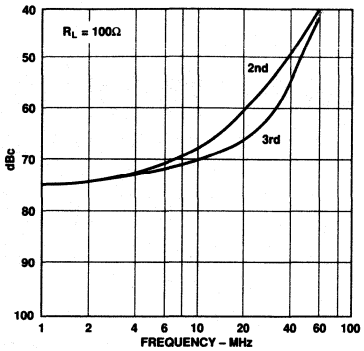
Short-Term Settling Time



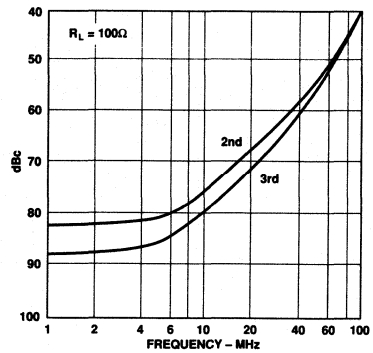
Long-Term Settling Time



Large-Signal Pulse Response



Harmonic Distortion V_{OUT} = 4 V p-p



Harmonic Distortion V_{OUT} = 2 V p-p

ANALOG DEVICES

Ultralow Offset Voltage Op Amp

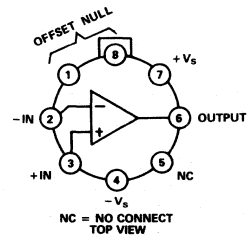
AD OP-07

FEATURES

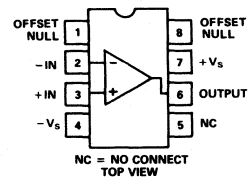
Ultralow Offset Voltage: 10μV
Ultralow Offset Voltage Drift: 0.2μV/°C
Ultrastable vs. Time: 0.2μV/°C
Ultralow Noise: 0.35μV p–p
No External Components Required
Monolithic Construction
High Common-Mode Input Range: ±14.0V
Wide Power Supply Voltage Range: ±3V to ±18V
Fits 725, 108A/308A Sockets
Military Parts and Plus Parts Available
8-Pin Plastic Mini-DIP, Cerdip, TO-99 Hermetic Metal Can, or SOIC
Available in Wafer-Trimmed Chip Form
Available in Tape and Reel in Accordance with EIA-481A Standard
Surface Mount (SOIC)

CONNECTION DIAGRAMS

TO-99 (H) Package



Plastic Mini-DIP (N), Cerdip (Q) and SOIC (R) Packages



PRODUCT DESCRIPTION

A guaranteed minimum open-loop voltage gain of 3,000,000 (AD OP-07A) represents an order of magnitude improvement over older designs; this affords increased accuracy in high closed-loop gain applications. Typical input offset voltages as low as 10μV, typical bias currents of 0.7nA, internal compensation and device protection eliminate the need for external components and adjustments. An input offset voltage temperature coefficient of 0.2μV/°C (typ) and long-term stability of 0.2μV/month (typ) eliminate recalibration or loss of initial accuracy.

A true differential operational amplifier, the AD OP-07 has a high common-mode input voltage range (±13V min) common-mode rejection ratio (typically up to 126dB) and high differential input impedance (50MΩ typ); these features combine to assure high accuracy in noninverting configurations. Such applications include instrumentation amplifiers where the increased open-loop gain maintains high linearity at high closed-loop gains.

The AD OP-07 is available in five performance grades. The AD OP-07E, AD OP-07C and AD OP-07D are specified for operation over the 0 to +70°C temperature range, while the AD OP-07A and AD OP-07 are specified for −55°C to +125°C operation. All devices are available in either the TO-99 hermetically sealed metal cans or the hermetically sealed cerdip packages, while the commercial grades are also available in plastic 8-pin mini-DIP and plastic surface mount (SOIC) packages.

PRODUCT HIGHLIGHTS

1. Increased open-loop voltage gain (3.0 million min) results in better accuracy and linearity in high closed-loop gain applications.
2. Ultralow offset voltage and offset voltage drift, combined with low input bias currents, allow the AD OP-07 to maintain high accuracy over the entire operating temperature range.
3. Internal frequency compensation, ultralow input offset voltage and full device protection eliminate the need for additional components. This reduces circuit size and complexity and increases reliability.
4. High input impedances, large common-mode input voltage range and high common-mode rejection ratio make the AD OP-07 ideal for noninverting and differential instrumentation applications.
5. Monolithic construction along with advanced circuit design and processing techniques result in low cost.
6. The input offset voltage is trimmed at the wafer stage. Unmounted chips are available for hybrid circuit applications.

AD OP-07—SPECIFICATIONS (T_A = +25°C, V_S = ±15 V, unless otherwise specified)

Model		AD OP-07E			AD OP-07C			AD OP-07D		
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
OPEN LOOP GAIN	A_{VO}	**2,000**	5,000		**1,200**	4,000		**1,200**	4,000	
		1,800	4,500		1,000	4,000		1,000	4,000	
		300	1,000		300	1,000		300	1,000	
OUTPUT CHARACTERISTICS										
Maximum Output Swing	V_{OM}	**±12.5**	±13.0		**±12.0**	±13.0		**±12.0**	±13.0	
		±12.0	±12.8		**±11.5**	±12.8		**±11.5**	±12.8	
		±10.5	±12.0			±12.0				
		±12.0	±12.6		±11.0	±12.6		±11.0	±12.6	
Open-Loop Output Resistance	R_O		60			60			60	
FREQUENCY RESPONSE										
Closed Loop Bandwidth	BW		0.6			0.6			0.6	
Slew Rate	SR		0.17			0.17			0.17	
INPUT OFFSET VOLTAGE										
Initial	V_{OS}		30	**75**		60	**150**		60	**150**
			45	130		85	250		85	250
Adjustment Range			±4			±4			±4	
Average Drift										
No External Trim	TCV_{OS}		0.3	1.3		0.5	1.8		0.7	2.5
With External Trim	TCV_{OSN}		0.3	1.3		0.4	1.6		0.7	2.5
Long Term Stability	V_{OS}/Time		0.3	1.5		0.4	2.0		0.5	3.0
INPUT OFFSET CURRENT										
Initial	I_{OS}		0.5	**3.8**		0.8	**6.0**		0.8	**6.0**
			0.9	5.3		1.6	8.0		1.6	8.0
Average Drift	TCI_{OS}		8	35		12	50		12	50
INPUT BIAS CURRENT										
Initial	I_B		±1.2	**±4.0**		±1.8	**±7.0**		±2.0	**±12**
			±1.5	±5.5		±2.2	±9.0		±3.0	±14
Average Drift	TCI_B		13	35		18	50		18	50
INPUT RESISTANCE										
Differential	R_{IN}	15	50		8	33		7	31	
Common Mode	R_{INCM}		160			120			120	
INPUT NOISE										
Voltage	e_n p-p		0.35	0.6		0.38	0.65		0.38	0.65
Voltage Density	e_n		10.3	18.0		10.5	20.0		10.5	20.0
			10.0	13.0		10.2	13.5		10.2	13.5
			9.6	11.0		9.8	11.5		9.8	11.5
Current	i_n p-p		14	30		15	35		15	35
Current Density	i_n		0.32	0.80		0.35	0.90		0.35	0.90
			0.14	0.23		0.15	0.27		0.15	0.27
			0.12	0.17		0.13	0.18		0.13	0.18
INPUT VOLTAGE RANGE										
Common Mode	CMVR	**±13.0**	±14.0		**±13.0**	±14.0		**±13.0**	±14.0	
		±13.0	±13.5		±13.0	±13.5		±13.0	±13.5	
Common-Mode Rejection Ratio	CMRR	**106**	123		**100**	120		**94**	110	
		103	123		97	120		94	106	
POWER SUPPLY										
Current, Quiescent	I_Q		3.0	**4.0**		3.5	**5.0**		3.5	**5.0**
Power Consumption	P_D		90	**120**		105	**150**		105	**150**
			6.0	**9.0**		6.0	**9.0**		6.0	**9.0**
Rejection Ratio	PSRR	**94**	107		**90**	104		**90**	104	
		90	104		86	100		86	100	
OPERATING TEMPERATURE RANGE	T_{min}, T_{max}	0		+70	0		+70	0		+70

NOTES

[1]Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. Additionally, the AD OP-07A offset voltage is guaranteed fully warmed up.

[2]Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods of time and is extrapolated from high temperature test data. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV – Parameter is not 100% tested: 90% of units meet this specification.

Specifications subject to change without notice.

AD OP-07A			AD OP-07				
Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Test Conditions**	**Units**
3,000	5,000		**2,000**	5,000		$R_L \geq 2k\Omega$, $V_O = \pm 10V$	V/mV
2,000	4,000		**1,500**	4,000		$R_L \geq 2k\Omega$, $V_O = \pm 10V$, T_{min} to T_{max}	V/mV
300	1,000		300	1,000		$R_L = 500\Omega$, $V_O = \pm 0.5V$, $V_S = \pm 3V$	V/mV
±12.5	±13.0		**±12.5**	±13.0		$R_L \geq 10k\Omega$	V
±12.0	±12.8		**±12.0**	±12.8		$R_L \geq 2k\Omega$	V
±10.5	±12.0		**±10.5**	±12.0		$R_L \geq 1k\Omega$	V
±12.0	±12.6		**±12.0**	±12.6		$R_L \geq 2k\Omega$, T_{min} to T_{max}	V
	60			60		$V_O = 0$, $I_O = 0$	Ω
	0.6			0.6		$A_{VCL} = +1.0$	MHz
	0.17			0.17		$R_L \geq 2k$	V/μs
	10	**25**		30	**75**	Note 1	μV
	25	**60**[1]		60	**200**[1]	T_{min} to T_{max}	μV
	±4			±4		$R_P = 20k\Omega$	mV
	0.2	**0.6**		0.3	**1.3**	T_{min} to T_{max}	μV/°C
	0.2	0.6		0.3	1.3	$R_P = 20k\Omega$, T_{min} to T_{max}	μV/°C
	0.2	1.0		0.2	1.0	Note 2	μV/Month
	0.3	**2.0**		0.4	**2.8**		nA
	0.8	**4.0**		1.2	**5.6**	T_{min} to T_{max}	nA
	5	25		8	50	T_{min} to T_{max}	pA/°C
	±0.7	**±2.0**		±1.0	**±3.0**		nA
	±1.0	**±4.0**		±2.0	**±6.0**	T_{min} to T_{max}	nA
	8	25		13	50	T_{min} to T_{max}	pA/°C
30	80		20	60			MΩ
	200			200			GΩ
	0.35	0.6		0.35	0.6	0.1Hz to 10Hz	μV p-p
	10.3	18.0		10.3	18.0	$f_O = 10Hz$	nV/√Hz
	10.0	13.0		10.0	13.0	$f_O = 100Hz$	nV/√Hz
	9.6	11.0		9.6	11.0	$f_O = 1kHz$	nV/√Hz
	14	30		14	30	0.1Hz to 10Hz	pA p-p
	0.32	0.80		0.32	0.80	$f_O = 10Hz$	pA/√Hz
	0.14	0.23		0.14	0.23	$f_O = 100Hz$	pA/√Hz
	0.12	0.17		0.12	0.17	$f_O = 1kHz$	pA/√Hz
±13.0	±14.0		**±13.0**	±14.0			V
±13.0	±13.5		**±13.0**	±13.5		T_{min} to T_{max}	V
110	126		**110**	126		$V_{CM} = \pm CMVR$	dB
106	123		**106**	123		$V_{CM} = \pm CMVR$, T_{min} to T_{max}	dB
	3.0	**4.0**		30	**4.0**	$V_S = \pm 15V$	mA
	90	**120**		90	**120**	$V_S = \pm 15V$	mW
	6.0	**8.4**		6.0	**8.4**	$V_S = \pm 3V$	mW
100	110		**100**	110		$V_S = \pm 3V$ to $\pm 18V$	dB
94	106		**94**	106		$V_S = \pm 3V$ to $\pm 18V$, T_{min} to T_{max}	dB
−55		+125	−55		+125		°C

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

AD OP-07

ABSOLUTE MAXIMUM RATINGS

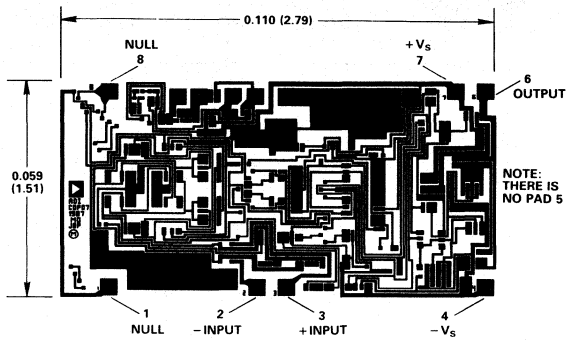
Supply Voltage . . . . . ±22V
Internal Power Dissipation (Note 1) 500mW
Differential Input Voltage . . . . . ±30V
Input Voltage . . . . . $\pm V_S$
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range
AD OP-07A, AD OP-07 . . . . . −55°C to +125°C
AD OP-07E, AD OP-07C, AD OP-07D . . . . 0 to +70°C
Lead Temperature Range (Soldering 60sec) . . . . . +300°C

NOTE
Note 1: Maximum package power dissipation vs. ambient temperature.

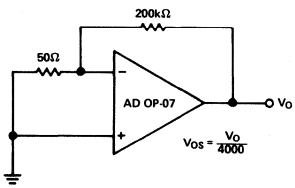
Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (H)	80°C	7.1mW/°C
Mini-DIP (N)	36°C	5.6mW/°C
Cerdip (Q)	75°C	6.7mW/°C

CHIP DIMENSIONS AND BONDING DIAGRAM

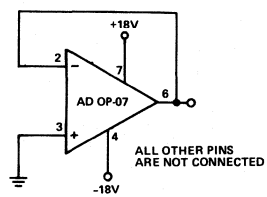
Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



THE AD OP-07 IS AVAILABLE IN WAFER-TRIMMED CHIP FORM FOR PRECISION HYBRIDS. CONSULT THE FACTORY FOR DETAILS.



Offset Voltage Test Circuit



Burn-In Circuit

ORDERING GUIDE[1]

Model	Temperature Range (°C)	Max Initial Offset (µV)	Max Offset Drift (µV/°C)	Package Description	Package Option[2]
ADOP-07EH	0 to +70	75	1.3	TO-99	H-08A
ADOP-07EN	0 to +70	75	1.3	Mini-DIP	N-8
ADOP-07EQ	0 to +70	75	1.3	Cerdip	Q-8
ADOP-07CH	0 to +70	150	1.8	TO-99	H-08A
ADOP-07CN	0 to +70	150	1.8	Mini-DIP	N-8
ADOP-07CQ	0 to +70	150	1.8	Cerdip	Q-8
ADOP-07CR	0 to +70	150	1.8	SOIC	R-8
ADOP-07CR-REEL	0 to +70	150	1.8	SOIC	
ADOP-07DH	0 to +70	150	2.5	TO-99	H-08A
ADOP-07DN	0 to +70	150	2.5	Mini-DIP	N-8
ADOP-07DQ	0 to +70	150	2.5	Cerdip	Q-8
ADOP-07AH	−55 to +125	25	0.6	TO-99	H-08A
ADOP-07AQ	−55 to +125	25	0.6	Cerdip	Q-8
ADOP-07H	−55 to +125	75	1.3	TO-99	H-08A
ADOP-07Q	−55 to +125	75	1.3	Cerdip	Q-8

NOTES
[1]A, C and D grade chips are also available.
[2]For outline information see Package Information section.

The AD OP-07 may be directly substituted for other OP-07s as well as 725, 108/208/308, 108A/208A/308A, 714, OP-05 or LM11 devices, with or without removal of external frequency compensation or offset nulling components. If used to replace 741 devices, offset nulling components must be removed (or referenced to $+V_S$). Input offset voltage of AD OP-07 is very low, but if additional nulling is required, the circuit shown in Figure 1 is recommended.

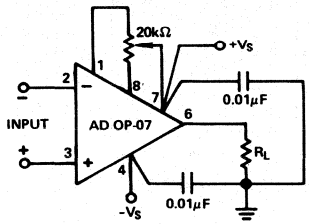


Figure 1. Optional Offset Nulling Circuit and Power Supply Bypassing

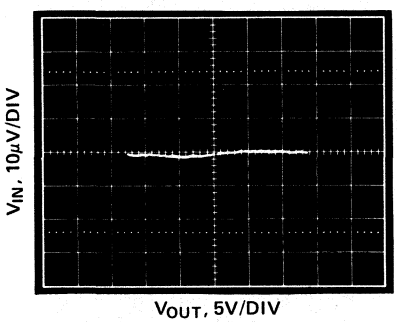
The AD OP-07 provides stable operation with load capacitances up to 500pF and ±10V swings; larger capacitances should be decoupled with 50Ω resistor.

Stray thermoelectric voltages generated by dissimilar metals (thermocouples) at the contacts to the input terminals can prevent realization of the drift performance indicated. Best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the temperature of the device's package.

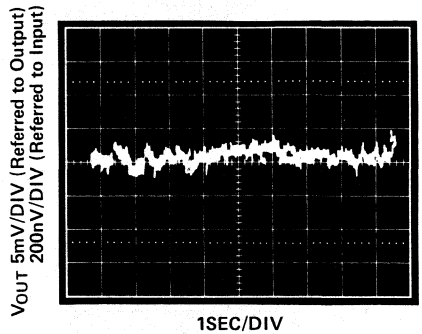
Although the AD OP-07 features high power supply rejection, the effects of noise on the power supplies may be minimized by bypassing the power supplies as close to Pins 4 and 7 of the AD OP-07 as possible, to load ground with a good-quality 0.01μF ceramic capacitor as shown in Figure 1.

2

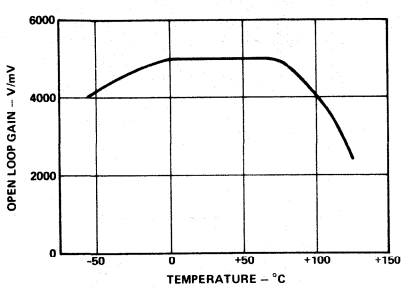
Performance Curves (typical @ T_A = +25°C, V_S = ±15V, AD OP-07 Grade Device unless otherwise noted)



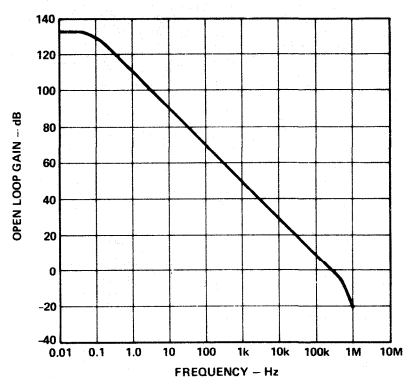
AD OP-07 Open-Loop Gain Curve



AD OP-07 Low Frequency Noise (See Test Circuit, on the Previous Page)

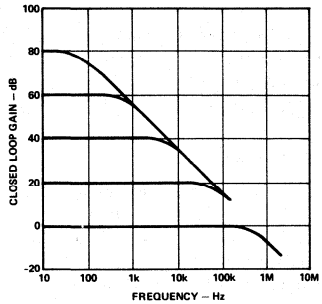


Open-Loop Gain vs. Temperature

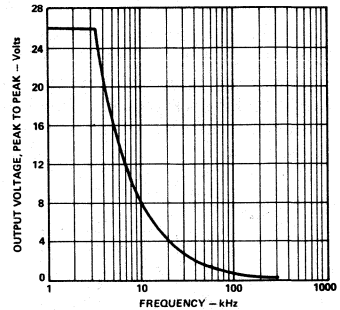


Open-Loop Frequency Response

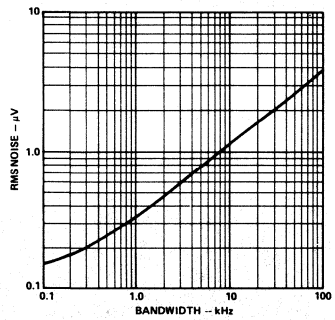
AD OP-07—Typical Performance Curves



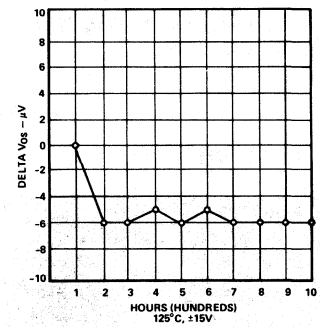
Closed-Loop Response for Various Gain Configurations



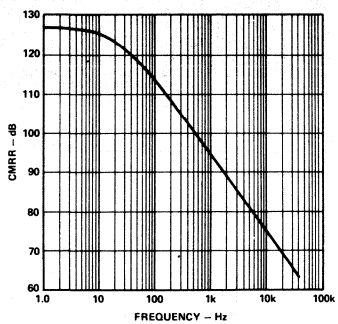
Maximum Undistorted Output vs. Frequency



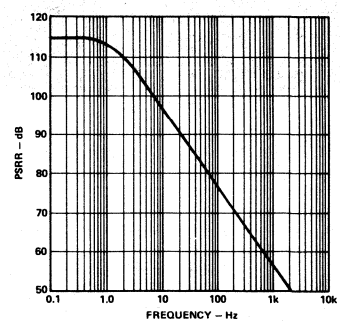
Input Wideband Noise vs. Bandwidth (0.1kHz to Frequency Indicated)



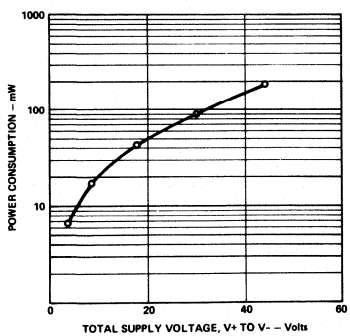
Offset Voltage vs. Time



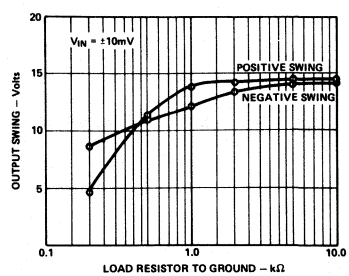
CMRR vs. Frequency



PSRR vs. Frequency



Power Consumption vs. Power Supply



Output Voltage vs. Load Resistance

ANALOG DEVICES

Ultralow Noise, Precision Op Amp

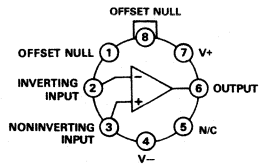
AD OP-27

FEATURES

Ultralow Noise: 80nV p-p (0.1Hz to 10Hz), 3nV/$\sqrt{Hz}$ at 1kHz
Ultralow Offset Voltage Drift: 0.2μV/°C
High Offset Stability Over Time: 0.2μV/month
High Slew Rate: 2.8V/μs
High Gain Bandwidth Product: 8MHz
Low Offset Voltage: 10μV
High CMRR: 126dB Over ±11V Input Voltage Range
Military Grade and Plus Parts Available
8-Pin Plastic Mini-DIP, Cerdip, TO-99 Hermetic Metal Can or Chip Form
Available in Chip Form

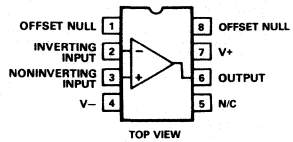
CONNECTION DIAGRAMS

TO-99
(H) Package



TOP VIEW
NOTE: PIN 4 CONNECTED TO CASE

Plastic Mini-DIP (N) Package
and
Cerdip (Q) Package



TOP VIEW

PRODUCT DESCRIPTION

The AD OP-27 offers the combined features of high precision, ultralow noise and high speed in a monolithic bipolar operational amplifier. State-of-the-art performance for high accuracy amplification of very low level signals, where inherent device noise can be the limiting factor, is attainable with the AD OP-27. As a device directly compatible with other low noise op amps, the AD OP-27 features industry standard dc performance; typical input offset voltages of 10μV and typical input offset voltage temperature coefficients of 0.2μV/°C. The super low input voltage noise performance of the AD OP-27 is characterized by an e_n p-p (typ) of 80nV (0.1Hz to 10Hz), an e_n (typ) of 3.0nV/$\sqrt{Hz}$ (at 1kHz) and a 1/f noise corner frequency of 2.7Hz. AC specifications including a 2.8V/μs (typ) slew rate and an 8MHz (typ) gain bandwidth product are possible without sacrificing dc accuracy. Long-term stability is assured by an input offset voltage drift specification of 0.2μV/month.

Source resistance related errors with the AD OP-27 are minimized by a low input bias current at ambient of ± 10nA (typ) and an input offset current of 7nA (typ). An input bias current cancellation circuit limits bias and offset currents over the extented temperature range to ± 20nA (typ) and 15nA (typ), respectively. Other factors inducing input referred errors such as power supply variations and common-mode voltages are attenuated by a PSRR and CMRR of at least 120dB.

The AD OP-27 is available in six performance grades. The AD OP-27E, AD OP-27F and AD OP-27G are specified for operation over the −25°C to +85°C temperature range, while the AD OP-27A, AD OP-27B and AD OP-27C are specified for −55°C to +125°C operation. All devices are available in either the TO-99 hermetically sealed metal cans or the hermetically sealed cerdip packages, while the E, F and G grades are also available in plastic mini-DIPs.

PRODUCT HIGHLIGHTS

1. Precision amplification of very low level, low frequency voltage inputs is enhanced by ultralow input voltage noise.
2. The AD OP-27 maintains high dc accuracy over an extended temperature range due to ultra-low offset voltage, offset voltage drift and input bias current.
3. Internal frequency compensation, factory adjusted offset voltage and full device protection eliminate the need for additional components. Circuit size and complexity are reduced while reliability is increased.
4. Long-term stability and accuracy is assured with low offset voltage drift over time.
5. Input referred errors are greatly reduced by superior common mode and power supply rejection characteristics.
6. Monolithic construction along with advanced circuit design and processing techniques result in low cost.

AD OP-27—SPECIFICATIONS ($T_A = +25°C$, $V_S = \pm 15V$, unless otherwise specified)

Model		AD OP-27G			AD OP-27F			AD OP-27E		
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
OPEN LOOP GAIN	A_{VO}	**700**	1,500		**1,000**	1,800		**1,000**	1,800	
		400	1,500		**800**	1,500		**800**	1,500	
		200	500		250	700		250	700	
		450	1,000		700	1,300		750	1,500	
OUTPUT CHARACTERISTICS										
Voltage Swing	V_O	**±11.5**	±13.5		**±12.0**	±13.8		**±12.0**	±13.8	
		±10.0	±11.5		**±10.0**	±11.5		**±10.0**	±11.5	
		±11.0	±13.3		±11.4	±13.5		±11.7	±13.6	
Open-Loop Output Resistance	R_O		70			70			70	
FREQUENCY RESPONSE										
Gain Bandwidth Product	GBW	5.0	8.0		5.0	8.0		5.0	8.0	
Slew Rate	SR	1.7	2.8		1.7	2.8		1.7	2.8	
INPUT OFFSET VOLTAGE										
Initial	V_{OS}		30	**100**		20	**60**		10	**25**
			55	220		40	140		20	**60**
Average Drift	TCV_{OS}		0.4	1.8		0.3	1.3		0.2	**0.6**
Long Term Stability	V_{OS}/Time		0.4	2.0		0.3	1.5		0.2	1.0
Adjustment Range			±4.0			±4.0			±4.0	
INPUT BIAS CURRENT										
Initial	I_B		±15	**±80**		±12	**±55**		±10	**±40**
			±25	±150		±18	±95		±14	±60
INPUT OFFSET CURRENT										
Initial	I_{OS}		12	**75**		9	**50**		7	**35**
			20	135		14	85		10	50
INPUT NOISE										
Voltage	e_n p-p		0.09	0.25		0.08	0.18		0.08	0.18
Voltage Density	e_n		3.8	8.0		3.5	5.5		3.5	5.5
			3.3	5.6		3.1	4.5		3.1	4.5
			3.2	4.5		3.0	3.8		3.0	3.8
Current Density	i_n		1.7	–		1.7	4.0		1.7	4.0
			1.0	–		1.0	2.3		1.0	2.3
			0.4	0.6		0.4	0.6		0.4	0.6
INPUT VOLTAGE RANGE										
Common Mode	CMVR	**±11.0**	±12.3		**±11.0**	±12.3		**±11.0**	±12.3	
		±10.5	±11.8		±10.5	±11.8		±10.5	±11.8	
Common-Mode Rejection Ratio	CMRR	**100**	120		**106**	123		**114**	126	
		96	118		102	121		110	124	
INPUT RESISTANCE										
Differential	R_{IN}	0.8	4		1.2	5		1.5	6	
Common Mode	R_{INCM}		2			2.5			3	
POWER SUPPLY										
Rated Performance			±15			±15			±15	
Operating			±(4–18)			±(4–18)			±(4–18)	
Current, Quiescent	I_Q		3.3	**5.6**		3.0	**4.6**		3.0	**4.6**
Rejection	PSR		2	**20**		1	**10**		1	**10**
			2	32		2	16		2	15
Power Consumption	P_d		100	**170**		90	**140**		90	**140**
OPERATING TEMPERATURE RANGE	T_{min}, T_{max}	−25		+85	−25		+85	−25		+85

NOTES

[1]Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A and E grades are guaranteed fully warmed up.

[2]Long-Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. time after the first 30 days.

Specifications subject to change without notice.

AD OP-27C			AD OP-27B			AD OP-27A			Conditions	Units
Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**		
700	1,500		**1,000**	1,800		**1,000**	1,800		$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	V/mV
400	1,500		**800**	1,500		**800**	1,500		$R_L \geq 1k\Omega$, $V_{OUT} = \pm 10V$	V/mV
200	500		250	700		250	700		$R_L = 600\Omega$, $V_{OUT} = \pm 1V$, $V_S = \pm 4V$	V/mV
300	800		**500**	1,000		**600**	1,200		$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$, T_a = min to max	V/mV
±11.5	±13.5		**±12.0**	±13.8		**±12.0**	±13.8		$R_L \geq 2k\Omega$	V
±10.0	±11.5		**±10.0**	±11.5		**±10.0**	±11.5		$R_L \geq 600\Omega$	V
±10.5	±13.0		**±11.0**	±13.2		**±11.5**	±13.5		$R_L \geq 2k\Omega$, T_a = min to max	V
	70			70			70		$I_{OUT} = 0A$, $V_{OUT} = 0V$	Ω
5.0	8.0		5.0	8.0		5.0	8.0			MHz
1.7	2.8		1.7	2.8		1.7	2.8		$R_L \geq 2k\Omega$	V/μs
	30	**100**		20	**60**		10	**25**	(Note 1)	μV
	70	**300**		50	**200**		30	**60**	T_a = min to max	μV
	0.4	1.8		0.3	1.3		0.2	**0.6**	T_a = min to max	μV/°C
	0.4	2.0		0.3	1.5		0.2	1.0	(Note 2)	μV/month
	±4.0			±4.0			±4.0		$R_p = 10k\Omega$	mV
	±15	**±80**		±12	**±55**		±10	**±40**		nA
	±35	**±150**		±28	**±95**		±20	**±60**	T_a = min to max	nA
	12	**75**		9	**50**		7	**35**		nA
	30	**135**		22	**85**		15	**50**	T_a = min to max	nA
	0.09	0.25		0.08	0.18		0.08	0.18	0.1Hz to 10Hz	μV p-p
	3.8	8.0		3.5	5.5		3.5	5.5	$f_o = 10Hz$	$nV/\sqrt{Hz}$
	3.3	5.6		3.1	4.5		3.1	4.5	$f_o = 30Hz$	$nV/\sqrt{Hz}$
	3.2	4.5		3.0	3.8		3.0	3.8	$f_o = 1000Hz$	$nV/\sqrt{Hz}$
	1.7	–		1.7	4.0		1.7	4.0	$f_o = 10Hz$	$pA/\sqrt{Hz}$
	1.0	–		1.0	2.3		1.0	2.3	$f_o = 30Hz$	$pA/\sqrt{Hz}$
	0.4	0.6		0.4	0.6		0.4	0.6	$f_o = 1000Hz$	$pA/\sqrt{Hz}$
±11.0	±12.3		**±11.0**	±12.3		**±11.0**	±12.3			V
±10.2	±11.5		±10.3	±11.5		±10.3	±11.5		T_a = min to max	V
100	120		**106**	123		**114**	126		$V_{CM} = \pm 11V$	dB
94	116		**100**	119		**108**	122		$V_{CM} = \pm 10V$, T_a = min to max	dB
0.8	4		1.2	5		1.5	6			MΩ
	2			2.5			3			GΩ
	±15			±15			±15			V
	±(4–18)			±(4–18)			±(4–18)			V
	3.3	**5.6**		3.0	**4.6**		3.0	**4.6**	$V_S = \pm 15V$	mA
	2	**20**		1	**10**		1	**10**	$V_S = \pm 4V$ to $\pm 18V$	μV/V
	4	**51**		2	**20**		2	**16**	$V_S = \pm 4.5V$ to $\pm 18V$, T_a = min to max	μV/V
	100	**170**		90	**140**		90	**140**	$V_{OUT} = 0V$	mW
−55		+125	−55		+125	−55		+125		°C

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±18V
Internal Power Dissipation (Note 1) 500mW
Input Voltage . . . . . ±V_S
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage (Note 2) . . . . . ±0.7V
Differential Input Current (Note 2) . . . . . ±25mA
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range
AD OP-27A, AD OP-27B, AD OP-27C . −55°C to +125°C
AD OP-27E, AD OP-27F, AD OP-27G . −25°C to +85°C
Lead Temperature Range (Soldering 60sec) . . . . . 300°C

NOTES:
Note 1: Maximum package power dissipation vs. ambient temperature.

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (H)	80°C	7.1mW/°C
Mini-DIP (N)	36°C	5.6mW/°C
Cerdip (Q)	75°C	6.7mW/°C

Note 2: The AD OP-27's inputs are protected by back-to-back diodes. To achieve low noise current limiting resistors could not be used. If the differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

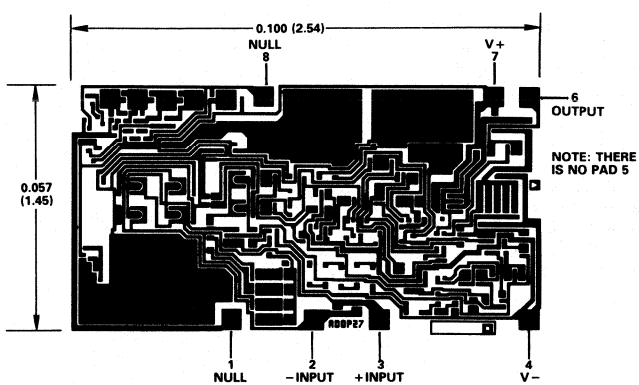
ORDERING GUIDE

Model	Package Description	Temperature Range (°C)	Max Initial Offset (µV)	Max Offset Drift (µV/°C)	Package Option*
ADOP-27GH	TO-99	−25 to +85	100	1.8	H-08A
ADOP-27GN	Mini-DIP	−25 to +85	100	1.8	N-8
ADOP-27GQ	Cerdip	−25 to +85	100	1.8	Q-8
ADOP-27FH	TO-99	−25 to +85	60	1.3	H-08A
ADOP-27FN	Mini-DIP	−25 to +85	60	1.3	N-8
ADOP-27FQ	Cerdip	−25 to +85	60	1.3	Q-8
ADOP-27EH	TO-99	−25 to +85	25	0.6	H-08A
ADOP-27EN	Mini-DIP	−25 to +85	25	0.6	N-8
ADOP-27EQ	Cerdip	−25 to +85	25	0.6	Q-8
ADOP-27CH	TO-99	−55 to +125	100	1.8	H-08A
ADOP-27CQ	Cerdip	−55 to +125	100	1.8	Q-8
ADOP-27BH	TO-99	−55 to +125	60	1.3	H-08A
ADOP-27BQ	Cerdip	−55 to +125	60	1.3	Q-8
ADOP-27AH	TO-99	−55 to +125	25	0.6	H-08A
ADOP-27AQ	Cerdip	−55 to +125	25	0.6	Q-8
ADOP-27A Chips	Die	−55 to +125	25	0.6	
ADOP-27C Chips	Die	−55 to +125	100	1.8	
ADOP-27G Chips	Die	−25 to +85	100	1.8	

*For outline information see Package Information section.

CHIP DIMENSIONS AND BONDING DIAGRAM

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



APPLICATION NOTES FOR THE AD OP-27

The AD OP-27 can be used in the sockets of many of the popular precision bipolar input operational amplifiers on the market. Elimination of external frequency compensation or nulling circuitry may be possible in many cases. In 741 replacement situations, if nulling has been implemented, it should be modified or removed for optimum AD OP-27 performance.

In applications where the initial factory adjusted input offset voltage provides insufficient accuracy, further offset trimming can be accomplished with the resistor network shown in Figure 1. The adjustment range attainable using a 10kΩ potentiometer will be ±4mV. If a smaller adjustment range is required, the sensitivity of the nulling can be increased by using a smaller potentiometer in series with fixed resistor(s). For example, a 1kΩ pot in series with two 4.7kΩ resistors will yield a ±280μV range.

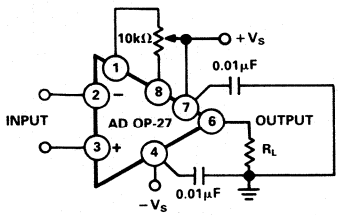


Figure 1. Optional Offset Nulling Circuit and Power Supply Bypassing

Zeroing the initial offset with potentiometers other than 10kΩ, but between 1kΩ and 1MΩ, will introduce an additional input offset voltage temperature drift error of from 0.1 to 0.2μV/°C. Additionally, by intentionally trimming in a dc level shift a voltage dependent offset drift will be created. It will be approximately the input offset voltage at 25°C divided by 300 (in μV/°C).

Parasitic thermocouple EMF's can be generated where dissimilar metals meet the contacts to the input terminals of the AD OP-27. These temperature dependent voltages can manifest themselves as drift type errors. Optimized temperature performance will be obtained when both contacts are maintained at the same temperature—a temperature close to the device's package.

Output stability with the AD OP-27 is possible with capacitive loads of up to 2000pF and ±10V output swings. Larger capacitances should be decoupled with a 50Ω resistor.

High closed loop gain and excellent linearity can be achieved by operating the AD OP-27 within an output current range of ±10mA. Minimizing output current will provide the highest linearity.

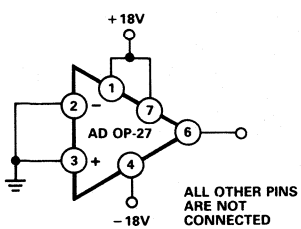


Figure 2. Burn-In Circuit

SLEW RATE DISCUSSION

In unity gain buffer applications with feedback resistances of less than 100Ω where the input is driven with a fast, large (greater than 1V) pulse, the output waveform will appear as in Figure 3.

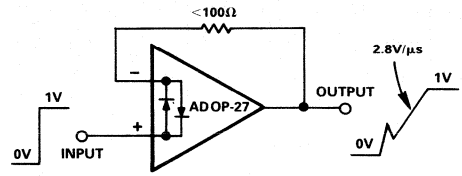


Figure 3. Unity Gain Buffer/Pulsed Operation

During the initial portion of the output slew the input protection back-to-back diodes effectively short the output to the input. A current limited only by the output short circuit protection will be drawn from the source. After the input diodes saturate, the amplifier will slew at its nominal 2.8V/μs. With feedback resistances of more than 500Ω the output is capable of handling the current requirements without limiting (less than 20mA at 10V) and the amplifier will stay in the linear region.

As with all operational amplifiers a feedback resistance of greater than 2kΩ will create a pole with the input capacitance (8pF). Additional phase shift will be introduced and the phase margin will be reduced. A small capacitor (20 to 50pF) in parallel with the feedback resistor will alleviate this problem.

CAUTION: NOISE MEASUREMENTS

Precise measurement of the extremely low input noise associated with the AD OP-27 is a difficult task. In order to observe the rated noise in the 0.1Hz to 10Hz frequency range the following cautions should be exercised.

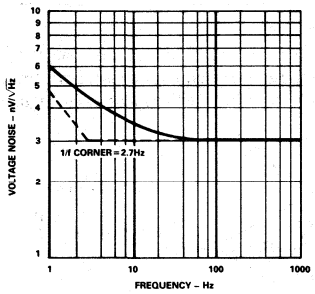
(1) The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds. As shown in the noise test frequency response plot in this data sheet the 0.1Hz corner is only defined by a single zero. A test time of 10 seconds acts as an additional zero to eliminate noise contributions from frequencies lower than 0.1Hz.

(2) Warm-up for a least five minutes will eliminate temperature induced effects. During the first few minutes the offset voltage typically increases 4μV. In a 10 second measurement interval prior to temperature stabilization the reading could include several nanovolts of warm-up offset error in addition to the noise.

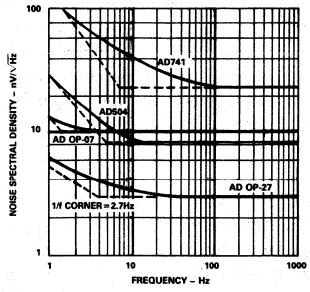
(3) For reasons similar to (2) the device under test should be well shielded from air currents or other heat sinks to eliminate the possibility of temperature changes over time invalidating the measurements. Sudden motion in the vicinity or physical contact with the package can also increase the observed noise.

An input voltage noise spectral density test is recommended when measuring noise on a large number of units. Because the 1/f noise corner frequency is around 3Hz, a 1kHz noise voltage density measurement combined with a 0.1Hz to 10Hz peak-to-peak noise reading will guarantee 1/f and white noise performance over the rated frequency spectrum.

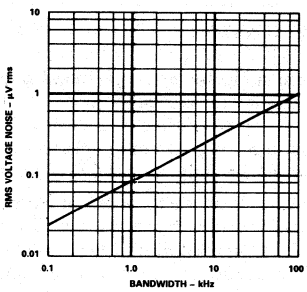
AD OP-27—Typical Performance Curves (@ T_A = +25°C, V_S = ±15V)



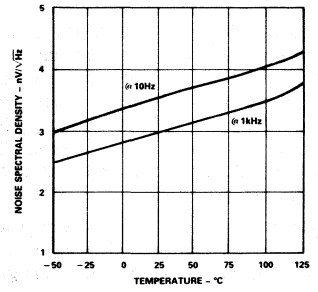
Input Voltage Noise Spectral Density



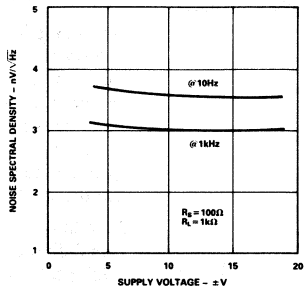
Comparison of Op Amp Input Voltage Noise Spectrums



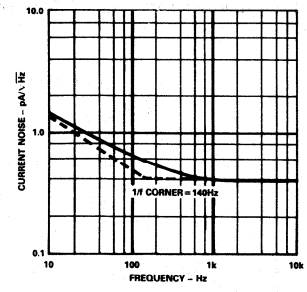
Input Wideband Noise vs. Bandwidth (0.1Hz to Frequency Indicated)



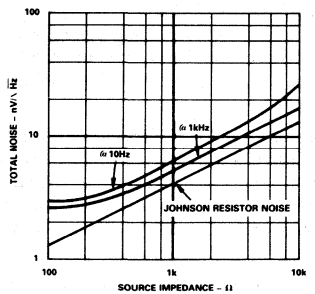
Input Voltage Noise vs. Temperature



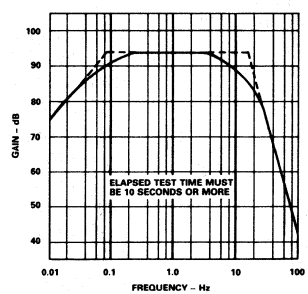
Input Voltage Noise vs. Supply Voltage



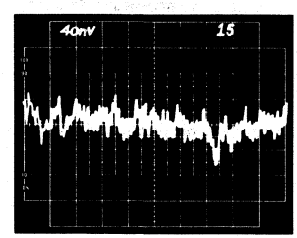
Input Current Noise Spectral Density



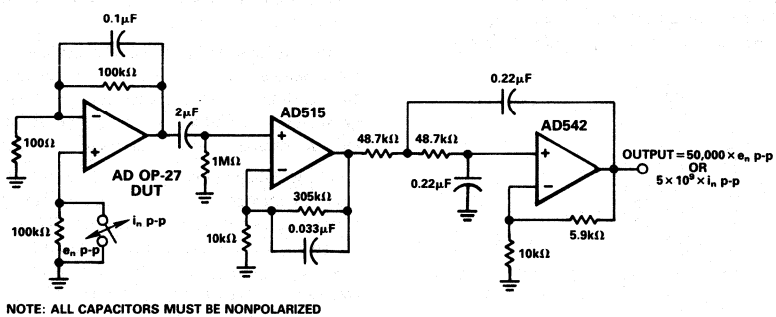
Total Noise vs. Source Impedance



0.1Hz to 10Hz Noise Test Frequency Response

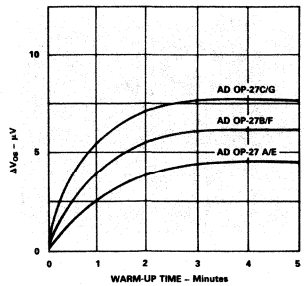


0.1Hz to 10Hz p-p Voltage Noise

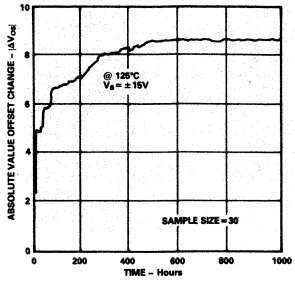


NOTE: ALL CAPACITORS MUST BE NONPOLARIZED

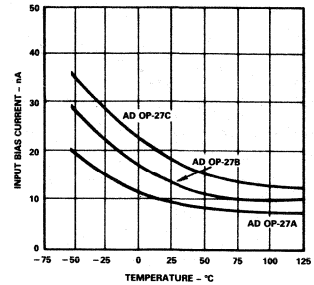
0.1Hz to 10Hz Noise Test Bandpass Filter (Voltage Gain = 50,000)



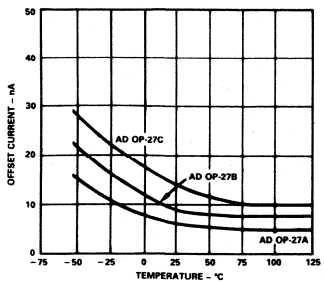
Input Offset Voltage Turn-On Drift vs. Warm-Up Time



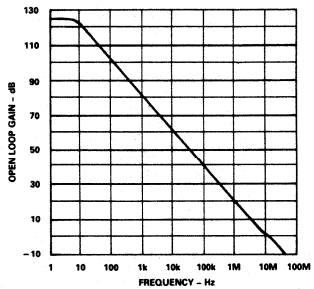
Long Term Offset Stability @ Temperature



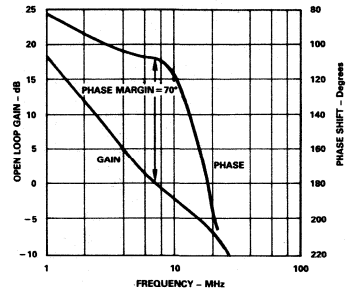
Input Bias Current vs. Temperature



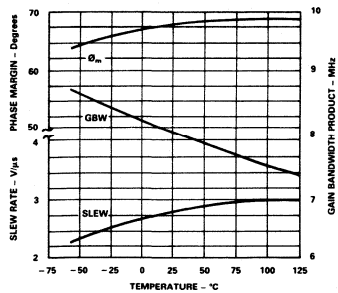
Input Offset Current vs. Temperature



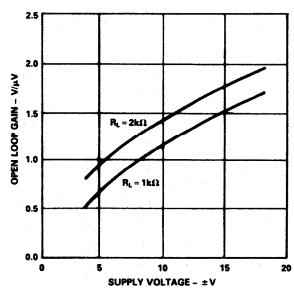
Open Loop Frequency Response



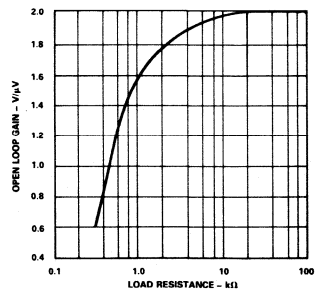
Open Loop Gain and Phase Shift vs. Frequency



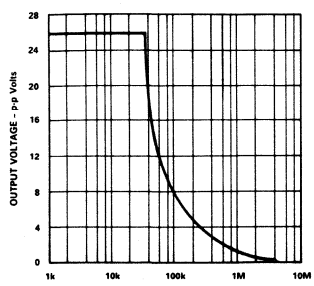
Slew Rate, Gain Bandwidth Product and Phase Margin vs. Temperature



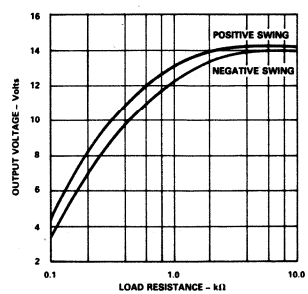
Open Loop Gain vs. Supply Voltage



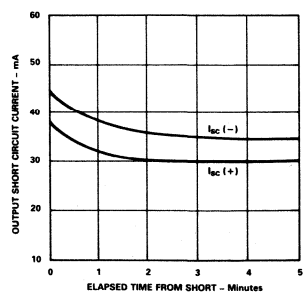
Open Loop Gain vs. Load Resistance



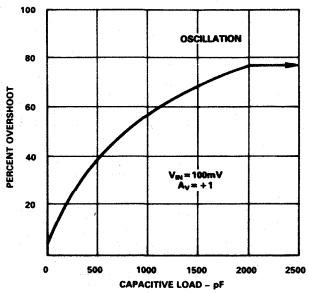
Undistorted Output Swing vs. Frequency



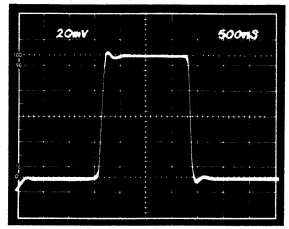
Output Swing vs. Load Resistance



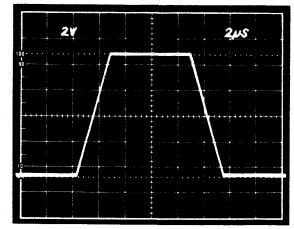
Output Short Circuit Current vs. Time



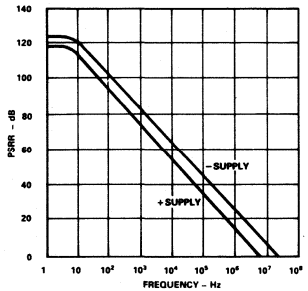
Small Signal Overshoot vs. Capacitive Load



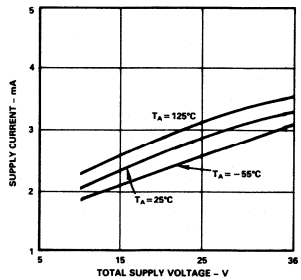
Unity Gain Follower Pulse Response (Small Signal)



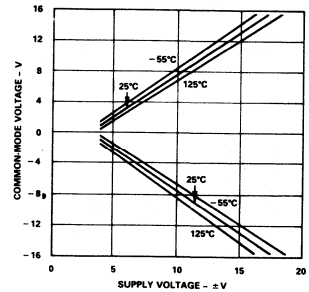
Unity Gain Follower Pulse Response (Large Signal)



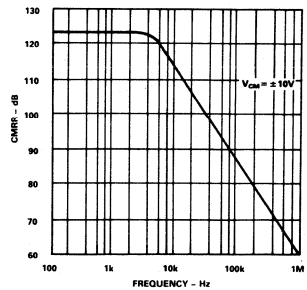
Power Supply Rejection Ratio vs. Frequency



Supply Current vs. Supply Voltage



Common-Mode Input Range vs. Supply Voltage



CMRR vs. Frequency

ANALOG DEVICES

Ultralow Noise, High Speed, Precision Op Amp ($A_{VCL} \geq 5$)

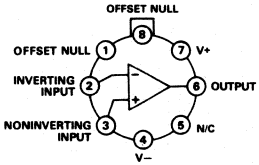
AD OP-37

FEATURES

Ultralow Noise: 80nV p–p (0.1Hz to 10Hz), 3nV/$\sqrt{Hz}$ at 1kHz
High Speed: 17V/μs
High Gain Bandwidth Product: 63MHz
Ultralow Offset Voltage Drift: 0.2μV/°C
High Offset Stability Over Time: 0.2μV/month
Low Offset Voltage: 10μV
High CMRR: 126dB Over ±11V Input Voltage Range
Military Grade and Plus Parts Available
8-Pin Plastic Mini-DIP, Cerdip or TO-99 Hermetic Metal Can
Available in Chip Form

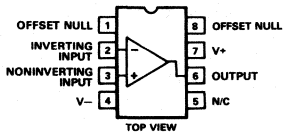
CONNECTION DIAGRAMS

TO-99 (H) Package



NOTE: PIN 4 CONNECTED TO CASE
TOP VIEW

Plastic Mini-DIP (N) Package and Cerdip (Q) Package



TOP VIEW

PRODUCT DESCRIPTION

The AD OP-37 offers the combined features of high precision, ultralow noise and high speed in a monolithic bipolar operational amplifier. High speed, accurate amplification of very low level signals, where inherent device noise can be the limiting factor, is attainable with the AD OP-37 in applications requiring gains greater than or equal to five. This instrumenation grade op amp features industry standard dc performance; typical input offset voltages of 10μV and typical input offset voltage temperature coefficients of 0.2μV/°C. The super low input voltage noise performance of the AD OP-37 is characterized by an e_n p-p (typ) of 80nV (0.1Hz to 10Hz), an e_n (typ) of 3.0nV/$\sqrt{Hz}$ (at 1kHz) and a 1/f noise corner frequency of 2.7Hz. High speed performance is assured by a typical 17V/μs slew rate and a typical 63MHz gain bandwidth product. Long-term stability is guaranteed by an input offset voltage drift specification of 0.2μV/month.

Source resistance related input errors with the AD OP-37 are minimized by a low input bias current of ±10nA (typ) and an input offset current of 7nA (typ). An input bias current cancellation circuit restricts bias and offset currents over the extended temperature range to ±20nA (typ) and 15nA (typ), respectively.

Other factors inducing input referred errors such as power supply variations and common-mode voltages are attenuated by a PSRR and CMRR of 120dB.

The AD OP-37 is available in six performance grades. The AD OP-37E, AD OP-37F and AD OP-37G are specified for operation over the extended commercial temperature range of −25°C to +85°C, while the AD OP-37A, AD OP-37B and AD OP-37C are specified for −55°C to +125°C operation. All devices are available in either the TO-99 hermetically sealed metal cans or the hermetically sealed cerdip packages, while the commercial grades are also available in plastic mini-DIPs.

PRODUCT HIGHLIGHTS

1. High speed accurate amplification (gains ≥ 5) of very low level low frequency voltage inputs is enhanced by a high gain bandwidth product and ultralow input voltage noise.
2. The AD OP-37 maintains high dc accuracy over an extended temperature range due to ultralow offset voltage, offset voltage drift and input bias current.
3. Internal frequency compensation, factory adjusted offset voltage and full device protection eliminate the need for additional components. Circuit size and complexity are reduced while reliability is increased.
4. Long-term stability and accuracy is assured with low offset voltage drift over time.
5. Input referred errors are greatly reduced by superior common-mode and power supply rejection characteristics.
6. Monolithic construction along with advanced circuit design and processing techniques result in low cost.

AD OP-37—SPECIFICATIONS (T_A = +25°C, V_S = ±15V, unless otherwise specified)

Model		AD OP-37G			AD OP-37F			AD OP-37E		
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
OPEN LOOP GAIN	A_{VO}	**700**	1,500		**1,000**	1,800		**1,000**	1,800	
		400	1,500		**800**	1,500		**800**	1,500	
		200	500		250	700		250	700	
		450	1,000		700	1,300		750	1,500	
OUTPUT CHARACTERISTICS										
Voltage Swing	V_O	**±11.5**	±13.5		**±12.0**	±13.8		**±12.0**	±13.8	
		±10.0	±11.5		**±10.0**	±11.5		**±10.0**	±11.5	
		±11.0	±13.3		±11.4	±13.5		±11.7	±13.6	
Open-Loop Output Resistance	R_O		70			70			70	
FREQUENCY RESPONSE										
Gain Bandwidth Product	GBW	45	63		45	63		45	63	
		–	40		–	40		–	40	
Slew Rate	SR	11	17		11	17		11	17	
INPUT OFFSET VOLTAGE										
Initial	V_{OS}		30	**100**		20	**60**		10	**25**
			55	220		40	140		20	**60**
Average Drift	TCV_{OS}		0.4	1.8		0.3	1.3		0.2	**0.6**
Long-Term Stability	V_{OS}/Time		0.4	2.0		0.3	1.5		0.2	1.0
Adjustment Range			±4.0			±4.0			±4.0	
INPUT BIAS CURRENT										
Initial	I_B		±15	**±80**		±12	**±55**		±10	**±40**
			±25	±150		±18	±95		±14	±60
INPUT OFFSET CURRENT										
Initial	I_{OS}		12	**75**		9	**50**		7	**35**
			20	135		14	85		10	50
INPUT NOISE										
Voltage	e_n p-p		0.09	0.25		0.08	0.18		0.08	0.18
Voltage Density	e_n		3.8	8.0		3.5	5.5		3.5	5.5
			3.3	5.6		3.1	4.5		3.1	4.5
			3.2	4.5		3.0	3.8		3.0	3.8
Current Density	i_n		1.7	–		1.7	4.0		1.7	4.0
			1.0	–		1.0	2.3		1.0	2.3
			0.4	0.6		0.4	0.6		0.4	0.6
INPUT VOLTAGE RANGE										
Common Mode	CMVR	**±11.0**	±12.3		**±11.0**	±12.3		**±11.0**	±12.3	
		±10.5	±11.8		±10.5	±11.8		±10.5	±11.8	
Common-Mode Rejection Ratio	CMRR	**100**	120		**106**	123		**114**	126	
		96	118		102	121		110	124	
INPUT RESISTANCE										
Differential	R_{IN}	0.8	4		1.2	5		1.5	6	
Common Mode	R_{INCM}		2			2.5			3	
POWER SUPPLY										
Rated Performance			±15			±15			±15	
Operating			±(4–18)			±(4–18)			±(4–18)	
Current, Quiescent	I_Q		3.3	**5.6**		3.0	**4.6**		3.0	**4.6**
Rejection	PSR		2	**20**		1	**10**		1	**10**
			2	32		2	16		2	15
Power Consumption	P_d		100	**170**		90	**140**		90	**140**
OPERATING TEMPERATURE RANGE	T_{min}, T_{max}	−25		+85	−25		+85	−25		+85

NOTES

[1]Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A and E grades are guaranteed fully warmed up.

[2]Long-Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. time after the first 30 days.

Specifications subject to change without notice.

AD OP-37C			AD OP-37B			AD OP-37A			Conditions	Units
Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**		
700	1,500		**1,000**	1,800		**1,000**	1,800		$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	V/mV
400	1,500		**800**	1,500		**800**	1,500		$R_L \geq 1k\Omega$, $V_{OUT} = \pm 10V$	V/mV
200	500		250	700		250	700		$R_L = 600\Omega$, $V_{OUT} = \pm 1V$, $V_S = \pm 4V$	V/mV
300	800		**500**	1,000		**600**	1,200		$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$, T_a = min to max	V/mV
±11.5	±13.5		**±12.0**	±13.8		**±12.0**	±13.8		$R_L \geq 2k\Omega$	V
±10.0	±11.5		**±10.0**	±11.5		**±10.0**	±11.5		$R_L \geq 600\Omega$	V
±10.5	±13.0		**±11.0**	±13.2		**±11.5**	±13.5		$R_L \geq 2k\Omega$, T_a = min to max	V
	70			70			70		$I_{OUT} = 0A$, $V_{OUT} = 0V$	Ω
45	63		45	63		45	63		$f_o = 10kHz$	MHz
–	63		–	40		–	40		$f_o = 1MHz$	MHz
11	17		11	17		11	17		$R_L \geq 2k\Omega$	V/μs
	30	**100**		20	**60**		10	**25**	(Note 1)	μV
	70	**300**		50	**200**		30	**60**	T_a = min to max	μV
	0.4	1.8		0.3	1.3		0.2	**0.6**	T_a = min to max	μV/°C
	0.4	2.0		0.3	1.5		0.2	1.0	(Note 2)	μV/month
	±4.0			±4.0			±4.0		$R_p = 10k\Omega$	mV
	±15	**±80**		±12	**±55**		±10	**±40**		nA
	±35	**±150**		±28	**±95**		±20	**±60**	T_a = min to max	nA
	12	**75**		9	**50**		7	**35**		nA
	30	**135**		22	**85**		15	**50**	T_a = min to max	nA
	0.09	0.25		0.08	0.18		0.08	0.18	0.1Hz to 10Hz	μV p-p
	3.8	8.0		3.5	5.5		3.5	5.5	$f_o = 10Hz$	$nV/\sqrt{Hz}$
	3.3	5.6		3.1	4.5		3.1	4.5	$f_o = 30Hz$	$nV/\sqrt{Hz}$
	3.2	4.5		3.0	3.8		3.0	3.8	$f_o = 1000Hz$	$nV/\sqrt{Hz}$
	1.7	–		1.7	4.0		1.7	4.0	$f_o = 10Hz$	$pA/\sqrt{Hz}$
	1.0	–		1.0	2.3		1.0	2.3	$f_o = 30Hz$	$pA/\sqrt{Hz}$
	0.4	0.6		0.4	0.6		0.4	0.6	$f_o = 1000Hz$	$pA/\sqrt{Hz}$
±11.0	±12.3		**±11.0**	±12.3		**±11.0**	±12.3			V
±10.2	±11.5		±10.3	±11.5		±10.3	±11.5		T_a = min to max	V
100	120		**106**	123		**114**	126		$V_{CM} = \pm 11V$	dB
94	116		**100**	119		**108**	122		$V_{CM} = \pm 10V$, T_a = min to max	dB
0.8	4		1.2	5		1.5	6			MΩ
	2			2.5			3			GΩ
	±15			±15			±15			V
	±(4–18)			±(4–18)			±(4–18)			V
	3.3	**5.6**		3.0	**4.6**		3.0	**4.6**	$V_S = \pm 15V$	mA
	2	**20**		1	**10**		1	**10**	$V_S = \pm 4V$ to $\pm 18V$	μV/V
	4	**51**		2	**20**		2	**16**	$V_S = \pm 4.5V$ to $\pm 18V$, T_a = min to max	μV/V
	100	**170**		90	**140**		90	**140**	$V_{OUT} = 0V$	mW
−55		+125	−55		+125	−55		+125		°C

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±18V
Internal Power Dissipation (Note 1) 500mW
Input Voltage . . . . . $\pm V_S$
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage (Note 2) . . . . . ±0.7V
Differential Input Current (Note 2) . . . . . ±25mA
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range
AD OP-37A, AD OP-37B, AD OP-37C . −55°C to +125°C
AD OP-37E, AD OP-37F, AD OP-37G . −25°C to +85°C
Lead Temperature Range (Soldering 60sec) . . . . . 300°C

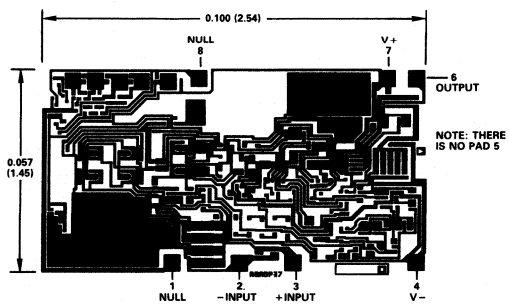
NOTES:
Note 1: Maximum package power dissipation vs. ambient temperature.

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (H)	80°C	7.1mW/°C
Mini-DIP (N)	36°C	5.6mW/°C
Cerdip (Q)	75°C	6.7mW/°C

Note 2: The AD OP-37's inputs are protected by back-to-back diodes. To achieve low noise current limiting resistors could not be used. If the differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

CHIP DIMENSIONS AND BONDING DIAGRAM

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



THE AD OP-37 IS AVAILABLE IN WAFER-TRIMMED CHIP FORM. CONSULT THE FACTORY FOR DETAILS.

ORDERING GUIDE

Model	Package Description	Temperature Range (°C)	Max Initial Offset (μV)	Max Offset Drift (μV/°C)	Package Option*
ADOP-37GH	TO-99	−25 to +85	100	1.8	H-08
ADOP-37GN	Mini-DIP	−25 to +85	100	1.8	N-8
ADOP-37GQ	Cerdip	−25 to +85	100	1.8	Q-8
ADOP-37FH	TO-99	−25 to +85	60	1.3	H-08
ADOP-37FN	Mini-DIP	−25 to +85	60	1.3	N-8
ADOP-37FQ	Cerdip	−25 to +85	60	1.3	Q-8
ADOP-37EH	TO-99	−25 to +85	25	0.6	H-08
ADOP-37EN	Mini-DIP	−25 to +85	25	0.6	N-8
ADOP-37EQ	Cerdip	−25 to +85	25	0.6	Q-8
ADOP-37CH	TO-99	−55 to +125	100	1.8	H-08
ADOP-37CQ	Cerdip	−55 to +125	100	1.8	Q-8
ADOP-37BH	TO-99	−55 to +125	60	1.3	H-08
ADOP-37BQ	Cerdip	−55 to +125	60	1.3	Q-8
ADOP-37AH	TO-99	−55 to +125	25	0.6	H-08
ADOP-37AQ	Cerdip	−55 to +125	25	0.6	Q-8
ADOP-37G Chips	Die	−25 to +85	100	1.8	
ADOP-37C Chips	Die	−55 to +125	100	1.8	

*For outline information see Package Information section.

APPLICATION NOTES FOR THE AD OP-37

The AD OP-37 can be used in the sockets of many of the popular precision bipolar input operational amplifiers on the market. Elimination of external frequency compensation or nulling circuitry may be possible in many cases. In 741 replacement situations, if nulling has been implemented, it should be modified or removed for correct AD OP-37 performance.

In applications where the initial factory adjusted input offset voltage provides insufficient accuracy, further offset trimming can be accomplished with the resistor network shown in Figure 1. The adjustment range attainable using a 10kΩ potentiometer will be ±4mV. If a smaller adjustment range is required, the sensitivity of the nulling can be increased by using a smaller potentiometer in series with fixed resistor(s). For example, a 1kΩ pot in series with two 4.7kΩ resistors will yield a ±280μV range.

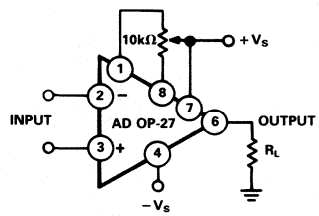


Figure 1. Optional Offset Nulling Circuit

Zeroing the initial offset with potentiometers other than 10kΩ, but between 1kΩ and 1MΩ, will introduce an additional input offset voltage temperature drift error of from 0.1 to 0.2μV/°C. Additionally, by intentionally trimming in a dc level shift a voltage dependent offset drift will be created. It will be approximately the input offset voltage at 25°C divided by 300 (in μV/°C).

Parasitic thermocouple EMF's can be generated where dissimilar metals meet the contacts to the input terminals of the AD OP-37. These temperature dependent voltages can manifest themselves as drift type errors. Optimized temperature performance will be obtained when both contacts are maintained at the same temperature.

Although the AD OP-37 features high-power supply rejection, the effects of noise on the power supplies may be minimized by bypassing the power supplies as close to Pins 4 and 7 of the AD OP-37 as possible, to load ground with a good quality 0.01μF ceramic capacitor as shown in Figure 1.

High closed loop gain and excellent linearity can be achieved by operating the AD OP-37 within an output current range of ±10mA. Minimizing output current will provide the highest linearity.

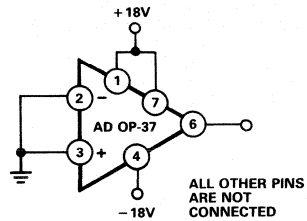


Figure 2. Burn-In Circuit

CAUTION: NOISE MEASUREMENTS

Precise measurement of the extremely low input noise associated with the AD OP-37 is a difficult task. In order to observe the rated noise in the 0.1Hz to 10Hz frequency range the following cautions should be exercised.

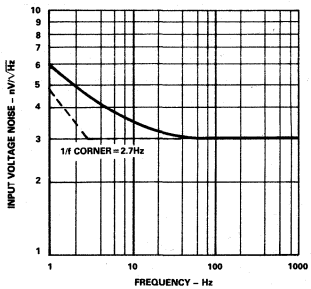
(1) The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds. As shown in the noise test frequency response plot in this data sheet the 0.1Hz corner is only defined by a single zero. A test time of 10 seconds acts as an additional zero to eliminate noise contributions from frequencies lower than 0.1Hz.

(2) Warm-up for a least five minutes will eliminate temperature induced effects. During the first few minutes the offset voltage typically increases 4μV. In a 10 second measurement interval prior to temperature stabilization the reading could include several nanovolts of warm-up offset error in addition to the noise.

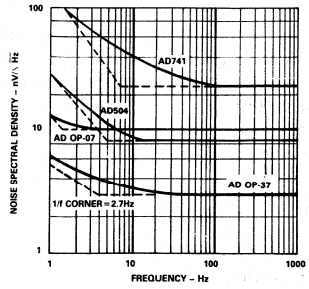
(3) For reasons similar to (2) the device under test should be well shielded from air currents or other heat sinks to eliminate the possibility of temperature changes over time invalidating the measurements. Sudden motion in the vicinity or physical contact with the package can also increase the observed noise.

An input voltage noise spectral density test is recommended when measuring noise on a large number of units. Because the l/f noise corner frequency is around 3Hz, a 1kHz noise voltage density measurement combined with a 0.1Hz to 10Hz peak-to-peak noise reading will guarantee l/f and white noise performance over the rated frequency spectrum.

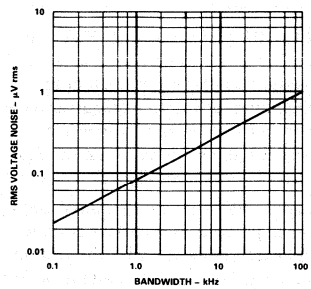
AD OP-37—Typical Performance Curves (@ T_A = +25°C, V_S = ±15V)



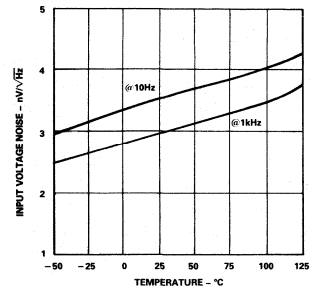
Input Voltage Noise Spectral Density



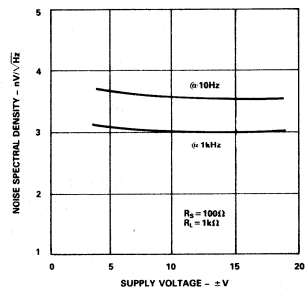
Comparison of Op Amp Input Voltage Noise Spectrums



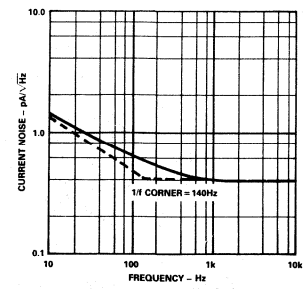
Input Wideband Noise vs. Bandwidth (0.1Hz to Frequency Indicated)



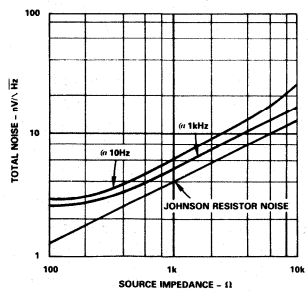
Input Voltage Noise vs. Temperature



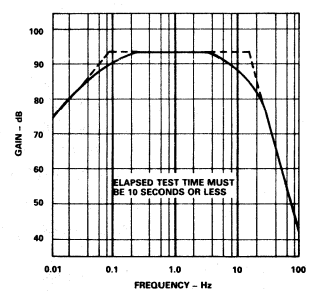
Input Voltage Noise vs. Supply Voltage



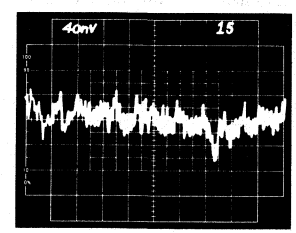
Input Current Noise Spectral Density



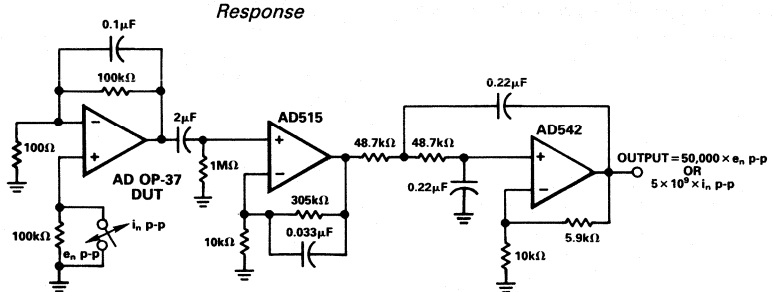
Total Noise vs. Source Impedance



0.1Hz to 10Hz Noise Test Frequency Response

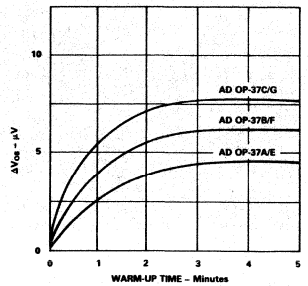


0.1Hz to 10Hz p–p Voltage Noise

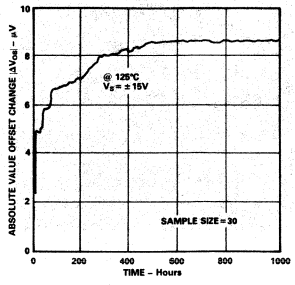


NOTE: ALL CAPACITORS MUST BE NONPOLARIZED

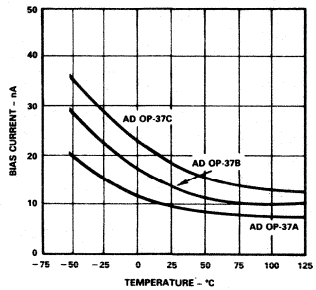
0.1Hz to 10Hz Noise Test Bandpass Filter (Voltage Gain = 50,000)



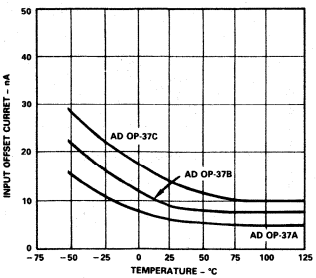
Input Offset Voltage Turn-On Drift vs. Warm-Up Time



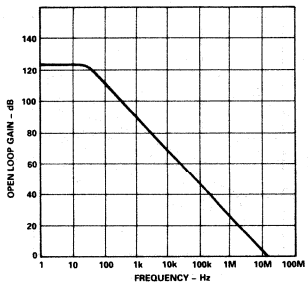
Long Term Offset Stability @ Temperature



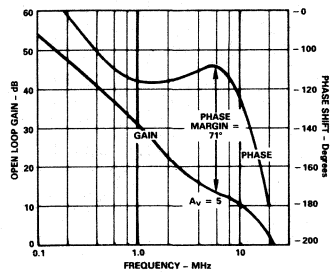
Input Bias Current vs. Temperature



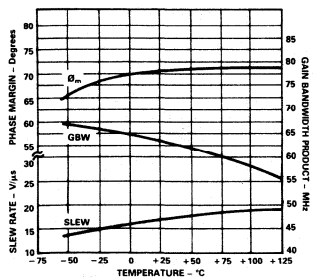
Input Offset Current vs. Temperature



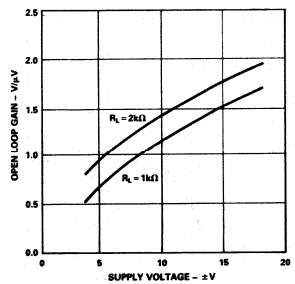
Open-Loop Frequency Response



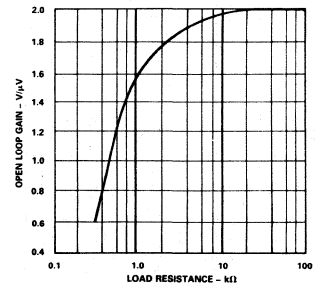
Open-Loop Gain and Phase Shift vs. Frequency



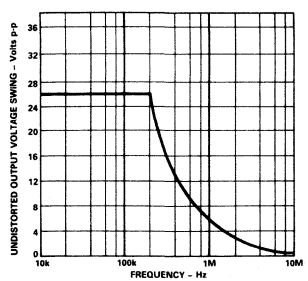
Slew Rate, Gain Bandwidth Product and Phase Margin vs. Temperature



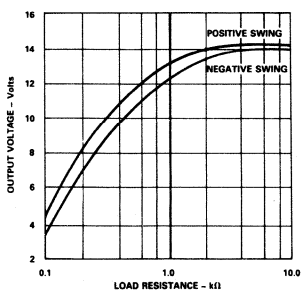
Open-Loop Gain vs. Supply Voltage



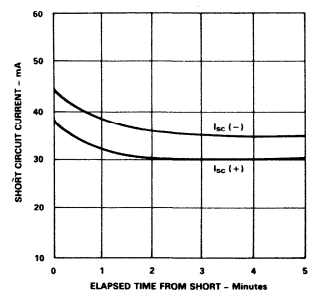
Open-Loop Gain vs. Load Resistance



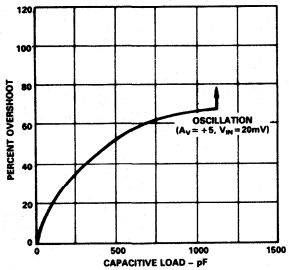
Undistorted Output Voltage Swing vs. Frequency



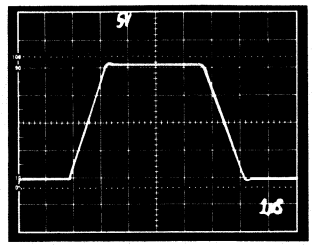
Output Swing vs. Load Resistance



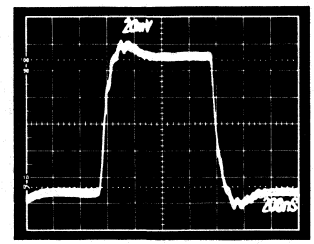
Output Short Circuit Current vs. Time



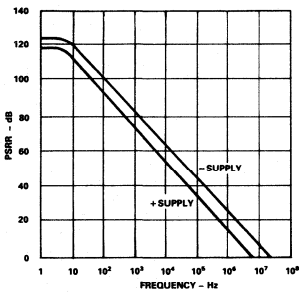
Small Signal Overshoot vs. Capacitive Load



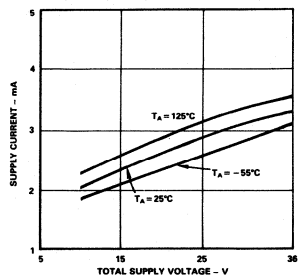
Large Signal Pulse Response (A_V = 5, R_L = 2k)



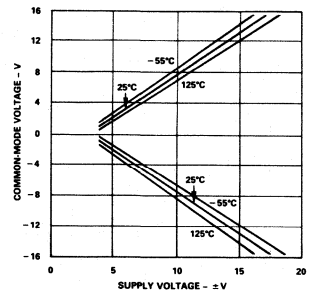
Small Signal Pulse Response (A_V = 5, R_L = 2k)



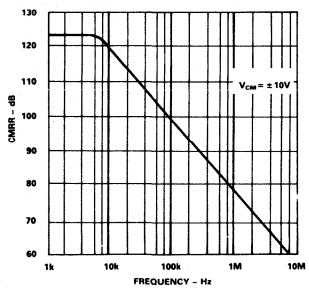
Power Supply Rejection Ratio vs. Frequency



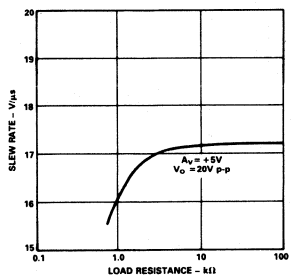
Supply Current vs. Supply Voltage



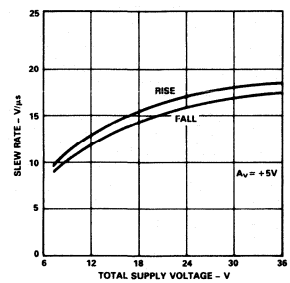
Common-Mode Input Range vs. Supply Voltage



CMRR vs. Frequency



Slew Rate vs. Resistive Load



Slew Rate vs. Supply Voltage

ANALOG DEVICES

High-Speed Voltage Follower/Buffer

BUF-03

FEATURES

- **Very High Slew Rate** ..... **220V/μs Min**
- **Wide Bandwidth** **63MHz**
- **Load Drive Current** ..... **70mA Peak**
- **Easily Drives Large Capacitive Loads Without Oscillation**
- **High Input Resistance** ..... **$5 \times 10^{11}\Omega$**
- **Low Output Resistance** **2Ω**
- **Very Low Bias Current (Warmed-Up)** ..... **400pA Max**
- **Low Offset Voltage** ..... **6mV Max**
- **Unity Gain** **0.997V/V**
- **Excellent Gain Linearity** **0.015%**
- **Available in Die Form**

ORDERING INFORMATION†

T_A = 25°C V_{OS} MAX (mV)	PACKAGE TO-99 8-PIN	OPERATING TEMPERATURE RANGE
6	BUF03AJ*	MIL
6	BUF03EJ	COM
15	BUF03BJ*	MIL
15	BUF03FJ	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

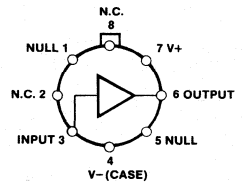
† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

The BUF-03 is the first very high-speed monolithic voltage follower. Featuring performance previously unobtainable in a monolithic unit, it offers a combination of both exceptional speed and excellent input/output specifications. Implemented in an open-loop circuit employing source followers and emitter followers, the BUF-03 utilizes a quasi-quad FET input structure to optimize both speed and D.C. input characteristics. On-chip zener-zap trimming is used to achieve low offset voltage while careful biasing throughout results in excellent gain linearity over the full input voltage range.

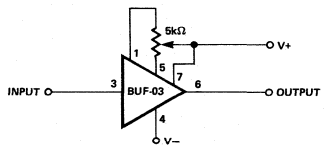
Applications for which the BUF-03 is well-suited include high-speed line drivers, isolation amplifiers for driving reactive loads, and high-speed sample-hold circuits.

PIN CONNECTIONS

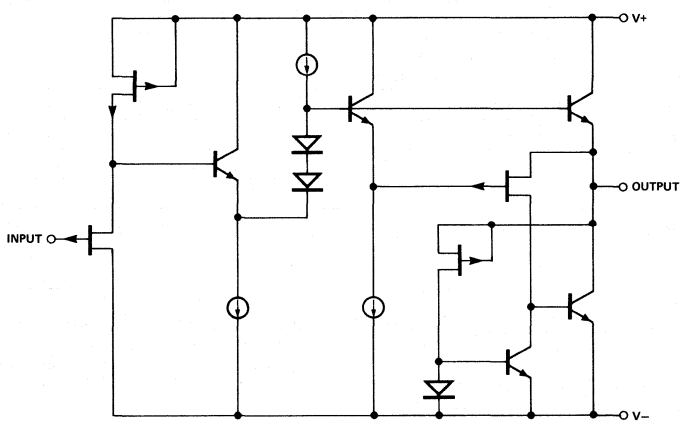


TO-99 (J-Suffix)

OPTIONAL OFFSET NULLING CIRCUIT



SIMPLIFIED SCHEMATIC



BUF-03

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
Internal Power Dissipation (P_d)
In Still Air Without Heat Sink (Note 1) 1.00W
Input Voltage (Note 2) ..... ±18V
Continuous Output Current (Note 3) 70mA
Peak Output Current (Note 3) 100mA
Short Circuit Protection (Note 3) ..... Indefinite (Note 4)
Maximum Junction Temperature (T_j) ..... 175°C
Storage Temperature Range ..... −65°C to +175°C
Operating Temperature Range (Note 5)
..... −55°C to +125°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

Dice Junction Temperature (T_j) ..... −65°C to +175°C
Thermal Resistance θ_{JA} (Note 1) ..... 150°C/W
Thermal Resistance θ_{JC} (Note 1) ..... 18°C/W

NOTES:
1. Based on MIL-STD-38510 published thermal resistance specification for 8 lead can-case outline C.
2. When $V_{CC} < \pm 18V$, the maximum input voltage is equal to the supply voltage.
3. The maximum P_d or T_j are not to be exceeded.
4. At 80mA.
5. When operating at $T_A > +25°C$, heat sinking is required to insure $T_{jMAX} = +175°C$ specification is not exceeded using the equation $T_{jMAX} = T_A + (P_d \times \theta J_{CMAX} + \theta_{SA})$ where θ_{SA} = sink to ambient thermal resistance. PMI recommends using either the Thermalloy 2227 or 1101 or equivalent when operating up to $T_A = +125°C$.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $R_S = 0\Omega$, $T_A = T_j = 25°C$, unless otherwise noted. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	BUF-03A/E MIN	BUF-03A/E TYP	BUF-03A/E MAX	BUF-03B/F MIN	BUF-03B/F TYP	BUF-03B/F MAX	UNITS
AC SPECIFICATIONS									
Slew Rate	SR	$R_L \geq 2k\Omega$, $C_L = 50pF$, $T_A = T_j = 75°C$	220	250	—	180	250	—	V/μs
Power Bandwidth	PBW	$V_{IN} = 10V_{p-p}$, $R_L \geq 2k\Omega$	—	9	—	—	8	—	MHz
Bandwidth	BW	$\Delta V_{IN} = \leq 2V_{p-p}$	—	63	—	—	50	—	MHz
Settling Time	t_S	To 0.1%, ±10V step	—	90	—	—	100	—	ns
Capacitive Load Capability	C_{LOAD}	No Oscillations	—	1	—	—	1	—	μF
Propagation Delay	t_d	Step Input	—	7	—	—	7	—	ns
Rise Time	t_r	ΔV = 0.5V	—	7	—	—	7	—	ns
Wide Band Input Noise Voltage	V_n	DC to 50MHz	—	350	—	—	400	—	μV_{RMS}
Input Noise Voltage Density	e_n	f = 10kHz	—	50	—	—	60	—	$nV/\sqrt{Hz}$
DC SPECIFICATIONS									
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$ (Note 2)	—	2	6	—	4	15	mV
Input Bias Current	I_B		—	150	400	—	180	700	pA
Input Resistance	R_{IN}		—	5×10^{11}	—	—	4×10^{11}	—	Ω
Voltage Gain ($V_{IN} = \pm 10V$)	A_{VO}	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	0.9960 0.9945 0.9925	0.9975 0.9960 0.9945	— — —	0.9940 0.9930 0.9905	0.9970 0.9950 0.9930	— — —	V/V
Nonlinearity (Note 2)	NL	$V_{IN} = \pm 10V$, $R_L \geq 2k\Omega$ (Note 3) $V_{IN} = \pm 7V$, $R_L \geq 1k\Omega$	— —	0.015 0.013	0.023 0.023	— —	0.017 0.015	0.03 0.03	%F.S.
Maximum Output Error	OUT_{error}	$V_{IN} = +10V, 0V, -10V$ $R_S = 0$ to $20k\Omega$ (Note 2) $R_L \geq 2k\Omega$ in all combinations	—	40	60	—	50	85	mV
Power Supply Rejection Ratio	PSRR	$V_S = \pm 6V$ to $\pm 18V$	—	0.10	0.71	—	0.15	1.42	mV/V
Supply Current	I_{SY}	No Load	—	19	25	—	19	25	mA
Peak Load Current	$I_{L(PK)}$		—	70	—	—	70	—	mA
Output Resistance	R_O		—	2	—	—	2	—	Ω
Offset Voltage Nulling Range	ΔV_{OS}	$R_P \geq 1k\Omega$	—	±80	—	—	±80	—	mV
Input Voltage Range (Reduced Accuracy)	IVR		—	±11.5	—	—	±11.5	—	V

NOTES:
1. Electrical parameters are pulse tested on automated test equipment. Total test time at each temperature is limited to less than one second maximum to keep T_j approximately equal to T_A.
2. Parameters specified with $R_S \leq 20k\Omega$ are tested at $R_S = 0\Omega$. Limits in test program are adjusted to take into account worst case voltage offset induced by $R_S = 20k\Omega$, i.e., I_B max × 20kΩ.
3. Nonlinearity is computed using linear regression techniques with data from five points (e.g., −10V, −5V, 0V, +5V, +10V for ±10V full-scale linearity; −7V, −3.5V, 0V, +3.5V, and +7V for ±7V full-scale linearity).

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$, $T_A = T_j$, unless otherwise noted. (Note 1)

			BUF-03A			BUF-03B			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Slew Rate	SR	$R_L \ge 2k\Omega$, $C_L = 50pF$	—	220	—	—	220	—	V/μs
Input Offset Voltage	V_{OS}	$R_S \le 2k\Omega$	—	6	20	—	10	35	mV
Average Input Offset Voltage Drift	TCV_{OS}	$R_S \le 2k\Omega$, (Note 2)	—	50	100	—	90	170	μV/°C
Input Bias Current	I_B	$T_A = +125°C$	—	25	75	—	30	90	nA
Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_{IN} = \pm 10V$	0.9920	0.9955	—	0.9902	0.9942	—	V/V
Gain Drift with Temperature			—	5	—	—	8	—	ppm/°C
Power Supply Rejection Ratio	PSRR	$V_S = \pm 7V$ to $\pm 15V$	—	0.15	1.26	—	0.20	2.24	mV/V
Supply Current	I_{SY}	$T_A = +125°C$	—	18	24	—	18	24	mA

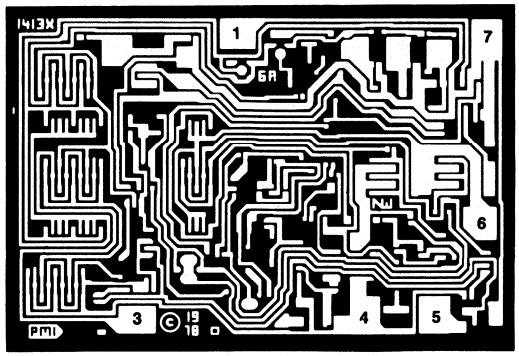
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0°C \le T_A \le +70°C$, $T_A = T_j$, unless otherwise noted.

			BUF-03E			BUF-03F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Slew Rate	SR	$R_L \ge 2k\Omega$	—	240	—	—	240	—	V/μs
Input Offset Voltage	V_{OS}	$R_S \le 2k\Omega$, $C_L = 50pF$	—	4	14	—	7	28	mV
Average Input Offset Voltage Drift	TCV_{OS}	$R_S \le 2k\Omega$, (Note 2)	—	40	90	—	80	150	μV/°C
Input Bias Current	I_B	$T_A = +70°C$	—	1.5	5	—	1.8	8	nA
Voltage Gain ($V_{IN} = \pm 10V$)	A_{VO}	$R_L \ge 2k\Omega$	0.9935	0.9958	—	0.9918	0.9946	—	V/V
Gain Drift with Temperature			—	5	—	—	8	—	ppm/°C
Power Supply Rejection Ratio	PSRR	$V_S = \pm 7V$ to $\pm 15V$	—	0.12	1	—	0.16	1.78	mV/V
Supply Current	I_{SY}	$T_A = +70°C$	—	19	25	—	19	25	mA

NOTES:
1. In order to operate the device at an ambient temperature of +125°C, more extensive heat sinking must be used to ensure that the chip temperature never exceeds the absolute maximum of +175°C. The chip temperature of +165°C is achieved by reducing the case-to-ambient thermal resistance to 30°C/W (e.g., Thermalloy 2227).
2. Guaranteed by design.

BUF-03

DICE CHARACTERISTICS



DIE SIZE 0.071 × 0.049 inch, 3479 sq. mils
(1.80 × 1.24 mm, 2.23 sq. mm)

1. NULL
3. INPUT
4. NEGATIVE SUPPLY
5. NULL
6. OUTPUT
7. POSITIVE SUPPLY

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_j = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	BUF-03N LIMIT	BUF-03G LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	6	15	mV MAX
Voltage Gain	A_{VO}	$R_L \geq 10k\Omega$, $V_{IN} = \pm 10V$	0.9960	0.9940	V/V MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 6V$ to $\pm 18V$	0.71	1.42	mV/V MAX
Supply Current	I_{SY}	No Load	25	25	mA MAX

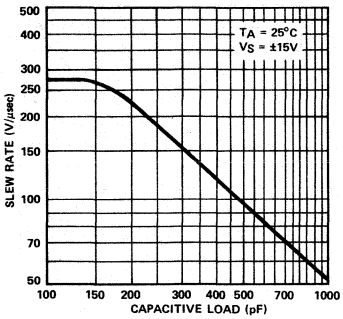
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_j = 25°C$, unless otherwise noted.

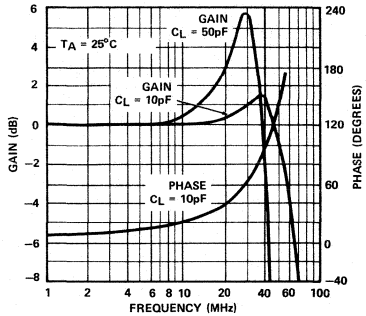
PARAMETER	SYMBOL	CONDITIONS	BUF-03N TYPICAL	BUF-03G TYPICAL	UNITS
Slew Rate	SR	$R_L \geq 2k\Omega$, $C_L = 50pF$	220	180	V/μs
Peak Load Current	$I_L(PK)$		70	70	mA
Input Bias Current	I_B		40	60	pA
Input Resistance	R_{IN}		5×10^{11}	5×10^{11}	Ω
Output Resistance	R_O		2	2	Ω
Offset Voltage Nulling Range	ΔV_{OS}	$R_P \geq 1k\Omega$	±80	±80	mV
Input Voltage Range (Reduced Accuracy)	IVR		±11.5	±11.5	V
Power Bandwidth	PBW	$V_{IN} = 10V_{p-p}$, $R_L \geq 2k\Omega$	9	8	MHz
Bandwidth	BW	$\Delta V_{IN} \leq 2V_{p-p}$	63	55	MHz
Settling Time	t_S	To 0.1%, ±10V step	90	100	ns
Capacitive Load Capacity	C_{LOAD}	No Oscillations	1	1	μF
Propagation Delay	t_d	Step Input	7	7	ns
Rise Time	t_r	$\Delta V_{IN} = 0.5V$	7	7	ns
Wide Band Input Noise Voltage	V_n	DC to 50MHz	350	400	μV_{RMS}
Input Noise Voltage Density	e_n	f = 10kHz	50	60	$nV/\sqrt{Hz}$

TYPICAL PERFORMANCE CHARACTERISTICS

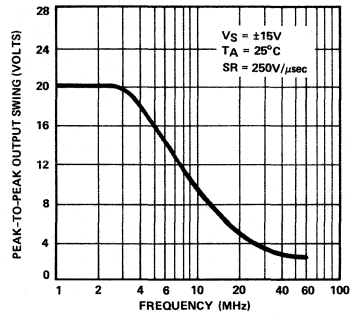
SLEW RATE vs CAPACITIVE LOAD



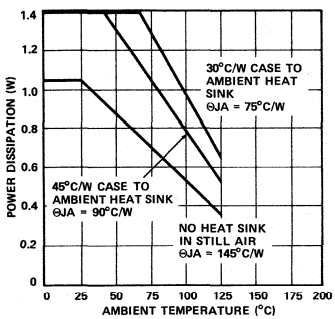
GAIN AND PHASE RESPONSE vs FREQUENCY



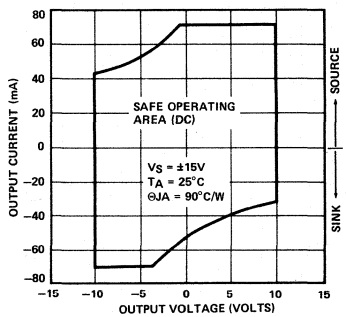
LARGE-SIGNAL FREQUENCY RESPONSE



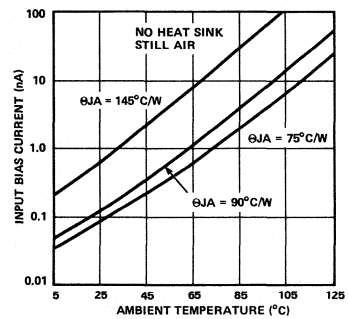
MAXIMUM POWER DISSIPATION vs AMBIENT TEMPERATURE



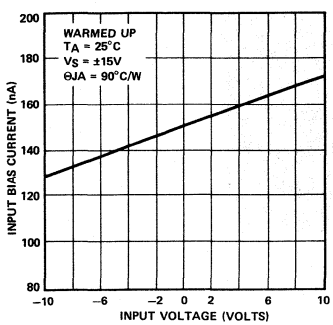
OUTPUT CURRENT vs OUTPUT VOLTAGE



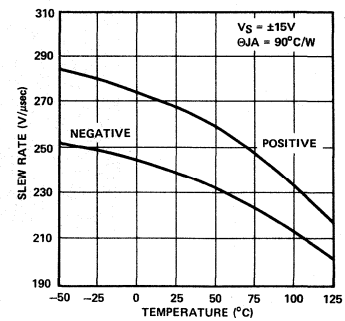
INPUT BIAS CURRENT vs TEMPERATURE (WARMED-UP)



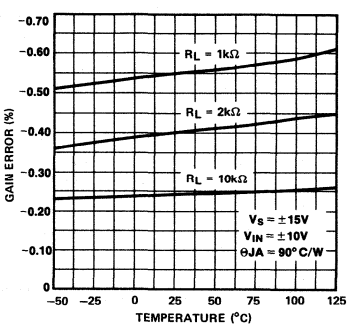
INPUT BIAS CURRENT vs INPUT VOLTAGE



SLEW RATE vs TEMPERATURE



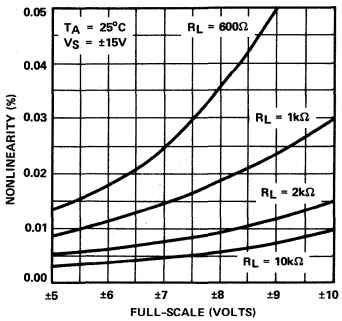
GAIN ERROR vs TEMPERATURE



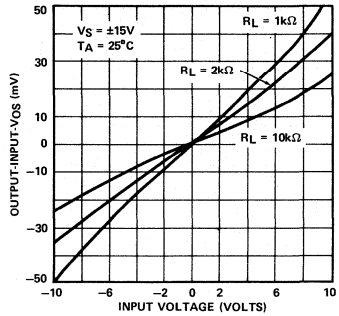
BUF-03

TYPICAL PERFORMANCE CHARACTERISTICS

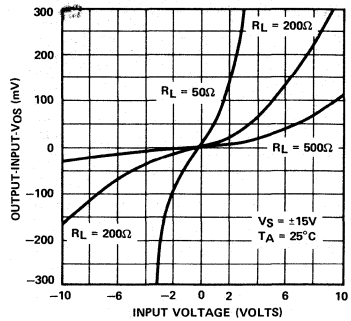
NONLINEARITY vs FULL-SCALE VOLTAGE



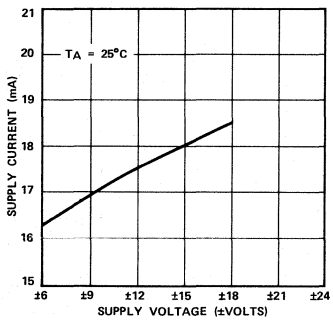
GAIN ERROR vs INPUT VOLTAGE



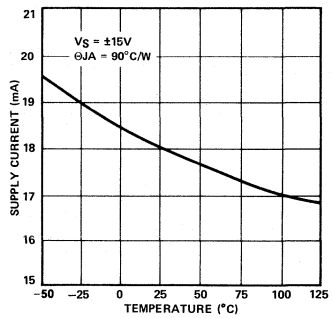
GAIN ERROR vs INPUT VOLTAGE



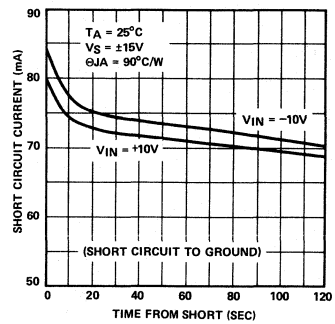
SUPPLY CURRENT vs SUPPLY VOLTAGE



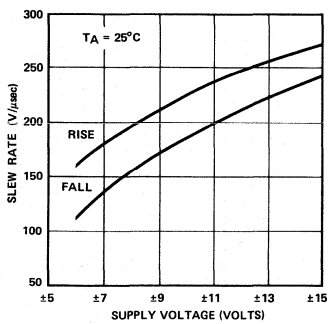
SUPPLY CURRENT vs TEMPERATURE



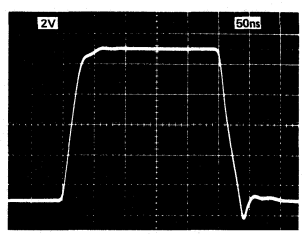
OUTPUT SHORT-CIRCUIT CURRENT vs TIME



SLEW RATE vs SUPPLY VOLTAGE



SLEW RATE

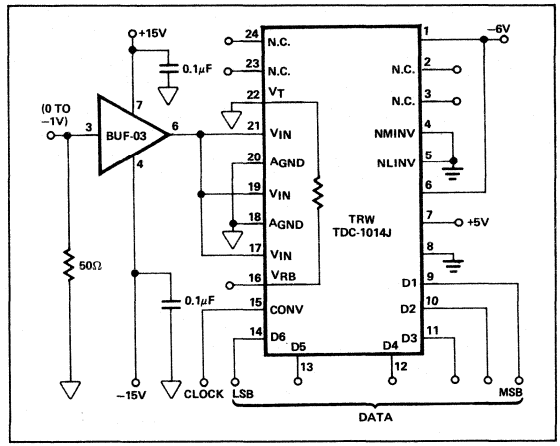


APPLICATIONS INFORMATION

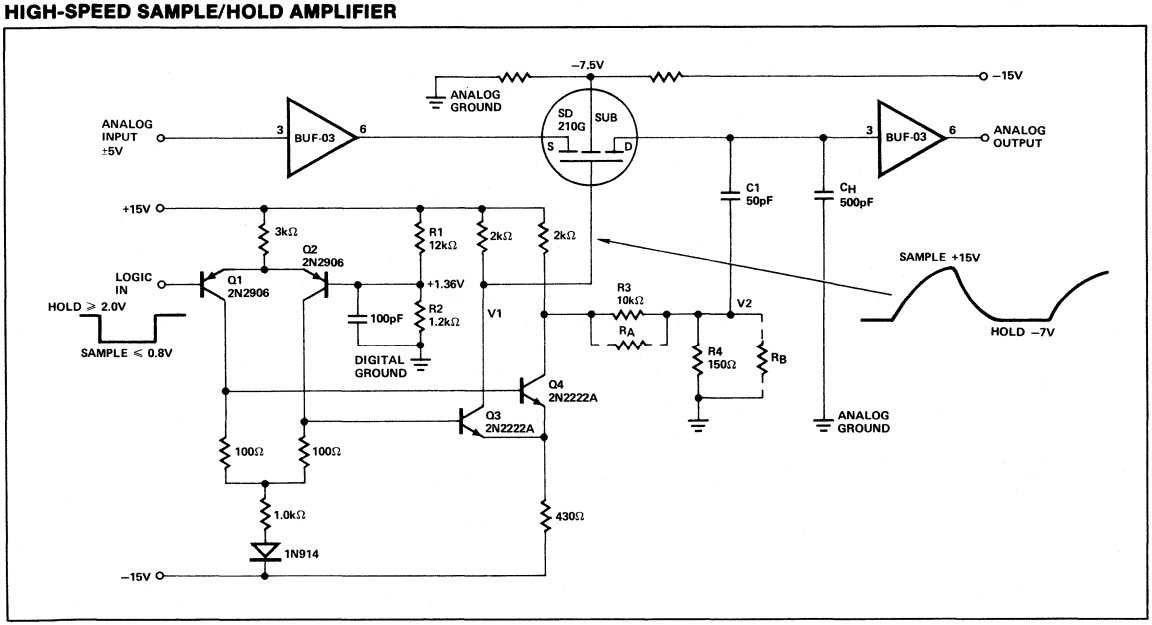
OPERATING THE BUF-03 AT REDUCED POWER SUPPLIES

In most video applications the signal levels are significantly lower than the 20V peak-to-peak capability of the BUF-03. This suggests operating the BUF-03 at reduced power supplies; for example, at ±6V supplies ±2V signals can be handled. The obvious advantage of reduced supplies is the accompanying decrease in power dissipation: from a typical 540mW (=30V×18mA) to 195mW (=12V×16.2mA) at ±6V. At lower supply voltages heat sinking is no longer necessary. However, as shown on the slew rate vs supply voltage curve, slew rate does degrade at lower supplies. This occurs because of higher internal node capacitances at lower voltages and because of the slightly decreased operating current.

HIGH-SPEED 6-BIT A/D BUFFER



HIGH-SPEED SAMPLE/HOLD AMPLIFIER



ANALOG DEVICES

Inverting High-Speed Operational Amplifier

OP-01

FEATURES

- **Fast Settling Time ..... 1μs to 0.1% Max**
- **High Slew Rate ..... 12V/μs Min**
- **Power Bandwidth ..... 150kHz Min**
- **Low Power Consumption ..... 90mW Max**
- **Excellent DC Specifications**
- **Internally Compensated**
- **Ideal DAC Output Amplifier**
- **MIL-STD-883 Processing Available**
- **Fits Standard 741 Sockets**
- **Low Cost**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = 25°C V_{OS} MAX (mV)	PACKAGE			OPERATING TEMPERATURE RANGE
	TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	
0.7	OP01J*	—	—	MIL
0.7	—	—	OP01HP	COM
5.0	OP01GJ	—	—	MIL
5.0	OP01CJ	OP01CZ	OP01CP	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

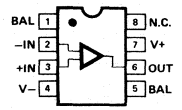
† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

The OP-01 series of monolithic inverting high-speed operational amplifiers combines high slew rate, fast settling time and excellent DC input characteristics. An internal feedforward frequency compensation network provides simplicity of application — no external capacitors are required for stable, high-speed performance. The fast output response is achieved without sacrifice of input bias current or power consumption. A 250kHz typical power bandwidth is attained with a small-signal bandwidth of only 2.5MHz, thus board layout is non-critical. The OP-01 is completely protected at both input and output, fits standard 741 sockets, and is offset nulled with a 10kΩ potentiometer.

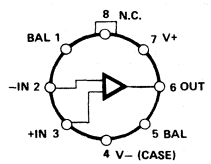
The fast output response combined with excellent settling time makes the OP-01 ideal for use as a D/A converter output amplifier.

PIN CONNECTIONS



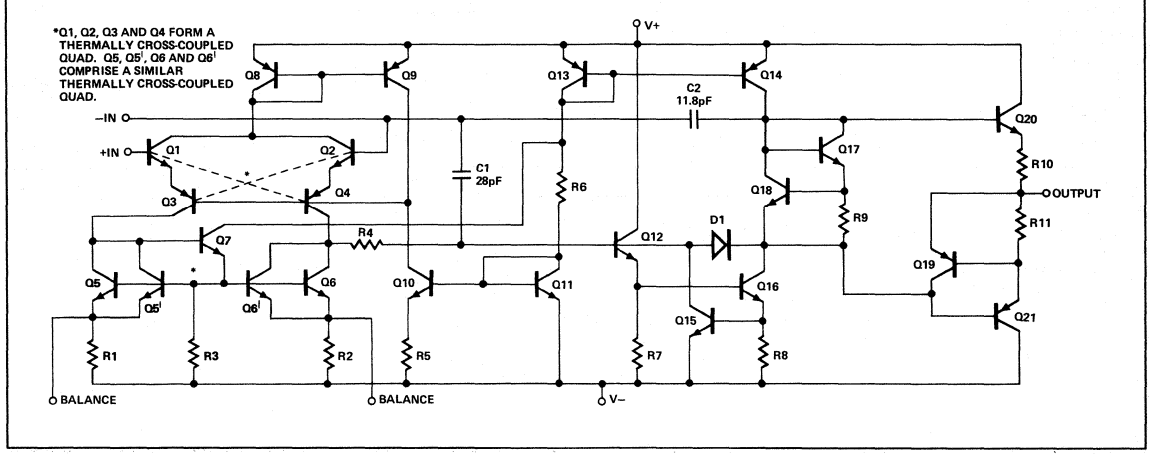
EPOXY MINI-DIP (P-Suffix)

8-PIN HERMETIC DIP (Z-Suffix)



TO-99 (J-Suffix)

SIMPLIFIED SCHEMATIC



OP-01

ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage, OP-01,OP-01H, OP-01N, OP-01NT,
OP-01G, OP-01GT ..... ±22V
OP-01G, OP-01C, OP-01GR ..... ±20V
Differential Input Voltage ..... ±30V
Input Voltage (Note 2) ..... ±15V
Short-Circuit Duration ..... Indefinite
Operating Temperature Range
OP-01, OP-01G ..... –5°C to +125°C
OP-01H, OP-01C ..... 0°C to +70°C
Junction Temperature (T_J) ..... –65°C to +150C
Storage Temperature
J and Z Packages ..... –65°C to +150°C
P Packages ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (NOTE 3)	Θ_{JC}	UNITS
TO-99 (J)	170	24	°C/W
8-Pin Hermetic DIP (Z)	162	26	°C/W
8-Pin Plastic DIP (P)	110	50	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. For supply voltages less than ±15V, the maximum input voltage is the supply voltage.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP and P-DIP packages.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-01 OP-01H			OP-01G OP-01C			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \le 20k\Omega$	—	0.3	0.7	—	2.0	5.0	mV
Input Offset Current	I_{OS}		—	0.5	2.0	—	2.0	20	nA
Input Bias Current	I_B		—	18	30	—	25	100	nA
Input Voltage Range	IVR		±12	±13	—	±12	±13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \le 20k\Omega$	85	110	—	80	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \le 20k\Omega$	—	10	60	—	100	150	μV/V
Output Voltage Swing	V_O	$R_L \ge 5k\Omega$ $R_L \ge 2k\Omega$	±12.5 ±12.0	±13.5 ±13.0	— —	±12.5 ±12.0	±13.5 ±13.0	— —	V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$ $V_O = \pm 10V$	50	100	—	25	75	—	V/mV
Power Consumption	P_d	$V_{OUT} = 0$	—	50	90	—	50	90	mW
Settling Time to 0.1% (Summing Node Error)	t_S	$A_V = -1$ (Notes 1, 2) $V_{IN} = 5V$	—	0.7	1.0	—	0.7	1.0	μs
Slew Rate (Notes 2, 3)	SR	$A_V = -1$, $R_S = 3k$ to $5k\Omega$	12	18	—	12	18	—	V/μs
Large-Signal Bandwidth (Notes 3, 4)			150	250	—	150	250	—	kHz
Small-Signal Bandwidth (Notes 3, 4)			1.5	2.5	—	1.5	2.5	—	MHz
Risetime	t_r	$A_V = -1$ $V_{IN} = 50mV$	—	150	—	—	150	—	ns
Overshoot	OS		—	2	—	—	2	—	%

NOTES:
1. $R_L = 25k\Omega$; $C_L = 50pF$. See Settling Time Test Circuit.
2. Sample tested.
3. See applications information.
4. Guaranteed by design.

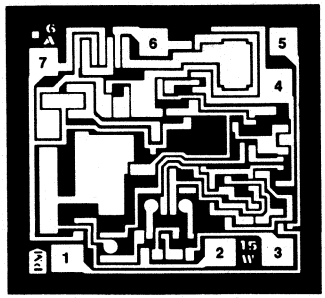
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$ for OP-01, OP-01G and $0°C \leq T_A \leq +70°C$ for OP-01H, OP-01C, unless otherwise noted.

			OP-01 OP-01H			OP-01G OP-01C			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.4	1.0	—	3.0	6.0	mV
Input Offset Current	I_{OS}		—	1	4	—	4	40	nA
Input Bias Current	I_B		—	30	50	—	50	200	nA
Input Voltage Range	IVR		±10	±13	—	±10	±13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	85	110	—	80	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	10	60	—	100	150	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	30	60	—	15	50	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 5k\Omega$ $R_L \geq 2k\Omega$	±12.5 ±12.0	±13.5 ±13.0	— —	±12.5 ±12.0	±13.5 ±13.0	— —	V
Offset Voltage Drift (Note 1)	TCV_{OS}	$R_S \leq 5k\Omega$	—	2	8	—	5	20	μV/°C

NOTE:
1. Sample tested.

OP-01

DICE CHARACTERISTICS (125°C TESTED DICE AVAILABLE)



DIE SIZE 0.047 × 0.043 inch, 2021 sq. mils
(1.19 × 1.09 mm, 1.30 sq. mm)

1. NULL
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V−
5. NULL
6. OUTPUT
7. V+

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$ for OP-01N, OP-01G and OP-01GR devices; $T_A = 125°C$ for OP-01NT and OP-01GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-01NT LIMIT	OP-01N LIMIT	OP-01GT LIMIT	OP-01G LIMIT	OP-01GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	1.0	0.7	3.0	2.0	5.0	mV MAX
Input Offset Current	I_{OS}		4	2	10	5	20	nA MAX
Input Bias Current	I_B		50	30	100	50	100	nA MAX
Input Voltage Range	IVR		±10	±12	±10	±12	±12	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	85	85	80	80	80	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	60	60	100	100	150	μV/V MAX
Output Voltage Swing	V_{OM}	$R_L \geq 5k\Omega$ $R_L \geq 2k\Omega$	±12.5 ±12.0	±12.5 ±12.0	±12.5 ±12.0	±12.5 ±12.0	±12.5 ±12.0	V MIN
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	30	50	25	50	25	V/mV MIN
Power Consumption	P_d	$V_{OUT} = 0$	—	90	—	90	90	mW MAX

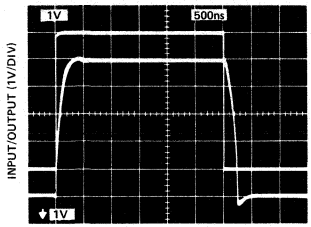
NOTES:
For 25°C characteristics of NT & GT devices, see N & G characteristics respectively.
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	ALL GRADES TYPICAL	UNITS
Slew Rate	SR	$A_{VCL} = -1$, $R_S = 3k\Omega$ to $5k\Omega$	18	V/μs
Settling Time to 0.1% (Summing Node Error)	t_S	$V_{IN} = 5V$ $A_V = -1$ $R_L = 2k\Omega$ (See Settling Time Test Circuit) $C_L = 50pF$	1.0	μs
Large-Signal Bandwidth			250	kHz
Small-Signal Bandwidth			2.5	MHz
Risetime	t_r	$V_{IN} = 50mV$ $A_V = -1$	150	ns

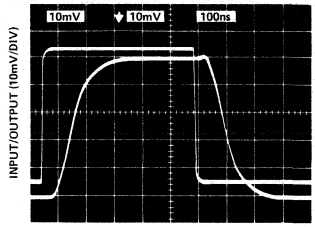
TYPICAL PERFORMANCE CHARACTERISTICS

LARGE-SIGNAL PULSE RESPONSE



$V_S = \pm 15V$, $A_V = -1$, $R_L = 2k\Omega$, $C_L = 50pF$

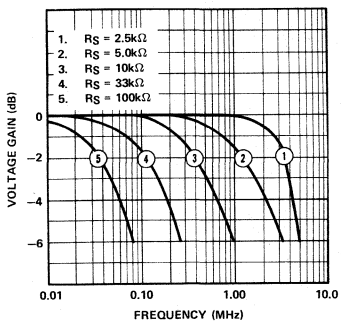
SMALL-SIGNAL PULSE RESPONSE



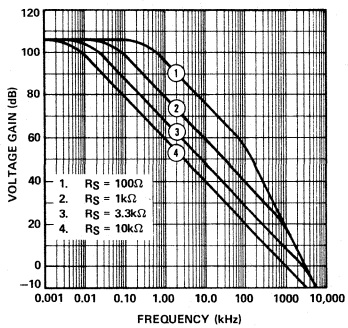
$V_S = \pm 15V$, $A_V = -1$, $R_L = 2k\Omega$, $C_L = 50pF$

2

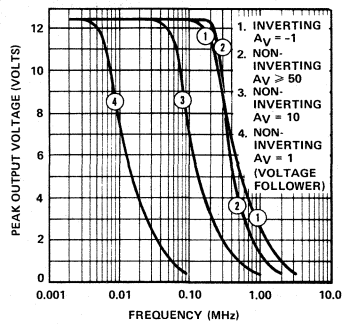
UNITY-GAIN BANDWIDTH vs SOURCE RESISTANCE



OPEN-LOOP GAIN vs FREQUENCY



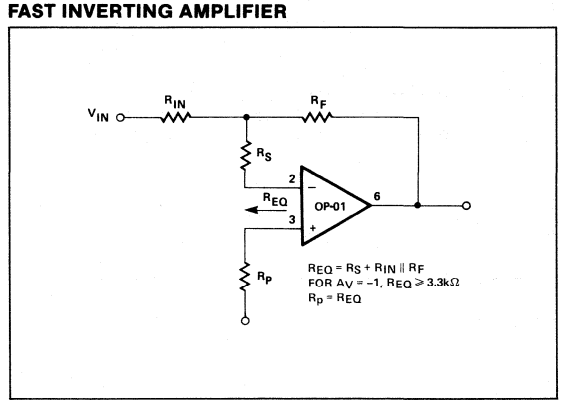
LARGE-SIGNAL OUTPUT SWING vs FREQUENCY



APPLICATIONS INFORMATION

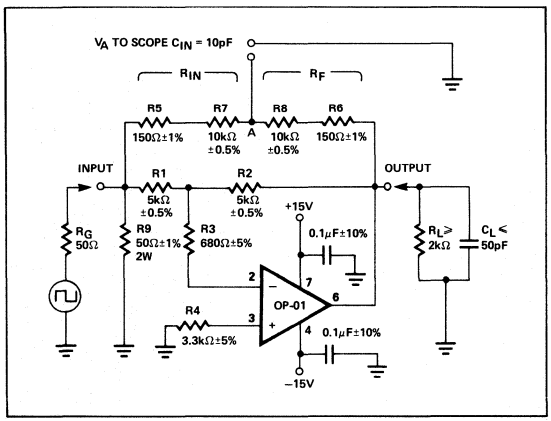
The OP-01 incorporates an internal feed-forward compensation network to provide fast slewing and settling times in all inverting and moderate-to-high-gain noninverting applications. Unity-gain bandwidth is a function of the total equivalent source resistance seen by the inverting terminal. Proper choice of this resistance will allow the user to maxmize bandwidth while assuring proper stability. The equivalent-inverting-terminal-resistance is defined as $R_{IN} || R_F$, and it must be greater than 3.3kΩ to assure stability in all closed-loop gain configurations including unity gain. Should $R_{IN} || R_F \leq 3.3k\Omega$, a resistor ($R_S$) may be placed between the inverting input and the sum node to provide the required resistance. (See Fast Inverting Amplifier Diagram.) Lower values of total equivalent resistance may be used to improve bandwidth in higher closed-loop gain configurations, as indicated by the Open-Loop Gain vs. Frequency plot.

FAST INVERTING AMPLIFIER

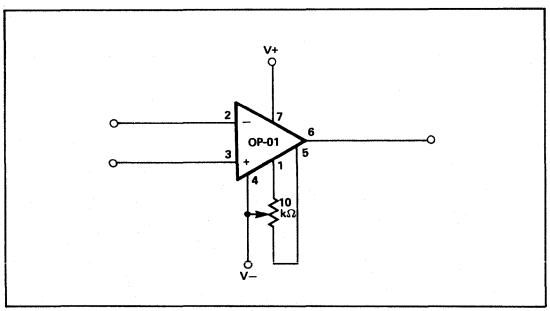


SETTLING-TIME TEST CIRCUIT

Settling time may be measured using the circuit shown below. This circuit incorporates the "false sum node" technique to produce accurate, repeatable results. For a 5V input step, 0.1% settling will be achieved when the false sum node settles to within ±2.5mV of its final value. The oscilloscope used for observation of the false sum node should have wide bandwidth, fast overload recovery time, and be used with a low capacity probe (≤ 10pF, including strays). A Tektronix 7504 scope with a 7A11 probe or equivalent is suggested. The pulse generator should have a 50Ω output impedance and be capable of a 5V rise time in ≤ 20ns with ringing less than 2.5mV after 0.5μs. Measurements to 0.1% require R_{IN} to equal R_F within 0.01%; R_5 and R_6 are used as trimming resistors to achieve this matching.

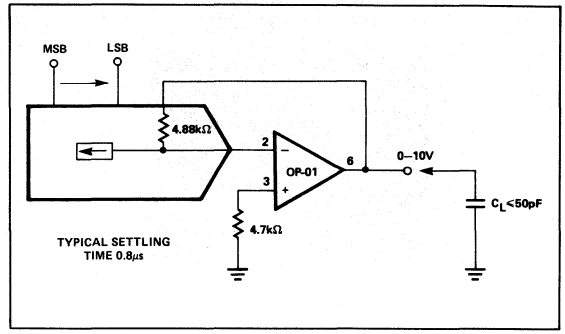


OFFSET NULLING CIRCUIT

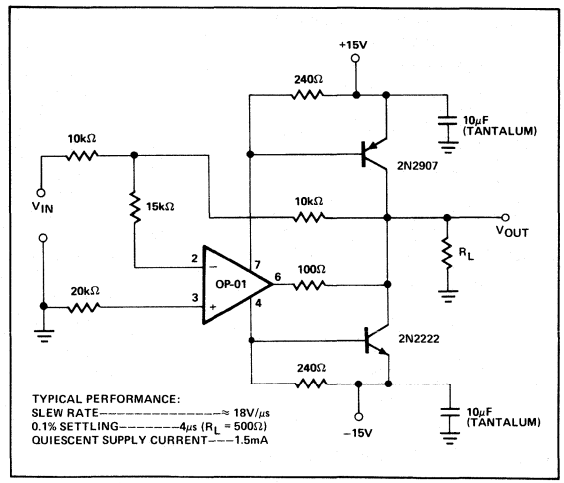


TYPICAL APPLICATIONS

FAST VOLTAGE-OUTPUT D/A CONVERTER



PRECISION POWER-BOOSTER CIRCUIT



ANALOG DEVICES

General-Purpose Operational Amplifier

OP-02

FEATURES

- **Excellent DC Specifications**
- **Low Noise** ..... **0.65μV_{p-p} Typ**
- **Low Drift (TCV_{OS})** ..... **8$\mu V/°C$ Max**
- **Silicon-Nitride Passivation**
- **125° C Tested Dice Available**
- **"Premium" 741 Replacement**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (mV)	PACKAGE TO-99	PACKAGE CERDIP 8-PIN	PACKAGE PLASTIC 8-PIN	OPERATING TEMPERATURE RANGE
0.5	OP02AJ*	OP02AZ*	–	MIL
2.0	OP02J/883	OP02Z	–	MIL
2.0	OP02CJ	OP02CZ	OP02CP	COM
5.0	–	–	OP02DP	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

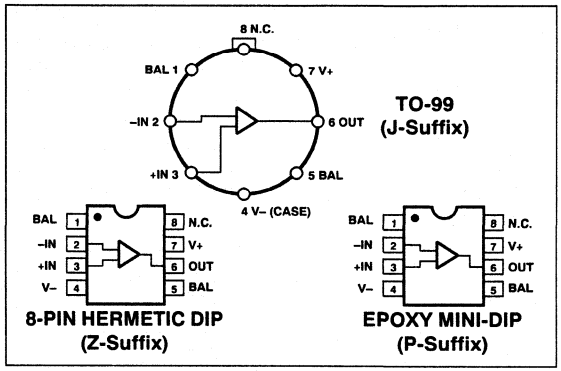
† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

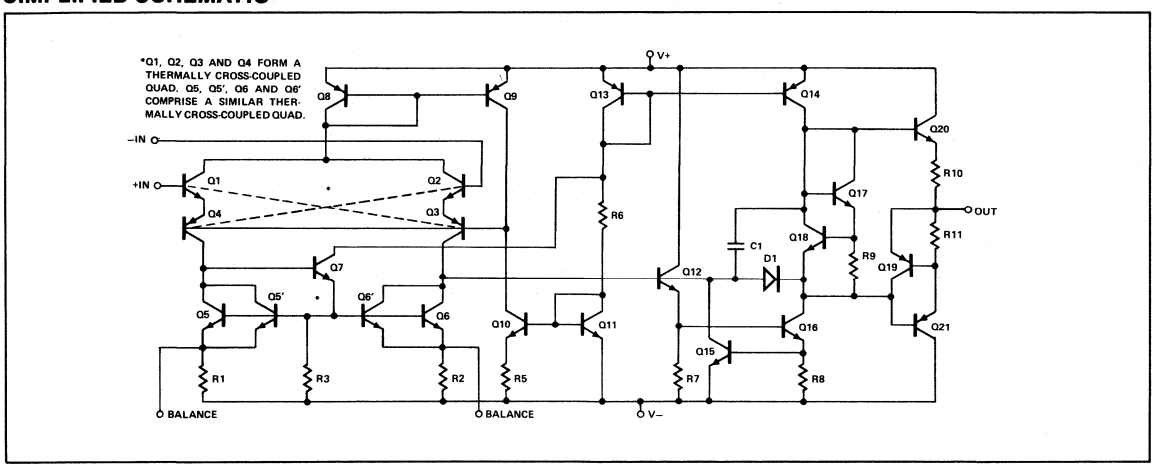
This high-performance general-purpose operational amplifier provides significant improvements over industry-standard and "premium" 741 types while maintaining pin-for-pin compatibility, ease of application, and low cost. Key specifications, such as V_{OS}, I_{OS}, I_B, CMRR, PSRR, and A_{VO} are guaranteed over the full operating temperature range. Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process reduces "popcorn noise." A thermally-symmetrical input-stage design provides low input offset voltage drift and insensitivity to output load conditions.

The OP-02 is a direct replacement for the 741. It is ideal for upgrading existing designs where accuracy improvements are required and for eliminating special low-drift or low-noise selected types.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



OP-02

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±22V
Differential Input Voltage ..... ±30V
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range
OP-02A, OP-02 ..... –55°C to +125°C
OP-02C, OP-02D ..... 0°C to +70°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
Junction Temperature (T_j) ..... –65°C to +150°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
TO-99 (J)	170	24	°C/W
8-Pin Hermetic DIP (Z)	162	26	°C/W
8-Pin Plastic DIP (P)	110	50	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP and P-DIP packages.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-02A			OP-02 OP-02C			OP-02D			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.3	0.5	—	1	2	—	3	5	mV
Input Offset Current	I_{OS}		—	0.5	2	—	1	5	—	5	25	nA
Input Bias Current	I_B		—	18	30	—	20	50	—	30	100	nA
Input Resistance-Differential-Mode	R_{IN}	(Note 2)	3.4	5.7	—	2.0	5.2	—	1	3.5	—	MΩ
Input Voltage Range	IVR		±10	±13	—	±10	±13	—	±10	±13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	85	100	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	10	60	—	30	100	—	100	150	μV/V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	—	±12	±13	—	±12	±13	—	V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	100	250	—	50	200	—	25	150	—	V/mV
Power Consumption	P_d	$V_O = 0V$	—	40	70	—	50	90	—	50	90	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.65	—	—	0.65	—	—	0.65	—	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$ $f_O = 100Hz$ $f_O = 1000Hz$	— — —	25 22 21	— — —	— — —	25 22 21	— — —	— — —	25 22 21	— — —	$nV/\sqrt{Hz}$
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	—	12.8	—	—	12.8	—	—	12.8	—	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10Hz$ $f_O = 100Hz$ $f_O = 1000Hz$	— — —	1.4 0.7 0.4	— — —	— — —	1.4 0.7 0.4	— — —	— — —	1.4 0.7 0.4	— — —	$pA/\sqrt{Hz}$
Slew Rate	SR	(Note 1)	0.25	0.5	—	0.25	0.5	—	0.25	0.5	—	V/μs
Large-Signal Bandwidth		$V_O = 20V_{p-p}$ (Notes 1, 4)	4	8	—	4	8	—	4	8	—	kHz
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$ (Note 3)	1	1.3	—	1	1.3	—	1	1.3	—	MHz
Risetime	t_r	$A_{VCL} = +1$ $V_{IN} = 50mV$ (Note 1)	—	200	350	—	200	350	—	200	350	ns
Overshoot	OS	(Note 1)	—	5	10	—	5	10	—	5	10	%

NOTES:
1. Sample tested.
2. Guaranteed by input bias current.
3. Guaranteed by maximum risetime.
4. Guaranteed by minimum slew rate.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, –55°C ≤ T_A +125°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-02A MIN	OP-02A TYP	OP-02A MAX	OP-02 MIN	OP-02 TYP	OP-02 MAX	UNITS
Input Offset Voltage	V_{OS}	R_S ≤ 20kΩ	–	0.5	1	–	1.4	3	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	R_S = 50Ω	–	2	8	–	4	10	µV/°C
Input Offset Current	I_{OS}		–	1	5	–	2	10	nA
Average Input Offset Current Drift (Note 1)	TCI_{OS}		–	7.5	75	–	15	150	pA/°C
Input Bias Current	I_B		–	30	60	–	40	100	nA
Input Voltage Range	IVR		±10	±13	–	±10	±13	–	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±10V R_S ≤ 20kΩ	80	95	–	80	95	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5V to ±20V R_S ≤ 20kΩ	–	10	60	–	30	100	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ V_O = ±10V	50	100	–	25	60	–	V/mV
Output Voltage Swing	V_O	R_L ≥ 2kΩ	±12	±13	–	±12	±13	–	V

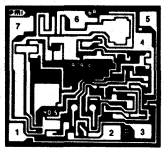
ELECTRICAL CHARACTERISTICS at V_S = ±15V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-02C MIN	OP-02C TYP	OP-02C MAX	OP-02D MIN	OP-02D TYP	OP-02D MAX	UNITS
Input Offset Voltage	V_{OS}	R_S ≤ 20kΩ	—	1.2	3	—	3	6	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	R_S = 50Ω	—	4	10	—	8	20	µV/°C
Input Offset Current	I_{OS}		—	1.4	10	—	5	50	nA
Average Input Offset Current Drift (Note 1)	TCI_{OS}		—	15	250	—	70	500	pA/°C
Input Bias Current	I_B		—	25	100	—	50	200	nA
Input Voltage Range	IVR		±10	±13	—	±10	±13	—	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±10V R_S ≤ 20kΩ	80	90	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5 to ±20V R_S ≤ 20kΩ	—	30	100	—	100	150	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ V_O = ±10V	25	60	—	15	25	—	V/mV
Output Voltage Swing	V_O	R_L ≥ 2kΩ	±12	±13	—	±10	±13	—	V

NOTE:
1. Sample tested.

OP-02

DICE CHARACTERISTICS (125°C TESTED DICE AVAILABLE)



DIE SIZE 0.047 × 0.043 inch, 2021 sq. mils
(1.19 × 1.09 mm, 1.30 sq. mm)

1. NULL
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V–
5. NULL
6. OUTPUT
7. V+

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$ for OP-02N, OP-02G and OP-02GR devices; $T_A = 125°C$ for OP-02NT and OP-02GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-02NT LIMIT	OP-02N LIMIT	OP-02GT LIMIT	OP-02G LIMIT	OP-02GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	1	0.5	3	2	5	mV MAX
Input Offset Current	I_{OS}		5	3	6	5	25	nA MAX
Input Bias Current	I_B		50	30	60	50	200	nA MAX
Input Voltage Range	IVR		±13	±13	±13	±13	±13	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	80	85	80	80	70	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	60	60	100	100	150	μV/V MAX
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±12	±12	±12	±12	V MIN
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	50	100	25	50	25	V/mV MIN
Power Consumption	P_d	$V_O = 0V$	—	90	—	90	90	mW MAX

NOTE:
For 25°C characteristics of NT and GT devices, see N and G characteristics, respectively.

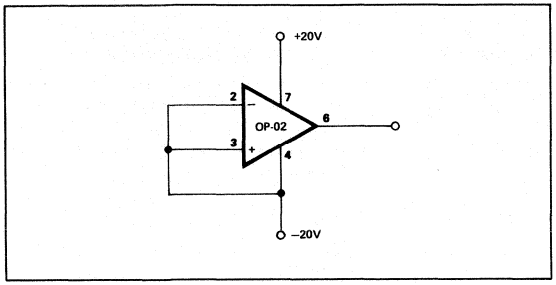
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

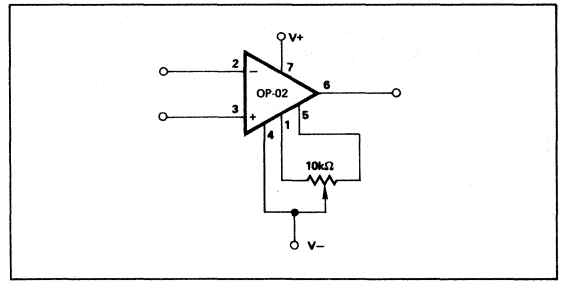
PARAMETER	SYMBOL	CONDITIONS	OP-02NT OP-02N TYPICAL	OP-02GT OP-02G TYPICAL	OP-02GR TYPICAL	UNITS
Input Resistance Differential-Mode	R_{IN}		5.7	5.2	3.5	MΩ
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	0.65	0.65	0.65	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$ $f_O = 100Hz$ $f_O = 1000Hz$	25 22 21	25 22 21	25 22 21	$nV/\sqrt{Hz}$
Input Noise Current	I_{np-p}	0.1Hz to 10Hz	12.8	12.8	12.8	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10Hz$ $f_O = 100Hz$ $f_O = 1000Hz$	1.4 0.7 0.4	1.4 0.7 0.4	1.4 0.7 0.4	$pA/\sqrt{Hz}$
Slew Rate	SR		0.5	0.5	0.5	V/μs
Large-Signal Bandwidth		$V_O = 20V_{p-p}$	8	8	8	kHz
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$	1.3	1.3	1.3	MHz
Risetime	t_r	$A_V = +1$ $V_{IN} = 50mV$	200	200	200	ns
Overshoot	OS		15	15	15	%
Average Input Offset Voltage Drift	TCV_{OS}	$R_S = 500\Omega$ (Note 1)	2	4	8	μV/°C
Average Input Offset Current Drift	TCI_{OS}		7.5	15	30	pA/°C

NOTE:
1. Sample tested.

BURN-IN CIRCUIT



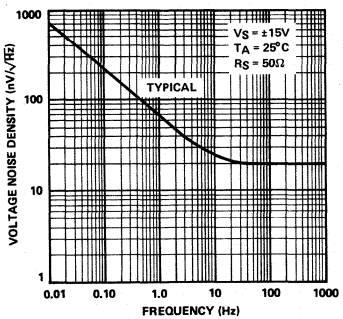
OFFSET NULLING CIRCUIT



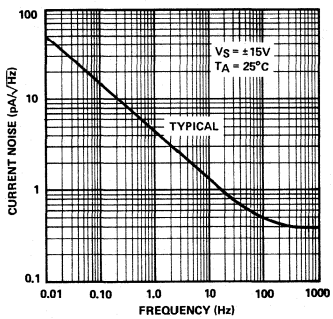
2

TYPICAL PERFORMANCE CHARACTERISTICS

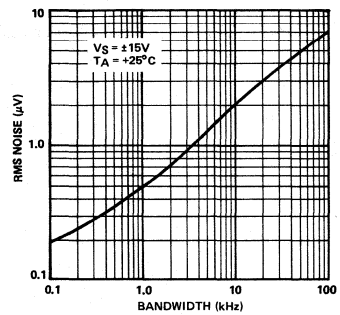
INPUT SPOT NOISE VOLTAGE vs FREQUENCY



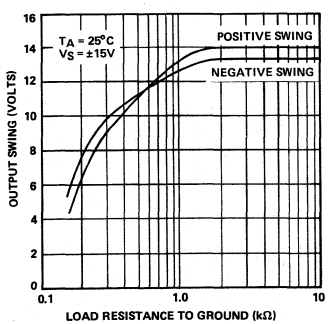
INPUT SPOT NOISE CURRENT vs FREQUENCY



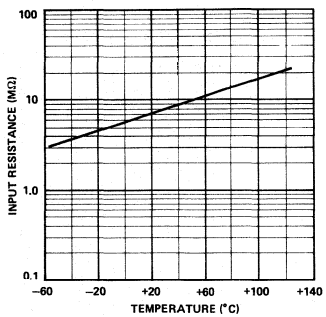
INPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



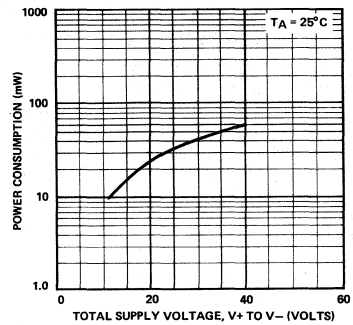
OUTPUT VOLTAGE vs LOAD RESISTANCE



DIFFERENTIAL INPUT RESISTANCE vs TEMPERATURE



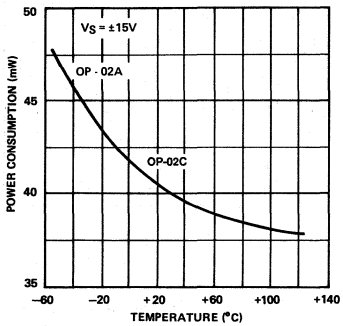
POWER CONSUMPTION vs POWER SUPPLY



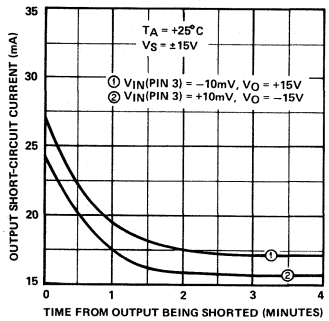
OP-02

TYPICAL PERFORMANCE CHARACTERISTICS

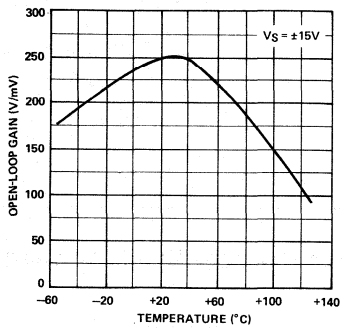
POWER CONSUMPTION vs TEMPERATURE



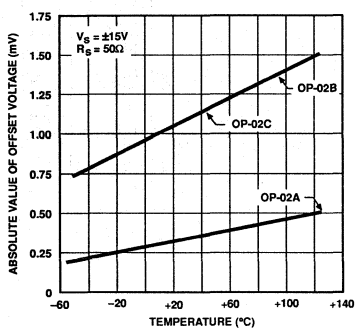
OUTPUT SHORT-CIRCUIT CURRENT vs TIME



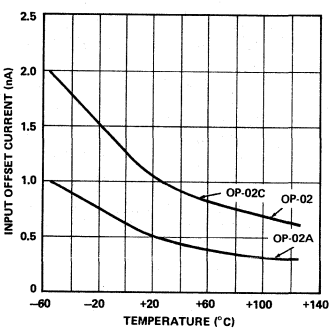
OPEN-LOOP GAIN vs TEMPERATURE



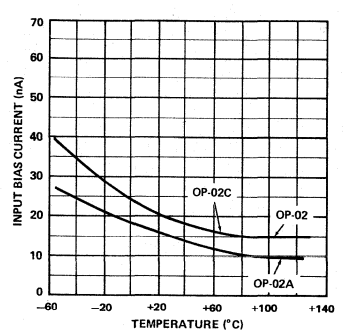
UNTRIMMED OFFSET VOLTAGE vs TEMPERATURE



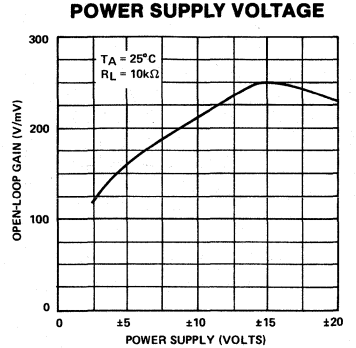
INPUT OFFSET CURRENT vs TEMPERATURE



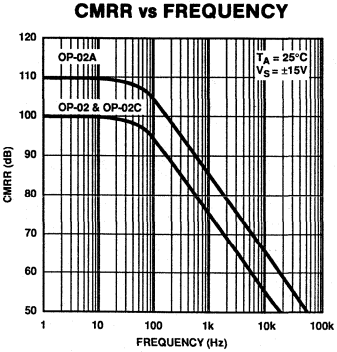
INPUT BIAS CURRENT vs TEMPERATURE



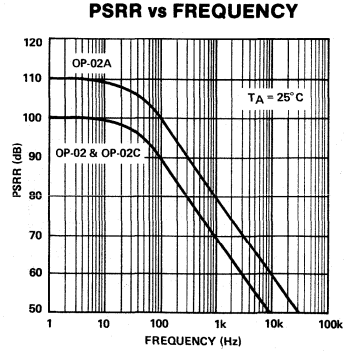
OPEN-LOOP GAIN vs POWER SUPPLY VOLTAGE



CMRR vs FREQUENCY

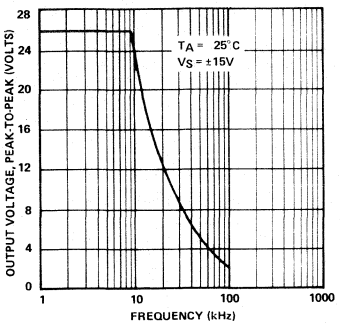


PSRR vs FREQUENCY

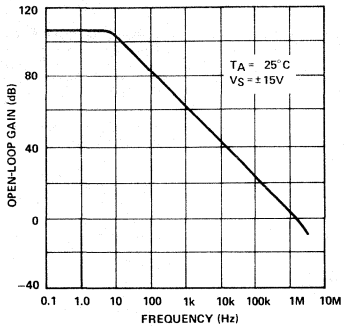


TYPICAL PERFORMANCE CHARACTERISTICS

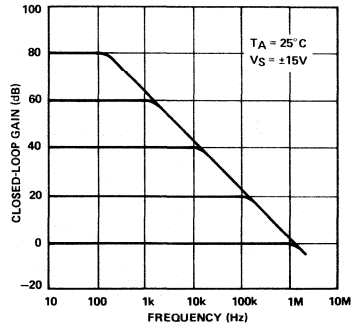
MAXIMUM UNDISTORTED OUTPUT vs FREQUENCY



OPEN-LOOP FREQUENCY RESPONSE



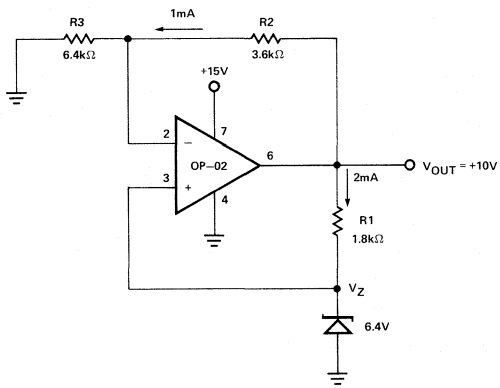
CLOSED-LOOP RESPONSE FOR VARIOUS GAIN CONFIGURATIONS



2

TYPICAL APPLICATIONS

HIGH-STABILITY VOLTAGE REFERENCE

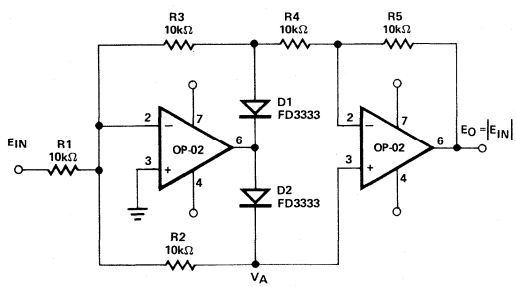


$$V_{OUT} = \left(1 + \frac{R_2}{R_3}\right) V_Z$$

FOR R2 = 3.6kΩ AND R3 = 6.4kΩ,
V_{OUT} = 1.5625V_Z

IF V_Z = 6.4V, THEN
V_{OUT} = +10V

ABSOLUTE VALUE CIRCUIT



DESIGN EQUATIONS

POSITIVE INPUT

1. V_A = 0, D2 OFF, D1 ON
2. $E_O = \left(\frac{-E_{IN}R3}{R1}\right) \bullet \left(\frac{-R5}{R4}\right) = E_{IN}\frac{R3}{R1}\frac{R5}{R4}$
3. With R1 = R3 = R4 = R5: $E_O = E_{IN}$
4. V_{OS} error included: $E_O = E_{IN} + 2V_{OS}$

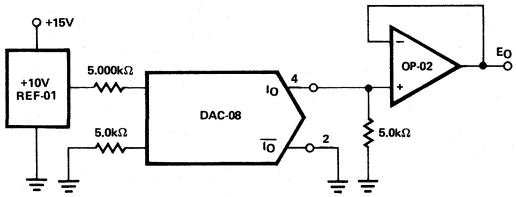
NEGATIVE INPUT

1. D1 OFF, D2 ON
2. $\frac{-E_{IN}}{R1} = \frac{V_A}{R2} + \frac{V_A}{R3 + R4}$
3. $E_O = V_A \left(1 + \frac{R5}{R3 + R4}\right)$
4. With R3 = R4 = R5: $E_O = 1.5V_A$
5. $E_O = -\frac{(R2)\ (R3 + R4)\ (1.5)\ E_{IN}}{R1\ (R2 + R3 + R4)}$
6. With R1 = R2 = R3 = R4: $E_O = -E_{IN}$
7. V_{OS} error included: $E_O = -E_{IN} + 1.5V_{OS2} - 0.5V_{OS1}$
8. For both inputs: $E_O = +|E_{IN}|$

OP-02

TYPICAL APPLICATIONS

DAC-08 OUTPUT AMPLIFIER



FOR COMPLEMENTARY OUTPUT (OPERATION AS A NEGATIVE LOGIC DAC) CONNECT NON-INVERTING INPUT OF OP-AMP TO $\overline{I_O}$ (PIN 2), CONNECT I_O (PIN 4) TO GROUND.

INPUT/OUTPUT TABLE

	B1	B2	B3	B4	B5	B6	B7	B8	I_OmA	E_O
FULL-SCALE −1 LSB	1	1	1	1	1	1	1	1	1.992	−9.960
FULL-SCALE −2 LSB	1	1	1	1	1	1	1	0	1.984	−9.920
HALF-SCALE +LSB	1	0	0	0	0	0	0	1	1.008	−5.040
HALF-SCALE	1	0	0	0	0	0	0	0	1.000	−5.000
HALF-SCALE −LSB	0	1	1	1	1	1	1	1	0.992	−4.960
ZERO-SCALE +LSB	0	0	0	0	0	0	0	1	0.0008	−0.040
ZERO-SCALE	0	0	0	0	0	0	0	0	0.000	0.000

ANALOG DEVICES

Dual Matched High Performance Operational Amplifiers

OP-04/OP-14

FEATURES

- **Excellent DC Input Specifications**
- **Matched V_{OS} and CMRR**
- **OP-14 Fits Standard 1458/1558 Sockets**
- **Internally Compensated**
- **Low Noise**
- **Low Drift**
- **Low Cost**
- **0°C/ +70°C and −55°C/ +125°C Models**
- **Silicon-Nitride Passivation**
- **Models with MIL-STD-883 Class B Processing Available From Stock**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (mV)	PACKAGE					OPERATING TEMPERATURE RANGE
	TO-99	TO-100	CERDIP 8-PIN	CERDIP 14-PIN	PLASTIC 8-PIN	
0.75	OP14AJ*	OP04AK*	OP14AZ*	OP14AY*	–	MIL
0.75	OP14EJ	–	OP14EZ	OP04EY	OP14EP	COM
2.0	OP14J	OP04K*	OP14Z*	OP04AY	–	MIL
2.0	OP14CJ	OP04CK	OP14CZ	OP04CY	OP14CP	XIND
2.0	–	–	–	–	OP14CS	XIND
5.0	–	OP04BK	–	–	–	MIL
5.0	OP14DJ	–	–	–	OP14DP	XIND

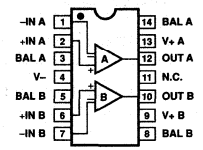
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

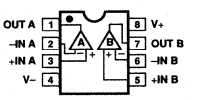
GENERAL DESCRIPTION

The OP-04/OP-14 series of dual general-purpose operational amplifiers provides significant improvements over industry-standard 747 and 1458/1558 (OP-14) types while maintaining pin-for-pin compatibility, ease of application, and low cost. Key specifications, such as V_{OS}, I_{OS}, I_B, CMRR, PSRR and A_{VO}, are guaranteed over the full operating temperature range. Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process reduces "popcorn noise". A thermally-symmetrical input stage design provides low TCV_{OS}, TCI_{OS}, and insensitivity to output load conditions. This series is ideal for upgrading existing designs where accuracy improvements are desired. For more stringent requirements, refer to the OP-200, OP-207, OP-220, or OP-221 dual-matched operational amplifier data sheets.

PIN CONNECTIONS



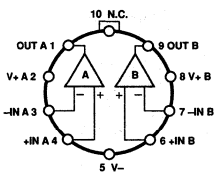
14-PIN HERMETIC DIP (Y-Suffix) OP-04



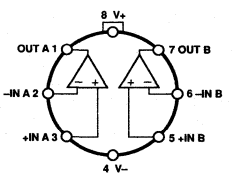
8-PIN HERMETIC DIP (Z-Suffix) OP-14

EPOXY MINI-DIP (P-Suffix) OP-14

8-PIN SO (S-Suffix) OP-14

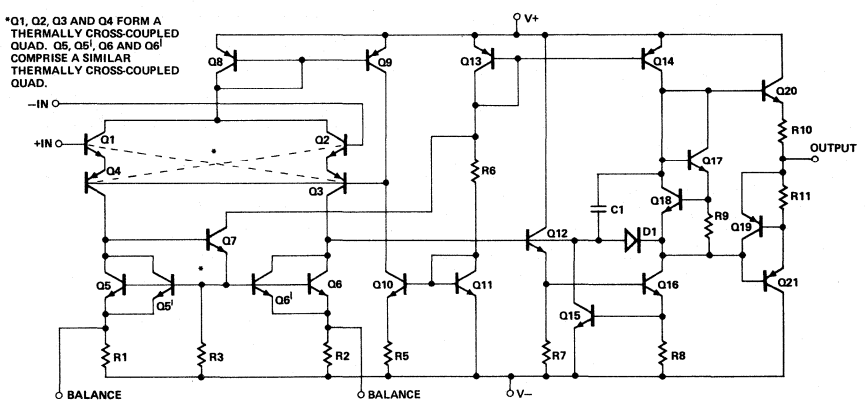


TO-100 (K-Suffix) OP-04



TO-99 (J-Suffix) OP-14

SIMPLIFIED SCHEMATIC (Each Amplifier)



BALANCE ACCESSIBLE WITH OP-04 IN 14-PIN HERMETIC DIP ONLY.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±22V
Differential Input Voltage ..... ±30V
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range
J, K, Y, and Z Packages ..... –65°C to +150°C
P Package ..... –65°C to +125°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Operating Temperature Range
A, Plain, B-Suffix ..... –55°C to +125°C
E-Suffix ..... 0°C to +70°C
C, D-Suffix ..... –40°C to +85°C
Junction Temperature (T_j) ..... –65°C to +150°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
TO-100 (K)	142	21	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
14-Pin Hermetic DIP (Y)	108	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP, and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-04A OP-04E OP-14A OP-14E MIN	TYP	MAX	OP-04 OP-04C OP-14 OP-14C MIN	TYP	MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}	$R_S \leq 20k\Omega$	—	0.3	1	—	1	2	mV
Common-Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm 10V$, $R_S \leq 100\Omega$	94	106	—	94	106	—	dB

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$ for OP-04A, OP-14A, OP-04 and OP-14, $0°C \leq T_A \leq +70°C$ for OP-04E, OP-14E, $-40°C \leq T_A \leq +85°C$ for OP-04C and OP-14C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-04A OP-04E OP-14A OP-14E MIN	TYP	MAX	OP-04 OP-04C OP-14 OP-14C MIN	TYP	MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}	$R_S \leq 20k\Omega$	—	0.5	1.5	—	1.5	3	mV
Common-Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm 10V$, $R_S \leq 100\Omega$	90	100	—	90	100	—	dB

ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-04A/OP-14A MIN	TYP	MAX	OP-04/OP-14 MIN	TYP	MAX	OP-04B MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.3	0.75	—	1	2	—	3	5	mV
Input Offset Current	I_{OS}		—	0.5	5	—	1	5	—	5	25	nA
Input Bias Current	I_B		—	18	50	—	20	75	—	30	100	nA
Input Resistance — Differential-Mode	R_{IN}	(Note 3)	2.0	7.5	—	1.35	7	—	1	5	—	MΩ
Input Voltage Range	IVR		±10	±13	—	±10	±13	—	±10	±13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	85	100	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	10	60	—	30	100	—	100	150	μV/V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	—	±12	±13	—	±12	±13	—	V

ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-04A/OP-14A MIN	OP-04A/OP-14A TYP	OP-04A/OP-14A MAX	OP-04/OP-14 MIN	OP-04/OP-14 TYP	OP-04/OP-14 MAX	OP-04B MIN	OP-04B TYP	OP-04B MAX	UNITS
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	100	250	—	50	200	—	25	200	—	V/mV
Power Consumption (Note 2)	P_d	$V_O = 0V$	—	50	90	—	50	90	—	50	90	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.65	—	—	0.65	—	—	0.65	—	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$ $f_O = 100Hz$ $f_O = 1000Hz$	— — —	25 22 21	— — —	— — —	25 22 21	— — —	— — —	25 22 21	— — —	$nV/\sqrt{Hz}$
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	—	12.8	—	—	12.8	—	—	12.8	—	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10Hz$ $f_O = 100Hz$ $f_O = 1000Hz$	— — —	1.4 0.7 0.4	— — —	— — —	1.4 0.7 0.4	— — —	— — —	1.4 0.7 0.4	— — —	$pA/\sqrt{Hz}$
Channel Separation	CS		100	—	—	100	—	—	80	—	—	dB
Slew Rate (Note 1)	SR	$R_L = 2k\Omega$, $C_L = 100pF$	0.25	0.5	—	0.25	0.5	—	0.25	0.5	—	V/μs
Large-Signal Bandwidth (Notes 1, 5)		$V_O = 20V_{p-p}$	4	8	—	4	8	—	4	8	—	kHz
Closed-Loop Bandwidth (Note 4)	BW	$A_{VCL} = +1.0$	1.0	1.3	—	1.0	1.3	—	1.0	1.3	—	MHz
Risetime (Note 1)	t_r	$A_V = +1$, $V_{IN} = 50mV_{p-p}$ $R_L = 2k\Omega$, $C_L = 50pF$	—	260	350	—	260	350	—	260	350	ns
Overshoot (Note 1)	OS	$A_V = +1$, $V_{IN} = 50mV_{p-p}$ $R_L = 2k\Omega$, $C_L = 50pF$	—	5	10	—	5	10	—	5	10	%

ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-04A/OP-14A MIN	OP-04A/OP-14A TYP	OP-04A/OP-14A MAX	OP-04/OP-14 MIN	OP-04/OP-14 TYP	OP-04/OP-14 MAX	OP-04B MIN	OP-04B TYP	OP-04B MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.4	1.5	—	1.2	3	—	3	6	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	$R_S = 50\Omega$	—	2	8	—	4	10	—	8	20	μV/°C
Input Offset Current	I_{OS}		—	1	10	—	2	10	—	10	50	nA
Average Input Offset Current Drift (Note 1)	TCI_{OS}		—	7.5	120	—	15	250	—	70	500	pA/°C
Input Bias Current	I_B		—	30	60	—	40	100	—	50	200	nA
Input Voltage Range	IVR		±10	±13	—	±10	±13	—	±10	±13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	80	100	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	10	60	—	30	100	—	100	150	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	50	100	—	25	60	—	25	60	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	—	±12	±13	—	±10	±13	—	V

NOTES:
1. Sample tested.
2. Power dissipation per amplifier.
3. Guaranteed by input bias current.
4. Guaranteed by maximum risetime.
5. Guaranteed by minimum slew rate.

ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-04E/OP-14E MIN	OP-04E/OP-14E TYP	OP-04E/OP-14E MAX	OP-04C/OP-14C MIN	OP-04C/OP-14C TYP	OP-04C/OP-14C MAX	OP-14D MIN	OP-14D TYP	OP-14D MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.3	0.75	—	1	2	—	3	5	mV
Input Offset Current	I_{OS}		—	0.5	5	—	1	5	—	5	25	nA
Input Bias Current	I_B		—	18	50	—	20	75	—	30	100	nA
Input Resistance — Differential-Mode	R_{IN}	(Note 3)	2.0	7.5	—	1.35	7	—	1	5	—	MΩ
Input Voltage Range	IVR		±10	±13	—	±10	±13	—	±10	±13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	85	100	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	10	60	—	30	100	—	100	150	μV/V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	—	±12	±13	—	±12	±13	—	V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	100	250	—	50	200	—	25	150	—	V/mV
Power Consumption (Note 2)	P_d	$V_O = 0V$	—	50	90	—	50	90	—	50	90	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.65	—	—	0.65	—	—	0.65	—	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$ $f_O = 100Hz$ $f_O = 1000Hz$	— — —	25 22 21	— — —	— — —	25 22 21	— — —	— — —	25 22 21	— — —	$nV/\sqrt{Hz}$
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	—	12.8	—	—	12.8	—	—	12.8	—	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10Hz$ $f_O = 100Hz$ $f_O = 1000Hz$	— — —	1.4 0.7 0.4	— — —	— — —	1.4 0.7 0.4	— — —	— — —	1.4 0.7 0.4	— — —	$pA/\sqrt{Hz}$
Channel Separation	CS		100	—	—	100	—	—	80	—	—	dB
Slew Rate (Note 1)	SR	$R_L = 2k\Omega$, $C_L = 100pF$	0.25	0.5	—	0.25	0.5	—	0.25	0.5	—	V/μs
Large-Signal Bandwidth (Notes 1, 5)		$V_O = 20V_{p-p}$	4	8	—	4	8	—	4	8	—	kHz
Closed-Loop Bandwidth (Note 4)	BW	$A_{VCL} = +1$	0.8	1.3	—	0.8	1.3	—	0.8	1.3	—	MHz
Risetime (Note 1)	t_r	$A_V = +1$, $V_{IN} = 50mV$ $R_L = 2k\Omega$, $C_L = 50pF$	—	260	350	—	260	350	—	260	350	ns
Overshoot (Note 1)	OS	$A_V = +1$, $V_{IN} = 50mV$ $R_L = 2k\Omega$, $C_L = 50pF$	—	5	10	—	5	10	—	5	10	%

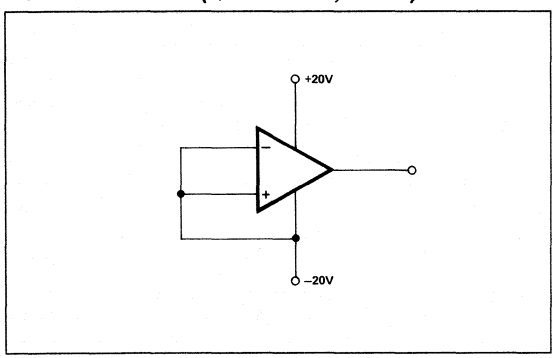
NOTES:
1. Sample tested.
2. Power dissipation per amplifier.
3. Guaranteed by input bias current.
4. Guaranteed by maximum risetime.
5. Guaranteed by minimum slew rate.

ELECTRICAL CHARACTERISTICS (Each Amplifier) at V_S = ±15V, 0°C ≤ T_A ≤ +70°C for E, –40°C to +85° for C and D, unless otherwise noted.

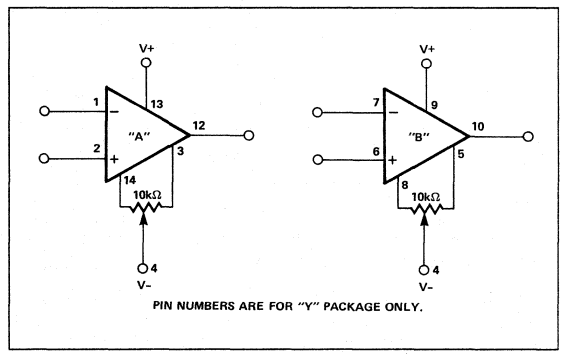
			OP-04E/OP-14E			OP-04C/OP-14C			OP-14D			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.4	1.5	—	1.2	3	—	3	6	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	$R_S = 50\Omega$	—	2	8	—	4	10	—	8	20	µV/°C
Input Offset Current	I_{OS}		—	1	10	—	2	10	—	10	50	nA
Average Input Offset Current Drift (Note 1)	TCI_{OS}		—	7.5	120	—	15	250	—	70	500	pA/°C
Input Bias Current	I_B		—	30	60	—	40	100	—	50	200	nA
Input Voltage Range	IVR		±10	±13	—	±10	±13	—	±10	±13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	80	100	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	10	60	—	30	100	—	100	150	µV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	50	100	—	25	60	—	15	25	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	—	±12	±13	—	±10	±13	—	V

NOTES:
1. Sample tested.

BURN-IN CIRCUIT (1/2 of OP-04, OP-14)

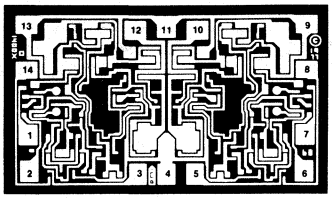


OFFSET ADJUST CIRCUIT



OP-04/OP-14

DICE CHARACTERISTICS



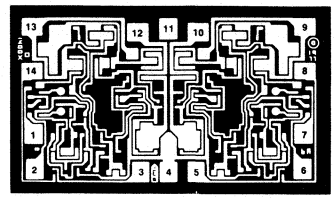
OP-14

DIE SIZE 0.080 × 0.050 inch, 4000 sq. mils (2.03 × 1.27 mm, 2.58 sq. mm)

1. INVERTING INPUT (A)
2. NONINVERTING INPUT (A)
3. BALANCE (A)
4. V–
5. BALANCE (B)
6. NONINVERTING INPUT (B)
7. INVERTING INPUT (B)
8. BALANCE (B)
9. V+
10. OUTPUT (B)
11. V+
12. OUTPUT (A)
13. V+
14. BALANCE (A)

NOTE: 9, 11 and 13 are internally connected.

OP-04



1. INVERTING INPUT (A)
2. NONINVERTING INPUT (A)
3. BALANCE (A)
4. V–
5. BALANCE (B)
6. NONINVERTING INPUT (B)
7. INVERTING INPUT (B)
8. BALANCE (B)
9. V+ (B)
10. OUTPUT (B)
11. NO CONNECTIONS
12. OUTPUT (A)
13. V+ (A)
14. BALANCE (A)

WAFER TEST LIMITS at $V_S = \pm15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-04N OP-14N LIMIT	OP-14G LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \le 20k\Omega$	0.75	2	mV MAX
Input Offset Voltage Match	ΔV_{OS}	$R_S \le 20k\Omega$	1	2	mV MAX
Input Offset Current	I_{OS}		5	5	nA MAX
Input Bias Current	I_B		50	75	nA MAX
Input Voltage Range	IVR		±10	±10	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm10V$ $R_S \le 20k\Omega$	85	80	dB MIN
Common-Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm10V$ $R_S \le 100\Omega$	94	94	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm5V$ to $\pm20V$ $R_S \le 20k\Omega$	60	100	µV/V MAX
Output Voltage Swing	V_O	$R_L \ge 10k\Omega$ $R_L \ge 2k\Omega$	±12 ±12	±12 ±12	V MIN
Large-Scale Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$ $V_O = \pm10V$	100	50	V/mV MIN
Power Consumption (Both Amplifiers)	P_d	$V_O = 0$	170	170	mW MAX
Channel Separation	CS		100	100	dB MIN

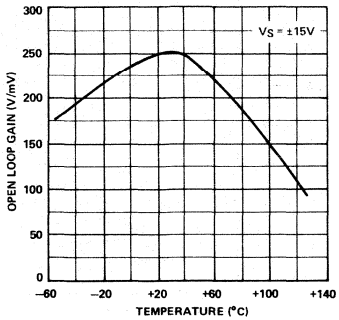
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $T_A = +25°C$, unless otherwise noted.

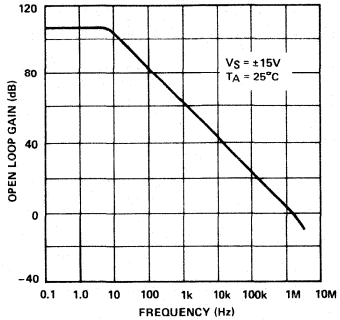
PARAMETER	SYMBOL	CONDITIONS	OP-04N OP-14N LIMIT	OP-04G OP-14G LIMIT	UNITS
Risetime	t_r	$A_V = +1$, $V_{IN} = 50mV$, $R_L = 2k\Omega$, $C_L = 50pF$	200	200	ns
Overshoot	OS	$A_V = +1$, $V_{IN} = 50mV$, $R_L = 2k\Omega$, $C_L = 50pF$	5	5	%
Slew Rate	SR	$R_L = 2k\Omega$, $C_L = 100pF$	0.25	0.25	V/µs

TYPICAL PERFORMANCE CHARACTERISTICS (Each Amplifier)

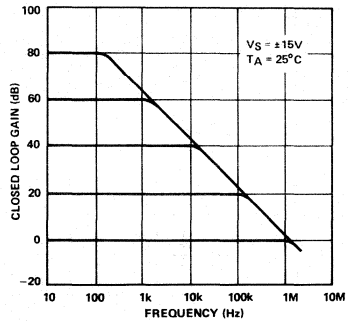
OPEN-LOOP GAIN vs TEMPERATURE



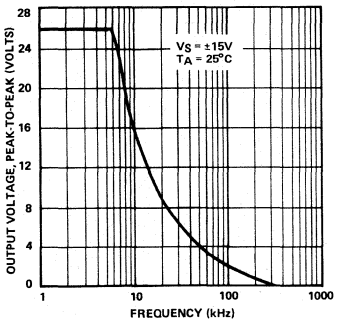
OPEN-LOOP FREQUENCY RESPONSE



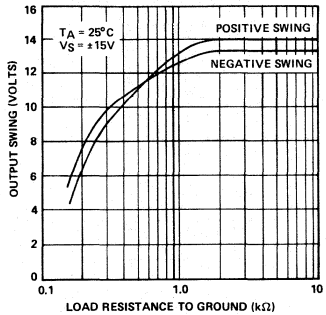
CLOSED-LOOP RESPONSE FOR VARIOUS GAIN CONFIGURATIONS



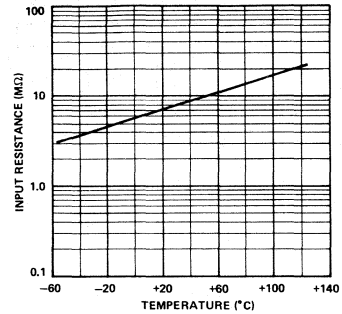
MAXIMUM UNDISTORTED OUTPUT vs FREQUENCY



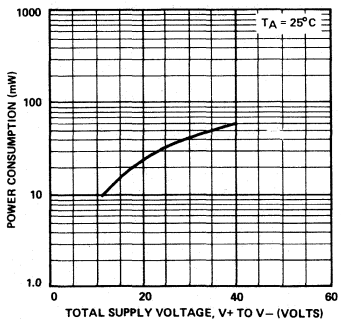
OUTPUT VOLTAGE vs LOAD RESISTANCE



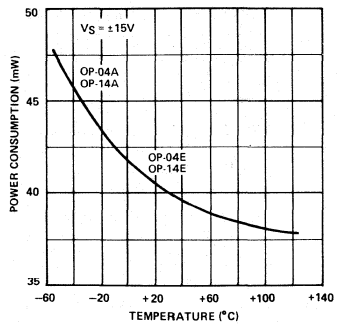
INPUT RESISTANCE vs TEMPERATURE



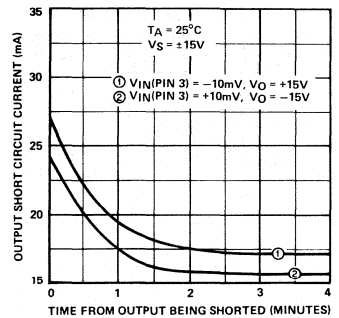
POWER CONSUMPTION vs POWER SUPPLY



POWER CONSUMPTION vs TEMPERATURE

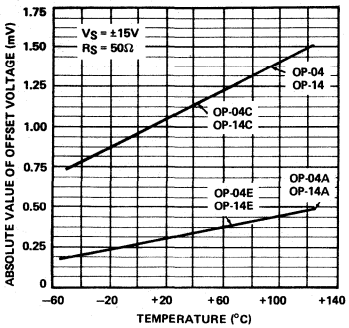


OUTPUT SHORT-CIRCUIT CURRENT vs TIME

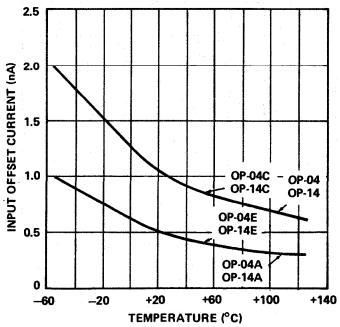


TYPICAL PERFORMANCE CHARACTERISTICS (Each Amplifier)

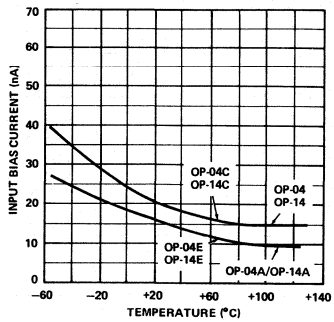
UNTRIMMED OFFSET VOLTAGE vs TEMPERATURE



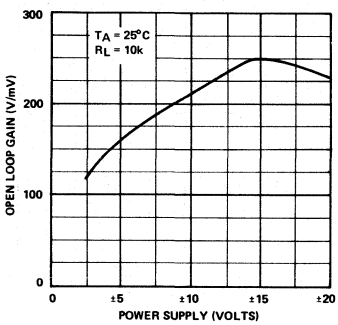
INPUT OFFSET CURRENT vs TEMPERATURE



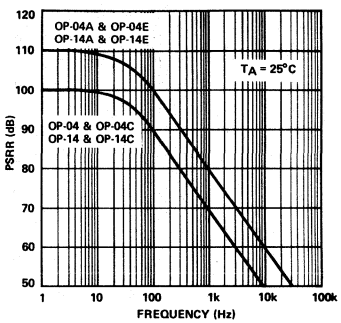
INPUT BIAS CURRENT vs TEMPERATURE



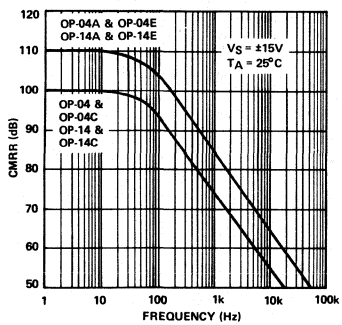
OPEN-LOOP GAIN vs POWER SUPPLY VOLTAGE



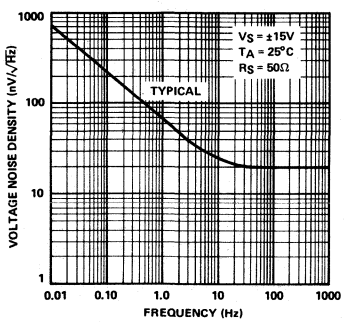
PSRR vs FREQUENCY



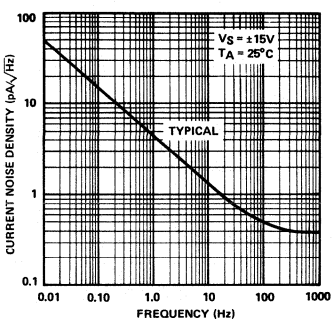
CMRR vs FREQUENCY



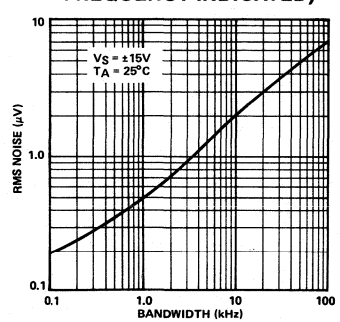
INPUT SPOT NOISE VOLTAGE vs FREQUENCY



INPUT SPOT NOISE CURRENT vs FREQUENCY



INPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



ANALOG DEVICES

Instrumentation Operational Amplifier

OP-05

FEATURES

- **Low Noise** ..... **0.6μV_{p-p} Max, 0.1 to 10Hz**
- **Low Drift vs. Temperature** ..... **0.5μV/°C Max**
- **Low Drift vs. Time** ..... **0.2μV/Month Typ**
- **Low Bias Current** ..... **2.0nA Max**
- **High CMRR** ..... **114dB Min**
- **High PSRR** ..... **100dB Min**
- **High Gain** ..... **300,000 Min**
- **High R_{IN} Differential** ..... **30MΩ Min**
- **High R_{IN} CM** ..... **200GΩ Typ**
- **Internally Compensated** ..... **Stable to 500pF Load**
- **Fits 725, 108A and 741 Sockets**
- **125°C Temperature Tested Dice**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = 25°C V_{OS} MAX (mV)	PACKAGE TO-99	PACKAGE CERDIP 8-PIN	PACKAGE PLASTIC 8-PIN	OPERATING TEMPERATURE RANGE
0.15	OP05AJ*	OP05AZ*	–	MIL
0.5	OP05J*	–	–	MIL
0.5	OP05EJ	OP05EZ	OP05EP	COM
1.3	OP05CJ	OP05CZ	OP05CP	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

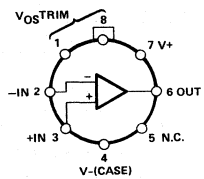
† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

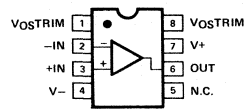
The OP-05 series of monolithic instrumentation operational amplifiers combine excellent performance in low-signal-level applications with the simplicity of use of a fully-protected, internally-compensated op amp. The OP-05 has low input offset voltage and bias current combined with very high levels of gain, input impedance, CMRR, and PSRR.

The OP-05 is a direct replacement in 725, 108A, and unnulled 741 sockets allowing instant system performance improvement without redesign. The OP-05 is an excellent choice for a wide variety of applications including strain gauge and thermocouple bridges, high-gain active filters, buffers, integrators, and sample-and-hold amplifiers. For dual-matched versions, refer to the OP-207 and OP-10 data sheets.

PIN CONNECTIONS



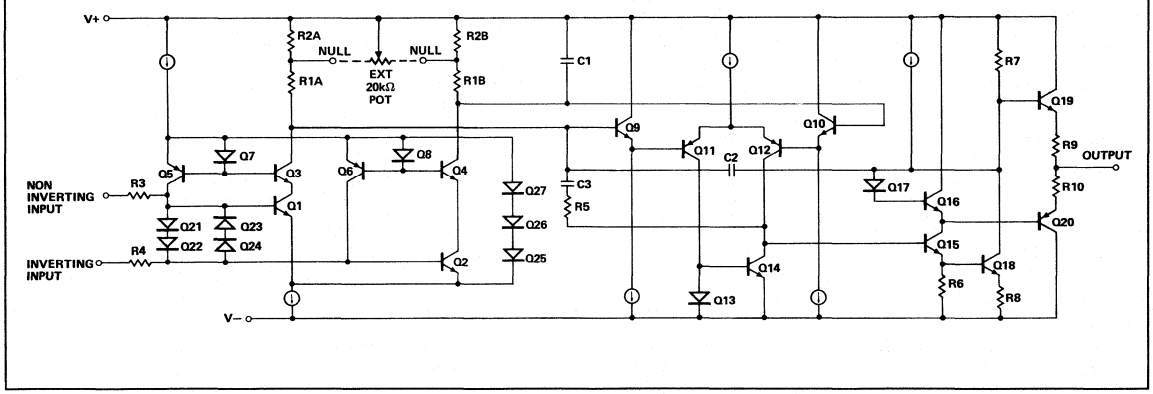
TO-99
(J-Suffix)



EPOXY MINI-DIP
(P-Suffix)

8-PIN HERMETIC DIP
(Z-Suffix)

SIMPLIFIED SCHEMATIC



OP-05

ABSOLUTE MAXIMUM RATINGS (Note 3)

Supply Voltage ..... ±22V
Differential Input Voltage ..... ±30V
Input Voltage (Note 1) ..... ±22V
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range
J and Z Packages ..... −65°C to +150°C
P Package ..... −65°C to +125°C
Operating Temperature Range
OP-05A, OP-05 ..... −55°C to +125°C
OP-05E, OP-05C ..... 0°C to +70°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature ..... −65°C to +150°C

PACKAGE TYPE	Θ_{JA} (NOTE 2)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W

NOTES:
1. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO and PLCC packages.
3. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-05A			OP-05			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.07	0.15	—	0.2	0.5	mV
Long-Term Input Offset Voltage Stability	ΔV_{OS}/Time	(Note 1)	—	0.2	1.0	—	0.2	1.0	μV/Mo
Input Offset Current	I_{OS}		—	0.7	2.0	—	1.0	2.8	nA
Input Bias Current	I_B		—	±0.7	±2.0	—	±1.0	±3.0	nA
Input Noise Voltage (Note 2)	e_{np-p}	0.1Hz to 10Hz	—	0.35	0.6	—	0.35	0.6	μV_{p-p}
Input Noise Voltage Density (Note 2)	e_n	$f_O = 10Hz$ $f_O = 100Hz$ $f_O = 1000Hz$	— — —	10.3 10.0 9.6	18.0 13.0 11.0	— — —	10.3 10.0 9.6	18.0 13.0 11.0	$nV/\sqrt{Hz}$
Input Noise Current (Note 2)	i_{np-p}	0.1Hz to 10Hz	—	14	30	—	14	30	pA_{p-p}
Input Noise Current Density (Note 2)	i_n	$f_O = 10Hz$ $f_O = 100Hz$ $f_O = 1000Hz$	— — —	0.32 0.14 0.12	0.80 0.23 0.17	— — —	0.32 0.14 0.12	0.80 0.23 0.17	$pA/\sqrt{Hz}$
Input Resistance — Differential-Mode	R_{IN}	(Note 3)	30	80	—	20	60	—	MΩ
Input Resistance — Common-Mode	R_{INCM}		—	200	—	—	200	—	GΩ
Input Voltage Range	IVR		±13.5	±14.0	—	±13.5	±14.0	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$	114	126	—	114	126	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	4	10	—	4	10	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$ $R_L \geq 500\Omega$, $V_O = \pm 0.5V$ $V_S = \pm 3V$ (Note 3)	300 150	500 500	— —	200 150	500 500	— —	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0	— — —	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0	— — —	V
Slew Rate (Note 2)	SR	$R_L \geq 2k\Omega$	0.1	0.3	—	0.1	0.3	—	V/μs
Closed-Loop Bandwidth (Note 2)	BW	$A_{VCL} = +1.0$	0.4	0.6	—	0.4	0.6	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	60	—	—	60	—	Ω
Power Consumption	P_d	No load $V_S = \pm 3V$, No load	— —	90 4	120 6	— —	90 4	120 6	mW
Offset Adjustment Range		$R_P = 20k\Omega$	—	4	—	—	4	—	mV

NOTES:
1. Long-term input offset voltage stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV. Refer to typical performance curve.
2. Sample tested.
3. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-05A MIN	OP-05A TYP	OP-05A MAX	OP-05 MIN	OP-05 TYP	OP-05 MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.10	0.24	—	0.3	0.7	mV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}	(Note 2)	—	0.3	0.9	—	0.7	2.0	µV/°C
With External Trim	TCV_{OSn}	$R_P = 20k\Omega$ (Note 3)	—	0.2	0.5	—	0.3	1.0	
Input Offset Current	I_{OS}		—	1.0	4.0	—	1.8	5.6	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	5	25	—	8	50	pA/°C
Input Bias Current	I_B		—	±1	±4	—	±2	±6	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	8	25	—	13	50	pA/°C
Input Voltage Range	IVR		±13.0	±13.5	—	±13.0	±13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.0V$	110	123	—	110	123	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	5	20	µV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	200	400	—	150	400	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.0	±12.6	—	±12.0	±12.6	—	V

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-05E MIN	OP-05E TYP	OP-05E MAX	OP-05C MIN	OP-05C TYP	OP-05C MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.2	0.5	—	0.3	1.3	mV
Long-Term Input Offset Voltage Stability	ΔV_{OS}/Time	(Notes 1, 2)	—	0.3	1.5	—	0.4	2.0	µV/Mo
Input Offset Current	I_{OS}		—	1.2	3.8	—	1.8	6.0	nA
Input Bias Current	I_B		—	±1.2	±4.0	—	±1.8	±7.0	nA
Input Noise Voltage (Note 2)	e_{np-p}	0.1Hz to 10Hz	—	0.35	0.6	—	0.38	0.65	μV_{p-p}
Input Noise Voltage Density (Note 2)	e_n	$f_O = 10Hz$	—	10.3	18.0	—	10.5	20.0	$nV/\sqrt{Hz}$
		$f_O = 100Hz$	—	10.0	13.0	—	10.2	13.5	
		$f_O = 1000Hz$	—	9.6	11.0	—	9.8	11.5	
Input Noise Current (Note 2)	i_{np-p}	0.1Hz to 10Hz	—	14	30	—	15	35	pA_{p-p}
Input Noise Current Density (Note 2)	i_n	$f_O = 10Hz$	—	0.32	0.80	—	0.35	0.90	$pA/\sqrt{Hz}$
		$f_O = 100Hz$	—	0.14	0.23	—	0.15	0.27	
		$f_O = 1000Hz$	—	0.12	0.17	—	0.13	0.18	
Input Resistance — Differential-Mode	R_{IN}	(Note 3)	15	50	—	8	33	—	MΩ
Input Resistance — Common-Mode	R_{INCM}		—	160	—	—	120	—	GΩ
Input Voltage Range	IVR		±13.5	±14.0	—	±13.0	±14.0	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$	110	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	7	32	µV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	200	500	—	120	400	—	V/mV
		$R_L \geq 500\Omega$, $V_O = \pm 0.5V$	150	500	—	100	400	—	
		$V_S = \pm 3V$ (Note 3)							
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	±12.5	±13.0	—	±12.0	±13.0	—	V
		$R_L \geq 2k\Omega$	±12.0	±12.8	—	±11.5	±12.8	—	
		$R_L \geq 1k\Omega$	±10.5	±12.0	—	—	±12.0	—	
Slew Rate (Note 2)	SR	$R_L = \geq 2k\Omega$	0.1	0.3	—	0.1	0.3	—	V/µs
Closed-Loop Bandwidth (Note 2)	BW	$A_{VCL} = +1.0$	0.4	0.6	—	0.4	0.6	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	60	—	—	60	—	Ω
Power Consumption	P_d	No load	—	90	120	—	95	150	mW
		$V_S = \pm 3V$, No load	—	4	6	—	4	8	
Offset Adjustment Range		$R_P = 20k\Omega$	—	4	—	—	4	—	mV

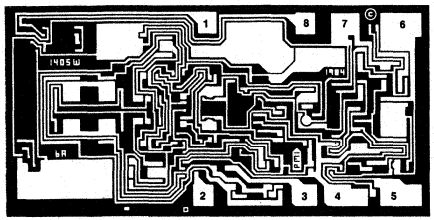
NOTE: See notes on previous page.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0°C \leq T_A \leq +70°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-05E MIN	OP-05E TYP	OP-05E MAX	OP-05C MIN	OP-05C TYP	OP-05C MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.25	0.6	—	0.35	1.6	mV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}	(Note 2)	—	0.7	2.0	—	1.3	4.5	µV/°C
With External Trim	TCV_{OSn}	$R_P = 20k\Omega$ (Note 3)	—	0.2	0.6	—	0.4	1.5	µV/°C
Input Offset Current	I_{OS}		—	1.4	5.3	—	2.0	8.0	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	8	35	—	12	50	pA/°C
Input Bias Current	I_B		—	±1.5	±5.5	—	±2.2	±9.0	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	13	35	—	18	50	pA/°C
Input Voltage Range	IVR		±13.0	±13.5	—	±13.0	±13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.0V$	107	123	—	97	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	7	32	—	10	51	µV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	180	450	—	100	400	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.0	±12.6	—	±11.0	±12.6	—	V

NOTES:
1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5µV. Refer to typical performance curve.
2. Sample tested.
3. Guaranteed by design.

DICE CHARACTERISTICS (125°C TESTED DICE AVAILABLE)



DIE SIZE 0.101 × 0.052 inch, 5300 sq. mils
(2.57 × 1.32 mm, 3.34 sq. mm)

1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V−
5. NO CONNECTION
6. OUTPUT
7. V+
8. BALANCE

2

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$ for OP-05N, OP-05G and OP-05GR devices; $T_A = 125°C$ for OP-05NT and OP-05GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-05NT LIMIT	OP-05N LIMIT	OP-05GT LIMIT	OP-05G LIMIT	OP-05GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		0.25	0.15	0.7	0.5	1.3	mV MAX
Input Offset Current	I_{OS}		4.0	2.0	5.7	3.8	6.0	nA MAX
Input Bias Current	I_B		±4	±2	±6	±4	±7	nA MAX
Input Resistance Differential Mode	R_{IN}	(Note 2)	—	20	—	15	8	MΩ MIN
Input Voltage Range	IVR		±13.0	±13.5	±13.0	±13.5	±13.0	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$ at +25°C $V_{CM} = \pm 13.0$ at +125°C	110	114	110	110	100	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	20	10	20	20	30	µV/V MAX
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$ $R_L = 1k\Omega$	— ±12.0 —	±12.5 ±12.0 ±10.5	— ±12.0 —	±12.5 ±12.0 ±10.5	±12.0 ±11.5 —	V MIN
Large-Signal Voltage Gain	A_{VO}	$R_L = 2k\Omega$ $V_O = \pm 10V$	200	200	150	200	120	V/mV MIN
Differential Input Voltage			±30	±30	±30	±30	±30	V MAX
Power Consumption	P_d	$V_{OUT} = 0V$	—	120	—	120	150	mW MAX

NOTES:
1. For 25°C characteristics of NT & GT devices see N & G characteristics respectively.
2. Guaranteed by design.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

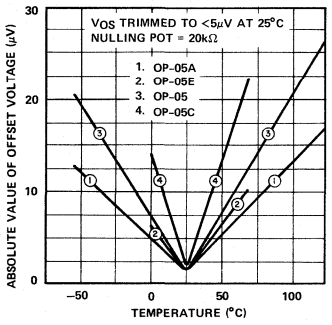
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-05NT TYPICAL	OP-05N TYPICAL	OP-05GT TYPICAL	OP-05G TYPICAL	OP-05GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	$R_S \leq 50\Omega$	0.3	0.3	0.7	0.7	1.2	µV/°C
Nulled Input Offset Voltage Drift	TCV_{OSn}	$R_S \leq 50\Omega$, $R_p = 20k\Omega$	0.2	0.2	0.3	0.3	0.4	µV/°C
Average Input Offset Current Drift	TCI_{OS}		5	5	8	8	12	pA/°C
Slew Rate	SR	$R_L \geq 2k\Omega$	0.3	0.3	0.3	0.3	0.3	V/µs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$	0.6	0.6	0.6	0.6	0.6	MHz

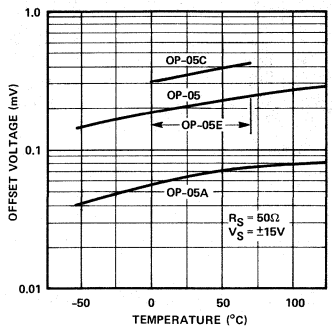
OP-05

TYPICAL PERFORMANCE CHARACTERISTICS

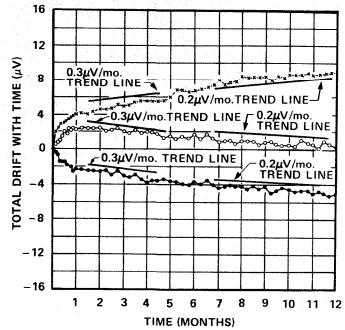
TRIMMED OFFSET VOLTAGE vs TEMPERATURE



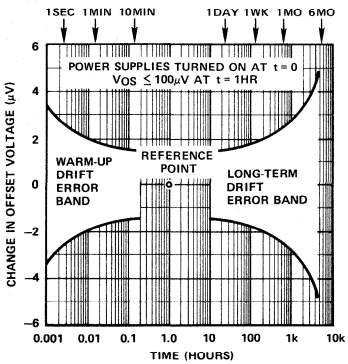
UNTRIMMED OFFSET VOLTAGE vs TEMPERATURE



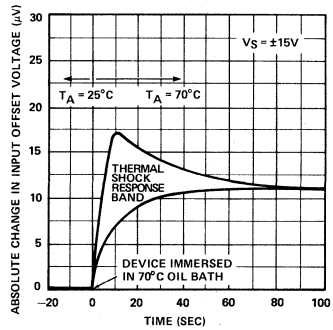
TYPICAL OFFSET VOLTAGE STABILITY vs TIME



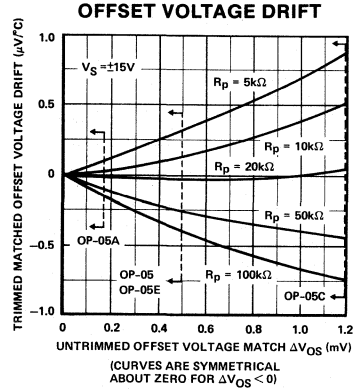
OFFSET VOLTAGE DRIFT WITH TIME



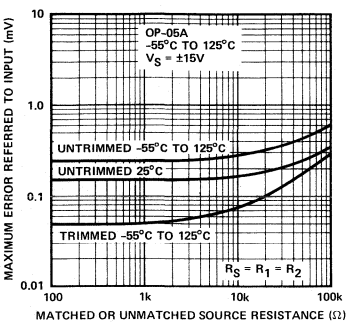
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



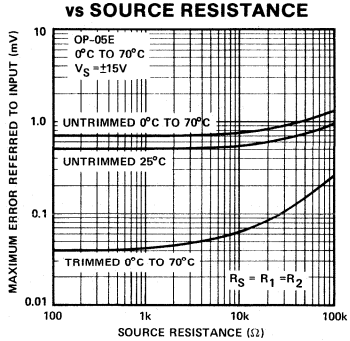
TRIMMED OFFSET VOLTAGE DRIFT



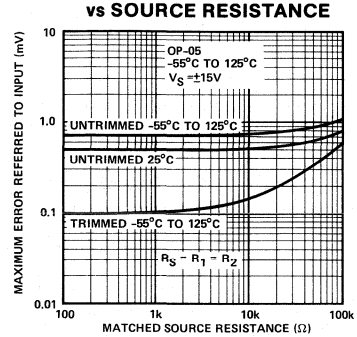
MAXIMUM ERROR vs SOURCE RESISTANCE



MAXIMUM ERROR vs SOURCE RESISTANCE

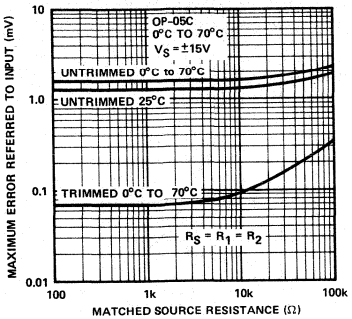


MAXIMUM ERROR vs SOURCE RESISTANCE

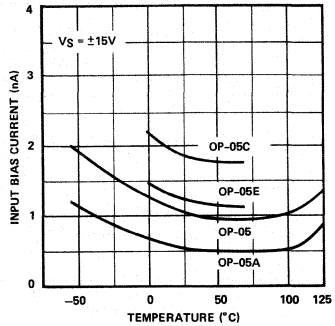


TYPICAL PERFORMANCE CHARACTERISTICS

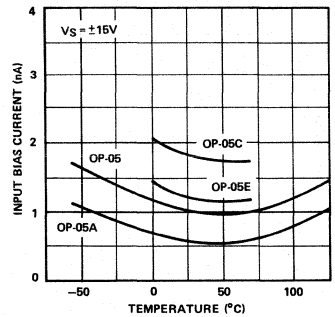
MAXIMUM ERROR vs SOURCE RESISTANCE



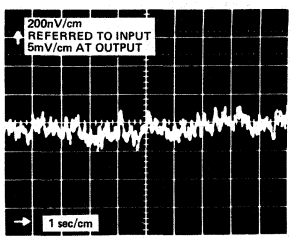
INPUT BIAS CURRENT vs TEMPERATURE



INPUT OFFSET CURRENT vs TEMPERATURE

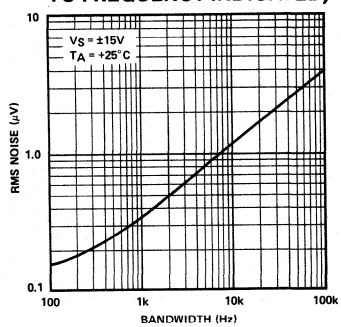


OP-05 LOW FREQUENCY NOISE

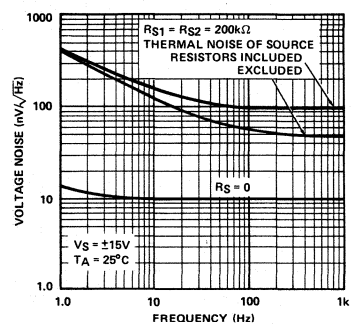


(SEE NOISE TEST CIRCUIT)

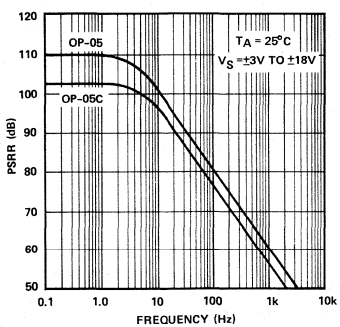
INPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



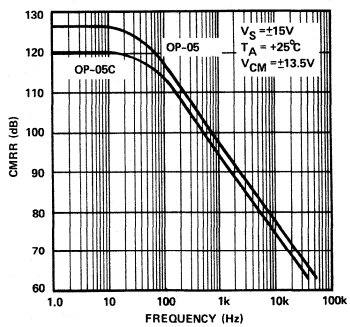
VOLTAGE NOISE DENSITY vs FREQUENCY



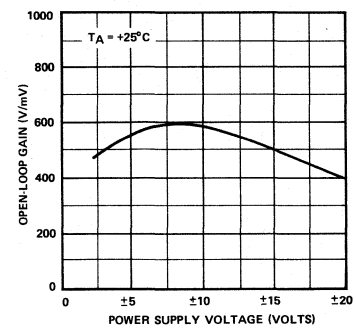
PSRR vs FREQUENCY



CMRR vs FREQUENCY



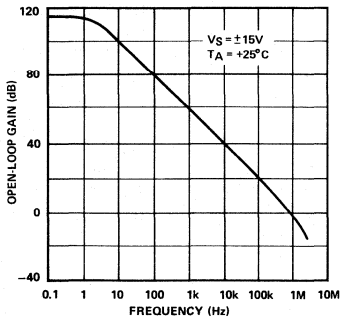
OPEN-LOOP GAIN vs POWER SUPPLY VOLTAGE



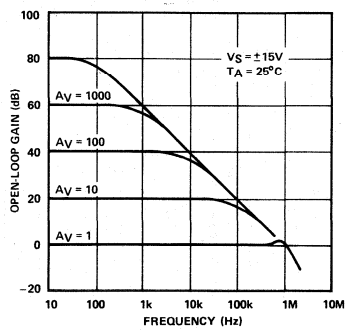
OP-05

TYPICAL PERFORMANCE CHARACTERISTICS

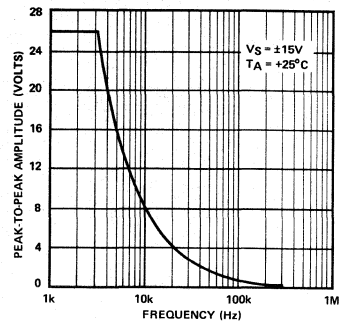
OPEN-LOOP GAIN vs FREQUENCY



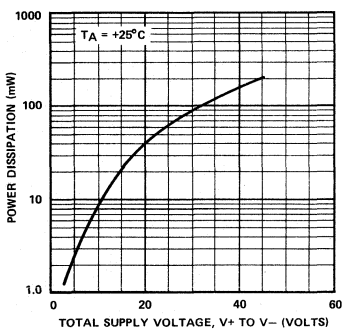
CLOSED-LOOP GAIN vs FREQUENCY



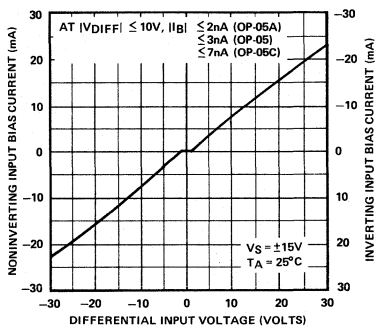
MAXIMUM OUTPUT SWING vs FREQUENCY



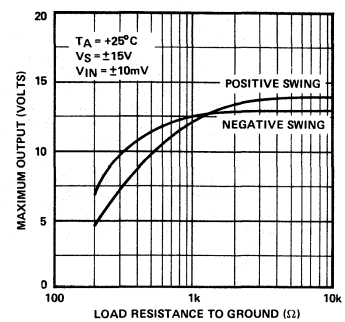
POWER CONSUMPTION vs POWER SUPPLY



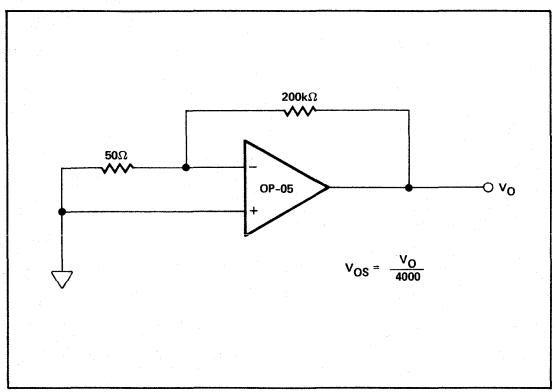
INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



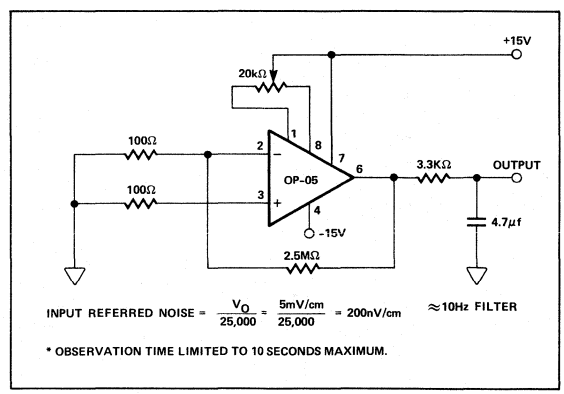
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



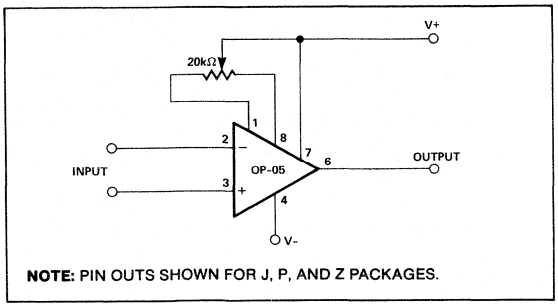
TYPICAL OFFSET VOLTAGE TEST CIRCUIT



TYPICAL LOW-FREQUENCY NOISE TEST CIRCUIT*

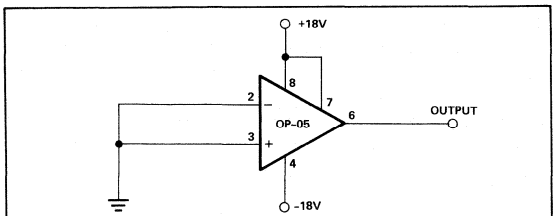


OFFSET NULLING CIRCUIT



NOTE: PIN OUTS SHOWN FOR J, P, AND Z PACKAGES.

BURN-IN CIRCUIT



NOTE: PIN OUTS SHOWN FOR J, P, AND Z PACKAGES.

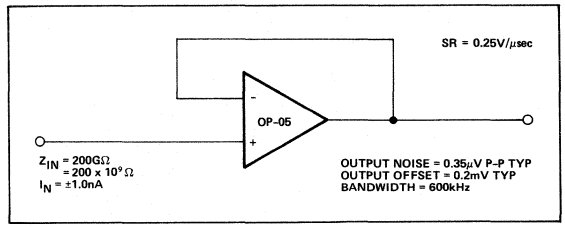
APPLICATIONS INFORMATION

OP-05 series devices may be fitted directly to 725 and 108/108A Series sockets with or without removal of external compensation components. Additionally, the OP-05 may be fitted to unnulled 741 series sockets. However, if conventional 741 nulling circuitry is in use, it should be modified or removed to enable proper OP-05 operation. The OP-05 provides stable operation with load capacitance of up to 500pF and ±10V swings; larger capacitances should be decoupled with a 50Ω resistor.

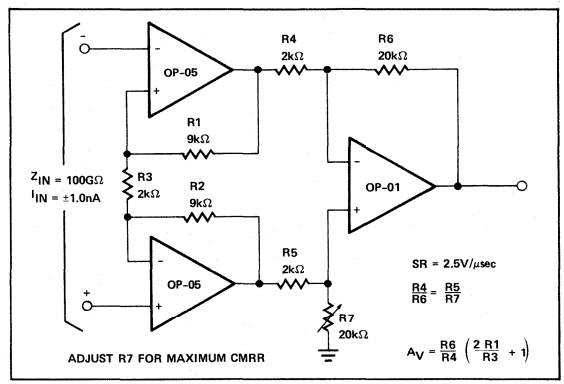
Offset stability can be degraded by stray thermoelectric voltages arising from dissimilar metals at the contacts to the input terminals. Best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the temperature of the device's package.

TYPICAL APPLICATIONS

STABLE, HIGH-IMPEDANCE BUFFER



HIGH IMPEDANCE, HIGH COMMON-MODE REJECTION INSTRUMENTATION AMPLIFIER



ANALOG DEVICES

High-Gain Instrumentation Operational Amplifier

OP-06

2

FEATURES

- **Very High Voltage Gain ..... 1,000V/mV Min**
- **Low Offset Voltage and Offset Current**
- **Low Drift vs. Temperature**
  (TCV_{OS}) ..... 0.8μV/°C Max
- **Low Input Voltage and Current Noise**
- **Low Offset Voltage Drift with Time**
- **High Common-Mode Rejection ..... 120dB Typ**
- **High Power Supply Rejection ..... 2μV/V Max**
- **Wide Supply Range ..... ±3.0V to ±22V**
- **MIL-STD-883 Processing Available**
- **Slew Rate to 100V/μs**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = 25°C V_{OS} MAX (mV)	PACKAGE TO-99 8-PIN	PACKAGE CERDIP 8-PIN	OPERATING TEMPERATURE RANGE
0.2	OP06AJ*	—	MIL
0.5	OP06FJ	—	COM
0.5	OP06BJ	—	MIL
1.3	OP06GJ	OP06GZ	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages.

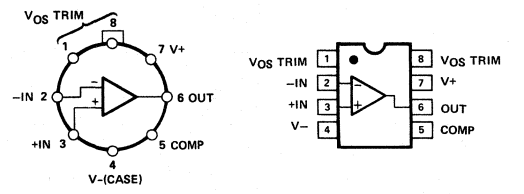
GENERAL DESCRIPTION

The OP-06 monolithic instrumentation operational amplifier is designed for accurate high-gain amplification of low level signals. High common-mode rejection reduces signal degradation when large common-mode voltages are present.

Superior DC input characteristics include very low offset voltage and current, extremely high open-loop gain, low 1/f and wideband noise, and low "popcorn" noise. Low offset voltage drift is improved by a nulling technique that optimizes TCV_{OS} performance when V_{OS} is nulled to zero. Very high common-mode and power supply rejection enable accurate performance in noisy environments.

Flexible external compensation provides wide-bandwidth and high slew rate operation in high closed-loop gain applications. Excellent long-term stability, and compatibility with MIL-STD-883 processing, make the OP-06 an excellent choice for high-reliability applications. For example, process control and aerospace applications; including strain gauge and thermocouple amplifiers, low-noise audio amplifiers, and instrumentation amplifiers. The OP-06 is a direct replacement for all 725 types providing superior DC and noise performance plus the unique feature of **complete input differential voltage and output short-circuit protection.**

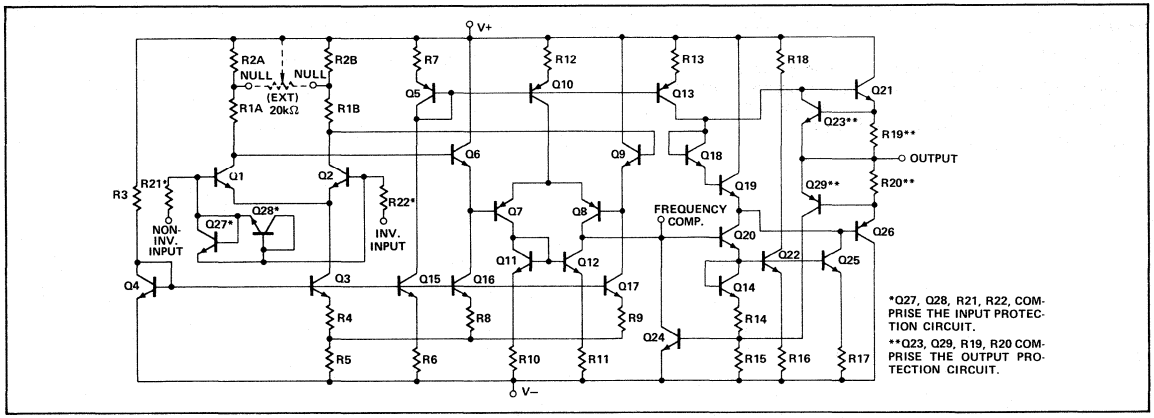
PIN CONNECTIONS



TO-99 (J-Suffix)

8-PIN HERMETIC DIP (Z-Suffix)

SIMPLIFIED SCHEMATIC



OP-06

ABSOLUTE MAXIMUM RATINGS (Note 3)

Supply Voltage ..... ±22V
Differential Input Voltage ..... ±30V
Input Voltage (Note 1) ..... ±22V
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range ..... –65°C to +150°C
Operating Temperature Range
OP-06A, OP-06B ..... –55°C to +125°C
OP-06F, OP-06G ..... 0°C to +70°C
Lead Temperature Range (Soldering, 60 sec) ..... +300°C
Junction Temperature ..... –65°C to +150°C

PACKAGE TYPE	Θ_{JA} (NOTE 2)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W

NOTES:
1. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO and CerDIP packages.
3. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-06A			OP-06B/F			OP-06G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$ (Note 2)	—	0.06	0.2	—	0.2	0.5	—	0.4	1.3	mV
Input Offset Current	I_{OS}		—	0.3	2.0	—	0.75	5.0	—	2	13	nA
Input Bias Current	I_B		—	30	70	—	30	80	—	40	110	nA
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 1)	—	9.0	15.0	—	9.0	15.0	—	9.0	15.0	$nV/\sqrt{Hz}$
		f_O = 100Hz (Note 1)	—	8.0	9.0	—	8.0	9.0	—	8.0	9.0	
		f_O = 1000Hz (Note 1)	—	7.0	7.5	—	7.0	7.5	—	7.0	7.5	
Input Noise Current Density	i_n	f_O = 10Hz (Note 1)	—	0.5	1.2	—	0.5	1.2	—	0.6	1.4	$pA/\sqrt{Hz}$
		f_O = 100Hz (Note 1)	—	0.25	0.6	—	0.25	0.6	—	0.3	0.7	
		f_O = 1000Hz (Note 1)	—	0.15	0.25	—	0.15	0.25	—	0.2	0.3	
Input Resistance	R_{IN}	(Note 3)	0.8	1.8	—	0.7	1.8	—	0.5	1.5	—	MΩ
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	1,000	3,000	—	1,000	3,000	—	500	3,000	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	±12.5	±13.0	—	±12.5	±13.0	—	±12.0	±13.0	—	V
		$R_L \geq 2k\Omega$	±12.0	±12.8	—	±12.0	±12.8	—	±11.5	±12.8	—	
		$R_L \geq 1k\Omega$	±11.0	±12.5	—	±11.0	±12.5	—	—	±12.0	—	
Input Voltage Range	IVR		±13.5	±14.0	—	±13.5	±14.0	—	±13.5	±14.0	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$, $R_S \leq 20k\Omega$	114	120	—	114	120	—	110	115	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$, $R_S \leq 20k\Omega$	—	0.5	2.0	—	1.0	5.0	—	2.0	10	μV/V
Power Consumption	P_d		—	90	120	—	90	120	—	110	150	mW
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 500\Omega$, (Note 3), $V_O = \pm 0.5V$, $V_S = \pm 3V$	100	600	—	100	600	—	60	600	—	V/mV
Power Consumption	P_d	$V_S = \pm 3V$	—	4	6	—	4	6	—	4	8	mW

NOTES:
1. Sample tested.
2. Thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can degrade drift performance. Both sides of the contacts should be kept at approximately the same temperature. All temperature gradients should be minimized.
3. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-06A MIN	OP-06A TYP	OP-06A MAX	OP-06B MIN	OP-06B TYP	OP-06B MAX	UNITS
Input Offset Voltage (Without external trim)	V_{OS}	$R_S \le 20k\Omega$ (Note 2)	—	0.08	0.28	—	0.3	0.7	mV
Average Input Offset Voltage Drift (Without external trim)	TCV_{OS}	$R_S = 50\Omega$ (Notes 1, 2)	—	0.3	0.8	—	0.7	2.0	µV/°C
Average Input Offset Voltage Drift (With external trim)	TCV_{OSn}	$R_S = 50\Omega$ (Notes 2, 3) $R_P = 20k\Omega$	—	0.2	0.6	—	0.28	1.0	µV/°C
Input Offset Current	I_{OS}	T_A MAX	—	0.25	1.0	—	0.6	4.0	nA
		T_A MIN	—	0.8	4.0	—	2.0	18.0	
Average Input Offset Current Drift	TCI_{OS}	(Note 1)	—	3	20	—	8	90	pA/°C
Input Bias Current	I_B	T_A MAX	—	22	60	—	25	70	nA
		T_A MIN	—	40	120	—	45	180	
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$ $R_S \le 20k\Omega$	109	112	—	109	112	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$ $R_S \le 20k\Omega$	—	1	5	—	2	8	µV/V
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$; $R_L \ge 2k\Omega$							V/mV
		T_A MAX	1,000	3,500	—	1,000	3,500	—	
		T_A MIN	700	2,000	—	700	1,800	—	
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12.0	±12.6	—	±12.0	±12.6	—	V

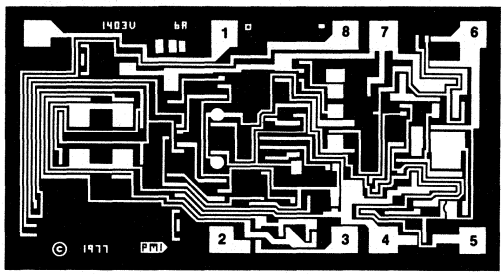
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0°C \le T_A \le 70°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-06F MIN	OP-06F TYP	OP-06F MAX	OP-06G MIN	OP-06G TYP	OP-06G MAX	UNITS
Input Offset Voltage (Without external trim)	V_{OS}	$R_S \le 20k\Omega$ (Note 2)	—	0.25	0.6	—	0.5	1.6	mV
Average Input Offset Voltage Drift (Without external trim)	TCV_{OS}	$R_S = 50\Omega$ (Notes 1, 2)	—	0.7	2.0	—	1.4	4.5	µV/°C
Average Input Offset Voltage Drift (With external trim)	TCV_{OSn}	$R_S = 50\Omega$ (Notes 2, 3) $R_P = 20k\Omega$	—	0.28	1.0	—	0.5	1.5	µV/°C
Input Offset Current	I_{OS}	T_A MAX	—	0.65	5.0	—	2.0	15	nA
		T_A MIN	—	2.0	18.0	—	3.0	25	
Average Input Offset Current Drift	TCI_{OS}	(Note 1)	—	8	90	—	14	150	pA/°C
Input Bias Current	I_B	T_A MAX	—	30	80	—	35	110	nA
		T_A MIN	—	45	180	—	45	180	
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$ $R_S \le 20k\Omega$	109	112	—	95	110	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$ $R_S \le 20k\Omega$	—	1.5	7.0	—	3.0	15	µV/V
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$; $R_L \ge 2k\Omega$							V/mV
		T_A MAX	1,000	3,500	—	400	3,200	—	
		T_A MIN	800	1,800	—	300	1,700	—	
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12.0	±12.6	—	±11.0	±12.6	—	V

NOTES:
1. Sample tested.
2. Thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can degrade drift performance. Both sides of the contacts should be kept at approximately the same temperature. All temperature gradients should be minimized.
3. Guaranteed by input bias current.

OP-06

DICE CHARACTERISTICS



1. NULL
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V−
5. COMPENSATION
6. OUTPUT
7. V+
8. NULL

DIE SIZE 0.095 × 0.051 inch, 4845 sq. mils
(2.41 × 1.30 mm, 3.13 sq. mm)

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$ for OP-06N, OP-06G and OP-06GR devices; $T_A = 125°C$ for OP-06NT and OP-06GT devices, unless otherwise noted. (Note 2)

PARAMETER	SYMBOL	CONDITIONS	OP-06NT LIMIT	OP-06N LIMIT	OP-06GT LIMIT	OP-06G LIMIT	OP-06GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	0.3	0.2	0.7	0.5	1.3	mV MAX
Input Offset Current	I_{OS}		1	2	4	5	13	nA MAX
Input Bias Current	I_B		60	70	70	80	110	nA MAX
Input Resistance Differential Mode	R_{IN}	(Note 1)	—	0.8	—	0.7	0.5	MΩ MIN
Input Voltage Range	IVR		±13.0	±13.5	±13.0	±13.5	±13.5	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5$ $R_S \leq 20k\Omega$	108	114	108	114	110	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$ $R_S \leq 20k\Omega$	6	2	8	5	10	μV/V MAX
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	— ±12.0 —	±12.5 ±12.0 ±11.0	— ±12.0 —	±12.5 ±12.0 ±11.0	±12.0 ±11.5 —	V MIN
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	1000	1000	800	1000	500	V/mV MIN
Differential Input Voltage			±30	±30	±30	±30	±30	V MAX
Power Consumption ($V_{OUT} = 0V$)	P_d		—	120	—	120	150	mW MAX

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

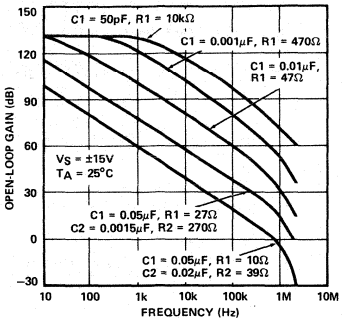
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-06NT TYPICAL	OP-06N TYPICAL	OP-06GT TYPICAL	OP-06G TYPICAL	OP-06GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	$R_S \leq 50\Omega$	0.3	0.3	0.7	0.7	1.4	μV/°C
Nulled Input Offset Voltage Drift	TCV_{OSn}	$R_S \leq 50k\Omega$ $R_P = 20k\Omega$	0.2	0.2	0.28	0.28	0.5	μV/°C
Average Input Offset Current Drift	TCI_{OS}		3	3	8	8	14	pA/°C

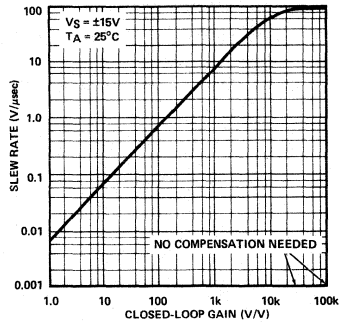
NOTES:
1. Guaranteed by input bias current.
2. For +25°C specifications of OP-06NT and OP-06GT, see OP-06N and OP-06G respectively.

TYPICAL PERFORMANCE CHARACTERISTICS

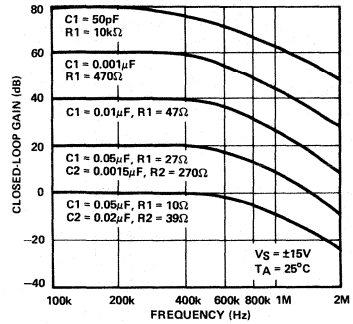
OPEN-LOOP RESPONSE FOR VALUES OF COMPENSATION



SLEW RATE USING RECOMMENDED COMPENSATION NETWORKS



CLOSED-LOOP FREQUENCY RESPONSE FOR VALUES OF COMPENSATION



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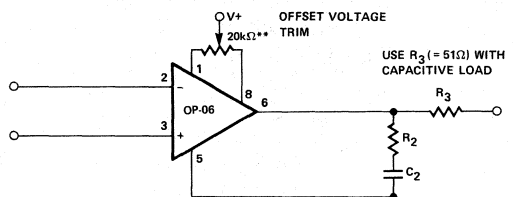
FREQUENCY COMPENSATION

COMPENSATION VALUES

Avcl	R_1 (Ω)	C_1 (μF)	R_2 (Ω)	C_2 (μF)
10000	10k	50pF	—	—
1000	470	0.001	—	—
100	47	0.01	—	—
10	27	0.05	270	0.0015
1	10	0.05	39	0.02

COMPENSATION CIRCUIT (J or Z PACKAGE)



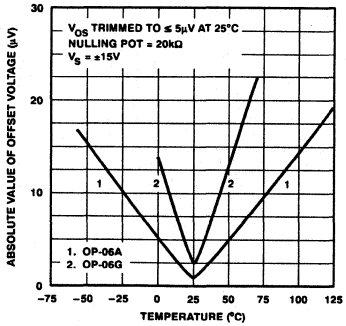
*THE COMPENSATION NETWORK (R_1, C_1) SHOULD BE RETURNED TO THE V–TERMINAL. IF THE NETWORK IS RETURNED TO GROUND, SERIOUS DEGRADATION OF POWER SUPPLY REJECTION PERFORMANCE WITH FREQUENCY WILL OCCUR. SEE TYPICAL CURVES (PSRR vs FREQUENCY).

**THE TRIMMING POTENTIOMETER SHOULD BE 20kΩ FOR OPTIMUM NULLED OFFSET VOLTAGE DRIFT. SEE TYPICAL CURVES (TRIMMED OFFSET VOLTAGE DRIFT AS A FUNCTION OF TRIMMING POTENTIOMETER).

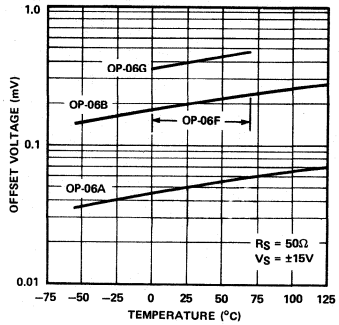
OP-06

TYPICAL PERFORMANCE CHARACTERISTICS

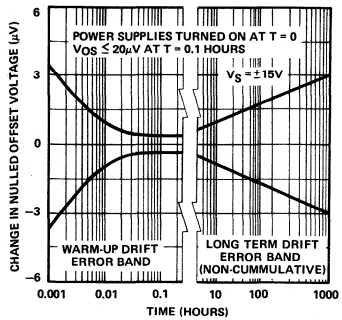
TRIMMED OFFSET VOLTAGE vs TEMPERAURE



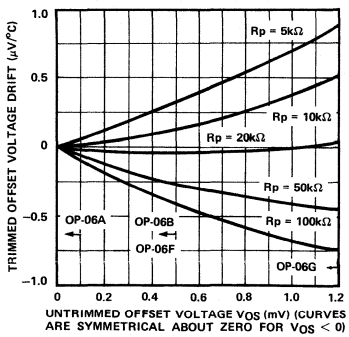
OFFSET VOLTAGE vs TEMPERATURE



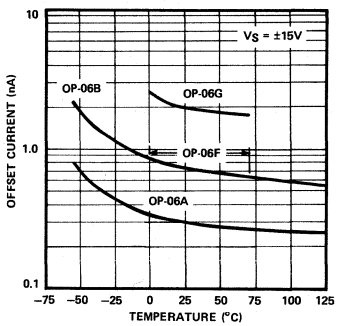
OFFSET VOLTAGE DRIFT WITH TIME



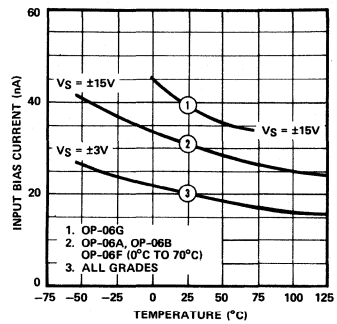
TRIMMED OFFSET VOLTAGE DRIFT AS A FUNCTION OF TRIMMING POTENTIOMETER (R_P) SIZE AND V_{OS}



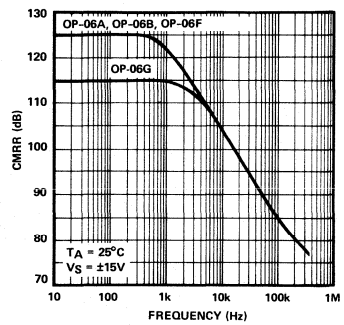
OFFSET CURRENT vs TEMPERATURE



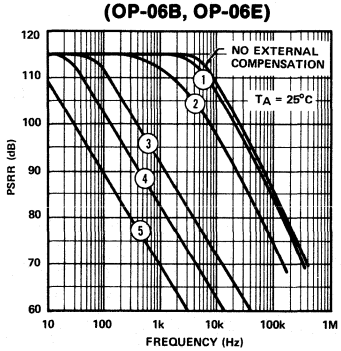
INPUT BIAS CURRENT vs TEMPERATURE



CMRR vs FREQUENCY

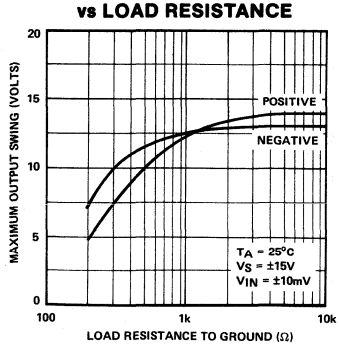


PSRR vs FREQUENCY (OP-06B, OP-06E)



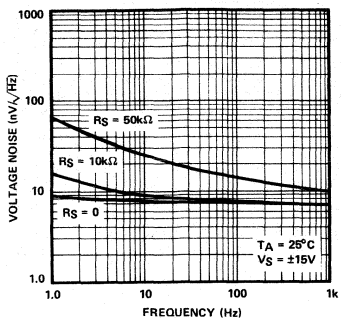
1. C1 = 0.001μF, R1 = 470Ω FROM PIN 5 TO V–
2. C1 = 0.1μF, R1 = 5Ω TO V–
3. C1 = 0.001μF; R1 = 470Ω FROM PIN 5 TO GND
4. C1 = 0.05μF, R1 = 10Ω, C2 = 0.02μF, R2 = 39Ω TO V–
5. C1 = 0.05μF, R1 = 10Ω, C2 = 0.02μF, R2 = 39Ω TO GND

MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE

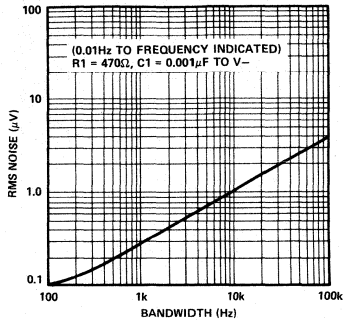


TYPICAL PERFORMANCE CHARACTERISTICS

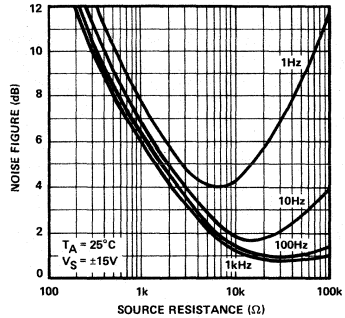
VOLTAGE NOISE DENSITY vs FREQUENCY



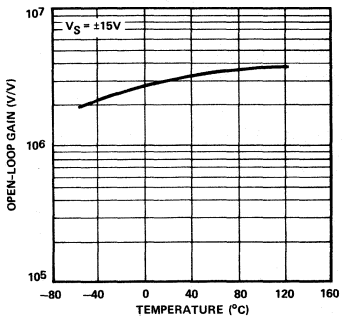
INPUT WIDEBAND NOISE vs BANDWIDTH



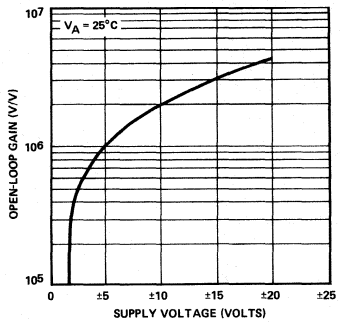
NOISE FIGURE vs SOURCE RESISTANCE



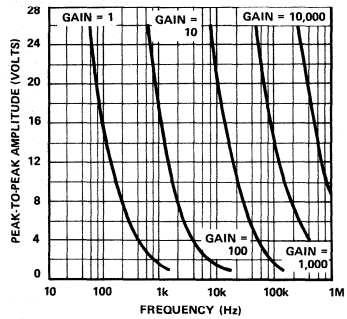
OPEN-LOOP GAIN vs TEMPERATURE



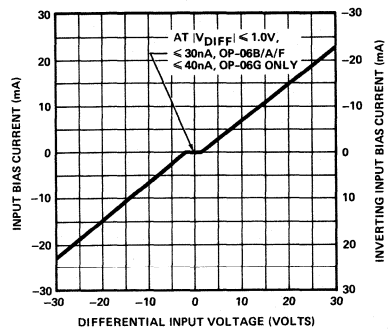
OPEN-LOOP GAIN vs SUPPLY VOLTAGE



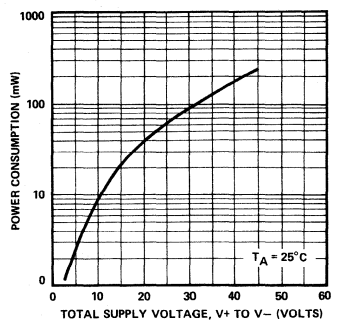
MAXIMUM OUTPUT SWING vs FREQUENCY



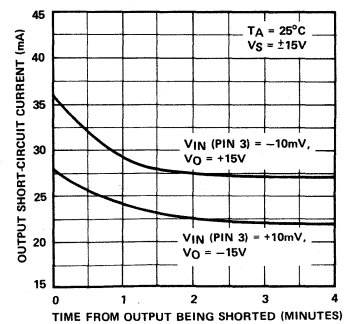
INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



POWER CONSUMPTION vs SUPPLY VOLTAGE

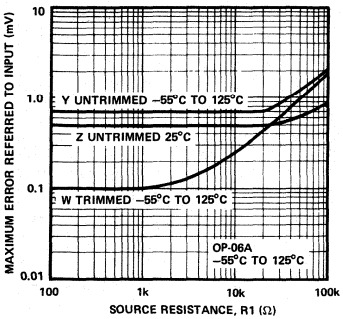


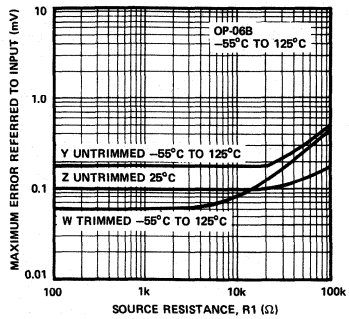
OUTPUT SHORT-CIRCUIT CURRENT

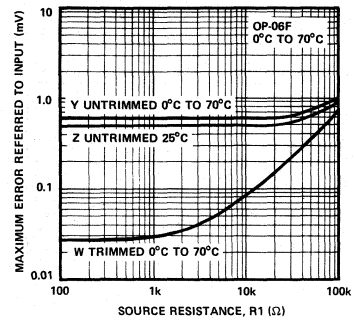


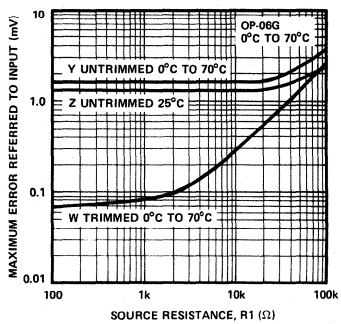
OP-06

GUARANTEED PERFORMANCE CHARACTERISTICS









These graphs depict maximum error referred to the input as a function of source resistance (R_1). Curves W are shown with V_{OS} trimmed at +25°C and include errors due to V_{OS} and I_{OS} over the indicated temperature range. Curves Y and Z plot maximum errors with V_{OS} not trimmed.

ANALOG DEVICES

Ultra-Low Offset Voltage Operational Amplifier

OP-07

FEATURES

- **Low V_{OS}** ..... **25μV Max**
- **Low V_{OS} Drift** ..... **0.6μV/°C Max**
- **Ultra-Stable vs Time** ..... **1.0μV/Month Max**
- **Low Noise** ..... **0.6μV_{p-p} Max**
- **Wide Input Voltage Range** ..... **±14V**
- **Wide Supply Voltage Range** ..... **±3V to ±18V**
- **Fits 725, 108A/308A, 741, AD510 Sockets**
- **125° C Temperature-Tested Dice**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (μV)	PACKAGE TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
25	OP07AJ*	OP07AZ*	—	—	MIL
75	OP07EJ	OP07EZ	OP07EP	—	COM
75	OP07J*	OP07Z*	—	OP07RC/883	MIL
150	OP07CJ	OP07CZ	OP07CP	—	XIND
150	—	—	OP07CS††	—	XIND
150	OP07DJ	—	OP07DP	—	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

The OP-07 has very low input offset voltage (25μV max for OP-07A) which is obtained by trimming at the wafer stage. These low offset voltages generally eliminate any need for external nulling. The OP-07 also features low input bias current (±2nA for OP-07A) and high open-loop gain (300V/mV for OP-07A). The low offsets and high open-loop gain make the OP-07 particularly useful for high-gain instrumentation applications.

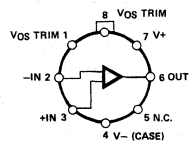
The wide input voltage range of ±13V minimum combined with high CMRR of 110dB (OP-07A) and high input impedace provides high accuracy in the noninverting circuit configuration. Excellent linearity and gain accuracy can be maintained even at high closed-loop gains.

Stability of offsets and gain with time or variations in temperture is excellent. The accuracy and stability of the OP-07, even at high gain, combined with the freedom from external nulling have made the OP-07 a new industry standard for instrumentation and military applications.

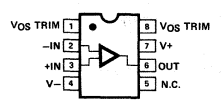
The OP-07 is available in five standard performance grades. The OP-07A and the OP-07 are specified for operation over the full military range of –55°C to +125°C; the OP-07E is specified for operation over the 0°C to +70°C range, and OP-07C and D over the –40°C to +85°C temperature range.

The OP-07 is available in hermetically-sealed TO-99 metal can or ceramic 8-pin Mini-DIP, and in epoxy 8-pin Mini-DIP. It is a direct replacement for 725, 108A, and OP-05 amplifiers; 741-types may be directly replaced by removing the 741's nulling potentiometer. The OP-207, a dual OP-07, is available for applications requiring close matching of two OP-07 amplifiers. For improved specifications, see the OP-77/OP-177.

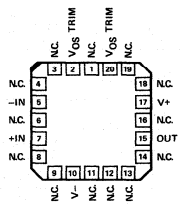
PIN CONNECTIONS



TO-99 (J-Suffix)

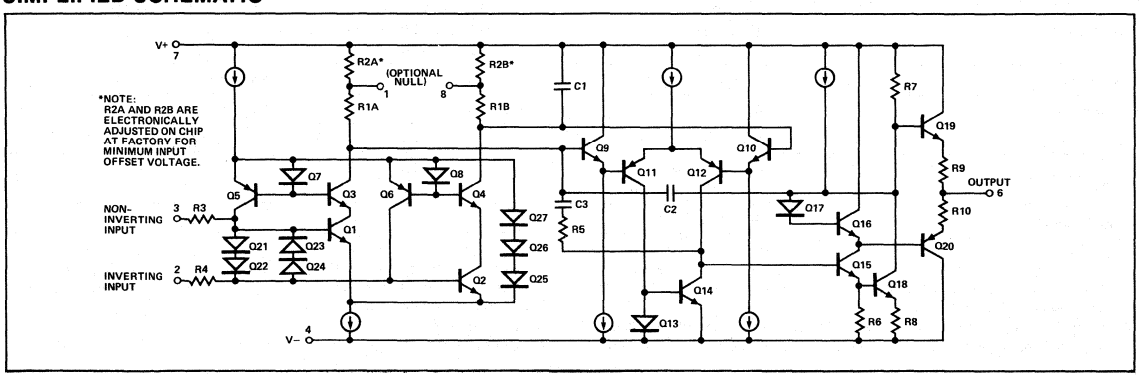


EPOXY MINI-DIP (P-Suffix)
8-PIN HERMETIC DIP (Z-Suffix)
8-PIN SO (S-Suffix)



OP-07RC/883 LCC (RC-Suffix)

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±22V
Differential Input Voltage ..... ±30V
Input Voltage (Note 2) ..... ±22V
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range
J, RC and Z Packages ..... –65°C to +150°C
P Package ..... –65°C to +125°C
Operating Temperature Range
OP-07A, OP-07, OP-07RC ..... –55°C to +125°C
OP-07E ..... 0°C to +70°C
OP-07C, OP-07D ..... –40°C to +85°C
Lead Temperature (Soldering, 60 sec) ..... +300°C
Junction Temperature (T_j) ..... +150°C

PACKAGE TYPE	Θ_{jA} (Note 3)	Θ_{jC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
3. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{jA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-07A			OP-07			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	10	25	—	30	75	μV
Long-Term Input Offset Voltage Stability	ΔV_{OS}/Time	(Note 2)	—	0.2	1.0	—	0.2	1.0	μV/Mo
Input Offset Current	I_{OS}		—	0.3	2.0	—	0.4	2.8	nA
Input Bias Current	I_B		—	±0.7	±2.0	—	±1.0	±3.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 3)	—	0.35	0.6	—	0.35	0.6	μV_{p-p}
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 3)	—	10.3	18.0	—	10.3	18.0	$nV/\sqrt{Hz}$
		f_O = 100Hz (Note 3)	—	10.0	13.0	—	10.0	13.0	
		f_O = 1000Hz (Note 3)	—	9.6	11.0	—	9.6	11.0	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 3)	—	14	30	—	14	30	pA_{p-p}
Input Noise Current Density	i_n	f_O = 10Hz (Note 3)	—	0.32	0.80	—	0.32	0.80	$pA/\sqrt{Hz}$
		f_O = 100Hz (Note 3)	—	0.14	0.23	—	0.14	0.23	
		f_O = 1000Hz (Note 3)	—	0.12	0.17	—	0.12	0.17	
Input Resistance — Differential-Mode	R_{IN}	(Note 4)	30	80	—	20	60	—	MΩ
Input Resistance — Common-Mode	R_{INCM}		—	200	—	—	200	—	GΩ
Input Voltage Range	IVR		±13	±14	—	±13	±14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	110	126	—	110	126	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	4	10	—	4	10	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	300	500	—	200	500	—	V/mV
		$R_L \geq 500\Omega$, $V_O = \pm 0.5V$, $V_S = \pm 3V$ (Note 4)	150	400	—	150	400	—	
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	±12.5	±13.0	—	±12.5	±13.0	—	V
		$R_L \geq 2k\Omega$	±12.0	±12.8	—	±12.0	±12.8	—	
		$R_L \geq 1k\Omega$	±10.5	±12.0	—	±10.5	±12.0	—	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 3)	0.1	0.3	—	0.1	0.3	—	V/μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$ (Note 3)	0.4	0.6	—	0.4	0.6	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	60	—	—	60	—	Ω
Power Consumption	P_d	$V_S = \pm 15V$, No Load	—	75	120	—	75	120	mW
		$V_S = \pm 3V$, No Load	—	4	6	—	4	6	
Offset Adjustment Range		R_P = 20kΩ	—	±4	—	—	±4	—	mV

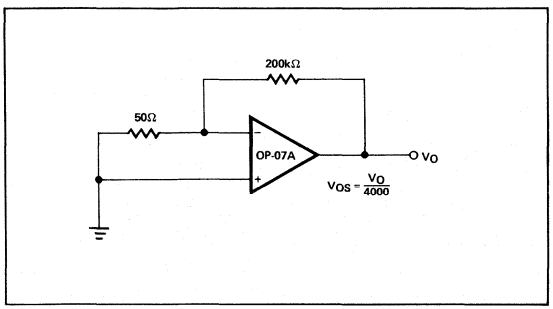
NOTES:
1. OP-07A grade V_{OS} is measured approximately one minute after application of power. For all other grades V_{OS} is measured approximately 0.5 seconds after application of power.
2. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV — refer to typical performance curves. Parameter is sample tested.
3. Sample tested.
4. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$, unless otherwise noted.

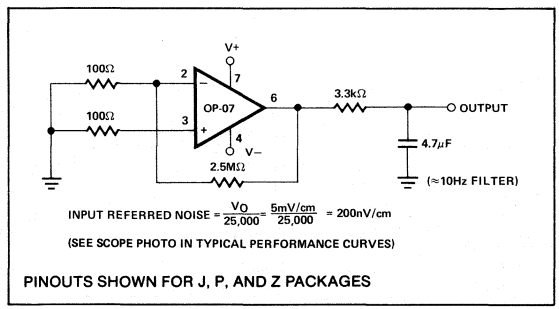
PARAMETER	SYMBOL	CONDITIONS	OP-07A MIN	OP-07A TYP	OP-07A MAX	OP-07 MIN	OP-07 TYP	OP-07 MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	25	60	—	60	200	μV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}	(Note 2)	—	0.2	0.6	—	0.3	1.3	μV/°C
With External Trim	TCV_{OSn}	$R_P = 20k\Omega$ (Note 3)	—	0.2	0.6	—	0.3	1.3	μV/°C
Input Offset Current	I_{OS}		—	0.8	4	—	1.2	5.6	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	5	25	—	8	50	pA/°C
Input Bias Current	I_B		—	±1	±4	—	±2	±6	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	8	25	—	13	50	pA/°C
Input Voltage Range	IVR		±13	±13.5	—	±13	±13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	106	123	—	106	123	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	5	20	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	200	400	—	150	400	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12	±12.6	—	±12	±12.6	—	V

NOTES:
1. OP-07A grade V_{OS} is measured approximately one minute after application of power. For all other grades V_{OS} is measured approximately 0.5 seconds after application of power.
2. Sample tested.
3. Guaranteed by design.

TYPICAL OFFSET VOLTAGE TEST CIRCUIT

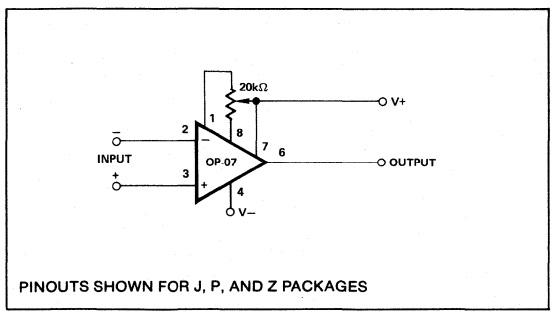


TYPICAL LOW-FREQUENCY NOISE TEST CIRCUIT



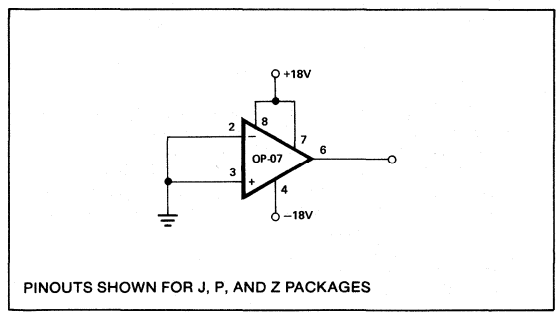
PINOUTS SHOWN FOR J, P, AND Z PACKAGES

OPTIONAL OFFSET NULLING CIRCUIT



PINOUTS SHOWN FOR J, P, AND Z PACKAGES

BURN-IN CIRCUIT



PINOUTS SHOWN FOR J, P, AND Z PACKAGES

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-07E MIN	OP-07E TYP	OP-07E MAX	OP-07C MIN	OP-07C TYP	OP-07C MAX	OP-07D MIN	OP-07D TYP	OP-07D MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	30	75	—	60	150	—	60	150	μV
Long-Term V_{OS} Stability	V_{OS}/Time	(Note 2)	—	0.3	1.5	—	0.4	2.0	—	0.5	3.0	μV/Mo
Input Offset Current	I_{OS}		—	0.5	3.8	—	0.8	6.0	—	0.8	6.0	nA
Input Bias Current	I_B		—	±1.2	±4.0	—	±1.8	±7.0	—	±2.0	±12	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 3)	—	0.35	0.6	—	0.38	0.65	—	0.38	0.65	μV_{p-p}
Input Noise Voltage Density	e_n	f_O = 10Hz	—	10.3	18.0	—	10.5	20.0	—	10.5	20.0	$nV/\sqrt{Hz}$
		f_O = 100Hz (Note 3)	—	10.0	13.0	—	10.2	13.5	—	10.3	13.5	
		f_O = 1000Hz	—	9.6	11.0	—	9.8	11.5	—	9.8	11.5	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 3)	—	14	30	—	15	35	—	15	35	pA_{p-p}
Input Noise Current Density	i_n	f_O = 10Hz	—	0.32	0.80	—	0.35	0.90	—	0.35	0.90	$pA/\sqrt{Hz}$
		f_O = 100Hz (Note 3)	—	0.14	0.23	—	0.15	0.27	—	0.15	0.27	
		f_O = 1000Hz	—	0.12	0.17	—	0.13	0.18	—	0.13	0.18	
Input Resistance — Differential-Mode	R_{IN}	(Note 4)	15	50	—	8	33	—	7	31	—	MΩ
Input Resistance — Common-Mode	R_{INCM}		—	160	—	—	120	—	—	120	—	GΩ
Input Voltage Range	IVR		±13	±14	—	±13	±14	—	±13	±14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	106	123	—	100	120	—	94	110	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to ±18V	—	5	20	—	7	32	—	7	32	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	200	500	—	120	400	—	120	400	—	V/mV
		$R_L \geq 500\Omega$ $V_O = \pm 0.5V$ $V_S = \pm 3V$ (Note 4)	150	400	—	100	400	—	—	400	—	
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	±12.5	±13.0	—	±12.0	±13.0	—	±12.0	±13.0	—	V
		$R_L \geq 2k\Omega$	±12.0	±12.8	—	±11.5	±12.8	—	±11.5	±12.8	—	
		$R_L \geq 1k\Omega$	±10.5	±12.0	—	—	±12.0	—	—	±12.0	—	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 3)	0.1	0.3	—	0.1	0.3	—	0.1	0.3	—	V/μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$ (Note 5)	0.4	0.6	—	0.4	0.6	—	0.4	0.6	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	60	—	—	60	—	—	60	—	Ω
Power Consumption	P_d	$V_S = \pm 15V$, No Load	—	75	120	—	80	150	—	80	150	mW
		$V_S = \pm 3V$, No Load	—	4	6	—	4	8	—	4	8	
Offset Adjustment Range		$R_P = 20k\Omega$	—	±4	—	—	±4	—	—	±4	—	mV

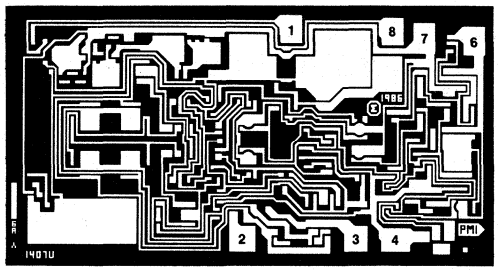
NOTES:
1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV — refer to typical performance curves. Parameter is sample tested.
3. Sample tested.
4. Guaranteed by design.
5. Guaranteed but not tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0°C \le T_A \le +70°C$ for OP-07E, and $-40°C \le T_A \le +85°C$ for OP-07C/D, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-07E MIN	OP-07E TYP	OP-07E MAX	OP-07C MIN	OP-07C TYP	OP-07C MAX	OP-07D MIN	OP-07D TYP	OP-07D MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	45	130	—	85	250	—	85	250	μV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}	(Note 3)	—	0.3	1.3	—	0.5	1.8	—	0.7	2.5	μV/°C
With External Trim	TCV_{OSn}	$R_P = 20k\Omega$ (Note 3)	—	0.3	1.3	—	0.4	1.6	—	0.7	2.5	μV/°C
Input Offset Current	I_{OS}		—	0.9	5.3	—	1.6	8.0	—	1.6	8.0	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	8	35	—	12	50	—	12	50	pA/°C
Input Bias Current	I_B		—	±1.5	±5.5	—	±2.2	±9.0	—	±3.0	±14	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	13	35	—	18	50	—	18	50	pA/°C
Input Voltage Range	IVR		±13.0	±13.5	—	±13.0	±13.5	—	±13.0	±13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	103	123	—	97	120	—	94	106	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	7	32	—	10	51	—	10	51	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$ $V_O = \pm 10V$	180	450	—	100	400	—	100	400	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12	±12.6	—	±11	±12.6	—	±11	±12.6	—	V

NOTES:
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. Sample tested.
3. Guaranteed by design.

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



DIE SIZE 0.100 × 0.055 inch, 5500 sq. mils
(2.54 × 1.40 mm, 3.56 sq. mm)

1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V–
6. OUTPUT
7. V+
8. BALANCE

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$ for OP-07N, OP-07G and OP-07GR devices; $T_A = 125°C$ for OP-07NT and OP-07GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-07NT LIMIT	OP-07N LIMIT	OP-07GT LIMIT	OP-07G LIMIT	OP-07GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		140	40	210	80	150	μV MAX
Input Offset Current	I_{OS}		4.0	2.0	5.6	2.8	6.0	nA MAX
Input Bias Current	I_B		±4	±2	±6	±3	±7	nA MAX
Input Resistance Differential-Mode	R_{IN}	(Note 2)	—	20	—	20	8	MΩ MIN
Input Voltage Range	IVR		±13	±13	±13	±13	±13	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	100	110	100	110	100	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	20	10	20	10	30	μV/V MAX
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$ $R_L = 1k\Omega$	— ±12.0 —	±12.5 ±12.0 ±10.5	— ±12.0 —	±12.0 ±11.5 ±10.5	±12.0 ±11.5 —	V MIN
Large-Signal Voltage Gain	A_{VO}	$R_L = 2k\Omega$ $V_O = \pm 10V$	200	200	150	120	120	V/mV MIN
Differential Input Voltage			±30	±30	±30	±30	±30	V MAX
Power Consumption	P_d	$V_{OUT} = 0V$	—	120	—	120	150	mW MAX

NOTES:
1. For 25°C characteristics of OP-07NT and OP-07GT, see OP-07N and OP-07G characteristics, respectively.
2. Guaranteed by design.

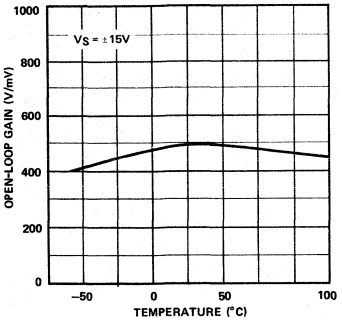
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

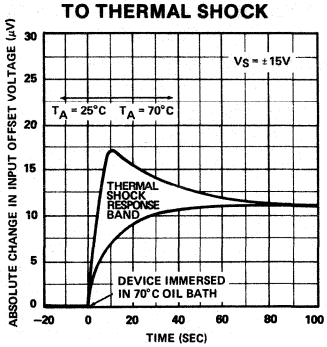
PARAMETER	SYMBOL	CONDITIONS	OP-07NT TYPICAL	OP-07N TYPICAL	OP-07GT TYPICAL	OP-07G TYPICAL	OP-07GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	0.2	0.2	0.3	0.3	0.7	μV/°C
Nulled Input Offset Voltage Drift	TCV_{OSn}	$R_S = 50\Omega$, $R_P = 20k\Omega$	0.2	0.2	0.3	0.3	0.7	μV/°C
Average Input Offset Current Drift	TCI_{OS}		5	5	8	8	12	pA/°C
Slew Rate	SR	$R_L \geq 2k\Omega$	0.3	0.3	0.3	0.3	0.3	V/μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$	0.6	0.6	0.6	0.6	0.6	MHz

TYPICAL PERFORMANCE CHARACTERISTICS

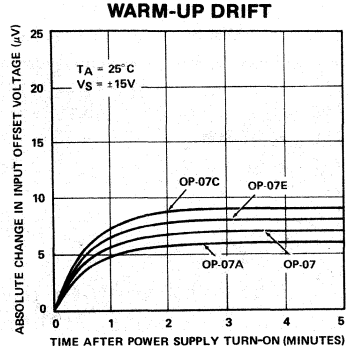
OPEN-LOOP GAIN vs TEMPERATURE



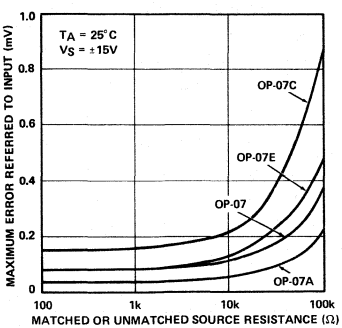
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



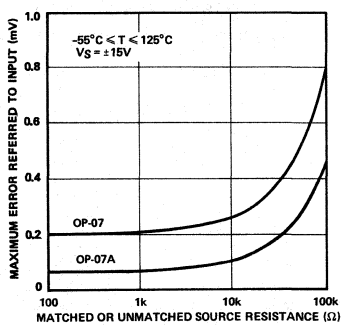
WARM-UP DRIFT



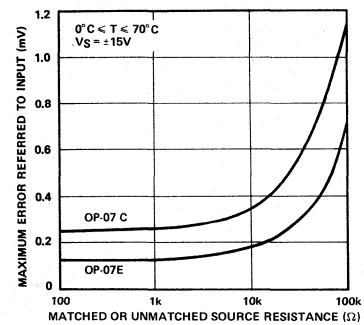
MAXIMUM ERROR vs SOURCE RESISTANCE



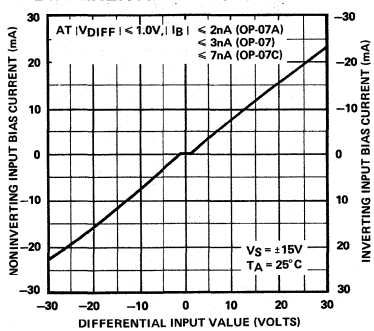
MAXIMUM ERROR vs SOURCE RESISTANCE



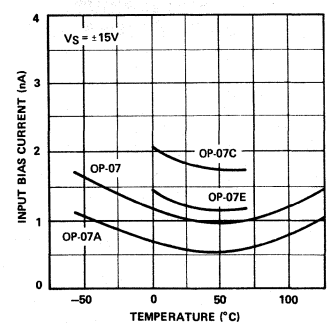
MAXIMUM ERROR vs SOURCE RESISTANCE



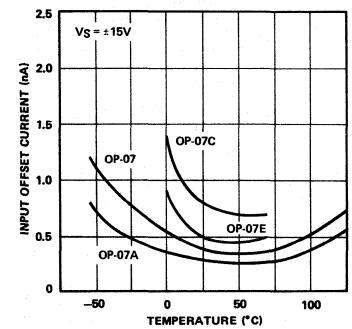
INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



INPUT BIAS CURRENT vs TEMPERATURE

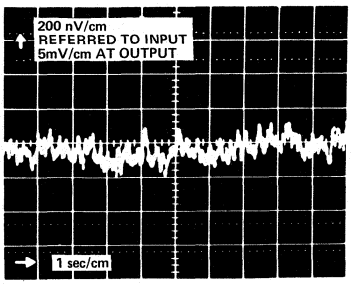


INPUT OFFSET CURRENT vs TEMPERATURE

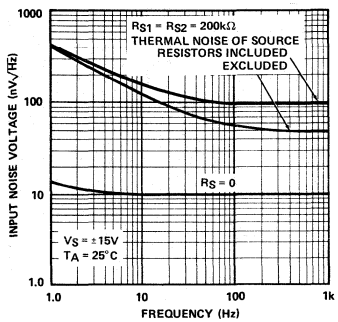


TYPICAL PERFORMANCE CHARACTERISTICS

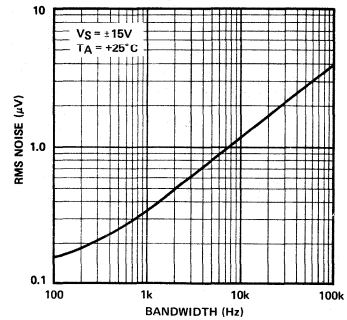
OP-07 LOW FREQUENCY NOISE



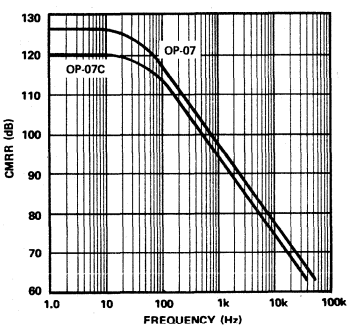
TOTAL INPUT NOISE VOLTAGE vs FREQUENCY



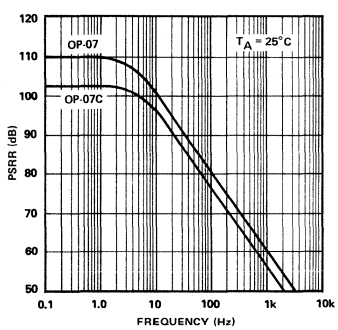
INPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



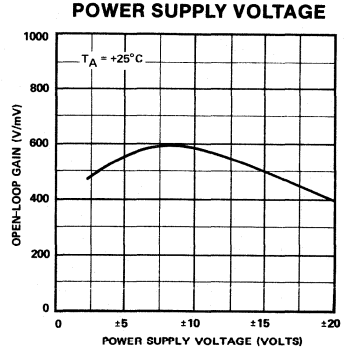
CMRR vs FREQUENCY



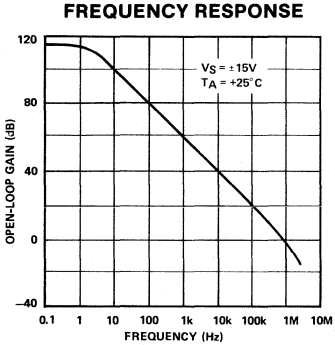
PSRR vs FREQUENCY



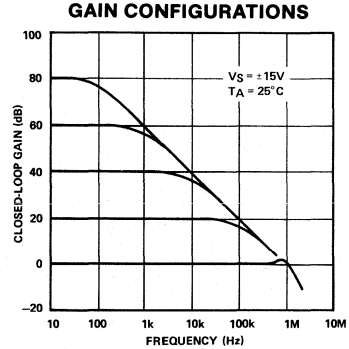
OPEN-LOOP GAIN vs POWER SUPPLY VOLTAGE



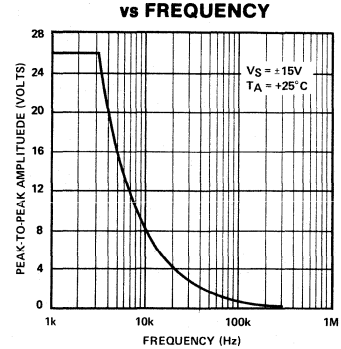
OPEN-LOOP FREQUENCY RESPONSE



CLOSED-LOOP RESPONSE FOR VARIOUS GAIN CONFIGURATIONS

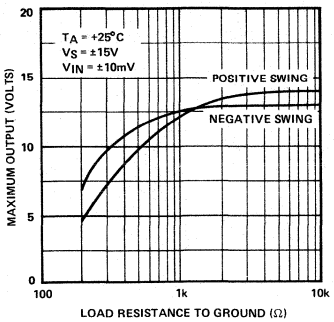


MAXIMUM OUTPUT SWING vs FREQUENCY

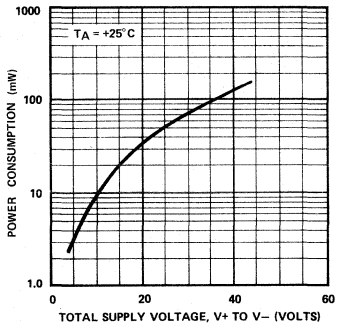


TYPICAL PERFORMANCE CHARACTERISTICS

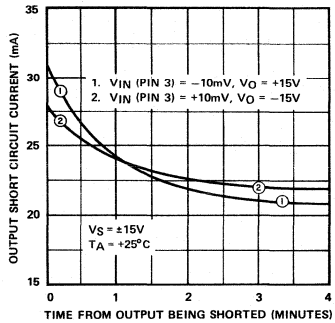
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



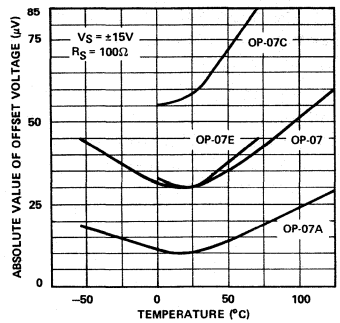
POWER CONSUMPTION vs POWER SUPPLY



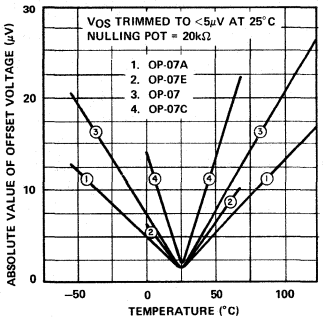
OUTPUT SHORT-CIRCUIT CURRENT vs TIME



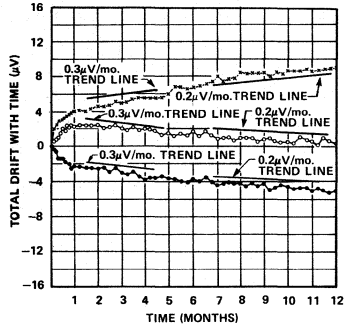
UNTRIMMED OFFSET VOLTAGE vs TEMPERATURE



TRIMMED OFFSET VOLTAGE vs TEMPERATURE

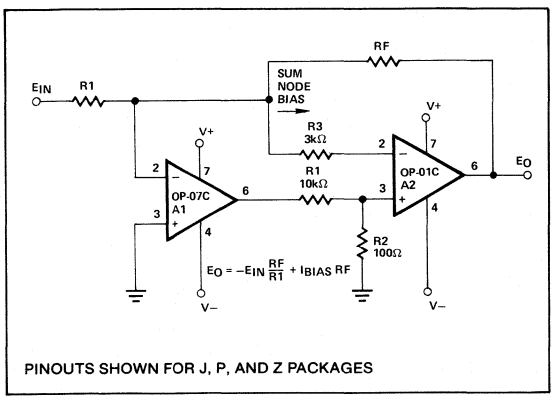


OFFSET VOLTAGE STABILITY vs TIME



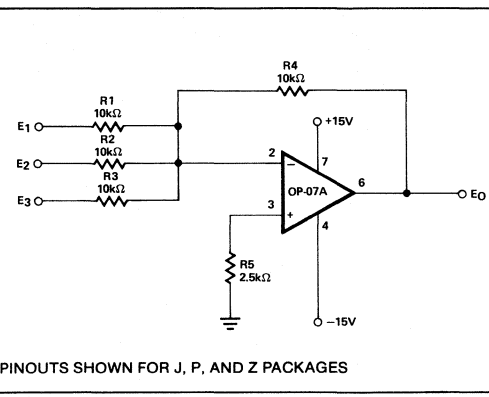
TYPICAL APPLICATIONS

HIGH SPEED, LOW V_{OS}, COMPOSITE AMPLIFIER



PINOUTS SHOWN FOR J, P, AND Z PACKAGES

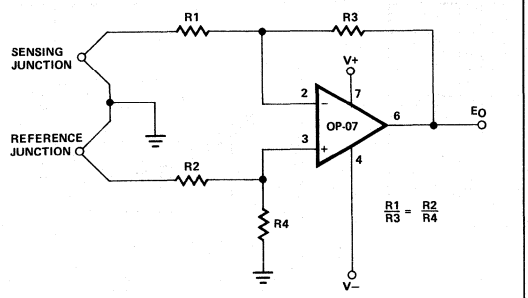
ADJUSTMENT-FREE PRECISION SUMMING AMPLIFIER



PINOUTS SHOWN FOR J, P, AND Z PACKAGES

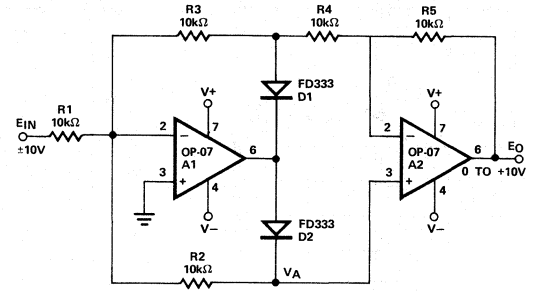
TYPICAL APPLICATIONS

HIGH-STABILITY THERMOCOUPLE AMPLIFIER



PINOUTS SHOWN FOR J, P, AND Z PACKAGES

PRECISION ABSOLUTE-VALUE CIRCUIT



PINOUTS SHOWN FOR J, P, AND Z PACKAGES

APPLICATIONS INFORMATION

OP-07 series units may be substituted directly into 725, 108A/308A* and OP-05 sockets with or without removal of external compensation or nulling components. Additionally, the OP-07 may be used in unnulled 741-type sockets. However, if conventional 741 nulling circuitry is in use, it should be modified or removed to enable proper OP-07 operation. OP-07 offset voltage may be nulled to zero through use of a potentiometer (see offset nulling circuit diagram).

The OP-07 provides stable operation with load capacitance of up to 500pF and ±10V swings; larger capacitances should be decoupled with a 50Ω decoupling resistor.

Stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can degrade drift performance. Therefore, best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the package temperature.

*TO-99 Package only

ANALOG DEVICES

Quad Matched 741-Type Operational Amplifiers

OP-09/OP-11

FEATURES

- **Guaranteed V_{OS} ..... 500μV Max**
- **Guaranteed Matched CMRR ..... 94dB Min**
- **Guaranteed Matched V_{OS} ..... 750μV Max**
- **RC/RM4136 Direct Replacement (OP-09)**
- **LM148/LM348 Direct Replacement (OP-11)**
- **Low Noise**
- **Silicon-Nitride Passivation**
- **Internal Frequency Compensation**
- **Low Crossover Distortion**
- **Continuous Short-Circuit Protection**
- **Low Input Bias Current**
- **Available in Die Form**

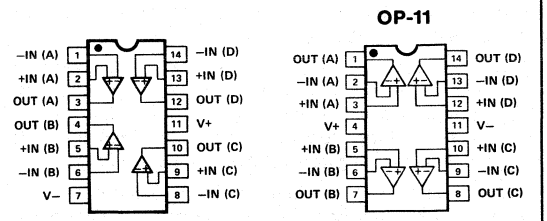
ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (mV)	PACKAGE CERDIP 14-PIN	PACKAGE PLASTIC	PACKAGE LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
0.5	OP09AY*	–	–	MIL
	OP11AY*	–	OP11ARC/883	
0.5	OP09EY	–	–	COM
	OP11EY	OP11EP	–	
2.5	OP11BY*	–	–	MIL
2.5	–	OP09FP	–	XIND
	OP11FY	OP11FP	–	
5.0	OP11CY/883	–	–	MIL
5.0	–	OP11GP	–	XIND
	–	OP11GS	–	

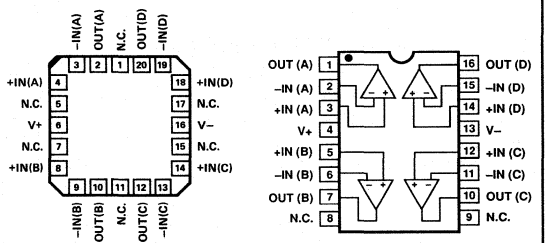
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

PIN CONNECTIONS



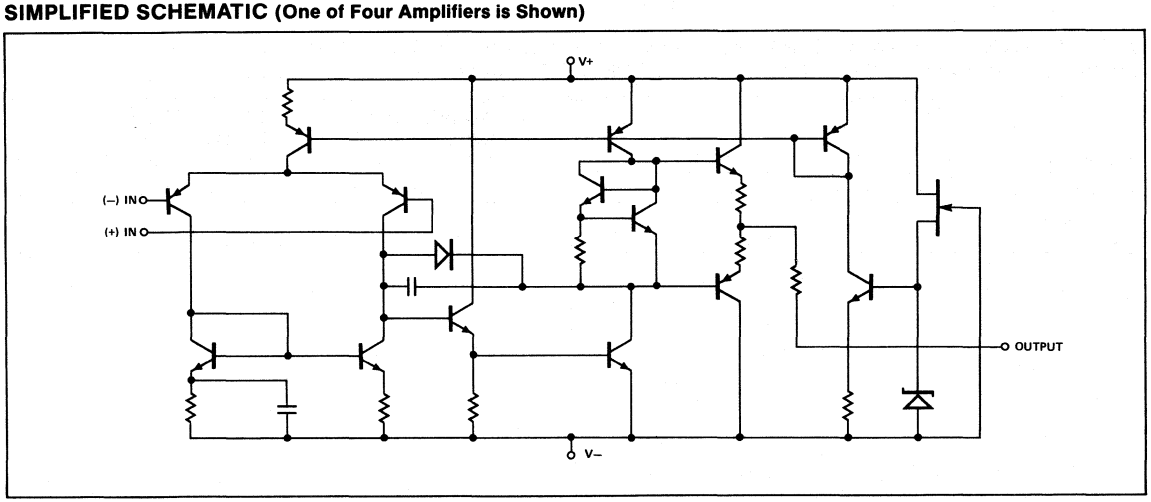
14-PIN HERMETIC DIP (Y-Suffix)
EPOXY DIP (P-Suffix)



OP-11ARC/883
LCC
(RC-Suffix)

16-PIN SOL
(S-Suffix)
OP-11

SIMPLIFIED SCHEMATIC (One of Four Amplifiers is Shown)



OP-09/OP-11

GENERAL DESCRIPTION

The OP-09 and OP-11 provide four matched 741-type operational amplifiers in a single 14-pin DIP package. The OP-11 is pin compatible with the LM148, LM348, RM4156, and HA4741 amplifiers. The OP-09 is pin compatible with the RM4136 and RC4136. The amplifiers are matched for common-mode rejection ratio and offset voltage which is very important in designing instrumentation amplifiers. In addition, the amplifier is designed to have equal positive-going and negative-going slew rates. This is an important consideration for good audio system performance.

Each of the four amplifiers has the proven OP-02 advantages of low noise, low drift, and excellent long-term stability. Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process reduces "popcorn noise", provides high reliability, and assures long-term stability of parameters.

The OP-09 and OP-11 are ideal for use in designs requiring minimum space and cost while maintaining OP-02-type performance.

OP-09's and OP-11's with processing per the requirements of MIL-STD-883 are available. For dual-741-type versions, see the OP-04/14 data sheet.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±22V
OP-09GR and OP-11GR (Only) ..... ±18V
Differential Input Voltage ..... ±30V
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous
(One Amplifier Only)

Storage Temperature Range
RC, Y-Package ..... –65°C to +150°C
P-Package ..... –65°C to +125°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature (T_j) ..... –65°C to +150°C
Operating Temperature Range
OP-09A, OP-09B ..... –55°C to +125°C
OP-09E ..... 0°C to +70°C
OP-09F ..... –40°C to +85°C
OP-11A, OP-11B,
OP-11C, OP-11ARC ..... –55°C to +125°C
OP-11E ..... 0°C to +70°C
OP-11F, OP-11G ..... –40°C to +85°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
14-Pin Hermetic DIP (Y)	108	16	°C/W
14-Pin Plastic DIP (P)	83	39	°C/W
20-Contact LCC (RC)	98	33	°C/W
16-Pin SOL (S)	98	30	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{jA} is specified for device soldered to printed circuit board for SOL package.

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, $R_S \leq 100\Omega$, unless otherwise noted.

			OP-09A, OP-09E OP-11A, OP-11E			OP-09B, OP-09F OP-11B, OP-11F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}		—	0.5	0.75	—	0.8	2.0	mV
Common-Mode Rejection	$\Delta CMRR$	$V_{CM} = \pm 12V$	—	1	20	—	1	20	µV/V
Ratio Match		$V_{CM} = \pm 12V$	94	120	—	94	120	—	dB

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$ for OP-09A, OP-09B, OP-11A, OP-11B, $0°C \leq T_A \leq +70°C$ for OP-09E, OP-11E and $-40°C \leq T_A \leq +85°C$ for OP-09F, OP-11F, $R_S \leq 100\Omega$, unless otherwise noted.

			OP-09A, OP-09E OP-11A, OP-11E			OP-09B, OP-09F OP-11B, OP-11F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}		—	0.6	1.0	—	1.0	2.5	mV
Common-Mode Rejection	$\Delta CMRR$	$V_{CM} = \pm 12V$	—	3.2	20	—	3.2	20	µV/V
Ratio Match		$V_{CM} = \pm 12V$	94	110	—	94	110	—	dB

ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15V$ $T_A = 25°C$, unless otherwise noted.

			OP-09A/E OP-11A/E			OP-09B/F OP-11B/F			OP-11C/G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	—	0.3	0.5	—	0.6	2.5	—	1.2	5.0	mV
Input Offset Current	I_{OS}		—	5.5	20	—	25	50	—	75	200	nA
Input Bias Current	I_B		—	180	300	—	300	500	—	300	500	nA
Input Resistance Differential Mode	R_{IN}	(Note 3)	0.17	0.29	—	0.1	0.17	—	0.1	0.17	—	MΩ
Input Voltage Range	IVR		±12	±13	—	±12	±13	—	±12	±13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 12V$, $R_S \leq 10k\Omega$	100	120	—	100	120	—	70	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 15V$, $R_S \leq 10k\Omega$	—	4	32	—	4	32	—	10	100	μV/V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±11	±13	—	±11	±13	—	±11	±13	—	V
Large-Signal Voltage Gain	A_{VO}	$R_L \leq 2k\Omega$, $V_O = \pm 10V$	100	650	—	100	650	—	50	500	—	V/mV
Power Consumption (Note 1)	P_d	$V_O = 0V$	—	105	180	—	123	180	—	210	340	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.7	—	—	0.7	—	—	0.7	—	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$	—	18	—	—	18	—	—	18	—	$nV/\sqrt{Hz}$
		$f_O = 100Hz$	—	14	—	—	14	—	—	14	—	
		$f_O = 1000Hz$	—	12	—	—	12	—	—	12	—	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	—	17	—	—	17	—	—	17	—	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10Hz$	—	1.8	—	—	1.8	—	—	1.8	—	$pA/\sqrt{Hz}$
		$f_O = 100Hz$	—	1.5	—	—	1.5	—	—	1.5	—	
		$f_O = 1000Hz$	—	1.2	—	—	1.2	—	—	1.2	—	
Channel Separation	CS		100	130	—	100	130	—	—	130	—	dB
Slew Rate (Note 2)	SR		0.7	1.0	—	0.7	1.0	—	0.7	1.0	—	V/μs
Large-Signal Bandwidth (Note 2)		$V_O = 20V_{p-p}$	11	16	—	11	16	—	11	16	—	kHz
Closed-Loop Bandwidth (Note 4)	BW	$A_{VCL} = +1.0$	2.4	3.0	—	2.4	3.0	—	2.4	3.0	—	MHz
Risetime (Note 2)	t_r	$A_V = +1$, $V_{IN} = 50mV$	—	110	145	—	110	145	—	110	145	ns
Overshoot (Note 2)	OS		—	15	25	—	15	25	—	15	25	%

NOTES:
1. Total dissipation for all four amplifiers in package.
2. Sample tested.
3. Guaranteed by input bias current.
4. Guaranteed by risetime.

ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-09A OP-11A MIN	OP-09A OP-11A TYP	OP-09A OP-11A MAX	OP-09B OP-11B MIN	OP-09B OP-11B TYP	OP-09B OP-11B MAX	OP-11C MIN	OP-11C TYP	OP-11C MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	—	0.4	1.0	—	1.0	3.5	—	1.5	6.0	mV
Average Input Offset Voltage Drift (Note 3)	TCV_{OS}	$R_S \leq 10k\Omega$	—	2.0	10	—	4.0	15	—	4.0	—	µV/°C
Input Offset Current	I_{OS}		—	20	40	—	40	80	—	250	300	nA
Average Input Offset Current Drift (Note 3)	TCI_{OS}		—	0.1	0.3	—	0.3	0.6	—	0.3	0.6	nA/°C
Input Bias Current	I_B		—	200	375	—	400	650	—	400	800	nA
Input Voltage Range	IVR		±12	±13	—	±12	±13	—	±12	±13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 12V$, $R_S \leq 10k\Omega$	100	120	—	100	120	—	70	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 15V$, $R_S \leq 10k\Omega$	—	4	32	—	4	32	—	10	100	µV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	50	250	—	50	250	—	25	100	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±11	±13	—	±11	±13	—	±11	±13	—	V
Power Consumption (Note 1)	P_d	$V_O = 0V$	—	115	200	—	115	200	—	250	400	mW

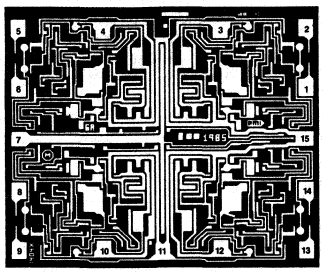
ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15V$, $0°C \leq T_A \leq +70°C$ for OP-09E, OP-11E, $-40°C \leq T_A \leq +85°C$ for OP-09F, OP11F, OP-11G, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-09E OP-11E MIN	OP-09E OP-11E TYP	OP-09E OP-11E MAX	OP-09F OP-11F MIN	OP-09F OP-11F TYP	OP-09F OP-11F MAX	OP-11G MIN	OP-11G TYP	OP-11G MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	—	0.4	0.8	—	0.8	3.0	—	1.5	6.0	mV
Average Input Offset Voltage Drift	TCV_{OS}	$R_S \leq 10k\Omega$	—	2.0	10	—	4.0	15	—	4.0	—	µV/°C
Input Offset Current	I_{OS}		—	14	30	—	40	60	—	250	300	nA
Average Input Offset Current Drift (Note 3)	TCI_{OS}		—	0.1	0.3	—	0.3	0.6	—	0.3	0.6	nA/°C
Input Bias Current	I_B		—	200	350	—	400	550	—	400	800	nA
Input Voltage Range	IVR		±12	±13	—	±12	±13	—	±12	±13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 12V$, $R_S \leq 10k\Omega$	100	120	—	100	120	—	70	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 15V$, $R_S \leq 10k\Omega$	—	4	32	—	4	32	—	10	100	µV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	50	250	—	50	250	—	25	100	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±11	±13	—	±11	±13	—	±11	±13	—	V
Power Consumption (Note 1)	P_d	$V_O = 0V$	—	115	200	—	115	200	—	250	400	mW

NOTES:
1. Total dissipation for all four amplifiers in package.
2. Sample tested.
3. Guaranteed but not tested.

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)

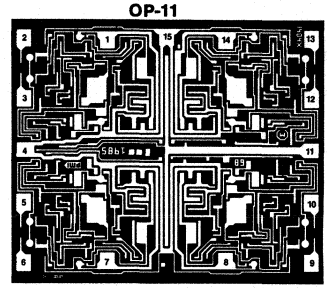
OP-09



1. INVERTING INPUT (A)
2. NONINVERTING INPUT (A)
3. OUTPUT (A)
4. OUTPUT (B)
5. NONINVERTING INPUT (B)
6. INVERTING INPUT (B)
7. V−
8. INVERTING INPUT (C)
9. NONINVERTING INPUT (C)
10. OUTPUT (C)
11. V+
12. OUTPUT (D)
13. NONINVERTING INPUT (D)
14. INVERTING INPUT (D)
15. V+

DIE SIZE 0.086 × 0.072 inch, 6192 sq. mils
(2.18 × 1.83 mm, 3.99 sq. mm)

OP-11



1. OUTPUT (A)
2. INVERTING INPUT (A)
3. NONINVERTING INPUT (A)
4. V+
5. NONINVERTING INPUT (B)
6. INVERTING INPUT (B)
7. OUTPUT (B)
8. OUTPUT (C)
9. INVERTING INPUT (C)
10. NONINVERTING INPUT (C)
11. V−
12. NONINVERTING INPUT (D)
13. INVERTING INPUT (D)
14. OUTPUT (D)
15. V+

DIE SIZE 0.086 × 0.072 inch, 6192 sq. mils
(2.18 × 1.83 mm, 3.99 sq. mm)

NOTE:
Either or both V+ pads may be used without any change in performance.

2

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$ for OP-09/11N, OP-09/11G and OP-09/11GR devices; $T_A = 125°C$ for OP-09/11NT and OP-09/11GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-09NT OP-11NT LIMIT	OP-09N OP-11N LIMIT	OP-09GT OP-11GT LIMIT	OP-11G LIMIT	OP-09GR OP-11GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	1.0	0.5	3.5	2.5	5.0	mV MAX
Input Offset Current	I_{OS}		20	20	50	50	200	nA MAX
Input Bias Current	I_B		300	300	500	500	500	nA MAX
Input Voltage Range	IVR		±12	±12	±12	±12	±12	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 12V$ $R_S \leq 10k\Omega$	100	100	100	100	70	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$ $R_S \leq 10k\Omega$	32	32	32	32	100	µV/V MAX
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L = 2k\Omega$	±11 ±11	±12 ±11	±11 ±11	±12 ±11	±11 ±11	V MIN
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	50	100	50	100	50	V/mV MIN
Power Consumption (Four Amplifiers)	P_d	$V_{OUT} = 0$ No Load	200	180	200	180	340	mW MAX

NOTES:
For 25°C characteristics of NT & GT devices, see N & G characteristics, respectively.

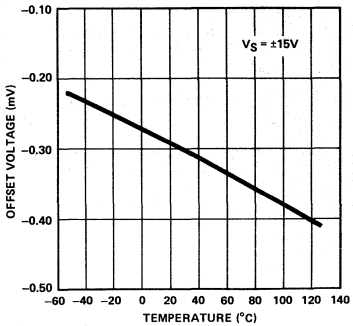
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

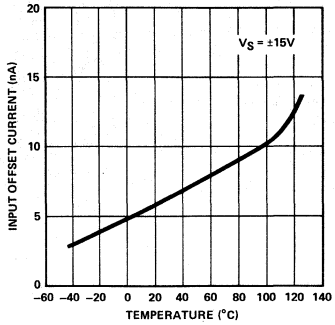
PARAMETER	SYMBOL	CONDITIONS	OP-09NT OP-11NT TYPICAL	OP-09N OP-11N TYPICAL	OP-09GT OP-11GT TYPICAL	OP-11G TYPICAL	OP-09GR OP-11GR TYPICAL	UNITS
Slew Rate	SR	$A_V = 1$ $R_L \geq 2k\Omega$	1	1	1	1	1	V/µs
Unity Gain Bandwidth	GBW		2	2	2	2	2	MHz
Channel Separation	CS	$A_V = 100$ $f = 10kHz$ $R_S = 1k\Omega$	130	130	130	130	130	dB

TYPICAL PERFORMANCE CHARACTERISTICS

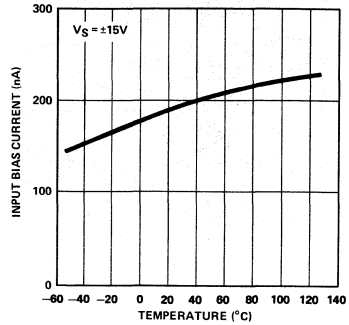
INPUT OFFSET VOLTAGE vs TEMPERATURE



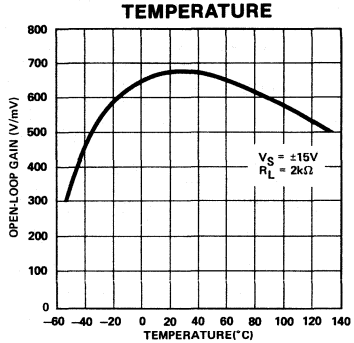
OFFSET CURRENT vs TEMPERATURE



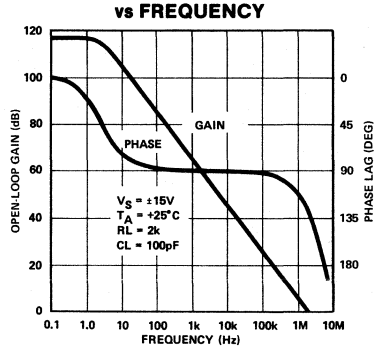
BIAS CURRENT vs TEMPERATURE



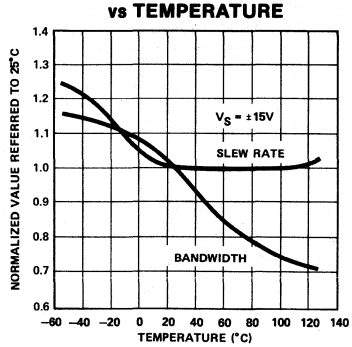
OPEN-LOOP GAIN vs TEMPERATURE



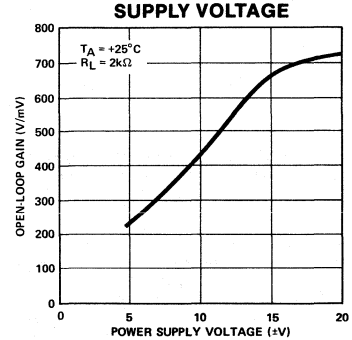
OPEN-LOOP GAIN AND PHASE vs FREQUENCY



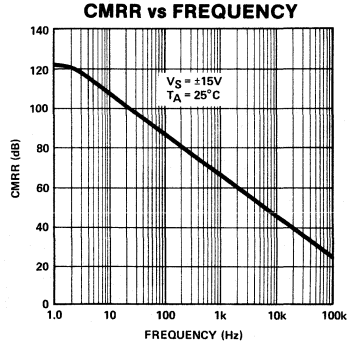
NORMALIZED SLEW RATE AND BANDWIDTH vs TEMPERATURE



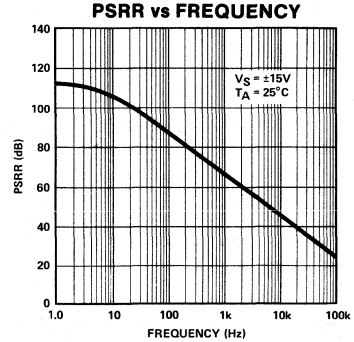
OPEN-LOOP GAIN vs SUPPLY VOLTAGE



CMRR vs FREQUENCY

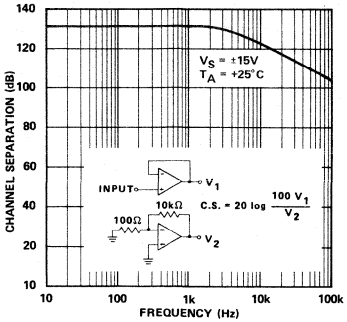


PSRR vs FREQUENCY

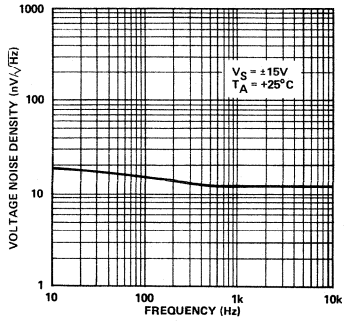


TYPICAL PERFORMANCE CHARACTERISTICS

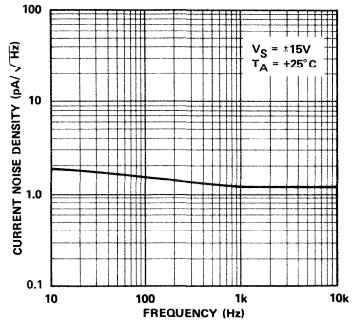
CHANNEL SEPARATION vs FREQUENCY



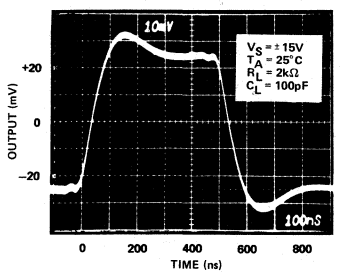
NOISE VOLTAGE DENSITY vs FREQUENCY



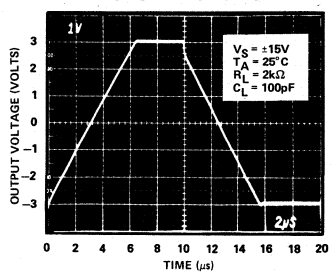
NOISE CURRENT DENSITY vs FREQUENCY



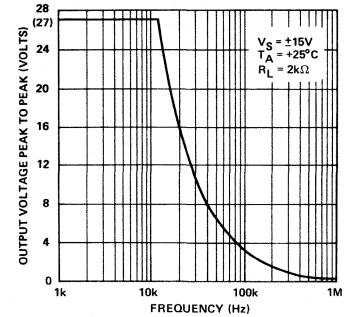
TRANSIENT RESPONSE



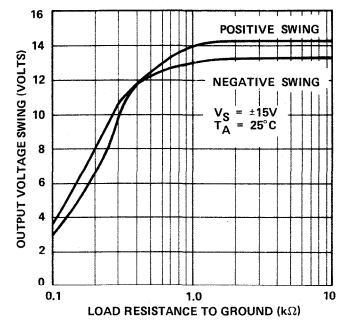
VOLTAGE FOLLOWER PULSE RESPONSE



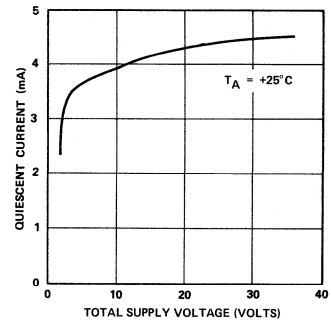
MAXIMUM OUTPUT SWING vs FREQUENCY



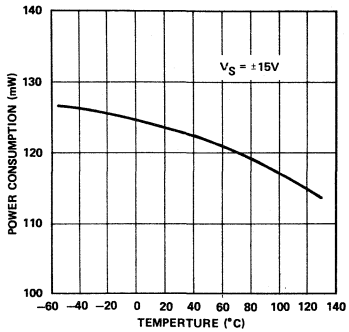
OUTPUT VOLTAGE vs LOAD RESISTANCE



QUIESCENT CURRENT vs SUPPLY VOLTAGE



POWER CONSUMPTION vs TEMPERATURE



ANALOG DEVICES

Dual Matched Instrumentation Operational Amplifier

OP-10

FEATURES

- **Extremely Tight Matching**
- **Excellent Individual Amplifier Parameters**
- **Offset Voltage Match ..... 0.18mV Max**
- **Offset Voltage Match vs Temp. ..... 0.8μV/°C Max**
- **Common-Mode Rejection Match ..... 114dB Min**
- **Power Supply Rejection Match ..... 100dB Min**
- **Bias Current Match ..... 3.0nA Max**
- **Low Noise ..... 0.6μV_{p-p} Max**
- **Low Bias Current ..... 3.0nA Max**
- **High Common-Mode Input Impedance .... 200GΩ Typ**
- **Excellent Channel Separation ..... 126dB Min**

ORDERING INFORMATION†

T_A = 25°C V_{OS} MAX (mV)	HERMETIC DIP 14-PIN	OPERATING TEMPERATURE RANGE
0.5	OP10AY*	MIL
0.5	OP10EY	COM
0.5	OP10Y*	MIL
0.5	OP10CY	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

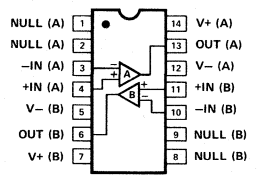
GENERAL DESCRIPTION

The OP-10 series of dual-matched instrumentation operational amplifiers consists of two independent monolithic high-performance operational amplifiers in a single 14-pin dual-in-line package. Tight matching of critical parameters is provided between channels of the dual operational amplifier.

The excellent specifications of the individual amplifiers and tight matching over temperature enable construction of high-performance instrumentation amplifiers. The designer can achieve the guaranteed specifications because the common package eliminates temperature differentials which occur in designs using separately housed amplifiers.

Matching between channels is provided on all critical parameters including offset voltage, tracking of offset voltage vs. temperature, noninverting bias currents, and common-mode and power-supply rejection ratios. The individual amplifiers feature extremely low offset voltage, offset voltage drift, low noise voltage, low bias current, internal compensation and input/output protection.

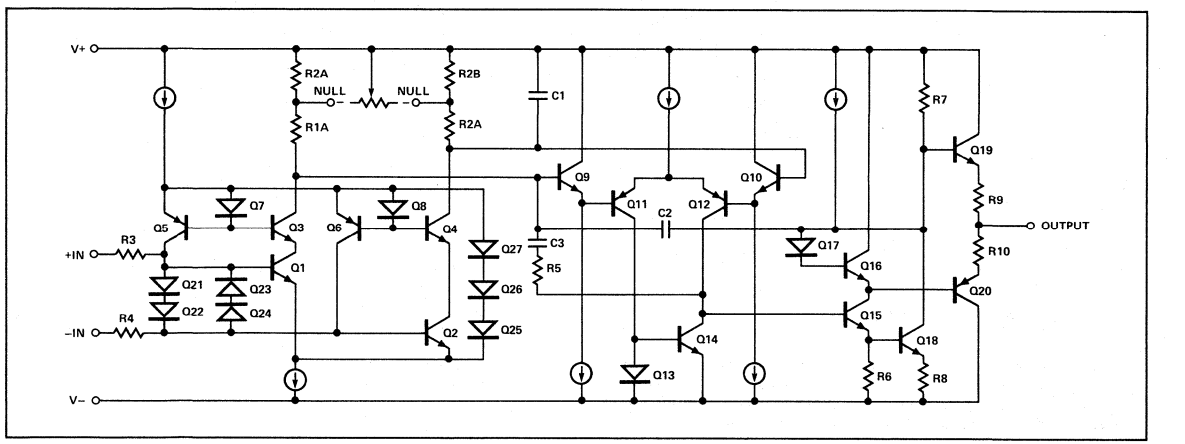
PIN CONNECTIONS



14-PIN CERAMIC DIP (Y-Suffix)

NOTE:
Device may be operated even if insertion is reversed; this is due to inherent symmetry of pin locations of amplifiers A and B.

SIMPLIFIED SCHEMATIC (1/2 OP-10)



OP-10

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Differential Input Voltage ..... ±30V
Input Voltage (Note 1) ..... ±22V
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range ..... –65°C to +150°C
Operating Temperature Range
OP-10A, OP-10 ..... –55°C to +125°C
OP-10E, OP-10C ..... 0°C to +70°C

DICE Junction Temperature (T_j) ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (NOTE 2)	Θ_{JC}	UNITS
14-Pin Hermetic DIP (Y)	108	16	°C/W

NOTES:
1. For supply voltages less than +22V, the absolute maximum input voltage is equal to the supply voltage.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP package.

INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-10A			OP-10			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.2	0.5	—	0.2	0.5	mV
Long-Term Input Offset Voltage Stability	ΔV_{OS}/Time	(Notes 1, 2)	—	0.25	1.0	—	0.25	1.0	µV/Mo
Input Offset Current	I_{OS}		—	1.0	2.8	—	1.0	2.8	nA
Input Bias Current	I_B		—	±1	±3	—	±1	±3	nA
Input Noise Voltage	e_{np-p}	(Note 2) 0.1Hz to 10Hz	—	0.35	0.6	—	0.35	0.6	μV_{p-p}
Input Noise Voltage Density	e_n	f_O = 10Hz	—	10.3	18.0	—	10.3	18.0	$nV/\sqrt{Hz}$
		(Note 2) f_O = 100Hz	—	10.0	13.0	—	10.0	13.0	
		f_O = 1000Hz	—	9.6	11.0	—	9.6	11.0	
Input Noise Current	i_{np-p}	(Note 2) 0.1Hz to 10Hz	—	14	30	—	14	30	pA_{p-p}
Input Noise Current Density	i_n	f_O = 10Hz	—	0.32	0.80	—	0.32	0.80	$pA/\sqrt{Hz}$
		(Note 2) f_O = 100Hz	—	0.14	0.23	—	0.14	0.23	
		f_O = 1000Hz	—	0.12	0.17	—	0.12	0.17	
Input Resistance — Differential-Mode	R_{IN}	(Note 3)	20	60	—	20	60	—	MΩ
Input Resistance — Common-Mode	R_{INCM}		—	200	—	—	200	—	GΩ
Input Voltage Range	IVR		±13	±14	—	±13	±14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	110	126	—	110	126	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to ±18V	—	4	10	—	4	10	µV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	200	500	—	200	500	—	V/mV
		$R_L \geq 500\Omega$, $V_O = \pm 0.5V$, $V_S = \pm 3V$ (Note 3)	150	500	—	150	500	—	
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	±12.5	±13.0	—	±12.5	±13.0	—	V
		$R_L \geq 2k\Omega$	±12.0	±12.8	—	±12.0	±12.8	—	
		$R_L \geq 1k\Omega$	±10.5	±12.0	—	±10.5	±12.0	—	
Slew Rate	SR	$R_L \geq 2k\Omega$	—	0.17	—	—	0.17	—	V/µs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1.0$	—	0.6	—	—	0.6	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	60	—	—	60	—	Ω
Power Consumption	P_d	Each Amplifier	—	90	120	—	90	120	mW
		$V_S = \pm 3V$	—	4	6	—	4	6	
Offset Adjustment Range		$R_P = 20k\Omega$	—	±4	—	—	±4	—	mV
Input Capacitance	C_{IN}		—	8	—	—	8	—	pF

NOTES:
1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5µV — refer to typical performance curves.
2. Sample tested.
3. Guaranteed by design.

INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-10A MIN	OP-10A TYP	OP-10A MAX	OP-10 MIN	OP-10 TYP	OP-10 MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.3	0.7	—	0.3	0.7	mV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}	(Note 2)	—	0.7	2.0	—	0.7	2.0	µV/°C
With External Trim	TCV_{OSn}	$R_P = 20k\Omega$ (Note 3)	—	0.3	1.0	—	0.3	1.0	µV/°C
Input Offset Current	I_{OS}		—	1.8	5.6	—	1.8	5.6	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	8	50	—	8	50	pA/°C
Input Bias Current	I_B		—	±2	±6	—	±2	±6	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	13	50	—	13	50	pA/°C
Input Voltage Range	IVR		±13.0	±13.5	—	±13.0	±13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	106	123	—	106	123	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	5	20	µV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	150	400	—	150	400	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12.0	±12.6	—	±12.0	±12.6	—	V

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-10A MIN	OP-10A TYP	OP-10A MAX	OP-10 MIN	OP-10 TYP	OP-10 MAX	UNITS
Input Offset Voltage	ΔV_{OS}		—	0.07	0.18	—	0.12	0.5	mV
Average Noninverting Bias Current	I_B^+		—	±1.0	±3.0	—	±1.3	±4.5	nA
Noninverting Offset Current	I_{OS}^+		—	0.8	2.8	—	1.1	4.5	nA
Inverting Offset Current	I_{OS}^-		—	0.8	2.8	—	1.1	4.5	nA
Common-Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm 13V$	114	123	—	106	120	—	dB
Power Supply Rejection Ratio Match	ΔPSRR	$V_S = \pm 3V$ to $\pm 18V$	—	3	10	—	4	20	µV/V
Channel Separation	CS	(Note 2)	126	140	—	126	140	—	dB

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-10A MIN	OP-10A TYP	OP-10A MAX	OP-10 MIN	OP-10 TYP	OP-10 MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}		—	0.1	0.3	—	0.2	0.9	mV
Input Offset Voltage Tracking Without External Trim	$TC\Delta V_{OS}$	(Note 2)	—	0.45	1.3	—	0.9	2.5	µV/°C
With External Trim	$TC\Delta V_{OSn}$	$R_P = 20k\Omega$ (Note 3) Channel A only	—	0.3	0.8	—	0.4	1.2	µV/°C

NOTES:
1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5µV — refer to typical performance curves.
2. Sample tested.
3. Guaranteed by design.

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-10A MIN	OP-10A TYP	OP-10A MAX	OP-10 MIN	OP-10 TYP	OP-10 MAX	UNITS
Average Noninverting Bias Current	I_B+		—	±2.0	±6.0	—	±2.4	±8.0	nA
Average Drift of Noninverting Bias Current	TCI_B+	(Note 2)	—	10	40	—	15	—	pA/°C
Noninverting Offset Current	$I_{OS}+$		—	2.0	6.5	—	2.4	9.0	nA
Average Drift of Noninverting Offset Current	$TCI_{OS}+$	(Note 2)	—	12	50	—	18	—	pA/°C
Inverting Offset Current	$I_{OS}-$		—	2.0	6.5	—	2.4	9.0	nA
Common-Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm 13V$	108	120	—	103	117	—	dB
Power Supply Rejection Ratio Match	ΔPSRR	$V_S = \pm 3V$ to $\pm 18V$	—	6	20	—	7	32	μV/V

INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-10E MIN	OP-10E TYP	OP-10E MAX	OP-10C MIN	OP-10C TYP	OP-10C MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.2	0.5	—	0.2	0.5	mV
Long-Term Input Offset Voltage Stability	ΔV_{OS}/Time	(Notes 1, 2)	—	0.3	1.5	—	0.5	—	μV/Mo
Input Offset Current	I_{OS}		—	1.2	3.8	—	1.8	6.0	nA
Input Bias Current	I_B		—	±1.2	±4.0	—	±1.8	±7.0	nA
Input Noise Voltage	e_{np-p}	(Note 2) 0.1Hz to 10Hz	—	0.35	0.6	—	0.38	0.65	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$	—	10.3	18.0	—	10.5	20.0	$nV/\sqrt{Hz}$
		(Note 2) $f_O = 100Hz$	—	10.0	13.0	—	10.2	13.5	
		$f_O = 1000Hz$	—	9.6	11.0	—	9.8	11.5	
Input Noise Current	i_{np-p}	(Note 2) 0.1Hz to 10Hz	—	14	30	—	15	35	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10Hz$	—	0.32	0.80	—	0.35	0.90	$pA/\sqrt{Hz}$
		(Note 2) $f_O = 100Hz$	—	0.14	0.23	—	0.15	0.27	
		$f_O = 1000Hz$	—	0.12	0.17	—	0.13	0.18	
Input Resistance — Differential-Mode	R_{IN}	(Note 3)	15	50	—	8	33	—	MΩ
Input Resistance — Common-Mode	R_{INCM}		—	160	—	—	120	—	GΩ
Input Voltage Range	IVR		±13	±14	—	±13	±14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	106	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	4	20	—	10	32	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	200	500	—	120	400	—	V/mV
		$R_L \geq 500\Omega$, $V_O = \pm 0.5V$, $V_S = \pm 3V$ (Note 3)	150	500	—	100	400	—	
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	±12.5	±13.0	—	±12.0	±13.0	—	V
		$R_L \geq 2k\Omega$	±12.0	±12.8	—	±11.5	±12.8	—	
		$R_L \geq 1k\Omega$	±10.5	±12.0	—	—	±12.0	—	

NOTES:

1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV — refer to typical performance curves.
2. Sample tested.
3. Guaranteed by design.

INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm 15V$, $0°C \leq T_A \leq +70°C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-10E MIN	OP-10E TYP	OP-10E MAX	OP-10C MIN	OP-10C TYP	OP-10C MAX	UNITS
Slewing Rate	SR	$R_L \geq 2k\Omega$	—	0.17	—	—	0.17	—	V/μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1.0$	—	0.6	—	—	0.6	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	60	—	—	60	—	Ω
Power Consumption	P_d	Each Amplifier	—	90	120	—	95	150	mW
		$V_S = \pm 3V$	—	4	6	—	4	8	
Offset Adjustment Range		$R_P = 20k\Omega$	—	±4	—	—	±4	—	mV
Input Capacitance	C_{IN}		—	8	—	—	8	—	pF

INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm 15V$, $0°C \leq T_A \leq +70°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		OP-10E MIN	OP-10E TYP	OP-10E MAX	OP-10C MIN	OP-10C TYP	OP-10C MAX	UNITS
Input Offset Voltage	V_{OS}			—	0.25	0.6	—	0.35	1.6	mV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}		(Note 2)	—	0.7	2.0	—	1.2	4.5	μV/°C
With External Trim	TCV_{OSn}	$R_P = 20k\Omega$	(Note 3)	—	0.3	1.0	—	0.4	1.5	μV/°C
Input Offset Current	I_{OS}			—	1.4	5.3	—	2.0	8.0	nA
Average Input Offset Current Drift	TCI_{OS}		(Note 2)	—	8	50	—	12	50	pA/°C
Input Bias Current	I_B			—	±1.5	±5.5	—	±2.2	±9.0	nA
Average Input Bias Current Drift	TCI_B		(Note 2)	—	13	50	—	18	50	pA/°C
Input Voltage Range	IVR			±13.0	±13.5	—	±13.0	±13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$		103	123	—	97	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$		—	7	32	—	10	51	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$		100	400	—	100	400	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$		±12.0	±12.6	—	±11.0	±12.6	—	V

NOTES:
1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV — refer to typical performance curves.
2. Sample tested.
3. Guaranteed by design.

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

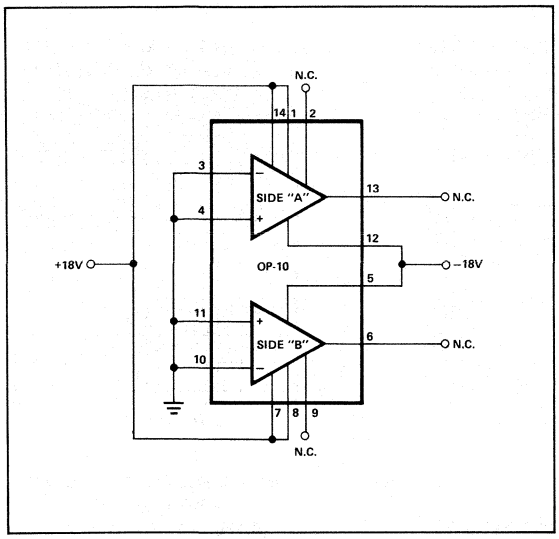
PARAMETER	SYMBOL	CONDITIONS	OP-10E MIN	OP-10E TYP	OP-10E MAX	OP-10C MIN	OP-10C TYP	OP-10C MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}		—	0.12	0.5	—	0.3	—	mV
Average Noninverting Bias Current	I_B+		—	±1.3	±4.5	—	±2.0	—	nA
Noninverting Offset Current	$I_{OS}+$		—	1.1	4.5	—	1.8	—	nA
Inverting Offset Current	$I_{OS}-$		—	1.1	4.5	—	1.8	—	nA
Common-Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm 13V$	106	120	—	—	117	—	dB
Power Supply Rejection Ratio Match	ΔPSRR	$V_S = \pm 3V$ to $\pm 18V$	—	4	20	—	5	—	μV/V
Channel Separation	CS	(Note 1)	126	140	—	120	137	—	dB

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $0°C \leq T_A \leq +70°C$, unless otherwise noted.

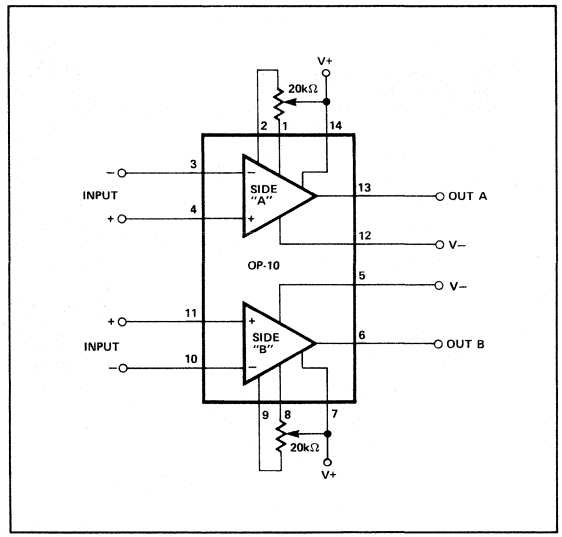
PARAMETER	SYMBOL	CONDITIONS	OP-10E MIN	OP-10E TYP	OP-10E MAX	OP-10C MIN	OP-10C TYP	OP-10C MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}		—	0.18	0.7	—	0.4	—	mV
Input Offset Voltage Tracking Without External Trim	$TC\Delta V_{OS}$	(Note 1)	—	0.9	2.3	—	1.3	—	μV/°C
With External Trim	$TC\Delta V_{OSn}$	$R_L = 20k\Omega$ Channel A Only (Note 2)	—	0.3	0.9	—	0.6	—	μV/°C
Average Noninverting Bias Current	I_B+		—	±2.0	±6.0	—	±2.8	—	nA
Average Drift of Noninverting Bias Current	TCI_B+	(Note 1)	—	12	40	—	18	—	pA/°C
Noninverting Offset Current	I_B+		—	2.0	6.0	—	2.8	—	nA
Average Drift of Noninverting Offset Current	$TCI_{OS}+$	(Note 1)	—	15	50	—	20	—	pA/°C
Input Offset Current	$I_{OS}-$		—	2.0	6.0	—	2.8	—	nA
Common-Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm 13V$	103	117	—	—	114	—	dB
Power Supply Rejection Ratio Match	ΔPSRR	$V_S = \pm 3V$ to $\pm 18V$	—	6	32	—	8	—	μV/V

NOTES:
1. Sample tested.
2. Guaranteed by design.

BURN-IN CIRCUIT



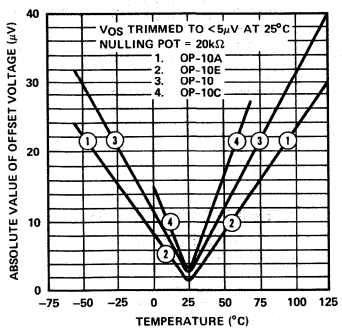
OFFSET NULLING CIRCUIT



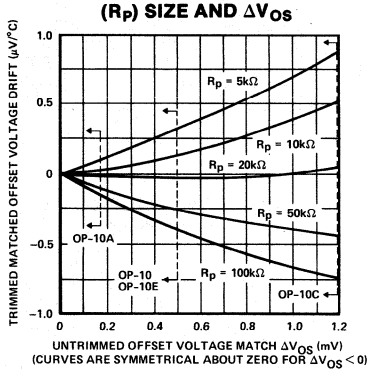
2

TYPICAL PERFORMANCE CHARACTERISTICS

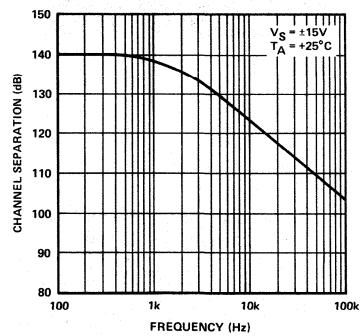
MATCHING CHARACTERISTICS TRIMMED OFFSET VOLTAGE MATCH vs TEMPERATURE



MATCHING CHARACTERISTICS TRIMMED MATCHED OFFSET VOLTAGE DRIFT AS A FUNCTION OF TRIMMING POT (R_P) SIZE AND ΔV_{OS}



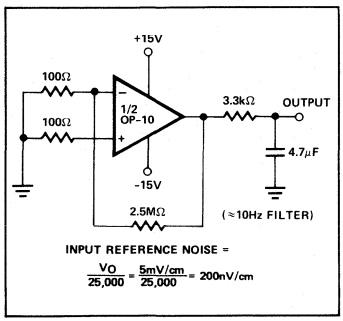
MATCHING CHARACTERISTICS CHANNEL SEPARATION vs FREQUENCY



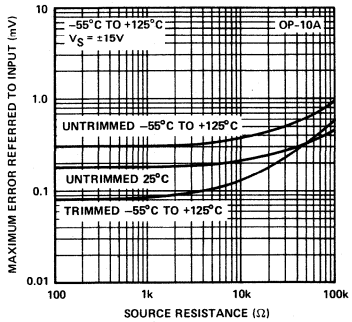
OP-10

TYPICAL PERFORMANCE CHARACTERISTICS

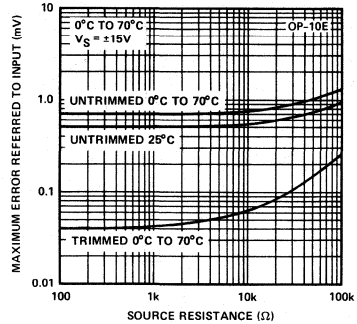
TYPICAL LOW-FREQUENCY NOISE TEST CIRCUIT



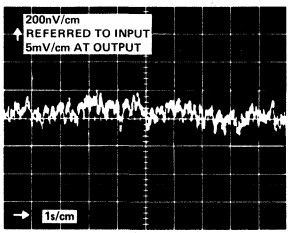
MATCHING CHARACTERISTIC MAXIMUM INPUT ERROR vs SOURCE RESISTANCE



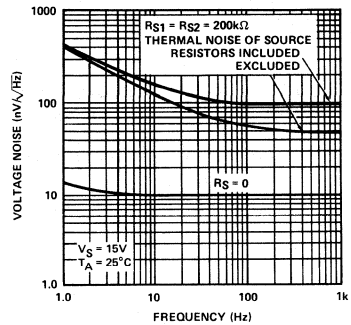
MATCHING CHARACTERISTIC MAXIMUM INPUT ERROR vs SOURCE RESISTANCE



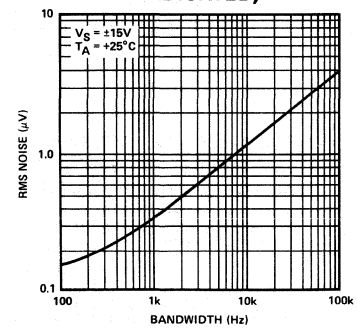
OP-10 LOW FREQUENCY NOISE



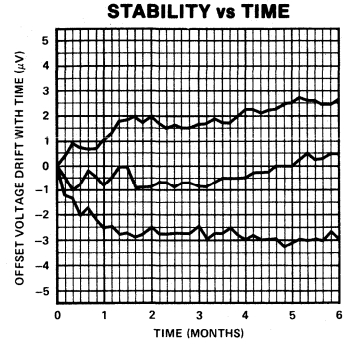
VOLTAGE NOISE DENSITY vs FREQUENCY



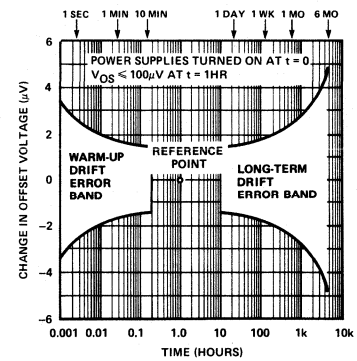
INPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



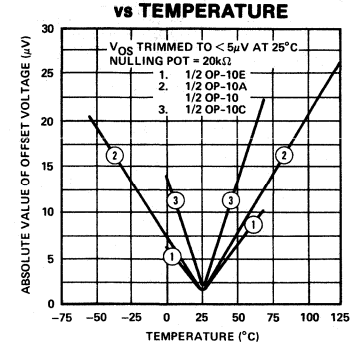
TYPICAL OFFSET VOLTAGE STABILITY vs TIME



OFFSET VOLTAGE DRIFT WITH TIME

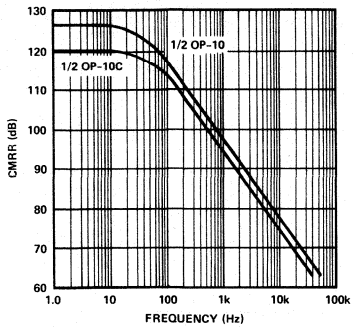


TRIMMED OFFSET VOLTAGE vs TEMPERATURE

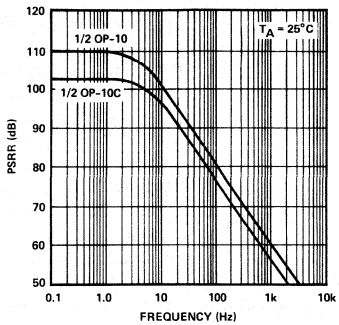


TYPICAL PERFORMANCE CHARACTERISTICS

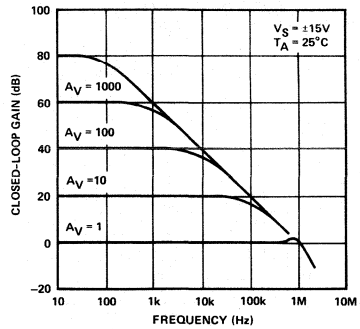
CMRR vs FREQUENCY



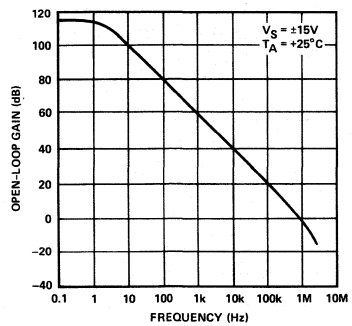
PSRR vs FREQUENCY



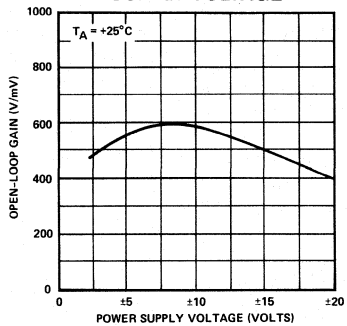
CLOSED-LOOP GAIN vs FREQUENCY



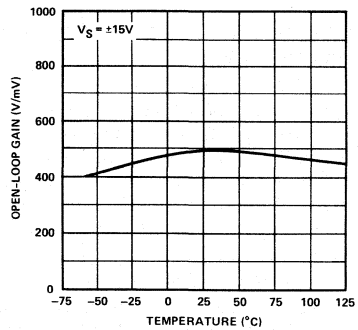
OPEN-LOOP GAIN vs FREQUENCY



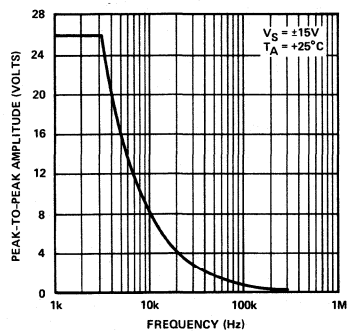
OPEN-LOOP GAIN vs POWER SUPPLY VOLTAGE



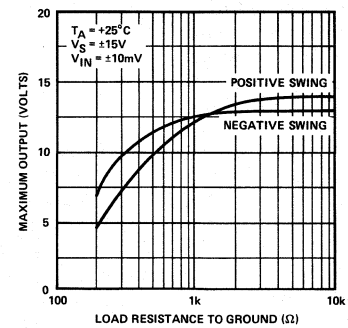
OPEN-LOOP GAIN vs TEMPERATURE



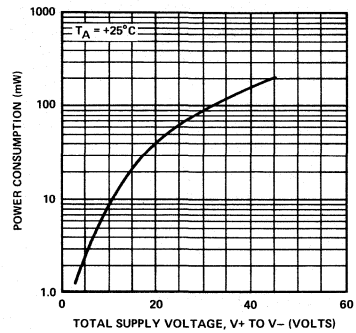
MAXIMUM OUTPUT SWING vs FREQUENCY



MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE

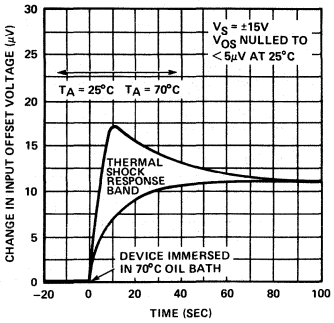


POWER CONSUMPTION vs POWER SUPPLY

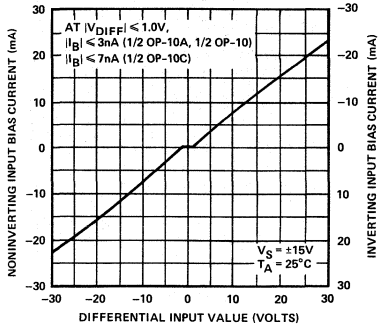


TYPICAL PERFORMANCE CHARACTERISTICS

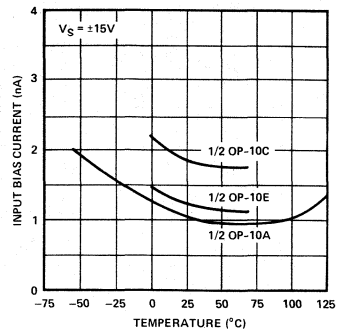
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



INPUT BIAS CURRENT vs TEMPERATURE



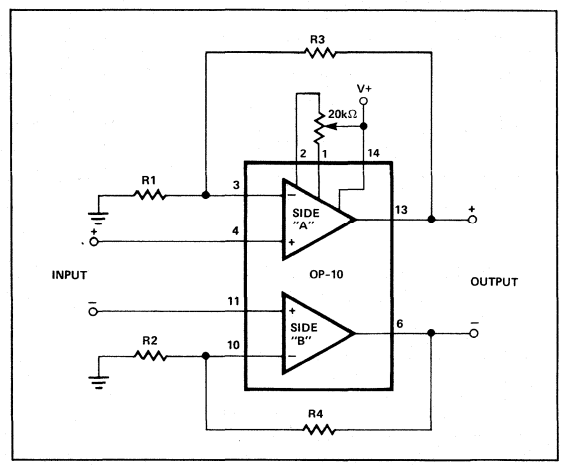
APPLICATIONS INFORMATION

ADVANTAGES OF DUAL MATCHED OPERATIONAL AMPLIFIERS

Dual matched operational amplifiers provide a powerful tool for the solution of some difficult circuit design problems. Circuits include true instrumentation amplifiers, extremely low drift, high common-mode rejection DC amplifiers, low DC drift active filters, dual tracking voltage references and many other demanding applications. These designs all require good matching between two operational amplifiers.

The adjacent circuit, a differential-in, differential-out amplifier, shows how errors can be reduced. Assuming the resistors used are matched, the gain of each side will be identical; if the offset voltage of each amplifier is matched, then the net differential voltage at the amplifiers output will be zero. Note that the output offset error of this amplifier is not a function of the offset voltage of the individual amplifiers, but only a function of the **difference** between the amplifiers' offset voltages. This error-cancellation principle holds for a number of input-referred error parameters — offset voltage, offset voltage drift, inverting and noninverting bias currents, common-mode and power supply rejection ratios. Note also that the impedances of each input, both common-mode and differential-mode, are extremely high, an important feature not possible with single operational amplifier circuits. Common-mode rejection can be made very high; this is especially important in instrumentation amplifiers where errors due to large common-mode voltages can be far greater than errors due to noise or drift with temperature.

For example, consider the case of two op amps, each with 80dB (100μV/V) CMRR. If the CMRR of one device is +100μV/V while CMRR of the other is −100μV/V, then the net CMRR will be 200μV/V, a 6dB degradation. The matching of CMRR increases the effective CMRR when used as an instrumentation input stage.



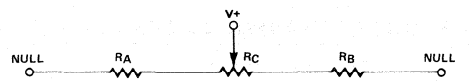
POWER SUPPLIES

The V+ supply terminals are completely independent and may be powered by separate supplies if desired (this approach, however, would sacrifice the advantages of the power supply rejection ratio matching). The V− supply terminals are both connected to the common substrate and must be tied to the same voltage.

OFFSET TRIMMING

Offset trimming terminals are provided for each amplifier of the OP-10. Guaranteed performance over temperature is obtained by trimming only one side (side A) to match the offset of the other; a net differential offset of zero results. This procedure is used during factory testing of the devices; however, essentially the same results may be obtained by trimming side B to match side A, or by nulling each side individually.

The OP-10 provides lowest drift when trimmed with a 20kΩ potentiometer; this value provides about ±4mV of adjustment range which should be more than adequate for most applications. Where finer trimming resolution is desired, or where unwanted changes in potentiometer position with time and temperature could create unacceptable offsets, the adjustment sensitivity may be reduced by using the circuit shown below.



Model	Null Range	Fixed Resistors R_A, R_B	Potentiometer R_C
OP-10AY, OP-10Y, OP-10EY	±1.2mV	5.1kΩ	10.0kΩ

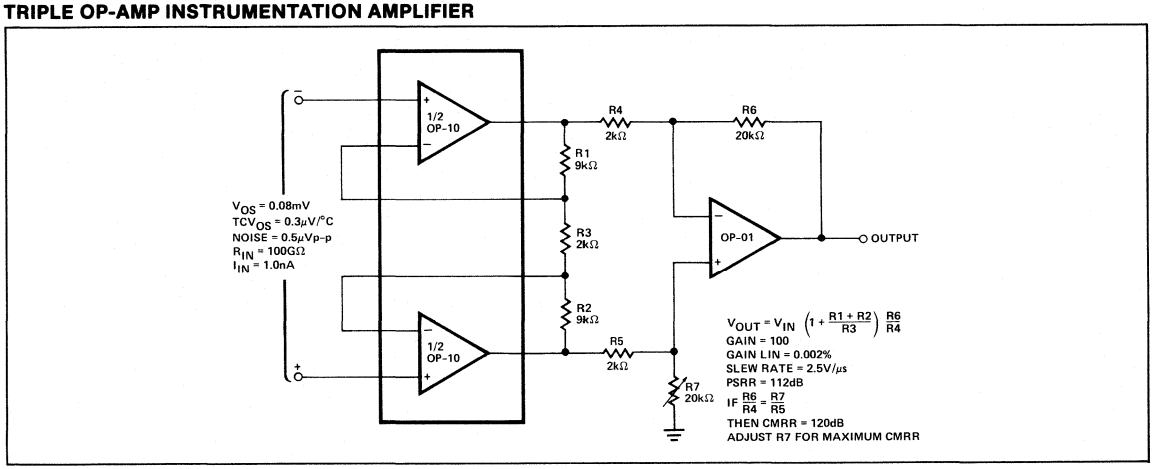
INSTRUMENTATION AMPLIFIERS USING OP-10

Instrumentation amplifiers with excellent performance can be easily built using the OP-10. Typical performance for a two and three-amplifier design are given in the table. The three-amplifier design, while more complex, has the advantages of simple gain adjustment by trimming a single resistor (R_3) and wide common-mode voltage capability at any gain, plus improved gain linearity. Slew rate, small-signal bandwidth, and full power bandwidth are also superior. Speed will be improved by using an OP-01 for the output stage.

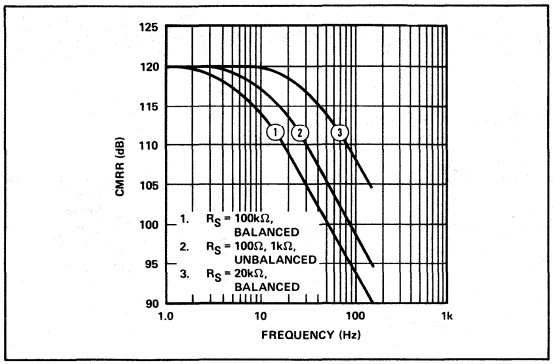
TYPICAL PERFORMANCE OF INSTRUMENTATION AMPLIFIERS GAIN = 100

PARAMETER	2 OP AMP DESIGN	3 OP AMP DESIGN
Gain Nonlinearity	0.004%	0.001% (OP-05)
		0.002% (OP-01)
Initial Input Offset Voltage	70μV	75μV
vs. Temperature (amplifier A nulled with 20k pot)	0.3μV/°C	0.3μV/°C
vs. Time	3.5μV/month	3.5μV/month
Input Bias Current	±1nA	±1nA
vs. Temperature	10pA/°C	10pA/°C
Input Offset Current	0.8nA	0.8nA
vs. Temperature	12pA/°C	12pA/°C
Input Impedance Differential	80GΩ	100GΩ
Common-Mode	100GΩ	100GΩ
Input Noise Voltage (0.1 to 10Hz)	$0.5\mu V_{p-p}$	$0.5\mu V_{p-p}$
Input Noise Current (0.1 to 10Hz)	$14pA_{p-p}$	$14pA_{p-p}$
Common-Mode Rejection	120dB	120dB
Power Supply Rejection	112dB	112dB
Frequency Response		
Small-Signal (−3dB)	6.0Hz	26kHz (OP-05) 85kHz (OP-01)
Full Power	2.5Hz	4.3kHz (OP-05) 43kHz (OP-01)
Slew Rate	0.17V/μs	0.17V/μs (OP-05) 4.0V/μs (OP-01)

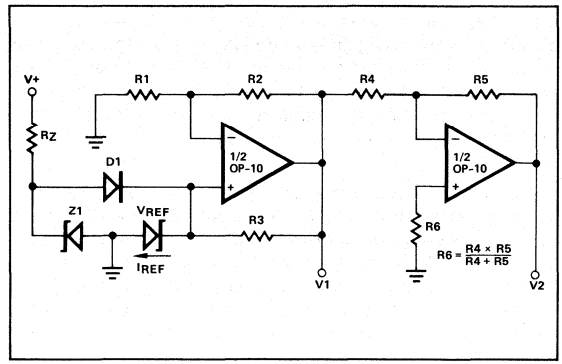
TRIPLE OP-AMP INSTRUMENTATION AMPLIFIER



CMRR vs FREQUENCY INSTRUMENTATION AMPLIFIER (3 OP-AMP DESIGN)



PRECISION DUAL TRACKING VOLTAGE REFERENCES USING OP-10



PRECISION DUAL TRACKING VOLTAGE REFERENCES USING OP-10

Precision dual tracking voltage references using a single reference source are easily constructed using OP-10. These references exhibit low noise, excellent stability vs. temperature and time, and have excellent power supply rejection.

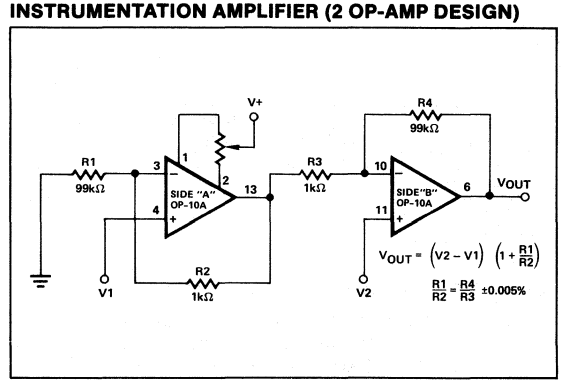
In the circuit shown, R_3 should be adjusted to set I_{REF} to operate V_{REF} at its minimum temperature coefficient current. Proper circuit start-up is assured by R_Z, Z_1, and D_1.

$$V_{Z1} \leq V_{REF} + 2V \qquad V1 = V_{REF}\left(1 + \frac{R2}{R1}\right)$$

$$I_{REF} = (V1 - V_{REF})/R3 \qquad V2 = V1\left(\frac{-R5}{R4}\right)$$

Output Impedance (ΔI_L:1.0mA-5.0mA) ..... $0.25 \times 10^{-3}\Omega$

INSTRUMENTATION AMPLIFIER (2 OP-AMP DESIGN)



ANALOG DEVICES

Precision Low-Input-Current Operational Amplifier

OP-12

FEATURES

- **Low Offset Voltage ..... 150μV Max**
- **Low Offset Voltage Drift ..... 2.5μV/°C Max**
- **Load Current Capability ..... 5mA Min**
- **Internal Frequency Compensation**
- **125°C Temperature Tested Die**
- **Low Offset Current ..... 200pA Max**
- **Low Bias Current ..... 2.0nA Max**
- **Low Power Consumption ..... 18mW Max @ ±15V**
- **High Common-Mode Input Range ..... ±13V Min**
- **MIL-STD-883 Class B Processing Available**
- **Silicon-Nitride Passivation**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (mV)	PACKAGE TO-99 8-PIN	PACKAGE CERDIP 8-PIN	OPERATING TEMPERATURE RANGE
0.15	–	OP12AZ*	MIL
0.15	OP12EJ	OP12EZ	COM
0.30	OP12BJ	OP12BZ/883	MIL
0.30	OP12FJ	OP12FZ	COM
1.0	OP12GJ	–	COM

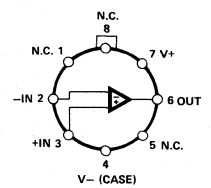
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

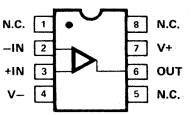
GENERAL DESCRIPTION

The PMI OP-12 is an improved version of the popular LM108A low-power op amp. The OP-12 is internally compensated and its chip dimensions are only 42 X 58 mils. Offset voltage is lower; the total worst-case input offset voltage over −55°C to +125°C for the OP-12A is only 350μV. In addition, the OP-12 drives a 2kΩ load which is five times the output current capability of the 108A. This excellent performance is achieved by applying PMI's ion-implanted super-beta process and on-chip zener-zap trimming capabilities. The internal compensation makes this op amp ideal for hybrid assembly applications.

PIN CONNECTIONS

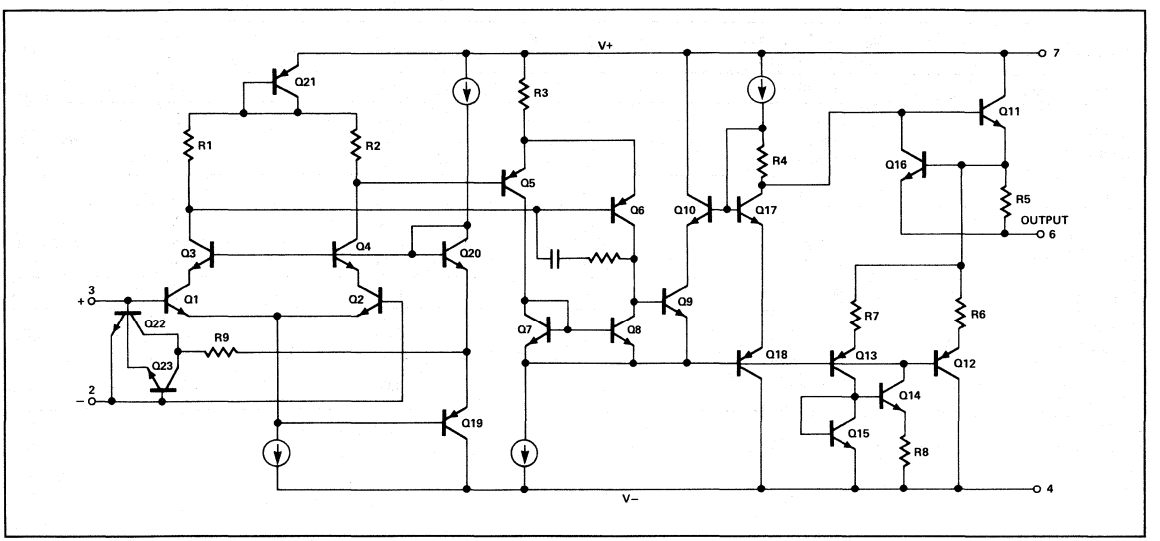


TO-99 (J-Suffix)



8-PIN HERMETIC MINI-DIP (Z-Suffix)

SIMPLIFIED SCHEMATIC



OP-12

ABSOLUTE MAXIMUM RATINGS (Note 4)

Supply Voltage
- OP-12A, OP-12B, OP-12E, OP-12F, All DICE except GR ..... ±20V
- OP-12G, GR DICE Only ..... ±18V

Operating Temperature Range
- OP-12A, OP-12B ..... –55°C to +125°C
- OP-12E, OP-12F, OP-12G ..... 0°C to +70°C

Storage Temperature Range ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Differential Input Current (Note 1) ..... ±10mA
Input Voltage (Note 2) ..... ±15V
Output Short-Circuit Duration ..... Indefinite
Junction Temperature (T_J) ..... –65°C to +150°C

PACKAGE TYPE	Θ_{JA} (NOTE 3)	Θ_{JC}	UNITS
TO-99 (J)	170	24	°C/W
8-Pin Hermetic DIP (Z)	162	26	°C/W

NOTES:
1. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is provided.
2. For supply voltages less than –15V, the absolute maximum input voltage is equal to the supply voltage.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO and CerDIP packages.
4. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 20V$ and $T_A = 25°C$ for A, B, E and F grades, $V_S = \pm 15V$, and $T_A = 25°C$ for C and G grades, unless otherwise noted.

			OP-12A/E			OP-12B/F			OP-12G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.07	0.15	—	0.18	0.30	—	0.25	1.0	mV
Input Offset Current	I_{OS}		—	0.05	0.20	—	0.05	0.20	—	0.08	0.50	nA
Input Bias Current	I_B		—	0.8	2.0	—	0.8	2.0	—	1.0	5.0	nA
Input Resistance — Differential-Mode	R_{IN}	(Note 1)	26	70	—	26	70	—	10	50	—	MΩ
Input Voltage Range	IVR	$V_S = \pm 15V$	±13	±14	—	±13	±14	—	±13	±14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	104	120	—	104	120	—	84	116	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	—	1	7	—	1	7	—	4	63	μV/V
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$, $V_S = \pm 15V$ $R_L \geq 2k\Omega$, $V_S = \pm 15V$	±13 ±10	±14 ±12	— —	±13 ±10	±14 ±12	— —	±13 ±10	±14 ±12	— —	V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 10k\Omega$ $V_O = \pm 10V$ $R_L \geq 2k\Omega$ $V_O = \pm 10V$	80 50	300 150	— —	80 50	300 150	— —	40 —	250 100	— —	V/mV
Power Consumption	P_d	$V_S = \pm 15V$, No Load $V_S = \pm 5V$, No Load	— —	9 3	18 6	— —	9 3	18 6	— —	12 4	24 8	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.9	—	—	0.9	—	—	0.9	—	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$ $f_O = 100Hz$ $f_O = 1000Hz$	— — —	22 21 20	— — —	— — —	22 21 20	— — —	— — —	22 21 20	— — —	$nV/\sqrt{Hz}$
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	—	3	—	—	3	—	—	3	—	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10Hz$ $f_O = 100Hz$ $f_O = 1000Hz$	— — —	0.15 0.14 0.13	— — —	— — —	0.15 0.14 0.13	— — —	— — —	0.15 0.14 0.13	— — —	$pA/\sqrt{Hz}$
Slew Rate	SR	$R_L \geq 2k\Omega$	—	0.12	—	—	0.12	—	—	0.12	—	V/μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$	—	0.80	—	—	0.80	—	—	0.80	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	200	—	—	200	—	—	200	—	Ω

NOTE:
1. Guaranteed by input bias current.

ELECTRICAL CHARACTERISTICS at V_S = ±20V for A and B grades, –55°C ≤ T_A ≤ +125°C, unless otherwise noted.

			OP-12A			OP-12B			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		–	0.12	0.35	–	0.28	0.60	mV
Average Input Offset Voltage Drift	TCV_{OS}		–	0.50	2.5	–	1.0	3.5	µV/°C
Input Offset Current	I_{OS}		–	0.12	0.40	–	0.12	0.40	nA
Average Input Offset Current Drift	TCI_{OS}		–	0.50	2.5	–	0.50	2.5	pA/°C
Input Bias Current	I_B		–	1.2	3.0	–	1.2	3.0	nA
Input Voltage Range	IVR	V_S = ±15V	±13	± 14	–	±13	±14	–	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V	100	116	–	100	116	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5 to ±15V	–	4	10	–	4	10	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 5kΩ V_O = ±10V	40	120	–	40	120	–	V/mV
Output Voltage Swing	V_O	R_L ≥ 10kΩ, V_S = ±15V R_L ≥ 5kΩ, V_S = ±15V	±13 ±10	±14 ±13	– –	±13 ±10	±14 ±13	– –	V
Power Consumption	P_d	V_S = ±15V, No Load	–	9	18	–	9	18	mW

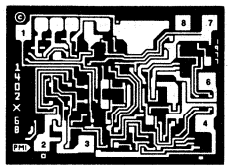
ELECTRICAL CHARACTERISTICS at V_S = ±15V for G grade, V_S = ±20V for E and F grades, 0°C ≤ T_A ≤ 70°C, unless otherwise noted.

			OP-12E			OP-12F			OP-12G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.10	0.26	—	0.23	0.45	—	0.32	1.4	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.50	2.5	—	1.0	3.5	—	1.5	10	µV/°C
Input Offset Current	I_{OS}		—	0.08	0.30	—	0.11	0.60	—	0.12	0.70	nA
Average Input Offset Current Drift	TCI_{OS}		—	0.50	2.5	—	1.0	5.0	—	1.0	5.0	pA/°C
Input Bias Current	I_B		—	1.0	2.6	—	1.2	5.2	—	1.4	6.5	nA
Input Voltage Range	IVR	V_S = ±15V	±13	±14	—	±13	±14	—	±13	±14	—	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V	100	116	—	100	116	—	80	112	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5 to ±15V	—	4	10	—	4	10	—	6	100	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 10kΩ V_O = ±10V R_L ≥ 2kΩ V_O = ±10V	60 25	200 100	— —	60 25	200 100	— —	25 —	150 80	— —	V/mV
Output Voltage Swing	V_O	R_L ≥ 10kΩ V_S = ±15V R_L ≥ 5kΩ V_S = ±15V	±13 ±10	±14 ±12	— —	±13 ±10	±14 ±12	— —	±13 ±10	±14 ±12	— —	V
Power Consumption	P_d	V_S = ±15V, No Load	—	9	18	—	9	18	—	15	24	mW

For typical performance characteristics, see OP-08 data sheet. Assume C_C = 30pF.

OP-12

DICE CHARACTERISTICS (125°C TESTED DICE AVAILABLE)



DIE SIZE 0.059 × 0.043 inch, 2537 sq. mils
(1.50 × 1.09 mm, 1.64 sq. mm)

1. NO CONNECTION
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V–
6. OUTPUT
7. V +
8. NO CONNECTION

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$ for OP-12N, OP-12G and OP-12GR devices; $T_A = 125°C$ for OP-12NT and OP-12GT devices, unless otherwise noted. (Note 2)

PARAMETER	SYMBOL	CONDITIONS	OP-12NT LIMIT	OP-12N LIMIT	OP-12GT LIMIT	OP-12G LIMIT	OP-12GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		0.35	0.15	0.6	0.3	1	mV MAX
Input Offset Current	I_{OS}		0.4	0.2	0.4	0.2	0.5	nA MAX
Input Bias Current	I_B		3	2	3	2	5	nA MAX
Input Voltage Range	IVR		±13	±13	±13	±13	±13	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	100	104	100	104	84	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	10	7	10	7	63	µV/V MAX
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	±13	±13	±13	±13	±13	V MIN
		$R_L \geq 2k\Omega$	—	±10	—	±10	±10	
		$R_L \geq 5k\Omega$	±10	—	±10	—	—	
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 10k\Omega$, $V_O = \pm 10V$	80	80	80	80	40	V/mV MIN
		$R_L \geq 2k\Omega$, $V_O = \pm 10V$	—	50	—	50	—	
		$R_L \geq 5k\Omega$, $V_O = \pm 10V$	40	—	40	—	—	
Input Resistance	R_{IN}	(Note 1)	26	26	26	26	10	MΩ MIN
Supply Current	I_{SY}	$I_{OUT} = 0$, $V_{OUT} = 0$	0.6	0.6	0.6	0.6	0.8	mA MAX

NOTES:
1. Guaranteed by design.
2. For 25°C specifications of OP-12NT and OP-12GT, see OP-12N and OP-12G, respectively.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-12NT TYPICAL	OP-12N TYPICAL	OP-12GT TYPICAL	OP-12G TYPICAL	OP-12GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}		0.5	0.5	1.0	1.0	1.5	µV/°C
Average Input Offset Current Drift	TCI_{OS}		0.5	0.5	1.0	1.0	1.0	pA/°C

ANALOG DEVICES

Precision JFET-Input Operational Amplifiers

OP-15/OP-16/OP-17

FEATURES (All Devices)

- Significant Performance Advantages over LF155, 156 and 157 Devices.
- Low Input Offset Voltage ..... 500μV Max
- Low Input Offset Voltage Drift ..... 2.0μV/°C
- Minimum Slew Rate Guaranteed on All Models
- Temperature-Compensated Input Bias Currents
- Guaranteed Input Bias Current @ 125°C
- Bias Current Specified WARMED UP Over Temperature
- Internal Compensation
- Low Input Noise Current .....0.01pA/$\sqrt{Hz}$
- High Common-Mode Rejection Ratio 100dB
- Models With MIL-STD-883 Processing Available
- 125°C Temperature Tested DICE

OP-15

- 156 Speed With 155 Dissipation ..... (80mW Typ)
- Wide Bandwidth 6MHz
- High Slew Rate 13V/μs
- Fast Settling to ±0.1% 1200ns
- Available in Die Form

OP-16

- Higher Slew Rate 25V/μs
- Faster Settling to ±0.1% 900ns
- Wider Bandwidth 8MHz
- Available in Die Form

OP-17

- Highest Slew Rate 60V/μs
- Fastest Settling to ±0.1% 600ns
- Highest Gain Bandwidth Product (A_{VCL} = 5 Min) 30MHz
- Available in Die Form

GENERAL DESCRIPTION

The PMI JFET-input series of devices offer clear advantages over industry-generic devices and are superior in both cost and performance to many dielectrically-isolated and hybrid op amps. All devices offer offset voltages as low as 0.5mV with TCV_{OS} guaranteed to 5μV/°C. A unique input bias cancellation circuit reduces the I_B by a factor of 10 over conventional designs. In addition, PMI specifies I_B and I_{OS} with the devices warmed up and operating at 25°C ambient.

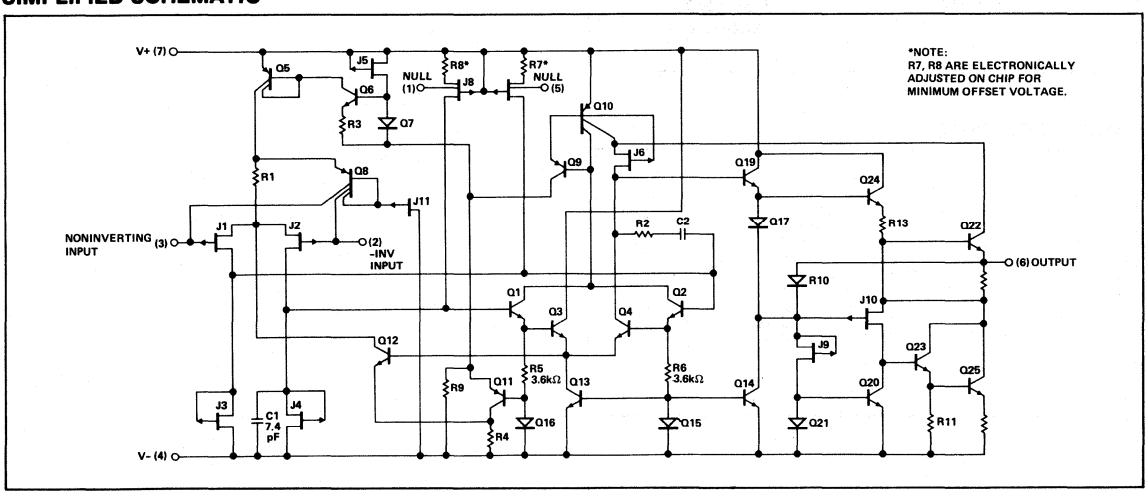
These devices were designed to provide real precision performance along with high speed. Although they can be nulled, the design objective was to provide low offset-voltage without nulling. Systems generally become more cost effective as the number of trim circuits is decreased. PMI achieves this performance by use of an improved Bipolar compatible JFET process coupled with on-chip, zener-zap offset trimming.

The OP-15 provides an excellent combination of high speed and low input offset voltage. In addition, the OP-15 offers the speed of the 156A op amp with the power dissipation of a 155A. The combination of a low input offset voltage of 500μV, slew rate of 13V/μs, and settling time of 1200ns to 0.1% makes the OP-15 an op amp of both precision and speed. The additional features of low supply current coupled with an input bias current of 9nA at 125°C ambient (not junction) temperature makes the OP-15 ideal for a wide range of applications.

The OP-16 features a slew rate of 25V/μs and a settling time of 900ns to 0.1% which represents a significant improvement in speed over the 156. Also, the OP-16 has all the DC features of the OP-15.

The OP-17 has a slew rate of 60V/μs and is the best choice for applications requiring high closed-loop gain with high speed. See the OP-42 data sheet for unity gain applications and the OP-215 data sheet for a dual configuration of the OP-15.

SIMPLIFIED SCHEMATIC



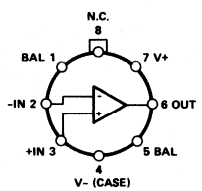
ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (mV)	PACKAGE TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	SO 8-PIN	OPERATING TEMPERATURE RANGE
0.5	OP15AJ*	OP15AZ*	–	–	MIL
	OP16AJ*	–	–	–	
	OP17AJ*	OP17AZ*	–	–	
0.5	OP15EJ	OP15EZ	–	–	COM
	OP16EJ	OP16EZ	–	–	
	OP17EJ	OP17EZ	–	–	
1.0	OP15BJ/883	OP15BZ/883	–	–	MIL
	OP16BJ/883	OP16BZ/883	–	–	
	OP17BJ*	OP17BZ	–	–	
1.0	OP15FJ	OP15FZ	OP15FP	–	COM
	OP16FJ	OP16FZ	OP16FP	–	
	–	–	OP17FP	–	
3.0	–	OP17CZ/883	–	–	MIL
	OP17CJ/883C	–	–	–	
3.0	OP15GJ	OP15GZ	OP15GP	OP15GS	XIND
	OP16GJ	OP16GZ	OP16GP	OP16GS	
	OP17GJ	OP17GZ	OP17GP	OP17GS	

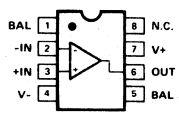
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

PIN CONNECTIONS



TO-99
(J-Suffix)

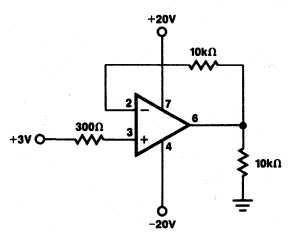


8-PIN CERDIP
(Z-Suffix)

8-PIN PLASTIC DIP
(P-Suffix)

8-PIN SO
(S-Suffix)

BURN-IN CIRCUIT



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage
- All Devices Except C, G (Packaged) & GR Grades ..... ±22V
- C, G (Packaged) & GR Grades ..... ±18V

Operating Temperature
- A, B, & C Grades ..... –55°C to +125°C
- E & F Grades ..... 0°C to +70°C
- G Grade ..... –40°C to +85°C

Maximum Junction Temperature ..... +150°C

DICE Junction Temperature (T_j) ..... –65°C to +150°C

Differential Input Voltage
- All Devices Except C, G (Packaged) & GR Grades ..... ±40V
- C, G (Packaged) & GR Grades ..... ±30V

Input Voltage (Note 2)
- All Devices Except C, G (Packaged) & GR Grades ..... ±20V
- C, G (Packaged) & GR Grades ..... ±16V

Input Voltage
- OP-15A, OP-15B, OP-15E, OP-15F ..... ±20V
- OP-15G ..... ±16V
- OP-16A, OP-16B, OP-16E, OP-16F ..... ±20V
- OP-16C, OP-16G ..... ±16V
- OP-17A, OP-17B, OP-17E, OP-17F ..... ±20V
- OP-17C, OP-17G ..... ±16V

Output Short-Circuit Duration ..... Indefinite

Storage Temperature Range ..... –65°C to +150°C

Lead Temperature Range (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 3)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power-supply voltage.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		OP-15A/E OP-16A/E OP-17A/E MIN	TYP	MAX	OP-15B/F OP-16B/F OP-17B/F MIN	TYP	MAX	OP-15G OP-16C/G OP-17C/G MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$		—	0.2	0.5	—	0.4	1.0	—	0.5	3.0	mV
Input Offset Current	I_{OS}	$T_j = 25°C$ (Note 1)	OP-15	—	3	10	—	6	20	—	12	50	pA
		Device Operating	OP-15	—	5	22	—	10	40	—	20	100	pA
		$T_j = 25°C$ (Note 1)	OP-16/OP-17	—	3	10	—	6	20	—	12	50	pA
		Device Operating	OP-16/OP-17	—	5	25	—	10	50	—	20	125	pA
Input Bias Current	I_B	$T_j = 25°C$ (Note 1)	OP-15	—	±15	±50	—	±30	±100	—	±60	±200	pA
		Device Operating	OP-15	—	±18	±110	—	±40	±200	—	±80	±400	pA
		$T_j = 25°C$ (Note 1)	OP-16/OP-17	—	±15	±50	—	±30	±100	—	±60	±200	pA
		Device Operating	OP-16/OP-17	—	±20	±130	—	±40	±250	—	±80	±500	pA
Input Resistance	R_{IN}			—	10^{12}	—	—	10^{12}	—	—	10^{12}	—	Ω
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$		100	240	—	75	220	—	50	200	—	V/mV
Output Voltage Swing	V_O	$R_L = 10k\Omega$		±12	±13	—	±12	±13	—	±12	±13	—	V
		$R_L = 2k\Omega$		±11	±12.7	—	±11	±12.7	—	±11	±12.7	—	V
Supply Current	I_{SY}		OP-15	—	2.7	4.0	—	2.7	4.0	—	2.8	5.0	mA
			OP-16/OP-17	—	4.6	7.0	—	4.6	7.0	—	4.8	8.0	mA
Slew Rate	SR	$A_{VCL} = +1$ (Note 3)	OP-15	10	13	—	7.5	11	—	5	9	—	V/μs
			OP-16	18	25	—	12	21	—	9	17	—	V/μs
		$A_{VCL} = +5$ (Note 3)	OP-17	45	60	—	35	50	—	25	40	—	V/μs
Gain Bandwidth Product	GBW	(Note 3)	OP-15	4.0	6.0	—	3.5	5.7	—	3.0	5.4	—	MHz
			OP-16	6.0	8.0	—	5.5	7.6	—	5.0	7.2	—	MHz
			OP-17	20	30	—	15	28	—	11	26	—	MHz
Closed-Loop Bandwidth	CLBW	$A_{VCL} = +1$	OP-15	—	14	—	—	13	—	—	12	—	MHz
			OP-16	—	19	—	—	18	—	—	17	—	MHz
		$A_{VCL} = +5$	OP-17	—	11	—	—	10	—	—	9	—	MHz
Settling Time	t_S	to 0.01%		—	4.5	—	—	4.5	—	—	4.7	—	μs
		to 0.05% (Note 2)	OP-15	—	1.5	—	—	1.5	—	—	1.6	—	μs
		to 0.10%		—	1.2	—	—	1.2	—	—	1.3	—	μs
		to 0.01%		—	3.8	—	—	3.8	—	—	4.0	—	μs
		to 0.05% (Note 2)	OP-16	—	1.2	—	—	1.2	—	—	1.3	—	μs
		to 0.10%		—	0.9	—	—	0.9	—	—	1.0	—	μs
		to 0.01%		—	1.5	—	—	1.5	—	—	1.6	—	μs
		to 0.05% (Note 4)	OP-17	—	0.7	—	—	0.7	—	—	0.8	—	μs
		to 0.10%		—	0.6	—	—	0.6	—	—	0.7	—	μs
Input Voltage Range	IVR			±10.5	—	—	±10.5	—	—	±10.3	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10.5V$		86	100	—	86	100	—	—	—	—	dB
		$V_{CM} = \pm 10.3V$		—	—	—	—	—	—	82	96	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 18V$		—	10	51	—	10	51	—	—	—	μV/V
		$V_S = \pm 10V$ to $\pm 15V$		—	—	—	—	—	—	—	10	80	μV/V
Input Noise Voltage Density	e_n	$f_O = 100Hz$		—	20	—	—	20	—	—	20	—	$nV/\sqrt{Hz}$
		$f_O = 1000Hz$		—	15	—	—	15	—	—	15	—	$nV/\sqrt{Hz}$
Input Noise Current Density	i_n	$f_O = 100Hz$		—	0.01	—	—	0.01	—	—	0.01	—	$pA/\sqrt{Hz}$
		$f_O = 1000Hz$		—	0.01	—	—	0.01	—	—	0.01	—	$pA/\sqrt{Hz}$
Input Capacitance	C_{IN}			—	3	—	—	3	—	—	3	—	pF

NOTES:

1. Input bias current is specified for two different conditions. The $T_j = 25°C$ specification is with the junction at ambient temperature; the Device Operating specification is with the device operating in a warmed-up condition at 25°C ambient. The warmed-up bias current value is correlated to the junction temperature value via the curves of I_B vs T_j and I_B vs T_A. PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
2. Settling time is defined here for a unity gain inverter connection using 2kΩ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within a specified percent of its final value from the time a 10V step input is applied to the inverter. See settling time test circuit.
3. Sample tested.
4. Settling time is defined here for a $A_V = -5$ connection with $R_F = 2k\Omega$. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 2V step input is applied to the inverter. See settling time test circuit.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq 125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		OP-15A OP-16A OP-17A MIN	TYP	MAX	OP-15B OP-16B OP-17B MIN	TYP	MAX	OP-16C OP-17C MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$		—	0.4	0.9	—	0.7	2.0	—	0.9	4.5	mV
Average Input Offset Voltage Drift		(Note 2)											
Without External Trim	TCV_{OS}			—	2	5	—	3	10	—	4	15	µV/°C
With External Trim	TCV_{OSn}	$R_P = 100k\Omega$		—	2	—	—	3	—	—	4	—	µV/°C
Input Offset Current (Note 1)	I_{OS}	$T_j = 125°C$		—	0.6	4.0	—	0.8	6.0	—	1.0	9.0	nA
		$T_A = 125°C$ Device Operating	OP-15	—	0.8	7.0	—	1.2	11	—	1.5	17	nA
		$T_j = 125°C$		—	0.6	4.0	—	0.8	6.0	—	1.0	9.0	nA
		$T_A = 125°C$ Device Operating	OP-16/OP-17	—	1.0	8.5	—	1.3	14.5	—	1.7	22	nA
Input Bias Current (Note 1)	I_B	$T_j = 125°C$		—	±1.2	±5.0	—	±1.5	±7.5	—	±1.8	±10	nA
		$T_A = 125°C$ Device Operating	OP-15	—	±1.7	±9.0	—	±2.2	±14	—	±2.7	±19	nA
		$T_j = 125°C$		—	±1.2	±5.0	—	±1.5	±7.5	—	±1.8	±10	nA
		$T_A = 125°C$ Device Operating	OP-16/OP-17	—	±2.0	±11	—	±2.5	±18	—	±3.0	±25	nA
Input Voltage Range	IVR			±10.4	—	—	±10.4	—	—	±10.25	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10.4V$		85	97	—	85	97	—	—	—	—	dB
		$V_{CM} = \pm 10.25V$		—	—	—	—	—	—	80	93	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 18V$		—	15	57	—	15	57	—	—	—	µV/V
		$V_S = \pm 10V$ to $\pm 15V$		—	—	—	—	—	—	—	23	100	µV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$		35	120	—	30	110	—	25	100	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$		±12	±13	—	±12	±13	—	±12	±13	—	V

NOTES:

1. Input bias current is specified for two different conditions. The $T_j = 25°C$ specification is with the junction at ambient temperature; the Device Operating specification is with the device operating in a warmed-up condition at 25°C ambient. The warmed-up bias current value is correlated to the junction temperature value via the curves of I_B vs T_j and I_B vs T_A. PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
2. Sample tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0°C \le T_A \le 70°C$ for E and F, $-40 \le T_A \le +85°C$ for G grade, unless otherwise noted.

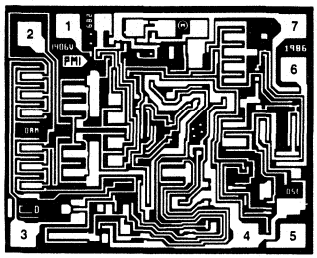
PARAMETER	SYMBOL	CONDITIONS		OP-15E OP-16E OP-17E MIN	TYP	MAX	OP-15F OP-16F OP-17F MIN	TYP	MAX	OP-15G OP-16G OP-17G MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$		—	0.3	0.75	—	0.55	1.5	—	0.7	3.8	mV
Average Input Offset Voltage Drift											(Note 2)		
Without External Trim	TCV_{OS}			—	2	5	—	3	10	—	4	30	µV/°C
With External Trim	TCV_{OSn}	$R_P = 100k\Omega$		—	2	—	—	3	—	—	4	—	
Input Offset Current (Note 1)	I_{OS}	$T_j = 70°C$		—	0.04	0.30	—	0.06	0.45	—	0.08	0.65	nA
		$T_A = 70°C$ Device Operating	OP-15	—	0.06	0.55	—	0.08	0.80	—	0.10	1.2	
		$T_j = 70°C$		—	0.04	0.30	—	0.06	0.45	—	0.08	0.65	
		$T_A = 70°C$ Device Operating	OP-16/OP-17	—	0.07	0.70	—	0.10	1.1	—	0.15	1.7	
Input Bias Current (Note 1)	I_B	$T_j = 70°C$		—	±0.10	±0.40	—	±0.12	±0.60	—	±0.14	±0.80	nA
		$T_A = 70°C$ Device Operating	OP-15	—	±0.13	±0.75	—	±0.16	±1.1	—	±0.19	±1.5	
		$T_j = 70°C$		—	±0.10	±0.40	—	±0.12	±0.60	—	±0.14	±0.80	
		$T_A = 70°C$ Device Operating	OP-16/OP-17	—	±0.15	±0.90	—	±0.20	±1.4	—	±0.25	±2.0	
Input Voltage Range	IVR			±10.4	—	—	±10.4	—	—	±10.25	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10.4V$		85	98	—	85	98	—	—	—	—	dB
		$V_{CM} = \pm 10.25V$		—	—	—	—	—	—	80	94	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 18V$		—	13	57	—	13	57	—	—	—	µV/V
		$V_S = \pm 10V$ to $\pm 15V$		—	—	—	—	—	—	—	20	100	
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$ $V_O = \pm 10V$		65	200	—	50	180	—	35	160	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 10k\Omega$		±12	±13	—	±12	±13	—	±12	±13	—	V

NOTES:

1. Input bias current is specified for two different conditions. The $T_j = 25°C$ specification is with the junction at ambient temperature; the Device Operating specification is with the device operating in a warmed-up condition at 25°C ambient. The warmed-up bias current value is correlated to the junction temperature value via the curves of I_B vs T_j and I_B vs T_A. PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
2. Sample tested.

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)

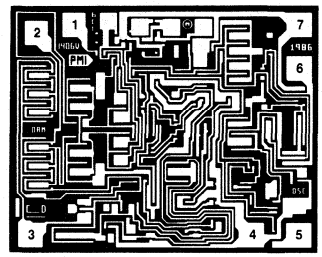
OP-15



DIE SIZE 0.068 × 0.056 inch, 3808 sq. mils (1.73 × 1.42mm, 2.46 sq. mm)

1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V−
5. BALANCE
6. OUTPUT
7. V+

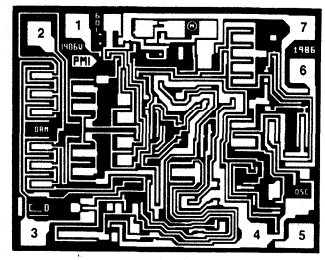
OP-16



DIE SIZE 0.068 × 0.056 inch, 3808 sq. mils (1.73 × 1.42mm, 2.46 sq. mm)

1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V−
5. BALANCE
6. OUTPUT
7. V+

OP-17



DIE SIZE 0.068 × 0.056 inch, 3808 sq. mils (1.73 × 1.42mm, 2.46 sq. mm)

1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V−
5. BALANCE
6. OUTPUT
7. V+

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$ for OP-15/16/17N, OP-15/16/17G and OP-15/16/17GR devices; $T_A = 125°C$ for OP-15/16/17NT and OP-15/16/17GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-15NT OP-16NT OP-17NT LIMIT	OP-15N OP-16N OP-17N LIMIT	OP-15GT OP-16GT OP-17GT LIMIT	OP-15G OP-16G OP-17G LIMIT	OP-15GR OP-16GR OP-17GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	0.9	0.5	2.0	1.0	3.0	mV MAX
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$, $R_L = 2k\Omega$	35	100	30	75	50	V/mV MIN
Input Voltage Range	IVR		±10.4	±10.5	±10.4	±10.5	±10.3	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm IVR$	85	86	85	86	82	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 20V$	57	51	57	51	—	µV/V MAX
		$V_S = \pm 10V$ to $\pm 15V$	—	—	—	—	80	
Output Voltage Swing	V_O	$R_L = 10k\Omega$	±12	±12	±12	±12	±12	V MIN
		$R_L = 2k\Omega$	—	±11	—	±11	±11	
Supply Current	I_{SY}	OP-15	—	4	—	4	5	mA MAX
		OP-16, OP-17	—	7	—	7	8	
Input Bias Current	I_B	OP-15	±9	—	±14	—	—	nA MAX
		OP-16, OP-17	±11	—	±18	—	—	
Input Offset Current	I_{OS}	OP-15	7.0	—	11.0	—	—	nA MAX
		OP-16, OP-17	8.5	—	14.5	—	—	

NOTES:
For 25° C characteristics of OP-15/16/17NT and OP-15/16/17GT, see OP-15/16/17N and OP-15/16/17G characteristics, respectively.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

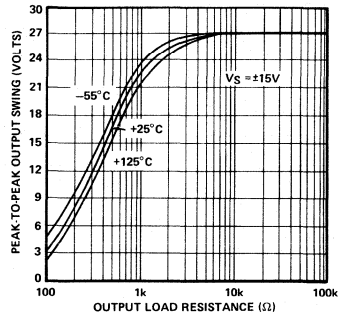
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		OP-15NT OP-16NT OP-17NT TYPICAL	OP-15N OP-16N OP-17N TYPICAL	OP-15GT OP-16GT OP-17GT TYPICAL	OP-15G OP-16G OP-17G TYPICAL	OP-15GR OP-16GR OP-17GR TYPICAL	UNITS
Average Input Offset Drift Unnulled	TCV_{OS}			2	2	3	3	4	µV/°C
Average Input Offset Drift Nulled	TCV_{OSn}	$R_P = 100k\Omega$		2	2	3	3	4	µV/°C
Input Offset Current	I_{OS}			3	3	3	3	3	pA
Input Bias Current	I_B			±15	±15	±15	±15	±15	pA
Slew Rate	SR	$A_{VCL} = +1$	OP-15	13	13	11	11	9	V/µs
			OP-16	25	25	21	21	17	
		$A_{VCL} = +5$	OP-17	60	60	50	50	40	
Settling Time (see settling time test circuits)	t_S	to 0.01%		4.5	4.5	4.5	4.5	4.7	µs
		to 0.05%	OP-15	1.5	1.5	1.5	1.5	1.6	
		to 0.10%		1.2	1.2	1.2	1.2	1.3	
		to 0.01%		3.8	3.8	3.8	3.8	4.0	
		to 0.05%	OP-16	1.2	1.2	1.2	1.2	1.3	
		to 0.10%		0.9	0.9	0.9	0.9	1.0	
		to 0.01%		1.5	1.5	1.5	1.5	1.6	
		to 0.05%	OP-17	0.7	0.7	0.7	0.7	0.8	
		to 0.10%		0.6	0.6	0.6	0.6	0.7	
Gain Bandwidth Product	GBW		OP-15	6.0	6.0	5.7	5.7	5.4	MHz
			OP-16	8.0	8.0	7.6	7.6	7.2	
			OP-17	30	30	28	28	26	
Closed-Loop Bandwidth	CLBW	$A_{VCL} = +1$	OP-15	14	14	13	13	12	MHz
			OP-16	19	19	18	18	17	
		$A_{VCL} = +5$	OP-17	11	11	10	10	9	
Input Noise Voltage Density	e_n	f = 100Hz		20	20	20	20	20	$nV/\sqrt{Hz}$
		f = 1000Hz		15	15	15	15	15	
Input Noise Current Density	i_n	f = 100Hz		0.01	0.01	0.01	0.01	0.01	$pA/\sqrt{Hz}$
		f = 1000Hz		0.01	0.01	0.01	0.01	0.01	
Input Capacitance	C_{IN}			3	3	3	3	3	pF

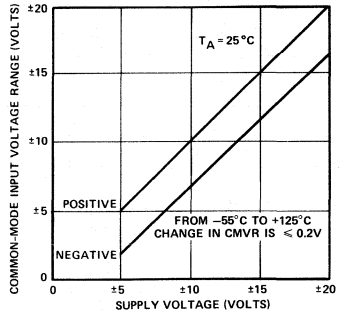
NOTES:
For 25°C characteristics of OP-15/16/17NT and OP-15/16/17GT, see OP-15/16/17N and OP-15/16/17G characteristics, respectively.

TYPICAL PERFORMANCE CHARACTERISTICS (OP-15/OP-16/OP-17)

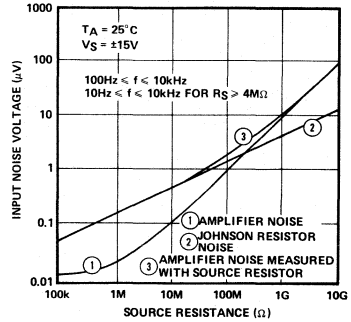
MAXIMUM OUTPUT SWING vs LOAD RESISTANCE



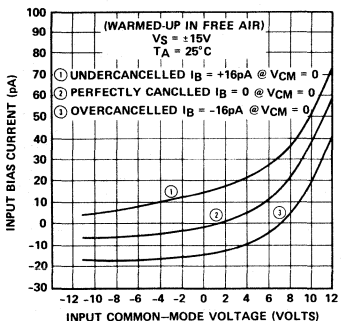
COMMON-MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE



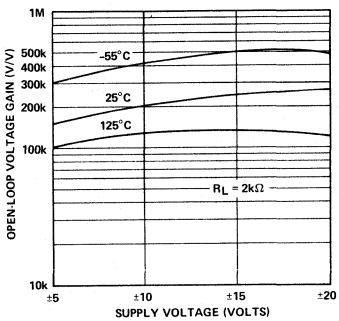
VOLTAGE NOISE vs SOURCE RESISTANCE



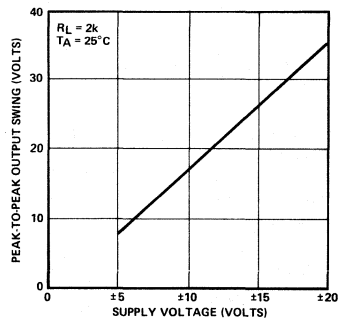
INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE



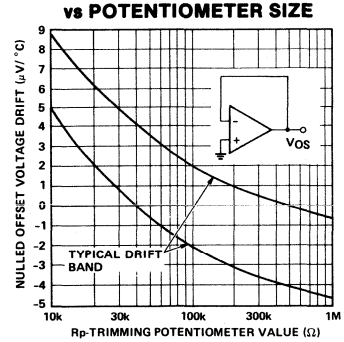
OPEN-LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE



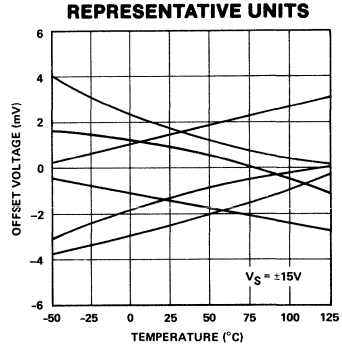
OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE



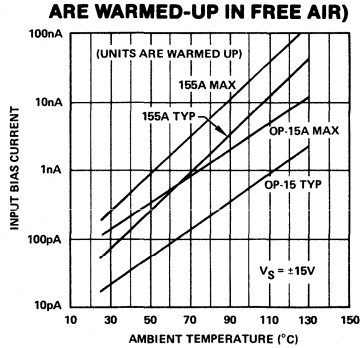
NULLED OFFSET VOLTAGE DRIFT vs POTENTIOMETER SIZE



OFFSET VOLTAGE DRIFT vs TEMPERATURE OF REPRESENTATIVE UNITS

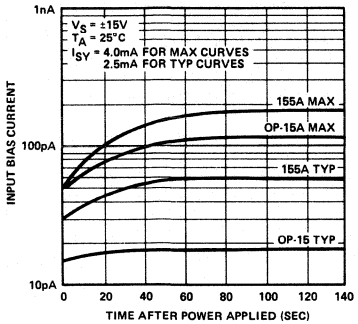


INPUT BIAS CURRENT vs AMBIENT TEMPERATURE (UNITS ARE WARMED-UP IN FREE AIR)

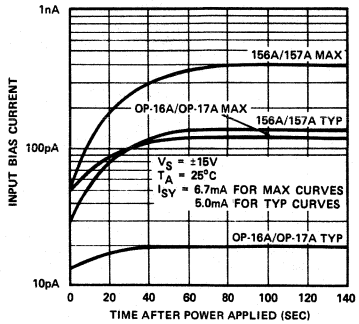


TYPICAL PERFORMANCE CHARACTERISTICS (OP-15/OP-16/OP-17)

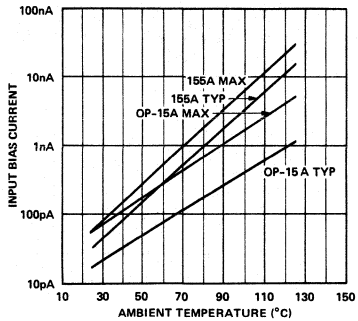
BIAS CURRENT vs TIME IN FREE AIR (OP-15)



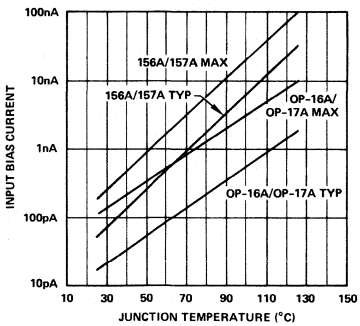
BIAS CURRENT vs TIME IN FREE AIR (OP-16/OP-17)



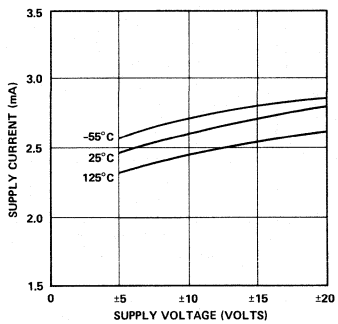
INPUT BIAS CURRENT vs AMBIENT TEMPERATURE (UNITS ARE WARMED-UP IN FREE AIR) (OP-15)



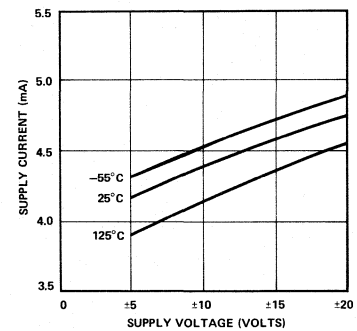
INPUT BIAS CURRENT vs AMBIENT TEMPERATURE (UNITS ARE WARMED-UP IN FREE AIR) (OP-16/OP-17)



SUPPLY CURRENT vs SUPPLY VOLTAGE (OP-15)

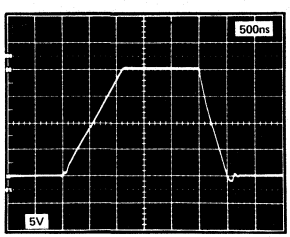


SUPPLY CURRENT vs SUPPLY VOLTAGE (OP-16/OP-17)

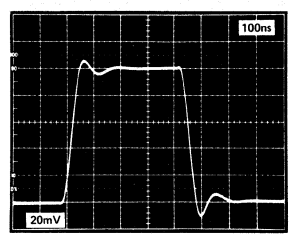


TYPICAL PERFORMANCE CHARACTERISTICS (OP-15)

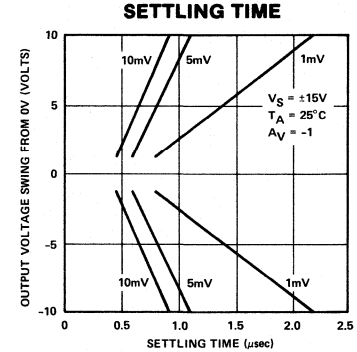
LARGE-SIGNAL TRANSIENT RESPONSE



SMALL-SIGNAL TRANSIENT RESPONSE

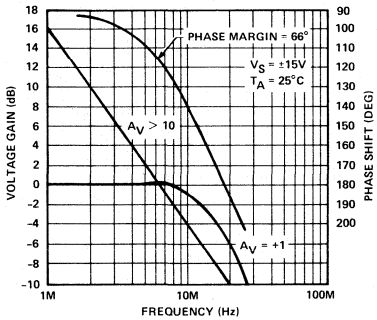


SETTLING TIME

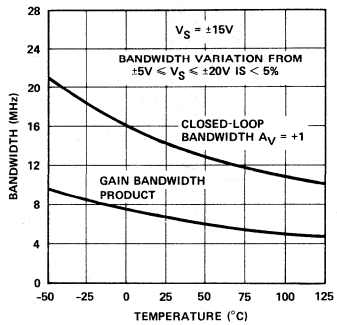


TYPICAL PERFORMANCE CHARACTERISTICS (OP-15)

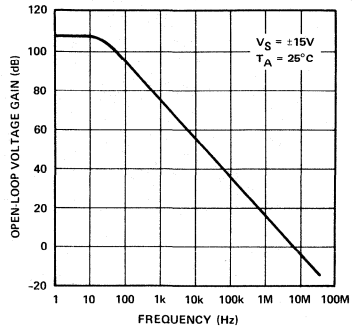
CLOSED-LOOP BANDWIDTH AND PHASE SHIFT vs FREQUENCY



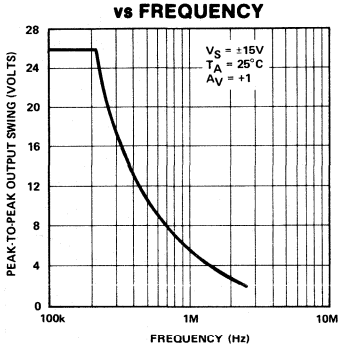
BANDWIDTH vs TEMPERATURE



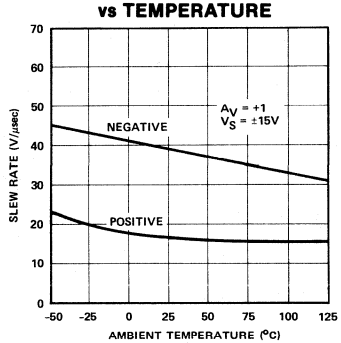
OPEN-LOOP GAIN vs FREQUENCY



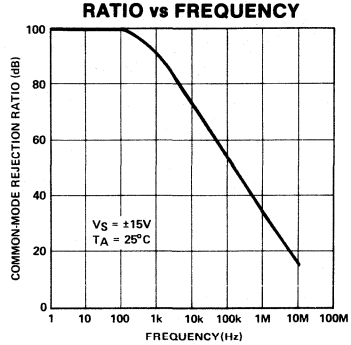
MAXIMUM OUTPUT SWING vs FREQUENCY



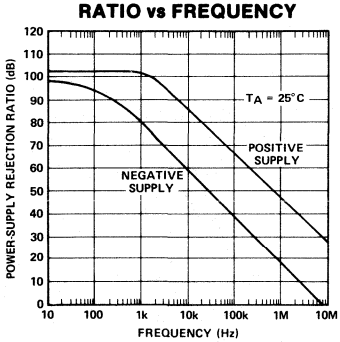
SLEW RATE vs TEMPERATURE



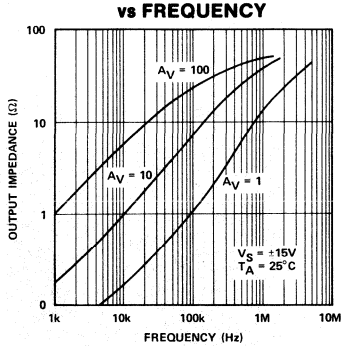
COMMON-MODE REJECTION RATIO vs FREQUENCY



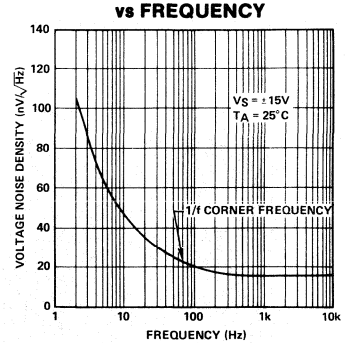
POWER-SUPPLY REJECTION RATIO vs FREQUENCY



OUTPUT IMPEDANCE vs FREQUENCY

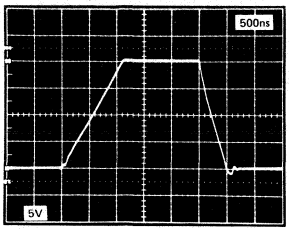


VOLTAGE NOISE DENSITY vs FREQUENCY

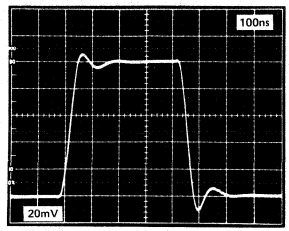


TYPICAL PERFORMANCE CHARACTERISTICS (OP-16)

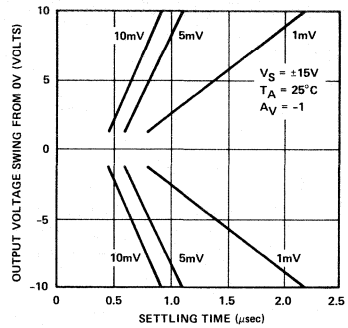
LARGE-SIGNAL TRANSIENT RESPONSE



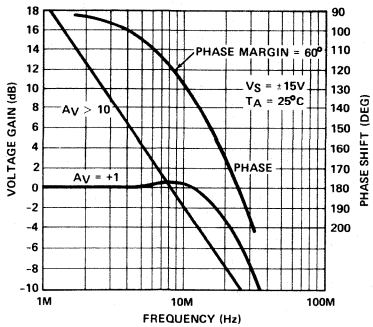
SMALL-SIGNAL TRANSIENT RESPONSE



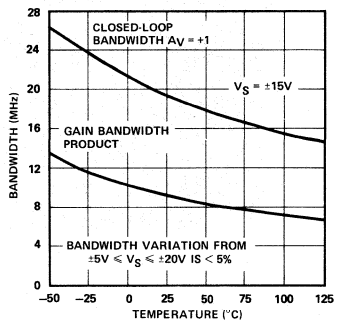
SETTLING TIME



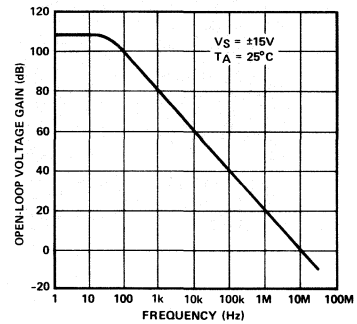
CLOSED-LOOP BANDWIDTH AND PHASE SHIFT vs FREQUENCY



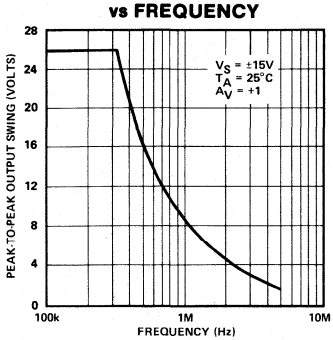
BANDWIDTH vs TEMPERATURE



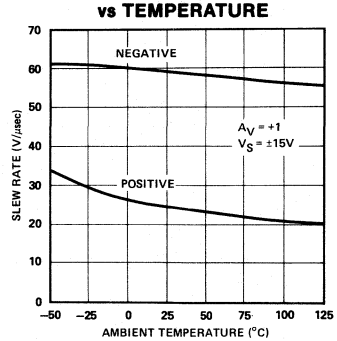
OPEN-LOOP GAIN vs FREQUENCY



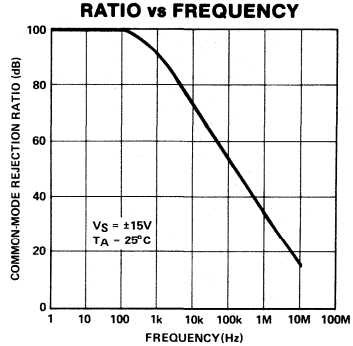
MAXIMUM OUTPUT SWING vs FREQUENCY



SLEW RATE vs TEMPERATURE

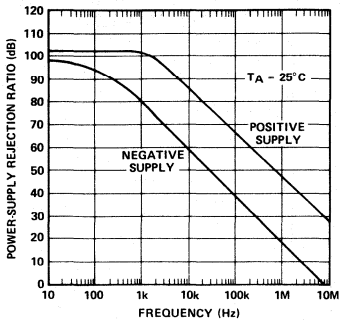


COMMON-MODE REJECTION RATIO vs FREQUENCY

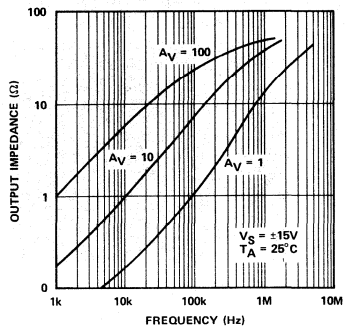


TYPICAL PERFORMANCE CHARACTERISTICS (OP-16)

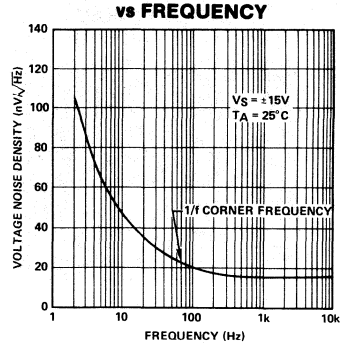
POWER-SUPPLY REJECTION RATIO vs FREQUENCY



OUTPUT IMPEDANCE vs FREQUENCY

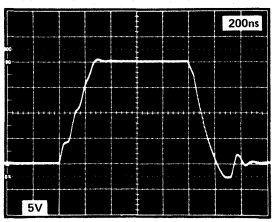


VOLTAGE NOISE DENSITY vs FREQUENCY

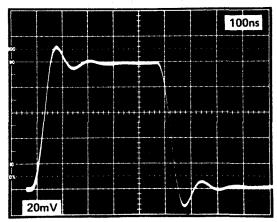


TYPICAL PERFORMANCE CHARACTERISTICS (OP-17)

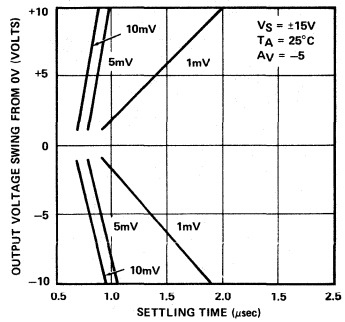
LARGE-SIGNAL TRANSIENT RESPONSE



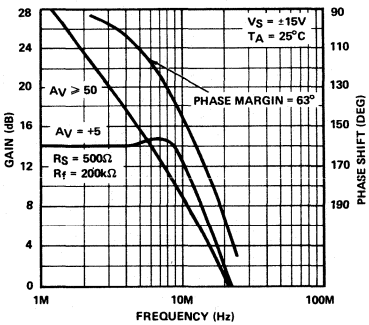
SMALL-SIGNAL TRANSIENT RESPONSE



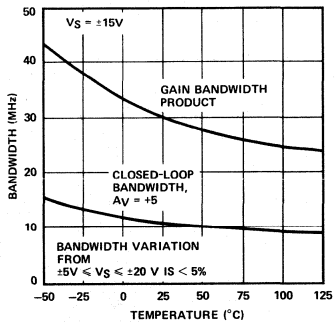
SETTLING TIME



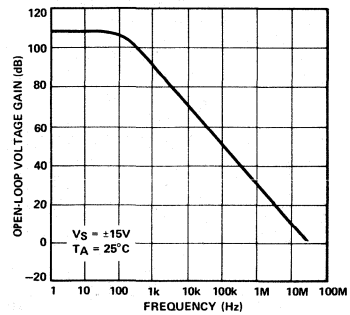
CLOSED-LOOP BANDWIDTH AND PHASE SHIFT vs FREQUENCY



BANDWIDTH vs TEMPERATURE

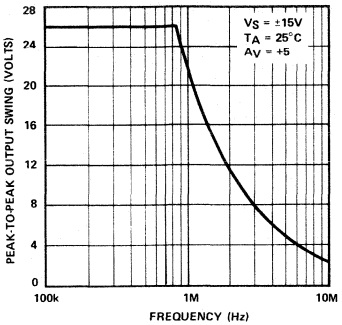


OPEN-LOOP FREQUENCY RESPONSE

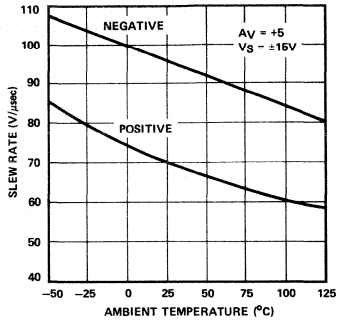


TYPICAL PERFORMANCE CHARACTERISTICS (OP-17)

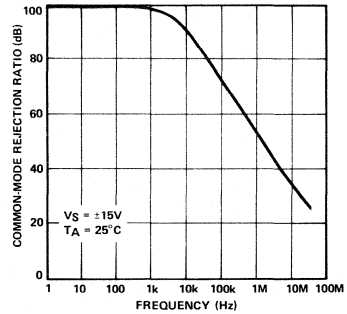
MAXIMUM OUTPUT SWING vs FREQUENCY



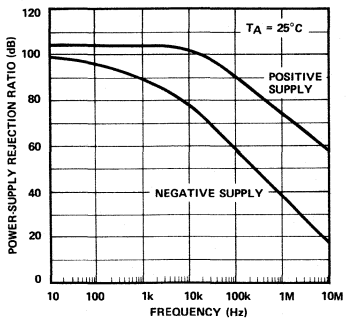
SLEW RATE vs TEMPERATURE



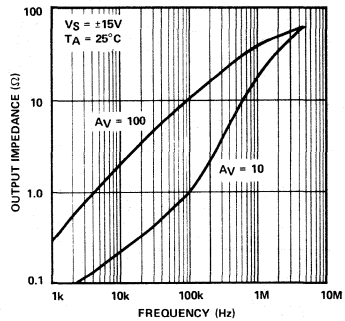
COMMON-MODE REJECTION RATIO vs FREQUENCY



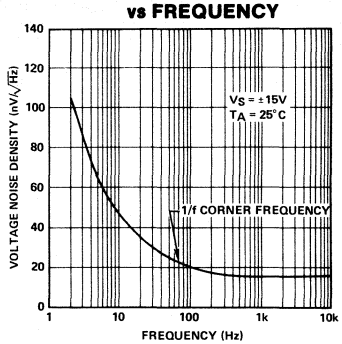
POWER-SUPPLY REJECTION RATIO vs FREQUENCY



OUTPUT IMPEDANCE vs FREQUENCY

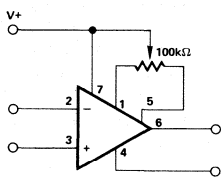


VOLTAGE NOISE vs FREQUENCY



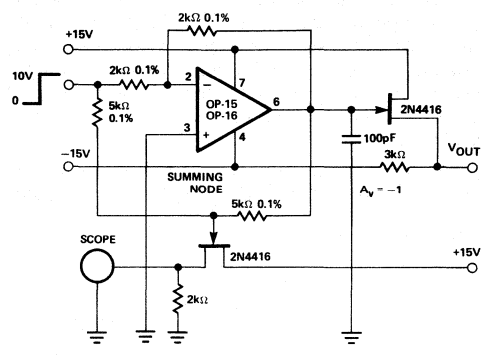
BASIC CONNECTIONS

INPUT OFFSET VOLTAGE NULLING

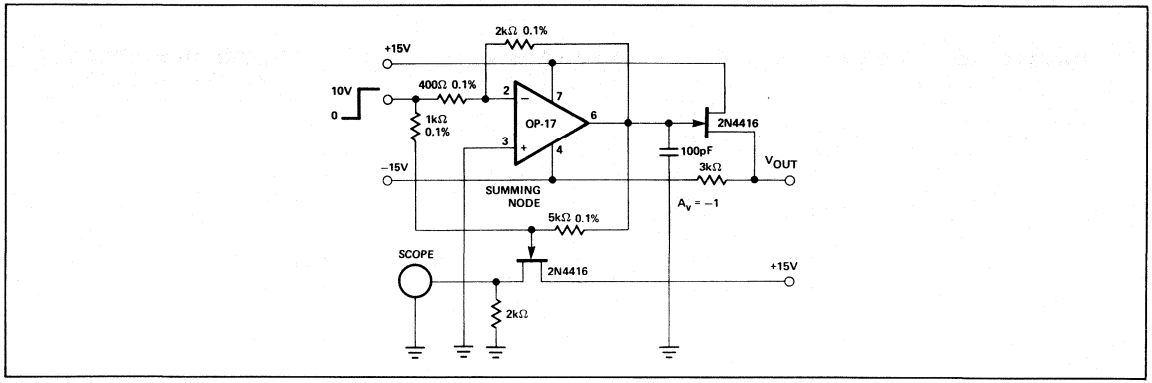


NOTE: V_{OS} CAN BE TRIMMED WITH POTENTIOMETERS RANGING FROM 10kΩ TO 1MΩ. FOR MOST UNITS TCV_{OS} WILL BE MINIMUM WHEN V_{OS} IS ADJUSTED WITH A 100kΩ POTENTIOMETER.

SETTLING-TIME TEST CIRCUIT — OP-15/OP-16

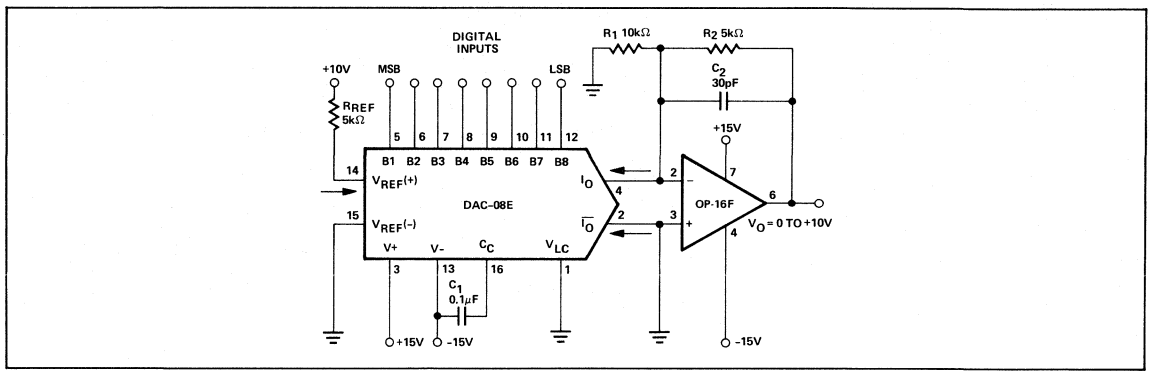


SETTLING-TIME TEST CIRCUIT — OP-17



TYPICAL APPLICATIONS

CURRENT-TO-VOLTAGE AMPLIFIER OUTPUT



APPLICATIONS INFORMATION

DYNAMIC OPERATING CONSIDERATIONS

As with most amplifiers, care should be taken with lead dress, component placement, and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3dB frequency of the closed-loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3dB frequency, a lead capacitor should be placed from the output to the negative input of the op amp. The value of the added capacitor should be such that the RC time-constant of this capacitor and the resistance it parallels is greater than, or equal to, the original feedback pole time constant.

ANALOG DEVICES

Micropower Operational Amplifier Single or Dual Supply

OP-20

FEATURES

- **Low Supply Current** ..... **55μA Max**
- **Single-Supply Operation** ..... **+5V to +30V**
- **Dual-Supply Operation** ..... **±2.5V to ±15V**
- **Low Input Offset Voltage** ..... **250μV Max**
- **Low Input Offset Voltage Drift** ..... **1.5μV/°C Max**
- **High Common-Mode Input Range** ... **V− to V+ (−1.5V)**
- **High CMRR and PSRR** ..... **100dB Min**
- **High Open-Loop Gain** ..... **120dB Min**
- **No External Components Required**
- **741 Pinout and Nulling**
- Available in Die Form

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (mV)	PACKAGE TO-99	PACKAGE CERDIP 8-PIN	PACKAGE PLASTIC 8-PIN	OPERATING TEMPERATURE RANGE
250	OP20BJ*	OP20BZ	–	MIL
250	OP20FJ	OP20FZ	–	IND
250	–	–	OP20FP	COM
500	–	OP20CZ	–	MIL
500	OP20GJ	OP20GZ	–	IND
500	–	–	OP20GP	COM
1000	OP20HJ	OP20HZ	OP20HS††	XIND
1000	–	–	OP20HP	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerDIP, plastic DIP, and TO-can packages.

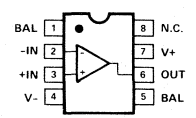
†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

The OP-20 is a monolithic micropower operational amplifier that can be operated from a single power supply of +5V to +30V, or from dual supplies of ±2.5V to ±15V. The input voltage range extends to the negative rail, therefore input signals down to zero volts can be accomodated when operating from a single supply.

Precision performance in high-gain applications is readily obtained when using the OP-20. The B/F grade features a maximum input offset voltage of 250μV, minimum CMRR of 95dB, and open-loop gain of over 500,000. Quiescent supply current is a maximum of only 55μA at ±2.5V or 80μA at ±15V. The low input offset, high gain, and low power consumption brings precision performance to portable instruments, satellites, missile control systems, and many other battery-powered applications.

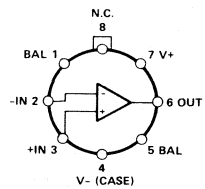
PIN CONNECTIONS



EPOXY MINI-DIP (P-Suffix)

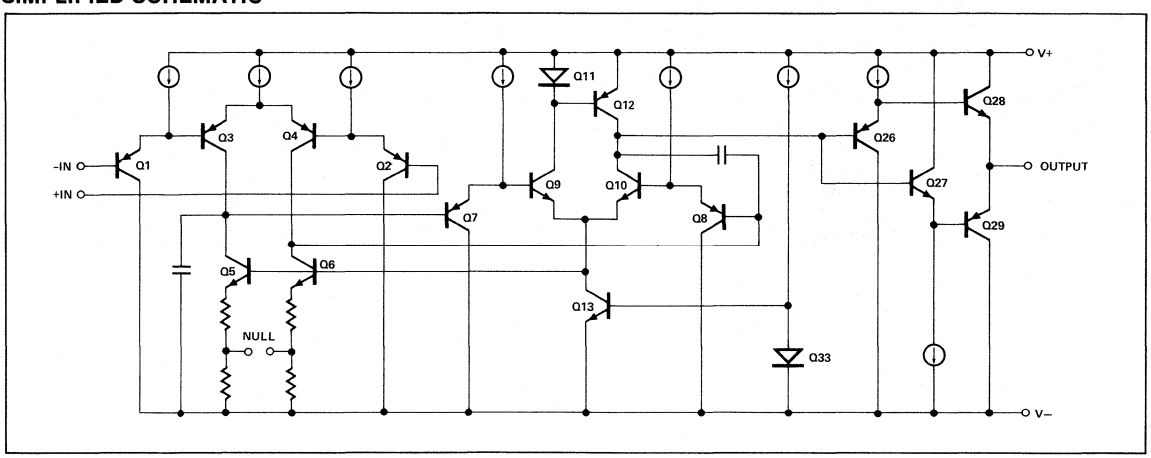
8-PIN HERMETIC DIP (Z-Suffix)

8-PIN SO (S-Suffix)



TO-99 (J-Suffix)

SIMPLIFIED SCHEMATIC



OP-20

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Differential Input Voltage ..... ±30V
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range
  J and Z Packages ..... –65°C to +150°C
  P Package ..... –65°C to +125°C
Operating Temperature Range
  OP-20B, OP-20C (J, Z) ..... –55°C to +125°C
  OP-20F, OP-20G (J, Z) ..... –25°C to +85°C
  OP-20H (S, P, J, Z) ..... –40°C to +85°C
  OP-20FP, OP-20GP ..... 0°C to +70°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature ..... –65°C to +150°C

PACKAGE TYPE	Θ_{JA} (NOTE 2)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $T_A = +25°C$, unless otherwise noted.

			OP-20B/F			OP-20C/G			OP-20H			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$V_S = \pm 15V$	—	55	250	—	150	500	—	300	1000	μV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	0.15	1.5	—	0.2	2.5	—	0.3	4.0	nA
Input Bias Current	I_B	$V_{CM} = 0$	—	12	25	—	14	30	—	16	40	nA
Input Voltage Range	IVR	V+ = +5V, V– = 0V	0/3.5	—	—	0/3.5	—	—	0/3.5	—	—	V
		$V_S = \pm 15V$	–15/13.5	—	—	–15/13.5	—	—	–15/13.5	—	—	
Common-Mode Rejection Ratio	CMRR	V+ = +5V, V– = 0V, $0V \le V_{CM} \le 3.5V$	95	105	—	90	95	—	85	90	—	dB
		$V_S = \pm 15V$, $-15V \le V_{CM} \le 13.5V$	100	110	—	94	105	—	90	100	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$, V– = 0V, V+ = 5V to 30V	—	4	6	—	6	10	—	10	32	μV/V
Large-Signal Voltage Gain	A_{VO}	V+ = +5V, V– = 0V, $1V \le V_O \le 3.5V$	300	500	—	200	500	—	—	500	—	V/mV
		$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 25k\Omega$	1000	2000	—	800	2000	—	500	1000	—	
Output Voltage Swing	V_O	V+ = 5V, V– = 0V, $R_L = 10k\Omega$	0.6/4.1	—	—	0.7/4.1	—	—	0.8/4.0	—	—	V
		$V_S = \pm 15V$, $R_L = 25k\Omega$	±14.1	—	—	±14.1	—	—	±14.0	—	—	
Closed-Loop Bandwidth	BW	$A_{VCL} = +1.0$, $R_L = 10k\Omega$	—	100	—	—	100	—	—	100	—	kHz
Slew Rate	SR	$V_S = \pm 15V$, $R_L = 25k\Omega$	—	0.05	—	—	0.05	—	—	0.05	—	V/μs
Supply Current	I_{SY}	$V_S = \pm 2.5V$, No Load	—	40	55	—	44	63	—	45	70	μA
		$V_S = \pm 15V$, No Load	—	55	80	—	57	85	—	60	95	

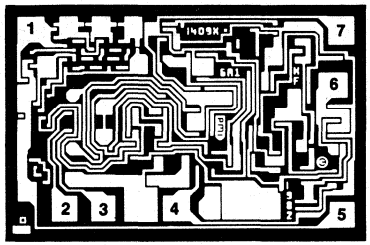
ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $-55°C \le T_A \le +125°C$ for OP-20BJ/BZ and OP-20CZ, $-25°C \le T_A \le +85°C$ for OP-20FJ/FZ and OP-20GJ/GZ, and $0°C \le T_A \le +70°C$ for OP-20FP, OP-20GP, and $-40°C \le T_A \le +85°C$ for OP-20HZ, OP-20HJ, and OP-20HP/HS, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-20B/F MIN	OP-20B/F TYP	OP-20B/F MAX	OP-20C/G MIN	OP-20C/G TYP	OP-20C/G MAX	OP-20H MIN	OP-20H TYP	OP-20H MAX	UNITS
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	Unnulled	—	0.75	1.5	—	1.0	3.0	—	1.5	7.0	µV/°C
Input Offset Voltage	V_{OS}	$V_S = \pm 15V$	—	155	400	—	250	800	—	500	1700	µV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	0.5	2.5	—	1.0	3.5	—	1.5	5.0	nA
Input Bias Current	I_B	$V_{CM} = 0$	—	12	27	—	14	33	—	16	45	nA
Input Voltage Range	IVR	V+ = +5V, V− = 0V	0/3.2	—	—	0/3.2	—	—	0/3.2	—	—	V
		$V_S = \pm 15V$	−15/13.2	—	—	−15/13.2	—	—	−15/13.2	—	—	
Common-Mode Rejection Ratio	CMRR	V+ = +5V, V− = 0V $0V \le V_{CM} \le 3.2V$	90	100	—	85	90	—	80	85	—	dB
		$V_S = \pm 15V$ $-15V \le V_{CM} \le 13.2V$	96	110	—	90	105	—	85	100	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$	—	4	10	—	6	18	—	10	32	µV/V
		V− = 0V, V+ = 5V to 30V	—	4	10	—	6	18	—	10	57	
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_O = \pm 10V$ $R_L = 50k\Omega$	500	700	—	400	600	—	250	400	—	V/mV
Output Voltage Swing	V_O	V+ = 5V, V− = 0V, $R_L = 50k\Omega$	0.8/4.0	—	—	0.9/3.9	—	—	1.0/3.8	—	—	V
		$V_S = \pm 15V$, $R_L = 50k\Omega$	±14.0	—	—	±13.9	—	—	±13.9	—	—	
Supply Current	I_{SY}	$V_S = \pm 2.5V$, No Load or +5V, 0V	—	50	65	—	53	75	—	55	85	µA
		$V_S = \pm 15V$, No Load	—	64	95	—	68	100	—	72	115	

NOTE:
1. Sample tested.

OP-20

DICE CHARACTERISTICS



DIE SIZE 0.069 x 0.047 inch, 3174 sq. mils
(1.75 x 1.17 mm, 2.05 sq. mm)

1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V−
5. BALANCE
6. OUTPUT
7. V+

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-20N LIMIT	OP-20G LIMIT	OP-20GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		300	600	1000	μV MAX
Input Offset Current	I_{OS}		1.5	2.5	4.0	nA MAX
Input Bias Current	I_B		25	30	40	nA MAX
Input Voltage Range	IVR	V+ = +5V, V− = 0V $V_S = \pm 15V$	0/3.5 −15/13.5	0/3.5 −15/13.5	0/3.5 −15/13.5	V MIN
Common-Mode Rejection Ratio	CMRR	V+ = +5V, V− = 0V, $0V \le V_{CM} \le +3.5V$ $V_S = \pm 15V$, $-15V \le V_{CM} \le \pm 13.5V$	95 100	90 94	85 90	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ V− = 0V, V+ = +5V to +30V	6	10	32	μV/V MAX
Large-Signal Voltage Gain	A_{VO}	$R_L = 25k\Omega$ $V_O = \pm 10V$	1000	800	500	V/mV MIN
Output Voltage Swing	V_O	$R_L = 10k\Omega$, V+ = +5V, V− = 0V $R_L = 25k\Omega$, $V_S = \pm 15V$	0.7/4.1 ±14.1	0.8/4.1 ±14.1	0.9/4.0 ±14.0	V MIN
Supply Current	I_{SY}	$V_S = \pm 2.5V$, No Load $V_S = \pm 15V$, No Load	55 80	63 85	70 95	μA MAX

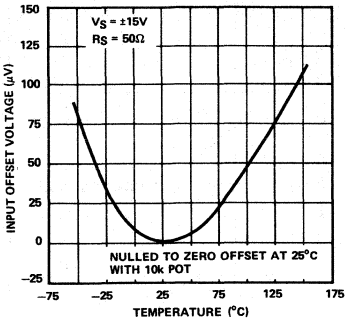
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

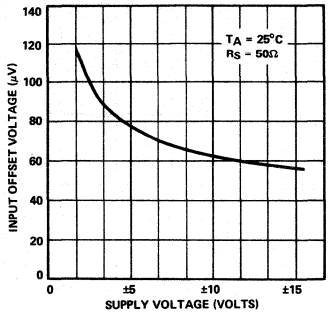
PARAMETER	SYMBOL	CONDITIONS	OP-20N TYPICAL	OP-20G TYPICAL	OP-20GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS} TCV_{OSn}	Unnulled Nulled, $R_P = 10k\Omega$	1.0 1.0	1.5 1.5	2.5 2.5	μV/°C
Large-Signal Voltage Gain	A_{VO}	$R_L = 25k\Omega$	2000	2000	1000	V/mV

TYPICAL PERFORMANCE CHARACTERISTICS

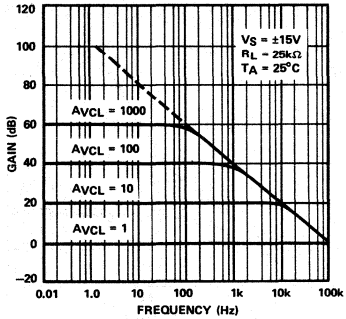
TRIMMED OFFSET VOLTAGE vs TEMPERATURE



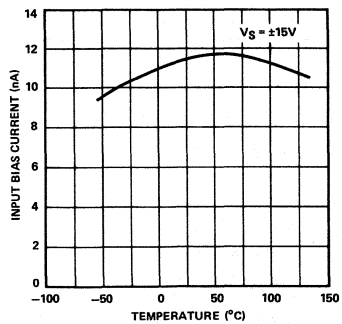
INPUT OFFSET VOLTAGE vs POWER SUPPLY VOLTAGE



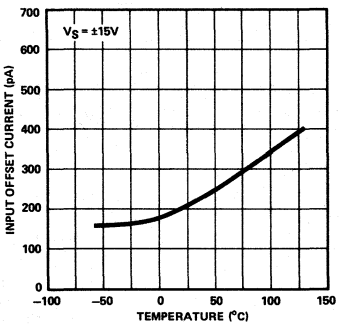
CLOSED-LOOP GAIN vs FREQUENCY



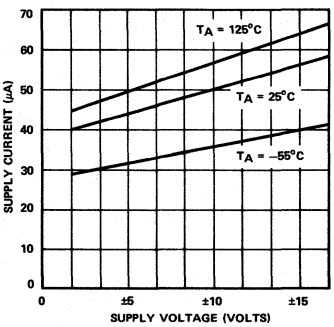
INPUT BIAS CURRENT vs TEMPERATURE



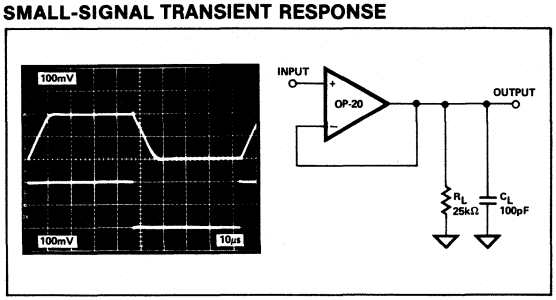
INPUT OFFSET CURRENT vs TEMPERATURE



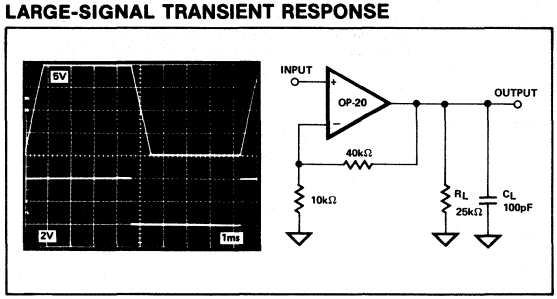
SUPPLY CURRENT vs SUPPLY VOLTAGE



SMALL-SIGNAL TRANSIENT RESPONSE



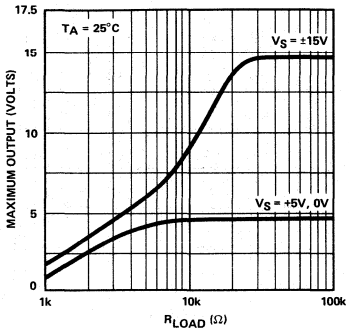
LARGE-SIGNAL TRANSIENT RESPONSE



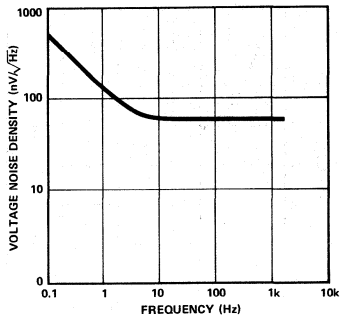
OP-20

TYPICAL PERFORMANCE CHARACTERISTICS

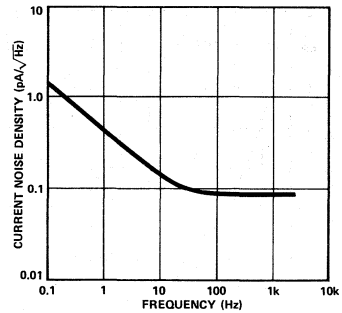
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



VOLTAGE NOISE DENSITY vs FREQUENCY

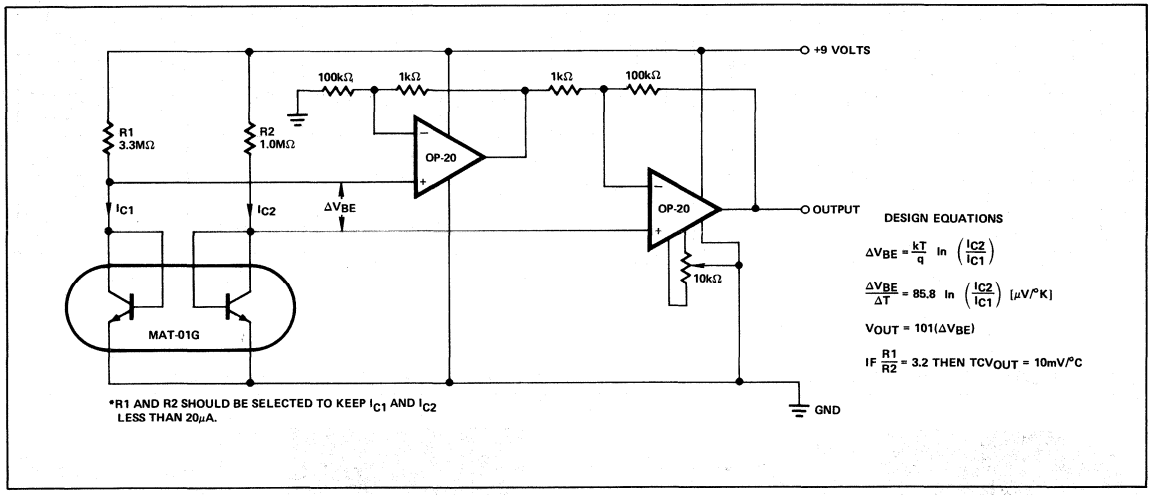


CURRENT NOISE DENSITY vs FREQUENCY



TYPICAL APPLICATIONS

TEMPERATURE SENSOR



ANALOG DEVICES

Low-Power Operational Amplifier Single or Dual Supply

OP-21

FEATURES

- **Low Supply Current** ..... **230μA Max**
- **Wide Supply Range** ..... **±2.5V to ±15V**
- **Low Input Offset Voltage** ..... **100μV Max**
- **Low Input Offset Voltage Drift** ..... **1.0μV/°C Max**
- **High Common-Mode Input Range** ..... **V− (+0.5V) to V+ (−1.5V)**
- **High CMRR and PSRR** ..... **100dB Min**
- **High Open-Loop Gain** ..... **1000V/mV Min**
- **125°C Temperature Tested Dice**

GENERAL DESCRIPTION

The OP-21 is a precision low-power operational amplifier offering the benefits of low offset voltage and high slew rate with the advantages of low power. A supply range of ±2.5V to ±15V allows a wide range of applications.

Two military temperature range models and three industrial temperature range models are available in TO-99 cans and 8-Pin hermetic DIPs. Industrial temperature range models are also available in 8-Pin epoxy DIPs. See OP-221 for dual and OP-421 for quad versions of the OP-21.

ORDERING INFORMATION †

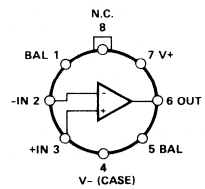
T_A = +25°C V_{OS} MAX (μV)	PACKAGE TO-99	PACKAGE CERDIP 8-PIN	PACKAGE PLASTIC 8-PIN	OPERATING TEMPERATURE RANGE
100	OP21AJ	OP21AZ*	–	MIL
100	–	OP21EZ	–	IND
200	OP21FJ	OP21FZ	OP21FP	IND
500	OP21GJ	–	OP21GP	XIND
500	–	–	OP21HS††	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

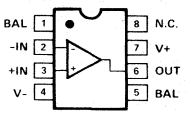
† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

PIN CONNECTIONS



TO-99
(J-Suffix)

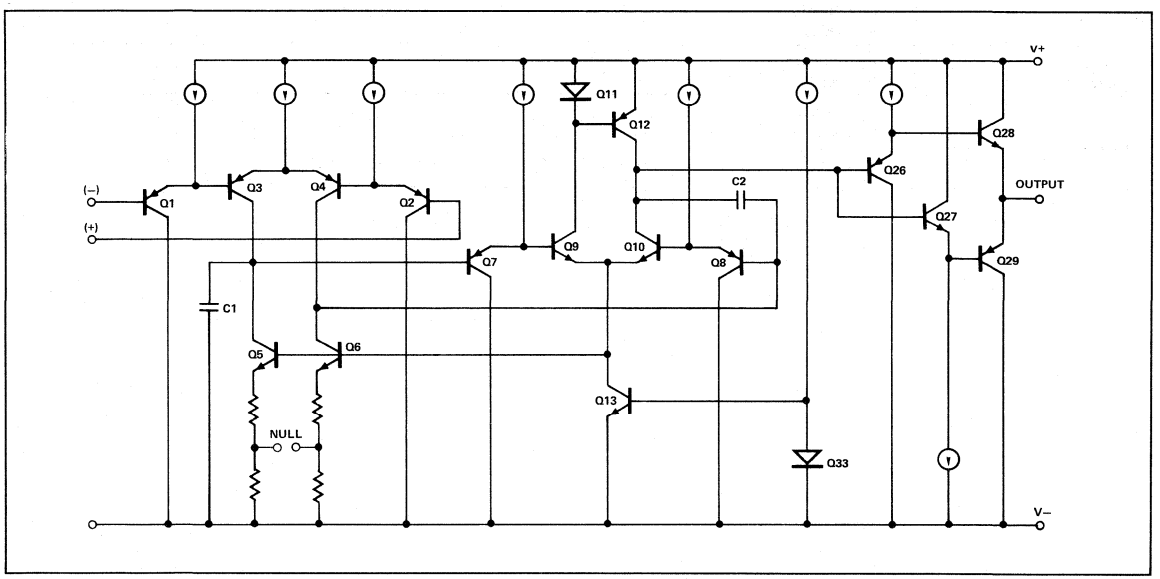


EPOXY MINI-DIP
(P-Suffix)

8-PIN HERMETIC DIP
(Z-Suffix)

8-PIN SO
(S-Suffix)

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage ..... ±18V
Differential Input Voltage ..... ±30V
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range
J and Z Packages ..... –65°C to +125°C
P Package ..... –65°C to +125°C
Operating Temperature Range
OP-21A ..... –55°C to +125°C
OP-21E, OP-21F ..... –25°C to +85°C
OP-21HS, OP-21G ..... –40°C to +85°C
Junction Temperature (T_J) ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.
2. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$ and $T_A = +25°C$, unless otherwise noted.

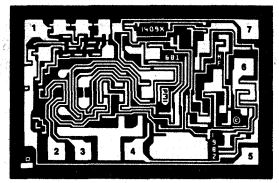
			OP-21A/E			OP-21F			OP-21G/H			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$V_S = \pm 15V$	—	40	100	—	150	200	—	300	500	µV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	0.6	4	—	0.8	5	—	1.2	6	nA
Input Bias Current	I_B	$V_{CM} = 0$	—	50	100	—	60	120	—	70	150	nA
Input Voltage Range	IVR	$V_S = \pm 15V$	−14.5/13.5	—	—	−14.5/13.5	—	—	−14.5/13.5	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_S = \pm 15V$, No Load $-14.5V \le V_{CM} \le 13.5V$	100	110	—	90	105	—	84	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$, No Load	—	2	6	—	4	10	—	10	32	µV/V
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 10k\Omega$, $V_O \pm 10V$	1000	2000	—	500	1500	—	500	1000	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm 15V$, $R_L = 10k\Omega$	−13.7/14.0	—	—	−13.7/13.9	—	—	−13.6/13.8	—	—	V
Slew Rate	SR	$C_L = 100pF$, $R_L = 25k\Omega$	—	0.25	—	—	0.25	—	—	0.25	—	V/µs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$, $R_L = 10k\Omega$	—	600	—	—	600	—	—	600	—	kHz
Supply Current	I_{SY}	$V_S = \pm 2.5V$, No Load	—	170	230	—	180	275	—	190	300	µA
		$V_S = \pm 15V$, No Load	—	230	300	—	235	360	—	250	420	

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $-55°C \le T_A \le +125°C$ for OP-21A, $-25°C \le T_A \le +85°C$ for OP-21E and OP-21F, $-40°C \le T_A \le +85°C$ for OP-21G and OP-21H, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-21A/E MIN	OP-21A/E TYP	OP-21A/E MAX	OP-21F MIN	OP-21F TYP	OP-21F MAX	OP-21G/H MIN	OP-21G/H TYP	OP-21G/H MAX	UNITS
Average Input Offset Voltage Drift (Notes 1, 2)	TCV_{OS} TCV_{OSn}	Unnulled Nulled	—	0.5	1.0	—	1.0	2.0	—	2.5	5.0	μV/°C
Input Offset Voltage	V_{OS}		—	75	200	—	200	500	—	500	1000	μV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	0.7	5	—	0.7	6	—	0.8	8	nA
Input Bias Current	I_B	$V_{CM} = 0$	—	50	110	—	60	130	—	70	165	nA
Input Voltage Range	IVR		−14.3/13.2	—	—	−14.3/13.2	—	—	−14.3/13.2	—	—	V
Common-Mode Rejection Ratio	CMRR	No Load, $V_S = \pm 15V$, $-14.5V \le V_{CM} \le 13.2V$	96	105	—	86	100	—	80	95	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$, No Load	—	4	10	—	6	18	—	18	57	μV/V
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 20k\Omega$, $V_O = \pm 10V$	500	1500	—	250	1300	—	250	1000	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm 15V$, $R_L = 20k\Omega$	−13.5/13.8	—	—	−13.5/13.7	—	—	−13.5/13.6	—	—	V
Supply Current	I_{SY}	$V_S = \pm 2.5V$, No Load	—	205	275	—	215	330	—	230	360	μA
		$V_S = \pm 15V$, No Load	—	275	360	—	285	430	—	300	500	

NOTES:
1. Sample tested.
2. TCV_{OSn} is guaranteed by unnulled TCV_{OS} and device design.

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



DIE SIZE 0.069 × 0.046 inch, 3174 sq. mils
(1.75 × 1.17 mm, 2.05 sq. mm)

1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V−
5. BALANCE
6. OUTPUT
7. V+

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C for OP-21N and OP-21G devices; T_A = +125°C for OP-21NT and OP-21GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-21NT LIMIT	OP-21N LIMIT	OP-21GT LIMIT	OP-21G LIMIT	UNITS
Input Offset Voltage	V_{OS}		200	100	500	200	μV MAX
Input Offset Current	I_{OS}	V_{CM} = 0	4	4	5	5	nA MAX
Input Bias Current	I_B	V_{CM} = 0	100	100	120	120	nA MAX
Input Voltage Range	IVR		−14.3 +13.5	−14.5 +13.5	−14.3 +13.5	−14.5 +13.5	V MIN
Common-Mode Rejection Ratio	CMRR	No Load CMVR = IVR	96	100	86	90	dB MIN
Power Supply Rejection Ratio	PSRR	V_S = ±2.5V to ±15V No Load	10	6	18	10	μV/V MAX
Large-Signal Voltage Gain	A_{VO}	R_L = 10kΩ, V_O = ±10V	500	1000	250	500	V/mV MIN
Output Voltage Swing	V_O	R_L = 10kΩ	−13.5 +13.8	−13.7 +14.0	−13.5 +13.8	−13.7 +13.9	V MIN
Supply Current	I_{SY}	No Load	300	300	360	360	μA MAX

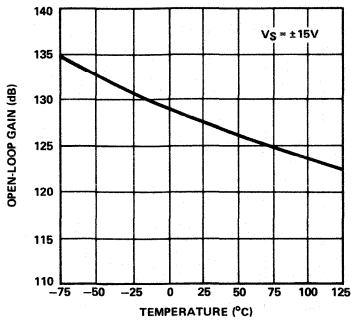
NOTES:
For 25° C characteristics of NT & GT devices, see N & G characteristics respectively.
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25° C, unless otherwise noted.

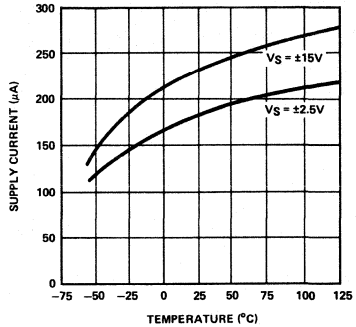
PARAMETER	SYMBOL	CONDITIONS	OP-21NT TYPICAL	OP-21N TYPICAL	OP-21GT TYPICAL	OP-21G TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	Unnulled	0.5	0.5	1	1	μV/° C
Nulled Input Offset Voltage Drift	TCV_{OSn}	Nulled, R_p = 10kΩ	0.5	0.5	1	1	μV/° C
Large-Signal Voltage Gain	A_{VO}	R_L = 10kΩ	2000	2000	1500	1500	V/mV
Slew Rate	SR	R_L = 25kΩ C_L = 100pF	0.25	0.25	0.25	0.25	V/μs
Closed-Loop Bandwidth	BW	A_{VCL} = +1 R_L = 10kΩ	600	600	600	600	kHz

TYPICAL PERFORMANCE CHARACTERISTICS

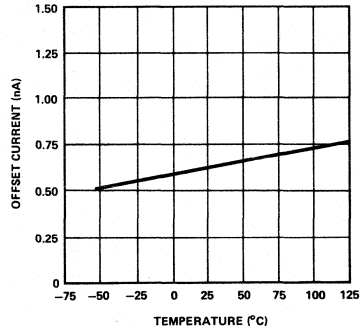
OPEN-LOOP GAIN vs TEMPERATURE



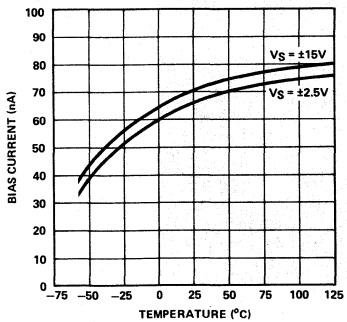
SUPPLY CURRENT vs TEMPERATURE



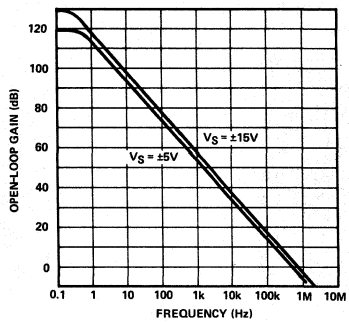
OFFSET CURRENT vs TEMPERATURE



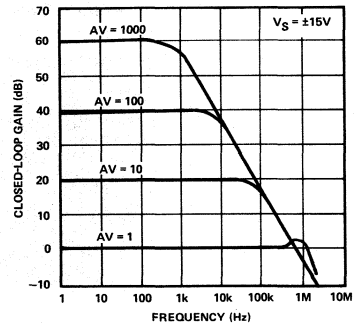
BIAS CURRENT vs TEMPERATURE



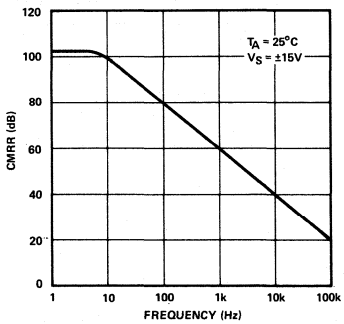
OPEN-LOOP GAIN vs FREQUENCY



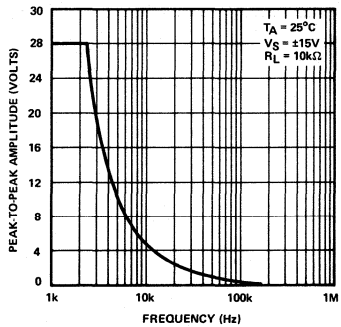
CLOSED-LOOP GAIN vs FREQUENCY



CMRR vs FREQUENCY

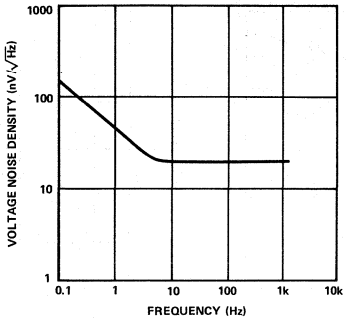


MAXIMUM OUTPUT SWING vs FREQUENCY

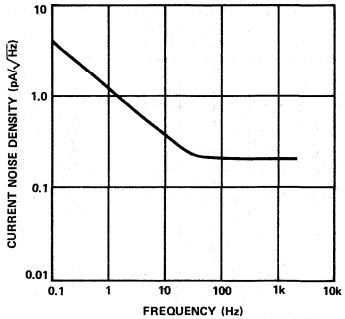


TYPICAL PERFORMANCE CHARACTERISTICS

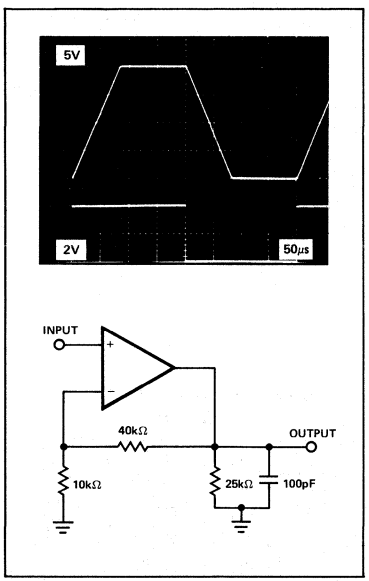
VOLTAGE NOISE DENSITY vs FREQUENCY



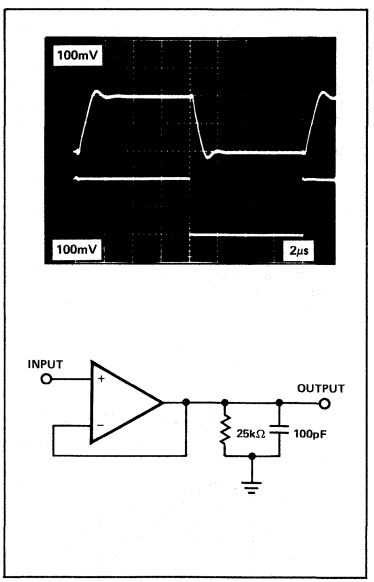
CURRENT NOISE DENSITY vs FREQUENCY



NONINVERTING LARGE-SIGNAL RESPONSE



NONINVERTING SMALL-SIGNAL RESPONSE



ANALOG DEVICES

Programmable Micropower Operational Amplifier

OP-22

FEATURES

- Programmable Supply Current ..... 500nA to 400μA
- Single Supply Operation ..... +3V to +30V
- Dual Supply Operation ..... ±1.5V to ±15V
- Low Input Offset Voltage 100μV
- Low Input Offset Voltage Drift ..... 0.75μV/°C
- High Common-Mode Input Range ..... V– to V+ (–1.5V)
- High CMRR and PSRR 115dB
- High Open-Loop Gain 1800V/mV
- ±30V Input Overvoltage Protection
- Unity-Gain Stable
- LM4250 Pinout and Nulling
- Available in Die Form

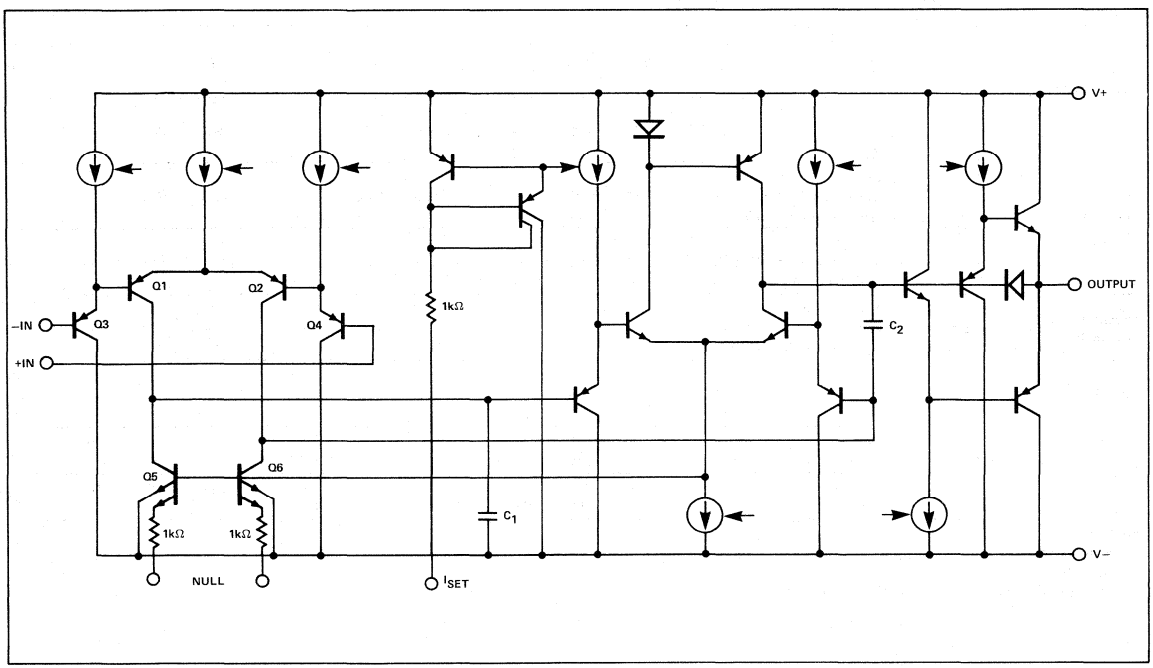
GENERAL DESCRIPTION

The OP-22 is a monolithic micropower operational amplifier designed to provide excellent accuracy in high-gain applications. Offsets are very low which generally eliminates any need for external nulling of V_{OS}. The OP-22 is internally compensated and unity-gain stable. It also features high open-loop gain, CMRR, and PSRR. This assures good gain accuracy and rejection of power supply variations even when used in circuits with high closed-loop gain. The low offsets and high gain accuracy of the OP-22 bring precision performance to the micropower field.

The OP-22 is a versatile op amp designed for operation from battery or solar-cell power sources. Supply current is programmable over a range of 500nA to 400μA with a single external resistor. Input voltage range is very wide and extends down to the negative rail, thus the common-mode input voltage range includes ground when operating from a single supply voltage. This ability to provide high DC performance over a wide input range is particularly useful in single-battery applications. In addition, the OP-22 is characterized over a wide supply range of ±1.5V to ±15V, or +3V to +30V for single supply.

The OP-22 pin-out and offset nulling are identical to the LM4250 and many other micropower operational amplifiers. This functional commonality allows easy upgrading of system performance. By selection of set resistor value, the circuit designer can readily use the OP-22 in place of such amplifiers as the LM108, LM112, LM4250, μA776, and ICL8021 in high-gain, low-frequency applications.

SIMPLIFIED SCHEMATIC



OP-22

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Differential Input Voltage ..... ±30V
Input Voltage ..... Supply Voltage
Storage Temperature Range
J and Z Packages ..... –65°C to +150°C
Operating Temperature Range
OP-22A ..... –55°C to +125°C
OP-22E, OP-22F ..... –25°C to +85°C
OP-22H ..... –40°C to +85°C
Lead Temperature Range (Soldering, 60 sec) ..... +300°C
Junction Temperature ..... –65°C to +150°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5V$ to $\pm 15V$, $1\mu A \le I_{SET} \le 10\mu A$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-22A/E MIN	OP-22A/E TYP	OP-22A/E MAX	OP-22F MIN	OP-22F TYP	OP-22F MAX	OP-22H MIN	OP-22H TYP	OP-22H MAX	UNITS
Input Offset Voltage	V_{OS}		—	100	300	—	200	500	—	400	1000	µV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	0.2	1	—	0.3	2	—	0.5	3	nA
Input Bias Current	I_B	$I_{SET} = 1\mu A$, $V_{CM} = 0$	—	2.6	5	—	3.0	7.5	—	4.0	10	nA
		$I_{SET} = 10\mu A$, $V_{CM} = 0$	—	19	30	—	24	35	—	30	50	
Input Voltage Range	IVR	V+ = +5V, V− = 0V.	0/3.5	—	—	0/3.5	—	—	0/3.5	—	—	V
		$V_S = \pm 15V$	−15/+13.5	—	—	−15/+13.5	—	—	−15/+13.5	—	—	
Common-Mode Rejection Ratio	CMRR (Note 2)	$V_S = \pm 15V$, $-15V \le V_{CM} \le +13.5V$	100	115	—	95	105	—	85	95	—	dB
Power Supply Rejection Ratio (Note 1)	PSRR (Note 2)	$V_S = \pm 1.5V$ to $\pm 15V$; and V− = 0V, V+ = 3V to 30V.	—	1.8	6	—	6	18	—	10	32	µV/V
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $I_{SET} = 1\mu A$, $R_L = 100k\Omega$.	1000	1800	—	500	900	—	250	500	—	V/mV
		$V_S = \pm 15V$, $I_{SET} = 10\mu A$, $R_L = 10k\Omega$.	1000	1800	—	500	900	—	300	500	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm 1.5V$, $I_{SET} = 1\mu A$, $R_L = 100k\Omega$ & $I_{SET} = 10\mu A$, $R_L = 10k\Omega$.	±0.8	±0.82	—	±0.8	±0.82	—	±0.75	±0.8	—	V
		$V_S = \pm 15V$, $I_{SET} = 1\mu A$, $R_L = 100k\Omega$ & $I_{SET} = 10\mu A$, $R_L = 10k\Omega$.	±14	±14.2	—	±14	±14.2	—	±13.5	±14	—	V
Closed-Loop Bandwidth	BW	$A_{VCL} = +1.0$, $V_S = \pm 15V$, $I_{SET} = 10\mu A$, $R_L = 10k\Omega$.	—	250	—	—	250	—	—	250	—	kHz
Slew Rate	SR	$V_S = \pm 15V$, $I_{SET} = 10\mu A$, $R_L = 10k\Omega$.	—	0.08	—	—	0.08	—	—	0.08	—	V/µs
Supply Current No Load	I_{SY}	$V_S = \pm 15V$, $I_{SET} = 1\mu A$.	—	15	17	—	16	19	—	18	21	µA
		$V_S = \pm 15V$, $I_{SET} = 10\mu A$.	—	150	170	—	160	190	—	180	210	
		$V_S = \pm 1.5V$, $I_{SET} = 1\mu A$.	—	10.5	12.5	—	14	16	—	17	20	µA
		$V_S = \pm 1.5V$, $I_{SET} = 10\mu A$.	—	105	125	—	140	160	—	170	200	

NOTES:
1. Sample tested for single-supply operation, 100% tested for dual-supply operation.
2. Measured with V_{OS} unnulled and I_{SET} constant.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5V$ to $\pm 15V$, $1\mu A \le I_{SET} \le 10\mu A$, $-55°C \le T_A \le +125°C$ for OP-22A, $-25°C \le T_A \le +85°C$ for OP-22E/F, and $-40°C \le T_A \le +85°C$ for OP-22H, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-22A/E MIN	OP-22A/E TYP	OP-22A/E MAX	OP-22F MIN	OP-22F TYP	OP-22F MAX	OP-22H MIN	OP-22H TYP	OP-22H MAX	UNITS
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	Unnulled	—	0.75	1.5	—	1.0	2.0	—	1.5	3.0	μV/°C
Input Offset Voltage	V_{OS}		—	175	400	—	350	600	—	500	1200	μV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	0.2	1	—	0.3	2	—	0.5	3	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 1)	—	2	10	—	3	15	—	5	25	pA/°C
Input Bias Current	I_B	$I_{SET} = 1\mu A$, $V_{CM} = 0$	—	2.8	5	—	3.3	7.5	—	4.5	10	nA
		$I_{SET} = 10\mu A$, $V_{CM} = 0$	—	21	30	—	27	35	—	34	50	
Input Voltage Range	IVR	$V+ = +5V$, $V- = 0V$	0/3.2	—	—	0/3.2	—	—	0/3.2	—	—	V
		$V_S = \pm 15V$	−15/+13.2	—	—	−15/+13.2	—	—	−15/+13.2	—	—	
Common-Mode Rejection Ratio	CMRR (Note 3)	$V_S = \pm 15V$, $-15V \le V_{CM} \le +13.2V$										dB
		$I_{SET} = 1\mu A$	80	105	—	80	99	—	80	90	—	
		$I_{SET} = 10\mu A$	90	115	—	86	105	—	80	90	—	
Power Supply Rejection Ratio	PSRR (Note 3)	$V_S = \pm 1.5V$ to $\pm 15V$ & $V- = 0V$, $V+ = 3V$ to $30V$ (Note 2)	—	3.2	10	—	10	32	—	32	56	μV/V
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $I_{SET} = 1\mu A$, $R_L = 100k\Omega$.	200	400	—	200	400	—	100	250	—	V/mV
		$V_S = \pm 15V$, $I_{SET} = 10\mu A$, $R_L = 10k\Omega$.	500	1000	—	300	750	—	150	300	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm 1.5V$, $I_{SET} = 1\mu A$, $R_L = 100k\Omega$ & $I_{SET} = 10\mu A$, $R_L = 10k\Omega$.	±0.65	±0.75	—	±0.65	±0.75	—	±0.6	±0.7	—	V
		$V_S = \pm 15V$, $I_{SET} = 1\mu A$, $R_L = 100k\Omega$ & $I_{SET} = 10\mu A$, $R_L = 10k\Omega$.	±13.6	±13.8	—	±13.6	±13.8	—	±13.0	±13.5	—	V
Supply Current No Load	I_{SY}	$V_S = \pm 15V$, $I_{SET} = 1\mu A$.	—	16	18	—	17	20	—	20	25	μA
		$V_S = \pm 15V$, $I_{SET} = 10\mu A$.	—	160	180	—	170	200	—	200	250	
		$V_S = \pm 1.5V$, $I_{SET} = 1\mu A$.	—	12	14	—	15	18	—	19	25	μA
		$V_S = \pm 1.5V$, $I_{SET} = 10\mu A$.	—	120	140	—	150	180	—	190	250	

NOTES:
1. Sample tested.
2. $V_{CM} = 1.5V$
3. Measured with V_{OS} unnulled and I_{SET} constant.

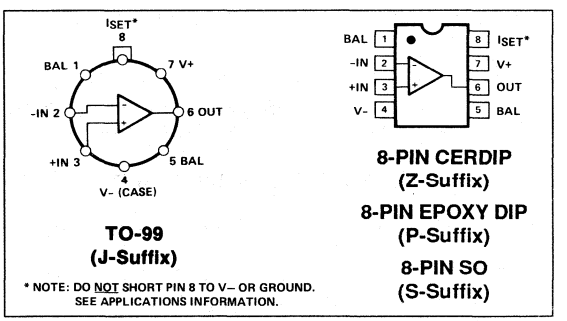
ORDERING INFORMATION †

$T_A = +25°C$ V_{OS} MAX (μV)	PACKAGE TO-99	PACKAGE CERDIP 8-PIN	PACKAGE PLASTIC 8-PIN	OPERATING TEMPERATURE RANGE
300	OP22AJ/883	OP22AZ*	–	MIL
300	–	OP22EZ	–	IND
500	–	OP22FZ	–	IND
1000	–	OP22HZ	OP22HP	XIND
1000	–	–	OP22HS	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

PIN CONNECTIONS



TO-99 (J-Suffix)

* NOTE: DO NOT SHORT PIN 8 TO V– OR GROUND. SEE APPLICATIONS INFORMATION.

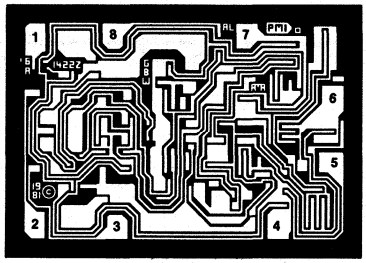
8-PIN CERDIP (Z-Suffix)

8-PIN EPOXY DIP (P-Suffix)

8-PIN SO (S-Suffix)

OP-22

DICE CHARACTERISTICS



DIE SIZE 0.070 × 0.050 inch, 3500 sq. mils
(1.78 × 1.27 mm, 2.26 sq. mm)

1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V–
5. BALANCE
6. OUTPUT
7. V+
8. I_{SET}

WAFER TEST LIMITS at $V_S = \pm 1.5V$ to $\pm 15V$, $1\mu A \leq I_{SET} \leq 10\mu A$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-22N LIMIT	OP-22G LIMIT	OP-22GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		300	500	1000	μV MAX
Input Offset Current	I_{OS}	(Note 1)	1	2	3	nA MAX
Input Bias Current	I_B	$I_{SET} = 1\mu A$ (Note 1) $I_{SET} = 10\mu A$	5 30	7.5 35	10 50	nA MAX
Input Voltage Range	IVR	V+ = +5V, V– = 0V $V_S = \pm 15V$	0/3.5 –15/+13.5	0/3.5 –15/+13.5	0/3.5 –15/+13.5	V MIN
Common-Mode Rejection Ratio	CMRR	$V_S = \pm 15V$, $-15V \leq V_{CM} \leq +13.5V$ (Note 2)	100	95	85	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 1.5V$ to $\pm 15V$ V– = 0V, V+ = 3V to 30V (Note 2)	6	18	32	μV/V MIN
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $I_{SET} = 1\mu A$, $R_L = 100k\Omega$.	1000	500	250	V/mV MIN
		$V_S = \pm 15V$, $I_{SET} = 10\mu A$, $R_L = 10k\Omega$.	1000	500	300	V/mV MIN
Output Voltage Swing	V_O	$V_S = \pm 1.5V$, $I_{SET} = 1\mu A$, $R_L = 100k\Omega$ & $I_{SET} = 10\mu A$, $R_L = 10k\Omega$.	±0.8	±0.8	±0.75	V MIN
		$V_S = \pm 15V$, $I_{SET} = 1\mu A$, $R_L = 100k\Omega$ & $I_{SET} = 10\mu A$, $R_L = 10k\Omega$.	±14	±14	±13.5	V MIN
Supply Current No Load	I_{SY}	$V_S = \pm 15V$, $I_{SET} = 1\mu A$. $V_S = \pm 15V$, $I_{SET} = 10\mu A$.	17 170	19 190	21 210	μA MAX
		$V_S = \pm 1.5V$, $I_{SET} = 1\mu A$. $V_S = \pm 1.5V$, $I_{SET} = 10\mu A$.	12.5 125	16 160	20 200	μA MAX

NOTES:
1. $V_{CM} = 0$
2. Measured with V_{OS} unnulled and I_{SET} held constant.

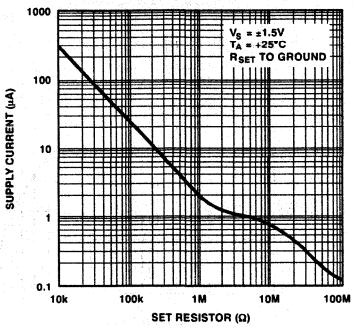
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5V$ to $\pm 15V$, $1\mu A \leq I_{SET} \leq 10\mu A$, $T_A = +25°C$, unless otherwise noted.

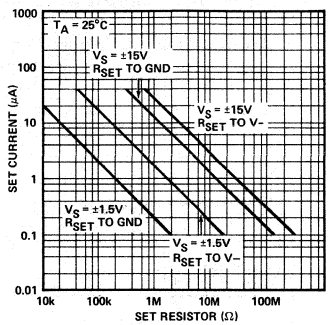
PARAMETER	SYMBOL	CONDITIONS	OP-22N TYPICAL	OP-22G TYPICAL	OP-22GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	Unnulled	1.0	1.5	2.5	μV/°C
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$ $I_{SET} = 1\mu A$, $R_L = 100k\Omega$ & $I_{SET} = 10\mu A$, $R_L = 10k\Omega$	1800	900	500	V/mV

TYPICAL PERFORMANCE CHARACTERISTICS

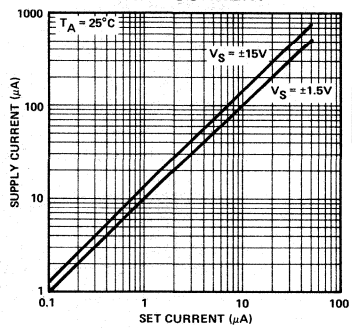
SUPPLY CURRENT vs SET RESISTOR



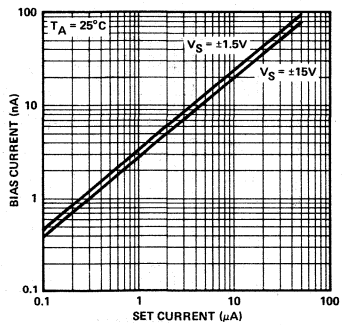
SET CURRENT vs SET RESISTOR



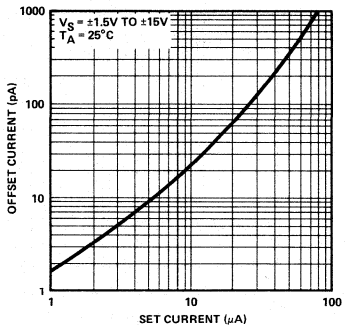
SUPPLY CURRENT vs SET CURRENT



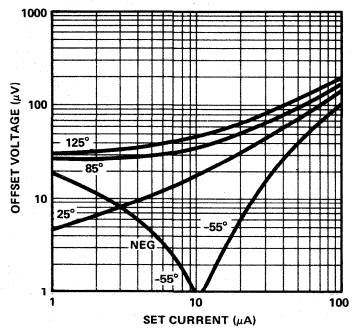
BIAS CURRENT vs SET CURRENT



OFFSET CURRENT vs SET CURRENT



OFFSET VOLTAGE vs SET CURRENT



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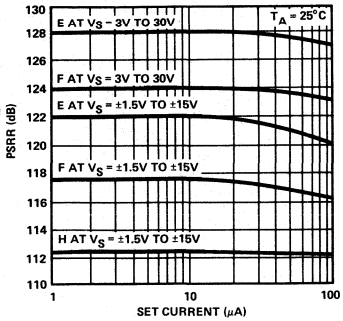
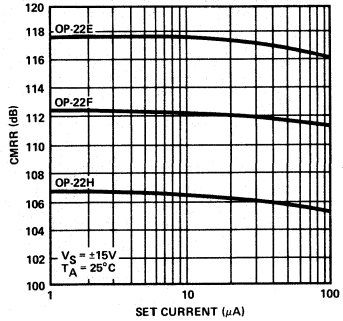
TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

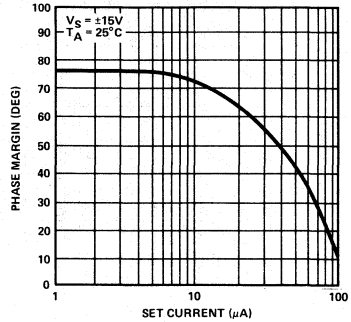
POWER SUPPLY REJECTION vs SET CURRENT



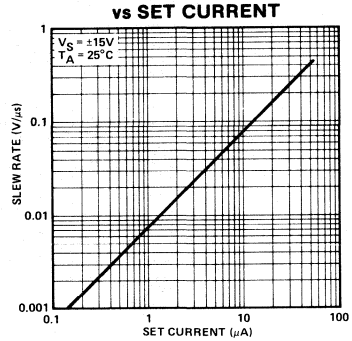
COMMON-MODE REJECTION vs SET CURRENT



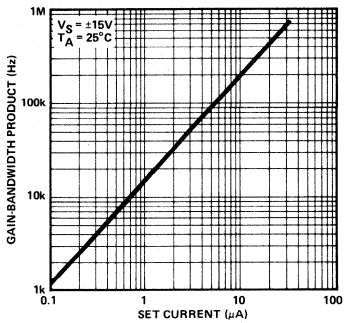
PHASE MARGIN vs SET CURRENT



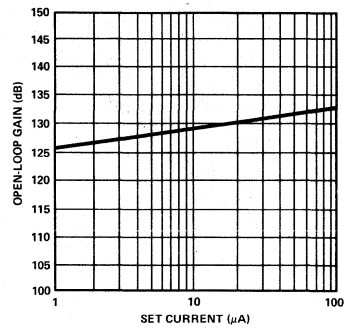
SLEW RATE vs SET CURRENT



GAIN-BANDWIDTH PRODUCT vs SET CURRENT

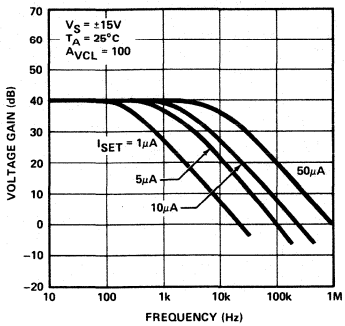


OPEN-LOOP GAIN vs SET CURRENT

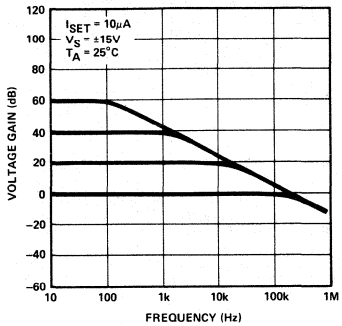


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

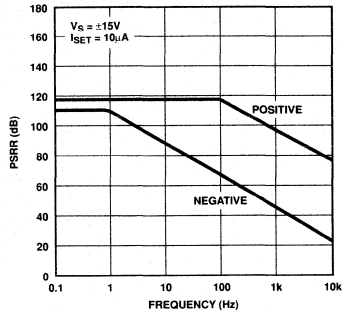
FREQUENCY RESPONSE vs SET CURRENT



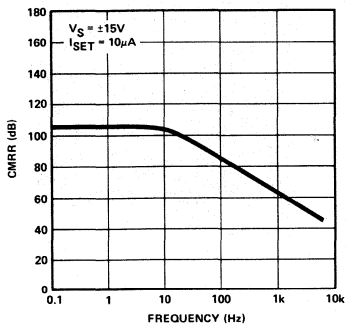
CLOSED-LOOP FREQUENCY RESPONSE



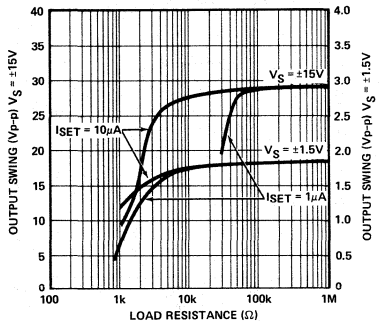
POWER SUPPLY REJECTION vs FREQUENCY



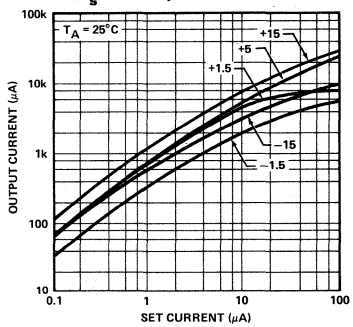
COMMON-MODE REJECTION vs FREQUENCY



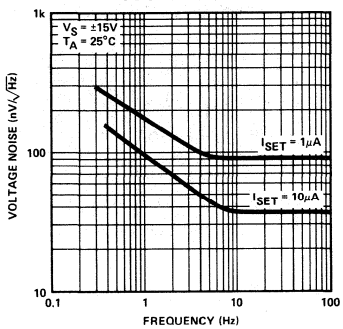
PEAK-TO-PEAK OUTPUT SWING vs LOAD RESISTANCE



MAXIMUM OUTPUT CURRENT vs SET CURRENT AT V_s = ±15V, +5V and ±1.5V

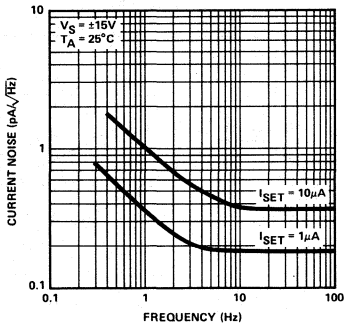


VOLTAGE NOISE vs FREQUENCY

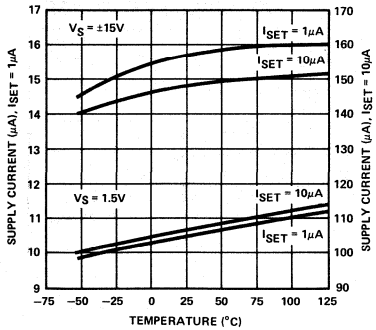


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

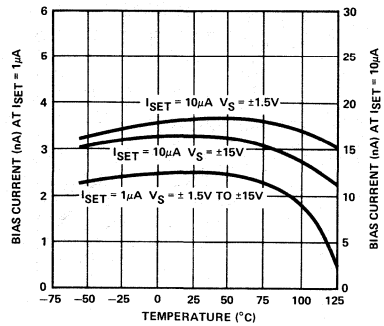
CURRENT NOISE vs FREQUENCY



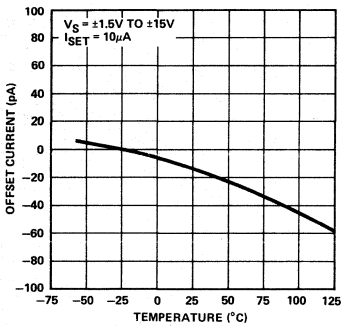
SUPPLY CURRENT vs TEMPERATURE



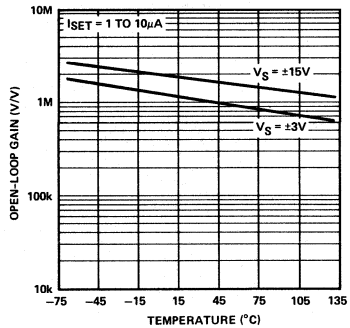
BIAS CURRENT vs TEMPERATURE



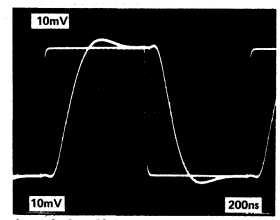
OFFSET CURRENT vs TEMPERATURE



OPEN-LOOP GAIN vs TEMPERATURE

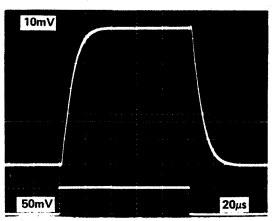


SMALL-SIGNAL TRANSIENT RESPONSE



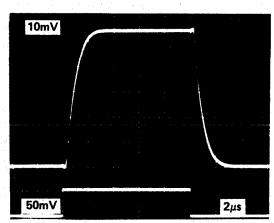
A_V = +1, C_L = 30pF
I_{SET} = 50μA
V_S = ±15V

SMALL-SIGNAL TRANSIENT RESPONSE



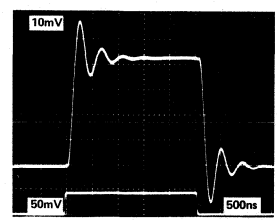
A_V = +1, C_L = 30pF
I_{SET} = 1μA
V_S = ±15V

SMALL-SIGNAL TRANSIENT RESPONSE



A_V = +1, C_L = 30pF
I_{SET} = 10μA
V_S = ±15V

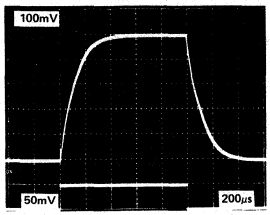
SMALL-SIGNAL TRANSIENT RESPONSE



A_V = +1, C_L = 30pF
I_{SET} = 100μA
V_S = ±15V

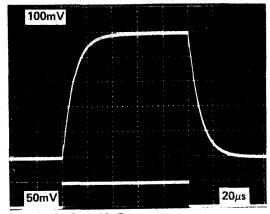
TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

SMALL-SIGNAL TRANSIENT RESPONSE



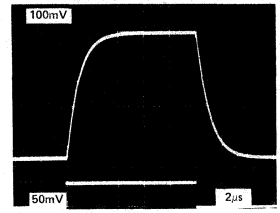
A_V = +10, C_L = 30pF
I_{SET} = 1µA
V_S = ±15V

SMALL-SIGNAL TRANSIENT RESPONSE



A_V = +10, C_L = 30pF
I_{SET} = 10µA
V_S = ±15V

SMALL-SIGNAL TRANSIENT RESPONSE



A_V = +10, C_L = 30pF
I_{SET} = 100µA
V_S = ±15V

2

APPLICATIONS INFORMATION

OP-22 series units may be inserted directly into LM4250, µA776 and ICL8021 sockets with or without removal of external nulling components. The value of set resistor for a given supply current varies between types and the manufacturer's data sheets should be consulted for this information. Table 1 compares set resistor values for the OP-22 and the LM4250. (R_{SET} connected to V−).

TABLE 1
Supply Current vs. Set Resistor for OP-22 and LM4250

	I_{SY} = 10µA		I_{SY} = 30µA		I_{SY} = 100µA	
V_{SUPPLY}	OP-22	LM4250	OP-22	LM4250	OP-22	LM4250
±1.5V	2.2MΩ	1.3MΩ	680kΩ	430kΩ	220kΩ	120kΩ
±3.0V	6.8MΩ	2.7MΩ	2.2MΩ	910kΩ	680kΩ	270kΩ
±5.0V	13MΩ	4.7MΩ	4.3MΩ	1.5MΩ	1.3MΩ	470kΩ
±12V	33MΩ	12MΩ	11MΩ	3.9MΩ	3.3MΩ	1.2MΩ
±15V	43MΩ	15MΩ	15MΩ	5.1MΩ	4.3MΩ	1.5MΩ
I_{SET}	0.67µA	1.8µA	2.0µA	6.0µA	6.7µA	20µA

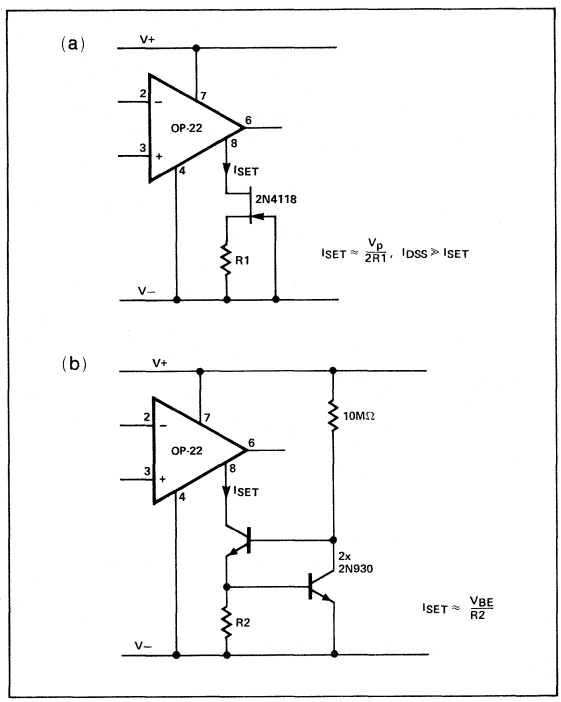
SET-RESISTOR SELECTION

The value of set resistor for selected supply current may be calculated using the "Supply current vs. Set current" curve and the formula;

$$R_{SET} = \frac{(V_{SUPPLY} - 2V_{BE})}{I_{SET}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (1)$$

Alternatively, the "Supply Current vs. Set Current" graph may be used in conjunction with the "Set Current vs. Set Resistor" graph. V_{SUPPLY} in formula (1) refers to the total supply voltage with R_{SET} connected between pin 8 and negative supply. R_{SET} may be connected to ground in which case V_{SUPPLY} in (1) is the positive supply.

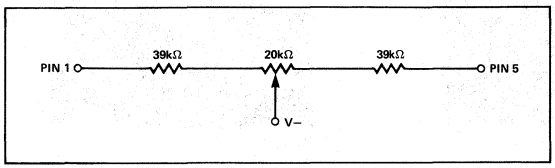
Biasing the OP-22 with a fixed resistor produces a supply current approximately proportional to supply voltage. In applications where a constant drain is required with varying supply, R_{SET} can be replaced by current generators. Two suggested arrangements are shown below:



CAUTION: Shorting of pin 8 to negative supply or ground will cause excessive I_{SET} which in turn will cause excessive supply current to flow. I_{SET} should always be limited.

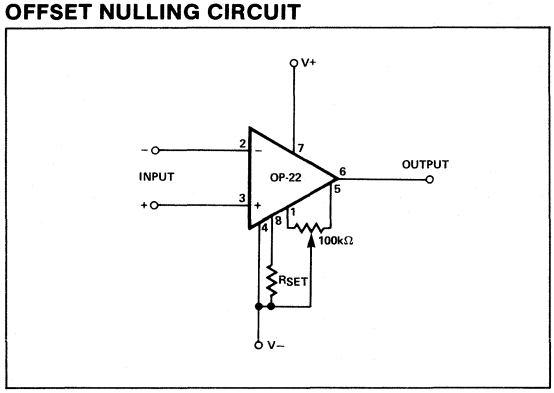
OFFSET VOLTAGE ADJUSTMENT

The offset voltage can be trimmed to zero using a 100kΩ potentiometer (see offset nulling circuit). Adjustment range is approximately ±5mV. Resolution of the nulling can be increased by using a smaller pot in conjunction with fixed resistors as shown below.

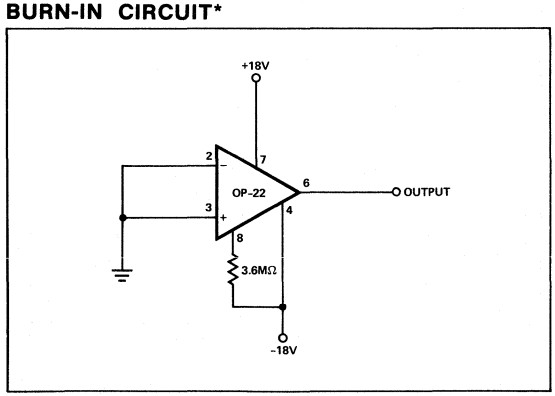


This arrangement has a ±500μV adjustment range. Offset nulling of the OP-22 has negligible effect on the value of TCV_{OS}.

OFFSET NULLING CIRCUIT



BURN-IN CIRCUIT*

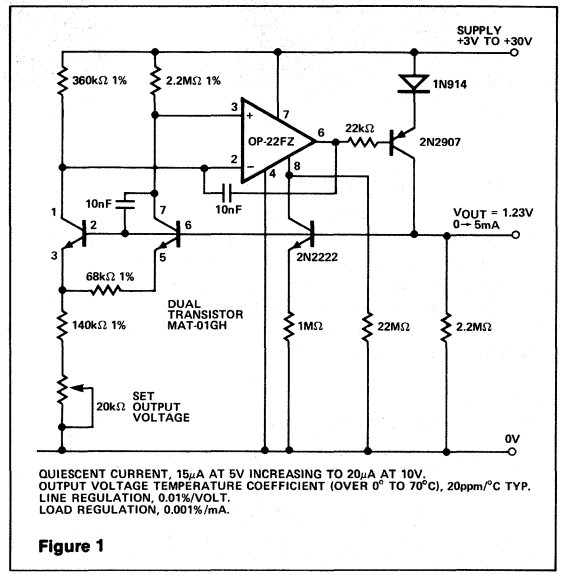


*Other circuits may apply at ADI's discretion.

APPLICATIONS CIRCUITS

A micropower bandgap voltage reference operating at a quiescent current of 15μA may be constructed using an OP-22 and a MAT-01 dual transistor (see Figure 1). The circuit provides a 1.23V reference with better performance than micropower I.C. shunt regulators and has the advantages of being a series regulator.

MICROPOWER 1.23 VOLT BANDGAP REFERENCE



QUIESCENT CURRENT, 15μA AT 5V INCREASING TO 20μA AT 10V.
OUTPUT VOLTAGE TEMPERATURE COEFFICIENT (OVER 0° TO 70°C), 20ppm/°C TYP.
LINE REGULATION, 0.01%/VOLT.
LOAD REGULATION, 0.001%/mA.

Figure 1

GATED MICROPOWER AMPLIFIER

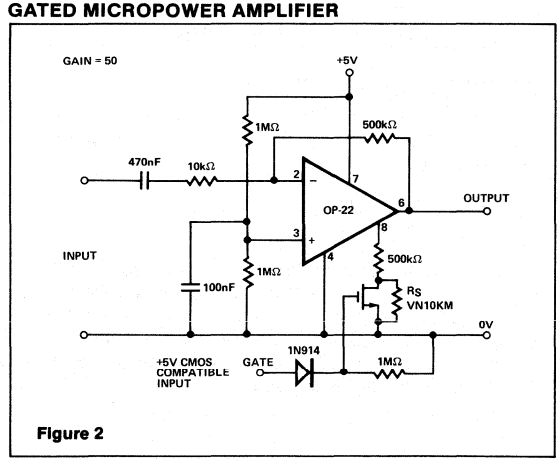


Figure 2

MICROPOWER INSTRUMENTATION AMPLIFIER — POWER DRAIN ≤ 3mW WITH ±5 VOLT SUPPLIES

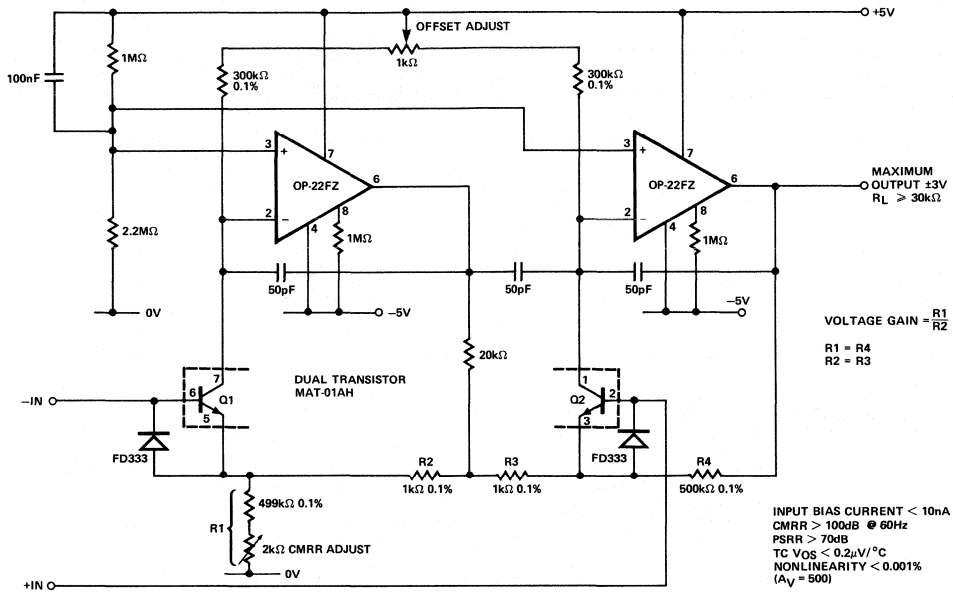


Figure 3

In Figure 2, the OP-22 is used as a gated amplifier where power consumption and bandwidth are controllable. R_S can be selected for a specific lower-power operation or omitted so the amplifier can be completely shut down.

A micropower instrumentation amplifier that consumes less than 3mW with ±5V supplies is shown in Figure 3. Offset voltage drift is less than 0.2μV/°C and common-mode input range is ±3V with CMRR of over 100dB at 60Hz.

Process control systems use two-wire 4-20mA current transmitters when sending analog signals through noisy environments. The "zero" or "offset" current of 4mA may be used to power the transmitter signal conditioning amplifiers and/or excite a d.c. transducer. This allows remote signal conditioning without having a remote power source. Power is provided at the receiving end where the signal current is monitored by a precision 50Ω resistor. The 4-20mA transmitter shown in Figure 4 has high stability, excellent linearity, and generates the 4-20mA current output. A 5V reference is available for powering transducers and micropower amplifiers at a maximum current of 2mA.

TWO TERMINAL 4-20mA TRANSMITTER

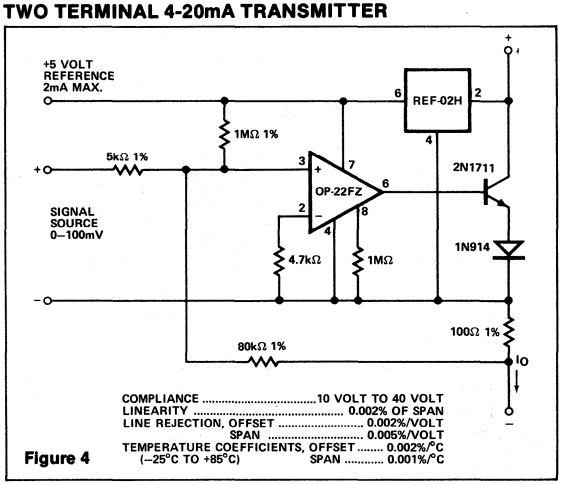


Figure 4

MICROPOWER WIEN-BRIDGE OSCILLATOR ($P_d < 500\mu W$)

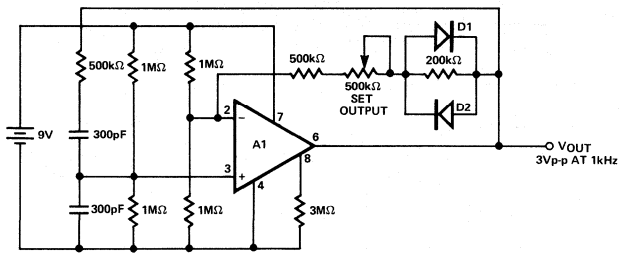


Figure 5

MICROPOWER 5 VOLT REGULATOR

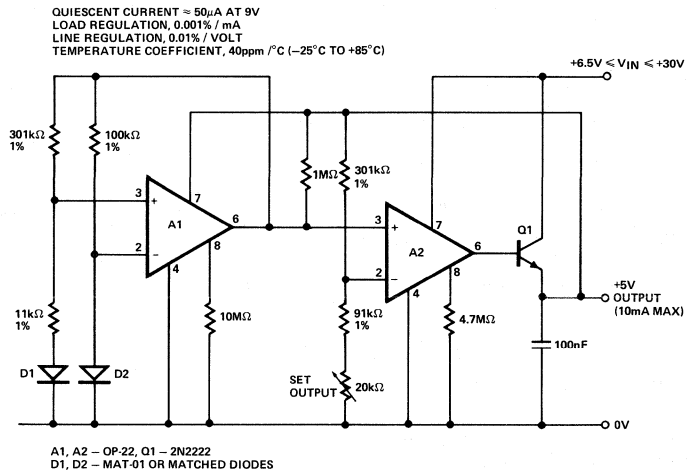


Figure 6

Figure 5 shows a micropower Wien-bridge oscillator designed for battery-powered instrumentation. Output level is controlled by nonlinear elements D1 and D2. When adjusted for 3V p-p output, the distortion level is below 0.5% at 1kHz.

The 5 volt regulator in Figure 6 is intended for instrumentation requiring good power efficiency. Low-power 3-terminal IC regulators typically draw 2mA to 5mA quiescent current compared to only 50μA with this discrete implementation. Maximum load current is 10mA as shown, and can be increased by changing Q1 to a power transistor and proportionately increasing the set current of A2.

ANALOG DEVICES

Low-Noise Precision Operational Amplifier

OP-27

FEATURES

- **Low Noise** ..... **80nV$_{p-p}$ (0.1Hz to 10Hz)**
  ..... **3nV/$\sqrt{Hz}$**
- **Low Drift** ..... **0.2μV/°C**
- **High Speed** ..... **2.8V/μs Slew Rate**
  ..... **8MHz Gain Bandwidth**
- **Low V_{OS}** **10μV**
- **Excellent CMRR** ..... **126dB at V_{CM} of ±11V**
- **High Open-Loop Gain** ..... **1.8 Million**
- **Fits 725, OP-07, OP-05, AD510, AD517, 5534A sockets**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (µV)	PACKAGE TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
25	OP27AJ*	OP27AZ*	–	–	MIL
25	OP27EJ	OP27EZ	OP27EP	–	IND/COM
60	OP27BJ*	OP27BZ*	–	OP27BR/883	MIL
60	OP27FJ	OP27FZ	OP27FP	–	IND/COM
100	OP27CJ	OP27CZ	–	–	MIL
100	OP27GJ	OP27GZ	OP27GP	–	XIND
100	–	–	OP27GS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

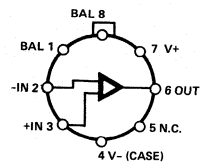
The OP-27 precision operational amplifier combines the low offset and drift of the OP-07 with both high speed and low noise. Offsets down to 25μV and drift of 0.6μV/°C maximum make the OP-27 ideal for precision instrumentation applications. Exceptionally low noise, e_n = 3.5nV/$\sqrt{Hz}$, at 10Hz, a low 1/f noise corner frequency of 2.7Hz, and high gain (1.8 million), allow accurate high-gain amplification of low-level signals. A gain-bandwidth product of 8MHz and a 2.8V/μsec slew rate provides excellent dynamic accuracy in high-speed data-acquisition systems.

A low input bias current of ±10nA is achieved by use of a bias-current-cancellation circuit. Over the military temperature range, this circuit typically holds I_B and I_{OS} to ±20nA and 15nA respectively.

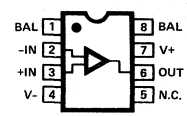
The output stage has good load driving capability. A guaranteed swing of ±10V into 600Ω and low output distortion make the OP-27 an excellent choice for professional audio applications.

PSRR and CMRR exceed 120dB. These characteristics, coupled with long-term drift of 0.2μV/month, allow the circuit designer to achieve performance levels previously attained only by discrete designs.

PIN CONNECTIONS



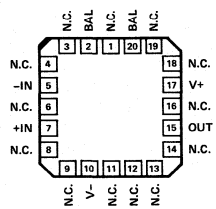
TO-99
(J-Suffix)



8-PIN HERMETIC DIP
(Z-Suffix)

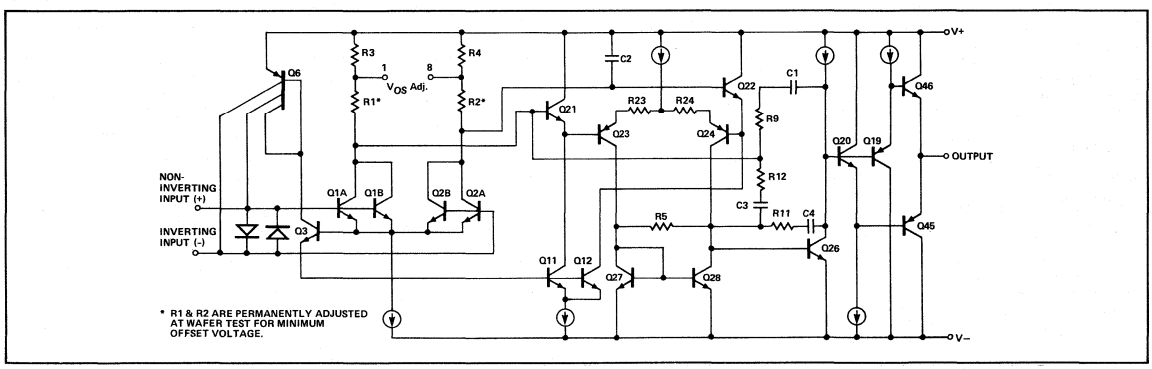
EPOXY MINI-DIP
(P-Suffix)

8-PIN SO
(S-Suffix)



OP-27BRC/883
LCC PACKAGE
(RC-Suffix)

SIMPLIFIED SCHEMATIC



OP-27

Low cost, high-volume production of OP-27 is achieved by using an on-chip zener-zap trimming network. This reliable and stable offset trimming scheme has proved its effectiveness over many years of production history.

The OP-27 provides excellent performance in low-noise high-accuracy amplification of low-level signals. Applications include stable integrators, precision summing amplifiers, precision voltage-threshold detectors, comparators, and professional audio circuits such as tape-head and microphone preamplifiers.

The OP-27 is a direct replacement for 725, OP-06, OP-07 and OP-05 amplifiers; 741 types may be directly replaced by removing the 741's nulling potentiometer.

ABSOLUTE MAXIMUM RATINGS (Note 4)

Supply Voltage ..... ±22V
Input Voltage (Note 1) ..... ±22V
Output Short-Circuit Duration ..... Indefinite
Differential Input Voltage (Note 2) ..... ±0.7V
Differential Input Current (Note 2) ..... ±25mA
Storage Temperature Range ..... –65°C to +150°C

Operating Temperature Range
OP-27A, OP-27B, OP-27C (J, Z, RC)..... –55°C to +125°C
OP-27E, OP-27F (J, Z) ..... –25°C to +85°C
OP-27E, OP-27F (P) ..... 0°C to +70°C
OP-27G (P, S, J, Z) ..... –40°C to +85°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature ..... –65°C to +150°C

PACKAGE TYPE	Θ_{JA} (Note 3)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC (RC)	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
2. The OP-27's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.
4. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-27A/E			OP-27B/F			OP-27C/G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	10	25	—	20	60	—	30	100	μV
Long-Term V_{OS} Stability	V_{OS}/Time	(Notes 2, 3)	—	0.2	1.0	—	0.3	1.5	—	0.4	2.0	μV/Mo
Input Offset Current	I_{OS}		—	7	35	—	9	50	—	12	75	nA
Input Bias Current	I_B		—	±10	±40	—	±12	±55	—	±15	±80	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Notes 3, 5)	—	0.08	0.18	—	0.08	0.18	—	0.09	0.25	μVp-p
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 3)	—	3.5	5.5	—	3.5	5.5	—	3.8	8.0	nV/√Hz
		f_O = 30Hz (Note 3)	—	3.1	4.5	—	3.1	4.5	—	3.3	5.6	
		f_O = 1000Hz (Note 3)	—	3.0	3.8	—	3.0	3.8	—	3.2	4.5	
Input Noise Current Density	i_n	f_O = 10Hz (Notes 3,6)	—	1.7	4.0	—	1.7	4.0	—	1.7	—	pA/√Hz
		f_O = 30Hz (Notes 3, 6)	—	1.0	2.3	—	1.0	2.3	—	1.0	—	
		f_O = 1000Hz (Notes 3, 6)	—	0.4	0.6	—	0.4	0.6	—	0.4	0.6	
Input Resistance — Differential-Mode	R_{IN}	(Note 7)	1.3	6	—	0.94	5	—	0.7	4	—	MΩ
Input Resistance — Common-Mode	R_{INCM}		—	3	—	—	2.5	—	—	2	—	GΩ
Input Voltage Range	IVR		±11.0	±12.3	—	±11.0	±12.3	—	±11.0	±12.3	—	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±11V	114	126	—	106	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±4V to ±18V	—	1	10	—	1	10	—	2	20	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10V	1000	1800	—	1000	1800	—	700	1500	—	V/mV
		$R_L \geq 600\Omega$, V_O = ±10V	800	1500	—	800	1500	—	600	1500	—	
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.0	±13.8	—	±12.0	±13.8	—	±11.5	±13.5	—	V
		$R_L \geq 600\Omega$	±10.0	±11.5	—	±10.0	±11.5	—	±10.0	±11.5	—	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 4)	1.7	2.8	—	1.7	2.8	—	1.7	2.8	—	V/μs

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-27A/E MIN	OP-27A/E TYP	OP-27A/E MAX	OP-27B/F MIN	OP-27B/F TYP	OP-27B/F MAX	OP-27C/G MIN	OP-27C/G TYP	OP-27C/G MAX	UNITS
Gain Bandwidth Prod.	GBW	(Note 4)	5.0	8.0	—	5.0	8.0	—	5.0	8.0	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	70	—	—	70	—	—	70	—	Ω
Power Consumption	P_d	V_O	—	90	140	—	90	140	—	100	170	mW
Offset Adjustment Range		$R_P = 10k\Omega$	—	±4.0	—	—	±4.0	—	—	±4.0	—	mV

NOTES:
1. Input offset voltage measurements are performed ~ 0.5 seconds after application of power. A/E grades guaranteed fully warmed-up.
2. Long-term input offset voltage stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5μV — refer to typical performance curve.
3. Sample tested.
4. Guaranteed by design.
5. See test circuit and frequency response curve for 0.1Hz to 10Hz tester.
6. See test circuit for current noise measurement.
7. Guaranteed by input bias current.

2

ELECTRICAL CHARACTERISTICS for $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$, unless otherwise noted.

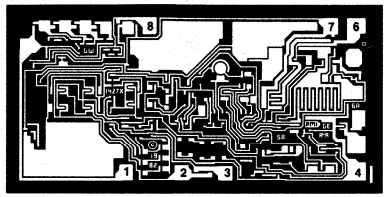
PARAMETER	SYMBOL	CONDITIONS	OP-27A MIN	OP-27A TYP	OP-27A MAX	OP-27B MIN	OP-27B TYP	OP-27B MAX	OP-27C MIN	OP-27C TYP	OP-27C MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	30	60	—	50	200	—	70	300	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSn}	(Note 2) (Note 3)	—	0.2	0.6	—	0.3	1.3	—	0.4	1.8	μV/°C
Input Offset Current	I_{OS}		—	15	50	—	22	85	—	30	135	nA
Input Bias Current	I_B		—	±20	±60	—	±28	±95	—	±35	±150	nA
Input Voltage Range	IVR		±10.3	±11.5	—	±10.3	±11.5	—	±10.2	±11.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	108	122	—	100	119	—	94	116	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	16	—	2	20	—	4	51	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	600	1200	—	500	1000	—	300	800	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±11.5	±13.5	—	±11.0	±13.2	—	±10.5	±13.0	—	V

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-25°C \le T_A \le +85°C$ for OP-27J and OP-27Z, $0°C \le T_A \le +70°C$ for OP-27EP, FP and $-40°C \le T_A \le +85°C$ for OP-27GP, GS, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-27E MIN	OP-27E TYP	OP-27E MAX	OP-27F MIN	OP-27F TYP	OP-27F MAX	OP-27G MIN	OP-27G TYP	OP-27G MAX	UNITS
Input Offset Voltage	V_{OS}		—	20	50	—	40	140	—	55	220	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSn}	(Note 2) (Note 3)	—	0.2	0.6	—	0.3	1.3	—	0.4	1.8	μV/°C
Input Offset Current	I_{OS}		—	10	50	—	14	85	—	20	135	nA
Input Bias Current	I_B		—	±14	±60	—	±18	±95	—	±25	±150	nA
Input Voltage Range	IVR		±10.5	±11.8	—	±10.5	±11.8	—	±10.5	±11.8	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	110	124	—	102	121	—	96	118	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	15	—	2	16	—	2	32	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	750	1500	—	700	1300	—	450	1000	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±11.7	±13.6	—	±11.4	±13.5	—	±11.0	±13.3	—	V

NOTES:
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E grades guaranteed fully warmed-up.
2. The TCV_{OS} performance is within the specifications unnulled or when nulled with $R_P = 8k\Omega$ to $20k\Omega$. TCV_{OS} is 100% tested for A/E grades, sample tested for B/C/F/G grades.
3. Guaranteed by design.

DICE CHARACTERISTICS



DIE SIZE 0.109 × 0.055 inch, 5995 sq. mils
(2.77 × 1.40mm, 3.88 sq. mm)

1. NULL
2. (–) INPUT
3. (+) INPUT
4. V–
6. OUTPUT
7. V+
8. NULL

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$ for OP-27N, OP-27G, and OP-27GR devices; $T_A = 125°C$ for OP-27NT and OP-27GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-27NT LIMIT	OP-27N LIMIT	OP-27GT LIMIT	OP-27G LIMIT	OP-27GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	60	35	200	60	100	μV MAX
Input Offset Current	I_{OS}		50	35	85	50	75	nA MAX
Input Bias Current	I_B		±60	±40	±95	±55	±80	nA MAX
Input Voltage Range	IVR		±10.3	±11	±10.3	±11	±11	V MIN
Common-Mode Rejection Ratio	CMRR	V_{CM} = IVR	108	114	100	106	100	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4V$ to $\pm 18V$	—	10	—	10	20	μV/V MAX
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$ $R_L \geq 600\Omega$, $V_O = \pm 10V$	600 —	1000 800	500 —	1000 800	700 600	V/mV MIN
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$ $R_L \geq 600\Omega$	±11.5 —	±12.0 ±10.0	±11.0 —	±12.0 ±10.0	±11.5 ±10.0	V MIN
Power Consumption	P_d	$V_O = 0$	—	140	—	140	170	mW MAX

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

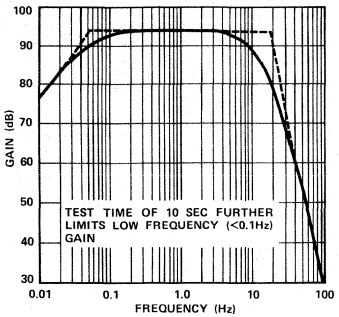
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-27N TYPICAL	OP-27G TYPICAL	OP-27GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS} or TCV_{OSn}	Nulled or Unnulled $R_P = 8k\Omega$ to $20k\Omega$	0.2	0.3	0.4	μV/°C
Average Input Offset Current Drift	TCI_{OS}		80	130	180	pA/°C
Average Input Bias Current Drift	TCI_B		100	160	200	pA/°C
Input Noise Voltage Density	e_n	$f_O = 10Hz$ $f_O = 30Hz$ $f_O = 1000Hz$	3.5 3.1 3.0	3.5 3.1 3.0	3.8 3.3 3.2	$nV/\sqrt{Hz}$
Input Noise Current Density	i_n	$f_O = 10Hz$ $f_O = 30Hz$ $f_O = 1000Hz$	1.7 1.0 0.4	1.7 1.0 0.4	1.7 1.0 0.4	$pA/\sqrt{Hz}$
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	0.08	0.08	0.09	μVp-p
Slew Rate	SR	$R_L \geq 2k\Omega$	2.8	2.8	2.8	V/μs
Gain Bandwidth Product	GBW		8	8	8	MHz

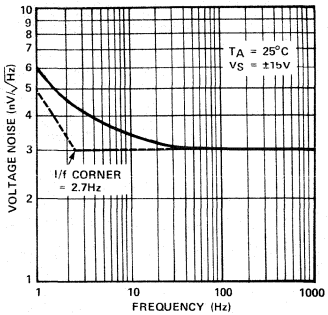
NOTE:
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

TYPICAL PERFORMANCE CHARACTERISTICS

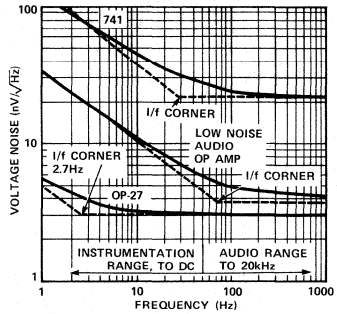
0.1Hz TO 10Hz$_{p-p}$ NOISE TESTER FREQUENCY RESPONSE



VOLTAGE NOISE DENSITY vs FREQUENCY

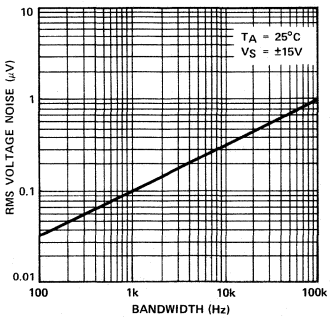


A COMPARISON OF OP AMP VOLTAGE NOISE SPECTRA

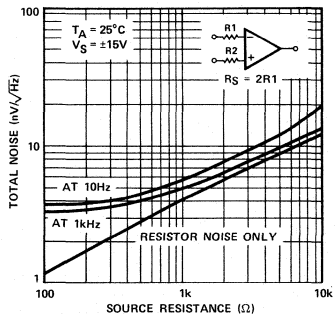


2

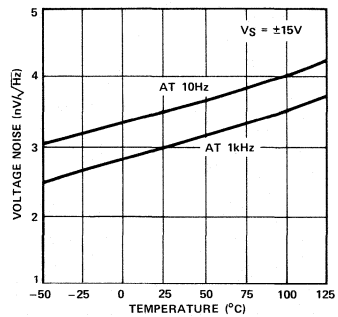
INPUT WIDEBAND VOLTAGE NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



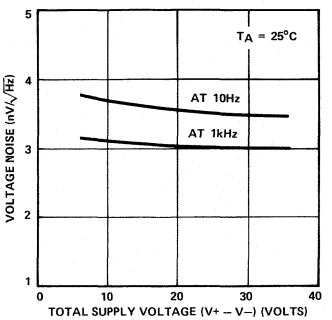
TOTAL NOISE vs SOURCE RESISTANCE



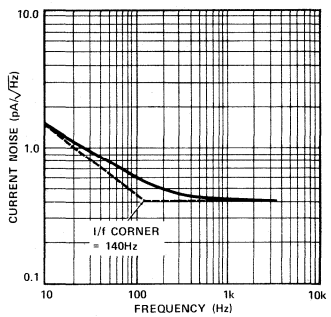
VOLTAGE NOISE DENSITY vs TEMPERATURE



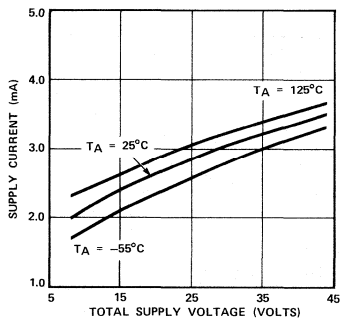
VOLTAGE NOISE DENSITY vs SUPPLY VOLTAGE



CURRENT NOISE DENSITY vs FREQUENCY

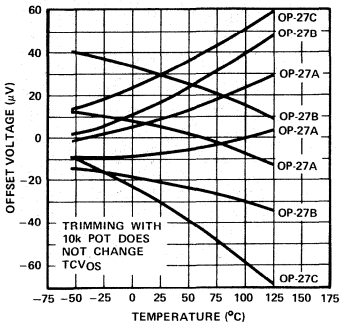


SUPPLY CURRENT vs SUPPLY VOLTAGE

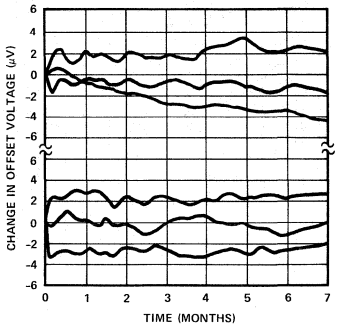


TYPICAL PERFORMANCE CHARACTERISTICS

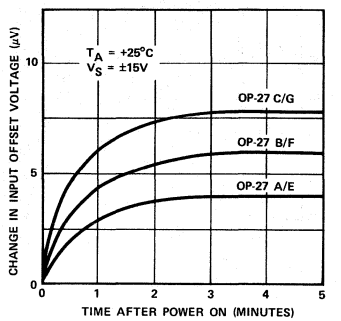
OFFSET VOLTAGE DRIFT OF EIGHT REPRESENTATIVE UNITS vs TEMPERATURE



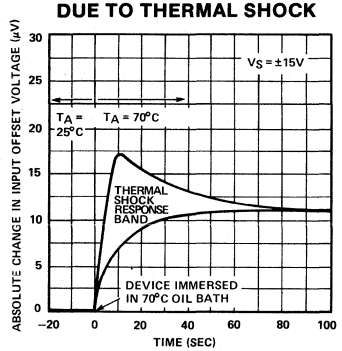
LONG-TERM OFFSET VOLTAGE DRIFT OF SIX REPRESENTATIVE UNITS



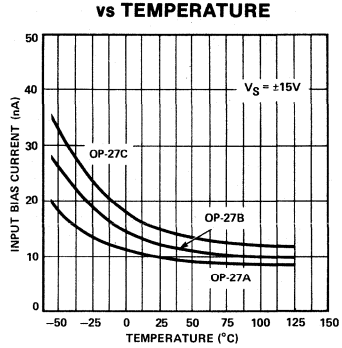
WARM-UP OFFSET VOLTAGE DRIFT



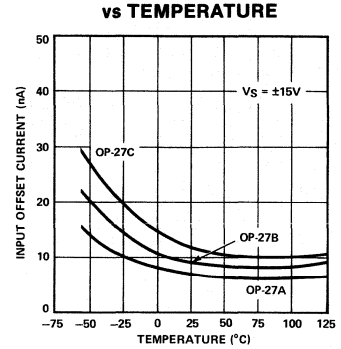
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



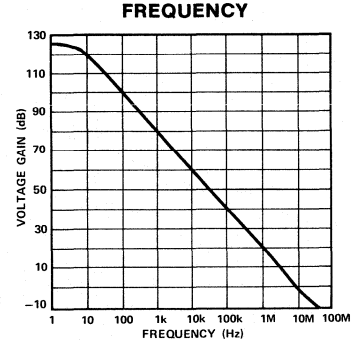
INPUT BIAS CURRENT vs TEMPERATURE



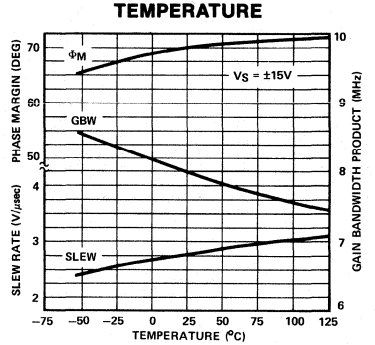
INPUT OFFSET CURRENT vs TEMPERATURE



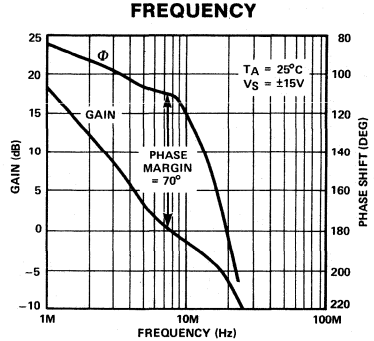
OPEN-LOOP GAIN vs FREQUENCY



SLEW RATE, GAIN-BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE

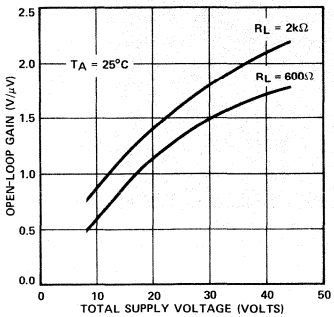


GAIN, PHASE SHIFT vs FREQUENCY

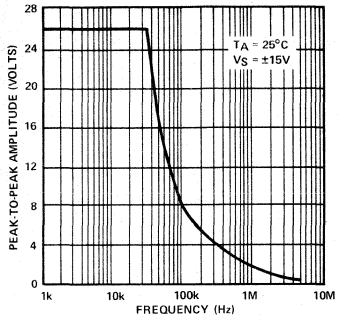


TYPICAL PERFORMANCE CHARACTERISTICS

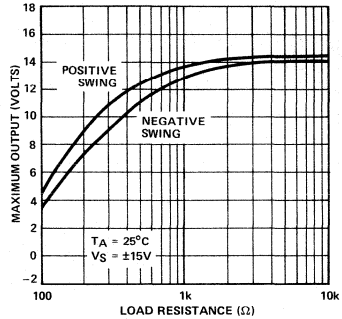
OPEN-LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE



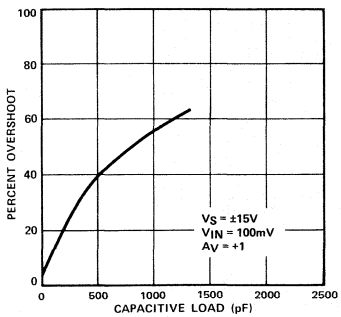
MAXIMUM OUTPUT SWING vs FREQUENCY



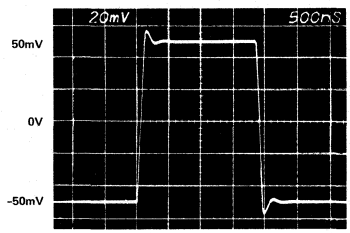
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD

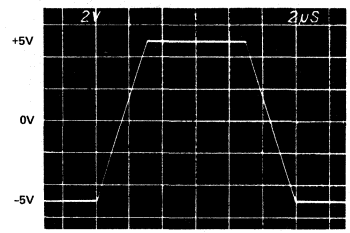


SMALL-SIGNAL TRANSIENT RESPONSE



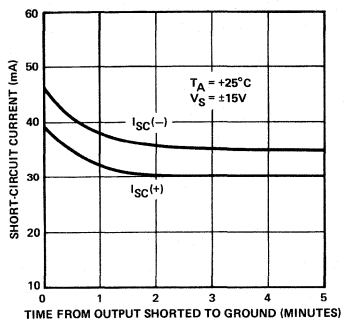
A_{VCL} = +1, C_L = 15pF
V_S = ±15V
T_A = 25°C

LARGE-SIGNAL TRANSIENT RESPONSE

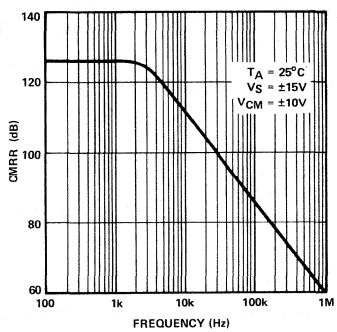


A_{VCL} = +1
V_S = ±15V
T_A = 25°C

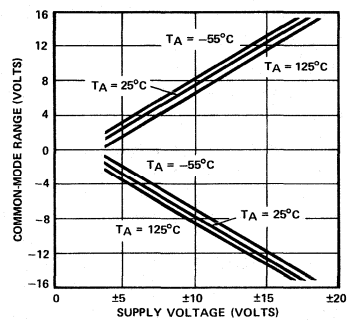
SHORT-CIRCUIT CURRENT vs TIME



CMRR vs FREQUENCY

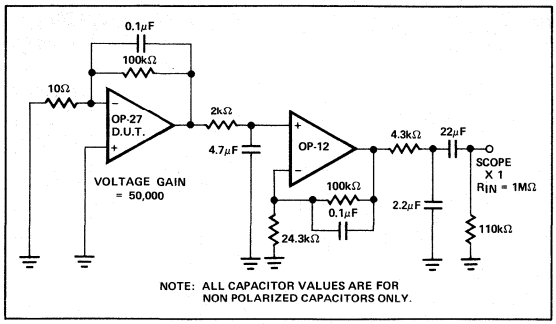


COMMON-MODE INPUT RANGE vs SUPPLY VOLTAGE

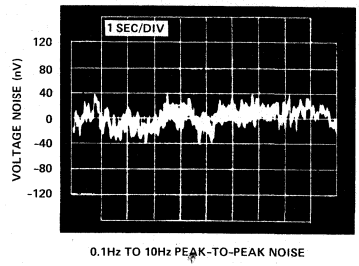


TYPICAL PERFORMANCE CHARACTERISTICS

VOLTAGE NOISE TEST CIRCUIT (0.1Hz-TO-10Hz)



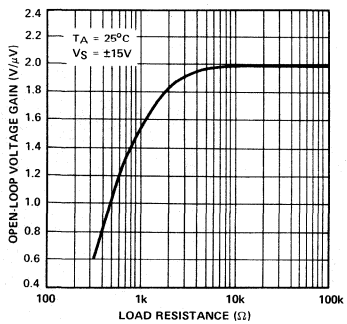
LOW-FREQUENCY NOISE



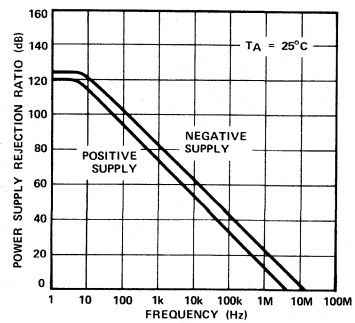
0.1Hz TO 10Hz PEAK-TO-PEAK NOISE

NOTE:
Observation time limited to 10 seconds.

OPEN-LOOP VOLTAGE GAIN vs LOAD RESISTANCE



PSRR vs FREQUENCY



APPLICATIONS INFORMATION

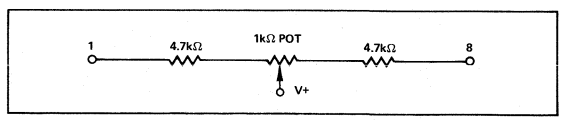
OP-27 Series units may be inserted directly into 725, OP-06, OP-07 and OP-05 sockets with or without removal of external compensation or nulling components. Additionally, the OP-27 may be fitted to unnulled 741-type sockets; however, if conventional 741 nulling circuitry is in use, it should be modified or removed to ensure correct OP-27 operation. OP-27 offset voltage may be nulled to zero (or other desired setting) using a potentiometer (see Offset Nulling Circuit).

The OP-27 provides stable operation with load capacitances of up to 2000pF and ±10V swings; larger capacitances should be decoupled with a 50Ω resistor inside the feedback loop. The OP-27 is unity-gain stable.

Thermoelectric voltages generated by dissimilar metals at the input terminal contacts can degrade the drift performance. Best operation will be obtained when both input contacts are maintained at the same temperature.

OFFSET VOLTAGE ADJUSTMENT

The input offset voltage of the OP-27 is trimmed at wafer level. However, if further adjustment of V_{OS} is necessary, a 10kΩ trim potentiometer may be used. TCV_{OS} is not degraded (see Offset Nulling Circuit). Other potentiometer values from 1kΩ to 1MΩ can be used with a slight degradation (0.1 to 0.2μV/°C) of TCV_{OS}. Trimming to a value other than zero creates a drift of approximately (V_{OS}/300) μV/°C. For example, the change in TCV_{OS} will be 0.33μV/°C if V_{OS} is adjusted to 100μV. The offset-voltage adjustment range with a 10kΩ potentiometer is ±4mV. If smaller adjustment range is required, the nulling sensitivity can be reduced by using a smaller pot in conjuction with fixed resistors. For example, the network below will have a ±280μV adjustment range.



NOISE MEASUREMENTS

To measure the 80nV peak-to-peak noise specification of the OP-27 in the 0.1Hz to 10Hz range, the following precautions must be observed:

(1) The device has to be warmed-up for at least five minutes. As shown in the warm-up drift curve, the offset voltage

typically changes 4μV due to increasing chip temperature after power-up. In the 10-second measurement interval, these temperature-induced effects can exceed tens-of-nanovolts.

(2) For similar reasons, the device has to be well-shielded from air currents. Shielding minimizes thermocouple effects.

(3) Sudden motion in the vicinity of the device can also "feed-through" to increase the observed noise.

(4) The test time to measure 0.1Hz-to-10Hz noise should not exceed 10 seconds. As shown in the noise-tester frequency-response curve, the 0.1Hz corner is defined by only one zero. The test time of 10 seconds acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

(5) A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage-density measurement will correlate well with a 0.1Hz-to-10Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the 1/f corner frequency.

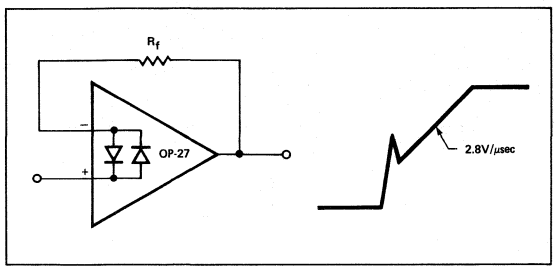
UNITY-GAIN BUFFER APPLICATIONS

When $R_f \leq 100\Omega$ and the input is driven with a fast, large signal pulse (>1V), the output waveform will look as shown in the pulsed operation diagram below.

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input and a current, limited only by the output short-circuit protection, will be drawn by the signal generator. With $R_f \geq 500\Omega$, the output is capable of handling the current requirements ($I_L \leq 20mA$ at 10V); the amplifier will stay in its active mode and a smooth transition will occur.

When $R_f > 2k\Omega$, a pole will be created with R_f and the amplifier's input capacitance (8pF) that creates additional phase shift and reduces phase margin. A small capacitor (20 to 50pF) in parallel with R_f will eliminate this problem.

PULSED OPERATION



COMMENTS ON NOISE

The OP-27 is a very low-noise monolithic op amp. The outstanding input voltage noise characteristics of the OP-27 are achieved mainly by operating the input stage at a high quiescent current. The input bias and offset currents, which would normally increase, are held to reasonable values by the input-bias-current cancellation circuit. The OP-27A/E has I_B and I_{OS} of only ±40nA and 35nA respectively at 25°C. This is particularly important when the input has a high source-resistance. In addition, many audio amplifier designers prefer to use direct coupling. The high I_B, V_{OS}, TCV_{OS} of previous designs have made direct coupling difficult, if not impossible, to use.

Voltage noise is inversely proportional to the square-root of bias current, but current noise is proportional to the square-root of bias current. The OP-27's noise advantage disappears when high source-resistors are used. Figures 1, 2, and 3 compare OP-27 observed total noise with the noise performance of other devices in different circuit applications.

Total noise = $[(\text{Voltage noise})^2 + (\text{current noise} \times R_S)^2 + (\text{resistor noise})^2]^{1/2}$

Figure 1 shows noise-versus-source-resistance at 1000Hz. The same plot applies to wideband noise. To use this plot, just multiply the vertical scale by the square-root of the bandwidth.

NOISE vs SOURCE RESISTANCE (INCLUDING RESISTOR NOISE) AT 1000Hz.

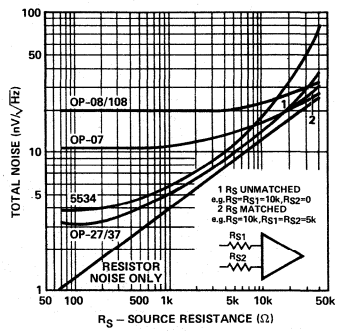


Figure 1

At $R_S < 1k\Omega$, the OP-27's low voltage noise is maintained. With $R_S > 1k\Omega$, total noise increases, but is dominated by the resistor noise rather than current or voltage noise. It is only beyond R_S of 20kΩ that current noise starts to dominate. The argument can be made that current noise is not important for applications with low-to-moderate source resistances. The crossover between the OP-27 and OP-07 and OP-08 noise occurs in the 15-to-40kΩ region.

Figure 2 shows the 0.1Hz-to-10Hz peak-to-peak noise. Here the picture is less favorable; resistor noise is negligible, current noise becomes important because it is inversely proportional to the square-root of frequency. The crossover with the OP-07 occurs in the 3-to-5kΩ range depending on whether balanced or unbalanced source resistors are used (at 3kΩ the I_B, I_{OS} error also can be three times the V_{OS} spec.).

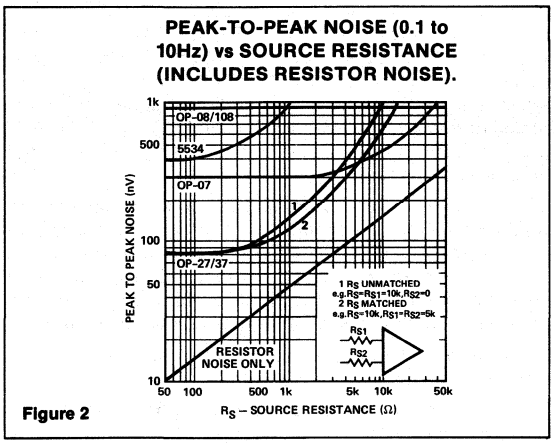


Figure 2

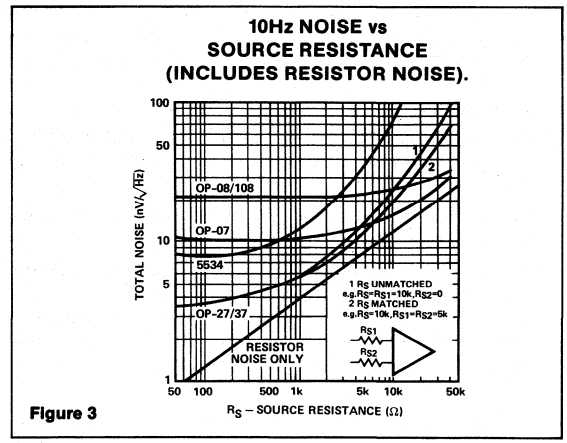


Figure 3

Therefore, for low-frequency applications, the OP-07 is better than the OP-27/37 when $R_S > 3k\Omega$. The only exception is when gain error is important. Figure 3 illustrates the 10Hz noise. As expected, the results are between the previous two figures.

For reference, typical source resistances of some signal sources are listed in Table 1.

Table 1

DEVICE	SOURCE IMPEDANCE	COMMENTS
Strain gauge	<500Ω	Typically used in low-frequency applications.
Magnetic tapehead	<1500Ω	Low I_B very important to reduce self-magnetization problems when direct coupling is used. OP-27 I_B can be neglected.
Magnetic phonograph cartridges	<1500Ω	Similar need for low I_B in direct coupled applications. OP-27 will not introduce any self-magnetization problem.
Linear variable differential transformer	<1500Ω	Used in rugged servo-feedback applications. Bandwidth of interest is 400Hz to 5kHz.

OPEN-LOOP GAIN

FREQUENCY AT:	OP-07	OP-27	OP-37
3Hz	100dB	124dB	125dB
10Hz	100dB	120dB	125dB
30Hz	90dB	110dB	124dB

For further information regarding noise calculations, see "Minimization of Noise in Op-Amp Applications," Application Note AN-15.

AUDIO APPLICATIONS

The following applications information has been abstracted from a PMI article in the 12/20/80 issue of Electronic Design magazine and updated.

Figure 4 is an example of a phono pre-amplifier circuit using the OP-27 for A_1; R_1-R_2-C_1-C_2 form a very accurate RIAA network with standard component values. The popular method to accomplish RIAA phono equalization is to employ frequency-dependent feedback around a high-quality gain block. Properly chosen, an RC network can provide the three necessary time constants of 3180, 318, and 75μs.[1]

For initial equalization accuracy and stability, precision metal-film resistors and film capacitors of polystyrene or polypropylene are recommended since they have low voltage coefficients, dissipation factors, and dielectric absorption.[4] (High-K ceramic capacitors should be avoided here, though low-K ceramics—such as NPO types, which have excellent dissipation factors, and somewhat lower dielectric absorption—can be considered for small values.)

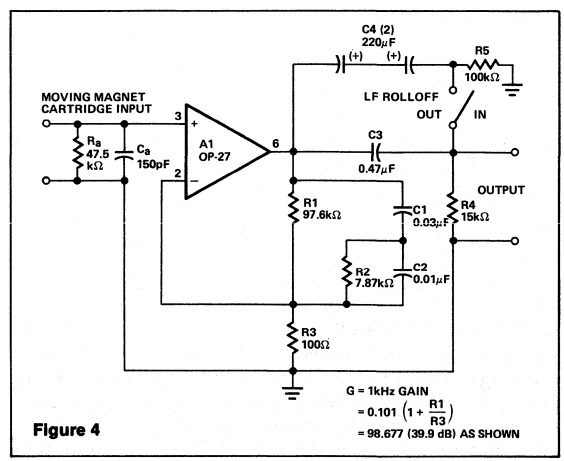


Figure 4

The OP-27 brings a 3.2nV/$\sqrt{Hz}$ voltage noise and 0.45 pA/$\sqrt{Hz}$ current noise to this circuit. To minimize noise from other sources, R_3 is set to a value of 100Ω, which generates a voltage noise of 1.3nV/$\sqrt{Hz}$. The noise increases the 3.2nV/$\sqrt{Hz}$ of the amplifier by only 0.7dB. With a 1kΩ source, the circuit noise measures 63dB below a 1mV reference level, unweighted, in a 20kHz noise bandwidth.

Gain (G) of the circuit at 1kHz can be calculated by the expression:

$$G = 0.101\ (1 + \frac{R_1}{R_3})$$

For the values shown, the gain is just under 100 (or 40dB). Lower gains can be accommodated by increasing R_3, but gains higher than 40dB will show more equalization errors because of the 8MHz gain-bandwidth of the OP-27.

This circuit is capable of very low distortion over its entire range, generally below 0.01% at levels up to 7V rms. At 3V output levels, it will produce less than 0.03% total harmonic distortion at frequencies up to 20kHz.

Capacitor C_3 and resistor R_4 form a simple −6dB-per-octave rumble filter, with a corner at 22Hz. As an option, the switch-selected shunt capacitor C_4, a nonpolarized electrolytic, bypasses the low-frequency rolloff. Placing the rumble filter's high-pass action after the preamp has the desirable result of discriminating against the RIAA-amplified low-frequency noise components and pickup-produced low-frequency disturbances.

A preamplifier for NAB tape playback is similar to an RIAA phono preamp, though more gain is typically demanded, along with equalization requiring a heavy low-frequency boost. The circuit in Fig. 4 can be readily modified for tape use, as shown by Fig. 5.

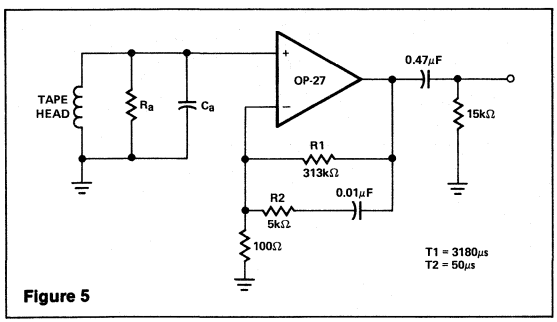


Figure 5

While the tape-equalization requirement has a flat high-frequency gain above 3kHz ($T_2 = 50\mu s$), the amplifier need not be stabilized for unity gain. The decompensated OP-37 provides a greater bandwidth and slew rate. For many applications, the idealized time constants shown may require trimming of R_1 and R_2 to optimize frequency response for nonideal tape-head performance and other factors.[5]

The network values of the configuration yield a 50dB gain at 1kHz, and the dc gain is greater than 70dB. Thus, the worst-case output offset is just over 500mV. A single 0.47μF output capacitor can block this level without affecting the dynamic range.

The tape head can be coupled directly to the amplifier input, since the worst-case bias current of 80nA with a 400mH, 100 μin. head (such as the PRB2H7K) will not be troublesome.

One potential tape-head problem is presented by amplifier bias-current transients which can magnetize a head. The OP-27 and OP-37 are free of bias-current transients upon power up or power down. However, it is always advantageous to control the speed of power supply rise and fall, to eliminate transients.

In addition, the dc resistance of the head should be carefully controlled, and preferably below 1kΩ. For this configuration, the bias-current-induced offset voltage can be greater than the 100μV maximum offset if the head resistance is not sufficiently controlled.

A simple, but effective, fixed-gain transformerless microphone preamp (Fig. 6) amplifies differential signals from low-impedance microphones by 50dB, and has an input impedance of 2kΩ. Because of the high working gain of the circuit, an OP-37 helps to preserve bandwidth, which will be 110kHz. As the OP-37 is a decompensated device (minimum stable gain of 5), a dummy resistor, R_p, may be necessary, if the microphone is to be unplugged. Otherwise the 100% feedback from the open input may cause the amplifier to oscillate.

Common-mode input-noise rejection will depend upon the match of the bridge-resistor ratios. Either close-tolerance (0.1%) types should be used, or R_4 should be trimmed for best CMRR. All resistors should be metal-film types for best stability and low noise.

Noise performance of this circuit is limited more by the input resistors R_1 and R_2 than by the op amp, as R_1 and R_2 each generate a 4nV/$\sqrt{Hz}$ noise, while the op amp generates a 3.2nV/$\sqrt{Hz}$ noise. The rms sum of these predominant noise sources will be about 6nV/$\sqrt{Hz}$, equivalent to 0.9μV in a 20kHz noise bandwidth, or nearly 61dB below a 1mV input signal. Measurements confirm this predicted performance.

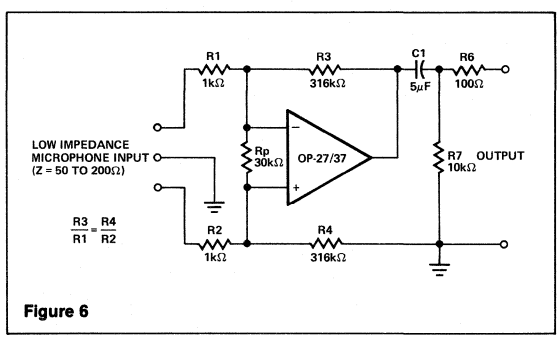
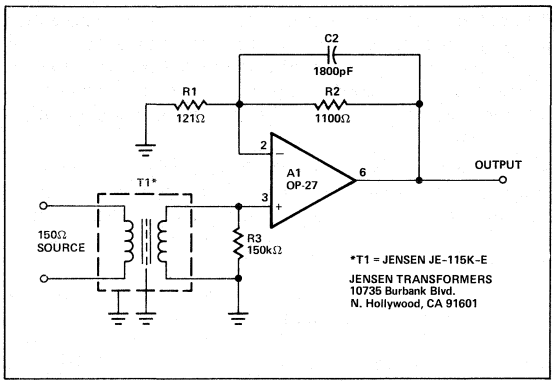


Figure 6

For applications demanding appreciably lower noise, a high-quality microphone-transformer-coupled preamp (Fig. 7) incorporates the internally-compensated OP-27. T_1 is a JE-115K-E 150Ω/15kΩ transformer which provides an optimum source resistance for the OP-27 device. The circuit has an overall gain of 40dB, the product of the transformer's voltage setup and the op amp's voltage gain.



Gain may be trimmed to other levels, if desired, by adjusting R_2 or R_1. Because of the low offset voltage of the OP-27, the output offset of this circuit will be very low, 1.7mV or less, for a 40dB gain. The typical output blocking capacitor can be eliminated in such cases, but is desirable for higher gains to eliminate switching transients.

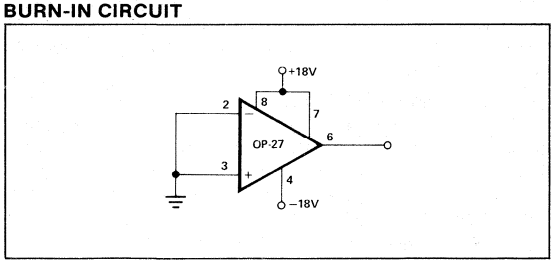
Capacitor C_2 and resistor R_2 form a 2μs time constant in this circuit, as recommended for optimum transient response by the transformer manufacturer. With C_2 in use, A_1 must have unity-gain stability. For situations where the 2μs time constant is not necessary, C_2 can be deleted, allowing the faster OP-37 to be employed.

Some comment on noise is appropriate to understand the capability of this circuit. A 150Ω resistor and R_1 and R_2 gain resistors connected to a noiseless amplifier will generate 220 nV of noise in a 20kHz bandwidth, or 73dB below a 1mV reference level. Any practical amplifier can only approach this noise level; it can never exceed it. With the OP-27 and T_1 specified, the additional noise degradation will be close to 3.6dB (or −69.5 referenced to 1mV).

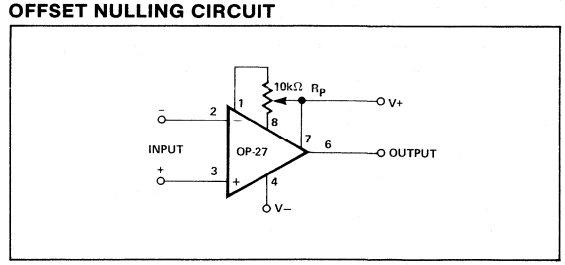
References

1. Lipshitz, S.P., "On RIAA Equalization Networks," *JAES*, Vol. 27, June 1979, p. 458-481.
2. Jung, W.G., *IC Op Amp Cookbook*, 2nd Ed., H.W. Sams and Company, 1980.
3. Jung, W.G., *Audio IC Op Amp Applications*, 2nd Ed., H.W. Sams and Company, 1978.
4. Jung, W.G., and Marsh, R.M., "Picking Capacitors," *Audio*, February & March, 1980.
5. Otala, M., "Feedback-Generated Phase Nonlinearity in Audio Amplifiers," London AES Convention, March 1980, preprint 1976.
6. Stout, D.F., and Kaufman, M., *Handbook of Operational Amplifier Circuit Design*, New York, McGraw Hill, 1976.

BURN-IN CIRCUIT



OFFSET NULLING CIRCUIT



High-Speed ($A_{VCL} \geq 10$) Programmable Micropower Operational Amplifier

OP-32

FEATURES

- Programmable Supply Current ..... 500nA to 2mA
- Single Supply Operation ..... +3V to +30V
- Dual Supply Operation ..... ±1.5V to ±15V
- Low Input Offset Voltage 100μV
- Low Input Offset Voltage Drift ..... 0.5μV/°C
- High Common-Mode Input Range ..... V– to V+ (–1.5V)
- High CMRR and PSRR 115dB
- High Open-Loop Gain 2000V/mV
- ±30V Input Overvoltage Protection
- Fast ..... 1V/μs @ I_{SY} = 300μA
- LM4250 Pinout
- Compensated for Minimum Gain of 10
- Available in Die Form

ORDERING INFORMATION †

T_A = 25°C V_{OS} MAX (μV)	PACKAGE CERDIP 8-PIN	PACKAGE PLASTIC 8-PIN	OPERATING TEMPERATURE RANGE
300	–	OP32AZ*	MIL
300	OP32EP	OP32EZ	IND
500	OP32FP	OP32FZ	IND
1000	OP32GP	OP32GZ	IND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

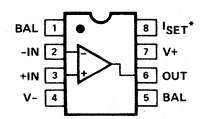
The OP-32 is a high-speed, high-gain programmable operational amplifier. Both offset voltage and offset current are low, and both are stable with changes in temperature, supply voltage, and set current. High CMRR and PSRR ensure precision performance when the OP-32 is used with an unregulated battery or vehicular electrical system.

The wide input voltage range, including the negative supply or ground, allows use in single-battery applications. The OP-32 is characterized over a wide supply range of ±1.5V to ±15V. This guarantees predictable performance with any commonly available supply.

The ability to operate at relatively high speed with low power consumption makes this amplifier ideal for remote applications where power is limited. The programmability allows each amplifier in a system to be set for the minimum power consumption necessary for each specific application. Programmability also makes it possible to adjust the bandwidth and phase shift.

The OP-32 pinout is identical to the LM4250 and many other micropower operational amplifiers. This allows easy upgrading of system performance.

PIN CONNECTIONS

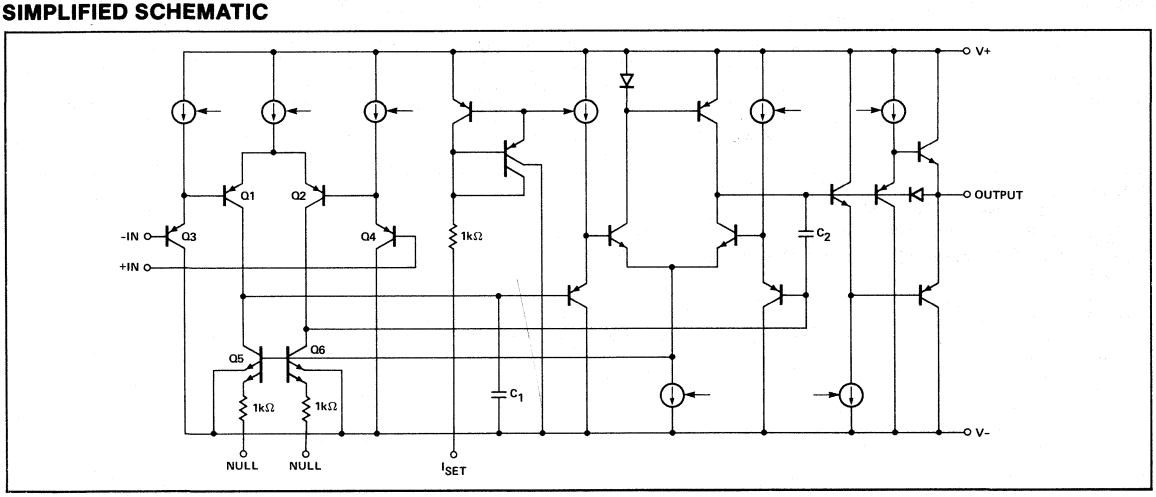


8-PIN EPOXY DIP (P-Suffix)

8-PIN HERMETIC DIP (Z-Suffix)

* DO **NOT** SHORT I_{SET} TO V– OR GROUND. SEE APPLICATIONS INFORMATION.

SIMPLIFIED SCHEMATIC



OP-32

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Differential Input Voltage ..... ±30
Input Voltage ..... Supply Voltage
Storage Temperature Range
Z Package ..... –65°C to +150°C
P Package ..... –55°C to +125°C
Operating Temperature Range
OP-32A ..... –55°C to +125°C
OP-32E, F, G ..... –25°C to +85°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature ..... –65°C to +150°C

PACKAGE TYPE	θ_{JA} (Note 2)	θ_{JC}	UNITS
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for CerDIP and P-DIP packages.

ELECTRICAL CHARACTERISTICS at $V_S = \pm1.5V$ to $\pm15V$, $15\mu A \le I_{SY} \le 450\mu A$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-32A/E MIN	OP-32A/E TYP	OP-32A/E MAX	OP-32F MIN	OP-32F TYP	OP-32F MAX	OP-32G MIN	OP-32G TYP	OP-32G MAX	UNITS
Input Offset Voltage	V_{OS}		—	100	300	—	200	500	—	400	1000	µV
Input Offset current	I_{OS}	$V_{CM} = 0$	—	—	2	—	—	2	—	—	3	nA
Input Bias Current (Note 1)	I_B	$I_{SY} = 15\mu A$	—	3	5	—	5	7.5	—	5	10	nA
		$I_{SY} = 150\mu A$	—	20	35	—	24	35	—	30	50	
		$I_{SY} = 450\mu A$	—	60	90	—	70	100	—	80	125	
Input Voltage Range	IVR	$V_S = \pm15V$	−15.0/13.5	—	—	−15.0/13.5	—	—	−15.0/13.5	—	—	V
Common-Mode Rejection Ratio (Note 2)	CMRR	$V_S = \pm15V$, $-15V \le V_{CM} \le +13.5V$	100	115	—	95	110	—	85	100	—	dB
Power Supply Rejection Ratio (Note 2)	PSRR	$V_S = \pm1.5V$ to $\pm15V$; and V− = 0V, V+ = 3V to 30V.	—	1	6	—	3	12	—	10	25	µV/V
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm15V$, $R_L = 100k\Omega$, $I_{SY} = 15\mu A$	1000	2000	—	750	1500	—	500	1000	—	V/mV
		$V_S = \pm15V$, $R_L = 10k\Omega$, $150\mu A \le I_{SY} \le 450\mu A$	1000	2000	—	750	1500	—	500	1000	—	
Output Voltage Swing	V_O	$V_S = \pm1.5V$, $R_L = 100k\Omega$, $I_{SY} = 15\mu A$	±0.8	±0.88	—	±0.8	±0.88	—	±0.75	±0.85	—	V
		$V_S = \pm1.5V$, $R_L = 10k\Omega$, $150\mu A \le I_{SY} \le 450\mu A$	±0.8	±0.88	—	±0.8	±0.88	—	±0.75	±0.85	—	
		$V_S \pm15V$, $R_L = 100k\Omega$, $I_{SY} = 15\mu A$	±14	±14.2	—	±14	±14.2	—	±13.8	±14.2	—	V
		$V_S \pm15V$, $R_L = 10k\Omega$, $150\mu A \le I_{SY} \le 450\mu A$	±14	±14.2	—	±14	±14.2	—	±13.8	±14.2	—	
Gain-Bandwidth Product		$I_{SY} = 15\mu A$, $R_L = 100k\Omega$	—	100	—	—	100	—	—	100	—	kHz
		$I_{SY} = 450\mu A$, $R_L = 10k\Omega$	—	4500	—	—	4500	—	—	4500	—	
Slew Rate	SR	$V_S = \pm15V$, $I_{SY} = 450\mu A$, $R_L = 10k\Omega$	—	1.5	—	—	1.5	—	—	1.5	—	V/µs
Supply Current No Load (Note 3)	I_{SY}	$V_S = \pm15V$, $I_{SET} = 1\mu A$	—	15	17	—	15	19	—	15	21	µA
		$I_{SET} = 10\mu A$	—	150	170	—	150	190	—	150	200	
		$I_{SET} = 30\mu A$	—	450	525	—	450	600	—	450	650	
		$V_S = \pm1.5V$, $I_{SET} = 1\mu A$	—	10.5	12.5	—	11	15	—	11	18	µA
		$I_{SET} = 10\mu A$	—	105	125	—	110	150	—	110	180	
		$I_{SET} = 30\mu A$	—	350	400	—	350	450	—	350	500	

NOTES:
1. I_B and I_{OS} are measured at $V_{CM} = 0$.
2. PSRR and CMRR measured with V_{OS} unnulled and I_{SET} held constant.
3. The supply current (I_{SY}) is dependent on the set current (I_{SET}) and supply voltage as follows:

$$\frac{I_{SY}}{I_{SET}} \approx 10 + \frac{(V+) - (V-)}{6}$$

The range of I_{SY}/I_{SET} is approximately 10.5 to 15 over the specified operating range of $V_S = \pm1.5V$ to $V_S = \pm15V$.

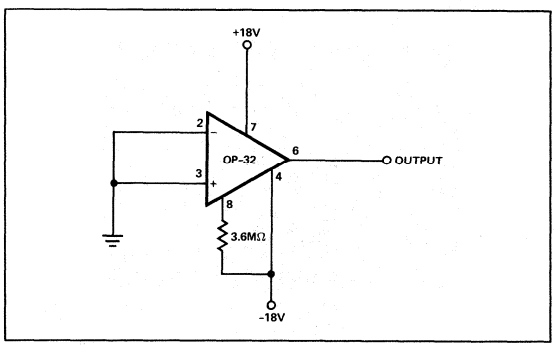
ELECTRICAL CHARACTERISTICS at $V_S = \pm1.5V$ to $\pm15V$, $15\mu A \le I_{SY} \le 450\mu A$, $-55°C \le T_A \le +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-32A MIN	OP-32A TYP	OP-32A MAX	UNITS
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	Unnulled	–	0.5	2.0	µV/°C
Input Offset Voltage	V_{OS}		–	175	400	µV
Input Offset Current	I_{OS}	$V_{CM} = 0$	–	–	2	nA
Average Input Offset Current Drift	TCI_{OS}	(Notes 1, 2)	–	1	10	pA/°C
Input Bias Current (Note 2)	I_B	$I_{SY} = 15\mu A$ $I_{SY} = 150\mu A$ $I_{SY} = 450\mu A$	– – –	3 20 60	5 35 90	nA
Input Voltage Range	IVR	$V_S = \pm15V$	−15.0/13.5	–	–	V
Common-Mode Rejection Ratio (Note 3)	CMRR	$V_S = \pm15V$ $-15V \le V_{CM} \le +13.5$ $I_{SET} = 10\mu A$ $I_{SET} = 1\mu A$	 90 80	 110 90	 – –	dB
Power Supply Rejection Ratio (Note 3)	PSRR	$V_S = \pm1.5V$ to $\pm15V$ & $V- = 0V$, $V+ = 3V$ to $30V$ ($V_{CM} = 1.5V$)	–	2	10	µV/V
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm15V$, $R_L = 100k\Omega$, $I_{SY} = 15\mu A$ $R_L = 10k\Omega$, $150\mu A \le I_{SY} \le 450\mu A$	 200 500	 400 1000	 – –	V/mV
Output Voltage Swing	V_O	$V_S = \pm1.5V$ $R_L = 100k\Omega$, $I_{SY} = 15\mu A$ $R_L = 10k\Omega$, $150\mu A \le I_{SY} \le 450\mu A$	±0.65	±0.75	–	V
		$V_S = \pm15V$ $R_L = 100k\Omega$, $I_{SY} = 15\mu A$ $R_L = 10k\Omega$, $150\mu A \le I_{SY} \le 450\mu A$	±13.6	±14.0	–	V
Supply Current No Load (Note 4)	I_{SY}	$V_S = \pm15V$ $I_{SET} = 1\mu A$ $I_{SET} = 10\mu A$ $I_{SET} = 30\mu A$	 – – –	 16 160 450	 18 180 550	µA
		$V_S = \pm1.5V$ $I_{SET} = 1\mu A$ $I_{SET} = 10\mu A$ $I_{SET} = 30\mu A$	 – – –	 12 120 360	 14 140 450	µA

NOTES:
1. Sample tested.
2. I_B and I_{OS} are measured at $V_{CM} = 0$.
3. PSRR and CMRR measured with V_{OS} unnulled and I_{SET} held constant.
4. The supply current (I_{SY}) is dependent on the set current (I_{SET}) and supply voltage as follows:

$$\frac{I_{SY}}{I_{SET}} \simeq 10 + \frac{(V+) - (V-)}{6}$$

BURN-IN CIRCUIT*



*Other circuits may apply at ADI's discretion.

OP-32

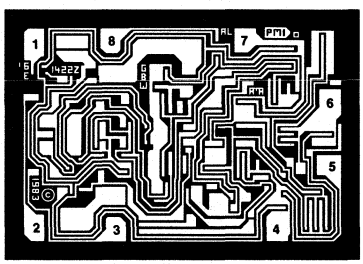
ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5V$ to $\pm 15V$, $15\mu A \le I_{SY} \le 450\mu A$, $-25°C \le T_A \le +85°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-32E MIN	OP-32E TYP	OP-32E MAX	OP-32F MIN	OP-32F TYP	OP-32F MAX	OP-32G MIN	OP-32G TYP	OP-32G MAX	UNITS
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	Unnulled	—	0.5	1.5	—	1.0	2.0	—	1.5	3.0	µV/°C
Input Offset Voltage	V_{OS}		—	100	400	—	200	600	—	500	1200	µV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	—	2	—	—	2	—	—	3	nA
Average Input Offset Current Drift	TCI_{OS}	(Notes 1, 2)	—	2	10	—	3	15	—	5	25	pA/°C
Input Bias Current (Note 2)	I_B	$I_{SY} = 15\mu A$	—	3	5	—	5	7.5	—	5	10	nA
		$I_{SY} = 150\mu A$	—	20	35	—	24	35	—	30	50	
		$I_{SY} = 450\mu A$	—	60	90	—	70	100	—	80	125	
Input Voltage Range	IVR	$V_S = \pm 15V$	−15.0/13.5	—	—	−15.0/13.5	—	—	−15.0/13.5	—	—	V
Common-Mode Rejection Ratio (Note 3)	CMRR	$V_S = \pm 15V$ & $-15V \le V_{CM} \le +13.5V$	95	110	—	90	105	—	80	100	—	dB
Power Supply Rejection Ratio (Note 3)	PSRR	$V_S = \pm 1.5V$ to $\pm 15V$ & V− = 0V, V+ = 3V to 30V	—	3.2	10	—	10	32	—	32	56	µV/V
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 100k\Omega$, $I_{SY} = 15\mu A$	750	1000	—	500	1000	—	400	1000	—	V/mV
		$R_L = 10k\Omega$, $150\mu A \le I_{SY} \le 450\mu A$	750	1000	—	500	1000	—	400	1000	—	
Output Voltage Swing	V_O	$V_S = \pm 1.5V$, $R_L = 100k\Omega$, $I_{SY} = 15\mu A$	±0.70	±0.75	—	±0.65	±0.75	—	±0.6	±0.7	—	V
		$R_L = 10k\Omega$, $150\mu A \le I_{SY} \le 450\mu A$										
		$V_S = \pm 15V$, $R_L = 100k\Omega$, $I_{SY} = 15\mu A$	±13.8	±14.1	—	±13.6	±14.1	—	±13.0	±14.0	—	V
		$R_L = 10k\Omega$, $150\mu A \le I_{SY} \le 450\mu A$										
Supply Current No Load (Note 4)	I_{SY}	$V_S = \pm 15V$, $I_{SET} = 1\mu A$	—	16	18	—	16	20	—	16	25	µA
		$I_{SET} = 10\mu A$	—	160	180	—	160	200	—	160	250	
		$I_{SET} = 30\mu A$	—	450	550	—	450	600	—	450	650	
		$V_S = \pm 1.5V$, $I_{SET} = 1\mu A$	—	12	14	—	12	17	—	12	25	µA
		$I_{SET} = 10\mu A$	—	120	140	—	120	170	—	120	200	
		$I_{SET} = 30\mu A$	—	360	450	—	360	500	—	360	550	

NOTES:
1. Sample tested.
2. I_B and I_{OS} are measured at $V_{CM} = 0$.
3. PSRR and CMRR measured with V_{OS} unnulled and I_{SET} held constant.
4. The supply current (I_{SY}) is dependent on the set current (I_{SET}) and supply voltage as follows:

$$\frac{I_{SY}}{I_{SET}} \simeq 10 + \frac{(V+) - (V-)}{6}$$

DICE CHARACTERISTICS



DIE SIZE 0.070 X 0.050 inch, 3500 sq. mils
(1.78 X 1.27 mm, 2.26 sq. mm)

1. **BALANCE**
2. **INVERTING INPUT**
3. **NONINVERTING INPUT**
4. **V–**
5. **BALANCE**
6. **OUTPUT**
7. **V+**
8. **I_{SET}**

WAFER TEST LIMITS at V_S = ±1.5V to ±15V, 15µA ≤ I_{SY} ≤ 450µA, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-32N LIMIT	OP-32G LIMIT	OP-32GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		300	500	1000	µV MAX
Input Offset Current	I_{OS}	V_{CM} = 0	2	2	3	nA MAX
Input Bias Current (Note 1)	I_B	I_{SY} = 15µA	5	7.5	10	nA MAX
		I_{SY} = 150µA	35	35	50	
		I_{SY} = 450µA	90	100	125	
Input Voltage Range	IVR	V_S = ±15V	–15/13.5	–15/13.5	–15/13.5	V MIN
Common-Mode Rejection Ratio (Note 2)	CMRR	V_S = ±15V, –15V ≤ V_{CM} ≤ +13.5V	100	95	85	dB MIN
Power Supply Rejection Ratio (Note 2)	PSRR	V_S = ±1.5V to ±15V & V– = 0V, V+ = 3V to 30V	6	12	25	µV/V MAX
Large-Signal Voltage Gain	A_{VO}	V_S = ±15V, R_L = 100kΩ, I_{SY} = 15µA	1000	750	500	V/mV MIN
		R_L = 10kΩ, 150µA ≤ I_{SY} ≤ 450µA	1000	750	500	
Output Voltage Swing	V_O	V_S = ±1.5V, R_L = 100kΩ, I_{SY} = 15µA, R_L = 100kΩ, 150µA ≤ I_{SY} ≤ 450µA	±0.8	±0.8	±0.75	V MIN
		V_S = ±15V, R_L = 100kΩ, I_{SY} = 15µA, R_L = 10kΩ, 150µA ≤ I_{SY} ≤ 450µA	±14	±14	±13.8	V MIN
Supply Current No Load (Note 3)	I_{SY}	V_S = ±1.5V, I_{SET} = 1µA	12.5	15	18	µA MAX
		I_{SET} = 10µA	125	150	180	
		I_{SET} = 30µA	400	450	500	
		V_S = ±15V, I_{SET} = 1µA	17	19	21	µA MAX
		I_{SET} = 10µA	170	190	200	
		I_{SET} = 30µA	525	600	650	

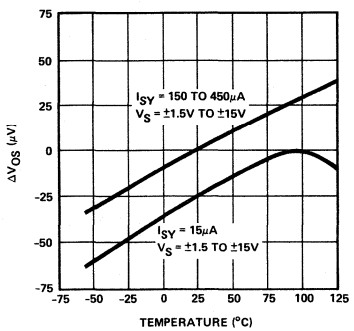
NOTES:
1. I_B and I_{OS} are measured at V_{CM} = 0.
2. PSRR and CMRR measured with V_{OS} unnulled and I_{SET} held constant.
3. The supply current (I_{SY}) is dependent on the set current (I_{SET}) and supply voltage as follows:

$$\frac{I_{SY}}{I_{SET}} \simeq 10 + \frac{(V+) - (V-)}{6}$$

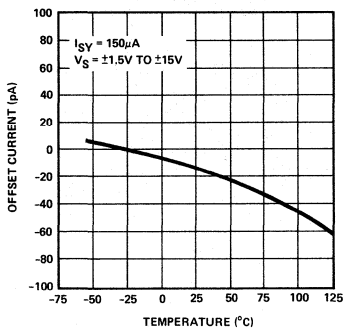
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL DC PERFORMANCE CHARACTERISTICS

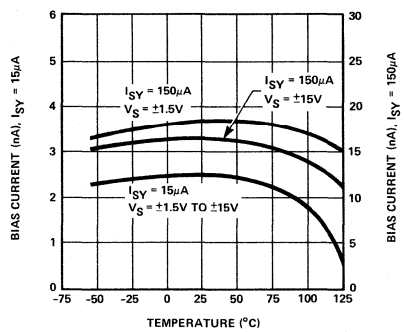
OFFSET VOLTAGE vs TEMPERATURE



OFFSET CURRENT vs TEMPERATURE



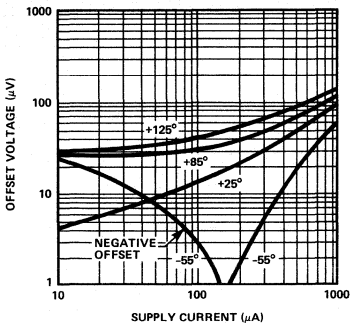
BIAS CURRENT vs TEMPERATURE



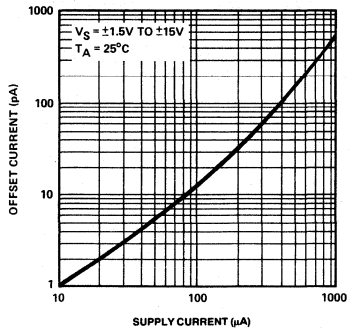
OP-32

TYPICAL DC PERFORMANCE CHARACTERISTICS

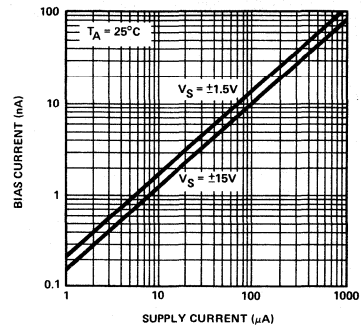
OFFSET VOLTAGE vs SUPPLY CURRENT



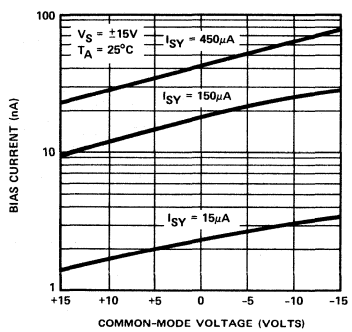
OFFSET CURRENT vs SUPPLY CURRENT



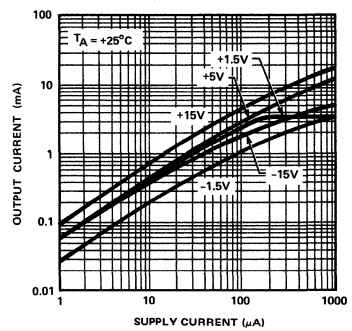
BIAS CURRENT vs SUPPLY CURRENT



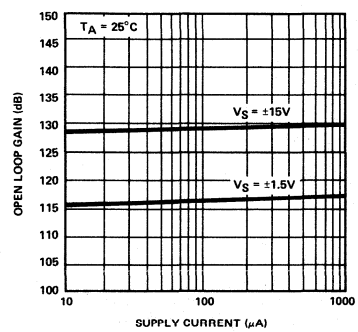
BIAS CURRENT vs COMMON-MODE VOLTAGE



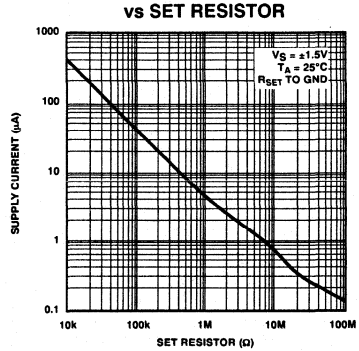
MAXIMUM OUTPUT CURRENT vs SUPPLY CURRENT AT $V_S = \pm 15V$, +5V AND ±1.5V



OPEN-LOOP GAIN vs SUPPLY CURRENT

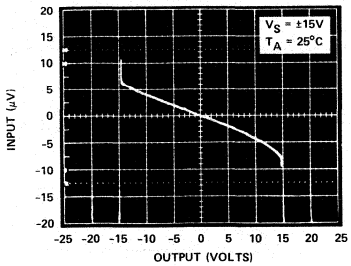


SUPPLY CURRENT vs SET RESISTOR

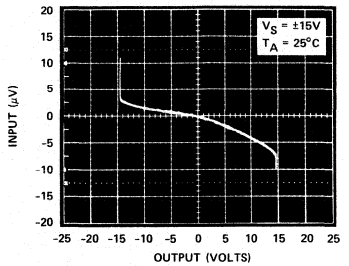


TYPICAL DC OPEN-LOOP INPUT-OUTPUT CHARACTERISTICS

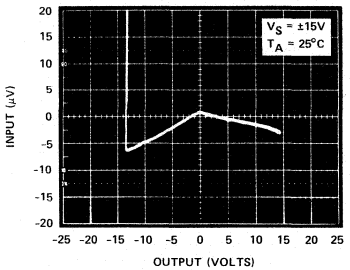
I_{SY} = 1mA, R_L = 100kΩ



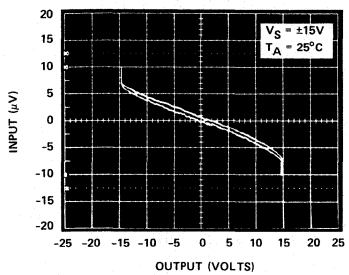
I_{SY} = 1mA, R_L = 10kΩ



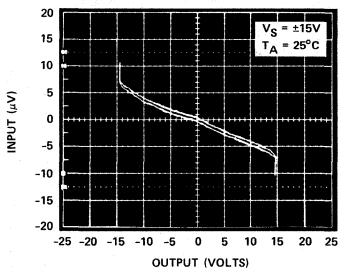
I_{SY} = 1mA, R_L = 2kΩ



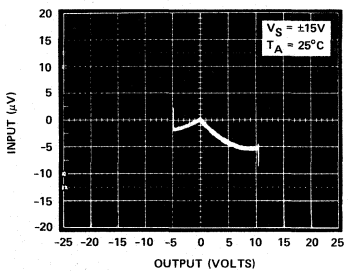
I_{SY} = 100μA, R_L = 100kΩ



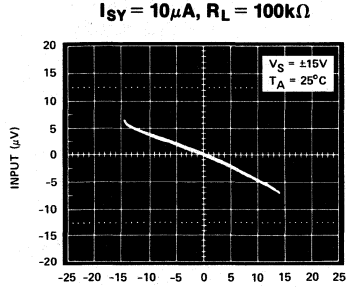
I_{SY} = 100μA, R_L = 10kΩ



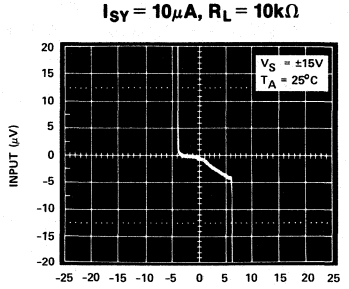
I_{SY} = 100μA, R_L = 2kΩ



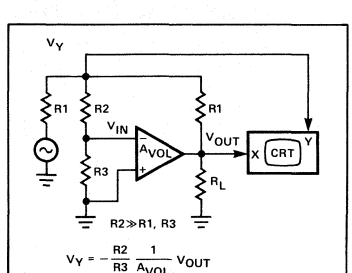
I_{SY} = 10μA, R_L = 100kΩ



I_{SY} = 10μA, R_L = 10kΩ

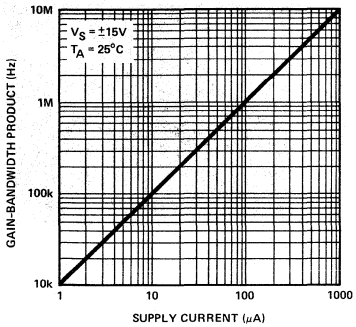


TEST CIRCUIT

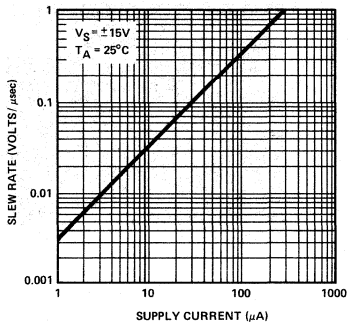


TYPICAL AC PERFORMANCE CHARACTERISTICS

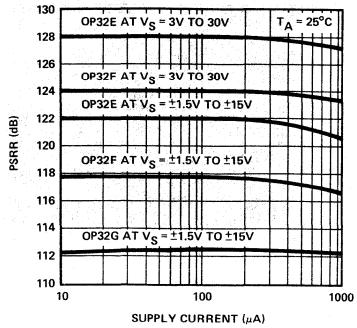
GAIN-BANDWIDTH PRODUCT vs SUPPLY CURRENT



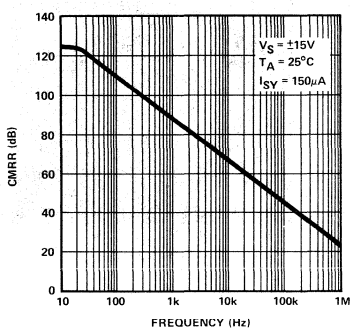
SLEW RATE vs SUPPLY CURRENT



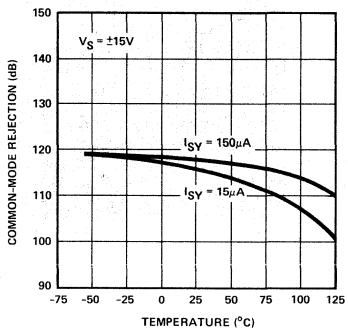
POWER SUPPLY REJECTION vs SUPPLY CURRENT



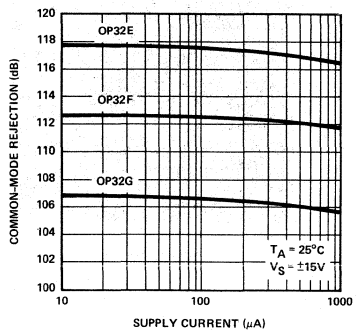
COMMON-MODE REJECTION vs FREQUENCY



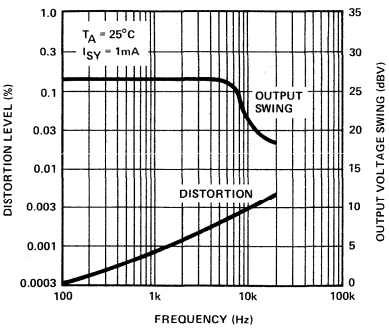
COMMON-MODE REJECTION vs TEMPERATURE



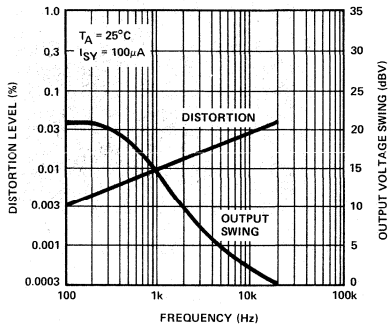
COMMON-MODE REJECTION vs SUPPLY CURRENT



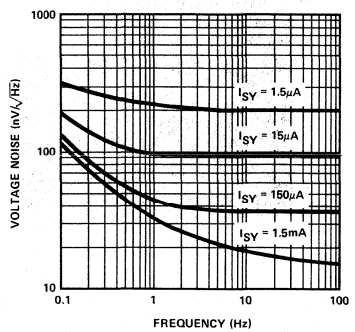
TOTAL HARMONIC DISTORTION vs FREQUENCY



TOTAL HARMONIC DISTORTION vs FREQUENCY



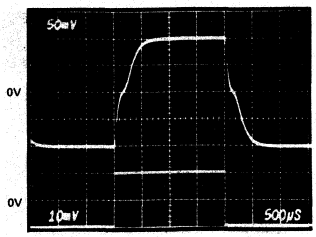
VOLTAGE NOISE vs FREQUENCY



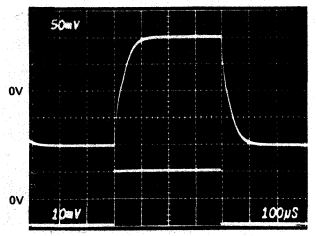
TYPICAL AC PERFORMANCE CHARACTERISTICS

SMALL-SIGNAL TRANSIENT RESPONSE vs SUPPLY CURRENT

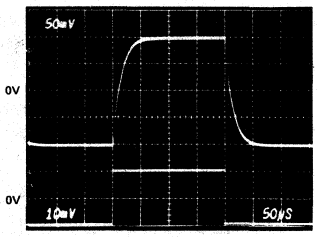
I_{SY} = 1.5μA



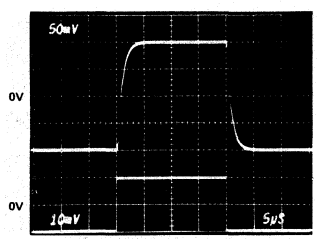
I_{SY} = 7.5μA



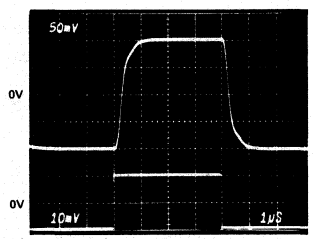
I_{SY} = 15μA



I_{SY} = 150μA

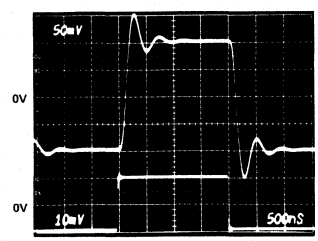


I_{SY} = 450μA

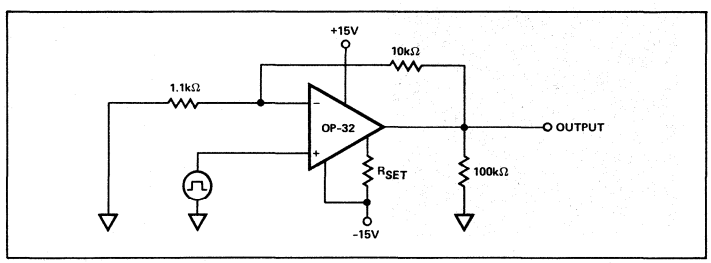


I_{SY} = 750μA

I_{SY} = 1.5mA



TEST CIRCUIT

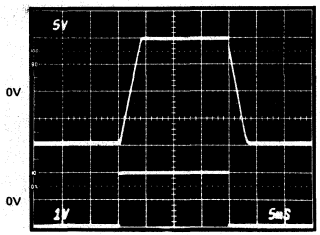


OP-32

TYPICAL AC PERFORMANCE CHARACTERISTICS

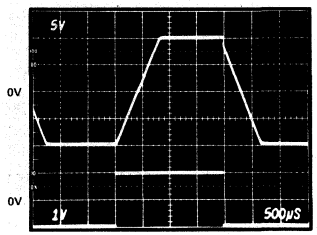
LARGE-SIGNAL TRANSIENT RESPONSE vs SUPPLY CURRENT

$I_{SY} = 1.5\mu A$



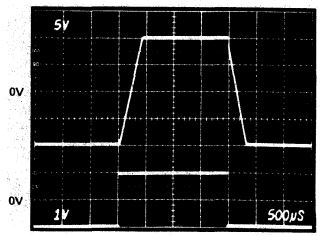
R_{F1} = 110kΩ, R_{F2} = 1MΩ, R_L = OPEN

$I_{SY} = 7.5\mu A$



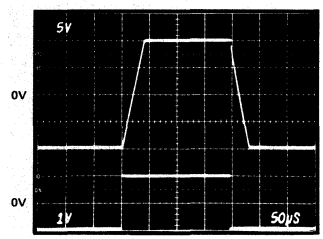
R_{F1} = 11kΩ, R_{F2} = 100kΩ, R_L = 1MΩ

$I_{SY} = 15\mu A$



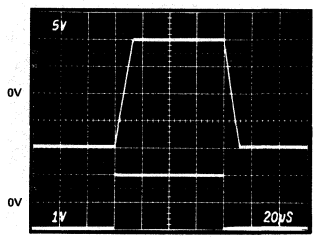
R_{F1} = 11kΩ, R_{F2} = 100kΩ, R_L = 1MΩ

$I_{SY} = 150\mu A$



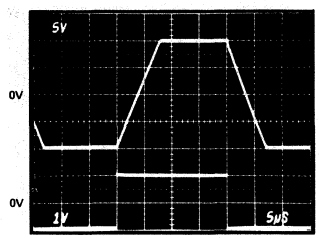
R_{F1} = 1.1kΩ, R_{F2} = 10kΩ, R_L = 100kΩ

$I_{SY} = 450\mu A$



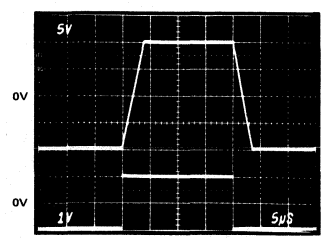
R_{F1} = 1.1kΩ, R_{F2} = 10kΩ, R_L = 100kΩ

$I_{SY} = 750\mu A$



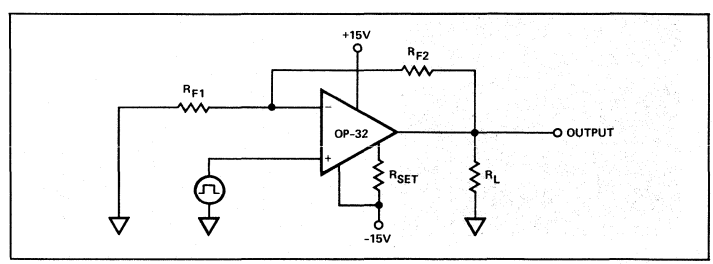
R_{F1} = 1.1kΩ, R_{F2} = 10kΩ, R_L = 100kΩ

$I_{SY} = 1.5mA$



R_{F1} = 1.1kΩ, R_{F2} = 10kΩ, R_L = 100kΩ

TEST CIRCUIT



APPLICATIONS INFORMATION

SETTING SUPPLY CURRENT

The op amp power supply current is determined by the current flowing out of pin 8. Pin 8 is at the V+ voltage less two diode drops, which is approximately V+ minus 1.1V. Do not connect pin 8 to ground or V− without a set resistor in series or excessive supply current will be drawn which may damage the OP-32.

The set resistor value is selected to make the power supply current optimum for the specific application. Adjusting the OP-32 power supply current determines the slew-rate, bandwidth, and the output current limits (see Performance Characteristics). The supply current is nominally 15 times the set current and the set resistor value is calculated from:

$$R_S = \frac{(V_{SUPPLY} - 1.1V)}{I_{SET}}, \text{ where } I_{SY} \simeq 15\, I_{SET}$$

(See graph below)

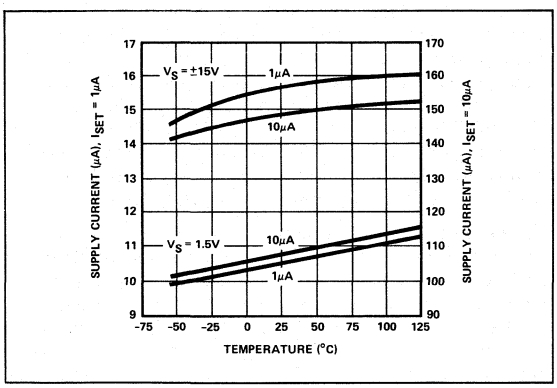
Note that the set resistor can go to either negative supply or to ground. If the set resistor goes to negative supply, then $V_{SUPPLY} = (V+) - (V-)$. For a single-supply circuit, V_{SUPPLY} is simply (V+). If the supply voltage varies widely, set current can be stabilized with circuits (a), (b), or (c).

The relationship between supply voltage, supply current and set current can be approximated by:

$$\frac{I_{SY}}{I_{SET}} \simeq 10 + \frac{(V+) - (V-)}{6} \quad (T_A = 25°C)$$

The ratio $\frac{I_{SY}}{I_{SET}}$ increases with temperature by approximately 0.05%/°C.

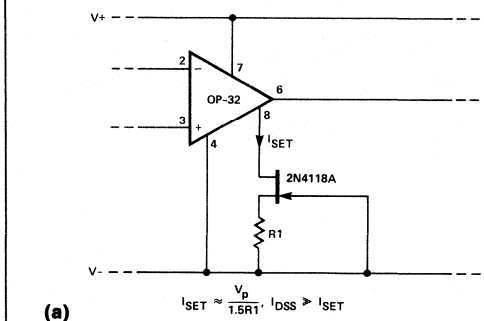
SUPPLY CURRENT vs TEMPERATURE



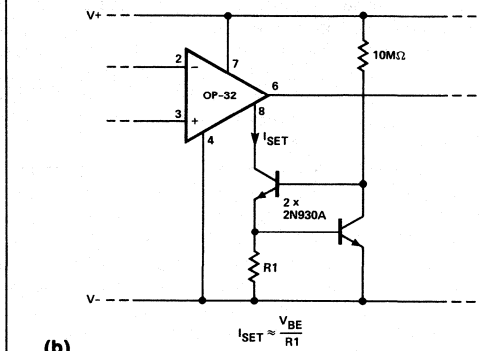
INPUT BIAS CURRENT

Input bias current varies directly with set current. The set current required for a given supply current ranges from $I_{SY}/10.5$ at ±1.5V supply voltage to $I_{SY}/15$ at ±15V. Therefore, I_B will be highest at the minimum supply voltage condition of ±1.5V (or 3V) for any given supply current.

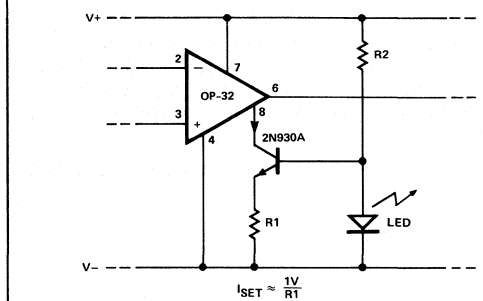
CURRENT SETTING CIRCUITS



(a) $I_{SET} \approx \frac{V_p}{1.5R1}$, $I_{DSS} \gg I_{SET}$

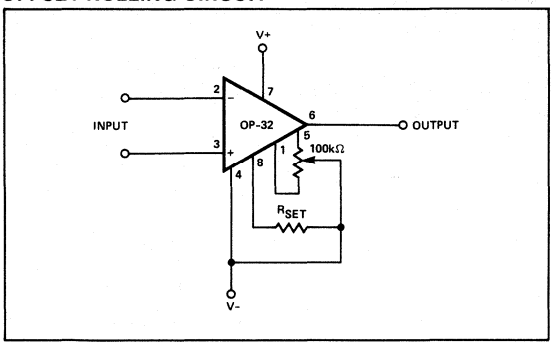


(b) $I_{SET} \approx \frac{V_{BE}}{R1}$



(c) $I_{SET} \approx \frac{1V}{R1}$

OFFSET NULLING CIRCUIT



BATTERY-POWERED, GAIN-OF-100 AMPLIFIER

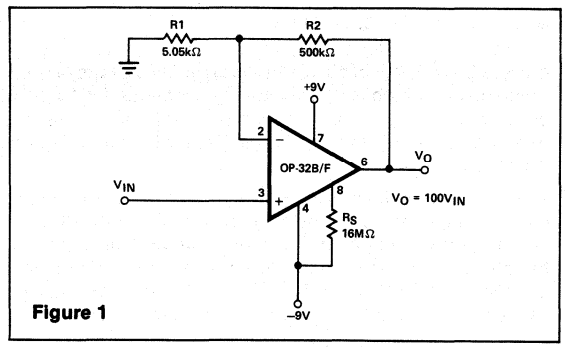


Figure 1

OFFSET VOLTAGE ADJUSTMENT

The offset voltage can be trimmed to zero using a 100kΩ potentiometer (see offset nulling circuit). Adjusting the pot wiper towards pin 5 causes the output to go positive. Adjustment range is approximately ±5mV at $V_S = \pm 15V$. The V_{OS} adjust range is proportional to supply voltage. Resolution of the nulling can be increased by using a smaller pot in conjunction with fixed resistors.

If power supply voltages vary widely and the set current is established by a resistor, the op amp supply currents will vary in proportion to the supply voltage changes. V_{OS} will remain almost constant with supply current changes if the null pins (1 and 5) are not used. If a V_{OS} adjust pot is used, current variations may flow through the offset pot causing an apparent V_{OS} change. If a V_{OS} adjust pot is used in combination with widely-varying supply voltages, a set-current stabilizer circuit as shown in (a), (b), or (c) is recommended.

APPLICATIONS EXAMPLE

BATTERY-POWERED, GAIN-OF-100 AMPLIFIER

The simple noninverting amplifier circuit shown in Figure 1 provides an accurate gain-of-100 while operating from a pair of 9V batteries. The circuit requires only 15μA of supply current. Slew-rate is approximately 0.06V/μsec and output swing is ±8V.

A value of 500kΩ was chosen for R_2. For a gain of 100, R_1 is calculated as:

$$A_{VCL} = 1 + \frac{R_2}{R_1}$$

$$100 = 1 + \frac{500k\Omega}{R_1}$$

$$\therefore R_1 = 5.05k\Omega$$

Using an OP-32B/F, we can expect an $I_B + I_{OS}/2$ of less than 8.5nA when operating at I_{SY} of 15μA, so the input offset caused by $I_B R_1$ will be negligible ($8.5nA \times 5.05k\Omega \sim 43\mu V$).

The set resistor R_S needed for a supply current of 15μA is calculated from:

$$R_S = \frac{V_{SUPPLY} - 1.1V}{I_{SY}/15} = \frac{18V - 1.1V}{1\mu A}$$

$$\therefore R_S = 16.9M\Omega$$

Offset voltage adjustment is optional. An OP-32B/F has maximum input offset voltage of 500μV which would cause an output offset voltage of 50mV. Drift over temperature is very low, typically less than 1.0μV/°C, and is guaranteed to be less than 2.0μV/°C. PSRR is also low, only 6μV/V, so battery voltage change has negligible effect on offset.

Most micropower programmable op amps lose open-loop gain and CMRR at low supply currents. The OP-32 design overcomes these limitations so accuracy is maintained at supply currents of only a few microamps. The OP-32B/F used in this example has a minimum open-loop gain of over 117dB. Gain error due to finite open-loop gain will be less than 100/750,000, which is only 133 PPM. CMRR will typically be 110dB, an error of 3 PPM. Gain accuracy of the circuit is almost entirely dependent on the accuracy of the R_1/R_2 ratio; the op amp contributes less than 0.015% gain error.

Considering all error sources, this simple ×100 battery-powered circuit using an OP-32B/F is capable of achieving excellent accuracy. Without external adjustments of any kind, output offset will be less than 54mV and gain accuracy will be better than ±0.015% (exclusive of R_2/R_1 error). Gain linearity, slew-rate symmetry, and stability over temperature are all excellent with the OP-32, making circuit performance very predictable.

ANALOG DEVICES

Low-Noise Precision High-Speed Operational Amplifier ($A_{VCL} \geq 5$)

OP-37

FEATURES

- **Low Noise** ..... **80nV p-p (0.1Hz to 10Hz)**
  ..... **3nV/$\sqrt{Hz}$ at 1kHz**
- **Low Drift** ..... **0.2μV/°C**
- **High Speed** ..... **17V/μs Slew Rate**
  ..... **63MHz Gain Bandwidth**
- **Low Input Offset Voltage** **10μV**
- **Excellent CMRR** ... **126dB (Common-Voltage of ±11V)**
- **High Open-Loop Gain** ..... **1.8 Million**
- **Replaces 725, OP-05, OP-06, OP-07, AD510, AD517, SE5534 in Gains >5**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (μV)	PACKAGE TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
25	OP37AJ*	OP37AZ*	–	–	MIL
25	OP37EJ	OP37EZ	OP37EP	–	IND/COM
60	OP37BJ*	OP37BZ*	–	OP37BRC/883	MIL
60	OP37FJ	OP37FZ	OP37FP	–	IND/COM
100	OP37CJ*	OP37CZ	–	–	MIL
100	OP37GJ	OP37GZ	OP37GP	–	XIND
100	–	–	OP37GS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO package, contact your local sales office.

GENERAL DESCRIPTION

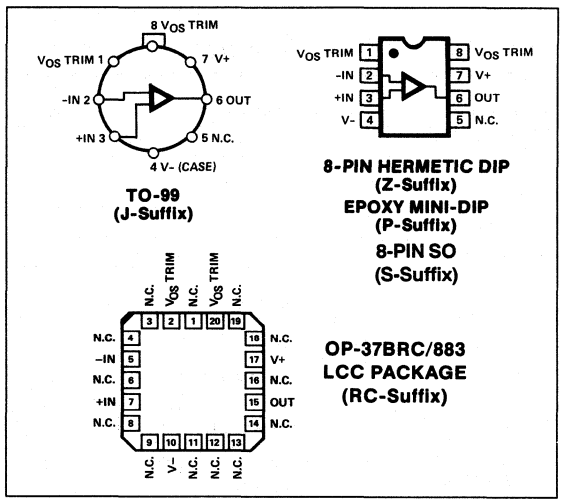
The OP-37 provides the same high performance as the OP-27, but the design is optimized for circuits with gains greater than five. This design change increases slew rate to 17V/μsec and gain-bandwidth product to 63MHz.

The OP-37 provides the low offset and drift of the OP-07 plus higher speed and lower noise. Offsets down to 25μV and drift of 0.6μV/°C maximum make the OP-37 ideal for precision instrumentation applications. Exceptionally low noise (e_n=3.5nV/$\sqrt{Hz}$ at 10Hz), a low 1/f noise corner frequency of 2.7Hz, and the high gain of 1.8 million, allow accurate high-gain amplification of low-level signals.

The low input bias current of ±10nA and offset current of 7nA are achieved by using a bias-current-cancellation circuit. Over the military temperature range this typically holds I_B and I_{OS} to ±20nA and 15nA respectively.

The output stage has good load driving capability. A guaranteed swing of ±10V into 600Ω and low output distortion make the OP-37 an excellent choice for professional audio applications.

PIN CONNECTIONS

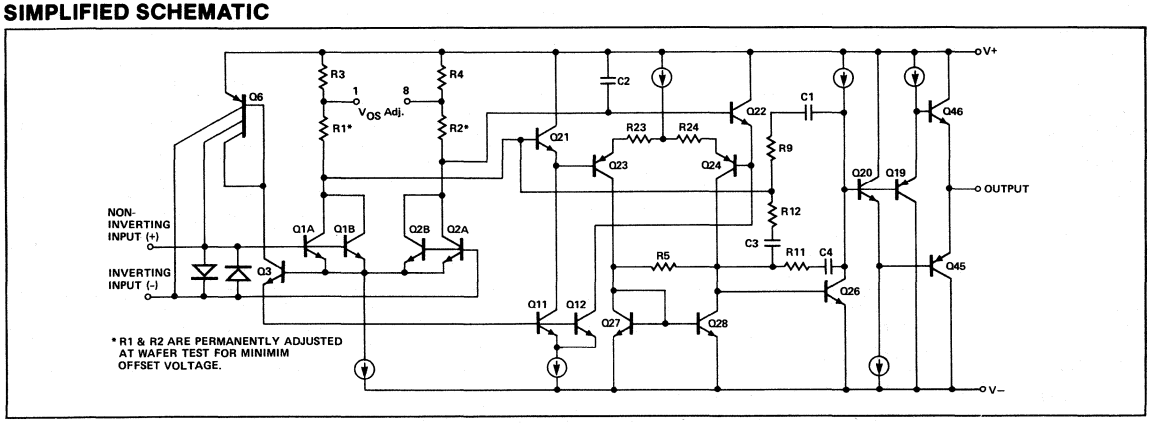


TO-99 (J-Suffix)

8-PIN HERMETIC DIP (Z-Suffix)
EPOXY MINI-DIP (P-Suffix)
8-PIN SO (S-Suffix)

OP-37BRC/883 LCC PACKAGE (RC-Suffix)

SIMPLIFIED SCHEMATIC



PSRR and CMRR exceed 120dB. These characteristics, coupled with long-term drift of 0.2μV/month, allow the circuit designer to achieve performance levels previously attained only by discrete designs.

Low-cost, high-volume production of the OP-37 is achieved by using on-chip zener-zap trimming. This reliable and stable offset trimming scheme has proved its effectiveness over many years of production history.

The OP-37 brings low-noise instrumentation-type performance to such diverse applications as microphone, tape-head, and RIAA phono preamplifiers, high-speed signal conditioning for data acquisition systems, and wide-bandwidth instrumentation.

ABSOLUTE MAXIMUM RATINGS (Note 4)

Supply Voltage ..... ±22V
Internal Voltage (Note 1) ..... ±22V
Output Short-Circuit Duration ..... Indefinite
Differential Input Voltage (Note 2) ..... ±0.7V
Differential Input Current (Note 2) ..... ±25mA
Storage Temperature Range ..... –65°C to +150°C

Operating Temperature Range
OP-37A, OP-37B, OP-37C (J, Z, RC) ..... –55°C to +125°C
OP-37E, OP-37F (J, Z) ..... –25°C to +85°C
OP-37E, OP-37F (P) ..... 0°C to +70°C
OP-37G (P, S, J, Z) ..... –40°C to +85°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature ..... –65°C to +150°C

PACKAGE TYPE	Θ_{JA} (NOTE 3)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC (RC, TC)	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
2. The OP-37's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.
4. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-37A/E			OP-37B/F			OP-37C/G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	10	25	—	20	60	—	30	100	μV
Long-Term V_{OS} Stability	V_{OS}/Time	(Notes 2, 3)	—	0.2	1.0	—	0.3	1.5	—	0.4	2.0	μV/Mo
Input Offset Current	I_{OS}		—	7	35	—	9	50	—	12	75	nA
Input Bias Current	I_B		—	±10	±40	—	±12	±55	—	±15	±80	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Notes 3, 5)	—	0.08	0.18	—	0.08	0.18	—	0.09	0.25	μVp-p
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 3)	—	3.5	5.5	—	3.5	5.5	—	3.8	8.0	nV/√Hz
		f_O = 30Hz (Note 3)	—	3.1	4.5	—	3.1	4.5	—	3.3	5.6	
		f_O = 1000Hz (Note 3)	—	3.0	3.8	—	3.0	3.8	—	3.2	4.5	
Input Noise Current Density	i_n	f_O = 10Hz (Notes 3, 6)	—	1.7	4.0	—	1.7	4.0	—	1.7	—	pA/√Hz
		f_O = 30Hz (Notes 3, 6)	—	1.0	2.3	—	1.0	2.3	—	1.0	—	
		f_O = 1000Hz (Notes 3, 6)	—	0.4	0.6	—	0.4	0.6	—	0.4	0.6	
Input Resistance — Differential-Mode	R_{IN}	(Note 7)	1.3	6	—	0.94	5	—	0.7	4	—	MΩ
Input Resistance — Common-Mode	R_{INCM}		—	3	—	—	2.5	—	—	2	—	GΩ
Input Voltage Range	IVR		±11.0	±12.3	—	±11.0	±12.3	—	±11.0	±12.3	—	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±11V	114	126	—	106	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSSR	V_S = ±4V to ±18V	—	1	10	—	1	10	—	2	20	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10V	1000	1800	—	1000	1800	—	700	1500	—	V/mV
		$R_L \geq 1k\Omega$, V_O = ±10V	800	1500	—	800	1500	—	400	1500	—	
		R_L = 600Ω, V_O = ±1V, V_S = ±4V, (Note 4)	250	700	—	250	700	—	200	500	—	
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.0	±13.8	—	±12.0	±13.8	—	±11.5	±13.5	—	V
		$R_L \geq 600\Omega$	±10.0	±11.5	—	±10.0	±11.5	—	±10.0	±11.5	—	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 4)	11	17	—	11	17	—	11	17	—	V/μs
Gain Bandwidth Prod.	GBW	f_O = 10kHz (Note 4)	45	63	—	45	63	—	45	63	—	MHz
		f_O = 1MHz	—	40	—	—	40	—	—	40	—	

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-37A/E MIN	OP-37A/E TYP	OP-37A/E MAX	OP-37B/F MIN	OP-37B/F TYP	OP-37B/F MAX	OP-37C/G MIN	OP-37C/G TYP	OP-37C/G MAX	UNITS
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	70	—	—	70	—	—	70	—	Ω
Power Consumption	P_d	$V_O = 0$	—	90	140	—	90	140	—	100	170	mW
Offset Adjustment Range		$R_P = 10k\Omega$	—	±4.0	—	—	±4.0	—	—	±4.0	—	mV

NOTES:
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E grades guaranteed fully warmed up.
2. Long-term input offset voltage stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5μV — refer to typical performance curve.
3. Sample tested.
4. Guaranteed by design.
5. See test circuit and frequency response curve for 0.1Hz to 10Hz tester.
6. See test circuit for current noise measurement.
7. Guaranteed by input bias current.

2

ELECTRICAL CHARACTERISTICS for $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-37A MIN	OP-37A TYP	OP-37A MAX	OP-37B MIN	OP-37B TYP	OP-37B MAX	OP-37C MIN	OP-37C TYP	OP-37C MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	30	60	—	50	200	—	70	300	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSn}	(Note 2) (Note 3)	—	0.2	0.6	—	0.3	1.3	—	0.4	1.8	μV/°C
Input Offset Current	I_{OS}		—	15	50	—	22	85	—	30	135	nA
Input Bias Current	I_B		—	±20	±60	—	±28	±95	—	±35	±150	nA
Input Voltage Range	IVR		±10.3	±11.5	—	±10.3	±11.5	—	±10.2	±11.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	108	122	—	100	119	—	94	116	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to ±18V	—	2	16	—	2	20	—	4	51	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	600	1200	—	500	1000	—	300	800	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±11.5	±13.5	—	±11.0	±13.2	—	±10.5	±13.0	—	V

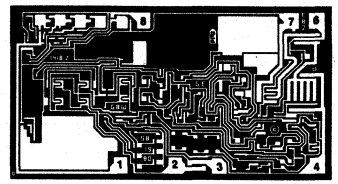
ELECTRICAL CHARACTERISTICS for $V_S = \pm 15V$, $-25°C \le T_A \le +85°C$ for OP-37EJ/FJ and OP-37EZ/FZ, $0°C \le T_A \le +70°C$ for OP-37EP/FP and $-40°C \le T_A \le +85°$ for OP-37GP/GS/GJ/GZ, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-37E MIN	OP-37E TYP	OP-37E MAX	OP-37F MIN	OP-37F TYP	OP-37F MAX	OP-37G MIN	OP-37G TYP	OP-37G MAX	UNITS
Input Offset Voltage	V_{OS}		—	20	50	—	40	140	—	55	220	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSn}	(Note 2) (Note 3)	—	0.2	0.6	—	0.3	1.3	—	0.4	1.8	μV/°C
Input Offset Current	I_{OS}		—	10	50	—	14	85	—	20	135	nA
Input Bias Current	I_B		—	±14	±60	—	±18	±95	—	±25	±150	nA
Input Voltage Range	IVR		±10.5	±11.8	—	±10.5	±11.8	—	±10.5	±11.8	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	110	124	—	102	121	—	96	118	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to ±18V	—	2	15	—	2	16	—	2	32	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	750	1500	—	700	1300	—	450	1000	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±11.7	±13.6	—	±11.4	±13.5	—	±11.0	±13.3	—	V

NOTES:
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E grades guaranteed fully warmed up.
2. The TCV_{OS} performance is within the specifications unnulled or when nulled with $R_P = 8k\Omega$ to $20k\Omega$. TCV_{OS} is 100% tested for A/E grades, sample tested for B/C/F/G grades.
3. Guaranteed by design.

DICE CHARACTERISTICS

DIE SIZE 0.098 × 0.056 inch, 5488 sq. mils
(2.49 × 1.42 mm, 3.54 sq. mm)



1. NULL
2. (–) INPUT
3. (+) INPUT
4. V–
6. OUTPUT
7. V+
8. NULL

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$ for OP-37N, OP-37G and OP-37GR devices; $T_A = 125°C$ for OP-37NT and OP-37GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-37NT LIMIT	OP-37N LIMIT	OP-37GT LIMIT	OP-37G LIMIT	OP-37GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	60	35	200	60	100	µV MAX
Input Offset Current	I_{OS}		50	35	85	50	75	nA MAX
Input Bias Current	I_B		±60	±40	±95	±55	±80	nA MAX
Input Voltage Range	IVR		±10.3	±11	±10.3	±11	±11	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 11V$	108	114	100	106	100	dB MIN
Power Supply Rejection Ratio	PSRR	$T_A = 25°C$, $V_S = \pm 4V$ to $\pm 18V$ $T_A = 125°C$, $V_S = \pm 4.5V$ to $\pm 18V$	10 16	10 —	10 20	10 —	20 —	µV/V MAX
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$ $R_L \geq 1k\Omega$, $V_O = \pm 10V$	600 —	1000 800	500 —	1000 800	700 —	V/mV MIN
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$ $R_L \geq 600\Omega$	±11.5 —	±12.0 ±10.0	±11.0 —	±12.0 ±10.0	±11.5 ±10.0	V MIN
Power Consumption	P_d	$V_O = 0$	—	140	—	140	170	mW MAX

NOTES:
For 25°C characteristics of OP-37NT and OP-37GT devices, see OP-37N and OP-37G characteristics, respectively.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot asembly and testing.

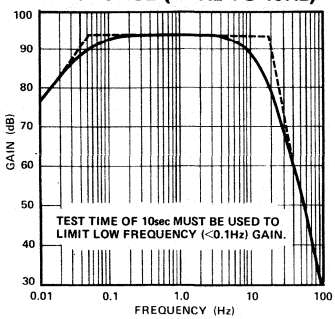
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-37NT TYPICAL	OP-37N TYPICAL	OP-37GT TYPICAL	OP-37G TYPICAL	OP-37GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS} or TCV_{OSn}	Nulled or Unnulled $R_P = 8k\Omega$ to $20k\Omega$	0.2	0.2	0.3	0.3	0.4	µV/°C
Average Input Offset Current Drift	TCI_{OS}		80	80	130	130	180	pA/°C
Average Input Bias Current Drift	TCI_B		100	100	160	160	200	pA/°C
Input Noise Voltage Density	e_n	$f_O = 10Hz$ $f_O = 30Hz$ $f_O = 1000Hz$	3.5 3.1 3.0	3.5 3.1 3.0	3.5 3.1 3.0	3.5 3.1 3.0	3.8 3.3 3.2	$nV/\sqrt{Hz}$
Input Noise Current Density	i_n	$f_O = 10Hz$ $f_O = 30Hz$ $f_O = 1000Hz$	1.7 1.0 0.4	1.7 1.0 0.4	1.7 1.0 0.4	1.7 1.0 0.4	1.7 1.0 0.4	$pA/\sqrt{Hz}$
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	0.08	0.08	0.08	0.08	0.09	μV_{P-P}
Slew Rate	SR	$R_L \geq 2k\Omega$	17	17	17	17	17	V/µs
Gain Bandwidth Product	GBW	$f_O = 10kHz$	63	63	63	63	63	MHz

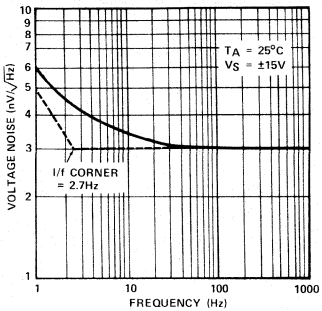
NOTE:
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

TYPICAL PERFORMANCE CHARACTERISTICS

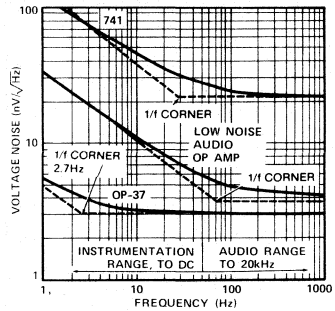
NOISE-TESTER FREQUENCY RESPONSE (0.1Hz TO 10Hz)



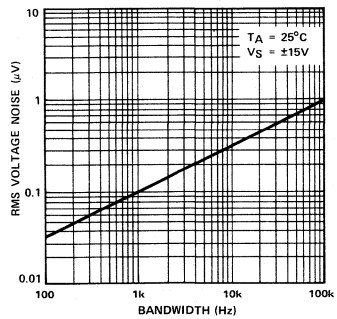
VOLTAGE NOISE DENSITY vs FREQUENCY



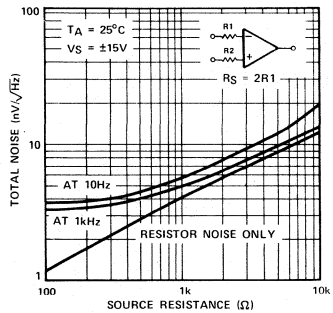
A COMPARISON OF OP AMP VOLTAGE NOISE SPECTRA



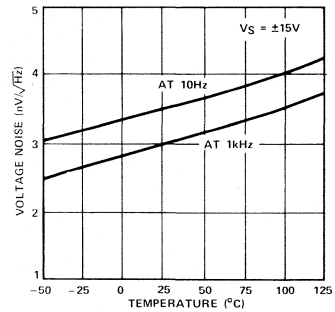
INPUT WIDEBAND VOLTAGE NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



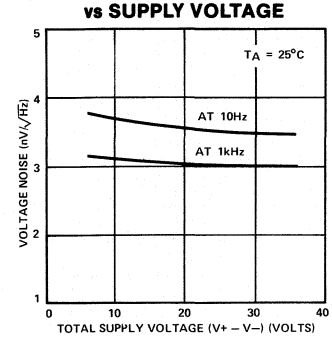
TOTAL NOISE vs SOURCE RESISTANCE



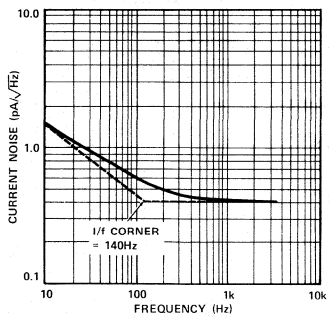
VOLTAGE NOISE DENSITY vs TEMPERATURE



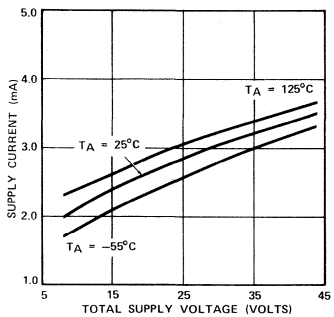
VOLTAGE NOISE DENSITY vs SUPPLY VOLTAGE



CURRENT NOISE DENSITY vs FREQUENCY

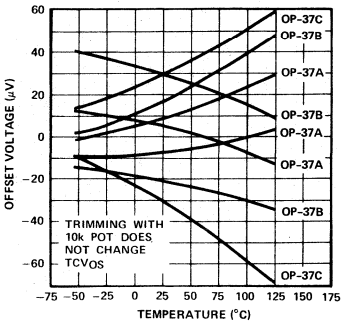


SUPPLY CURRENT vs SUPPLY VOLTAGE

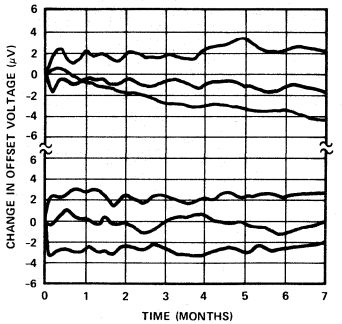


TYPICAL PERFORMANCE CHARACTERISTICS

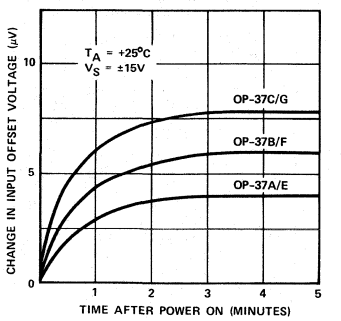
OFFSET VOLTAGE DRIFT OF EIGHT REPRESENTATIVE UNITS vs TEMPERATURE



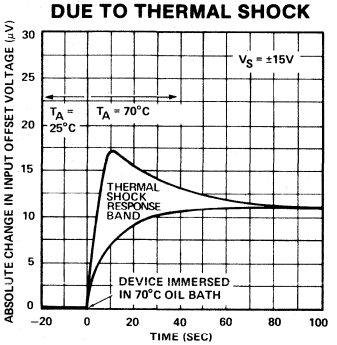
LONG-TERM OFFSET VOLTAGE DRIFT OF SIX REPRESENTATIVE UNITS



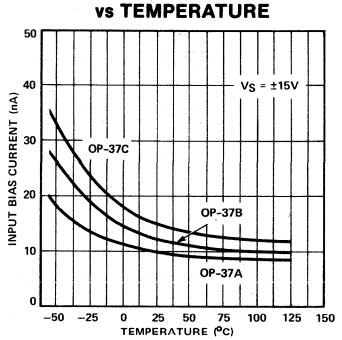
WARM-UP OFFSET VOLTAGE DRIFT



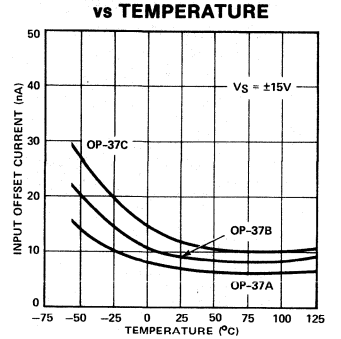
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



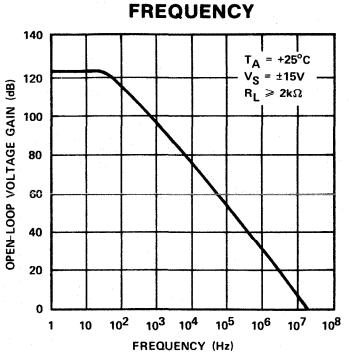
INPUT BIAS CURRENT vs TEMPERATURE



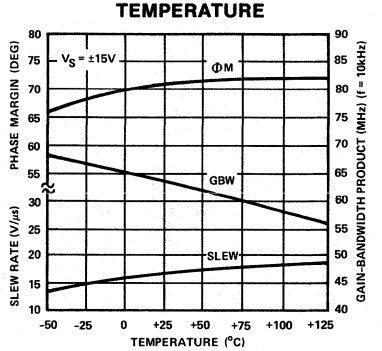
INPUT OFFSET CURRENT vs TEMPERATURE



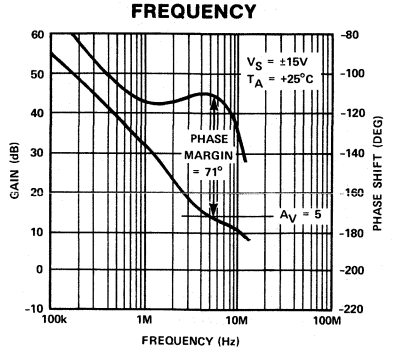
OPEN-LOOP GAIN vs FREQUENCY



SLEW RATE, GAIN BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE

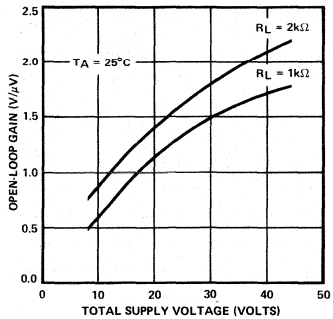


GAIN, PHASE SHIFT vs FREQUENCY

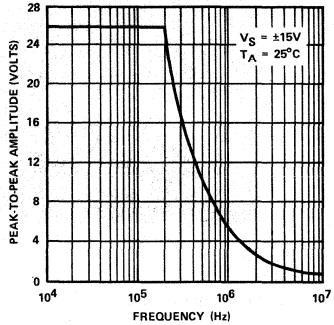


TYPICAL PERFORMANCE CHARACTERISTICS

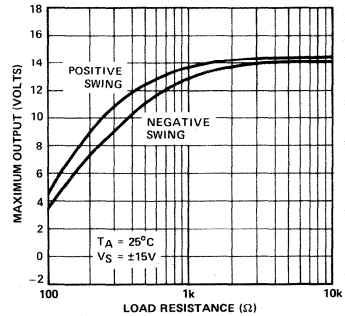
OPEN-LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE



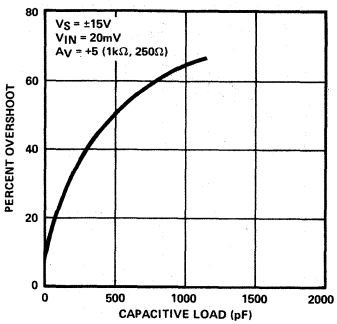
MAXIMUM OUTPUT SWING vs FREQUENCY



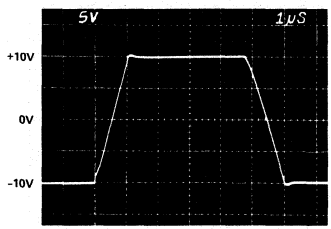
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD

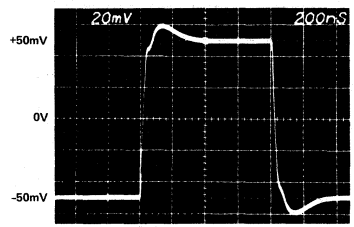


LARGE-SIGNAL TRANSIENT RESPONSE



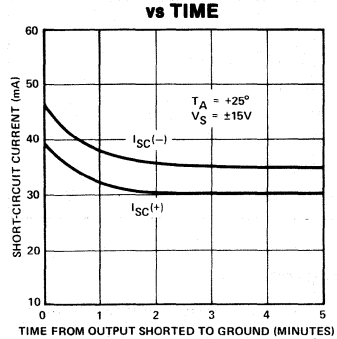
VS = ±15V
AV = +5 (1kΩ, 250Ω)
TA = +25°C

SMALL-SIGNAL TRANSIENT RESPONSE

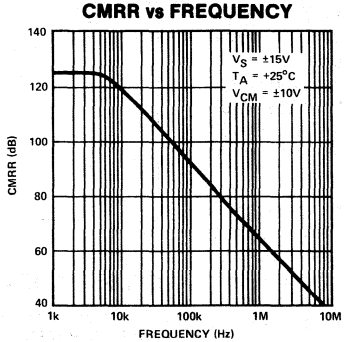


VS = ±15V
AV = +5 (1kΩ, 250Ω)
TA = +25°C

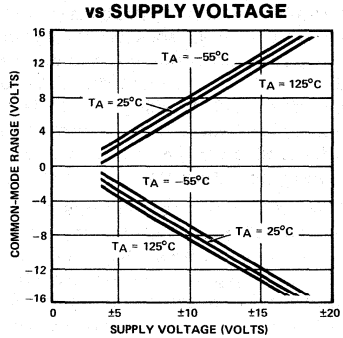
SHORT-CIRCUIT CURRENT vs TIME



CMRR vs FREQUENCY

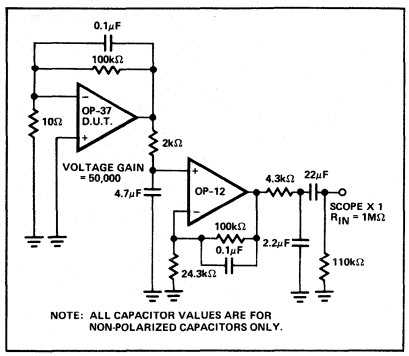


COMMON-MODE INPUT RANGE vs SUPPLY VOLTAGE

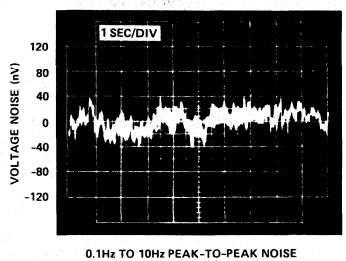


TYPICAL PERFORMANCE CHARACTERISTICS

NOISE TEST CIRCUIT (0.1Hz TO 10Hz)



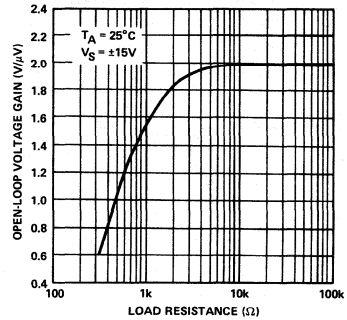
LOW-FREQUENCY NOISE



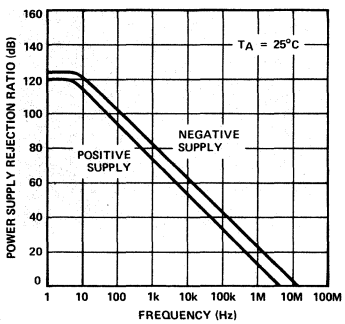
0.1Hz TO 10Hz PEAK-TO-PEAK NOISE

NOTE:
Observation time limited to 10 seconds.

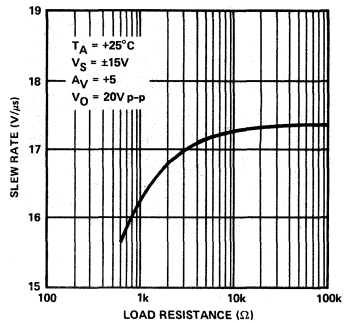
OPEN-LOOP VOLTAGE GAIN vs LOAD RESISTANCE



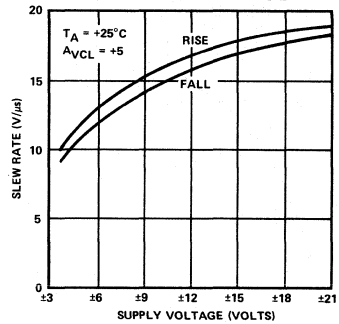
PSRR vs FREQUENCY



SLEW RATE vs LOAD



SLEW RATE vs SUPPLY VOLTAGE



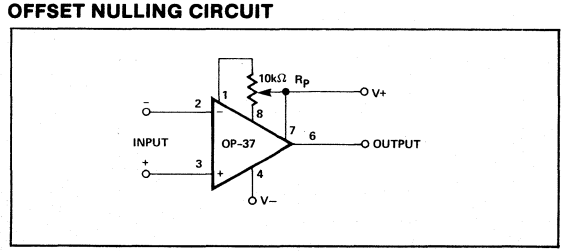
APPLICATIONS INFORMATION

OP-37 Series units may be inserted directly into 725, OP-06, OP-07, and OP-05 sockets with or without removal of external compensation or nulling components. Additionally, the OP-37 may be fitted to unnulled 741-type sockets; however, if conventional 741 nulling circuitry is in use, it should be modified or removed to ensure correct OP-37 operation. OP-37 offset voltage may be nulled to zero (or other desired setting) using a potentiometer (see offset nulling circuit).

The OP-37 provides stable operation with load capacitances of up to 1000pF and ± 10V swings; larger capacitances should be decoupled with a 50Ω resistor inside the feedback loop. Closed-loop gain must be at least five. For closed-loop gain between five to ten, the designer should consider both the OP-27 and the OP-37. For gains above ten, the OP-37 has a clear advantage over the unity-gain-stable OP-27.

Thermoelectric voltages generated by dissimilar metals at the input terminal contacts can degrade the drift performance. Best operation will be obtained when both input contacts are maintained at the same temperature.

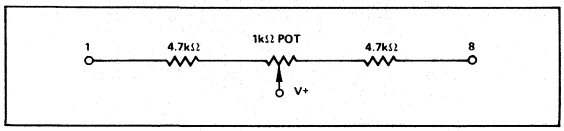
OFFSET NULLING CIRCUIT



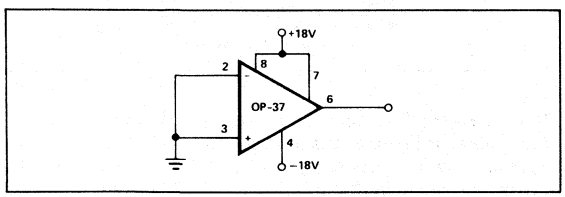
OFFSET VOLTAGE ADJUSTMENT

The input offset voltage of the OP-37 is trimmed at wafer level. However, if further adjustment of V_{OS} is necessary, a 10kΩ trim potentiometer may be used. TCV_{OS} is not degraded (see offset nulling circuit). Other potentiometer values from 1kΩ to 1MΩ can be used with a slight degradation (0.1 to 0.2μV/°C) of TCV_{OS}. Trimming to a value other than zero creates a drift of approximately (V_{OS}/300) μV/°C. For exam-

ple, the change in TCV_{OS} will be 0.33μV/° C if V_{OS} is adjusted to 100μV. The offset-voltage adjustment range with a 10kΩ potentiometer is ±4mV. If smaller adjustment range is required, the nulling sensitivity can be reduced by using a smaller pot in conjunction with fixed resistors. For example, the network below will have a ±280μV adjustment range.



BURN-IN CIRCUIT



NOISE MEASUREMENTS

To measure the 80nV peak-to-peak noise specification of the OP-37 in the 0.1Hz to 10Hz range, the following precautions must be observed:

(1) The device has to be warmed-up for at least five minutes. As shown in the warm-up drift curve, the offset voltage typically changes 4μV due to increasing chip temperature after power-up. In the 10 second measurement interval, these temperature-induced effects can exceed tens-of- nanovolts.

(2) For similar reasons, the device has to be well-shielded from air currents. Shielding minimizes thermocouple effects.

(3) Sudden motion in the vicinity of the device can also "feed-through" to increase the observed noise.

(4) The test time to measure 0.1Hz-to-10Hz noise should not exceed 10 seconds. As shown in the noise-tester frequency response curve, the 0.1Hz corner is defined by only one zero. The test time of 10 seconds acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

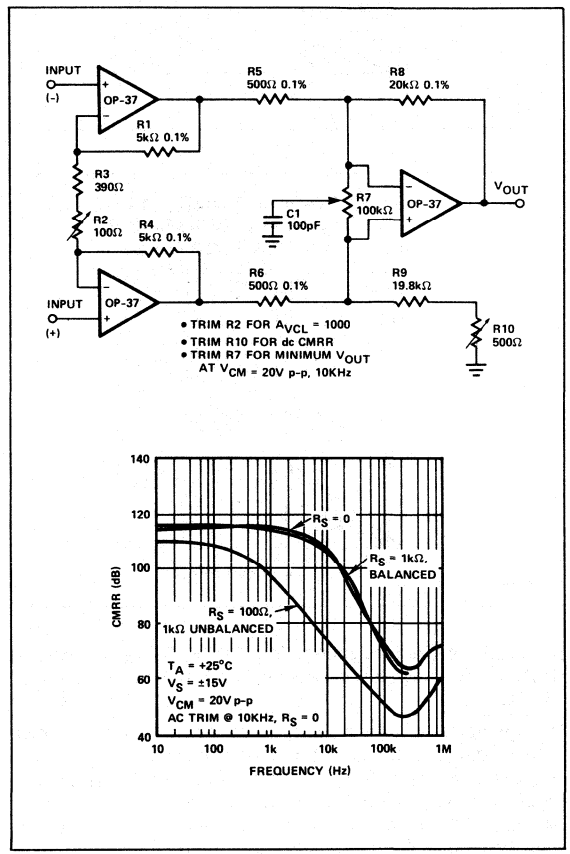
(5) A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage-density measurement will correlate well with a 0.1Hz-to-10Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the 1/f corner frequency.

OPTIMIZING LINEARITY

Best linearity will be obtained by designing for the minimum output current required for the application. High gain and excellent linearity can be achieved by operating the op amp with a peak output current of less than ±10mA.

INSTRUMENTATION AMPLIFIER

A three-op-amp instrumentation amplifier provides high gain and wide bandwidth. The input noise of the circuit below is $4.9nV/\sqrt{Hz}$. The gain of the input stage is set at 25 and the gain of the second stage is 40; overall gain is 1000. The amplifier bandwidth of 800kHz is extraordinarily good for a precision instrumentation amplifier. Set to a gain of 1000, this yields a gain-bandwidth product of 800MHz. The full-power bandwidth for a $20V_{p-p}$ output is 250kHz. Potentiometer R7 provides quadrature trimming to optimize the instrumentation amplifier's AC common-mode rejection.



COMMENTS ON NOISE

The OP-37 is a very low-noise monolithic op amp. The outstanding input voltage noise characteristics of the OP-37 are achieved mainly by operating the input stage at a high quiescent current. The input bias and offset currents, which would normally increase, are held to reasonable values by the input-bias-current cancellation circuit. The OP-37A/E has I_B and I_{OS} of only ±40nA and 35nA respectively at 25° C. This is particularly important when the input has a high source-resistance. In addition, many audio amplifier designers

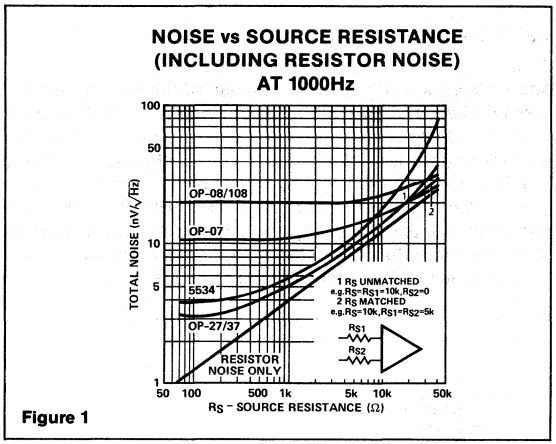


Figure 1

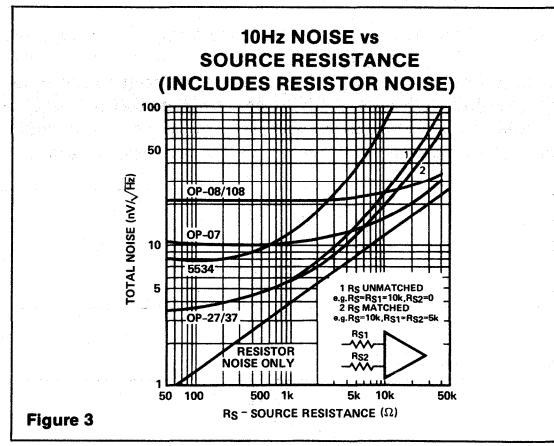


Figure 3

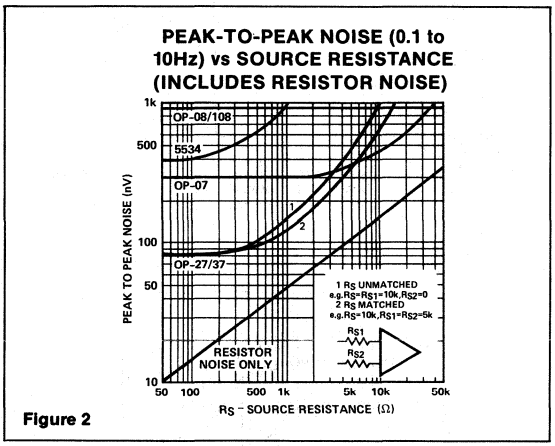


Figure 2

prefer to use direct coupling. The high I_B, TCV_{OS} of previous designs have made direct coupling difficult, if not impossible, to use.

Voltage noise is inversely proportional to the square-root of bias current, but current noise is proportional to the square-root of bias current. The OP-37's noise advantage disappears when high source-resistors are used. Figures 1, 2, and 3 compare OP-37 observed total noise with the noise performance of other devices in different circuit applications.

Total noise = $[(\text{Voltage noise})^2 + (\text{current noise} \times R_S)^2 + (\text{resistor noise}^2\ ]^{1/2}$

Figure 1 shows noise-versus-source-resistance at 1000Hz. The same plot applies to wideband noise. To use this plot, just multiply the vertical scale by the square-root of the bandwidth.

At R_S<1kΩ, the OP-37's low voltage noise is maintained. With R_S< 1kΩ, total noise increases, but is dominated by the resistor noise rather than current or voltage noise. It is only beyond R_S of 20kΩ that current noise starts to dominate. The argument can be made that current noise is not important for applications with low-to-moderate source resistances. The crossover between the OP-37 and OP-07 and OP-08 noise occurs in the 15-to-40kΩ region.

Figure 2 shows the 0.1Hz-to-10Hz peak-to-peak noise. Here the picture is less favorable; resistor noise is negligible, current noise becomes important because it is inversely proportional to the square-root of frequency. The crossover with the OP-07 occurs in the 3-to 5kΩ range depending on whether balanced or unbalanced source resistors are used (at 3kΩ the I_B, I_{OS} error also can be three times the V_{OS} spec.).

Therefore, for low-frequency applications, the OP-07 is better than the OP-27/37 when R_S > 3kΩ. The only exception is when gain error is important. Figure 3 illustrates the 10Hz noise. As expected, the results are between the previous two figures.

For reference, typical source resistances of some signal sources are listed in Table 1.

Table 1

DEVICE	SOURCE IMPEDANCE	COMMENTS
Strain gauge	<500Ω	Typically used in low-frequency applications.
Magnetic tapehead	<1500Ω	Low I_B very important to reduce self-magnetization problems when direct coupling is used. OP-37 I_B can be neglected.
Magnetic phonograph cartridges	<1500Ω	Similar need for low I_B in direct coupled applications. OP-37 will not introduce any self-magnetization problem.
Linear variable differential transformer	<1500Ω	Used in rugged servo-feedback applications. Bandwidth of interest is 400Hz to 5kHz.

AUDIO APPLICATIONS

The following applications information has been abstracted from a PMI article in the 12/20/80 issue of Electronic Design magazine and updated.

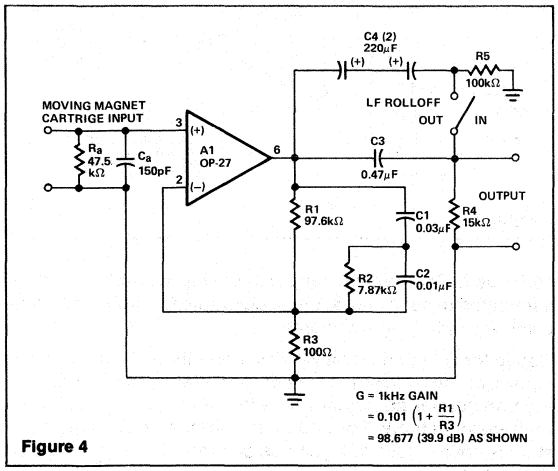


Figure 4

Figure 4 is an example of a phono pre-amplifier circuit using the OP-27 for A_1; R_1-R_2-C_1-C_2 form a very accurate RIAA network with standard component values. The popular method to accomplish RIAA phono equalization is to employ frequency-dependent feedback around a high-quality gain block. Properly chosen, an RC network can provide the three necessary time constants of 3180, 318, and 75μs.[1]

For initial equalization accuracy and stability, precision metal-film resistors and film capacitors of polystyrene or polypropylene are recommended since they have low voltage coefficients, dissipation factors, and dielectric absorption.[4] (High-K ceramic capacitors should be avoided here, though low-K ceramics—such as NPO types, which have excellent dissipation factors, and somewhat lower dielectric absorption — can be considered for small values or where space is at a premium.)

The OP-27 brings a $3.2nV/\sqrt{Hz}$ voltage noise and 0.45 $pA/\sqrt{Hz}$ current noise to this circuit. To minimize noise from other sources, R_3 is set to a value of 100Ω, which generates a voltage noise of $1.3nV/\sqrt{Hz}$. The noise increases the $3.2nV/\sqrt{Hz}$ of the amplifier by only 0.7dB. With a 1kΩ source, the circuit noise measures 63dB below a 1mV reference level, unweighted, in a 20kHz noise bandwidth.

Gain (G) of the circuit at 1kHz can be calculated by the expression:

$$G = 0.101\ (1 + \frac{R_1}{R_3})$$

For the values shown, the gain is just under 100 (or 40dB). Lower gains can be accommodated by increasing R_3, but gains higher than 40dB will show more equalization errors because of the 8MHz gain-bandwidth of the OP-27.

This circuit is capable of very low distortion over its entire range, generally below 0.01% at levels up to 7V rms. At 3V output levels, it will produce less than 0.03% total harmonic distortion at frequencies up to 20kHz.

Capacitor C_3 and resistor R_4 form a simple −6dB-per-octave rumble filter, with a corner at 22Hz. As an option, the switch-selected shunt capacitor C_4, a nonpolarized electrolytic, bypasses the low-frequency rolloff. Placing the rumble filter's high-pass action after the preamp has the desirable result of discriminating against the RIAA-amplified low-frequency noise components and pickup-produced low-frequency disturbances.

A preamplifier for NAB tape playback is similar to an RIAA phono preamp, though more gain is typically demanded, along with equalization requiring a heavy low-frequency boost. The circuit in Fig. 4 can be readily modified for tape use, as shown by Fig. 5.

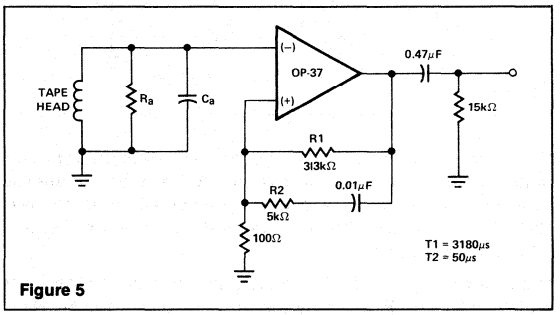


Figure 5

While the tape-equalization requirement has a flat high-frequency gain above 3kHz ($T_2 = 50\mu s$), the amplifier need not be stabilized for unity gain. The decompensated OP-37 provides a greater bandwidth and slew rate. For many applications, the idealized time constants shown may require trimming of R_1 and R_2 to optimize frequency response for nonideal tape-head performance and other factors.[5]

The network values of the configuration yield a 50dB gain at 1kHz, and the dc gain is greater than 70dB. Thus, the worst-case output offset is just over 500mV. A single 0.47μF output capacitor can block this level without affecting the dynamic range.

The tape head can be coupled directly to the amplifier input, since the worst-case bias current of 85nA with a 400mH, 100 μin. head (such as the PRB2H7K) will not be troublesome.

One potential tape-head problem is presented by amplifier bias-current transients which can magnetize a head. The OP-27 and OP-37 are free of bias-current transients upon power up or power down. However, it is always advantageous to control the speed of power supply rise and fall, to eliminate transients.

In addition, the dc resistance of the head should be carefully controlled, and preferably below 1kΩ. For this configuration, the bias-current-induced offset voltage can be greater than the 170μV maximum offset if the head resistance is not sufficiently controlled.

A simple, but effective, fixed-gain transformerless microphone preamp (Fig. 6) amplifies differential signals from low-impedance microphones by 50dB, and has an input impedance of 2kΩ. Because of the high working gain of the circuit, an OP-37 helps to preserve bandwidth, which will be 110kHz. As the OP-37 is a decompensated device (minimum stable gain of 5), a dummy resistor, R_p, may be necessary, if the microphone is to be unplugged. Otherwise the 100% feedback from the open input may cause the amplifier to oscillate.

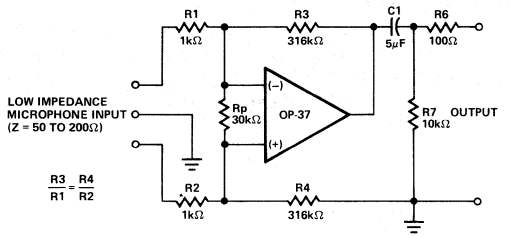


Figure 6

Common-mode input-noise rejection will depend upon the match of the bridge-resistor ratios. Either close-tolerance (0.1%) types should be used, or R_4 should be trimmed for best CMRR. All resistors should be metal-film types for best stability and low noise.

Noise performance of this circuit is limited more by the input resistors R_1 and R_2 than by the op amp, as R_1 and R_2 each generate a $4nV/\sqrt{Hz}$ noise, while the op amp generates a $3.2nV/\sqrt{Hz}$ noise. The rms sum of these predominant noise sources will be about $6nV/\sqrt{Hz}$, equivalent to 0.9μV in a 20kHz noise bandwidth, or nearly 61dB below a 1mV input signal. Measurements confirm this predicted performance.

For applications demanding appreciably lower noise, a high-quality microphone-transformer-coupled preamp (Fig. 7) incorporates the internally compensated OP-27. T_1 is a JE-115K-E 150Ω/15kΩ transformer which provides an optimum source resistance for the OP-27 device. The circuit has an overall gain of 40dB, the product of the transformer's voltage setup and the op amp's voltage gain.

Gain may be trimmed to other levels, if desired, by adjusting R_2 or R_1. Because of the low offset voltage of the OP-27, the output offset of this circuit will be very low, 1.7mV or less, for a

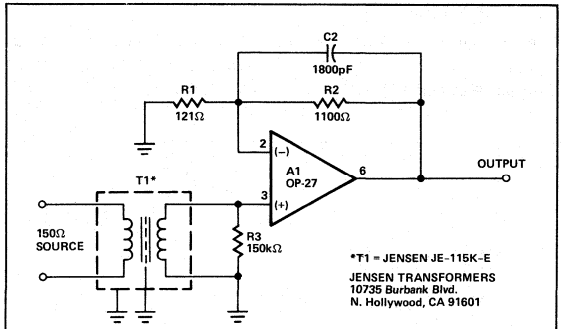


Figure 7

40dB gain. The typical output blocking capacitor can be eliminated in such cases, but is desirable for higher gains to eliminate switching transients.

Capacitor C_2 and resistor R_2 form a 2μs time constant in this circuit, as recommended for optimum transient response by the transformer manufacturer. With C_2 in use, A_1 must have unity-gain stability. For situations where the 2μs time constant is not necessary, C_2 can be deleted, allowing the faster OP-37 to be employed.

Some comment on noise is appropriate to understand the capability of this circuit. A 150Ω resistor and R_1 and R_2 gain resistors connected to a noiseless amplifier will generate 220 nV of noise in a 20kHz bandwidth, or 73dB below a 1mV reference level. Any practical amplifier can only approach this noise level; it can never exceed it. With the OP-27 and T_1 specified, the additional noise degradation will be close to 3.6dB (or −69.5 referenced to 1mV).

References

1. Lipshitz, S.P., "On RIAA Equalization Networks," *JAES*, Vol. 27, June 1979, p. 458-481.
2. Jung, W.G., *IC Op Amp Cookbook*, 2nd Ed., H.W. Sams and Company, 1980.
3. Jung, W.G., *Audio IC Op Amp Applications*, 2nd Ed., H.W. Sams and Company, 1978.
4. Jung, W.G., and Marsh, R.M., "Picking Capacitors," *Audio*, February & March, 1980.
5. Otala, M., "Feedback-Generated Phase Nonlinearity in Audio Amplifiers," London AES Convention, March 1980, preprint 1976.
6. Stout, D.F., and Kaufman, M., *Handbook of Operational Amplifier Circuit Design*, New York, McGraw Hill, 1976.

Low-Bias-Current, High-Stability JFET Operational Amplifier

OP-41*

FEATURES

- **Low Bias Current** ..... **5pA Max**
- **Low Current Consumption** ..... **1.0mA Max**
- **High Gain** ..... **1000V/mV Min**
- **High Common-Mode Rejection** ..... **100dB Min**
- **Symmetrical Slew-Rates** ..... **±1.0V/μs Min**
- **Low Harmonic Distortion** ..... **<0.01% at 5kHz**
- **Phase Margin** ..... **77° Typ**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = 25°C V_{OS} MAX (μV)	PACKAGE TO-99	PACKAGE PLASTIC 8-PIN	PACKAGE SO 8-PIN	OPERATING TEMPERATURE RANGE
500	OP41AJ*	–	–	MIL
250	OP41EJ	–	–	IND
1000	OP41BJ*	–	–	MIL
750	OP41FJ	–	–	IND
2000	–	OP41GP	OP41GS	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

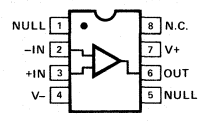
† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages.

GENERAL DESCRIPTION

The OP-41 JFET-input op amp features a 5pA max bias current with an open-loop gain of over 1 million. 77° of phase margin provides exceptional stability, even in unity-gain with capacitive loads. The output is guaranteed stable with 250pF loads at unity-gain, and will typically drive several thousand pF. Transient response is extremely clean, and is considerably improved over industry-standard JFET amplifiers.

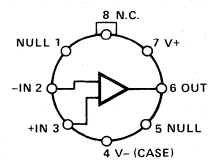
The OP-41's cascode input stage boosts CMR to over 100dB, improves CMR linearity, and stabilizes bias current with changing common-mode voltage. The linear common-mode rejection of 100dB min is unusually good for a FET input amplifier. The OP-41 consumes only 750μA supply current and has a power-supply rejection ratio of 25μV/V, making it an ideal choice for battery-operated systems. Despite the low supply-drain, the slew-rate is a respectable 1.3V/μs, and symmetrical. Using zener-zap trimming techniques, offset voltage is adjusted to below 500μV which eliminates the need for external nulling in many applications. The OP-41's guaranteed gain of 1 million into a 2kΩ load, combined with the linear 100dB minimum CMR, vastly improves linearity over competitive low-cost devices. Linearity is excellent in both low-gain and high-gain amplifier configurations. In voltage follower applications CMR effects dominate linearity, and in high-gain applications open-loop gain dominates linearity, hence the performance advantage of the OP-41.

PIN CONNECTIONS



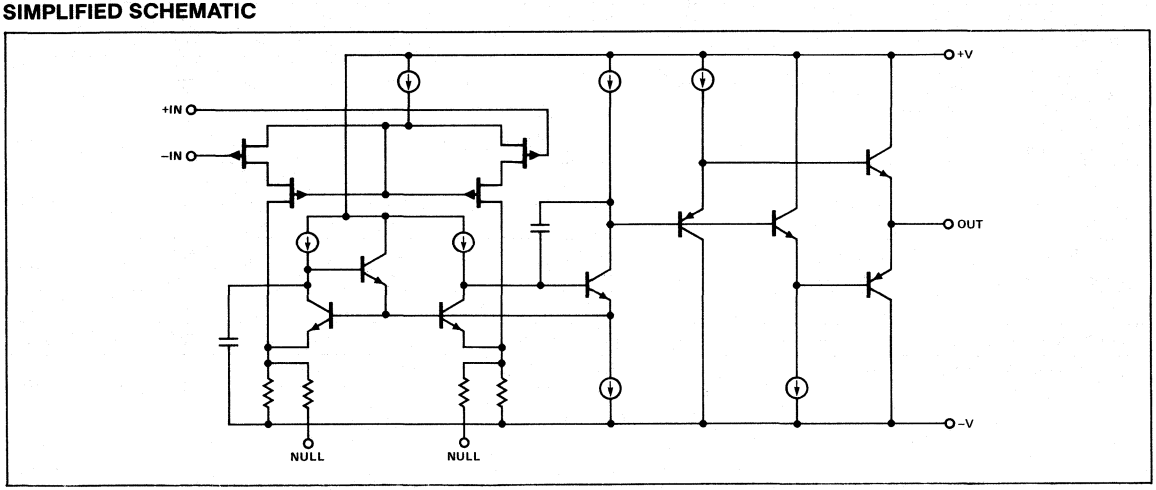
EPOXY MINI-DIP (P-Suffix)

8-PIN SO (S-Suffix)



TO-99 (J-Suffix)

SIMPLIFIED SCHEMATIC



*Manufactured under the following U.S. patent: 4,538,115.

The device exhibits rapid recovery from signal overload. Following saturation at the positive supply, the output recovers in only 6μs, and from a negative overdrive in only 100ns.

The combination of low-power, low bias current, and high-gain, plus the superior CMR and PSRR performance of the OP-41, make it suitable in a wide variety of demanding applications. The device makes an excellent output amplifier for CMOS DACs. Where low-power consumption is needed in portable instrumentation, the OP-41 permits high-gain and high-accuracy amplification with good speed performance. The low and stable bias current makes it an excellent choice as a photodiode amplifier in medical applications.

A standard 741 pin-out allows existing JFET designs and low-power bipolar designs to be upgraded by switching to the OP-41.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage ..... ±18V
Input Voltage (Note 1) ..... ±18V
Output Short-Circuit Duration ..... Indefinite
Differential Input Voltage (Note 1) ..... ±18V
Storage Temperature Range ..... –65°C to +150°C
Operating Temperature Range
OP-41A, B (J) ..... –55°C to +125°C
OP-41E, F (J) ..... –25°C to +85°C
OP-41G (P,S) ..... –40°C to +85°C
Lead Temperature Range (Soldering, 60 sec.) ..... +300°C
Junction Temperature ..... –65°C to +150°C

PACKAGE TYPE	Θ_{JA}(NOTE 3)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.
2. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-41A/E			OP-41B/F			OP-41G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Offset Voltage	V_{OS}	OP-41E/F/G OP-41A/B	— —	200 200	250 500	— —	400 400	750 1000	— —	500 —	2000 —	μV
Offset Current	I_{OS}	(Note 1)	—	0.04	1	—	0.05	2	—	0.05	5	pA
Bias Current	I_B	(Note 1)	—	3.0	5	—	3.5	10	—	3.5	20	pA
Open-Loop Voltage Gain	A_{VO}	$R_L = 2k\Omega$ $V_O = \pm 10V$	1000	5000	—	500	4000	—	500	4000	—	V/mV
Output Voltage Swing	V_O	$R_L = 2k\Omega$	±12.3	±12.6	—	±12.0	±12.6	—	±12.0	±12.6	—	V
Supply Current	I_{SY}	$V_O = 0V$	—	.75	1.0	—	.75	1.2	—	.75	1.2	mA
Input Voltage Range	IVR	(Note 2)	±11	+15 -11.5	—	±11	+15 -11.5	—	±11	+15 -11.5	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	100	115	—	90	110	—	90	110	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 18V$	—	5	25	—	10	80	—	10	80	μV/V
Noise Voltage Density Referred to Input	e_n	1kHz	—	32	—	—	32	—	—	32	—	$nV/\sqrt{Hz}$
Short Circuit Output Current	I_{SC}	Short Circuit to Ground	±12	+20 -18	±36	±12	+20 -18	±36	±6	+20 -18	±36	mA
Slew Rate	SR		1	1.3	—	1	1.3	—	1	1.3	—	V/μs
Gain Bandwidth	GBW		—	500	—	—	500	—	—	500	—	kHz
Power Bandwidth	BW_P		—	20	—	—	20	—	—	20	—	kHz

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-41A/E MIN	OP-41A/E TYP	OP-41A/E MAX	OP-41B/F MIN	OP-41B/F TYP	OP-41B/F MAX	OP-41G MIN	OP-41G TYP	OP-41G MAX	UNITS
Settling Time	t_s	10V Step $A_V = -1$ to 0.1%	—	10	—	—	10	—	—	10	—	μs
		to 0.01%	—	12	—	—	12	—	—	12	—	
Overload Recovery		Positive Going	—	0.1	—	—	0.1	—	—	0.1	—	μs
		Negative Going	—	6.0	—	—	6.0	—	—	6.0	—	
Capacitive Load Stability		$A_V = +1$ (Note 3)	250	>1000	—	250	>1000	—	250	>1000	—	pF
Open-Loop Output Resistance	R_O		—	150	—	—	150	—	—	150	—	Ω

NOTES:
1. Warmed up. $V_{CM} = 0$
2. Guaranteed by CMR test.
3. Guaranteed but not tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = -55°C/+125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-41A MIN	OP-41A TYP	OP-41A MAX	OP-41B MIN	OP-41B TYP	OP-41B MAX	UNITS
Offset Voltage	V_{OS}		—	400	1000	—	600	2000	μV
Temperature Coefficient of Input Offset Voltage	TCV_{OS}		—	2.5	5	—	3.5	10	μV/°C
Offset Current	I_{OS}	(Note 1)	—	40	1000	—	50	2000	pA
Bias Current	I_B	(Note 1)	—	4000	7500	—	4500	15000	pA
Open-Loop Voltage Gain	A_{VO}	$R_L = 2k\Omega$ $V_O = \pm 10V$	1000	5000	—	500	3000	—	V/mV
Output Voltage Swing	V_O	$R_L = 2k\Omega$	±12.0	±12.5	—	±11.5	±12.5	—	V
Supply Current	I_{SY}	$V_O = 0V$	—	.75	1.2	—	.75	1.2	mA
Input Voltage Range	IVR	(Note 2)	±11	+15 −11.5	—	±11	+15 −11.5	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	95	105	—	85	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 18V$	—	5	40	—	10	100	μV/V
Short Circuit Output Current	I_{SC}	Short Circuit to Ground	±6	+12 −17	±36	±6	+12 −17	±36	mA
Slew Rate	SR		1	1.3	—	1	1.3	—	V/μs
Gain Bandwidth	GBW		—	500	—	—	500	—	kHz
Power Bandwidth	BW_P		—	20	—	—	20	—	kHz
Capacitive Load Stability		$A_V = +1$ (Note 3)	100	>1000	—	100	>1000	—	pF

NOTES:
1. Warmed up. $V_{CM} = 0$
2. Guaranteed by CMR test.
3. Guaranteed but not tested.

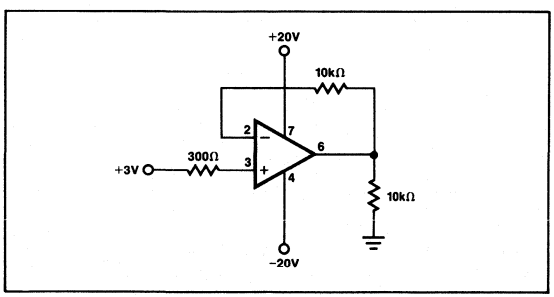
OP-41

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = –25°C/+85°C for E/F grades and –40°C/+85°C for G grade, unless otherwise noted.

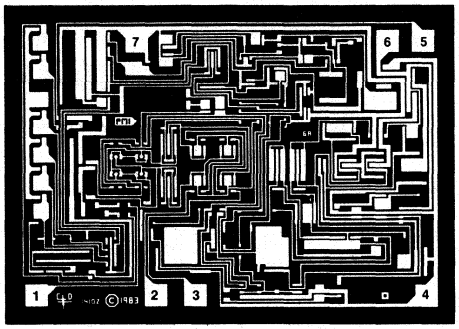
			OP-41E			OP-41F			OP-41G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Offset Voltage	V_{OS}		—	250	750	—	500	1750	—	500	2500	µV
Temperature Coefficient of Input Offset Voltage	TCV_{OS}		—	3.5	8	—	7.5	—	—	7.5	—	µV/°C
Offset Current	I_{OS}	(Note 1)	—	5	100	—	10	200	—	20	—	pA
Bias Current	I_B	(Note 1)	—	240	500	—	300	1000	—	100	500	pA
Open-Loop Voltage Gain	A_{VO}	R_L = 2kΩ V_O = ±10V	1000	5000	—	500	4000	—	500	4000	—	V/mV
Output Voltage Swing	V_O	R_L = 2kΩ	±12.0	±12.6	—	±11.5	±12.5	—	±11.5	±12.5	—	V
Supply Current	I_{SY}	V_O = 0V	—	0.75	1.2	—	0.75	1.2	—	0.75	1.2	mA
Input Voltage Range	IVR	(Note 2)	±11	+15 −11.5	—	±11	+15 −11.5	—	±11	+15 −11.5	—	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	95	110	—	85	100	—	85	100	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±10V to ±18V	—	5	40	—	10	100	—	10	100	µV/V
Short Circuit Output Current	I_{SC}	Short Circuit to Ground	±6	+16 −18	±36	±6	+16 −18	±36	±6	+20 −18	±36	mA
Slew Rate	SR		1	1.3	—	1	1.3	—	1	1.3	—	V/µs
Gain Bandwidth	GBW		—	500	—	—	500	—	—	500	—	kHz
Power Bandwidth	BW_P		—	20	—	—	20	—	—	20	—	kHz
Capacitive Load Stability		A_V = +1 (Note 3)	100	>1000	—	100	>1000	—	100	>1000	—	pF

NOTES:
1. Warmed up. V_{CM} = 0
2. Guaranteed by CMR test.
3. Guaranteed but not tested.

BURN-IN CIRCUIT



DICE CHARACTERISTICS



DIE SIZE 0.103 × 0.074 inch, 7622 sq. mils
(2.62 × 1.88mm, 4.92 sq. mm)

1. OFFSET VOLTAGE NULL
2. INVERTING INPUT
3. NONINVERTING INPUT
4. NEGATIVE SUPPLY
5. OFFSET VOLTAGE NULL
6. AMPLIFIER OUTPUT
7. POSITIVE SUPPLY

2

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-41N LIMIT	UNITS
Offset Voltage	V_{OS}		1000	μV MAX
Bias Current	I_B	(Note 1)	20	pA MAX
Open-Loop Voltage Gain	A_{VO}	$R_L = 2k\Omega$	500	V/mV MIN
Output Voltage Swing	V_O	$R_L = 2k\Omega$	±12	V MIN
Supply Current	I_{SY}	$V_O = 0V$	1.2	mA MAX
Input Voltage Range	IVR	(Note 2)	±11	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	90	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 18V$	80	μV/V MAX
Short Circuit Output Current	I_{SC}	Short Circuit to Ground	±6 ±36	mA MIN mA MAX
Slew Rate	SR		1	V/μs MIN
Capacitive Load Stability	$A_V = +1$	(Note 3)	250	pF MIN

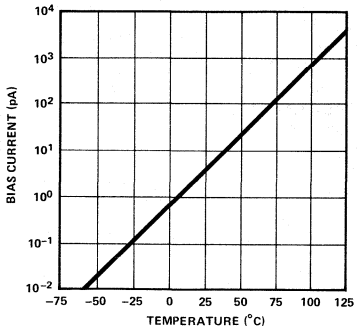
NOTES:
1. $V_{CM} = 0$
2. Guaranteed by CMR test.
3. Guaranteed but not tested.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

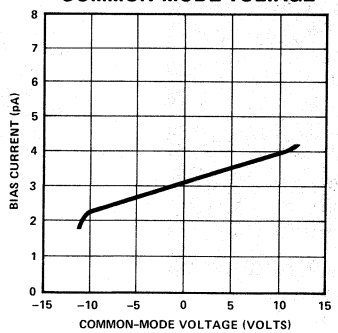
OP-41

TYPICAL PERFORMANCE CHARACTERISTICS

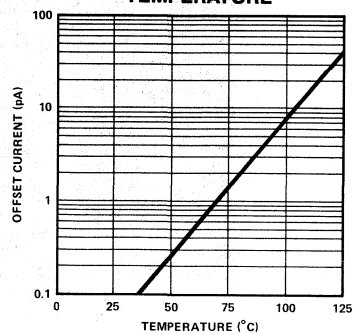
BIAS CURRENT vs TEMPERATURE



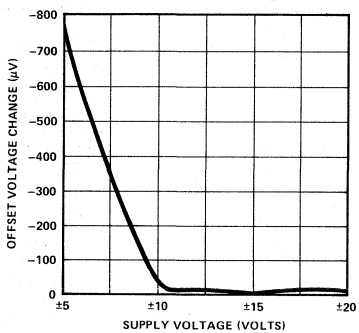
BIAS CURRENT vs COMMON-MODE VOLTAGE



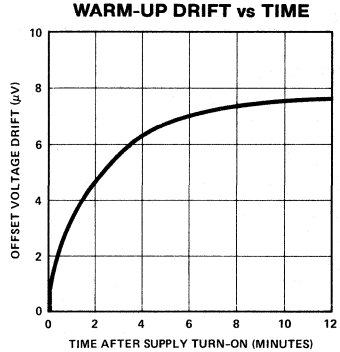
OFFSET CURRENT vs TEMPERATURE



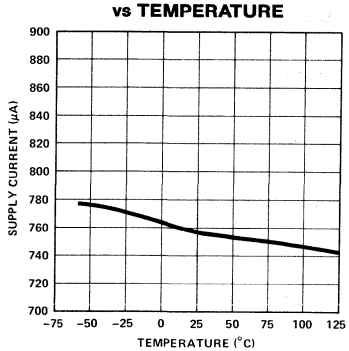
OFFSET VOLTAGE vs SUPPLY VOLTAGE



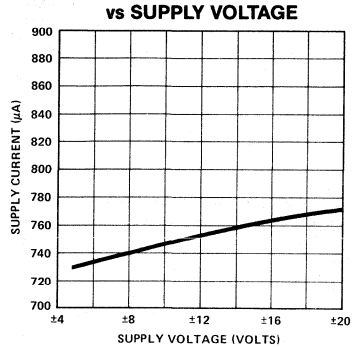
WARM-UP DRIFT vs TIME



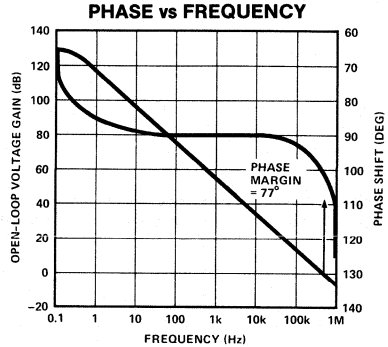
SUPPLY CURRENT vs TEMPERATURE



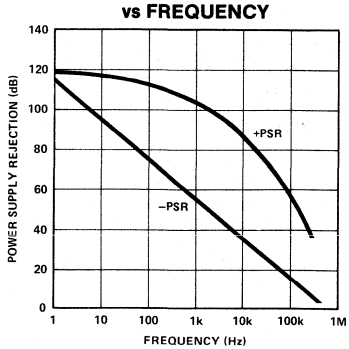
SUPPLY CURRENT vs SUPPLY VOLTAGE



OPEN-LOOP GAIN AND PHASE vs FREQUENCY

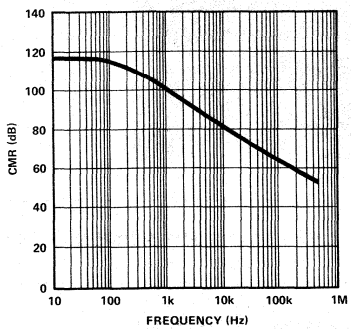


POWER SUPPLY REJECTION vs FREQUENCY

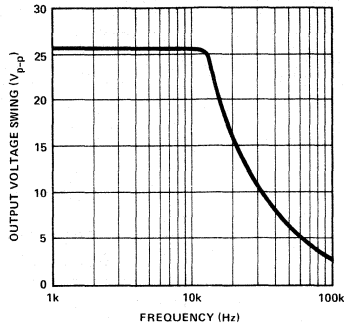


TYPICAL PERFORMANCE CHARACTERISTICS

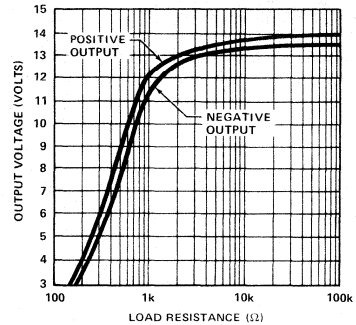
COMMON-MODE REJECTION vs FREQUENCY



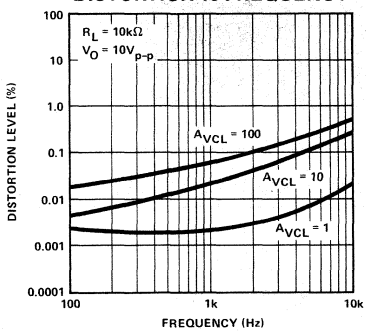
MAXIMUM OUTPUT SWING vs FREQUENCY



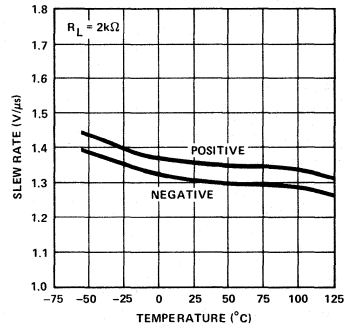
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



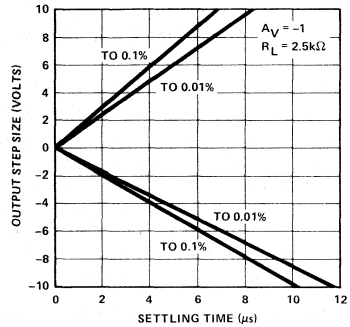
TOTAL HARMONIC DISTORTION vs FREQUENCY



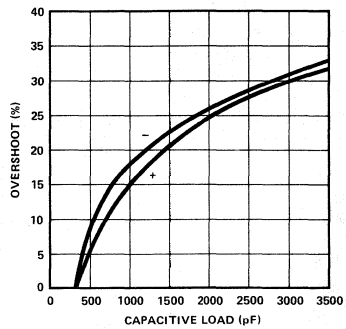
SLEW RATE vs TEMPERATURE



SETTLING TIME



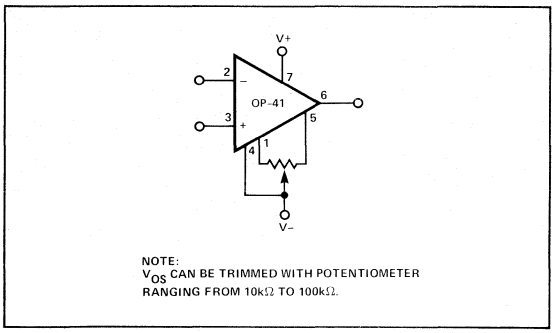
SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD



OFFSET VOLTAGE ADJUSTMENT

Offset voltage is adjusted by a potentiometer of 10kΩ to 100kΩ resistance. This potentiometer should be connected between pins 1 and 5 with the wiper connected to the V- supply. (See Figure 1.) Nulling V_{OS} will change TCV_{OS} by no more than 5μV/°C per millivolt of V_{OS} change.

FIGURE 1: INPUT OFFSET VOLTAGE NULLING



APPLICATIONS INFORMATION

TYPICAL AC PERFORMANCE CHARACTERISTICS

Figure 2 shows the overload recovery time after the output saturates at each supply. A high degree of slew-rate symmetry is maintained even during severe input overload. The photo also shows the well controlled linear characteristics of the amplifier and freedom from oscillations. The OP-41's symmetry greatly reduces the generation of large DC components in the output when the amplifier is overdriven. This significantly reduces system recovery time after an overload.

Figure 3 shows the unity-gain small-signal transient response of the OP-41. Note the clean symmetrical waveform.

Figure 4 illustrates the high degree of stability even when loaded with 1000pF at unity-gain. Heavy capacitive loading will cause stability problems with many amplifiers.

Figure 5 illustrates the use of the OP-41 in a high sensitivity, wide-dynamic-range light detector. This circuit will produce an output voltage proportional to the light input over a 60dB range.

FIGURE 2: OVERLOAD RECOVERY TIME AT A_V = 10

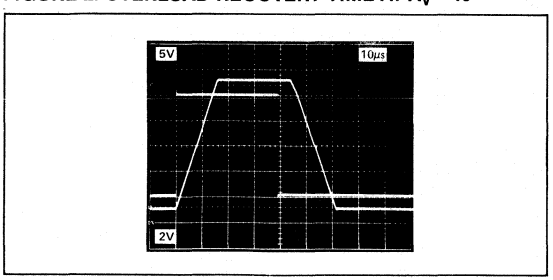


FIGURE 3: SMALL-SIGNAL TRANSIENT RESPONSE

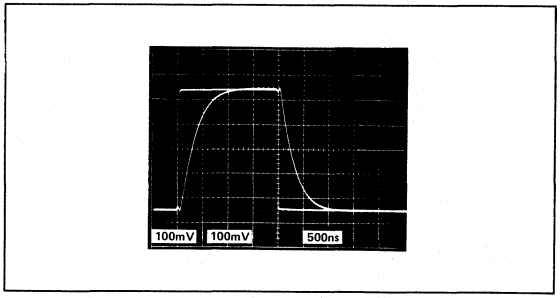


FIGURE 4: SMALL-SIGNAL TRANSIENT RESPONSE WITH 1000pF LOAD

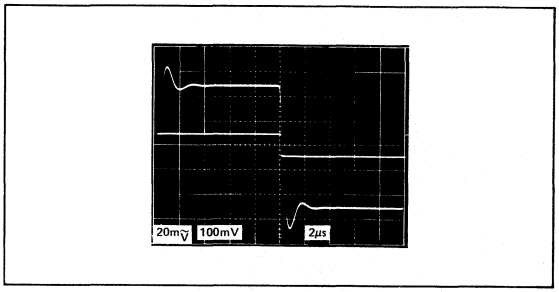
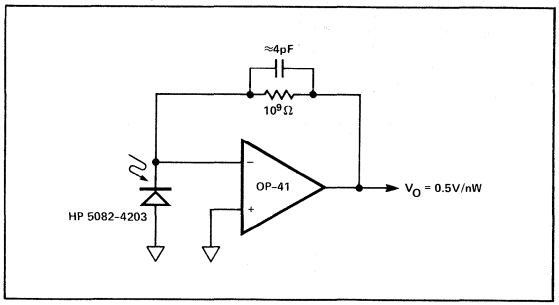


FIGURE 5: WIDE-DYNAMIC-RANGE LIGHT DETECTOR

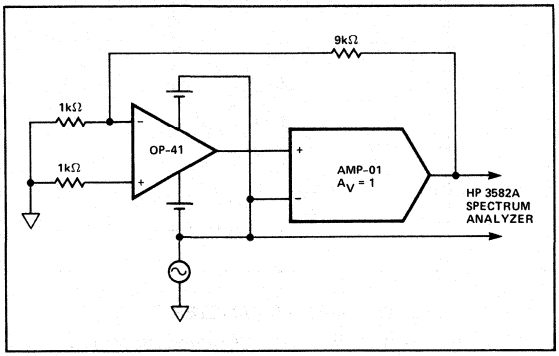


CMR MEASUREMENT METHODS

Two separate methods are used to measure the CMR. The first method is used over the range of 10Hz to 20kHz. This method grounds the input circuitry and applies the common-mode signal to the remainder of the op amp, Figure 6.

The AMP-01 eliminates loading on the output stage. This assures that the OP-41 output is not required to deliver current into the feedback circuit. The effects of the DUT open-loop gain changing with frequency are therefore significantly reduced. The circuit does not require tight resistor matching. DC data sheet limits may be verified using this method. Circuit accuracy is dependent on the high CMR of the AMP-01.

FIGURE 6: CIRCUIT USED TO MEASURE CMR FROM 10Hz TO 20kHz

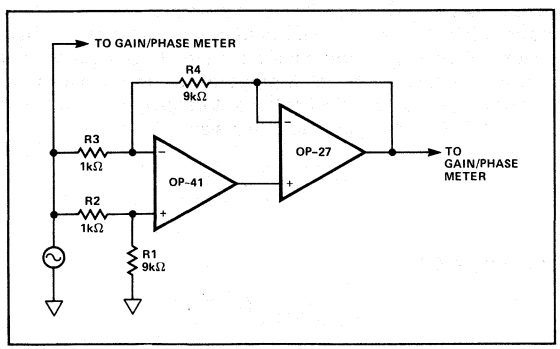


An alternate circuit may be used to make high-frequency measurements from 2kHz to 500kHz, Figure 7. The 2kHz to 20kHz data overlap can be used to verify the accuracy of the respective test methods.

This method drives the input stage with the test signal and requires an accurate ratio of resistors, R4/R3 = R1/R2. To measure CMR to 100dB requires ratio matching to better than 10ppm. For this reason, it is not practical to use the second method at low frequencies where CMR is greater than 80–100dB.

The DUT output is normally connected directly to R4 which may cause problems. If the DUT is not buffered with a broadband low-output-impedance amplifier, the frequency-dependent output impedance of the DUT, in series with R4, rapidly unbalances the resistor ratios. This causes frequency dependent errors. The OP-27 provides good performance over the range of frequencies used.

FIGURE 7: CIRCUIT USED TO MEASURE CMR FROM 2kHz TO 500kHz



GUARDING AND SHIELDING

In applications where the input is at high impedance, careful shielding is required to prevent hum pickup from power line sources or detection of RF from radio stations and nearby radar transmitters. Loss of accuracy can also occur from surface and bulk leakages in printed circuit boards. Both of these conditions can be avoided by the following methods.

Hum and RF pickup are eliminated or reduced by keeping all high impedance leads, including feedback resistor leads, inside shielded enclosures. In addition to shielding, power supply lines should be bypassed where they pass through the shielding. This will prevent noise from being retransmitted from the power supply lines inside the shielded enclosure.

Noise can also be created by the flexing of coax cable. These signals can be caused by mechanical vibrations inside or outside the shielding. Prevention consists of securely supporting all high-impedance shielded lines to prevent motion.

Printed circuit board leakage currents can easily exceed the OP-41 bias currents or the incoming signal. Leakage currents can be minimized by using Teflon insulators to support wires instead of using PC traces. An alternate method is guarding the high impedance traces. When the OP-41 is in the inverting mode, the signal traces should have grounded guard traces on both sides, Figure 8. The opposite side of the board should be used as a ground plane and shield, if not otherwise used. A ground plane is implemented by leaving copper on all areas that are not being used for signal or power conduction. Ground connection should be made to all areas of isolated copper. In the noninverting configuration, the OP-41's output signal or a portion of it should be used to drive the guard traces, Figure 9. When the guard drive voltage is equal to the input signal, leakage currents will be effectively eliminated.

FIGURE 8: CURRENT-TO-VOLTAGE CONVERTER

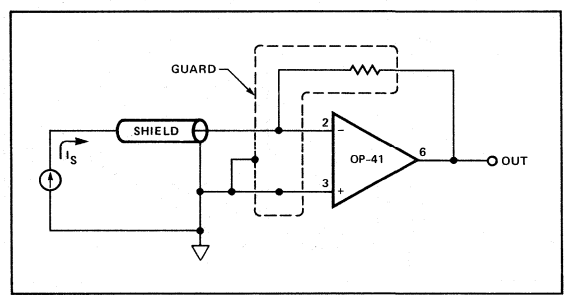
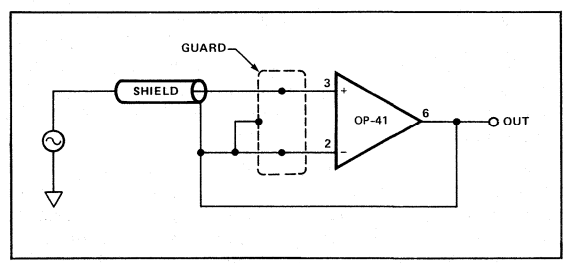
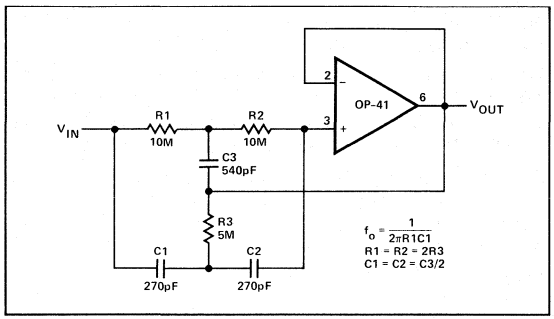


FIGURE 9: VERY HIGH IMPEDANCE NONINVERTING AMPLIFIER



The High Q Notch Filter benefits from the low bias current and high input impedance of the OP-41, Figure 10. These features enable small value capacitors and large resistors to be used in this 60Hz notch filter. The 5pA bias current only develops 100μV across R1 and R2.

FIGURE 10: HIGH Q NOTCH FILTER



Low power consumption, low bias current, and low offset voltage make the OP-41 an ideal current-to-voltage converter, Figure 11.

In this application, the PM-7541 and the OP-41 provide complete 12-bit digital-to-analog conversion with less than 3mA supply current.

FIGURE 11: DAC CIRCUIT USING THE OP-41

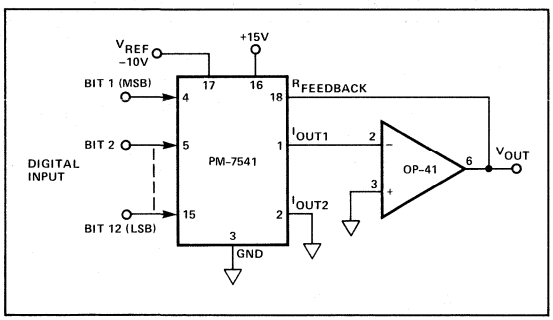
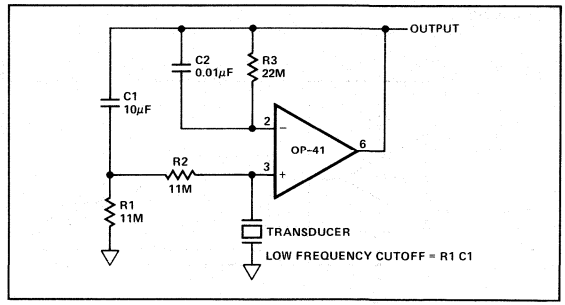


Figure 12 shows an amplifier for high-impedance ac transducers like a piezoelectric accelerometer. These sensors normally require a high-input-resistance amplifier. The OP-41 can provide input resistance in the range of $10^{12}\Omega$, however, a dc return for bias current is needed. To maintain a high R_{IN}, large value resistors above 22MΩ are often required. These may not be practicable.

Using the circuit in Figure 12, input resistances that are orders of magnitude greater than the values of the dc return resistors can be obtained. This is accomplished by bootstrapping the resistors to the output. With this arrangement, the lower cutoff frequency is determined more by the RC product of R1 and C1 than it is by resistor values and the equivalent capacitance of the transducer.

FIGURE 12: AMPLIFIER FOR PIEZOELECTRIC TRANSDUCERS



WIDE RANGE LOW-CURRENT AMMETER

The circuit shown in Figure 13 can measure currents from 100pA to 100μA without the use of high value resistors. Accuracy is better than 1% over most of the range, depending upon the accuracy of the divider resistor and the input bias current of the op amp. Using the OP-41 as the input amplifier allows low end measurement down to a few pA due to the 3.5pA input bias current.

One of the requirements for a good current meter is low series voltage drop. Since the voltage across the inputs of an op amp is forced to virtually zero, it makes a good choice for the input of a current meter. Amplifier A1 is used as an inverting amplifier for the input. This ensures less than 500μV drop at any current level.

Feedback around the op amp is accomplished with a transistor, rather than a resistor. The op amp forces the collector current of Q1A to equal the input current. This causes the emitter-base voltage of Q1A to be proportional to the log of the input current. Resistors R1, R2, R3 and capacitors C1, C2 frequency compensate the log circuit since Q1A provides gain in the feedback loop.

The output of the log amplifier is taken from the emitter of Q1A to drive Q1B. Q1B anti-logs the output and drives the meter. The output of Q1B is proportional to the log of the input current scaled by a constant, which is proportional to the voltage from the divider, selected by S1. For transistors operating at different current levels, the V_{be} difference equals:

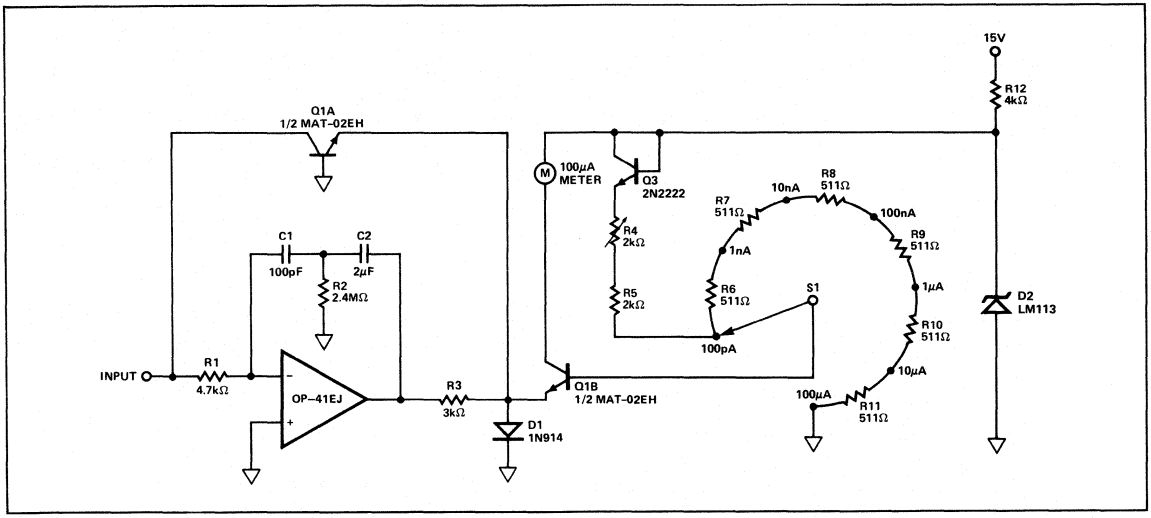
$$\Delta V_{be} = \frac{kT}{q} \ln \frac{IC2}{IC1}$$

solving for IC2

$$IC2 = IC1\ e^{\left(\frac{\Delta V_{be}\, q}{kT}\right)}$$

Where IC1 and IC2 are the collector currents of Q1A and Q1B; Q is the charge of an electron; k is Boltzmann's constant; T is temperature in degrees Kelvin; and V_{be} is the voltage applied to the base of Q1B. If V_{be} varies as absolute temperature, the exponent will be a constant.

FIGURE 13: WIDE RANGE LOW-CURRENT AMMETER



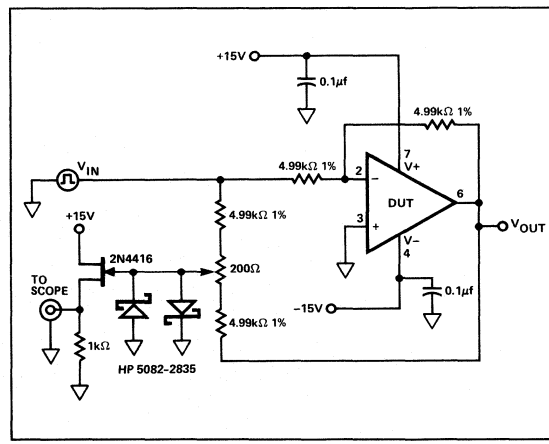
The voltage driving the divider is obtained from a 1.22V low voltage reference diode (LM113) through a 2N2222 transistor and resistor string. The voltage across the divider varies with absolute temperature, keeping the multiplier constant.

Calibration is simple, requiring only one adjustment. R4 is used to adjust full scale deflection with a 1μA input current. This will give maximum accuracy over the operating range of currents.

The low V_{OS} and exceptionally good log conformance of the MAT-02 assure high accuracy over the full 6 decade operating range.

Figure 14 is the test circuit used to measure the settling time. This circuit uses the "false sum-node" technique. When the system is initially set up, the 200Ω pot is adjusted until the DC output voltage to the scope is unchanged when the input is changed from +10V to −10V. The 2N4416 FET buffer isolates the sum node from the scope probe load capacitance. The pulse generator must be properly terminated and have ringing below the expected error signal. (2.5mV in a 5V pulse for 0.1% overshoot measurement.)

FIGURE 14: SETTLING-TIME TEST CIRCUIT



ANALOG DEVICES

High-Speed, Fast-Settling Precision Operational Amplifier

OP-42

FEATURES

Fast

- **Slew Rate ..... 50V/μs Min**
- **Settling-Time (0.01%) ..... 1μs Max**
- **Gain-Bandwidth Product ..... 10MHz Typ**

Precise

- **Common-Mode Rejection ..... 88dB Min**
- **Open-Loop Gain ..... 500V/mV Min**
- **Offset Voltage ..... 750μV Max**
- **Bias Current ..... 200pA Max**

Excellent Radiation Hardness
Available in Die Form

ORDERING INFORMATION †

T_A = 25°C, V_{OS} MAX (mV)	PACKAGE TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	SO 8-PIN	LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
1.0	OP42AJ*	OP42AZ*	–	–	OP42ARC/883	MIL
0.75	OP42EJ	OP42EZ	–	–	–	IND
1.5	OP42FJ	OP42FZ	–	–	–	IND
5.0	–	–	OP42GP	OP42GS	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages.

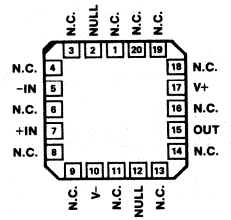
GENERAL DESCRIPTION

The OP-42 is a fast precision JFET-input operational amplifier. Similar in speed to the OP-17, the OP-42 offers a symmetric 58V/μs slew rate and is internally compensated for unity-gain operation. OP-42 speed is achieved with a supply current of less than 6mA. Unity-gain stability, a wide full-power bandwidth of 900kHz, and a fast settling-time of 800ns to 0.01% make the OP-42 an ideal output amplifier for fast digital-to-analog converters.

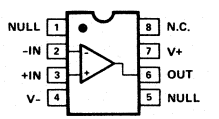
Equal attention was given to both speed and precision in the OP-42 design. Its tight 750μV maximum input offset voltage combined with well-controlled drift of less than 10μV/°C eliminates the need for external nulling in many circuits. The OP-42's

Continued

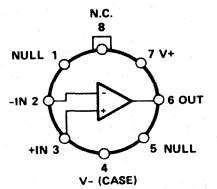
PIN CONNECTIONS



20-CONTACT LCC (RC-Suffix)

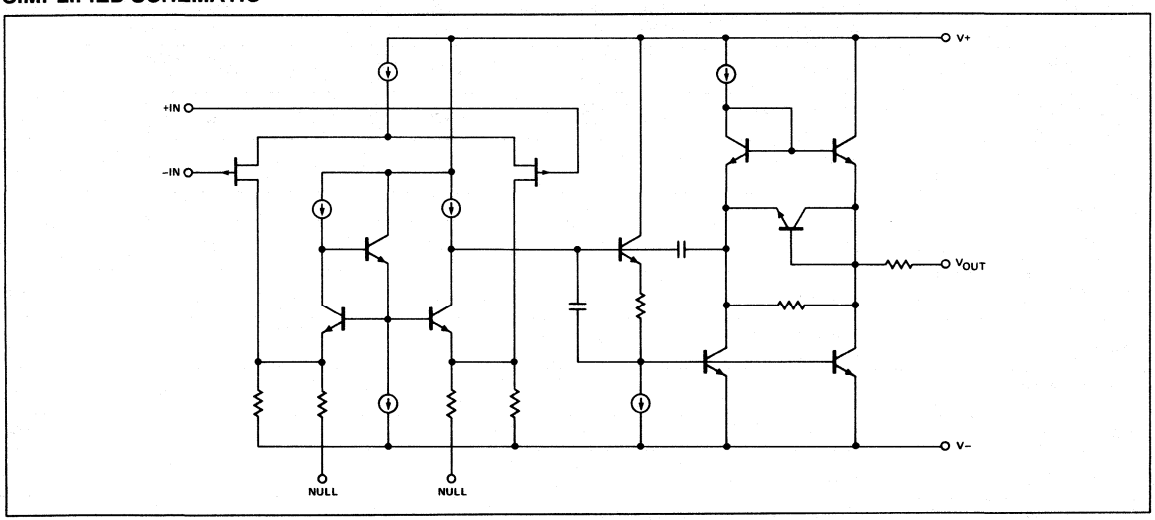


8-PIN CERDIP (Z Suffix)
EPOXY MINI-DIP (P-Suffix)
8-PIN SO (S-Suffix)



TO-99 (J-Suffix)

SIMPLIFIED SCHEMATIC



GENERAL DESCRIPTION *Continued*

common-mode rejection of 88dB minimum over a ±11V input voltage range is exceptional for a high-speed amplifier. High CMR combined with a minimum 500V/mV gain into 10kΩ load ensure excellent linearity in both noninverting and inverting gain configurations. The low input bias and offset currents provided by the JFET input stage suit the OP-42 for use in high-speed sample and hold circuits, peak detectors, and log amplifiers. Excellent radiation hardness characteristics make the OP-42 ideal for military and aerospace applications.

The OP-42 conforms to the standard 741 pinout with nulling to V–. The OP-42 upgrades the performance of circuits using the AD544, AD611, AD711, and LF400 by direct replacement. In circuits without nulling, the OP-42 offers an upgrade for designs using the OP-16, OP-17, LT1022, LT1056, and HA2510.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±20V
Input Voltage (Note 2) ..... ±20V
Differential Input Voltage (Note 2) 40V
Output Short-Circuit Duration ..... Indefined
Storage Temperature Range ..... –65°C to +175°C
Operating Temperature Range
OP42A (J, Z) ..... –55°C to +125°C
OP42E, F (J, Z) ..... –25°C to +85°C
OP42G ..... –40°C to +85°C
Junction Temperature ..... –65°C to +175°C
Lead Temperature Range (Soldering, 60 sec.) ..... +300°C

PACKAGE TYPE	Θ_{JA}(NOTE 3)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC (RC,TC)	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:

1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. For supply voltages less than ±20V, the absolute maximum input voltage is equal to the supply voltage.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CERDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

			OP-42E			OP-42F			OP-42G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Offset Voltage	V_{OS}		–	0.3	0.75	–	0.4	1.5	–	1.5	5.0	mV
Input Bias Current	I_B	V_{CM} = 0V T_j = 25°C	–	80	200	–	130	250	–	130	250	pA
Input Offset Current	I_{OS}	V_{CM} = 0V T_j = 25°C	–	4	40	–	6	50	–	6	50	pA
Input Voltage Range	IVR	(Note 1)	±11	+12.5 –12.0	–	±11	+12.5 –12.0	–	±11	+12.5 –12.0	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	88	98	–	80	92	–	80	92	–	dB
Power-Supply Rejection Ratio	PSRR	V_S = ±10V to ±20V	–	9	40	–	12	50	–	12	50	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L = 10kΩ R_L = 2kΩ R_L = 1kΩ V_O = ±10V T_j = 25°C	500 200 100	900 260 170	– – –	500 200 100	900 260 170	– – –	500 200 100	900 260 170	– – –	V/mV
Output Voltage Swing	V_O	R_L = 1kΩ	±11.5	+12.5 –11.9	–	±11.5	+12.5 –11.9	–	±11.5	+12.5 –11.9	–	V
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	±20	+33 –28	±60	±20	+33 –28	±60	±20	+33 –28	±60	mA
Supply Current	I_{SY}	No Load V_O = 0V	–	5.1	6.0	–	5.1	6.5	–	5.1	6.5	mA
Slew Rate	SR		50	58	–	40	50	–	40	50	–	V/µs
Full-Power Bandwidth	BW_p	(Note 2)	750	900	–	600	800	–	600	800	–	kHz
Gain-Bandwidth Product	GBW	f_O = 10kHz	–	10	–	–	10	–	–	10	–	MHz
Settling -Time	t_s	10V Step 0.01% (Note 3)	–	0.8	1.0	–	0.9	1.2	–	0.9	1.2	µs
Overload Recovery Time	t_{OR}		–	700	–	–	700	–	–	700	–	ns
Phase Margin	ϕ_o	0db Gain	–	47	–	–	47	–	–	47	–	degrees
Gain Margin	A_{180}	180° Open-Loop Phase Shift	–	9	–	–	9	–	–	9	–	dB
Capacitive Load Drive Capability	C_L	Unity-Gain Stable (Note 4)	100	300	–	100	300	–	100	300	–	pF

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	OP-42E MIN	OP-42E TYP	OP-42E MAX	OP-42F MIN	OP-42F TYP	OP-42F MAX	OP-42G MIN	OP-42G TYP	OP-42G MAX	UNITS
Differential Input Impedance	Z_{IN}		–	10^{12}||6	–	–	10^{12}||6	–	–	10^{12}||6	–	Ω||pF
Open-Loop Output Resistance	R_O		–	50	–	–	50	–	–	50	–	Ω
Voltage Noise	$e_{n\ p\text{-}p}$	0.1Hz to 10Hz	–	2	–	–	2	–	–	2	–	$\mu V_{p\text{-}p}$
Voltage Noise Density	e_n	f_O = 10Hz	–	38	–	–	38	–	–	38	–	nV/√Hz
		f_O = 100Hz	–	16	–	–	16	–	–	16	–	
		f_O = 1kHz	–	13	–	–	13	–	–	13	–	
		f_O = 10kHz	–	12	–	–	12	–	–	12	–	
Current Noise Density	i_n	f_O = 1kHz	–	0.007	–	–	0.007	–	–	0.007	–	pA/√Hz
External V_{OS} Trim Range		R_{pot} = 20kΩ	–	4	–	–	4	–	–	4	–	mV
Long-Term V_{OS} Drift			–	5	–	–	5	–	–	5	–	µV/month
Supply Voltage Range	V_S		±8	±15	±20	±8	±15	±20	±8	±15	±20	V

NOTES:
1. Guaranteed by CMR test.
2. Guaranteed by slew-rate test and formula $BW_p = SR/(2\pi 10V_{PEAK})$.
3. Settling-time is sample tested for A and E grades. Test circuit is shown in Figure 4. Settling-time for F grade is guaranteed but not tested.
4. Guaranteed but not tested.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-42A MIN	OP-42A TYP	OP-42A MAX	UNITS
Offset Voltage	V_{OS}		–	0.3	1.0	mV
Input Bias Current	I_B	V_{CM} = 0V T_j = 25°C	–	80	200	pA
Input Offset Current	I_{OS}	V_{CM} = 0V T_j = 25°C	–	4	40	pA
Input Voltage Range	IVR	(Note 1)	±11	+12.5 –12.0	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	86	96	–	dB
Power-Supply Rejection Ratio	PSRR	V_S = ±10V to ±20V	–	9	40	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L = 10kΩ, V_O = ±10V, T_j = 25°C	500	900	–	V/mV
		R_L = 2kΩ, V_O = ±10V, T_j = 25°C	200	260	–	
		R_L = 1kΩ, V_O = ±10V, T_j = 25°C	100	170	–	
Output Voltage Swing	V_O	R_L = 1kΩ	±11.5	+12.5 –11.9	–	V
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	±20	+33 –28	±60	mA
Supply Current	I_{SY}	No Load V_O = 0V	–	5.1	6.0	mA
Slew Rate	SR		45	52	–	V/µs
Full-Power Bandwidth	BW_p	(Note 2)	700	850	–	kHz
Gain-Bandwidth Product	GBW	f_O = 10kHz	–	10	–	MHz
Settling -Time	t_s	10V Step 0.01% (Note 3)	–	0.8	1.0	µs
Overload Recovery Time	t_{OR}		–	700	–	ns
Phase Margin	ϕ_o	0db Gain	–	47	–	degrees

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	OP-42A MIN	OP-42A TYP	OP-42A MAX	UNITS
Gain Margin	A_{180}	180° Open-Loop Phase Shift	–	9	–	dB
Capacitive Load Drive Capability	C_L	Unity-Gain Stable (Note 4)	100	300	–	pF
Differential Input Impedance	Z_{IN}		–	10^{12}||6	–	Ω||pF
Open-Loop Output Resistance	R_O		–	50	–	Ω
Voltage Noise	$e_{n\ p\text{-}p}$	0.1Hz to 10Hz	–	2	–	$\mu V_{p\text{-}p}$
Voltage Noise Density	e_n	f_O = 10Hz	–	38	–	$nV/\sqrt{Hz}$
		f_O = 100Hz	–	16	–	
		f_O = 1kHz	–	13	–	
		f_O = 10kHz	–	12	–	
Current Noise Density	i_n	f_O = 1kHz	–	0.007	–	$pA/\sqrt{Hz}$
External V_{OS} Trim Range		R_{pot} = 20kΩ	–	4	–	mV
Long-Term V_{OS} Drift			–	5	–	µV/month
Supply Voltage Range	V_S		±8	±15	±20	V

NOTES:
1. Guaranteed by CMR test.
2. Guaranteed by slew-rate test and formula $BW_p = SR/(2\pi 10V_{PEAK})$.
3. Settling-time is sample tested for A and E grades. Test circuit is shown in Figure 4. Settling-time for F grade is guaranteed but not tested.
4. Guaranteed but not tested.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, –25°C ≤ T_A ≤ 85°C for E/F grades, and –40°C ≤ T_A ≤ +85°C for G grade, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-42E MIN	OP-42E TYP	OP-42E MAX	OP-42F MIN	OP-42F TYP	OP-42F MAX	OP-42G MIN	OP-42G TYP	OP-42G MAX	UNITS
Offset Voltage	V_{OS}		–	0.4	1.2	–	0.6	2.5	–	2.0	6.0	mV
Offset Voltage Temperature Coefficient	TCV_{OS}		–	4	10	–	8	–	–	8	–	µV/°C
Input Bias Current	I_B	(Note 1)	–	0.5	1.2	–	0.6	2.0	–	0.6	2.0	nA
Input Offset Current	I_{OS}	(Note 1)	–	0.05	0.2	–	0.06	0.4	–	0.06	0.4	nA
Input Voltage Range	IVR	(Note 2)	±11	+12.5 –12.0	–	±11	+12.5 –12.0	–	±11	+12.5 –12.0	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	86	96	–	80	94	–	80	94	–	dB
Power-Supply Rejection Ratio	PSRR	V_S = ±10V to ±20V	–	2	40	–	6	50	–	6	50	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L = 10kΩ (Note 1)	200	500	–	200	500	–	200	500	–	V/mV
		R_L = 2kΩ V_O = ±10V	100	160	–	100	160	–	100	160	–	
Output Voltage Swing	V_O	R_L = 2kΩ	±11.0	+12.3 –11.8	–	±11.0	+12.3 –11.8	–	±11.0	+12.3 –11.8	–	V
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	±8	–	±60	±8	–	±60	±8	–	±60	mA
Supply Current	I_{SY}	No Load V_O = 0V	–	5.1	6.0	–	5.1	6.5	–	5.1	6.5	mA
Slew Rate	SR	R_L = 2kΩ	45	57	–	40	50	–	40	50	–	V/µs
Capacitive Load Drive Capability	C_L	Unity-Gain Stable (Note 3)	100	250	–	100	250	–	100	250	–	pF

NOTES:
1. T_j = 85°C for E/F/G Grades; T_j = 125°C for A grade.
2. Guaranteed by CMR test.
3. Guaranteed but not tested.

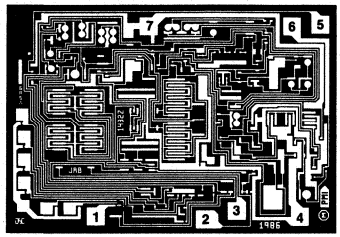
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le 125°C$ for A grade, unless otherwise noted.

			OP-42A			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Offset Voltage	V_{OS}		–	0.5	2.0	mV
Offset Voltage Temperature Coefficient	TCV_{OS}		–	4	10	µV/°C
Input Bias Current	I_B	(Note 1)	–	6	20	nA
Input Offset Current	I_{OS}	(Note 1)	–	0.2	1.0	nA
Input Voltage Range	IVR	(Note 2)	±11	+12.5 –12.0	–	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	80	94	–	dB
Power-Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to ±20V	–	10	50	µV/V
Large-Signal Voltage Gain	A_{VO}	$R_L = 10k\Omega$ (Note 1) $R_L = 2k\Omega$ $V_O = \pm 10V$	160 80	350 110	– –	V/mV
Output Voltage Swing	V_O	$R_L = 2k\Omega$	±11.0	+12.3 –11.8	–	V
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	±8	–	±60	mA
Supply Current	I_{SY}	No Load $V_O = 0V$	–	5.1	6.0	mA
Slew Rate	SR	$R_L = 2k\Omega$	40	52	–	V/µs
Capacitive Load Drive Capability	C_L	Unity-Gain Stable (Note 3)	100	250	–	pF

NOTES:
1. $T_j = 85°C$ for E/F Grades; $T_j = 125°C$ for A grade.
2. Guaranteed by CMR test.
3. Guaranteed but not tested.

OP-42

DICE CHARACTERISTICS



DIE SIZE 0.098 × 0.070 inch, 6860 sq. mils
(2.49 × 1.78 mm, 4.43 sq. mm)

1. OFFSET VOLTAGE NULL
2. INVERTING INPUT
3. NONINVERTING INPUT
4. NEGATIVE SUPPLY
5. OFFSET VOLTAGE NULL
6. AMPLIFIER OUTPUT
7. POSITIVE SUPPLY

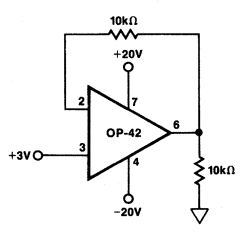
WAFER TEST LIMITS at $V_S = \pm 15V$, $T_j = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-42N LIMIT	UNITS
Offset Voltage	V_{OS}		1.5	mV MAX
Input Bias Current	I_B	$V_{CM} = 0V$	250	pA MAX
Input Offset Current	I_{OS}	$V_{CM} = 0V$	50	pA MAX
Input Voltage Range	IVR	(Note 1)	±11	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	80	dB MIN
Power-Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 20V$	50	µV/V MAX
Large-Signal Voltage Gain	A_{VO}	$R_L = 10k\Omega$ $R_L = 2k\Omega$ $R_L = 1k\Omega$	500 200 100	V/mV MIN
Output Voltage Swing	V_O	$R_L = 1k\Omega$	±11.5	V MIN
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	±20/±60	mA MIN/MAX
Supply Current	I_{SY}	No Load $V_O = 0V$	6.5	mA MAX
Slew Rate	SR		40	V/µs MIN
Capacitive Load Drive Capability	C_L	Unity-Gain Stable (Note 2)	100	pF MIN

NOTES:
1. Guaranteed by CMR test.
2. Guaranteed but not tested.

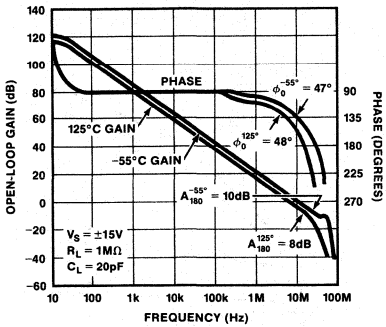
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

BURN-IN CIRCUIT

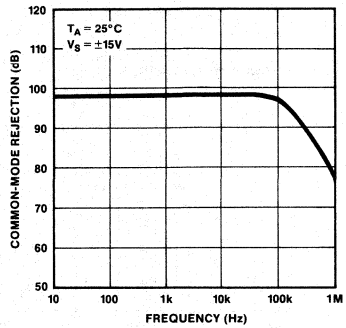


TYPICAL PERFORMANCE CHARACTERISTICS

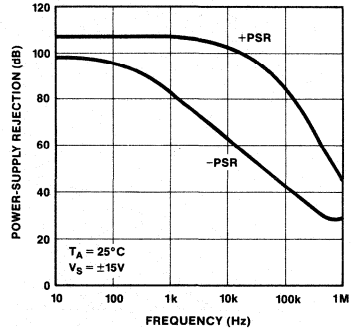
OPEN-LOOP GAIN, PHASE vs FREQUENCY



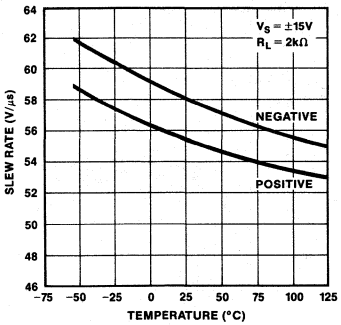
COMMON-MODE REJECTION vs FREQUENCY



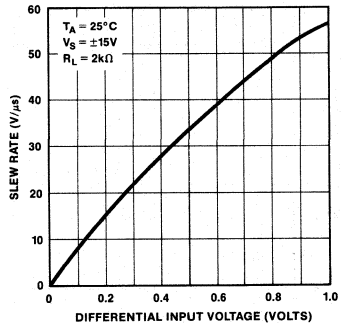
POWER-SUPPLY REJECTION vs FREQUENCY



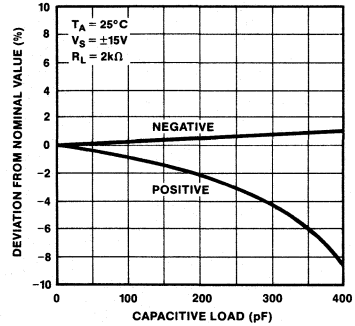
SLEW RATE vs TEMPERATURE



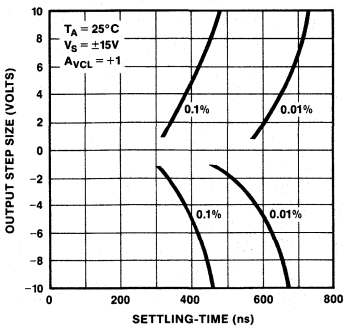
SLEW RATE vs DIFFERENTIAL INPUT VOLTAGE



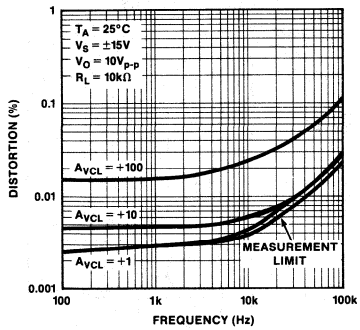
SLEW RATE vs CAPACITIVE LOAD



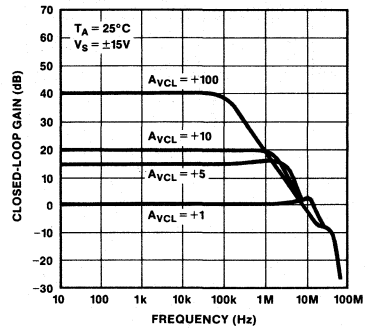
SETTLING-TIME vs STEP SIZE



DISTORTION vs FREQUENCY



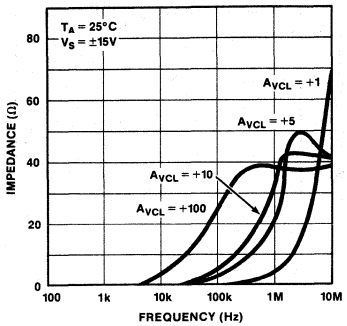
CLOSED-LOOP GAIN vs FREQUENCY



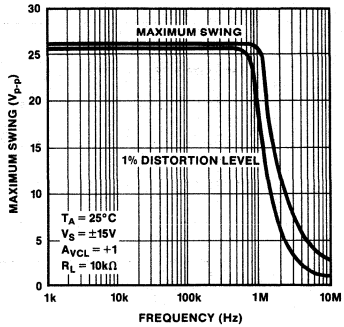
OP-42

TYPICAL PERFORMANCE CHARACTERISTICS

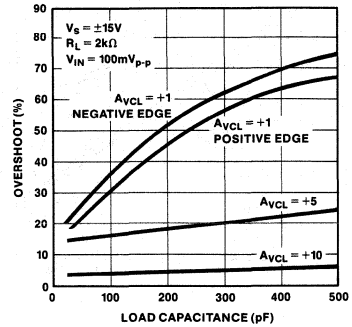
CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



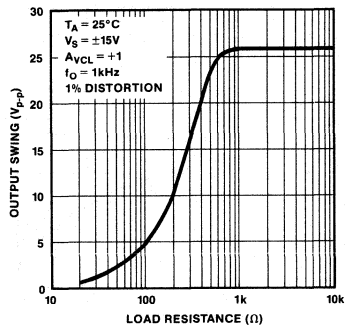
MAXIMUM OUTPUT SWING vs FREQUENCY



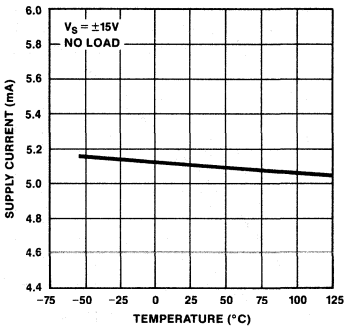
SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE



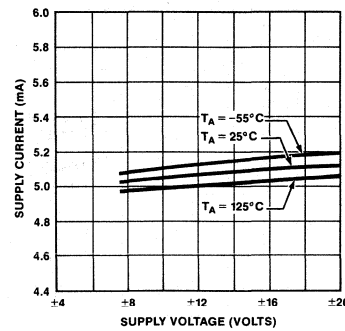
OUTPUT SWING vs LOAD RESISTANCE



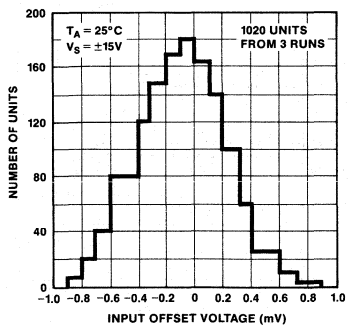
SUPPLY CURRENT vs TEMPERATURE



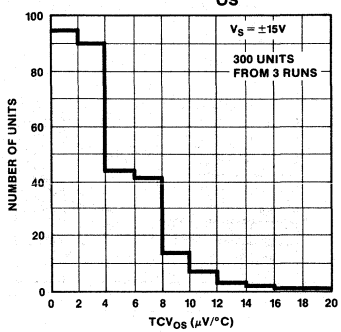
SUPPLY CURRENT vs SUPPLY VOLTAGE



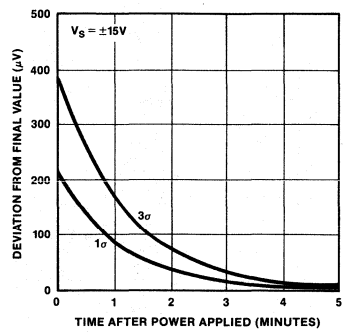
TYPICAL DISTRIBUTION OF INPUT OFFSET VOLTAGE



TYPICAL DISTRIBUTION OF TCV_{OS}

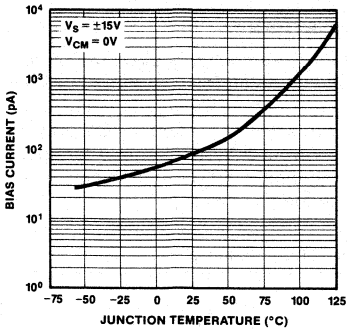


OFFSET VOLTAGE WARM-UP DRIFT

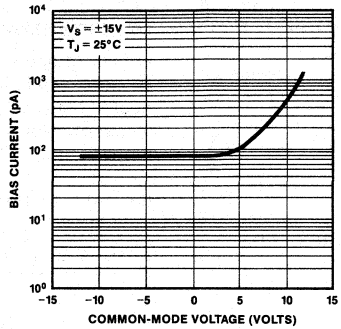


TYPICAL PERFORMANCE CHARACTERISTICS

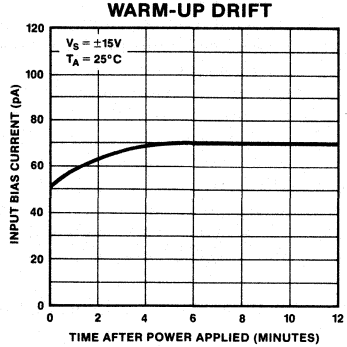
BIAS CURRENT vs JUNCTION TEMPERATURE



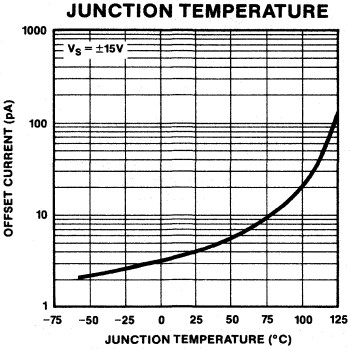
BIAS CURRENT vs COMMON-MODE VOLTAGE



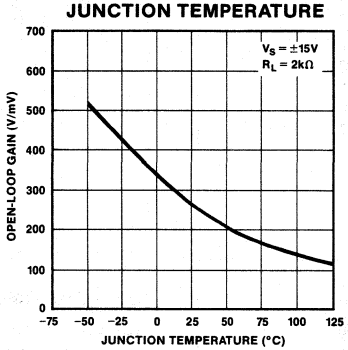
BIAS CURRENT WARM-UP DRIFT



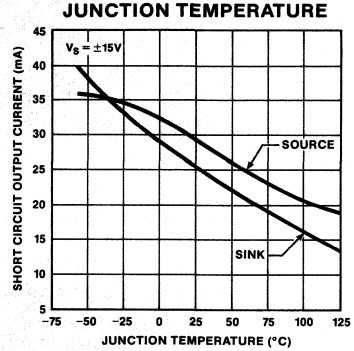
OFFSET CURRENT vs JUNCTION TEMPERATURE



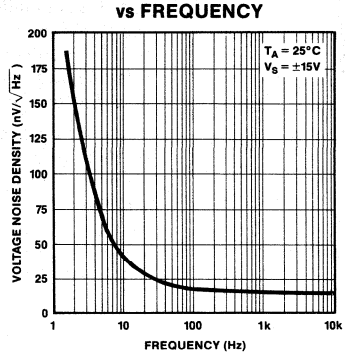
OPEN-LOOP GAIN vs JUNCTION TEMPERATURE



SHORT CIRCUIT OUTPUT CURRENT vs JUNCTION TEMPERATURE



VOLTAGE NOISE DENSITY vs FREQUENCY



APPLICATIONS INFORMATION

The OP-42 combines speed with a high level of input precision usually found only with slower devices. Well-behaved AC performance in the form of clean transient response, symmetrical slew-rates and a high degree of forgiveness to supply decoupling are the hallmarks of this amplifier. AC gain and phase response are quite independent of temperature or supply voltage. Figure 1 shows the OP-42's small-signal response. Even with 75pF loads, there is minimal ringing in the output waveform. Large-signal response is shown in Figure 2. This figure clearly shows the OP-42's exceptionally close matching between positive and negative slew-rates. Slew-rate symmetry decreases the DC offset a system encounters when processing high-frequency signals, and thus reduces the DC current necessary for load driving.

FIGURE 1: Small-Signal Transient Response, $Z_L = 2k\Omega||75pF$

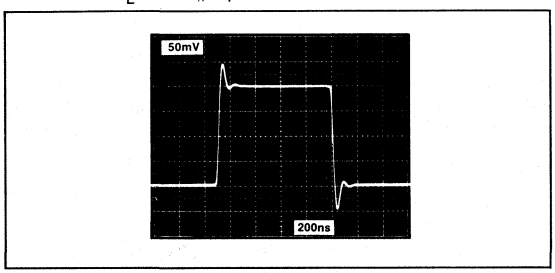
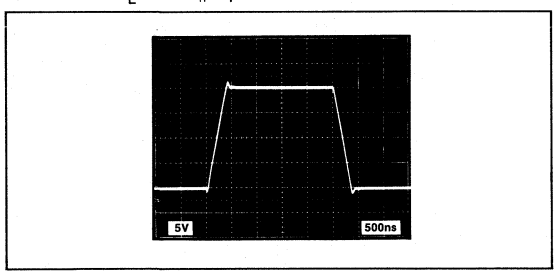


FIGURE 2: Large-Signal Transient Response, $Z_L = 2k\Omega||75pF$



As with most JFET-input amplifiers, the output of the OP-42 may undergo phase inversion if either input exceeds the specified input voltage range. Phase inversion will not damage the amplifier, nor will it cause an internal latch-up.

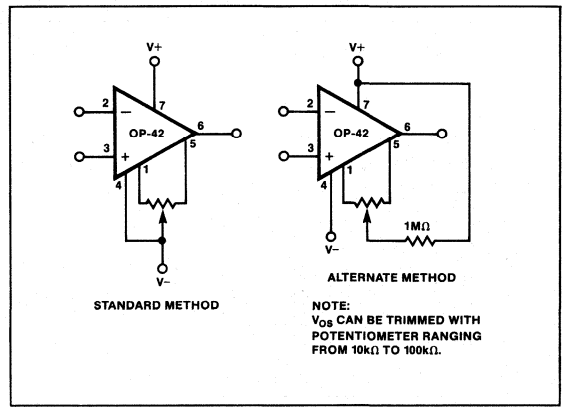
Supply decoupling should be used to overcome inductance and resistance associated with supply lines to the amplifier. For most applications a 0.1μF to 0.01μF capacitor should be placed between each supply pin and ground.

The OP-42 displays excellent resistance to radiation. Radiation hardness data is available by contacting the factory.

OFFSET VOLTAGE ADJUSTMENT

Offset voltage is adjusted with a 10kΩ to 100kΩ potentiometer as shown in Figure 3. The potentiometer should be connected between pins 1 and 5 with its wiper connected to the V– supply. Nulling V_{OS} in this manner changes TCV_{OS} by no more than 5μV/°C per millivolt of V_{OS} change. Alternately, V_{OS} may be nulled by attaching the potentiometer wiper through a 1MΩ resistor to the positive supply rail.

FIGURE 3: Input Offset Voltage Nulling



SETTLING-TIME

Guaranteed fast-settling is assured by sample-testing during production. The OP-42 is configured as a unity-gain follower in the test circuit of Figure 4. This test method has advantages over false-sum-node techniques in that the actual output of the amplifier is measured, instead of an error-voltage at the sum node. Common-mode settling effects are exercised in this circuit, in addition to the slew-rate and bandwidth effects measured by the false-sum-node method. A reasonably flat-top pulse is required as a stimulus.

The output waveform of the OP-42 being tested is clamped by Schottky diodes and buffered by the JFET source-follower. The signal is amplified by a factor of ten by the fast amplifier IC1, then Schottky-clamped before being output. The OP-41 provides overall offset nulling. Analysis of the waveform using a digitizing oscilloscope determines the op amp's settling-time.

FIGURE 4: Settling-Time Test Fixture

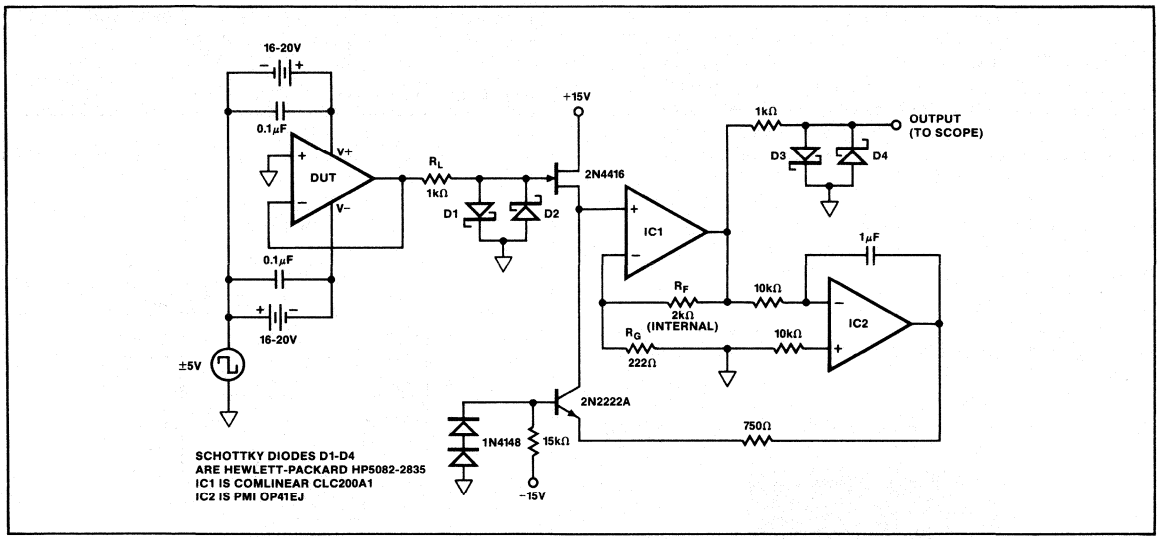
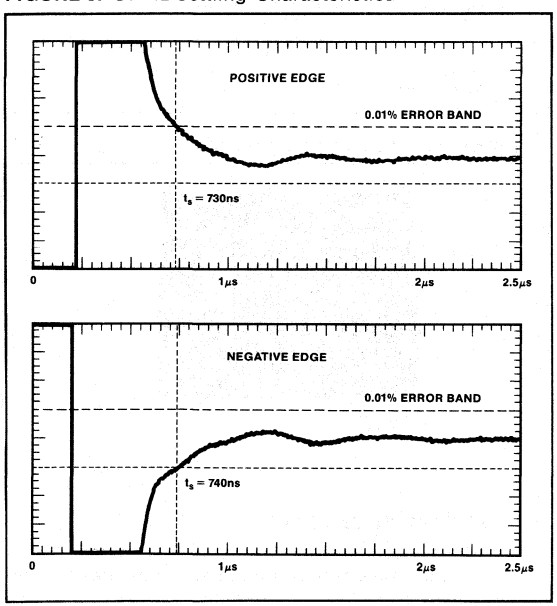


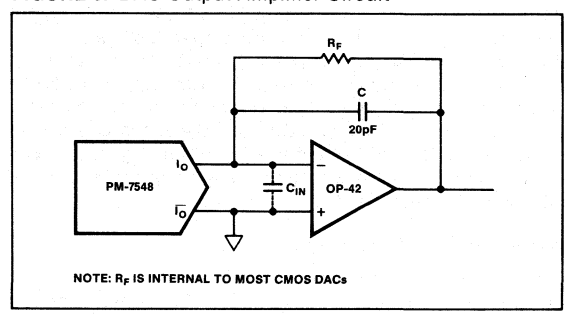
FIGURE 5: OP-42 Settling-Characteristics



DAC OUTPUT AMPLIFIER

The OP-42 is an excellent choice for a DAC output amplifier, since its high speed and fast settling-time allow quick transitions between codes, even for full-scale changes in output level. The DAC output capacitance appears at the operational amplifier inputs, and must be compensated to ensure optimal settling speed. Compensation is achieved with capacitor C in Figure 6. C must be adjusted to account for the DAC's output capacitance, the op amp's input capacitance, and any stray capacitance at the inputs. With a bipolar DAC, an additional shunt resistor may be used to optimize response. This technique is described in PMI's application note AN-24.

FIGURE 6: DAC Output Amplifier Circuit



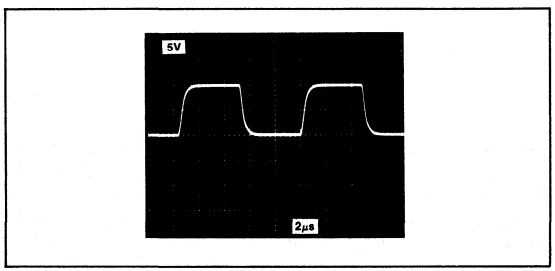
Highest speed is achieved using bipolar DACs such as PMI's DAC-08, DAC-10 or DAC-312. The output capacitances of these converters are up to an order of magnitude lower than their CMOS counterparts, resulting in substantially faster settling-times. The high output impedance of bipolar DACs allows the output amplifier to operate in a true current-to-voltage mode, with a noise gain of unity, thereby retaining the amplifier's full bandwidth. Offset voltage has minimal effect on linearity with bipolar converters.

CMOS digital-to-analog converters have higher output capacitances and lower output resistances than bipolar DACs.

This results in slower settling-times, higher sensitivity to offset voltages and a reduction in the output amplifier's bandwidth. These trade-offs must be balanced against the CMOS DAC's advantages in terms of interfacing capability, power dissipation, accuracy levels and cost. Using the internal feedback resistor which is present on most CMOS converters, the gain applied to offset voltage varies between 4/3 and 2, depending upon output code. Contributions to linearity error will be as much as $2/3V_{OS}$. In a 10-volt 12-bit system, this may add up to an additional 1/5LSB DNL with the OP-42E. Amplifier bandwidth is reduced by the same gain factor applied to offset voltage, however the OP-42's 10MHz gain-bandwidth product results in no reduction of the CMOS converter's multiplying bandwidth.

Individual DAC data-sheets should be consulted for more complete descriptions of the converters and their circuit applications.

FIGURE 7: DAC Output Amplifier Response (PM-7545 DAC)



DRIVING A HIGH-SPEED ADC

The OP-42's open-loop output resistance is approximately 50Ω. When feedback is applied around the amplifier, output resistance decreases in proportion to open-loop gain divided by closed-loop gain (A_{VOL}/A_{VCL}). Output impedance increases as open-loop gain rolls-off with frequency. High-speed analog-to-digital converters require low source impedances at high frequency. Output impedance at 1MHz is typically 5Ω for an OP-42 operating at unity-gain. If lower output impedances are required, an output buffer may be placed at the output of the OP-42.

HIGH-CURRENT OUTPUT BUFFER

The circuit in Figure 8 shows a high-current output stage for the OP-42. Output current is limited by R1 and R2. For good tracking between the output transistors Q1, Q2 and their biasing diodes D1 and D2, thermal contact must be maintained between the transistor and its associated diode. If good thermal contact is not maintained, R1 and R2 must be increased to 5-6Ω in order to prevent thermal runaway. Using 5Ω resistors, the circuit easily drives a 75Ω load (Figure 9). Output resistance is decreased and heavier loads may be driven by decreasing R1 and R2.

Base current and biasing for Q1 and Q2 are provided by two current sources, the MAT-02 and the JFET. The 2kΩ potentiometer in the JFET current source should be trimmed for optimum transient performance. The case of the MAT-02 should be connected to V–, and decoupled to ground with a 0.1μF capacitor. Compensation for the OP-42's input capacitance is provided by C_C. The circuit may be operated at any gain, in the usual op amp configurations.

FIGURE 8: High-Current Output Buffer

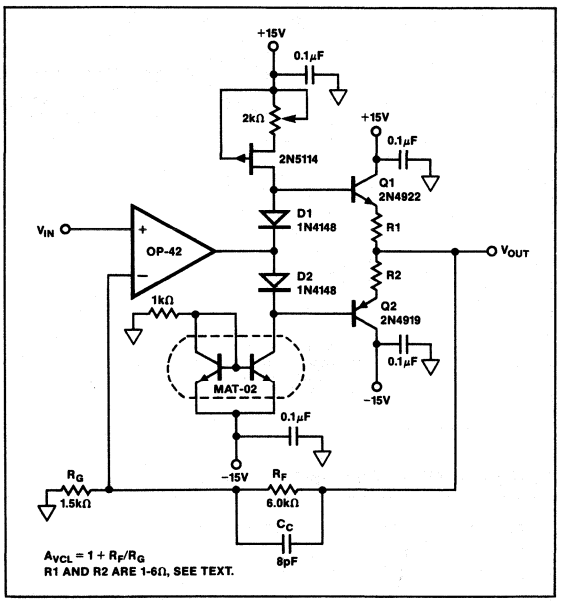
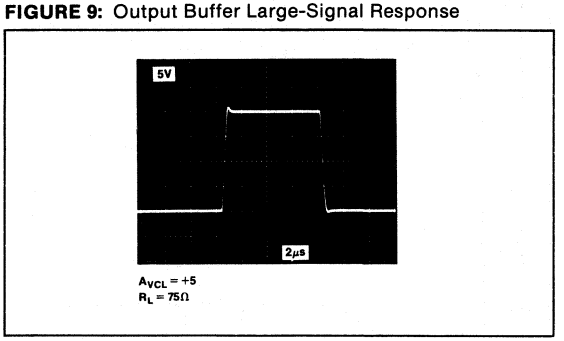


FIGURE 9: Output Buffer Large-Signal Response



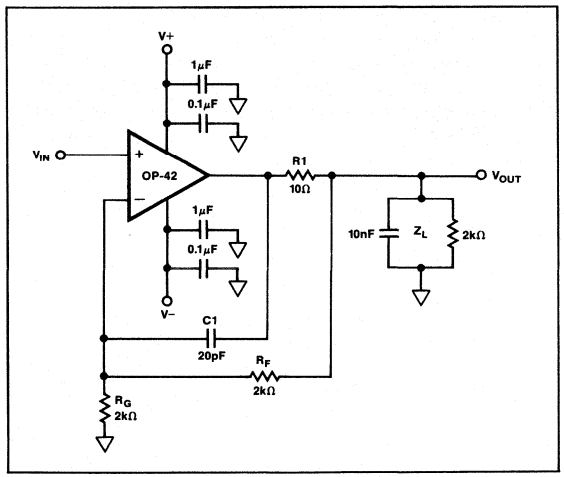
DRIVING CAPACITIVE LOADS

Best performance will always be achieved by minimizing input and load capacitances around any high-speed amplifier. However, the OP-42 is guaranteed capable of driving a 100pF capacitive load over its full operating temperature range while operating at any gain including unity. Typically, an OP-42 will drive more than 250pF at any temperature. Supply decoupling does affect capacitive load driving ability. Extra care should be given to ensure good decoupling when driving capacitive loads, and a larger decoupling capacitor between 1μF and 10μF should be placed in parallel with the usual decoupling capacitor on each supply.

Large capacitive loads may be driven utilizing the circuit shown in Figure 10. R1 and C1 introduce a small amount of feedforward compensation around the amplifier to counteract the phase lag induced by the output impedance and load capacitance. At DC and low frequencies, R1 is contained within the feedback loop. At higher frequencies, feedforward compensation becomes increasingly dominant, and R1's effect on output impedance will become more noticeable.

When driving very large capacitances, slew-rate will be limited by the short-circuit current limit. Although the unloaded slew-rate is insensitive to variations in temperature, the output current limit has a negative temperature coefficient, and is asymmetrical with regards to sourcing and sinking current. Therefore, slew-rate into excessive capacities will decrease with increasing temperature, and will lose symmetry.

FIGURE 10: Compensation for Large Capacitive Loads



COMPUTER SIMULATIONS

Many electronic design and analysis programs include models for op amps which calculate AC performance from the location of poles and zeros. As an aid to designers utilizing such a program, major poles and zeros of the OP-42 are listed below. Their location will vary slightly between production lots. Typically, they will be within ±15% of the frequency listed. Use of this data will enable the designer to evaluate gross circuit performance quickly, but should not supplant rigorous characterization of a breadboarded circuit.

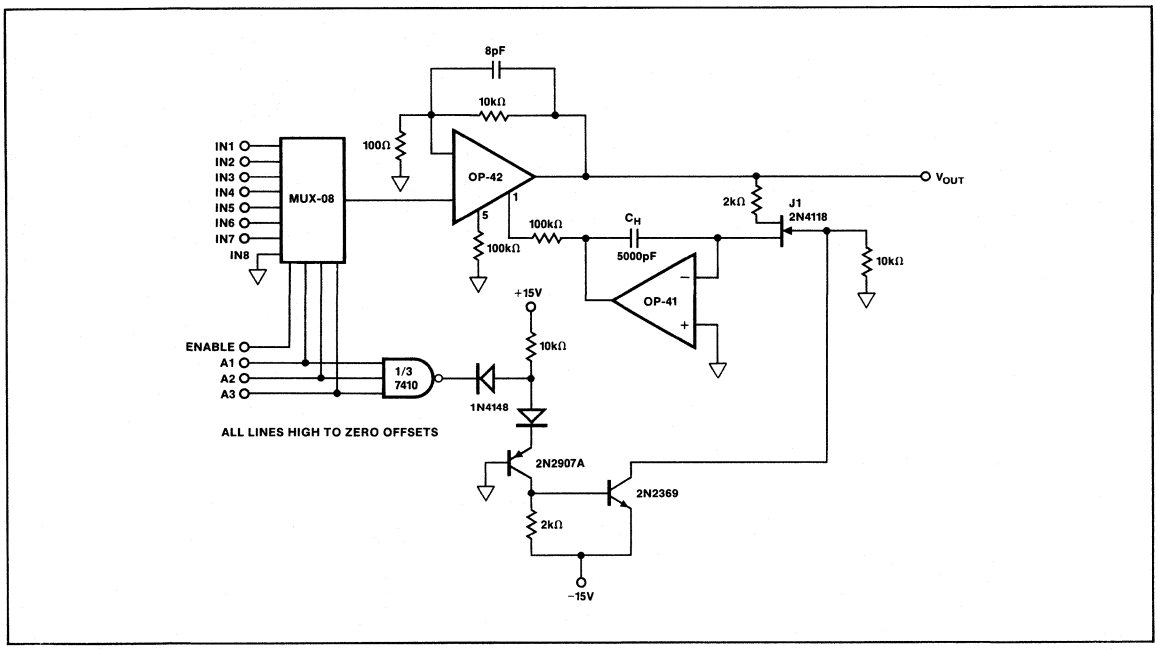
POLES	ZEROS
20Hz	1MHz
300kHz	
3MHz	

AUTOZEROING OFFSET VOLTAGE

Figure 11 describes a circuit for automatic offset voltage and drift correction. The OP-41 is used in a servo loop to force the OP-42 output equal to the OP-41's offset voltage. Thus, the OP-42's effective input offset is held below 10μV (1mV/A_{VCL} = 100) despite any temperature variations. This circuit will be most advantageous in high-gain applications.

Feedback is accomplished using the OP-42's null pins, leaving both inputs free for other purposes. In the application

FIGURE 11: OP-41 Servo Amplifier Provides Offset Correction



shown, the OP-42 has seven multiplexed inputs, while the eighth input provides a ground reference. Nulling is accomplished by addressing the grounded channel. This address should be held for at least 200μs. After this time, the address may be changed to another channel. The MUX-08 ENABLE pin must be high during the entire nulling cycle. During this time, JFET switch J1 turns on, completing feedback around the OP-41 servo amplifier. A charge is developed across C_H to compensate for the OP-42's offset voltage. When another channel is addressed, J1 turns off, and the correction charge is maintained across C_H by the OP-41. Droop is exceptionally low — only 1.3μV/s at 25° C. A correction range of more than 4mV allows nulling of minor system offsets as well as the OP-42's offset voltage.

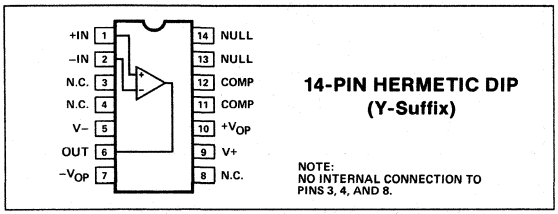
High-Output-Current Operational Amplifier ($A_{VCL} \geq 5$)

OP-50

FEATURES

- Open-Loop Gain ..... 10,000,000V/V Min
- Low Input Offset Voltage ..... 25μV Max
- Low Input Bias Current ..... 5nA Max
- Excellent TCV_{OS} ..... 0.3μV/°C Max
- High CMRR ..... 126dB Min
- High PSRR ..... 126dB Min
- Low Noise ..... 5.5nV/$\sqrt{Hz}$ @ f = 10Hz
  ..... 4.5nV/$\sqrt{Hz}$ @ f = 1kHz
- High Output Current ..... ±50mA
- Drives Capacitive Loads up to 10nF
- On-Board Thermal Shutdown Circuit
- Available in Die Form

PIN CONNECTIONS



14-PIN HERMETIC DIP (Y-Suffix)

NOTE:
NO INTERNAL CONNECTION TO PINS 3, 4, AND 8.

ORDERING INFORMATION†

T_A = 25°C V_{OS} MAX (μV)	PACKAGE CERDIP 14-PIN	OPERATING TEMPERATURE RANGE
25	OP-50AY*	MIL
100	OP-50BY*	MIL
25	OP-50EY	IND
100	OP-50FY	IND

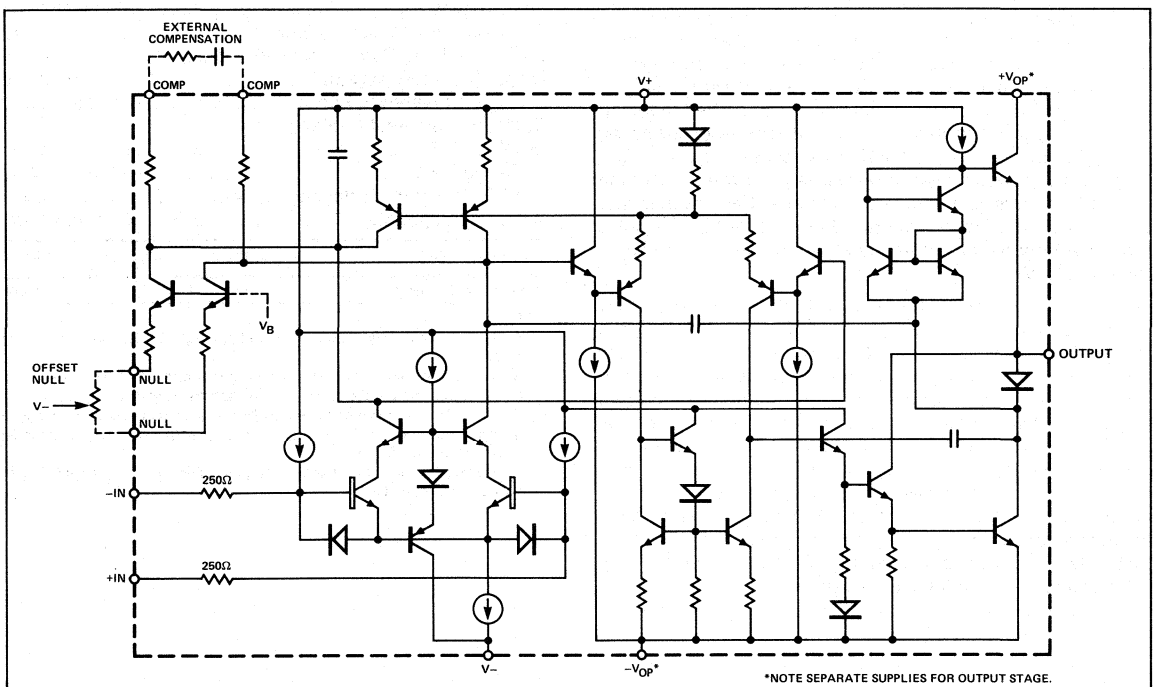
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

The OP-50 eliminates the need for an output buffer in applications which require high load-driving capability coupled with premium amplifier performance. The output stage can drive ±50mA into 50Ω loads. In addition, the output is stable with capacitive loads of up to 10nF. This load driving ability makes the OP-50 ideal for amplifying small signals for transmission through long cables. The amplifier features open-loop voltage gain of over 10 million with common-mode rejection and power supply rejection of greater than 126dB (A/E grades).

SIMPLIFIED SCHEMATIC



Manufactured under the following patents: 4,471,321 and 4,503,381.

OP-50

The OP-50 is stable for closed-loop gains above 50, and can be externally compensated for closed-loop gains in the range of 5 to 50. The amplifier is designed for use in high-gain and/or high-output-current applications. For example, an OP-07 coupled with an output buffer can be replaced by a single OP-50 amplifier.

Ion-implanted superbeta transistors, combined with a patented input bias current cancellation circuit, provide an input bias current of only 5nA and input offset current of 1nA. Over the full military temperature range, input bias current and input offset current for an A-grade device does not exceed 8nA and 3nA, respectively. Input offset voltages are trimmed to a maximum of 25μV (A/E grades) and 100μV (B/F grades) using PMI's zener-zapping technique. This low offset eliminates the need for an offset trimpot in most applications.

Low voltage-noise, typically 4.5nV/$\sqrt{Hz}$ at 1kHz, is achieved in the OP-50 with minimum sacrifice of input protection. Overload protection is provided by input resistors of 250Ω and emitter-base diodes. The input resistors provide current limit protection against differential inputs of up to ±10V; and the diodes prevent avalanche breakdown which could degrade the I_B, I_{OS}, and matching of the input stage transistors. External resistors can be added to the input to guard against higher input voltages; however, the added resistors will degrade noise voltage performance. When minimum noise voltage is required, source resistance should be kept below a few hundred ohms.

Separate output-stage power supply pins are provided on the OP-50 to allow control of device power dissipation and output voltage swing. The maximum voltage which may be applied across the power supply pins is ±18V. The guaranteed specifications are based on operating both stages at ±15V; however, there is minimal effect on DC performance when the main amplifier is operated at ±15V and the output stage is operated at a reduced voltage. When operating both the main amplifier and the output stage at the same voltages, the corresponding power supply pins may be tied together. Decoupling capacitors are recommended between the power supply pins and analog ground. It is necessary to use decoupling capacitors on each power supply pin when operating the output stage at supply voltages less than the amplifier supply voltage. Do not operate the output-stage negative power supply pin at a more negative voltage than the negative supply pin (V–).

A thermally-symmetric die layout, which differs from other op amp designs by the positioning of more devices along the center line, provides the OP-50 with a thermal drift of less than 0.3μV/°C. This layout feature is critical to the maintenance of high open-loop gain when driving large-current loads and dissipating hundreds of milliwatts in the device. The use of a heatsink is recommended to reduce internal temperature rise when operating at high output power levels. The use of standard dual-in-line package heatsinks will help to dissipate heat to the environment. Other techniques, such as the use of external voltage-dropping resistors, allow heat to be dissipated **outside** of the package. See Figure 5, "Driving 50Ω Loads", in the applications section.

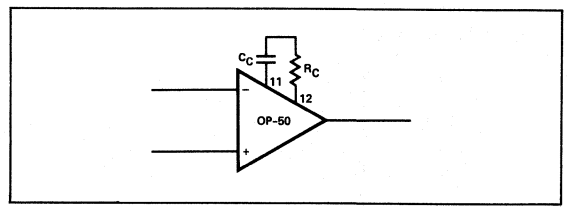
A thermal-shutdown circuit protects the OP-50 from overdissipation. When the die temperature reaches approximately 165°C, the output stage automatically shuts down. The amplifier input stage remains fully operational, thereby protecting the signal source from any loading changes caused by a complete shutdown.

COMPENSATION FOR GAINS BETWEEN 5 AND 50

The OP-50 can be compensated for inverting gains between 5 and 50 using a series resistor and capacitor. These values can be adjusted to minimize overshoot for a given application. The recommended compensation is:

GAIN RANGE	R_C	C_C
$5 \leq A_{VCL} \leq 20$	560Ω	4.7nF
$20 \leq A_{VCL} \leq 50$	3.3kΩ	1nF
$A_{VCL} \geq 50$	No compensation required	

COMPENSATION



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Note 2) ..... ±18V
Input Voltage ..... Supply Voltage
Differential Input Voltage (Note 3) ..... ±10V
Differential Input Current (Note 3) ..... ±20mA
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range ..... –65°C to +150°C
Operating Temperature Range
OP-50A, B ..... –55°C to +125°C
OP-50E, F ..... –25°C to +85°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
Junction Temperature (T_J) ..... –65°C to +150C

PACKAGE TYPE	Θ_{JA} (NOTE 4)	Θ_{JC}	UNITS
14-Pin Hermetic DIP (Y)	99	12	°C/W

NOTES:

1. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Supply voltage rating applies to all power supply pins. No device pins should be connected to a voltage more negative than the supply to V–, pin 5.
3. The OP-50's inputs are protected by 250Ω series resistors and protection diodes. If the differential input voltage exceeds ±10V, the input current must be limited to ±20mA.
4. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP package.

ELECTRICAL CHARACTERISTICS at V+ = $+V_{OP}$ = +15V, V− = $-V_{OP}$ = −15V, T_A = 25°C, no compensation, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-50A/E MIN	OP-50A/E TYP	OP-50A/E MAX	OP-50B/F MIN	OP-50B/F TYP	OP-50B/F MAX	UNITS
Input Offset Voltage	V_{OS}		—	10	25	—	50	100	µV
Input Bias Current	I_B		—	±1	±5	—	±1	±10	nA
Input Offset Current	I_{OS}		—	0.1	1	—	0.1	3	nA
Input Voltage Range	IVR	CMRR ≥ 100dB	±12	—	—	±12	—	—	V
Output Voltage Swing	V_O	$R_L \geq 500\Omega$ $R_L \geq 50\Omega$ (Note 1)	±13 ±2.5	±13.4 ±4.0	— —	±13 ±2.5	±13.4 ±4.0	— —	V
Output Voltage Swing	V_O	V+ = $+V_{OP}$ = +5V, V− = $-V_{OP}$ = −5V $R_L = 500\Omega$ $R_L = 50\Omega$	 ±3.5 ±2.5	 ±3.8 ±2.8	 — —	 ±3.5 ±2.5	 ±3.8 ±2.8	 — —	V
Slew Rate	SR	$R_L \geq 2k\Omega$ $R_C = 560\Omega$ C_C = 4.7nF	2.5	3.0	—	2.5	3.0	—	V/µs
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±10V	126	140	—	110	120	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5V to ±15V	—	0.1	0.5	—	0.5	1	µV/V
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V, R_L = 1kΩ	10	20	—	7.5	15	—	V/µV
Gain-Bandwidth Product	GBW	A_{VCL} = 50 (Note 2)	15	25	—	15	25	—	MHz
Offset Voltage Range Adjust		$R_P = 100k\Omega$	±1.0	±2.5	—	±1.0	±2.5	—	mV
Input Noise Voltage	e_{np-p}	f = 0.1Hz to 10Hz	—	0.12	—	—	0.12	—	μV_{p-p}
Noise Voltage Density	e_n	f = 10Hz (Note 3) f = 1kHz (Note 3)	— —	5.5 4.5	8.5 6.0	— —	5.5 4.5	8.5 6.0	$nV/\sqrt{Hz}$
Noise Current	i_{np-p}	f = 0.1Hz to 10Hz	—	2	—	—	2	—	pA_{p-p}
Noise Current Density	i_n	f = 100Hz f = 1kHz	— —	0.3 0.23	— —	— —	0.3 0.23	— —	$pA/\sqrt{Hz}$
Quiescent Supply Current	I_{SY}	No Load	—	2.6	3.3	—	2.6	3.3	mA
Positive Current Limit	$+I_{SC}$	Output shorted to Ground	60	95	120	60	95	120	mA
Negative Current Limit	$-I_{SC}$	Output shorted to Ground	60	85	120	60	85	120	mA
Differential-Mode Input Resistance	R_{IND}		—	2	—	—	2	—	MΩ
Common-Mode Input Resistance	R_{INCM}		—	20	—	—	20	—	GΩ
Capacitive Load Capability	C_L	$A_{VCL} \geq 5$ $R_C = 560\Omega$ (Note 2) C_C = 4.7nF	10	—	—	10	—	—	nF
Settling-Time	t_s	Settling to 0.01%, $V_O = 20V_{p-p}$ A_{VCL} = 500 A_{VCL} = 1000	 — —	 30 60	 — —	 — —	 30 60	 — —	µs

NOTES:
1. Guaranteed by current limit tests.
2. Guaranteed by design.
3. Sample tested.

OP-50

ELECTRICAL CHARACTERISTICS at $V+ = +V_{OP} = +15V$, $V- = -V_{OP} = -15V$, $-25°C \leq T_A \leq +85°C$, no compensation, unless otherwise noted.

			OP-50E			OP-50F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}		—	20	45	—	50	150	μV
Input Offset Voltage Drift	TCV_{OS}	(Note 1)	—	0.15	0.3	—	0.3	1	μV/°C
Input Bias Current	I_B		—	±2	±7	—	±2	±25	nA
Input Offset Current	I_{OS}		—	0.2	2.5	—	0.2	20	nA
Input Offset Current Drift	TCI_{OS}		—	3	—	—	5	—	pA/°C
Input Bias Current Drift	TCI_B		—	20	—	—	50	—	pA/°C
Input Voltage Range	IVR	CMRR ≥ 100dB	±11.5	—	—	±11.5	—	—	V
Output Voltage Swing	V_O	$R_L \geq 500Ω$	±12	±13.4	—	±12	±13.4	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = ±10V$	120	130	—	105	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = ±5V$ to ±15V	—	0.5	1.25	—	0.5	1.25	μV/V
Quiescent Supply Current	I_{SY}	No Load	—	2.8	4	—	2.8	4	mA
Open-Loop Gain	A_{VO}	$V_{OUT} = ±10V$, $R_L = 1kΩ$ (Note 2)	4	15	—	4	15	—	V/μV

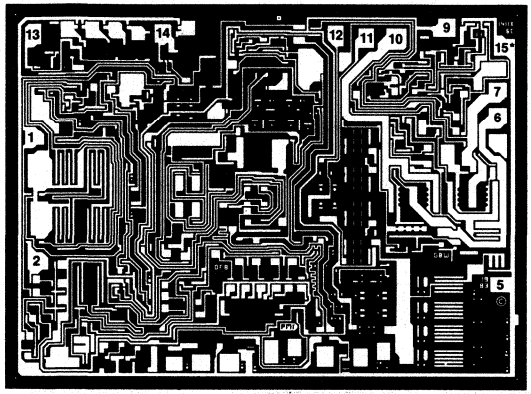
NOTES:
1. TCV_{OS} tested on E grade, guaranteed by design on F grade specification.
2. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V+ = +V_{OP} = +15V$, $V- = -V_{OP} = -15V$, $-55°C \leq T_A \leq +125°C$, no compensation, unless otherwise noted.

			OP-50A			OP-50B			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}		—	20	55	—	50	200	μV
Input Offset Voltage Drift	TCV_{OS}		—	0.15	0.3	—	0.3	1	μV/°C
Input Bias Current	I_B		—	±2	±8	—	±2	±20	nA
Input Offset Current	I_{OS}		—	0.5	3	—	0.5	12	nA
Input Offset Current Drift	TCI_{OS}		—	3	—	—	5	—	pA/°C
Input Bias Current Drift	TCI_B		—	20	—	—	50	—	pA/°C
Input Voltage Range	IVR	CMRR ≥ 100dB	±11.5	—	—	±11.5	—	—	V
Output Voltage Swing	V_O	$R_L \geq 500Ω$	±12	±13.2	—	±12	±13.2	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = ±10V$	120	130	—	105	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = ±5V$ to ±15V	—	0.5	1.25	—	0.5	1.25	μV/V
Quiescent Supply Current	I_{SY}	No Load	—	2.8	4	—	2.8	4	mA
Open-Loop Gain	A_{VO}	$V_O = ±10V$, $R_L = 1kΩ$ (Note 1)	4	10	—	4	10	—	V/μV

NOTE:
1. Tested at +125°C, guaranteed by design at −55°C.

DICE CHARACTERISTICS



DIE SIZE 0.149 × 0.111 inch, 16,539 sq. mils
(3.78 × 2.82 mm, 10.66 sq. mm)

1. NONINVERTING INPUT
2. INVERTING INPUT
5. V–
6. OUTPUT
7. $-V_{OP}$
9. V+
10. $+V_{OP}$
11. COMPENSATION
12. COMPENSATION
13. NULL
14. NULL
15. V– (OPTIONAL BONDING PAD)*

2

WAFER TEST LIMITS at V+ = $+V_{OP}$ = +15V, V– = $-V_{OP}$ = –15V, T_A = 25°C, no compensation, unless otherwise noted.

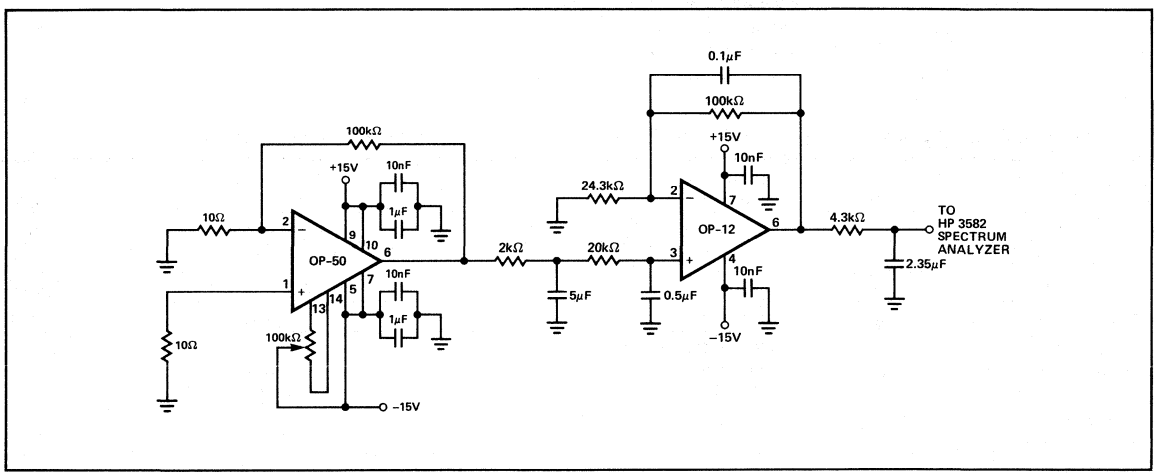
PARAMETER	SYMBOL	CONDITIONS	OP-50G LIMIT	UNITS
Input Offset Voltage	V_{OS}		100	μV MAX
Input Bias Current	I_B		±10	nA MAX
Input Offset Current	I_{OS}		3	nA MAX
Output Voltage Swing	V_O	$R_L \geq 500\Omega$	±13	V MIN
Output Voltage Swing	V_O	V+ = $+V_{OP}$ = +5V, V– = $-V_{OP}$ = –5V $R_L = 500\Omega$ $R_L = 50\Omega$	 ±3.5 ±2.5	V MIN
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±10V	110	dB MIN
Power Supply Rejection Ratio	PSRR	V_S = ±5V to ±15V	1	μV/V MAX
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V, R_L = 1kΩ	7.5	V/μV MIN
Positive Current Limit	$+I_{SC}$	Output shorted to Ground	60	mA MIN
Negative Current Limit	$-I_{SC}$	Output shorted to Ground	60	mA MIN
Quiescent Supply Current	I_{SY}	No Load	3.3	mA MAX

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

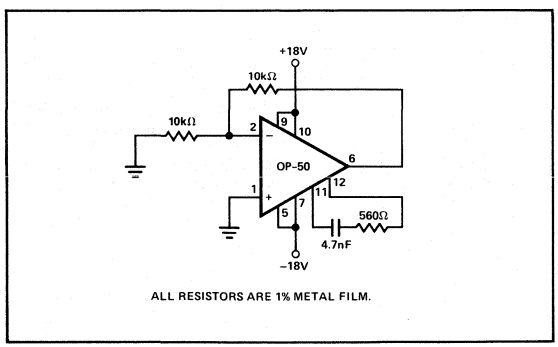
TYPICAL ELECTRICAL CHARACTERISTICS at $V+ = +V_{OP} = +15V$, $V- = -V_{OP} = -15V$, $T_A = 25°C$, no compensation, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-50G TYPICAL	UNITS
Slew Rate	SR	$R_L \geq 2k\Omega$ $R_C = 560\Omega$ $C_C = 4.7nF$	3	$V/\mu s$
Noise Voltage Density	e_n	f = 10Hz f = 1kHz	5.5 4.5	$nV/\sqrt{Hz}$
Input Noise Voltage	e_{np-p}	f = 0.1Hz to 10Hz	0.12	μV_{p-p}
Noise Current Density	i_n	f = 10Hz f = 1kHz	0.2 0.15	$pA/\sqrt{Hz}$
Capacitive Load Capability	C_L	$A_{VCL} \geq 5$ $R_C = 560\Omega$ $C_C = 4.7nF$	10	nF

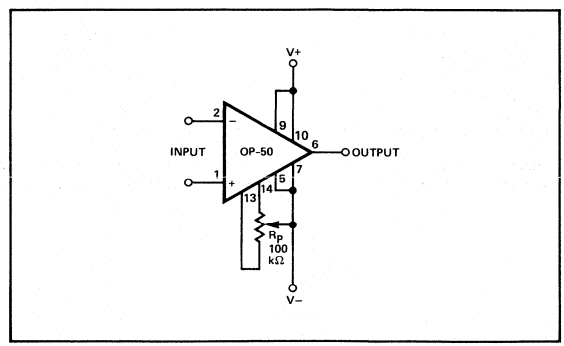
NOISE TEST CIRCUIT (0.1 TO 10Hz)



BURN-IN CIRCUIT

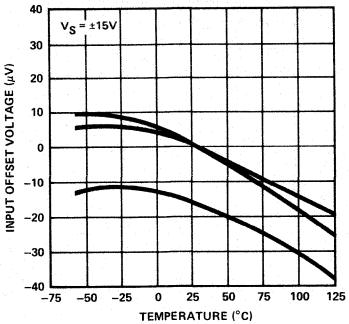


OFFSET NULLING CIRCUIT

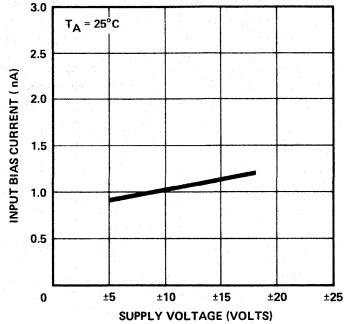


TYPICAL PERFORMANCE CHARACTERISTICS

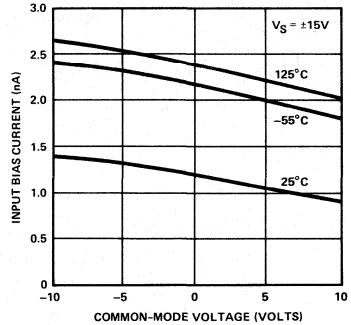
INPUT OFFSET VOLTAGE vs TEMPERATURE



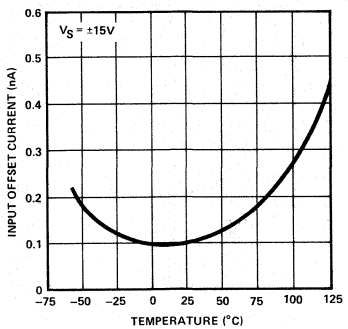
INPUT BIAS CURRENT vs SUPPLY VOLTAGE



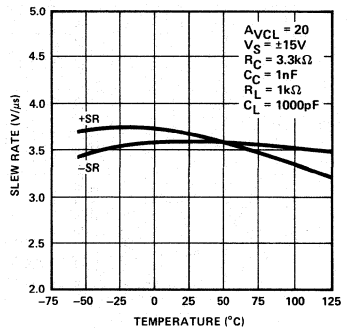
INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE



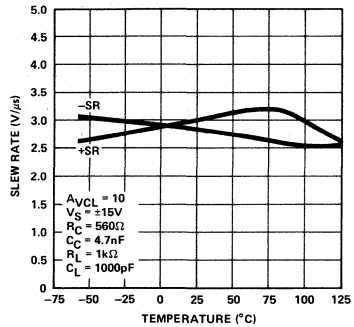
INPUT OFFSET CURRENT vs TEMPERATURE



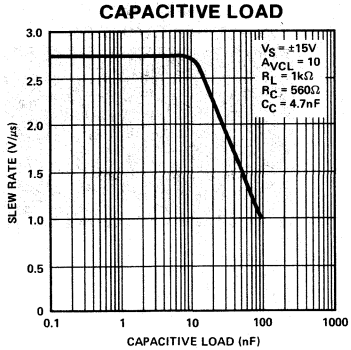
SLEW RATE vs TEMPERATURE



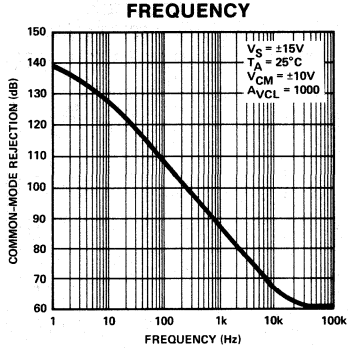
SLEW RATE vs TEMPERATURE



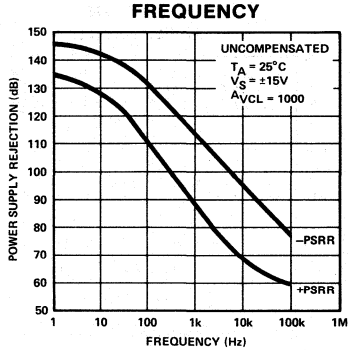
SLEW RATE vs CAPACITIVE LOAD



CMRR vs FREQUENCY



PSRR vs FREQUENCY

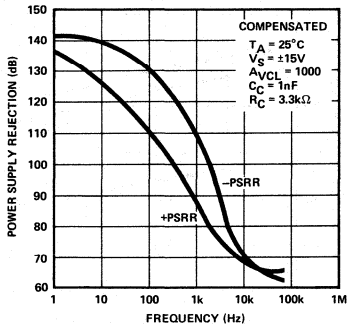


NOTE:
The symbol $\pm V_S$ is used to indicate the supply voltages when the main amplifier and the output stage are being operated at the same voltages.

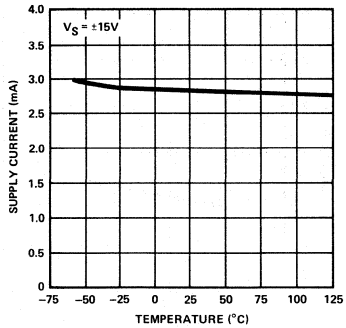
OP-50

TYPICAL PERFORMANCE CHARACTERISTICS

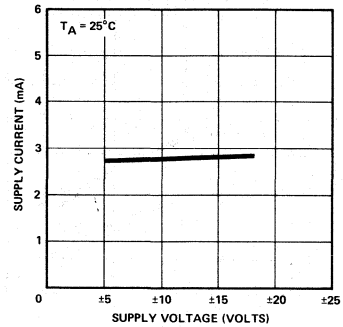
PSRR vs FREQUENCY



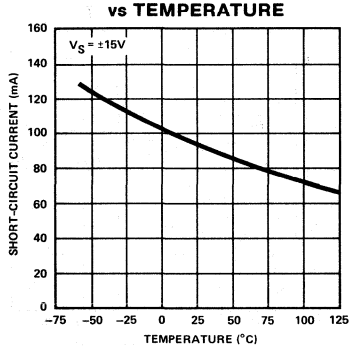
SUPPLY CURRENT vs TEMPERATURE



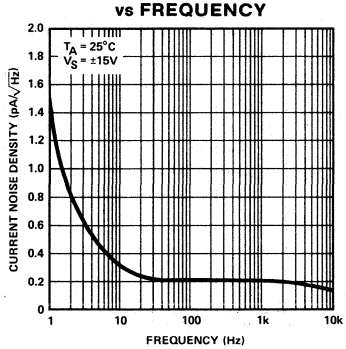
SUPPLY CURRENT vs SUPPLY VOLTAGE



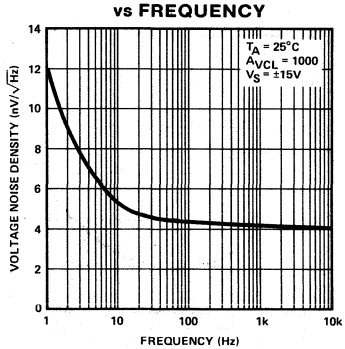
SHORT-CIRCUIT CURRENT vs TEMPERATURE



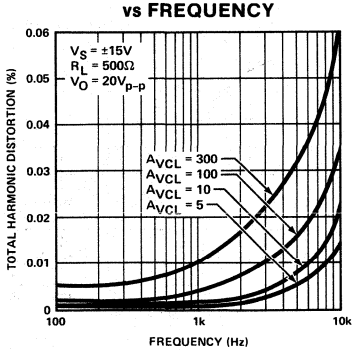
CURRENT NOISE DENSITY vs FREQUENCY



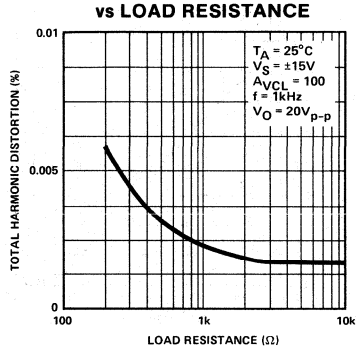
VOLTAGE NOISE DENSITY vs FREQUENCY



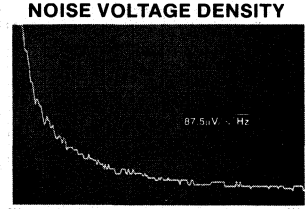
TOTAL HARMONIC DISTORTION vs FREQUENCY



TOTAL HARMONIC DISTORTION vs LOAD RESISTANCE



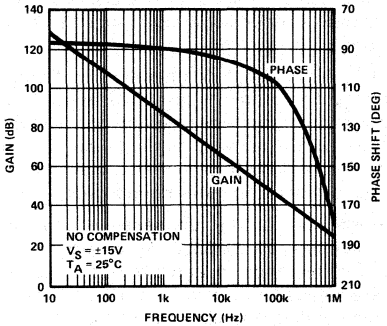
0 TO 1Hz NOISE VOLTAGE DENSITY



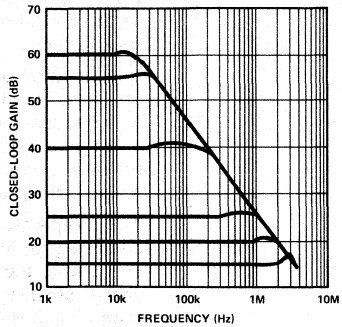
80.0μV FULL SCALE
10.0μV/DIV VERTICAL
A_{VCL} = 10,000

TYPICAL PERFORMANCE CHARACTERISTICS

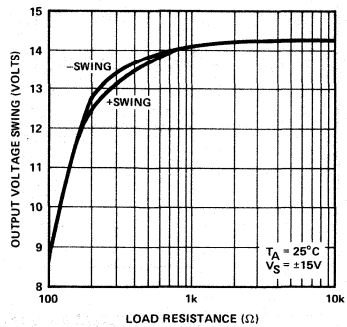
GAIN, PHASE SHIFT vs FREQUENCY



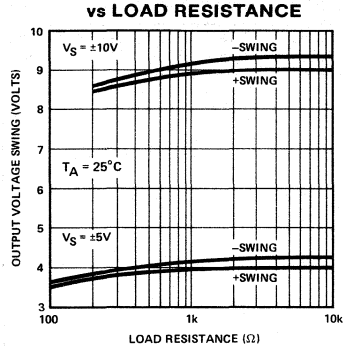
CLOSED-LOOP GAIN vs FREQUENCY



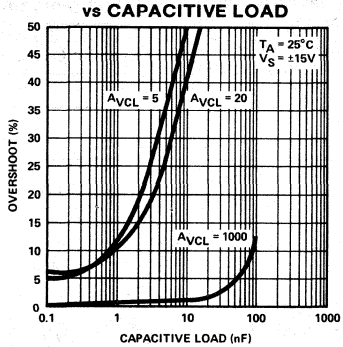
OUTPUT VOLTAGE SWING vs LOAD RESISTANCE



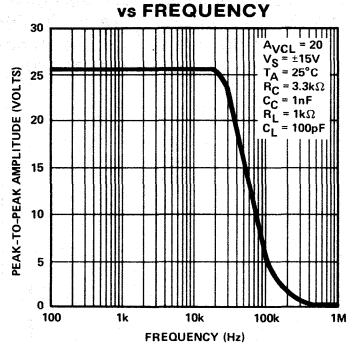
OUTPUT VOLTAGE SWING vs LOAD RESISTANCE



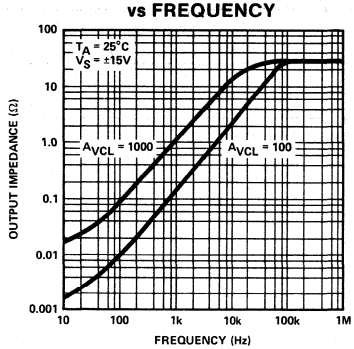
SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD



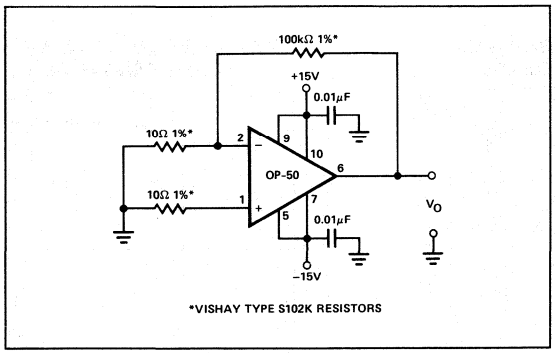
MAXIMUM OUTPUT SWING vs FREQUENCY



OUTPUT IMPEDANCE vs FREQUENCY



TCV_{OS} TEST CIRCUIT



APPLICATIONS INFORMATION

HIGH-SENSITIVITY VOLTAGE COMPARATOR

A comparator capable of resolving a submicrovolt difference signal is shown in Figure 1. The OP-50, operating without feedback, drives a second gain stage which generates a TTL-compatible output signal. Schottky-clamp diodes prevent overdriving of the long-tailed transistor pair and stop saturation of the output transistor. Power supply voltage is set to ±5V to lower the quiescent power dissipation and minimize thermal feedback due to output stage dissipation. Operating from ±5V supplies also reduces the OP-50 rise and fall times as the output slews over a reduced voltage range. This, in turn, reduces the output response time.

It is common practice with voltage comparators to ground one input terminal and to use a single-ended input. The historic reason is poor common-mode rejection on the input stage. In contrast, the OP-50 has very high common-mode rejection and is capable of detecting microvolt level differences in the presence of large common-mode signals.

The comparator is not fast, but it is very sensitive and can detect signal differences as low as 0.3μV. With large input overdrives, the circuit responds in approximately 3μs. If sharp transitions are needed, the use of a TTL Schmitt-trigger input is recommended. A table of Response Time vs. Input Overdrive is shown below.

INPUT OVERDRIVE	100mV	10mV	1mV	100μV	10μV
Positive Output Delay	3.2μs	5μs	40μs	340μs	2.4ms
Negative Output Delay	1.8μs	5μs	50μs	380μs	4.5ms

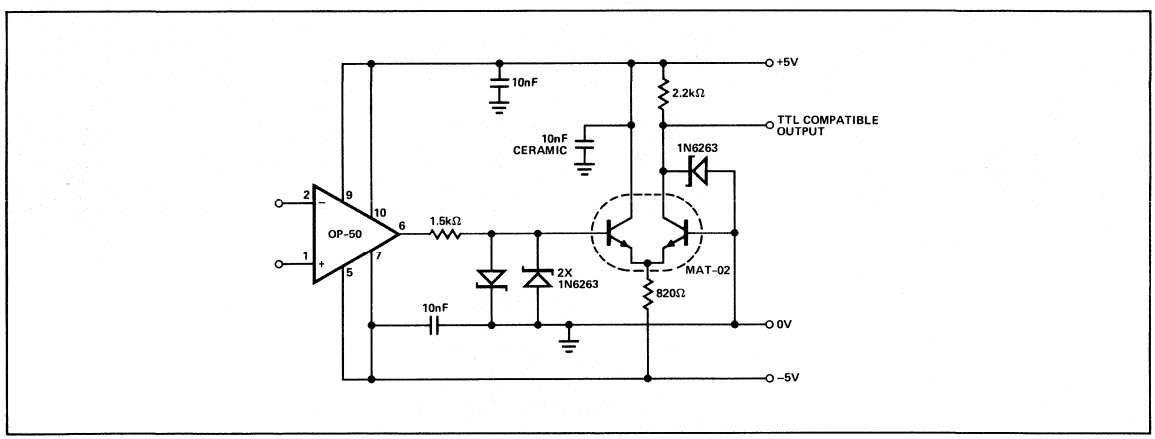


FIGURE 1: HIGH-SENSITIVITY VOLTAGE COMPARATOR

INTEGRATOR AND UNITY-GAIN BUFFER

Figure 2 shows a method of obtaining unity-gain in a buffer configuration. The R1 and C1 network provides input compensation to circumvent the minimum gain requirement. Figure 3 shows the same technique applied in the inverting mode to form a high precision integrator.

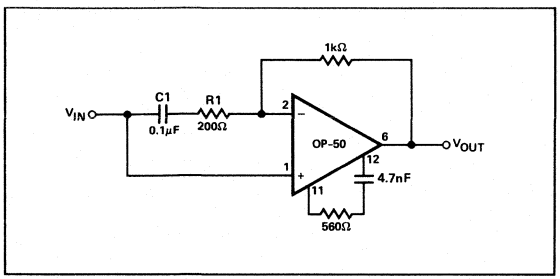


FIGURE 2: UNITY GAIN BUFFER

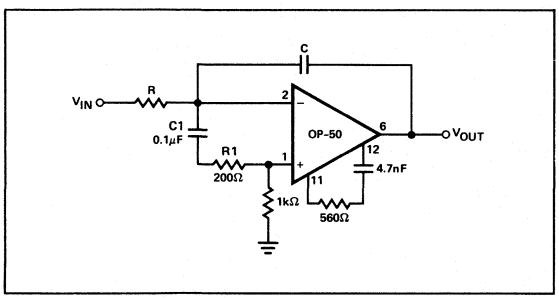


FIGURE 3: INTEGRATOR

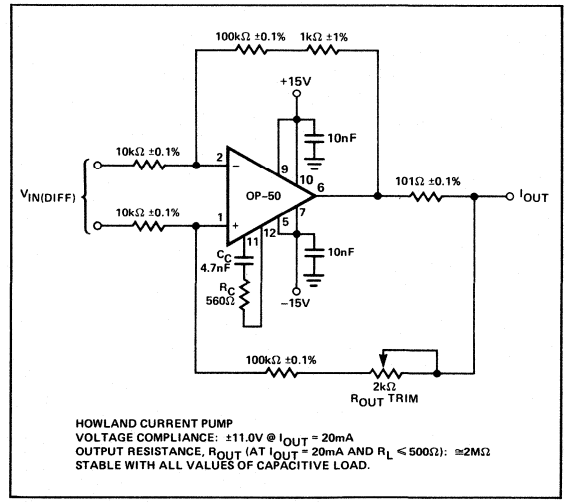
20mA CURRENT SOURCE

The 20mA current source exploits the high output current and high linearity capabilities of the OP-50. Five precision resistors and a trim potentiometer are required in this circuit configuration, known as the Howland Current Pump. The trim potentiometer is used to balance the resistive feedback dividers. This maximizes the current-source output impedance. Compensation is selected for a voltage gain of 10.

Compliance is better than ±11V at an output current of 20mA and the trimmed output resistance is typically 2MΩ with $R_L \leq 500\Omega$. The transfer function is given by:

$$I_{OUT} = \frac{V_{IN\ (DIFF)} \times 10.1}{101}\ \text{Amps}$$

$V_{IN\ (DIFF)}$ is the differential input voltage. For the resistor values shown in Figure 4, the maximum $V_{IN\ (DIFF)}$ is 200mV.



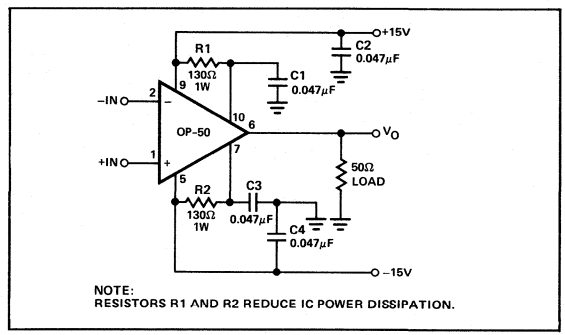
HOWLAND CURRENT PUMP
VOLTAGE COMPLIANCE: ±11.0V @ I_{OUT} = 20mA
OUTPUT RESISTANCE, R_{OUT} (AT I_{OUT} = 20mA AND $R_L \leq 500\Omega$): ≅2MΩ
STABLE WITH ALL VALUES OF CAPACITIVE LOAD.

FIGURE 4: 20mA CURRENT SOURCE

DRIVING 50Ω LOADS

The OP-50 can provide up to 50mA into a 50Ω load and up to 26mA into a 500Ω load. The output is stable driving capacitive loads of up to 10nF.

Applications that make use of the high output current capability of the OP-50 will cause increased power dissipation in the amplifier. To reduce internal dissipation in these applications, external voltage dropping resistors can be connected in series with the output-stage power supply pins. As shown in Figure 5, 130Ω resistors can be attached to pin 7 ($-V_{OP}$) and to pin 10 ($+V_{OP}$). To maintain stability and specified performance levels, 0.047μF decoupling capacitors should be used as indicated from pin 7 and pin 10 to ground.



NOTE:
RESISTORS R1 AND R2 REDUCE IC POWER DISSIPATION.

FIGURE 5: DRIVING 50Ω LOADS

Wide-Bandwidth Precision Operational Amplifier ($A_V \geq 10$)

OP-61

FEATURES

- **High Gain-Bandwidth Product ..... 200MHz Typ**
- **Low Voltage Noise ..... 3.4nV/$\sqrt{Hz}$ @ 1kHz**
- **High Speed ..... 45V/μs Typ**
- **Fast Settling Time (0.01%) ..... 330ns Typ**
- **High Gain ..... 475V/mV Typ**
- **Low Offset Voltage ..... 100μV Typ**

APPLICATIONS

- **Low Noise Preamplifier**
- **Wideband Signal Conditioning**
- **Pulse/RF Amplifiers**
- **Wideband Instrumentation Amplifiers**
- **Active Filters**
- **Fast Summing Amplifiers**

GENERAL DESCRIPTION

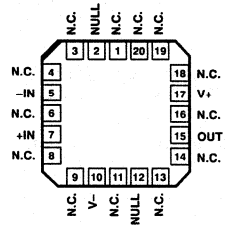
The OP-61 is a wide-bandwidth, precision operational amplifier designed to meet the requirements of fast, precision instrumentation systems. The OP-61's combination of DC accuracy with high bandwidth, fast slew rate and low noise, makes it unique among high-speed amplifiers. It is ideal for wideband systems requiring high signal-to-noise ratio, such as fast 12-16 bit data acquisition systems. The OP-61 maintains less than 3nV/$\sqrt{Hz}$ of input referred spot voltage noise over its closed-loop bandwidth.

The OP-61 offers noise and gain performance similar to that of the industry standard OP-27/37 amplifiers, but maintains a much larger gain-bandwith product of 200MHz. With slew rate exceeding 45V/μs, and settling time for 12 bits (0.01%) typically 330ns, the OP-61 has excellent dynamic accuracy.

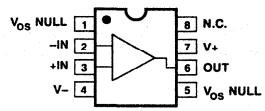
The OP-61 is an excellent upgrade for circuits using slower op amps such as the HA-5111, and the HA-5147. The OP-61 can also be used as a high-speed alternative to the HA-5101, HA-5127, HA-5137, OP-27, and OP-37 amplifiers, where closed-loop gains are greater than 10.

2

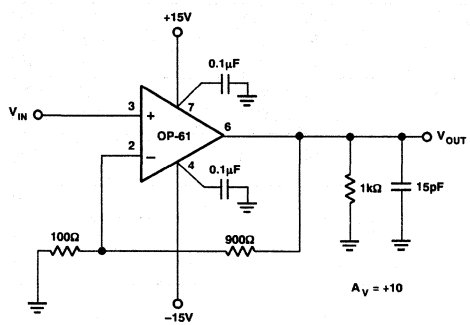
PIN CONNECTIONS

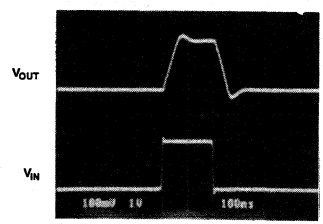


OP-61 ARC/883
20-CONTACT LCC
(RC-Suffix)



EPOXY MINI-DIP
(P-Suffix)
8-PIN CERDIP (Z-Suffix)
8-PIN SO (S-Suffix)





ORDERING INFORMATION †

PACKAGE			OPERATING TEMPERATURE RANGE
CERDIP 8-PIN	PLASTIC 8-PIN	LCC 20-CONTACT	
OP61AZ*	–	OP61ARC/883*	MIL
OP61FZ	OP61GP	–	XIND
–	OP61GS	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, and plastic DIP packages.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage ..... ±18V
Differential Input Voltage ..... ±5.0V
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous

Storage Temperature Range
P, RC, S, Z Package ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature (T_j) ..... 150°C
Operating Temperature Range
All A Grades ..... –55°C to +125°C
F & G Grades ..... –40°C to +85°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNIT
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC (RC)	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOpackage.
2. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted.

			OP-61A			OP-61F			OP-61G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		–	100	500	–	150	750	–	200	1000	µV
Input Offset Current	I_{OS}	V_{CM} = 0V	–	30	150	–	40	200	–	40	200	nA
Input Bias Current	I_B	V_{CM} = 0V	–	130	500	–	200	600	–	200	600	nA
Input Noise Voltage Density	e_n	f_O = 1000Hz	–	3.4	–	–	3.4	–	–	3.4	–	nV/√Hz
Input Noise Current Density	i_n	f_O = 10kHz	–	1.7	–	–	1.7	–	–	1.7	–	pA/√Hz
Input Voltage Range	IVR	(Note 1)	±11.0	–	–	±11.0	–	–	±11.0	–	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	100	108	–	94	100	–	94	100	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5V to ±18V	–	1.2	4.0	–	2.0	5.6	–	2.0	5.6	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L = 10kΩ R_L = 2kΩ R_L = 1kΩ	225 200 150	475 400 340	– – –	175 150 120	425 350 300	– – –	175 150 120	425 350 300	– – –	V/mV
Output Voltage Swing	V_O	R_L = 1kΩ R_L = 500Ω	±12.0 ±11.0	±13.2 ±12.8	– –	±12.0 ±11.0	±13.2 ±12.8	– –	±12.0 ±11.0	±13.2 ±12.8	– –	V
Slew Rate	SR	R_L = 1kΩ C_L = 50pF	40	45	–	35	45	–	35	45	–	V/µs
Gain Bandwidth Prod.	GBWP	f_O = 1MHz	–	200	–	–	200	–	–	200	–	MHz
SettlingTime	t_s	A_V = -10, 10V Step, 0.01%	–	300	–	–	330	–	–	330	–	ns
Supply Current	I_{SY}	No Load	–	6.1	7.5	–	6.1	7.5	–	6.1	7.5	mA

NOTES:
1. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, –55°C ≤ T_A ≤ +125°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-61A MIN	OP-61A TYP	OP-61A MAX	UNITS
Input Offset Voltage	V_{OS}		–	200	1000	µV
Average Input Offset Drift	TCV_{OS}		–	1.0	5.0	µV/°C
Input Offset Current	I_{OS}	V_{CM} = 0V	–	70	400	nA
Input Bias Current	I_B	V_{CM} = 0V	–	180	800	nA
Input Voltage Range	IVR	(Note 1)	±11V	–	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	94	104	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5V to ±18V	–	2.0	5.6	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L = 10kΩ R_L = 2kΩ R_L = 1kΩ	175 150 120	400 340 260	– – –	V/mV
Output Voltage Swing	V_O	R_L ≥ 1kΩ R_L = 500Ω	±11.0 ±10.0	±13.0 ±12.7	– –	V
Supply Current	I_{SY}	No Load	–	6.5	8.0	mA

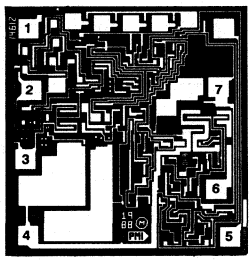
ELECTRICAL CHARACTERISTICS at V_S = ±15V, –40°C ≤ T_A ≤ +85°C.

PARAMETER	SYMBOL	CONDITIONS	OP-61F MIN	OP-61F TYP	OP-61F MAX	OP-61G MIN	OP-61G TYP	OP-61G MAX	UNITS
Input Offset Voltage	V_{OS}		–	300	1250	–	400	1500	µV
Average Input Offset Drift	TCV_{OS}		–	3.0	7.0	–	3.0	7.0	µV/°C
Input Offset Current	I_{OS}	V_{CM} = 0V	–	125	500	–	125	500	nA
Input Bias Current	I_B	V_{CM} = 0V	–	250	900	–	250	900	nA
Input Voltage Range	IVR	(Note 1)	±11V	–	–	±11V	–	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	88	96	–	88	96	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5V to ±18V	–	4.0	10.0	–	4.0	10.0	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L = 10kΩ R_L = 2kΩ R_L = 1kΩ	150 120 100	350 300 240	– – –	150 120 100	350 300 240	– – –	V/mV
Output Voltage Swing	V_O	R_L = 1kΩ R_L = 500Ω	±11.0 ±10.0	±13.0 ±12.7	– –	±11.0 ±10.0	±13.0 ±12.7	– –	V
Supply Current	I_{SY}	No Load	–	6.4	8.0	–	6.4	8.0	mA

NOTES:
1. Guaranteed by CMR test.

OP-61

DICE CHARACTERISTICS



DIE SIZE 0.064 x 0.068 inch, 4,352 sq. mils
(1.63 x 1.73 mm, 2.81 sq. mm)

1. V_{OS} NULL
2. –IN
3. +IN
4. V–
5. V_{OS} NULL
6. OUT
7. V+

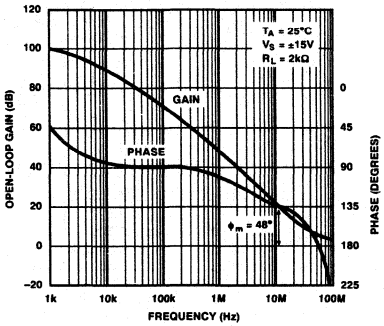
WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$.

PARAMETER	SYMBOL	CONDITIONS	OP-61GBC LIMITS	UNITS
Input Offset Voltage	V_{OS}		750	µV MAX
Input Offset Current	I_{OS}		200	nA MAX
Input Bias Current	I_B		600	nA MAX
Input Voltage Range	IVR		±11.0	V MIN
Common-Mode Rejection	CMR`	$V_{CM} = \pm 11V$	94	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 18V$	5.6	µV/V MAX
Large-Signal Voltage Gain	A_{VO}	$R_L = 10k\Omega$ $R_L = 2k\Omega$ $R_L = 1k\Omega$	175 150 120	V/mV MIN
Output Voltage Swing	V_O	$R_L = 1k\Omega$ $R_L = 500\Omega$	±12.0 ±11.0	V MIN
Slew Rate	SR	$R_L = 1k\Omega$ $C_L = 50pF$	35	V/µs MIN
Supply Current	I_{SY}	No Load	7.5	mA MAX

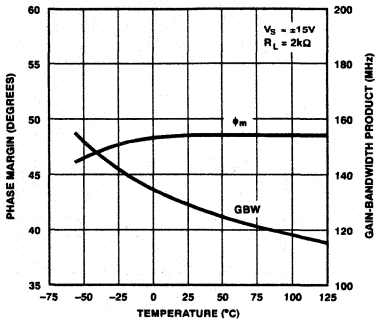
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

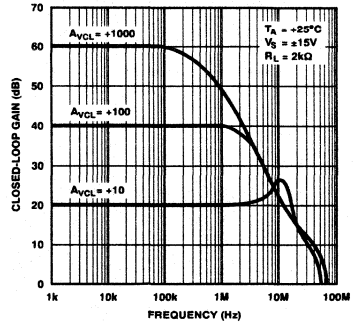
OPEN-LOOP GAIN, PHASE vs FREQUENCY



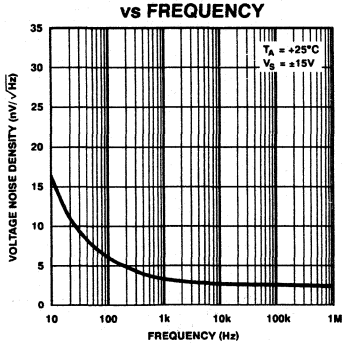
GAIN-BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE



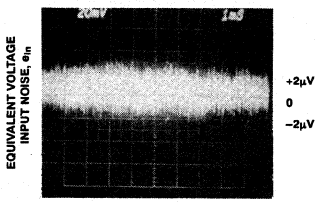
CLOSED-LOOP GAIN vs FREQUENCY



VOLTAGE NOISE DENSITY vs FREQUENCY

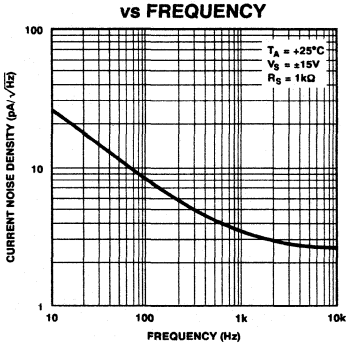


WIDEBAND PEAK-TO-PEAK VOLTAGE NOISE

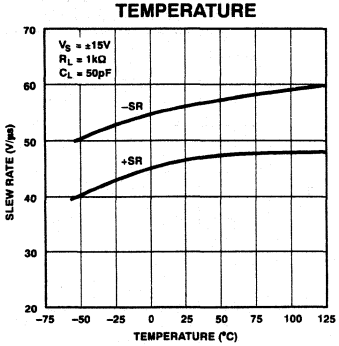


BANDWIDTH: 1kHz TO 100kHz
T_A = +25°C
V_S = ±15V

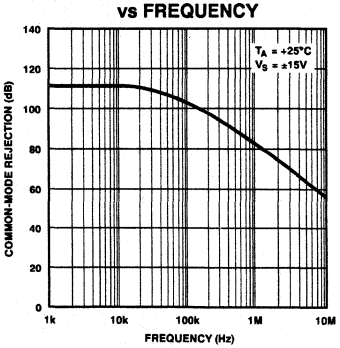
CURRENT NOISE DENSITY vs FREQUENCY



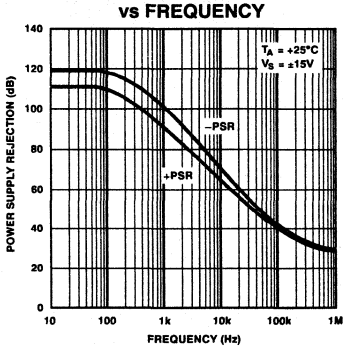
SLEW RATE vs TEMPERATURE



COMMON-MODE REJECTION vs FREQUENCY

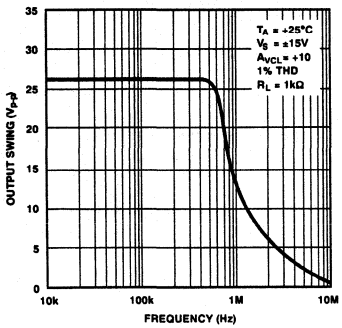


POWER SUPPLY REJECTION vs FREQUENCY

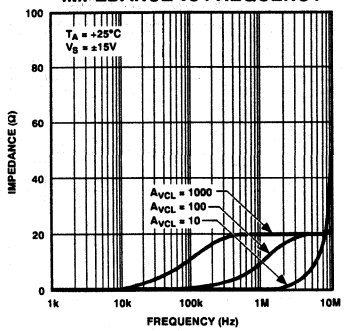


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

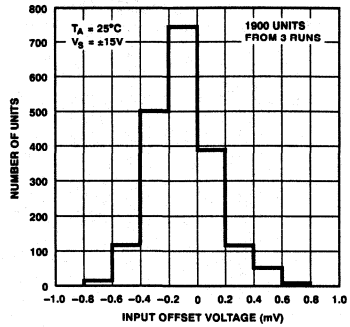
MAXIMUM OUTPUT SWING vs FREQUENCY



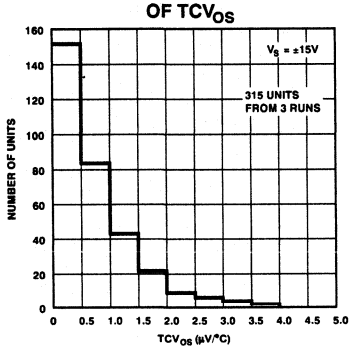
CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



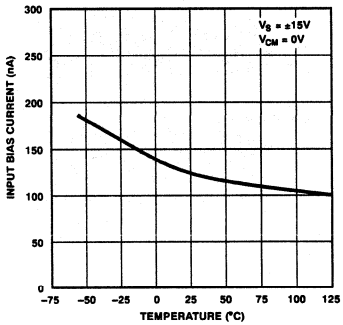
TYPICAL DISTRIBUTION OF INPUT OFFSET VOLTAGE



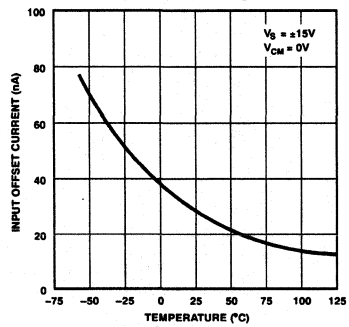
TYPICAL DISTRIBUTION OF TCV_{OS}



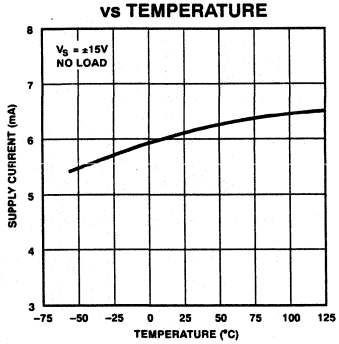
INPUT BIAS CURRENT vs TEMPERATURE



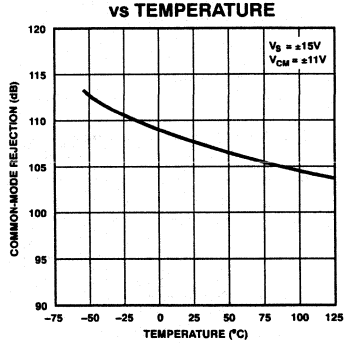
INPUT OFFSET CURRENT vs TEMPERATURE



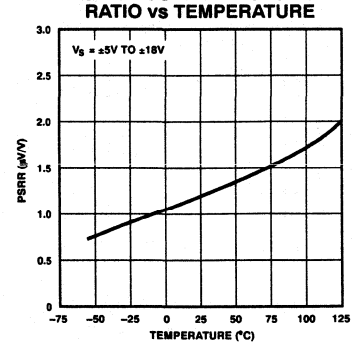
SUPPLY CURRENT vs TEMPERATURE



COMMON-MODE REJECTION vs TEMPERATURE

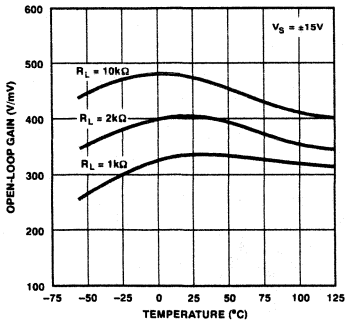


POWER SUPPLY REJECTION RATIO vs TEMPERATURE

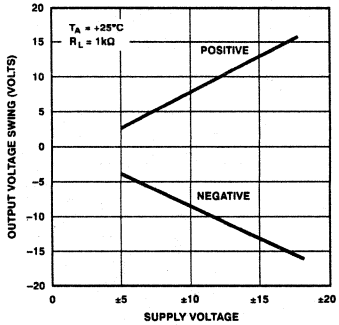


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

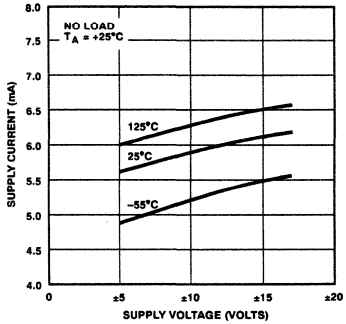
OPEN-LOOP GAIN vs TEMPERATURE



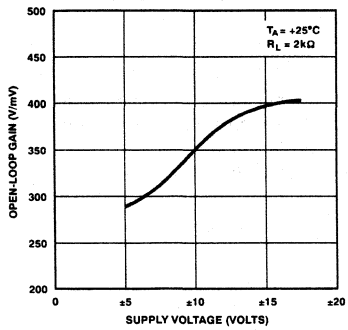
OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE



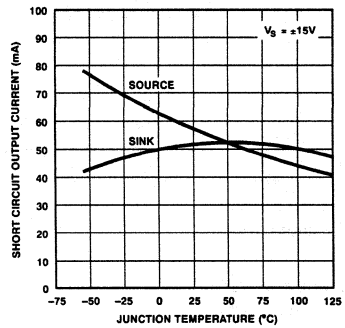
SUPPLY CURRENT vs SUPPLY VOLTAGE



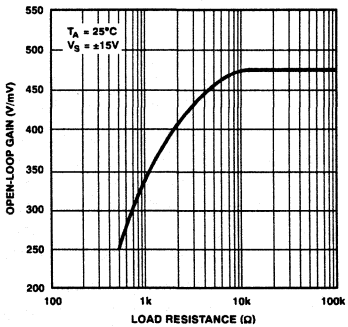
OPEN-LOOP GAIN vs SUPPLY VOLTAGE



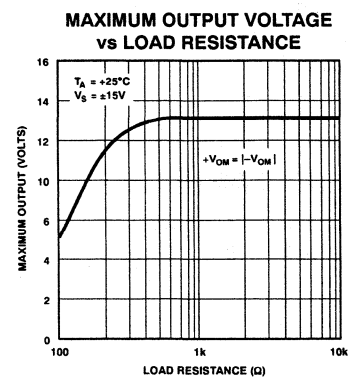
SHORT CIRCUIT OUTPUT CURRENT vs JUNCTION TEMPERATURE



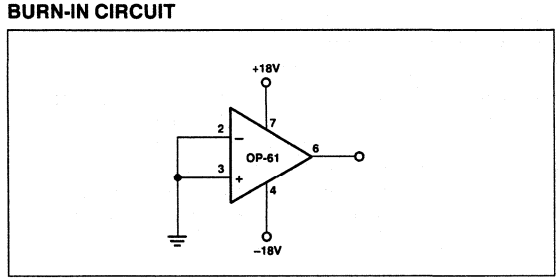
OPEN-LOOP GAIN vs LOAD RESISTANCE



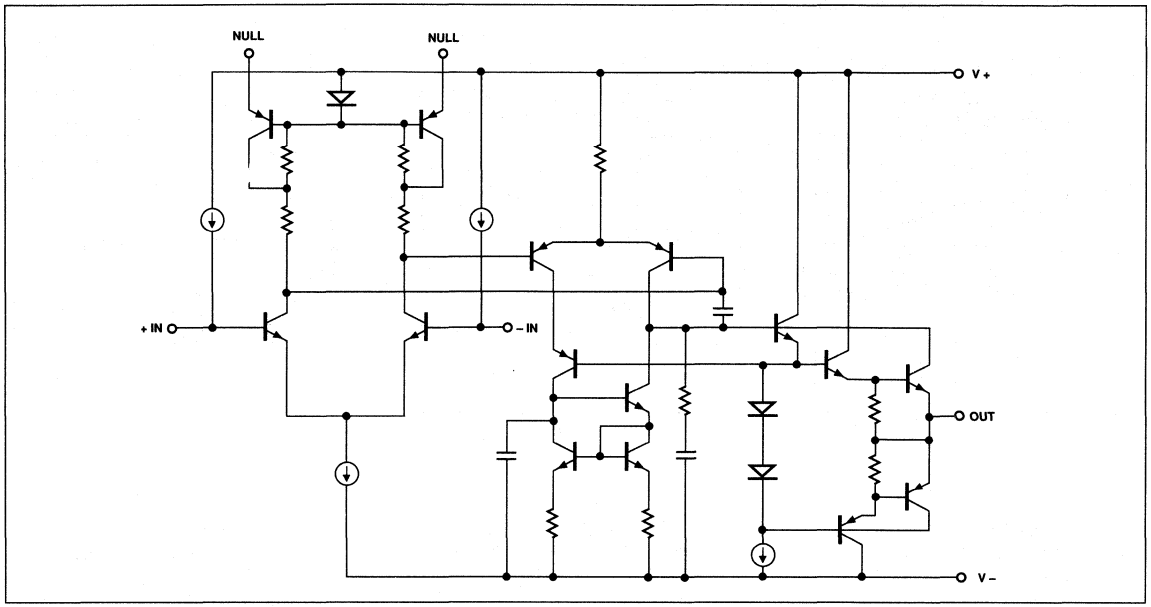
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



BURN-IN CIRCUIT



SIMPLIFIED SCHEMATIC



APPLICATIONS INFORMATION

The OP-61 combines high speed with a level of precision and noise performance normally only found with slower amplifiers. Data acquisition and instrumentation technology has progressed to where dynamic accuracy and high resolution are both maintained to a very high level. The OP-61 was specifically designed to meet the stringent requirements of these systems.

Signal-to-noise ratio degrades as input referred noise or bandwidth increases. The OP-61 has a very wide bandwidth, but its input noise is only $3nV/\sqrt{Hz}$. This makes the total noise generated over its closed-loop bandwidth considerably less than previously available wideband operational amplifiers.

The OP-61 provides stable operation in closed-loop gain configurations of 10 or more. Large load capacitances should be decoupled with a resistor placed inside the feedback loop (see Driving Large Capacitive Loads).

OFFSET VOLTAGE ADJUSTMENT

Offset voltage can be adjusted by a potentiometer of 10kΩ to 100kΩ resistance. This potentiometer should be connected between pins 1 and 5 with the wiper connected directly to the OP-61 V+ pin (see Figure 1). By connecting this line directly to the op amp V+ terminal, common impedance paths shared by both return currents and the null inputs will be avoided. Nulling inputs to any op amp are simply another set of sensitive differentially balanced inputs. Therefore, care must always be exercised in laying out signal paths by not placing the trimmer, or the nulling input lines, directly adjacent to high frequency signal lines.

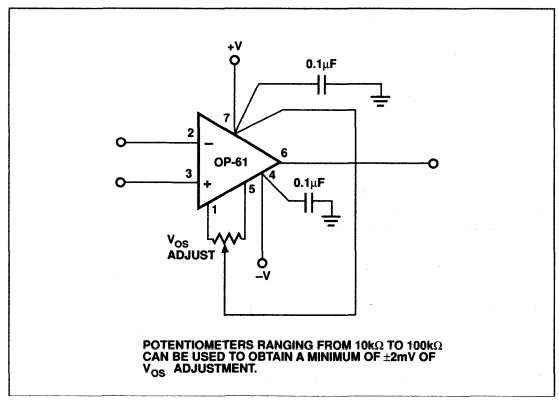


FIGURE 1: *Input Offset Voltage Nulling*

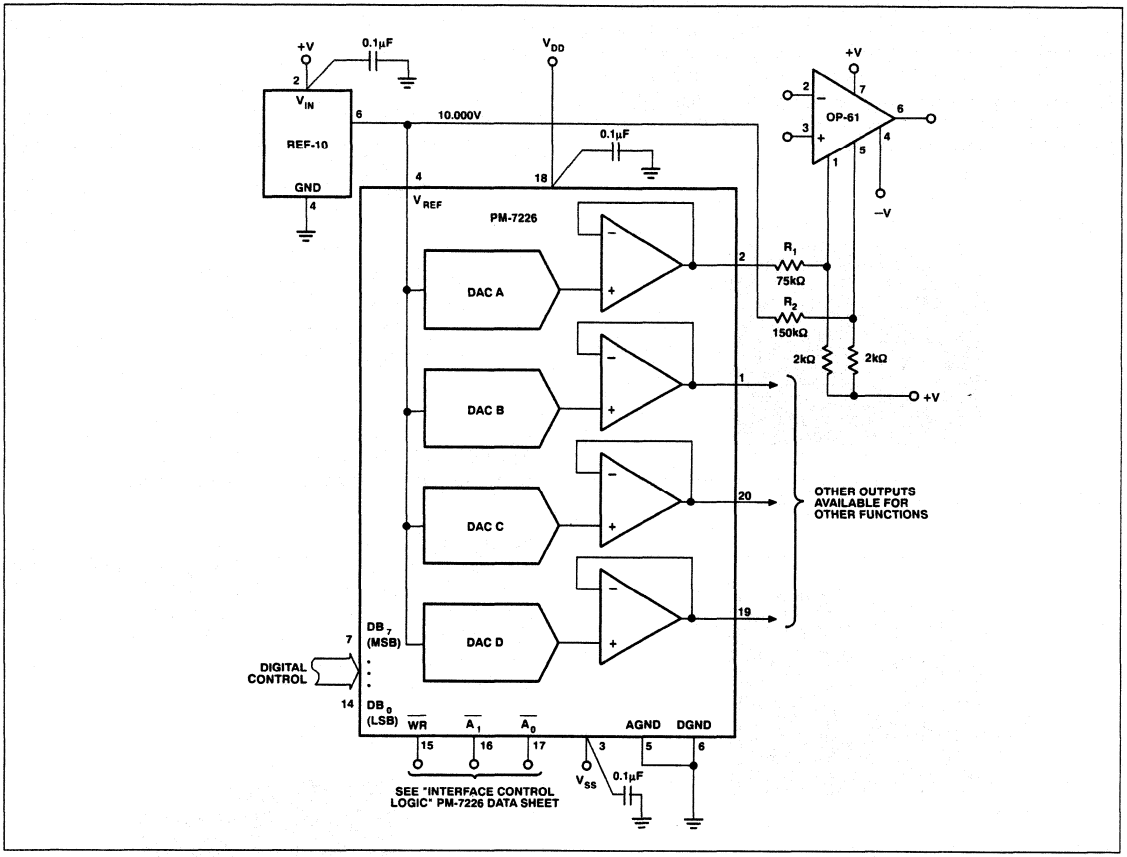


FIGURE 2: *Trimming OP-61 Voltage Offset with 0 to 10V Voltage Output, PM-7226 Quad D/A*

D/A converters can also be used for offset adjustments in systems that are microprocessor controlled. Figure 2 illustrates a PM-7226 quad, 8-bit D/A, used to null the OP-61's offset voltage. A stable fixed bias current is provided into pin 5 of the OP-61, from R_2, and a REF-10, +10V precision voltage reference. Current through R_1, from the D/A voltage output provides the programmed V_{OS} adjustment control. Symmetric control of the offset adjustment is effected since equal currents are sourced into R_1 and R_2 when the D/A is at half scale, binary input code = 10000000.

With the circuit components shown in Figure 2, the maximum V_{OS} adjustment range is ±500mV, referred to the input of the OP-61. Incremental adjustment range is approximately 2µV per bit, allowing V_{OS} to be trimmed to ±2µV.

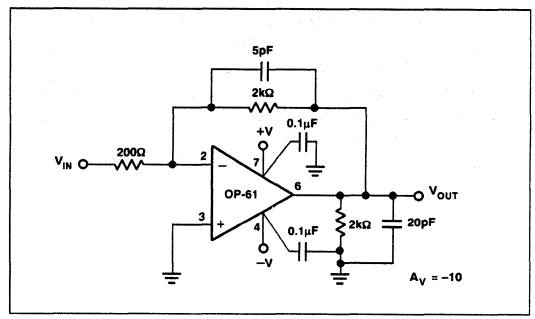


FIGURE 3: *Large- and Small-Signal Response Test Circuit*

TRANSIENT RESPONSE PERFORMANCE

Figures 4 and 5, respectively, show the small-signal and large-signal transient response of the OP-61 driving a 20pF load from the circuit in Figure 3. Both waveforms are symmetric and exhibit only minimal overshoot. The slew rate symmetry, apparent from the large-signal response, decreases the DC offsets that occur when processing input signals that extend outside the range of the OP-61's full-power bandwidth.

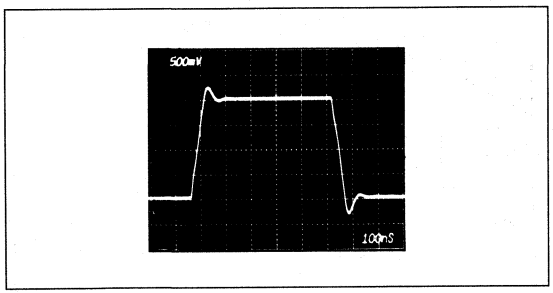


FIGURE 4: *Small-Signal Transient Response*

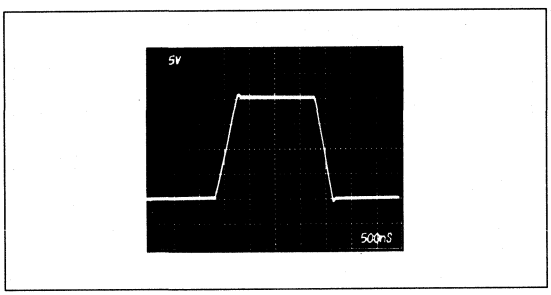


FIGURE 5: *Large-Signal Transient Response*

DRIVING CAPACITIVE LOADS

Direct capacitive loading will reduce the phase margin of any op amp. A pole is created by the combination of the op amp's output impedance and the capacitive load that induces phase lag and reduces stability. However, high-speed amplifiers can easily drive a capacitive load indirectly. This is shown in Figure 6. The OP-61 is driving a 1000pF capacitive load. R_1 and C_1 serve to counteract the loss of phase margin by feedforwarding a small amount of high frequency output signal back to the amplifier's inverting input,

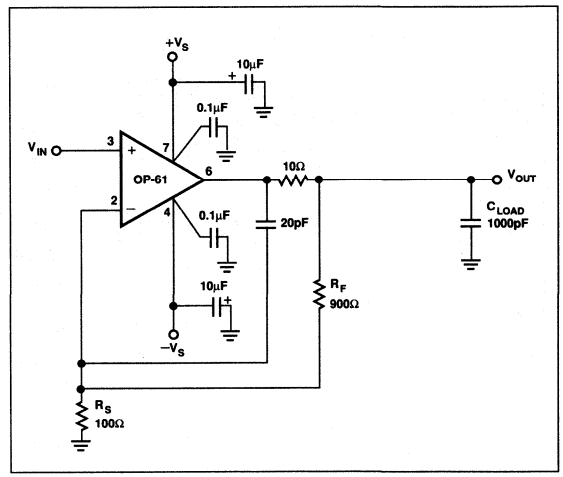


FIGURE 6: *OP-61 Noninverting Gain of 10 Amplifier, Compensated to Handle Large Capacitive Loads*

thereby preserving adequate phase margin. The resulting pulse response can be seen in Figure 7. Extra care may be required to ensure adequate decoupling by placing a 1µF to 10µF capacitor in parallel with the existing decoupling capacitor. Adequate decoupling ensures a low impedance path for high frequency energy transferred from the decoupling capacitors through the amplifier's output stage to a reactive load.

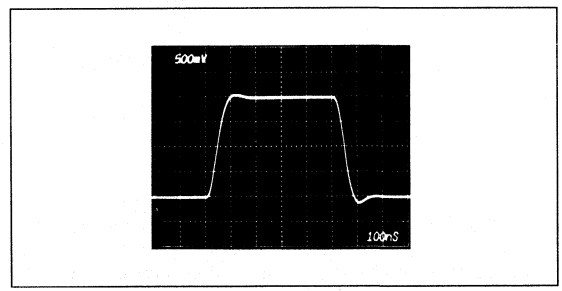


FIGURE 7: *Pulse Response of Compensated X10 Amplifier in Figure 6, V_{IN} = 100mV_{p-p}, V_{OUT} = 1V_{p-p}, Frequency of Square Wave = 1MHz, C_{LOAD} = 1000pF!*

DECOUPLING AND LAYOUT GUIDELINES

The OP-61 op amp is a superb choice for a wide range of precision high-speed, low noise amplifier applications. However, care must be exercized in both the design and layout of high-speed circuits in order for the specified performance to be realized.

Although the OP-61 has excellent power supply rejection over a wide bandwidth, the negative supply rejection is limited at high frequencies since the amplifier's internal integrator is biased via the negative supply line. This operation is typical performance for all monolithic op amps, and not unique to the OP-61. Since the negative supply rejection will approach zero for signals above the close-loop bandwidth, high-speed transients and wideband power supply noise, on the negative supply line, will result in spurious signals being directly added to the amplifier's output. Adequate power supply decoupling prevents this problem.

Generally, a 0.1μF tantalum decoupling capacitor, placed in close proximity across the amplifier's actual power supply pin and ground is recommended. This will satisfy most decoupling requirements, especially when the circuit is built on a low impedance ground plane. When a heavy copper clad ground plane is not used, it becomes especially important to confine the high frequency output load currents confined to as small a high-frequency signal path as possible, as suggested in Figure 8.

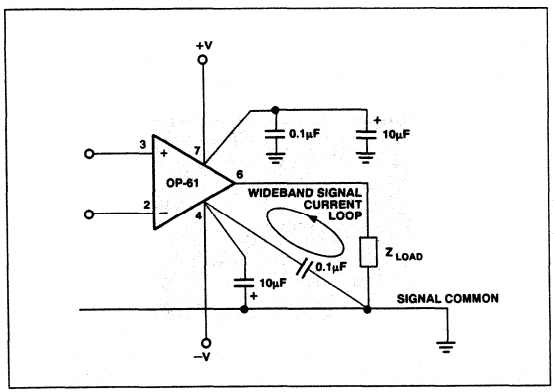


FIGURE 8: *Proper power supply bypassing is required to obtain optimum performance with the OP-61. Maintain as small wideband signal current path as possible. Where signal common is a low impedance ground plane, simply decouple 0.1μF to ground plane near the OP-61.*

Power management of complex systems sometimes results in a complex L-C network that has high frequency natural resonances that cause stability problems in circuits internal to the system. Resistors added in series to the supply lines can lower the Q of the undesired resonances, preventing oscillations on the supply lines. Resistors of 3 to 10 ohms work well and serve to ensure the stability of the OP-61 in such systems.

ADDITIONAL CAVEATS FOR HIGH-SPEED AMPLIFIERS INCLUDE:

1. Keep all leads as short as possible, using direct point-to-point wiring. Do not wire-wrap or use "plug-in" boards for prototyping circuits.
2. Op amp feedback networks should be placed in close proximity to the amplifiers inputs. This reduces stray capacitance that compromises stability margins.
3. Maintain low feedback and source resistance values. Impedance levels greater than several kilo-ohms may result in degrading the amplifier's overall bandwidth and stability.
4. The use of heavy ground planes reduces stray inductance, and provides a better return path for ground currents.
5. Decoupling capacitors must have short leads and be placed at the amplifier's supply pins. Use low equivalent series resistance (ESR) and low inductance chip capacitors wherever possible.
6. Evaluation of prototype circuits should be performed with a low input capacitance, X10 compensated oscilloscope probe. X1 uncompensated probes introduce excessive stray capacitance which alters circuit characteristics by introducing additional phase shifts.
7. Do not directly drive either large capacitive loads or coax cables with high-speed amplifiers (see DRIVING COAXIAL CABLES).
8. Watch out for parasitic capacitances at the +/– inputs to wideband noninverting op amp circuits. Since these nodes are not maintained at virtual ground as in the inverting amplifier configuration, parasitics may degrade bandwidth. Wideband noninverting amplifiers may require the ground plane trace removed from local proximity to the op amp's inputs.

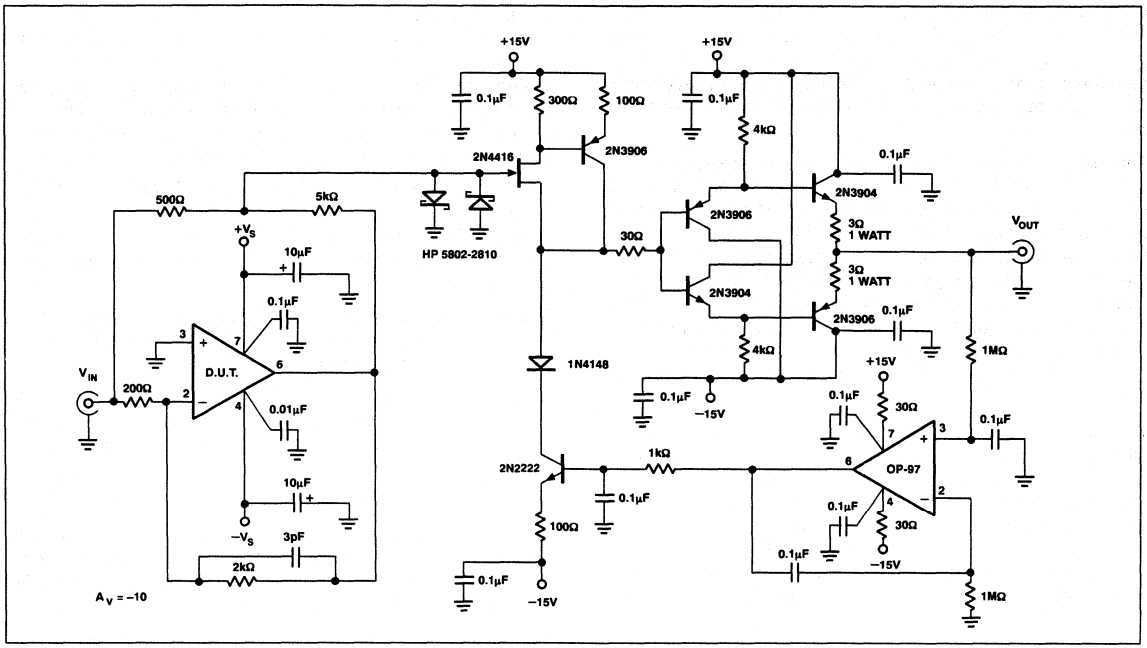


FIGURE 9: *High-Speed Settling Time Fixture (for 0.1 and 0.01%)*

SETTLING TIME

Settling time is the time between when the input signal begins to change and when the output permanently enters a prescribed error band. Figure 9 illustrates the artificial summing node test configuration, used to characterize the OP-61 settling time. The OP-61 is set in a gain of −10 with a 1.0V step input.The error bands on the output are 5mV and 0.5mV, respectively, for 0.1% and 0.01% accuracy.

The test circuit, built on a copper clad circuit board, has a FET input stage which maintains extremely low loading capacitance at the artificial sum node. Preceeding stages are complementary emitter follower stages, providing adequate drive current for a 50Ω oscilloscope input. The OP-97 establishes biasing for the input stage, and eliminates excessive offset voltage errors.

Figure 10 illustrates the OP-61's typical settling time of 330ns. Moreover, problems in settling response, such as thermal tails and long-term ringing are nonexistent. This performance of the OP-61 makes it a suberb choice for systems demanding both high sampling rates and high resolution.

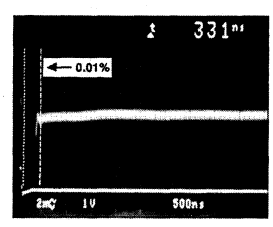


FIGURE 10: *Settling Characteristics of the OP-61 to 0.01%. No Thermal Settling Tail Appears as Part of the Settling Response.*

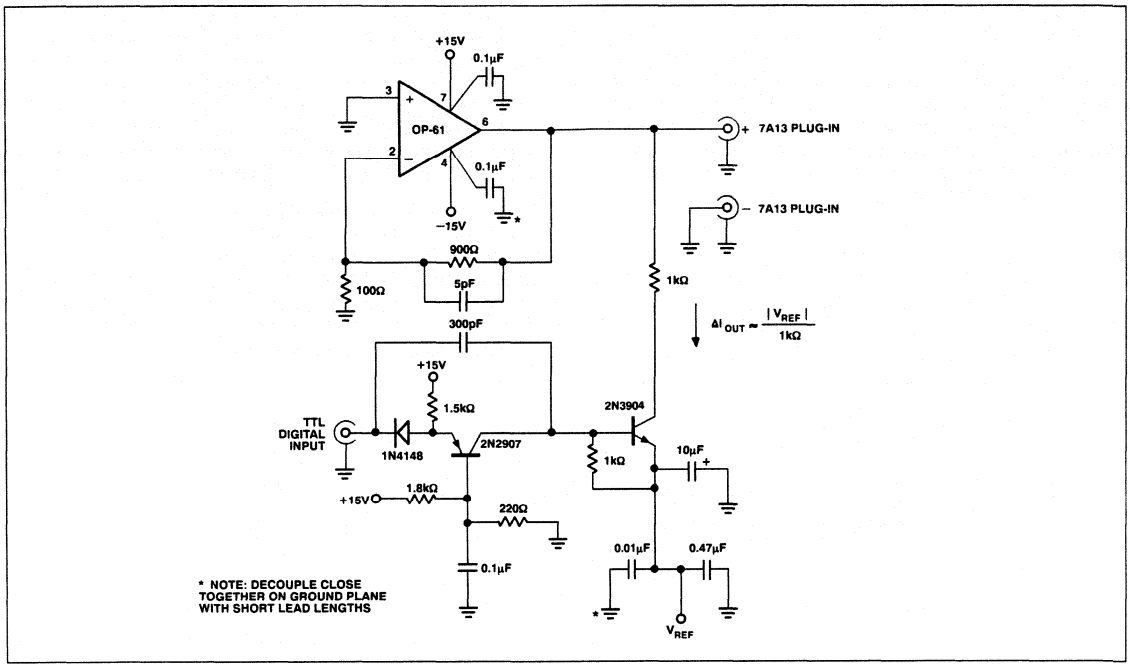


FIGURE 11: *Transient Output Impedance Test Fixture*

TRANSIENT OUTPUT IMPEDANCE

Settling characteristics of operational amplifiers also includes an amplifier's ability to recover, i.e., settle, from a transient current output load condition. An example of this includes an op amp driving the input from a SAR type A/D converter. Although the comparison point of the converter is usually diode clamped, the input swing of plus-and-minus a diode drop still gives rise to a significant modulation of input current. If the closed-loop output impedance is low enough and bandwidth of the amplifier is sufficiently large, the output will settle before the converter makes a comparison decision which will prevent linearity errors or missing codes.

Figure 11 shows a settling measurement circuit for evaluating recovery from an output current transient. An output disturbing current generator provides the transient change in output load current of 1mA. As seen in Figure 12, the OP-61 has extremely fast recovery of 180ns, (to 0.01%), for a 1mA load transient. The performance makes it an ideal amplifier for data acquisition systems.

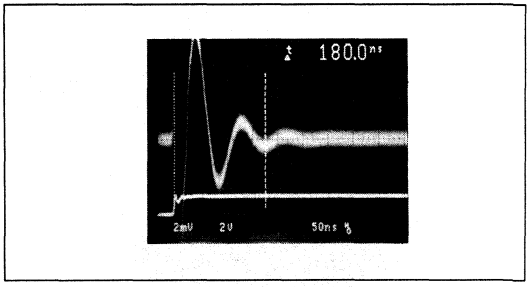


FIGURE 12: *OP-61's Extremely Fast Recovey Time from a 1mA Load Transient to 0.01%*

DRIVING COAXIAL CABLES

The OP-61 amplifier, and a BUF-03 unity-gain buffer, make an excellent drive circuit for 75Ω or 50Ω coaxial cables. To maintain optimum pulse response, and minimum reflections, op amp circuits driving coaxial cables should be terminated at both ends. Unterminated cables can appear as a resonant load to the amplifier, degrading stability margins. Also, since coaxial cables represent a significant capacitive load shunting the driving amplifier, it is not possible to drive them directly from the op amp's output (RG-58 coax. typically has 33pF/foot of capacitance).

Figure 13 illustrates an OP-61 noninverting, gain of 10, amplifier stage, driving a double-matched coaxial cable. Since the double-matching of the cable results in voltage gain loss of 6dB, the composite voltage gain of the entire circuit is 5, or 14dB.

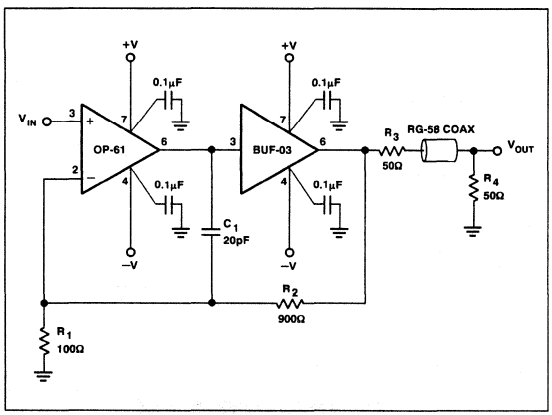


FIGURE 13: *OP-61 Noninverting Amplifier Driving Coaxial Cable, Composite Gain = 5 from V_{IN} to V_{OUT}. Adjust C_1 for Desired Pulse Response.*

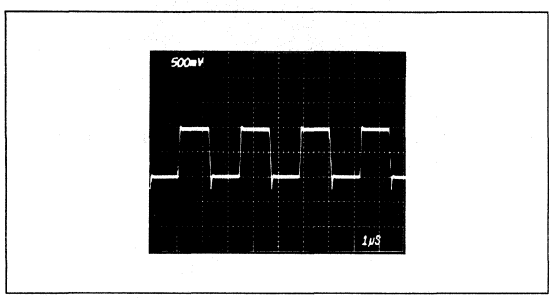


FIGURE 14: *Pulse Response from Amplifier Circuit in Figure 13, Driving 15 Ft. of RG-58 Coaxial Cable*

Resistors R_3 and R_4 serve to absorb reflections at both ends of the cable. The OP-61's wide bandwidth and fast symmetric slewing, results in a very clean pulse reponse, as can be seen in Figure 15. The BUF-03 serves to increase the output current capability to 70mA peak, and the ability to drive up to a 1µF capacitive load (or a longer cable). The value of C_1 may need to be slightly adjusted to provide an optimum value of phase lead, or pulse response. This capacitor serves to correct for the current buffers phase lag, internal to the OP-61's feedback loop.

NOISE MODEL AND DISCUSSION

The OP-61's exceptionally low voltage noise (e_n = 3.0nV/Hz, high open-loop gain, and wide bandwidth makes it ideal for accurately amplifying wideband low-level signals. Figure 15a shows the OP-61 cleanly amplifying a 5mV$_{p-p}$, 1MHz sine wave, with inverting gain of 100. Noise or limited bandwidth prevents most amplifiers from achieving this performance.

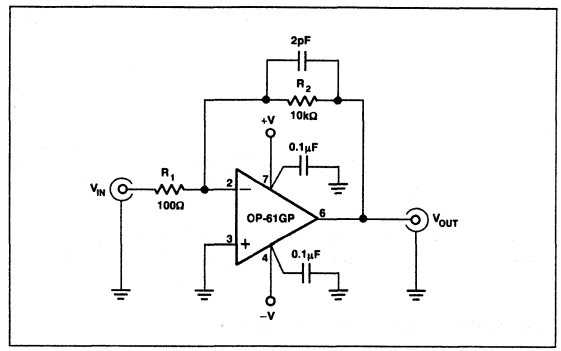


FIGURE 15a: *Example of Low Level Amplifier in an Inverting Configuration, Gain = V_{OUT}/V_{IN} = $-R_2/R_1$ = –100*

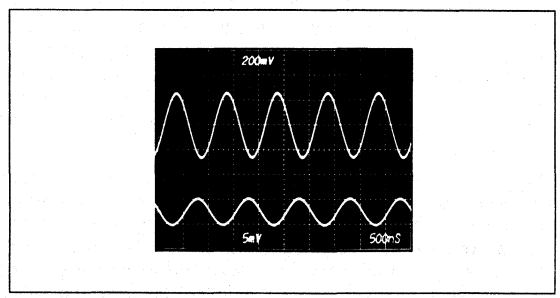


FIGURE 15b: *OP-61, Gain = –100.0, Wideband Amplifier, V_{IN} = 5mV$_{p-p}$ Signal at 1MHz, V_{OUT} = 500mV$_{p-p}$*

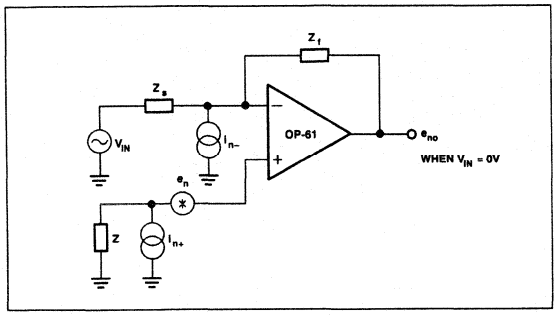


FIGURE 16: *Inverting Gain Configuration Noise Model for the OP-61*

The inverting amplifier model, seen in Figure 16, can be used to calculate the equivalent input noise, e_{ni}. e_{ni} is the voltage noise, modeled as part of the input signal. It represents all the current and voltage noise sources lumped into one equivalent input voltage.

Typical values for the OP-61 noise parameters are:

$e_n = 3.4nV/\sqrt{Hz}$ @ 1kHz

$i_n = 1.7pA/\sqrt{Hz}$ @ 10kHz

(where it is assumed that $i_n- = i_n+$).

It can be defined from the model in Figure 16:

e_{ni} = total input referred spot voltage noise (all noise contributions lumped into one equivalent voltage noise source).

e_n = spot voltage noise of OP-61

i_n = spot current noise of OP-61

Z_S = total input impedance

Z = impedance at OP-61 + input node

A_{VCL} = closed-loop gain for inverting amplifier

N.G. = $1 + |A_{VCL}|$ = noise gain for inverting amplifier

i_{ZS} = spot noise current generated by Z_s. If $Z_s = R_s$, then

$i_{ZS} = i_{RS} = 0.129\sqrt{(1/R_S)}$ nV/$\sqrt{Hz}$.

e_{Zf} = spot voltage noise generated by Z_f. If $Z_f = R_f$,

then $e_{Zf} = e_{Rf} = 0.129\sqrt{R_f}$ nV/$\sqrt{Hz}$.

Note: Equation is derived from Johnson noise relationship of resistor R:

$e_R = \sqrt{4kTR} = \sqrt{4kT}\sqrt{R} = 0.129\sqrt{R}$ nV/$\sqrt{Hz}$. R is in ohms.

The equivalent input voltage noise, referred to the output, can be found by adding all the noise sources in a sum-of-square fashion:

$$e_{no}^2 = e_n^2 (N.G.)^2 + i_n^2 |Z|^2 (N.G.)^2 + i_n^2 |Z_f|^2 + i_{ZS}^2 |Z_f|^2 + e_{Zf}^2$$

Referred back to the amplifiers input:

$$e_{ni} = \frac{e_{no}}{|A_{VCL}|} =$$

$$\frac{\sqrt{(e_n^2 (N.G.)^2 + i_n^2 |Z|^2 (N.G.)^2 + i_n^2 |Z_f|^2 + i_{ZS}^2 |Z_f|^2 + e_{Zf}^2)}}{|A_{VCL}|}$$

To capitalize on the low voltage performance of the OP-61, Z, Z_f and especially Z_S must be as low impedance as possible. With low impedance values of Z_f and Z_S:

$$e_{ni} \cong \frac{\sqrt{e_n^2 (1 + |A_{VCL}|)^2}}{|A_{VCL}|} \text{ or, } e_{ni} \cong \frac{e_n (N.G.)}{(N.G.) - 1}$$

All noise contributions are now easily modelled as a signal equivalent noise voltage source, e_{ni} (see Figure 17).

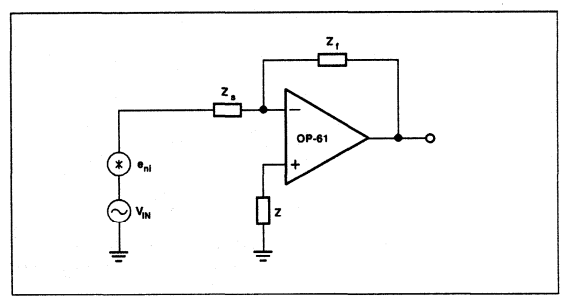


FIGURE 17: *Equivalent Noise Model, Where All Noise Contributions are Lumped Into e_{ni}*

OP-61 SPICE MACROMODEL

Figures 18 and 19 show the node and net list for a SPICE macromodel of the OP-61. The model is a simplified version of the actual device and simulates important DC parameters such as V_{OS}, I_{OS}, I_B, A_{VO}, CMR, V_O and I_{SY}. AC parameters such as slew rate, gain and phase reponse and CMR change with frequency are also simulated by the model.

The model uses typical parameters for the OP-61. The poles and zeros in the model were determined from the actual open and closed-loop gain and phase reponse of the OP-61. In this way the model presents an accurate AC representation of the actual device. The model assumes an ambient temperature of 25°C (see following pages).

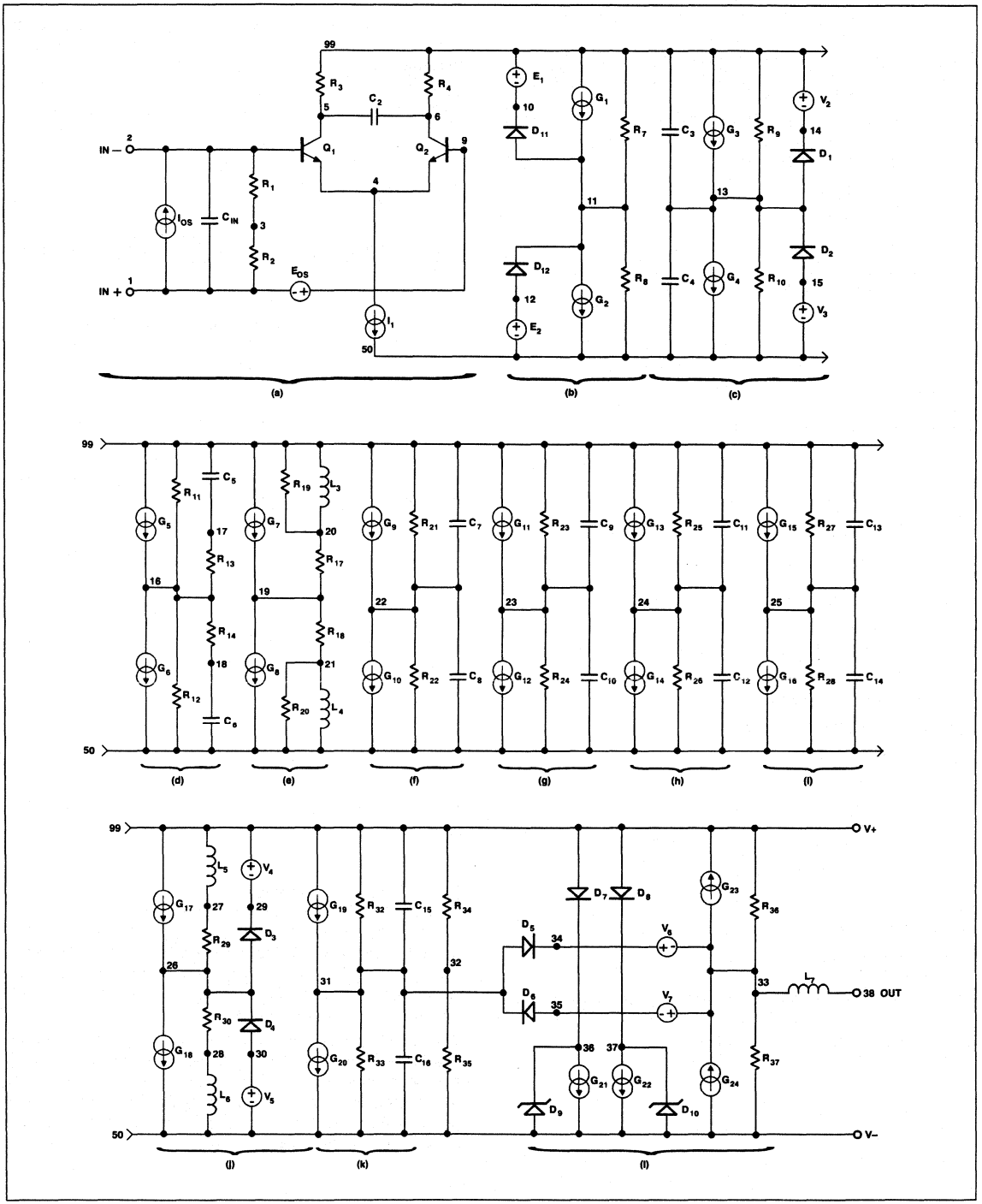


FIGURE 18: *OP-61 SPICE Macro-Model Schematic and Node List*

```
OP-61 MACROMODEL AND TEST CIRCUIT © ADI 1990
*
* subckt OP-61 1  2 38  99  50
*
* INPUT STAGE & POLE AT 300 MHz
*
r1   2   3        5E11
r2   1   3        5E11
r3   5   99       51.6
r4   6   99       51.6
cin  1   2        5E-12
c2   5   6        5.141E-12
i1   4   50       1E-3
ios  1   2        2E-7
eos  9   1        poly(1) 26 32 400E-6 1
q1   5   2   4    qx
q2   6   9   4    qx
*
* FIRST GAIN STAGE
*
r7   11  99       1E6
r8   11  50       1E6
d11  11  10       dx
d12  12  11       dx
g1   99  11       5 6 2E-4
g2   11  50       6 5 2E-4
e1   99  10       poly(1) 99 32 –4.4 1
e2   12  50       poly(1) 32 50 –4.4 1
*
* SECOND GAIN STAGE & POLE AT 2.5kHz
*
r9   13  99       5.1598E6
r10  13  50       5.1598E6
c3   13  99       12.338E-12
c4   13  50       12.338E-12
g3   99  13       poly(1) 11 32 4.24E-3 9.69E-5
g4   13  50       poly(1) 32 11 4.24E-3 9.69E-5
v2   99  14       2.3
v3   15  50       2.3
d1   13  14       dx
d2   15  13       dx
*
* POLE-ZERO PAIR AT 4MHz / 8MHz
*
r11  16  99       1E6
r12  16  50       1E6
r13  16  17       1E6
r14  16  18       1E6
c5   17  99       19.89E-15
c6   18  50       19.89E-15
g5   99  16       13 32 1E-6
g6   16  50       32 13 1E-6
*
* ZERO-POLE PAIR AT 85MHz / 300MHz
*
r17  19  20       1E6
r18  19  21       1E6
r19  20  99       2.529E6
r20  21  50       2.529E6
l3   20  99       1.342E-3
l4   21  50       1.342E-3
g7   99  19       16 32 1E-6
g8   19  50       32 16 1E-6
*
* POLE AT 40MHz
*
r21  22  99       1E6
r22  22  50       1E6
c7   22  99       3.979E-15
c8   22  50       3.979E-15
g9   99  22       19 32 1E-6
g10  22  50       32 19 1E-6
*
* POLE AT 200MHz
*
r23  23  99       1E6
r24  23  50       1E6
c9   23  99       .796E-15
c10  23  50       .796E-15
g11  99  23       22 32 1E-6
g12  23  50       32 22 1E-6
*
* POLE AT 200MHz
*
r25  24  99       1E6
26   24  50       1E6
c11  24  99       .796E-15
c12  24  50       .796E-15
g13  99  24       23 32 1E-6
g14  24  50       32 23 1E-6
*
* POLE AT 200MHz
*
r27  25  99       1E6
r28  25  50       1E6
c13  25  99       .796E-15
c14  25  50       .796E-15
g15  99  25       24 32  1E-6
g16  25  50       32 24 1E-6
*
* COMMON-MODE GAIN NETWORK WITH ZERO AT 40kHz
*
r29  26  27       1E6
r30  26  28       1E6
l5   27  99       3.979
l6   28  50       3.979
g17  99  26       3  32 1E-6
g18  26  50       32 3  1E-6
v4   99  29       2.5
v5   30  50       2.5
d3   26  29       dx
d4   30  26       dx
*
* POLE AT 300MHz
*
r32  31  99       1E6
r33  31  50       1E6
c15  31  99       .531E-15
c16  31  50       .531E-15
g19  99  31       25 32 1E-6
g20  31  50       32 25 1E-6
*
* OUTPUT STAGE
*
r34  32  99       20.0E3
r35  32  50       20.0E3
r36  33  99       30
r37  33  50       30
l7   33  38       1.65E-7
g21  36  50       31 33 33.3333333E-3
g22  37  50       33 31 33.3333333E-3
g23  33  99       99 31 33.3333333E-3
g24  50  33       31 50 33.3333333E-3
v6   34  33       .2
v7   33  35       .2
d5   31  34       dx
d6   35  31       dx
d7   99  36       dx
d8   99  37       dx
d9   50  36       dy
d10  50  37       dy
*
* MODELS USED
*
.model qx NPN(BF=1250)
.model dx  D(IS=1E-15)
.model dy  D(IS=1E-15 BV = 50)
.ends OP-61
```

FIGURE 19: *OP-61 SPICE Net List*

* PSpice is a registered trademark of MicroSim Corporation.
** HSPICE is a tradename of Meta-Software, Inc.

High-Speed, Wide Bandwidth Operational Amplifier ($A_{VCL} \geq 5$)

OP-64

FEATURES

- High Slew Rate ..... 130V/µs Min
- Fast Settling Time (+10V, 0.1%) ..... 100ns Typ
- Gain-Bandwidth Product (A_{VCL} = +5) ..... 80MHz Typ
- Low Supply Current ..... 8mA Max
- Low Noise ..... 8nV/√Hz Typ
- Low Offset Voltage ..... 1mV Max
- High Output Current ..... ±80mA Typ
- Eliminates External Buffer
- Standard 8-Pin Packages
- Available in Die Form

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (mV)	PACKAGE TO-99 8-PIN	HERMETIC DIP 8-PIN	PLASTIC 8-PIN	HERMETIC LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
1.0	OP64AJ*	OP64AZ*	–	OP64ARC/883	MIL
1.0	OP64EJ	OP64EZ	–	–	XIND
2.0	OP64FJ	OP64FZ	–	–	XIND
2.5	–	–	OP64GP	–	XIND
2.5	–	–	OP64GS††	–	XIND

XIND = Extended Industrial Temperature Range, –40°C to +85°C

* For devices processed in total compliance to MIL-SDT-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-99 can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

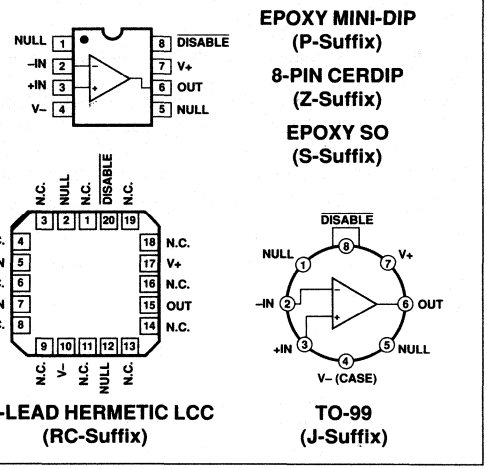
GENERAL DESCRIPTION

The OP-64 is a high-performance monolithic operational amplifier that combines high speed and wide bandwidth with low power consumption. Advanced processing techniques have en-

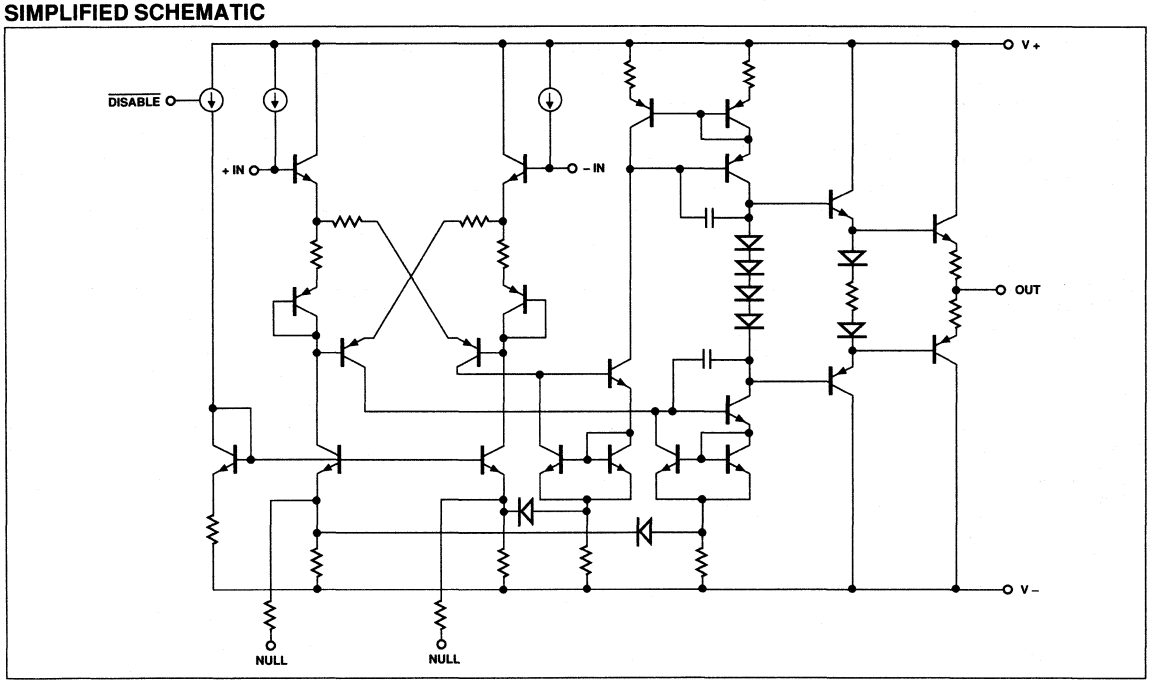
Continued

2

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



GENERAL DESCRIPTION *Continued*

enabled PMI to make the OP-64 superior in cost and performance to many dielectrically-isolated and hybrid op amps.

Slew rate of the OP-64 is over 130V/µs. It is stable in gains of ≥5 and has a settling time of only 100ns to 0.1% with a 10V step input. However, unlike other high-speed op amps which have high supply requirements, the OP-64 needs less than 8mA of supply current. This enables the OP-64 to be packaged in space saving 8-pin packages. The OP-64 can deliver ±80mA of output current eliminating the need for a separate buffer amplifier in many applications. Noise of the OP-64 is only $8nV\sqrt{Hz}$, reducing system noise in wideband applications. In addition to its dynamic performance, the OP-64 adds DC precision with an input offset voltage of under 1mV.

The OP-64 is an ideal choice for RF, video and pulse amplifier applications and in new designs can replace the HA-5190/95 or EL-2190/95 with improved performance and reduced power consumption. Its high output current also suits the OP-64 for use in A/D or cable driver applications. The OP-64 includes a $\overline{\text{DISABLE}}$ pin which, when set low, shuts the amplifier off and reduces the supply current to 0.75mA.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Input Voltage ..... Supply Voltage
Differential Input Voltage 20V
$\overline{\text{DISABLE}}$ Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... 10 sec
Storage Temperature Range
(J, Z, RC) ..... –65°C to +175°C
(P, S) ..... –65°C to +150°C
Operating Temperature Range
OP-64A (J, Z, RC) ..... –55°C to +125°C
OP-64E, F (J, Z) ..... –40°C to +85°C
OP-64G (P, S) ..... –40°C to +85°C
Maximum Junction Temperature
OP-64A (J ,Z, RC) ..... +175°C
OP-64E, F (J, Z) ..... +175°C
OP-64G (P, S) ..... +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC (RC, TC)	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-64A/E MIN	OP-64A/E TYP	OP-64A/E MAX	OP-64F MIN	OP-64F TYP	OP-64F MAX	OP-64G MIN	OP-64G TYP	OP-64G MAX	UNITS
Offset Voltage	V_{OS}		–	0.4	1	–	0.8	2	–	1.2	2.5	mV
Input Bias Current	I_B	V_{CM} = 0V	–	0.2	1	–	0.4	2	–	0.8	2.5	µA
Input Offset Current	I_{OS}	V_{CM} = 0V	–	0.1	1	–	0.3	2	–	0.6	2.5	µA
Input Voltage Range	IVR	(Note 1)	±11	–	–	±11	–	–	±11	–	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	90	100	–	84	94	–	84	94	–	dB
Power-Supply Rejection Ratio	PSRR	V_S = ±5V to ±18V	–	5	17.8	–	15	31.6	–	15	31.6	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L = 2kΩ, V_O = ±10V R_L = 200Ω, V_O = ±5V	30 12.5	45 18	– –	20 10	35 16	– –	20 10	35 16	– –	V/mV
Output Voltage Swing	V_O	R_L = 2kΩ R_L = 200Ω	±11 ±10	±12.5 ±11.7	– –	±11 ±10	±12.5 ±11.7	– –	±11 ±10	±12.5 ±11.7	– –	V
Output Current	I_{OUT}		–	±80	–	–	±80	–	–	±80	–	mA
Supply Current	I_{SY}	No Load	–	6.2	8	–	6.2	8	–	6.2	8	mA

NOTE:
1. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-64A/E MIN	OP-64A/E TYP	OP-64A/E MAX	OP-64F MIN	OP-64F TYP	OP-64F MAX	OP-64G MIN	OP-64G TYP	OP-64G MAX	UNITS
Disable Supply Current	$I_{SY\ \overline{DIS}}$	$\overline{DISABLE}$ = 0V Total for both supplies	–	0.75	1	–	0.75	1	–	0.75	1	mA
$\overline{DISABLE}$ Current	$I_{\overline{DIS}}$	$\overline{DISABLE}$ = 0V	–	0.5	–	–	0.5	–	–	0.5	–	mA
Slew Rate	SR	R_L = 2kΩ	130	170	–	130	170	–	130	170	–	V/µs
Full-Power Bandwidth	BW_p	(Note 2)	2	2.7	–	2	2.7	–	2	2.7	–	MHz
Gain-Bandwidth Product	GBWP	A_V = +5	–	80	–	–	80	–	–	80	–	MHz
Settling Time	t_s	10V Step 0.1%	–	100	–	–	100	–	–	100	–	ns
Phase Margin	$ø_m$	A_V = +5	–	57	–	–	57	–	–	57	–	degrees
Input Capacitance	C_{IN}		–	5	–	–	5	–	–	5	–	pF
Open-Loop Output Resistance	R_O		–	30	–	–	30	–	–	30	–	Ω
Voltage Noise Density	e_n	f_o = 10Hz	–	30	–	–	30	–	–	30	–	nV/√Hz
		f_o = 100Hz	–	10	–	–	10	–	–	10	–	
		f_o = 1kHz	–	8	–	–	8	–	–	8	–	
		f_o = 10kHz	–	8	–	–	8	–	–	8	–	
Current Noise Density	i_n	f_o = 10kHz	–	7.5	–	–	7.5	–	–	7.5	–	pA/√Hz
External V_{OS} Trim Range	R_{pot} = 20kΩ		–	4	–	–	4	–	–	4	–	mV
Supply Voltage Range	V_S		±5	±15	±18	±5	±15	±18	±5	±15	±18	V

NOTES:
1. Guaranteed by CMR test.
2. Guaranteed by slew-rate test and formula $BW_p = SR/(2\pi 10V_{PEAK})$.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, –40°C ≤ T_A ≤ +85°C for OP-64E/F/G, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-64E MIN	OP-64E TYP	OP-64E MAX	OP-64F MIN	OP-64F TYP	OP-64F MAX	OP-64G MIN	OP-64G TYP	OP-64G MAX	UNITS
Offset Voltage	V_{OS}		–	0.5	1.5	–	1.0	3	–	1.5	3.5	mV
Input Bias Current	I_B	V_{CM} = 0V	–	0.3	2.5	–	0.5	3	–	1.5	3.5	µA
Input Offset Current	I_{OS}	V_{CM} = 0V	–	0.2	2.5	–	0.5	3	–	1.0	3.5	µA
Input Voltage Range	IVR	(Note 1)	±11	–	–	±11	–	–	±11	–	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11	86	100	–	80	94	–	80	94	–	dB
Power-Supply Rejection Ratio	PSRR	V_S = ±5V to ±18V	–	5	31.6	–	15	50	–	15	50	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L = 2kΩ, V_O = ±10V R_L = 200Ω, V_O = ±5V	20 7.5	40 12	– –	15 5	35 10	– –	15 5	35 10	– –	V/mV
Output Voltage Swing	V_O	R_L = 2kΩ R_L = 200Ω	±11 ±10	±12.3 ±11.5	– –	±11 ±10	±12.3 ±11.5	– –	±11 ±10	±12.3 ±11.5	– –	V
Supply Current	I_{SY}	No Load	–	6.3	8.5	–	6.3	8.5	–	6.3	8.5	mA

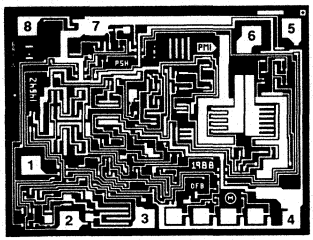
NOTE:
1. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, –55°C ≤ T_A ≤ +125°C for OP-64A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-64A MIN	OP-64A TYP	OP-64A MAX	UNITS
Offset Voltage	V_{OS}		–	0.4	2	mV
Input Bias Current	I_B	V_{CM} = 0V	–	0.35	2	µA
Input Offset Current	I_{OS}	V_{CM} = 0V	–	0.3	2	µA
Input Voltage Range	IVR	(Note 1)	±11	–	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11	86	100	–	dB
Power-Supply Rejection Ratio	PSRR	V_S = ±5V to ±18V	–	8	31.6	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L = 2kΩ, V_O = ±10V R_L = 200Ω, V_O = ±5V	20 7.5	30 10	– –	V/mV
Output Voltage Swing	V_O	R_L = 2kΩ R_L = 200Ω	±11 ±7.5	±12 ±10	– –	V
Supply Current	I_{SY}	No Load	–	6.4	8.5	mA

NOTE:
1. Guaranteed by CMR test.

DICE CHARACTERISTICS



DIE SIZE 0.086 x 0.065 inch, 5,590 sq. mils
(2.18 x 1.65 mm, 3.60 sq. mm)

1. NULL
2. –IN
3. +IN
4. V–
5. NULL
6. OUT
7. V+
8. DISABLE

2

WAFER TEST LIMITS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

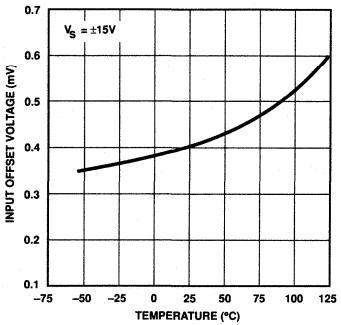
PARAMETER	SYMBOL	CONDITIONS	OP-64GBC LIMITS	UNITS
Offset Voltage	V_{OS}		2.5	mV MAX
Input Bias Current	I_B	V_{CM} = 0V	2.5	µA MAX
Input Offset Current	I_{OS}	V_{CM} = 0V	2.5	µA MAX
Input Voltage Range	IVR	(Note 1)	±11	V MIN
Common-Mode Rejection	CMR	V_{CM} = ±11V	84	dB MIN
Power Supply Rejection Ratio	PSRR	V_S = ±5V to ±18V	31.6	µV/V MAX
Large-Signal Voltage Gain	A_{VO}	R_L = 2kΩ, V_O = ±10V R_L = 200Ω, V_O = ±5V	20 10	V/mV MIN
Output Voltage Swing	V_O	R_L = 2kΩ R_L = 200Ω	±11 ±10	V MIN
Slew Rate SR	R_L = 2kΩ		120	V/µs MIN
Supply Current	I_{SY}	No Load	8	mA MAX

NOTES:
1. Guaranteed by CMR test.

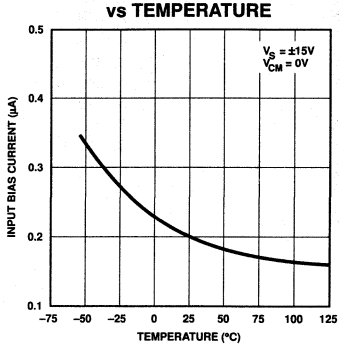
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

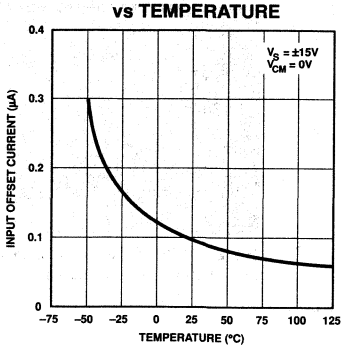
INPUT OFFSET VOLTAGE vs TEMPERATURE



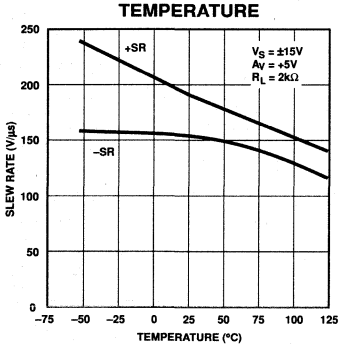
INPUT BIAS CURRENT vs TEMPERATURE



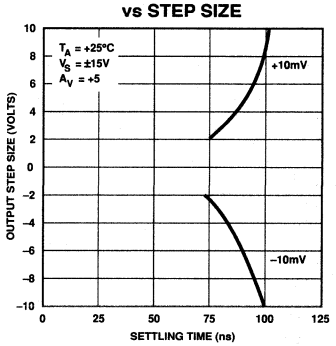
INPUT OFFSET CURRENT vs TEMPERATURE



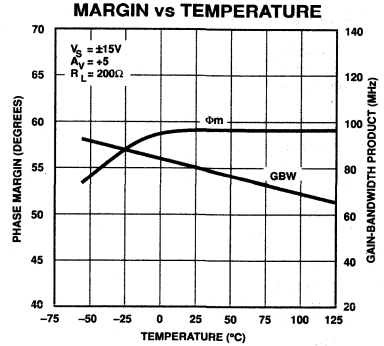
SLEW RATE vs TEMPERATURE



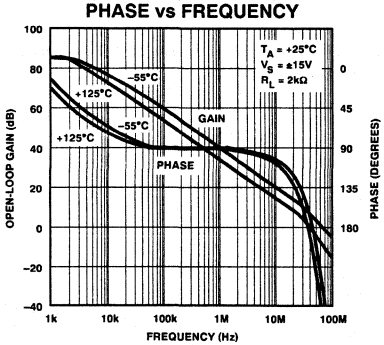
SETTLING TIME vs STEP SIZE



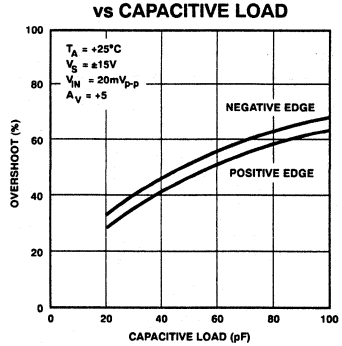
GAIN-BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE



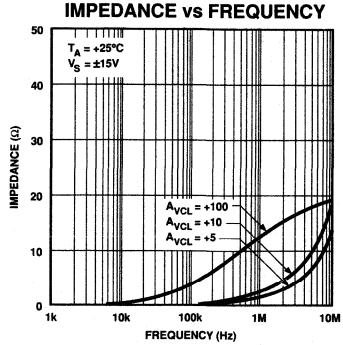
OPEN-LOOP GAIN, PHASE vs FREQUENCY



SMALL SIGNAL OVERSHOOT vs CAPACITIVE LOAD

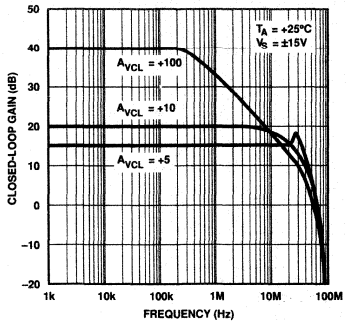


CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

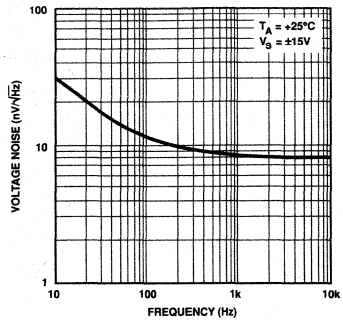


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

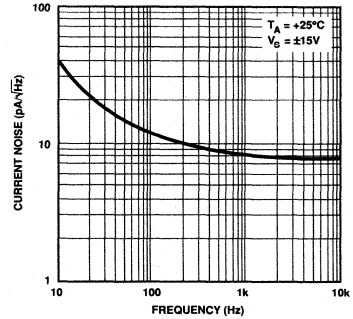
CLOSED-LOOP GAIN vs FREQUENCY



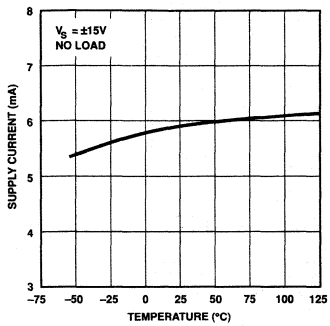
VOLTAGE NOISE DENSITY vs FREQUENCY



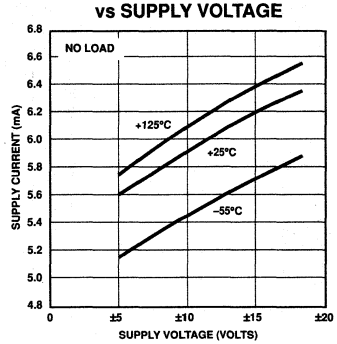
CURRENT NOISE DENSITY vs FREQUENCY



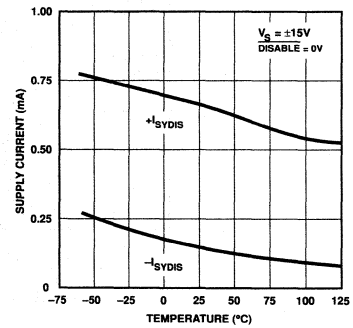
SUPPLY CURRENT vs TEMPERATURE



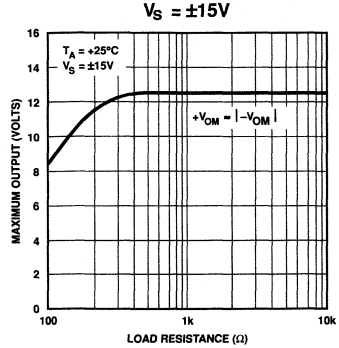
SUPPLY CURRENT vs SUPPLY VOLTAGE



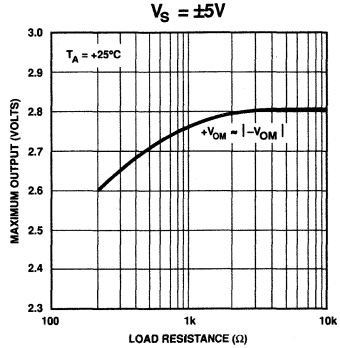
I_{SY} $\overline{\text{DISABLE}}$ vs TEMPERATURE



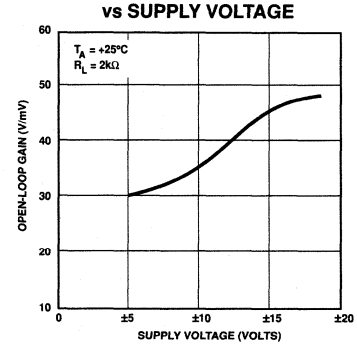
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE V_S = ±15V



MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE V_S = ±5V

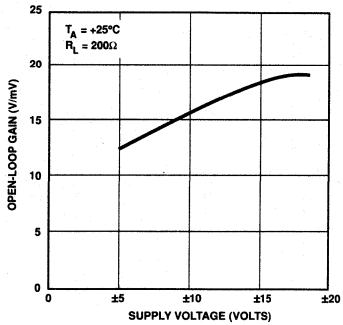


OPEN-LOOP GAIN vs SUPPLY VOLTAGE

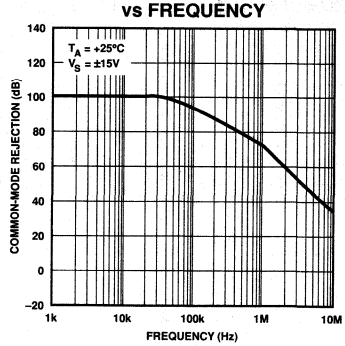


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

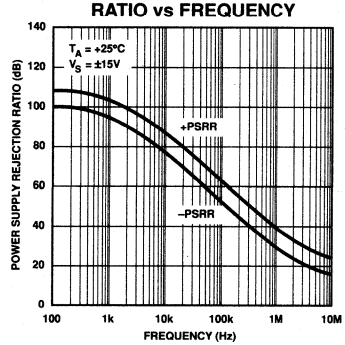
OPEN-LOOP GAIN vs SUPPLY VOLTAGE



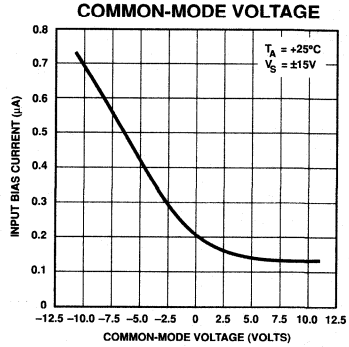
COMMON-MODE REJECTION vs FREQUENCY



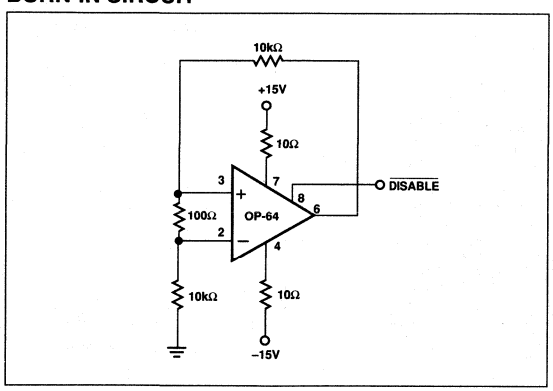
POWER SUPPLY REJECTION RATIO vs FREQUENCY



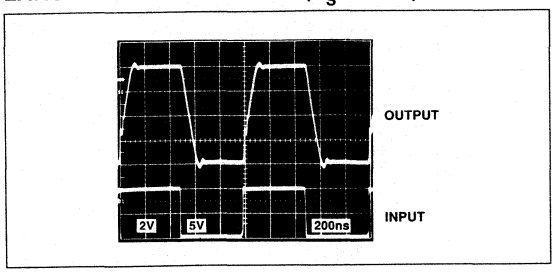
INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE



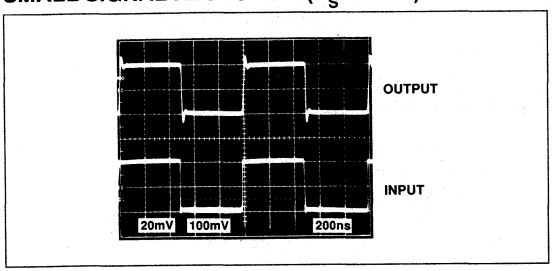
BURN-IN CIRCUIT



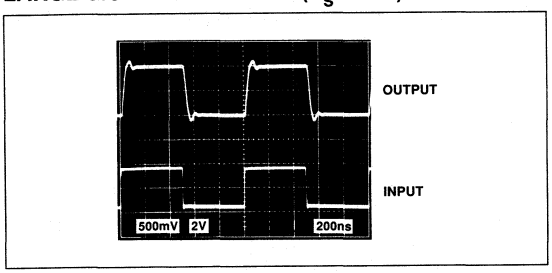
LARGE SIGNAL RESPONSE (V_S = ±15V)



SMALL SIGNAL RESPONSE (V_S = ±15V)



LARGE SIGNAL RESPONSE (V_S = ±5V)



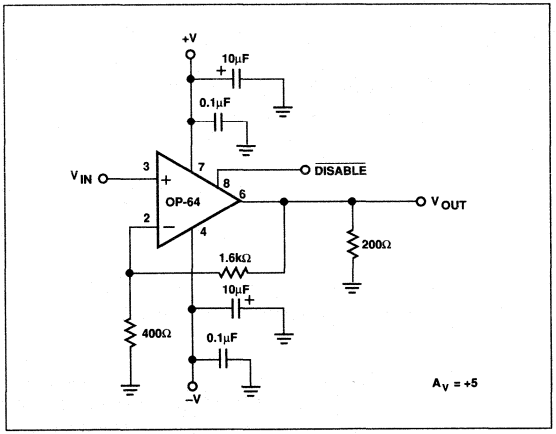
APPLICATIONS INFORMATION

POWER SUPPLY BYPASSING AND LAYOUT CONSIDERATIONS

Proper power supply bypassing is critical in all high-frequency circuit applications. For stable operation of the OP-64, the power supplies must maintain a low impedance-to-ground over an extremely wide bandwidth. This is most critical when driving a low resistance or large capacitance, since the current required to drive the load comes from the power supplies. A 10µF and 0.1µF ceramic bypass capacitor are recommended for each supply, as shown in Figure 1, and will provide adequate high-frequency bypassing in most applications. The bypass capacitors should be placed at the supply pins of the OP-64. As with all high frequency amplifiers, circuit layout is a critical factor in obtaining optimum performance from the OP-64. Proper high frequency layout reduces unwanted signal coupling in the circuit. When breadboarding a high frequency circuit, use direct point-to-point wiring, keeping all lead lengths as short as possible. Do not use wire-wrap boards or "plug-in" prototyping boards.

During PC board layout, keep all lead lengths and traces as short as possible to minimize inductance. The feedback and gain-setting resistors should be as close as possible to the inverting input to reduce stray capacitance at that point. To further reduce stray capacitance, remove the ground plane from the area around the inputs of the OP-64. Elsewhere, the use of a solid unbroken ground plane will insure a good high-frequency ground.

LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT



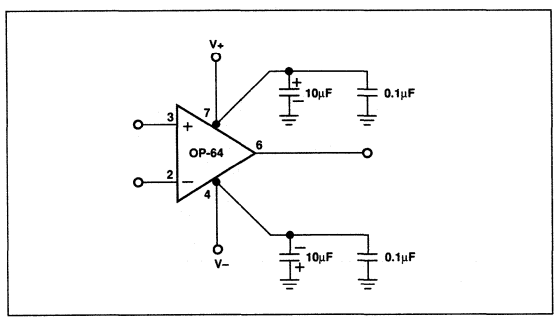


FIGURE 1: *Proper power supply bypassing is required to obtain optimum performance with the OP-64.*

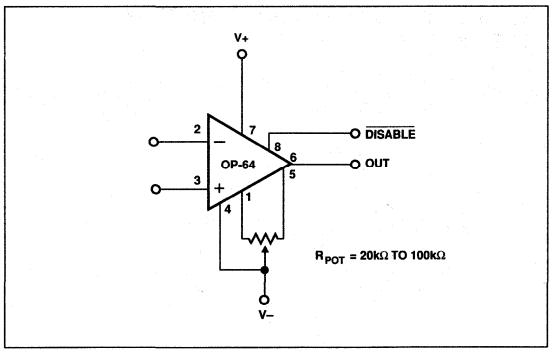


FIGURE 2: *Input Offset Voltage Nulling*

OFFSET VOLTAGE ADJUSTMENT

Offset voltage is adjusted with a 20kΩ potentiometer as shown in Figure 2. The potentiometer should be connected between pins 1 and 5 with its wiper connected to the V– supply. The typical trim range is ±4mV.

OP-64 $\overline{\text{DISABLE}}$ AMPLIFIER SHUTDOWN

Pin 8 of the OP-64, $\overline{\text{DISABLE}}$, is an amplifier shutdown control input. The OP-64 operates normally when Pin 8 is left floating. When greater than 250µA is drawn from the $\overline{\text{DISABLE}}$ pin, the OP-64 is disabled. The supply current drops to 1mA and the output impedance rises to 2kΩ. To draw current from the $\overline{\text{DISABLE}}$ pin, an open collector output logic gate or a discrete NPN transistor can be used as shown in Figure 3. An internal resistor

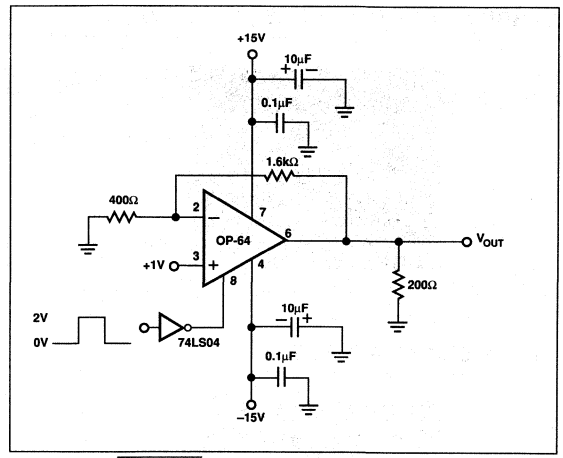


FIGURE 4: *$\overline{\text{DISABLE}}$ Turn-On/Turn-Off Test Circuit*

limits the $\overline{\text{DISABLE}}$ current to around 500µA if the $\overline{\text{DISABLE}}$ pin is grounded with the OP-64 powered by ±15V supplies. These logic interface methods have the added advantage of level shifting the TTL signal to whatever supply voltage is used to power the OP-64.

Figure 4 shows a test circuit for measuring the turn-on and turn-off times for the OP-64. The OP-64 is in a gain of 5 with a +1V DC input. As the input pulse to the 74LS04 rises its output falls,

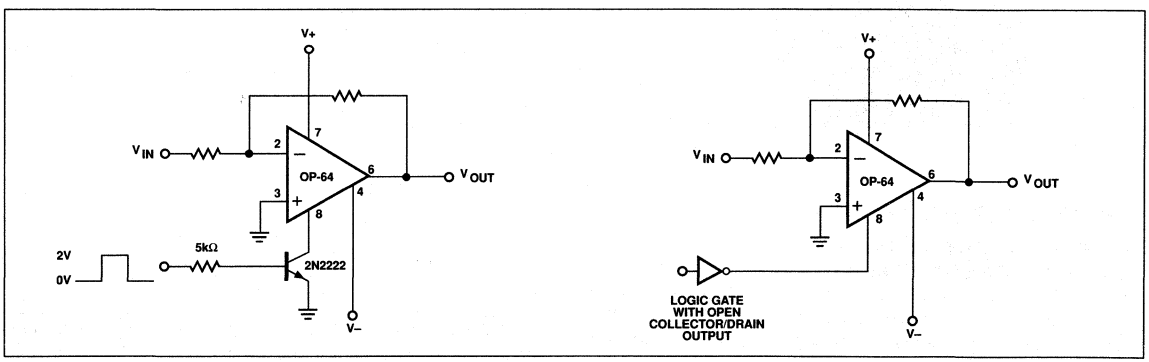


FIGURE 3: *Simple circuits allow the OP-64 to be shut down.*

drawing current from the $\overline{\text{DISABLE}}$ pin and disabling the amplifier. The output voltage delay is shown in Figure 5 and takes 500µs to reach ground due to the extra current supplied to the amplifier by the 10µF electrolytic bypass capacitors. The turn-on time is much quicker than the turn-off time. In this situation as the input to the 74LS04 falls its output rises, returning the OP-64 to normal operation. The amplifier's output turns on in 250ns.

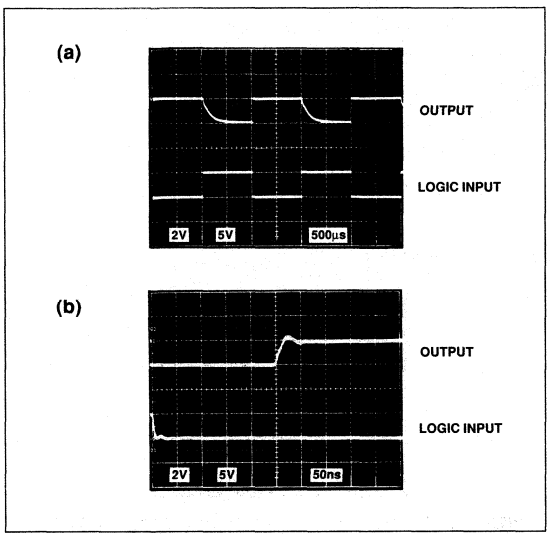


FIGURE 5: *(a) OP-64 turn-on and turn-off performance. (b) Expanded scale showing turn-on performance of the OP-64.*

OVERDRIVE RECOVERY

Figure 6 shows the overdrive recovery performance of the OP-64. Typical recovery time is 270ns from negative overdrive and 80ns from positive overdrive.

VIDEO AMPLIFIER/TERMINATED LINE DRIVER

The OP-64 can be used as a video amplifier/terminated line driver as shown in Figure 8. With its high output current capability, the OP-64 eliminates the need for an external buffer.

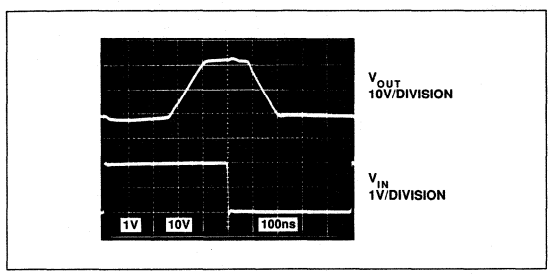


FIGURE 6: *OP-64 Overdrive Recovery*

The 75Ω cable termination resistor minimizes reflections from the end of the cable. The 75Ω series output resistor absorbs any reflections caused by a mismatch between the 75Ω termination resistor and the characteristic cable impedance. In this circuit the output voltage, V_{OUT}, is one-half of the OP-64's output voltage due to the divider formed by the 75Ω terminating resistors. The output voltage at the end of the terminated cable, V_{OUT}, spans –1V to +1V. The differential gain and phase for the video amplifier is summarized in Table1.

TABLE 1: Differential Gain and Phase of Video Amplifier/Line Driver

	Differential Gain		Differential Phase	
V_S	3.58MHz	5MHz	3.58MHz	5MHz
±15V	0.008dB	0.016dB	0.03°	0.03°
±12V	0.008dB	0.018dB	0.03°	0.03°

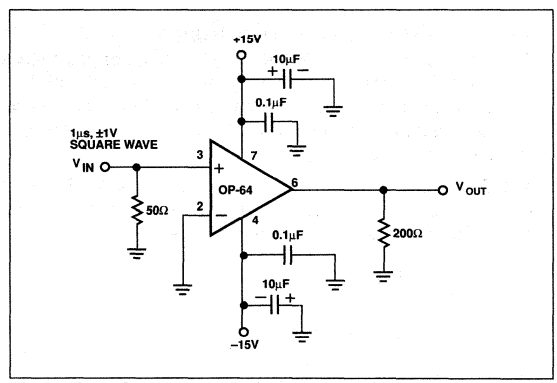


FIGURE 7: *Overdrive Recovery Test Circuit*

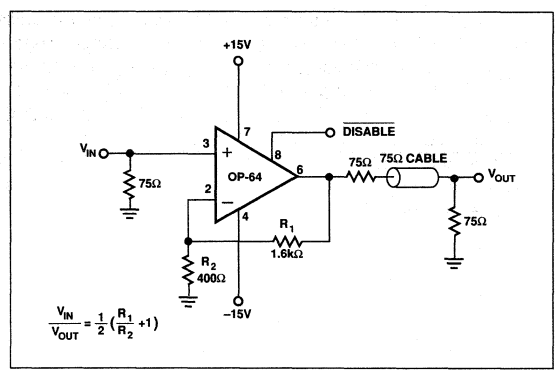


FIGURE 8: *Video Amplifier/Terminated Line Driver*

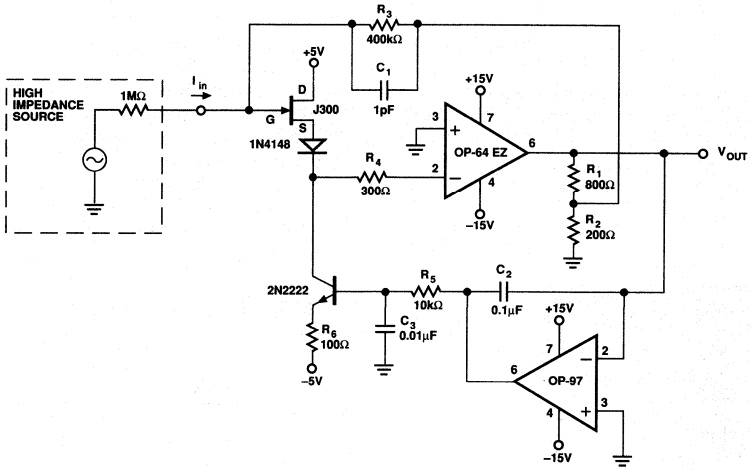


FIGURE 9: *Fast Transimpedance Amplifier*

FAST TRANSIMPEDANCE AMPLIFIER

The circuit shown in Figure 9 is a fast transimpedance amplifier designed to handle high speed signals from a high impedance source such as the output of a photomultiplier tube. The input current is amplified and converted to an output voltage by the transimpedance amplifier.

A JFET source-follower input is used to reduce the input bias current of the amplifier to 100 pA and lower the input current noise. Transimpedance of the amplifier is:

$$\frac{V_{OUT}}{I_{IN}} = \left(\frac{R_1}{R_2} + 1\right) R_3$$

and for the values shown equals

$$\frac{V_{OUT}}{I_{IN}} = \left(\frac{800\Omega}{200\Omega} + 1\right) 400k\Omega = 2V/\mu A$$

Figure 10 shows the output of the transimpedance amplifier when driven from a 1MΩ source impedance. The input signal of $10\mu A_{p\text{-}p}$ is converted into an output voltage of (10μA) 2V/μA = $20V_{p\text{-}p}$. Output slew rate is 100V/μs. The slew rate is limited by the combination of the capacitance of the JFET gate with the 1MΩ source impedance. For best performance, the stray input capacitance should be kept as small as possible. The OP-97 is used in an integrator loop to reduce the total amplifier offset voltage to under 25μV.

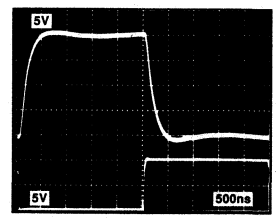


FIGURE 10: *Output of the Fast Transimpedance Amplifier*

OP-64 SPICE MACRO-MODEL

Figure 11 shows the node and net list for a SPICE macro-model of the OP-64. The model is a simplified version of the actual device and simulates important DC parameters such as V_{OS}, I_{OS}, I_B, A_{VO}, CMR, V_O and I_{SY}. AC parameters such as slew rate, gain and phase response and CMR change with frequency are also simulated by the model.

The model uses typical parameters for the OP-64. The poles and zeros in the model were determined from the actual open and closed-loop gain and phase response of the OP-64. In this way the model presents an accurate AC representation of the actual device. The model assumes an ambient temperature of 25°C (see following pages).

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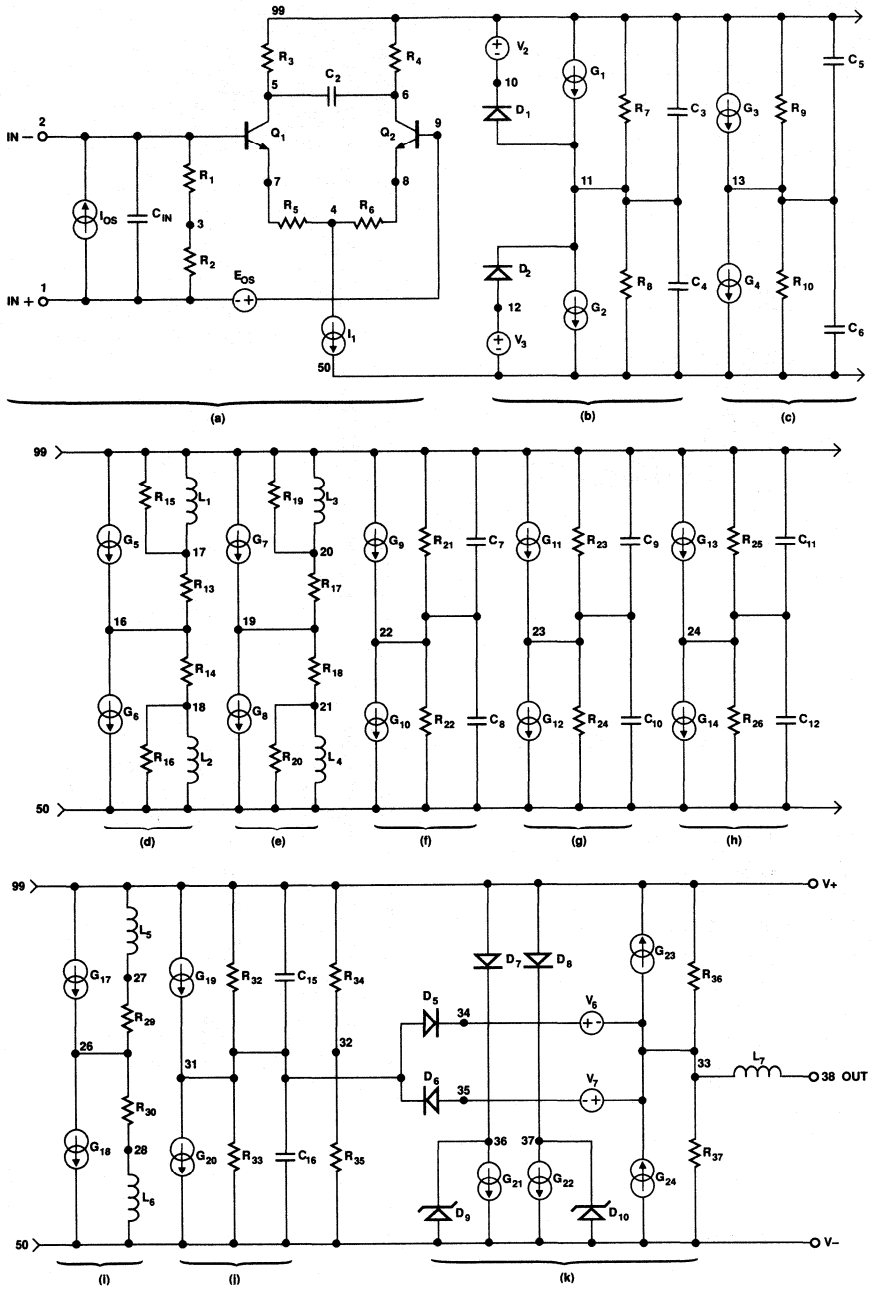


FIGURE 11a: *OP-64 SPICE Macro-Model Schematic and Node List*

* PSpice is a registered trademark of MicroSim Corporation.
** HSPICE is a tradename of Meta-Software, Inc.

```
OP-64 MACRO-MODEL © PMI 1989
*
* subckt OP-64 1  2 38  99  50
*
INPUT STAGE & POLE AT 39.8 MHz
*
r1   2   3        5E11
r2   1   3        5E11
r3   5   99       474.86
r4   6   99       474.86
r5   4   7        423.26
r6   4   8        423.26
cin  1   2        5E-12
c2   5   6        4.2106E-12
i1   4   50       1E-3
ios  1   2        1E-7
eos  9   1        poly(1) 26 32 4E-4 1
q1   5   2   7    qx
q2   6   9   8    qx
*
* SECOND STAGE & POLE AT 3.8 kHz
*
r7   11  99       7.1229E6
r8   11  50       7.1229E6
c3   11  99       5.88E-12
c4   11  50       5.88E-12
g1   99  11       poly(1) 5 6 4.31E-3 2.1059E-3
g2   11  50       poly(1) 6 5 4.31E-3 2.1059E-3
v2   99  10       2.25
v3   12  50       2.25
d1   11  10       dx
d2   12  11       dx
*
* POLE AT 39.8 MHz
*
r9   13  99       1E6
r10  13  50       1E6
c5   13  99       4E-15
c6   13  50       4E-15
g3   99  13       11 32 1E-6
g4   13  50       32 11 1E-6
*
* ZERO-POLE PAIR AT 26.5 MHz /159 MHz
*
r13  16  17       1E6
r14  16  18       1E6
r15  17  99       5E6
r16  18  50       5E6
l1   17  99       5.005E-3
l2   18  50       5.005E-3
g5   99  16       13 32 1E-6
g6   16  50       32 13 1E-6
*
* ZERO-POLE PAIR AT 31.8 MHz / 39.8 MHz
*
r17  19  20       1E6
r18  19  21       1E6
r19  20  99       2.5157E5
r20  21  50       2.5157E5
l3   20  99       1.006E-3
l4   21  50       1.006E-3
g7   99  19       16 32 1E-6
g8   19  50       32 16 1E-6
*
* POLE AT 100 MHz
*
r21  22  99       1E6
r22  22  50       1E6
c7   22  99       1.59E-15
c8   22  50       1.59E-15
g9   99  22       19 32 1E-6
g10  22  50       32 19 1E-6
*
*POLE AT 159 MHz
*
r23  23  99       1E6
r24  23  50       1E6
c9   23  99       1E-15
c10  23  50       1E-15
g11  99  23       22 32 1E-6
g12  23  50       32 22 1E-6
*
*POLE AT 159 MHz
*
r25  24  99       1E6
r26  24  50       1E6
c11  24  99       1E-15
c12  24  50       1E-15
g13  99  24       23 32 1E-6
g14  24  50       32 23 1E-6
*
*COMMON-MODE GAIN NETWORK WITH ZERO AT 20kHz
*
r29  26  27       1E6
r30  26  28       1E6
l5   27  99       7.9575
l6   28  50       7.9575
g17  99  26       33 32 1E-11
g18  26  50       32 33 1E-11
*
* POLE AT 159 MHz
*
r32  31  99       1E6
r33  31  50       1E6
c15  31  99       1E-15
c16  31  50       1E-15
g19  99  31       24 32 1E-6
g20  31  50       32 24 1E-6
*
* OUTPUT STAGE
*
r34  32  99       20.0E3
r35  32  50       20.0E3
r36  33  99       60
r37  33  50       60
l7   33  38       2.9E-7
g21  36  50       31  33  16.6666667E-3
g22  37  50       33  31  16.6666667E-3
g23  33  99       99  31  16.6666667E-3
g24  50  33       31  50  16.6666667E-3
v6   34  33       1.7
v7   33  35       1.7
d5   31  34       dx
d6   35  31       dx
d7   99  36       dx
d8   99  37       dx
d9   50  36       dy
d10  50  37       dy
*
* MODELS USED
*
.model qx NPN(BF=2500)
.model dx    D(IS=1E-15)
.model dy    D(IS=1E-15 BV=50)
.ends OP-64
```

FIGURE 11b: *OP-64 SPICE Net-List*

ANALOG DEVICES

Next Generation OP-07, Ultra-Low Offset Voltage Operational Amplifier

OP-77

FEATURES

- **Outstanding Gain Linearity**
- **Ultra High Gain ..... 5000V/mV Min**
- **Low V_{OS} Over Temperature ..... 60μV Max**
- **Excellent TCV_{OS} ..... 0.3μV/°C Max**
- **High PSRR ..... 3μV/V Max**
- **Low Power Consumption ..... 60mW Max**
- **Fits OP-07, 725, 108A/308A, 741 Sockets**
- **Available in Die Form**

ORDERING INFORMATION †

PACKAGE				OPERATING TEMPERATURE RANGE
TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	LCC 20-PIN	
OP77AJ*	OP77AZ*	–	–	MIL
OP77EJ	OP77EZ	–	–	IND
–	–	OP77EP	–	COM
OP77BJ*	OP77BZ*	–	OP77BRC/883	MIL
OP77FJ	OP77FZ	–	–	IND
–	–	OP77FP	–	COM
–	–	OP77GP	–	COM
–	–	OP77GS††	–	COM
–	–	OP77HP	–	XIND
–	–	OP77HS††	–	XIND

* For devices processed in total compliance to MIL-SDT-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

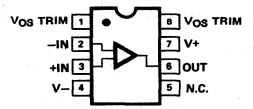
GENERAL DESCRIPTION

The OP-77 significantly advances the state-of-the-art in precision op amps. The OP-77's outstanding gain of 10,000,000 or more is maintained over the full ±10V output range. This exceptional gain-linearity eliminates incorrectable system nonlinearities common in previous monolithic op amps, and provides superior performance in high closed-loop-gain applications. Low initial V_{OS} drift and rapid stabilization time, combined with only 50mW power consumption, are significant improvements over previous designs. These characteristics, plus the exceptional TCV_{OS} of 0.3μV/°C maximum and the low V_{OS} of 25μV maximum, eliminates the need for V_{OS} adjustment and increases system accuracy over temperature.

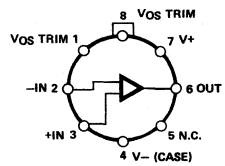
PSRR of 3μV/V (110dB) and CMRR of 1.0μV/V maximum virtually eliminiate errors caused by power supply drifts and common-mode signals. This combination of outstanding characteristics makes the OP-77 ideally suited for high-resolution instrumentation and other tight error budget systems.

Continued

PIN CONNECTIONS

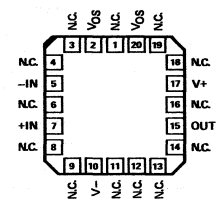


EPOXY MINI-DIP (P-Suffix)
8-PIN HERMETIC DIP (Z-Suffix)



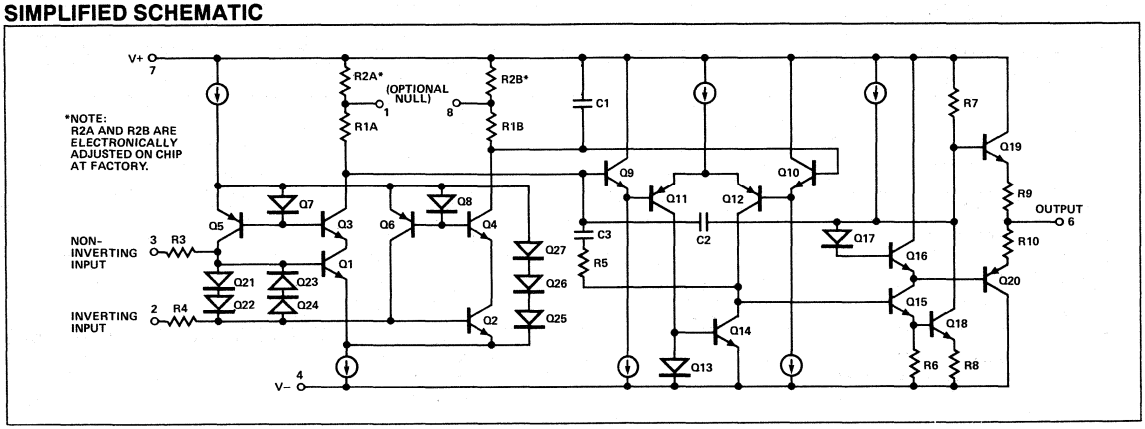
TO-99 (J-Suffix)

8-PIN SO (S-Suffix)



OP-77BRC/883 LCC (RC-Suffix)

SIMPLIFIED SCHEMATIC



OP-77

This product is available in six standard grades and five standard packages: the TO-99 can, the 8-pin mini-DIP in ceramic, SO or epoxy, and the 20-contact LCC.

The OP-77 is a direct or upgrade replacement for the OP-07, 05, 725, or 108A op amps. 741-types can be replaced by eliminating the V_{OS} adjust pot. For higher precision performance refer to OP-177.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage ..... ±22V
Differential Input Voltage ..... ±30V
Input Voltage (Note 1) ..... ±22V
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range
J, Z, and RC Packages ..... –65°C to +150°C
P Package ..... –65°C to +125°C
Operating Temperature Range
OP-77A, OP-77B (J, Z, RC) ..... –55°C to +125°C
OP-77E, OPP-77F (J, Z) ..... –25°C to +85°C
OP-77E, OP-77F, OP-77G (P, S) ..... 0°C to 70°
OP-77H (P, S) ..... –40°C to +85°C
Junction Temperature (T_j) ..... –65°C to +150C
Lead Temperature (Soldering, 60 sec.) ..... +300°C

PACKAGE TYPE	Θ_{jA} (Note 3)	Θ_{jC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC (RC, TC)	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
2. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
3. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{jA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

			OP-77A			OP-77B			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		–	10	25	–	20	60	µV
Long-Term Input Offset Voltage Stability	ΔV_{OS}/Time	(Note 1)	–	0.2	–	–	0.2	–	µV/Mo
Input Offset Current	I_{OS}		–	0.3	1.5	–	0.3	2.8	nA
Input Bias Current	I_B		–0.2	1.2	2.0	–0.2	1.2	2.8	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 2)	–	0.35	0.6	–	0.35	0.6	µVp-p
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 2) f_O = 100Hz (Note 2) f_O = 1000Hz (Note 2)	– – –	10.3 10.0 9.6	18.0 13.0 11.0	– – –	10.3 10.0 9.6	18.0 13.0 11.0	V/√Hz
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 2)	–	14	30	–	14	30	pAp-p
Input Noise Current Density	i_n	f_O = 10Hz (Note 2) f_O = 100Hz (Note 2) f_O = 1000Hz (Note 2)	– – –	0.32 0.14 0.12	0.80 0.23 0.17	– – –	0.32 0.14 0.12	0.80 0.23 0.17	pA/√Hz
Input Resistance – Differential-Mode	R_{IN}	(Note 3)	26	45	–	18.5	45	–	MΩ
Input Resistance – Common-Mode	R_{INCM}		–	200	–	–	200	–	GΩ
Input Voltage Range	IVR		±13	±14	–	±13	±14	–	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V	–	0.1	1.0	–	0.1	1.0	µV/V
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	–	0.7	3	–	0.7	3	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ, VO = ±10V	5000	12000	–	2000	8000	–	V/mV
Output Voltage Swing	V_O	R_L ≥ 10kΩ R_L ≥ 2kΩ R_L ≥ 1kΩ	±13.5 ±12.5 ±12.0	±14.0 ±13.0 ±12.5	– – –	±13.5 ±12.5 ±12.0	±14.0 ±13.0 ±12.5	– – –	V
Slew Rate	SR	R_L ≥ 2kΩ (Note 2)	0.1	0.3	–	0.1	0.3	–	V/µs
Closed-Loop Bandwidth	BW	A_{VCL} = +1 (Note 2)	0.4	0.6	–	0.4	0.6	–	MHz
Open-Loop Output Resistance	R_O		–	60	–	–	60	–	Ω
Power Consumption	P_d	V_S = ±15V, No Load V_S = ±3V, No Load	– –	50 3.5	60 4.5	– –	50 3.5	60 4.5	mW
Offset Adjustment Range		R_P = 20kΩ	–	±3	–	–	±3	–	mV

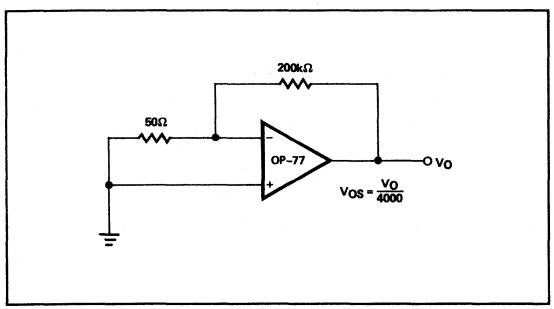
NOTES:
1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5µV.
2. Sample tested.
3. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$, unless otherwise noted.

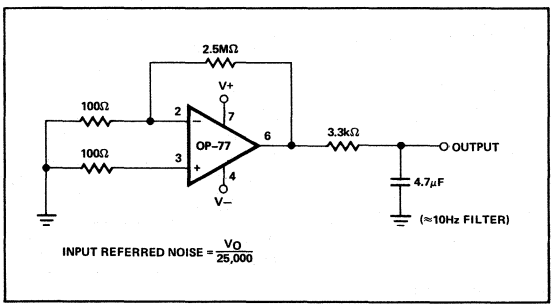
PARAMETER	SYMBOL	CONDITIONS	OP-77A MIN	OP-77A TYP	OP-77A MAX	OP-77B MIN	OP-77B TYP	OP-77B MAX	UNITS
Input Offset Voltage	V_{OS}		—	25	60	—	45	120	μV
Average Input Offset Voltage Drift	TCV_{OS}	(Note 1)	—	0.1	0.3	—	0.2	0.6	μV/°C
Input Offset Current	I_{OS}		—	0.5	2.2	—	0.5	4.5	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	1.5	25	—	1.5	50	pA/°C
Input Bias Current	I_B		−0.2	2.4	4	−0.2	2.4	6	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	8	25	—	15	35	pA/°C
Input Voltage Range	IVR		±13	±13.5	—	±13	±13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	—	0.1	1.0	—	0.1	3	μV/V
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	1	3	—	1	5	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	2000	6000	—	1000	4000	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13.0	—	±12	±13.0	—	V
Power Consumption	P_d	$V_S = \pm 15V$, No Load	—	60	75	—	60	75	mW

NOTES:
1. OP-77A: TCV_{OS} is 100% tested.
2. Guaranteed by end-point limits.

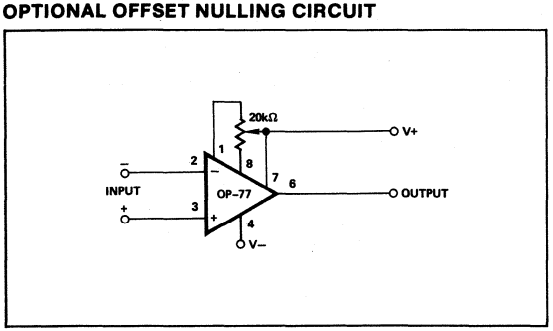
TYPICAL OFFSET VOLTAGE TEST CIRCUIT



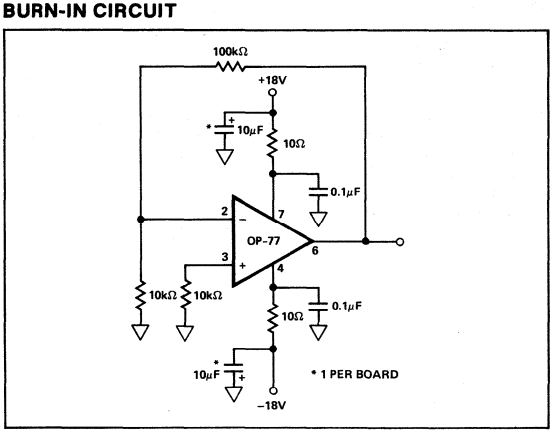
TYPICAL LOW-FREQUENCY NOISE TEST CIRCUIT



OPTIONAL OFFSET NULLING CIRCUIT



BURN-IN CIRCUIT



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-77E MIN	OP-77E TYP	OP-77E MAX	OP-77F MIN	OP-77F TYP	OP-77F MAX	OP-77G/H MIN	OP-77G/H TYP	OP-77G/H MAX	UNITS
Input Offset Voltage	V_{OS}		—	10	25	—	20	60	—	50	100	μV
Long-Term V_{OS} Stability	V_{OS}/Time	(Note 1)	—	0.3	—	—	0.4	—	—	0.4	—	μV/Mo
Input Offset Current	I_{OS}		—	0.3	1.5	—	0.3	2.8	—	0.3	2.8	nA
Input Bias Current	I_B		−0.2	1.2	2.0	−0.2	1.2	2.8	−0.2	1.2	2.8	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 2)	—	0.35	0.6	—	0.38	0.65	—	0.38	0.65	μV_{p-p}
Input Noise Voltage Density	e_n	f_O = 10Hz	—	10.3	18.0	—	10.5	20.0	—	10.5	20.0	$nV/\sqrt{Hz}$
		f_O = 100Hz (Note 2)	—	10.0	13.0	—	10.2	13.5	—	10.2	13.5	
		f_O = 1000Hz	—	9.6	11.0	—	9.8	11.5	—	9.8	11.5	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 2)	—	14	30	—	15	35	—	15	35	pA_{p-p}
Input Noise Current Density	i_n	f_O = 10Hz	—	0.32	0.80	—	0.35	0.90	—	0.35	0.90	$pA/\sqrt{Hz}$
		f_O = 100Hz (Note 2)	—	0.14	0.23	—	0.15	0.27	—	0.15	0.27	
		f_O = 1000Hz	—	0.12	0.17	—	0.13	0.18	—	0.13	0.18	
Input Resistance — Differential-Mode	R_{IN}	(Note 3)	26	45	—	18.5	45	—	18.5	45	—	MΩ
Input Resistance — Common-Mode	R_{INCM}		—	200	—	—	200	—	—	200	—	GΩ
Input Voltage Range	IVR		±13	±14	—	±13	±14	—	±13	±14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	—	0.1	1.0	—	0.1	1.6	—	0.1	1.6	μV/V
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	0.7	3.0	—	0.7	3.0	—	0.7	3.0	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	5000	12000	—	2000	6000	—	2000	6000	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	±13.5	±14.0	—	±13.5	±14.0	—	±13.5	±14.0	—	V
		$R_L \geq 2k\Omega$	±12.5	±13.0	—	±12.5	±13.0	—	±12.5	±13.0	—	
		$R_L \geq 1k\Omega$	±12.0	±12.5	—	±12.0	±12.5	—	±12.0	±12.5	—	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 2)	0.1	0.3	—	0.1	0.3	—	0.1	0.3	—	V/μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$ (Note 2)	0.4	0.6	—	0.4	0.6	—	0.4	0.6	—	MHz
Open-Loop Output Resistance	R_O		—	60	—	—	60	—	—	60	—	Ω
Power Consumption	P_d	$V_S = \pm 15V$, No Load	—	50	60	—	50	60	—	50	60	mW
		$V_S = \pm 3V$, No Load	—	3.5	4.5	—	3.5	4.5	—	3.5	4.5	
Offset Adjustment Range		$R_P = 20k\Omega$	—	±3	—	—	±3	—	—	±3	—	mV

NOTES:

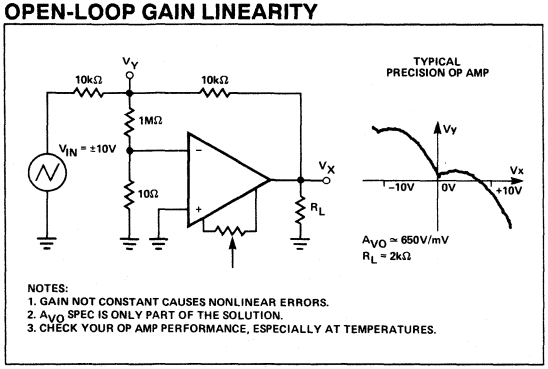
1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV.
2. Sample tested.
3. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, –25°C ≤ T_A ≤ +85°C for OP-77E/FJ and OP-77E/FZ, 0°C ≤ T_A ≤ +70°C for OP-77E/F/GP/GS, –40°C ≤ TA ≤ +85°C for OP-77HP/HS, unless otherwise noted.

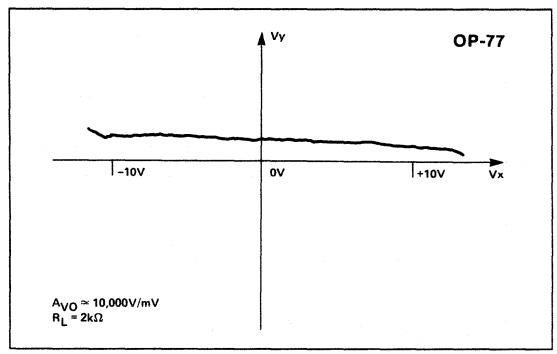
PARAMETER	SYMBOL	CONDITIONS	OP-77E MIN	OP-77E TYP	OP-77E MAX	OP-77F MIN	OP-77F TYP	OP-77F MAX	OP-77G/H MIN	OP-77G/H TYP	OP-77G/H MAX	UNITS
Input Offset Voltage	V_{OS}	J, Z Packages	–	10	45	–	20	100	–	–	–	µV
		P Package	–	10	55	–	20	100	–	80	150	
Average Input Offset Voltage Drift	TVC_{OS}	J, Z Packages (Note 1)	–	0.1	0.3	–	0.2	0.6	–	–	–	µV/°C
		P Package (Note 1)	–	0.3	0.6	–	0.4	1.0	–	0.7	1.2	
Input Offset Current	I_{OS}		–	0.5	2.2	–	0.5	4.5	–	0.5	4.5	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	–	1.5	40	–	1.5	85	–	1.5	85	pA/°C
Input Bias Current	I_B	E, F, G Grades	–0.2	2.4	4.0	–0.2	2.4	6.0	–0.2	2.4	6.0	nA
		H Grade	–	–	–	–	–	–	–	2.4	±6.0	
Average Input Bias Current Drift	TCI_B	(Note 2)	–	8	40	–	15	60	–	15	60	pA/°C
Input Voltage Range	IVR		±13.0	±13.5	–	±13.0	±13.5	–	±13.0	±13.5	–	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V	–	0.1	1.0	–	0.1	3.0	–	0.1	3.0	µV/V
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	–	1.0	3.0	–	1.0	5.0	–	1.0	5.0	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ, V_O = ±10V	2000	6000	–	1000	4000	–	1000	4000	–	V/mV
Output Voltage Swing	V_O	R_L ≥ 2kΩ	±12	±13.0	–	±12	±13.0	–	±12	±13.0	–	V
Power Consumption	P_d	V_S = ±15V, No Load	–	60	75	–	60	75	–	60	75	mW

NOTES:
1. OP-77E: TCV_{OS} is 100% tested on J and Z packages.
2. Guaranteed by end-point limits.

OPEN-LOOP GAIN LINEARITY



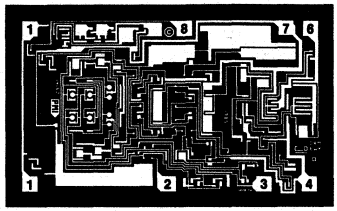
NOTES:
1. GAIN NOT CONSTANT CAUSES NONLINEAR ERRORS.
2. A_{VO} SPEC IS ONLY PART OF THE SOLUTION.
3. CHECK YOUR OP AMP PERFORMANCE, ESPECIALLY AT TEMPERATURES.



Actual open-loop voltage gain can vary greatly at various output voltages. All automated testers use end-point testing and therefore only show the average gain. This causes errors in high closed-loop gain circuits. Since this is so difficult for manufacturers to test, you should make your own evaluation. This simple test circuit makes it easy. An ideal op amp would show a horizontal scope trace.

This is the output gain linearity trace for the new OP-77. The output trace is virtually horizontal at all points, assuring extremely high gain accuracy. The average open-loop gain is truly impressive – approximately 10,000,000.

DICE CHARACTERISTICS



DIE SIZE 0.093 × 0.057 inch, 5301 sq. mils
(2.36 × 1.45 mm, 3.42 sq. mm)

1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V−
6. OUTPUT
7. V+
8. BALANCE

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$ for OP-77N/G devices.

PARAMETER	SYMBOL	CONDITIONS	OP-77N LIMIT	OP-77G LIMIT	UNITS
Input Offset Voltage	V_{OS}		40	75	μV MAX
Input Offset Current	I_{OS}		2.0	2.8	nA MAX
Input Bias Current	I_B		±2	±2.8	nA MAX
Input Resistance Differential-Mode	R_{IN}	(Note 1)	26	17	MΩ MIN
Input Voltage Range	IVR		±13	±13	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	1	1.6	μV/V MAX
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	3	3	μV/V MAX
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$ $R_L = 1k\Omega$	±13.5 ±12.5 ±12.0	±13.5 ±12.5 ±12.0	V MIN
Large-Signal Voltage Gain	A_{VO}	$R_L = 2k\Omega$ $V_O = \pm 10V$	2000	1000	V/mV MIN
Differential Input Voltage			±30	±30	V MAX
Power Consumption	P_d	$V_{OUT} = 0V$	60	60	mW MAX

NOTES:
1. Guaranteed by design.

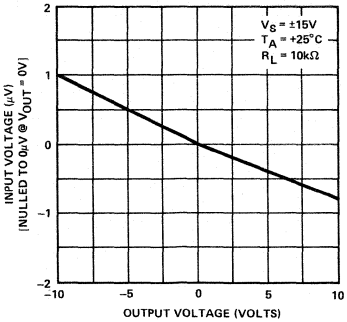
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

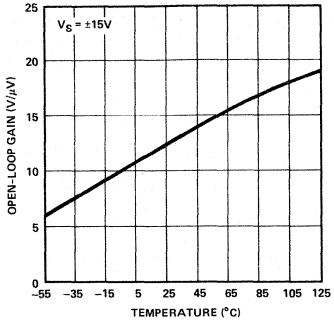
PARAMETER	SYMBOL	CONDITIONS	OP-77N TYPICAL	OP-77G TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	0.1	0.2	μV/°C
Nulled Input Offset Voltage Drift	TCV_{OSn}	$R_S = 50\Omega$, $R_P = 20k\Omega$	0.1	0.2	μV/°C
Average Input Offset Current Drift	TCI_{OS}		0.5	0.5	pA/°C
Slew Rate	SR	$R_L \geq 2k\Omega$	0.3	0.3	V/μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$	0.6	0.6	MHz

TYPICAL PERFORMANCE CHARACTERISTICS

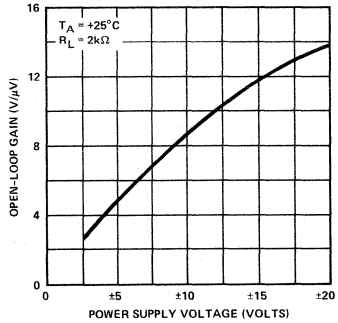
GAIN LINEARITY (INPUT VOLTAGE vs OUTPUT VOLTAGE)



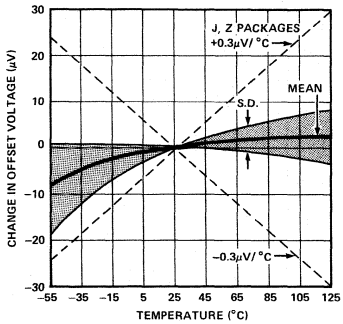
OPEN-LOOP GAIN vs TEMPERATURE



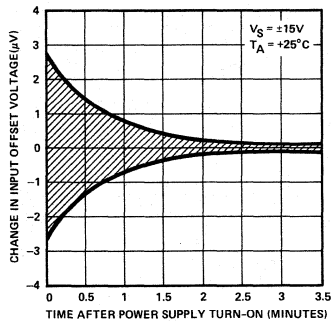
OPEN-LOOP GAIN vs POWER SUPPLY VOLTAGE



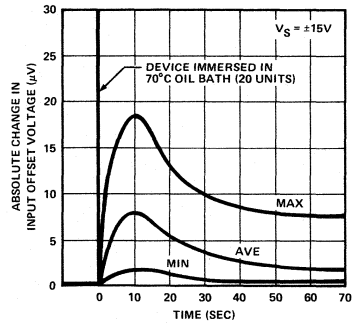
UNTRIMMED OFFSET VOLTAGE vs TEMPERATURE



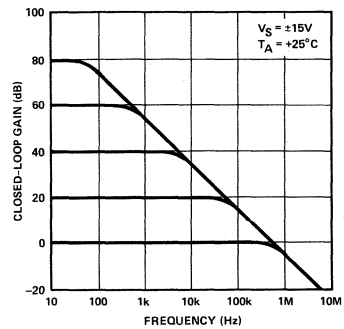
WARM-UP DRIFT



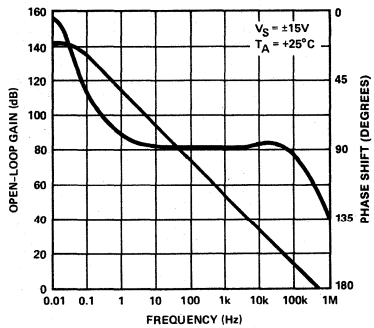
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



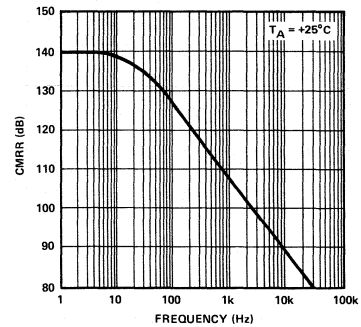
CLOSED-LOOP RESPONSE FOR VARIOUS GAIN CONFIGURATIONS



OPEN-LOOP GAIN/PHASE RESPONSE

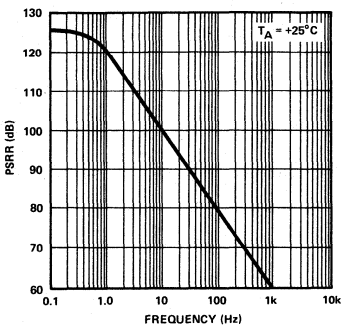


CMRR vs FREQUENCY

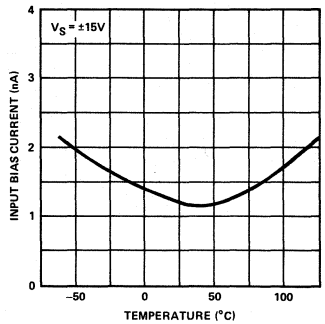


TYPICAL PERFORMANCE CHARACTERISTICS

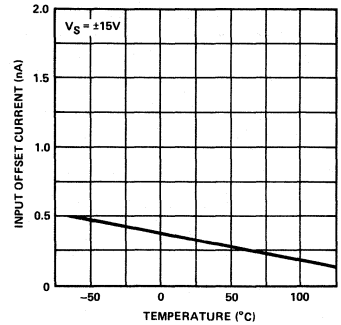
PSRR vs FREQUENCY



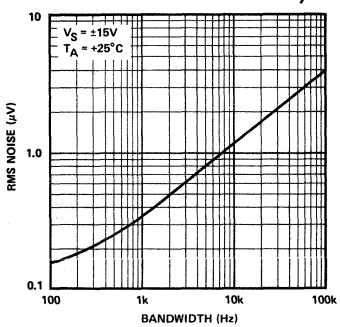
INPUT BIAS CURRENT vs TEMPERATURE



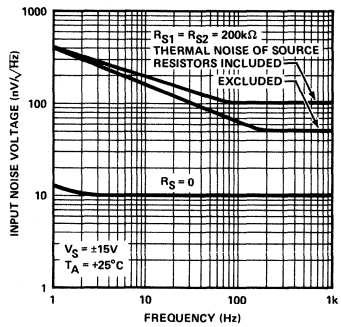
INPUT OFFSET CURRENT vs TEMPERATURE



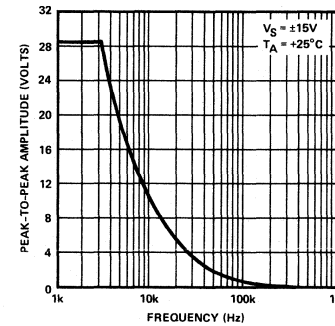
INPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



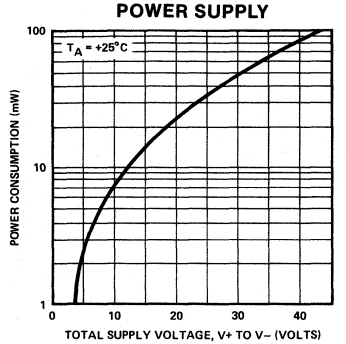
TOTAL INPUT NOISE VOLTAGE vs FREQUENCY



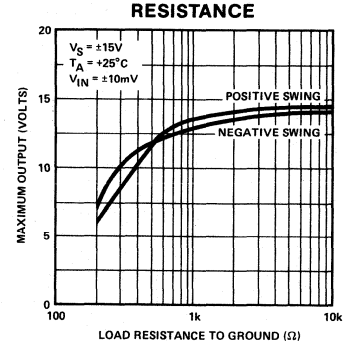
MAXIMUM OUTPUT SWING vs FREQUENCY



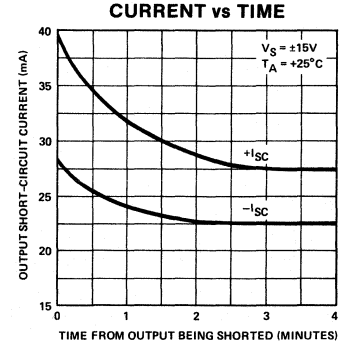
POWER CONSUMPTION vs POWER SUPPLY



MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE

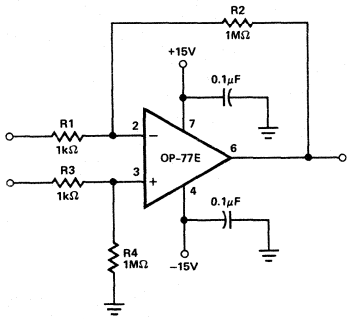


OUTPUT SHORT-CIRCUIT CURRENT vs TIME



APPLICATIONS INFORMATION

PRECISION HIGH-GAIN DIFFERENTIAL AMPLIFIER

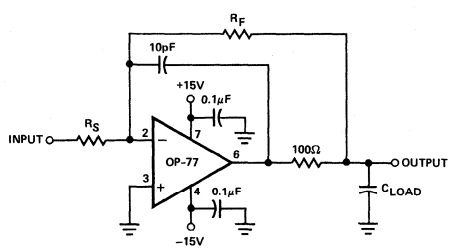


The high gain, gain linearity, CMRR, and low TCV_{OS} of the OP-77 make it possible to obtain performance not previously available in single stage very high-gain amplifier applications.

For best CMR, $\frac{R1}{R2}$ must equal $\frac{R3}{R4}$. In this example, with a 10mV differential signal, the maximum errors are as listed.

TYPE	AMOUNT
COMMON-MODE VOLTAGE	0.01%/V
GAIN LINEARITY, WORST CASE	0.02%
TCV_{OS}	0.003%/°C
TCI_{OS}	0.008%/°C

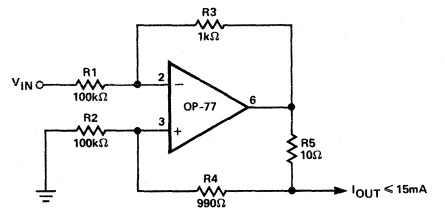
ISOLATING LARGE CAPACITIVE LOADS



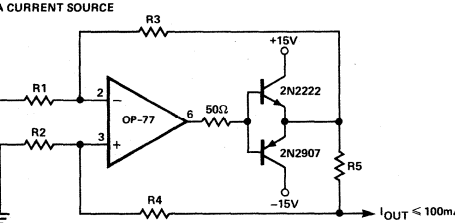
This circuit reduces maximum slew-rate but allows driving capacitive loads of any size without instability. Because the 100Ω resistor is inside the feedback loop, its effect on output impedance is reduced to insignificance by the high open-loop gain of the OP-77.

BILATERAL CURRENT SOURCE

BASIC CURRENT SOURCE



100mA CURRENT SOURCE



$I_{OUT} = V_{IN} \frac{R3}{R1 \cdot R5}$

GIVEN R3 = R4 + R5, R1 = R2

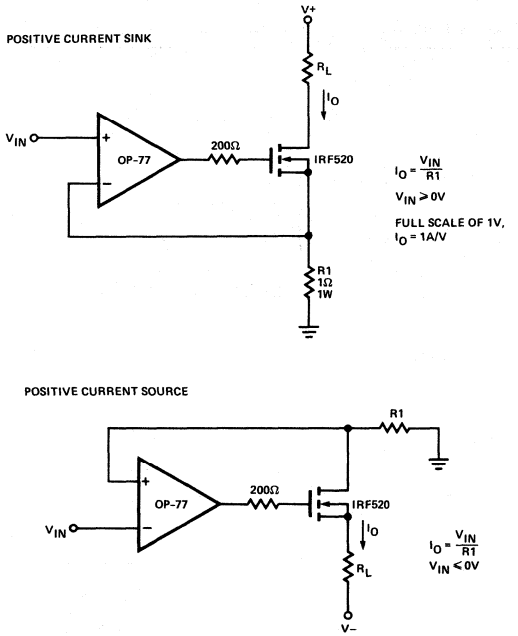
These current sources will supply both positive and negative current into a grounded load.

Note that $Z_O = \frac{R5\left(\frac{R4}{R2}+1\right)}{\frac{R5+R4}{R2} - \frac{R3}{R1}}$

and that for Z_O to be infinite,

$\frac{R5+R4}{R2}$ must $= \frac{R3}{R1}$.

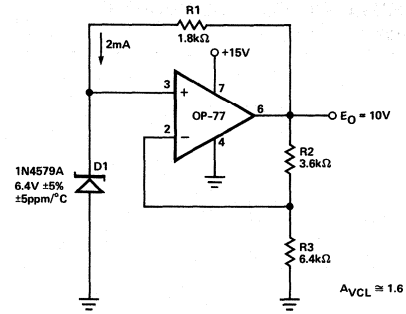
PRECISION CURRENT SINKS



These simple high current sinks require that the load float between the power supply and the sink.

In these circuits, OP-77's high gain, high CMRR, and low TCV_{OS} assure high accuracy.

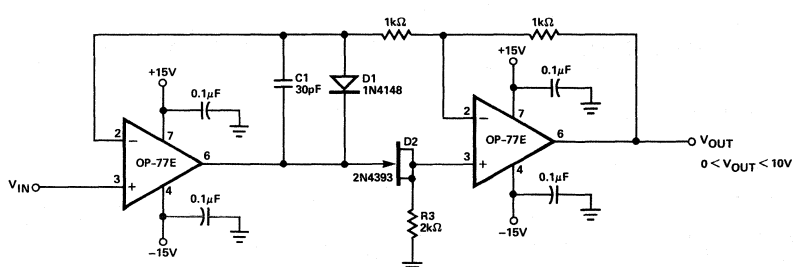
HIGH STABILITY VOLTAGE REFERENCE



This simple bootstrapped voltage reference provides a precise 10 volts virtually independent of changes in power supply voltage, ambient temperature, and output loading. Correct zener operating current of exactly 2mA is maintained by R1, a selected 5ppm/°C resistor, connected to the regulated output. Accuracy is primarily determined by three factors: the 5ppm/°C temperature coefficient of D1, 1ppm/°C ratio tracking of R2 and R3, and operational amplifier V_{OS} errors.

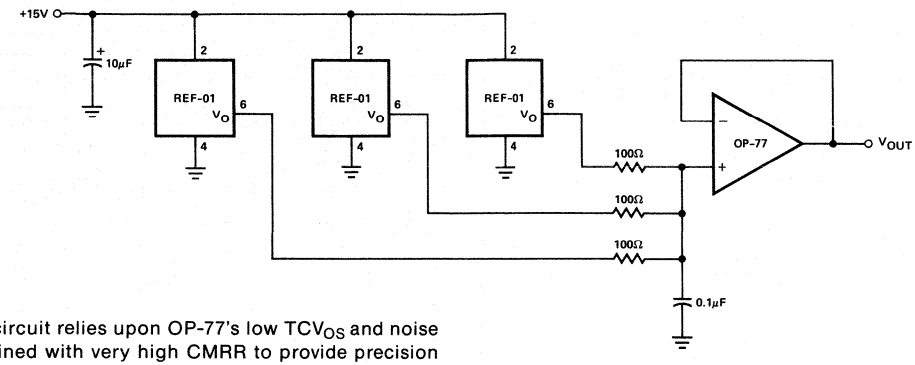
V_{OS} errors, amplified by 1.6 (A_{VCL}), appear at the output and can be significant with most monolithic amplifiers. For example: an ordinary amplifier with TCV_{OS} of 5μV/°C contributes 0.8ppm/°C of output error while the OP-77, with TCV_{OS} of 0.3μV/°C, contributes but 0.05ppm/°C of output error, thus effectively eliminating TCV_{OS} as an error consideration.

PRECISION ABSOLUTE VALUE AMPLIFIER



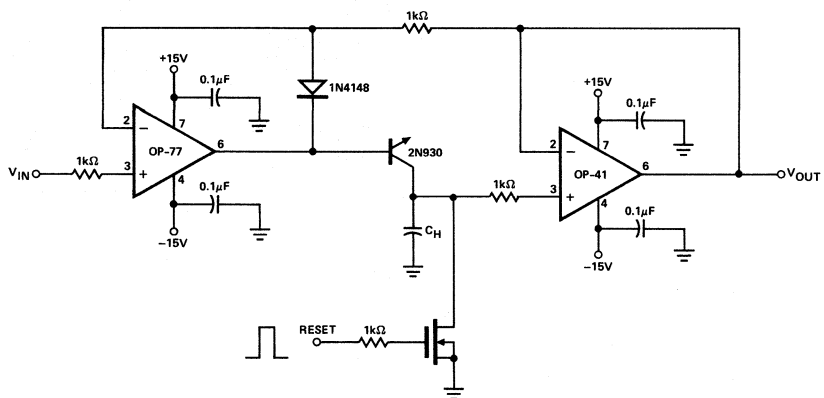
The high gain and low TCV_{OS} assure accurate operation with inputs from microvolts to volts. In this circuit, the signal always appears as a common-mode signal to the op amps. The OP-77E CMRR of 1μV/V assures errors of less than 2ppm.

LOW NOISE PRECISION REFERENCE



This circuit relies upon OP-77's low TCV_{OS} and noise combined with very high CMRR to provide precision buffering of the averaged REF-01 voltage outputs.

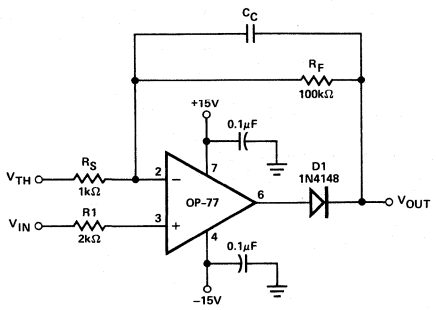
PRECISION POSITIVE PEAK DETECTOR



C_H must be of polystyrene, Teflon*, or polyethylene to minimize dielectric absorption and leakage. The droop rate is determined by the size of C_H and the bias current of the OP-41.

*Teflon is a registered trademark of the Dupont Company.

PRECISION THRESHOLD DETECTOR/ AMPLIFIER

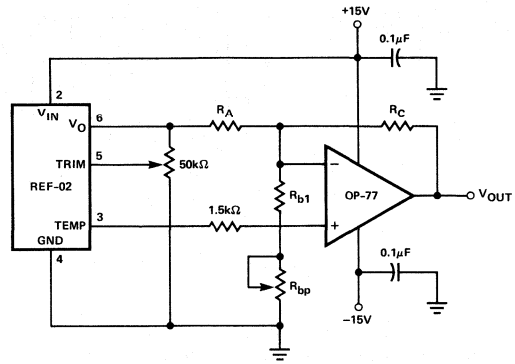


When $V_{IN} < V_{TH}$, amplifier output swings negative, reverse biasing diode D1. $V_{OUT} = V_{TH}$ if $R_L = \infty$. When $V_{IN} \geq V_{TH}$, the loop closes,

$$V_{OUT} = V_{TH} + (V_{IN} - V_{TH}) \left(1 + \frac{R_F}{R_S}\right).$$

C_C is selected to smooth the response of the loop.

PRECISION TEMPERATURE SENSOR



RESISTOR VALUES

TCV_{OUT} SLOPE (S)	10mV/°C	100mV/°C	10mV/°F
TEMPERATURE RANGE	−55°C to +125°C	−55°C to +125°C	−67°F to +257°C
OUTPUT VOLTAGE RANGE	−0.55V to +1.25V	−5.5V to +12.5V	−0.67V to +2.57V
ZERO-SCALE	0V @ 0°C	0V @ 0°C	0V @ 0°F
R_a (±1% Resistor)	9.09kΩ	15kΩ	7.5kΩ
R_{b1} (±1% Resistor)	1.5kΩ	1.82kΩ	1.21kΩ
R_{bp} (Potentiometer)	200Ω	500Ω	200Ω
R_c (±1% Resistor)	5.11kΩ	84.5kΩ	8.25kΩ

Ultra-Low Bias Current Operational Amplifier

OP-80

FEATURES

- **Ultra-Low Bias Current:**
  - **150 femtoamps Typ ..... at +25°C**
  - **300 femtoamps Typ ..... at +85°C**
  - **500 femtoamps Typ ..... at +125°C**
- **True Single Supply Operation**
  - **Common-Mode Range Includes Ground**
  - **Output Swings to Within 200μV of Ground Without Pulldown Resistors**
- **Low Supply Current ..... 325μA Max**
- **Lower Cost Alternative to AD549 and OPA128**
- **Low Cost**
- **Inputs Protected Against 700V of Static Discharge**
- **Available in Die Form**

APPLICATIONS

- **Electrometer Amplifier Input Stage**
- **Photodiode and Infrared Detector Preamplifier**
- **Chemical and Gas Analyzers**
- **pH Probe Buffer Amplifier**
- **Fire Detectors**
- **High Voltage Voltmeters**
- **Charge Amplifiers**

GENERAL DESCRIPTION

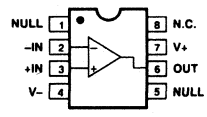
The OP-80 is a low cost CMOS operational amplifier offering exceptionally low input currents over a wide operating temperature range. Input current is typically 150 femtoamps at 25°C and increases to only 300 femtoamps at +85°C, with exceptionally high common-mode and differential input impedances. Incorporating a novel input protection design, the OP-80 achieves over 700V of ESD protection while maintaining very low input current.

For systems demanding both high performance at low supply voltages and high input impedances, the OP-80 is a powerful design tool. It is ideal for use in electrometers, portable medical instrumentation, chemical analyzers, smoke detectors, and sensitive current-to-voltage conversion circuits for photodiodes.

The low supply current minimizes thermal power dissipation, virtually eliminating the effects of chip self-heating. The OP-80's CMOS design gives a good speed/power ratio, permitting a

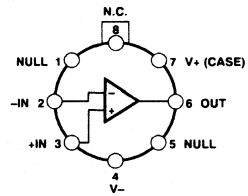
Continued

PIN CONNECTIONS



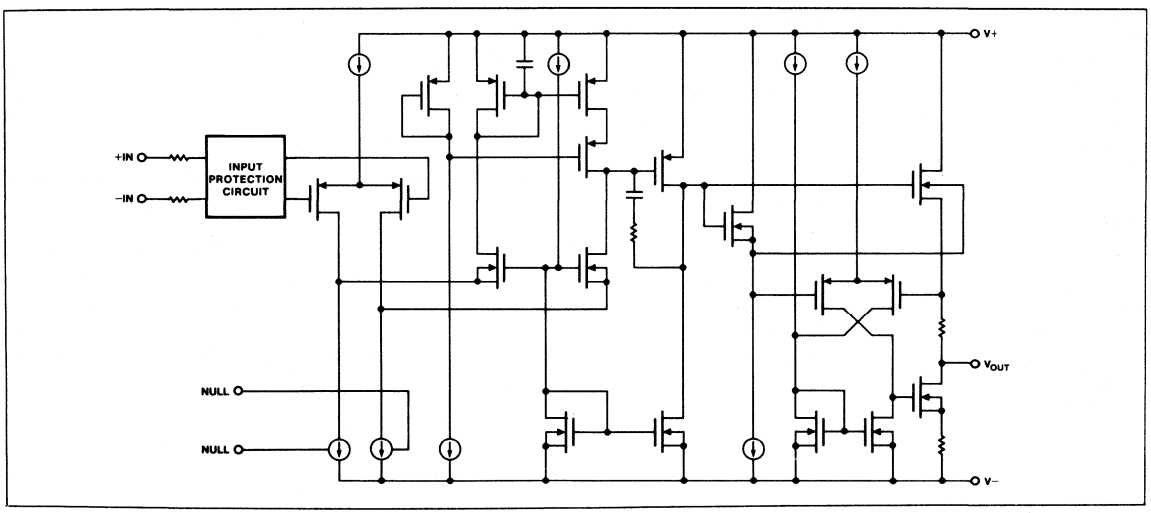
8-PIN PLASTIC DIP
(P-Suffix)

8-PIN SO
(S-Suffix)



TO-99
(J-Suffix)

SIMPLIFIED SCHEMATIC



GENERAL DESCRIPTION *Continued*

0.2V/μs minimum slew rate and a 300kHz gain-bandwidth product with unity-gain stability.

The OP-80 offers greater than 100dB of gain into a 2kΩ load, with output source/sink capability exceeding 15mA. In single supply applications, the OP-80's input range and output swing extends to ground. No pull-down resistor is required for the output to actively swing to within 200μV of ground.

Other applications for the OP-80 include precision pH, conductivity and ion measurement systems, low-level light and infrared detectors, barcode readers, and magnetic and electric field detectors. Its exceptional versatility makes it suitable for general-purpose applications, especially those requiring a single +5V supply.

The OP-80 conforms to the industry-standard 741 pinout, with the nulling potentiometer between pins 1 and 5, and the wiper to V–.

ORDERING INFORMATION †

I_B (pA)	PACKAGE TO-99	PACKAGE PLASTIC 8-PIN	OPERATING TEMPERATURE RANGE
2.0	OP80BJ*	–	MIL
0.250	OP80EJ	–	XIND
1.0	OP80FJ	–	XIND
2.0	–	OP80GP	XIND
2.0	–	OP80GS††	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO packages, contact your local sales office.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±8V
Input Voltage (Note 2) ..... +8V, –8.2V
Differential Input Voltage (Note 2) 16V
Output Short-Circuit Duration (Note 3) ..... Indefinite
Operating Temperature Range
OP-80G (P,S) ..... –40°C to +85°C
OP-80E,F,G (J) ..... –40°C to +85°C
OP-80B (J) ..... –55°C to +125°C
Storage Temperature Range ..... –65°C to +175°C
Junction Temperature Range ..... –65°C to +175°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE TYPE	Θ_{JA} (Note 4)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:

1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. For supply voltages less than ±8V, the absolute maximum input voltage is equal to (V+) and (V– –0.2V).
3. The output may be shorted to ground indefinitely, but current must be externally limited to 25mA if the output is shorted to V+.
4. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V_S = ±5V, V_{CM} = 0V, T_A = +25°C.

PARAMETER	SYMBOL	CONDITIONS	OP-80E MIN	OP-80E TYP	OP-80E MAX	OP-80F MIN	OP-80F TYP	OP-80F MAX	UNITS
Input Offset Voltage	V_{OS}		–	0.2	1.5	–	0.4	1.5	mV
Input Offset Current	I_{OS}		–	50	–	–	80	–	fA
Input Bias Current	I_B		–	0.15	0.250	–	0.2	1.0	pA
Input Voltage Range	IVR	Lower Limit Upper Limit	– –	(V –0V) (V + –1.5V)	– –	– –	(V –0V) (V + –1.5V)	– –	V
Common-Mode Rejection	CMR	V_{CM} = –4.75V, 3.5V	50	70	–	50	65	–	dB
Power-Supply Rejection	PSR	V_S = ±2.25V to ±8V	60	80	–	60	76	–	dB
Large-Signal Voltage Gain	A_{VO}	V_O = –4.5V to +3.25V, R_L = 10kΩ	100	400	–	100	300	–	V/mV

ELECTRICAL CHARACTERISTICS at V_S = ±5V, V_{CM} = 0V, T_A = +25°C. *Continued*

PARAMETER	SYMBOL	CONDITIONS	OP-80E MIN	OP-80E TYP	OP-80E MAX	OP-80F MIN	OP-80F TYP	OP-80F MAX	UNITS
Output Voltage Swing	V_O	V_S = ±5V, R_L = 10kΩ	+3.5/ −4.75	+3.7/ −4.9	–	+3.5/ −4.75	+3.7/ −4.9	–	V
	V_{OH}	V+ = +5V, V– = 0V, R_L = 10kΩ	+3.5	+3.7	–	+3.5	+3.7	–	V
	V_{OL}	V+ = +5V, V– = 0V, R_L = 10kΩ	–	0.2	1	–	0.2	1	mV
Supply Current	I_{SY}	No Load	–	200	325	–	200	325	µA
Input Noise Voltage Density	e_n	f_O = 1000Hz	–	70	–	–	70	–	nV/√Hz
Output Current	I_{OUT}	Source Sink	25 15	45 24	– –	25 15	45 24	– –	mA
Slew Rate	SR	A_V = +1	0.2	0.4	–	0.2	0.4	–	V/µs
Gain-Bandwidth Product	GBW		–	300	–	–	300	–	kHz
Input Resistance		Common-Mode Differential	– –	10^{16} 10^{13}	– –	– –	10^{16} 10^{13}	– –	Ω

ELECTRICAL CHARACTERISTICS at V_S = ±5V, V_{CM} = 0V, T_A = +25°C.

PARAMETER	SYMBOL	CONDITIONS	OP-80B MIN	OP-80B TYP	OP-80B MAX	UNITS
Input Offset Voltage	V_{OS}		–	0.5	2.0	mV
Input Offset Current	I_{OS}		–	100	–	fA
Input Bias Current	I_B		–	0.6	2.0	pA
Input Voltage Range	IVR	Lower Limit Upper Limit	– –	(V –0V) (V + –1.5V)	– –	V
Common-Mode Rejection	CMR	V_{CM} = –4.75V, 3.5V	50	65	–	dB
Power-Supply Rejection	PSR	V_S = ±2.25V to ±8V	60	76	–	dB
Large-Signal Voltage Gain	A_{VO}	V_O = –4.5V to +3.25V, R_L = 10kΩ	100	225	–	V/mV
Output Voltage Swing	V_O	V_S = ±5V, R_L = 10kΩ	+3.5/ −4.75	+3.7/ −4.9	–	V
	V_{OH}	V+ = +5V, V– = 0V, R_L = 10kΩ	+3.5	+3.7	–	V
	V_{OL}	V+ = +5V, V– = 0V, R_L = 10kΩ	–	0.2	1	mV
Supply Current	I_{SY}	No Load	–	200	325	µA
Input Noise Voltage Density	e_n	f_O = 1000Hz	–	70	–	nV/√Hz
Output Current	I_{OUT}	Source Sink	25 15	45 24	– –	mA
Slew Rate	SR	A_V = +1	0.2	0.4	–	V/µs
Gain-Bandwidth Product		GBW	–	300	–	kHz
Input Resistance		Common-Mode Differential	– –	10^{16} 10^{13}	– –	Ω

ELECTRICAL CHARACTERISTICS at $V_S = \pm5V$, $V_{CM} = 0V$, $-40°C \le T_A \le +85°C$ for E/F grades; $-55°C \le T_A \le +125°C$ for B grade.

PARAMETER	SYMBOL	CONDITIONS	OP-80E/F MIN	OP-80E/F TYP	OP-80E/F MAX	OP-80B MIN	OP-80B TYP	OP-80B MAX	UNITS
Input Offset Voltage	V_{OS}		–	0.5	5.0	–	1.0	8.0	mV
Input Bias Current	I_B	(Note 1)	–	0.3	15	–	0.5	50	pA
Common-Mode Rejection	CMR	$V_{CM} = -4.75, 3.5V$	50	90	–	50	85	–	dB
Power-Supply Rejection	PSR	$V_S = \pm2.25V$ to $\pm8V$	60	85	–	57	80	–	dB
Large-Signal Voltage Gain	A_{VO}	$V_O = -4.5V$ to $+3.25V$, $R_L = 10k\Omega$	50	400	–	20	350	–	V/mV
Output Voltage Swing	V_O	$V_S = \pm5V$, $R_L = 10k\Omega$	+3.25/ −4.75	+3.7/ −4.9	–	+3.25/ −4.75	+3.7/ −4.9	–	V
	V_{OH}	V+ = +5V, V− = 0V, $R_L = 10k\Omega$	+3.25	+3.7	–	+3.25	+3.7	–	V
	V_{OL}	V+ = +5V, V− = 0V, $R_L = 10k\Omega$	–	0.1	1.0	–	0.15	1.0	mV
Supply Current	I_{SY}	No Load	–	275	400	–	275	400	µA
Output Current	I_{OUT}	Source Sink	25 15	35 19	– –	20 15	35 19	– –	mA

NOTE:
1. Specification applies to +85°C and +125°C only.

ELECTRICAL CHARACTERISTICS at $V_S = \pm5V$, $V_{CM} = 0V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-80G MIN	OP-80G TYP	OP-80G MAX	UNITS
Input Offset Voltage	V_{OS}		–	0.6	2.5	mV
Input Offset Current	I_{OS}		–	100	–	fA
Input Bias Current	I_B		–	400	2000	fA
Input Voltage Range	IVR	Lower Limit Upper Limit		(V− −0V) (V+ −1.5V)		V
Common-Mode Rejection	CMR	$V_{CM} = -4.75V, 3.5V$	50	90	–	dB
Power-Supply Rejection	PSR	$V_S = \pm2.25V$ to $\pm8V$	60	80	–	dB
Large-Signal Voltage Gain	A_{VO}	$V_O = -4.5V$ to $+3.25V$, $R_L = 10k\Omega$	75	350	–	V/mV
Output Voltage Swing	V_O	$V_S = \pm5V$, $R_L = 10k\Omega$	+3.5/−4.75	+3.7/−4.9	–	V
	V_{OH}	V+ = +5V, V− = 0V, $R_L = 10k\Omega$	+3.5	+3.7	–	V
	V_{OL}	V+ = +5V, V− = 0V, $R_L = 10k\Omega$	–	0.2	1	mV

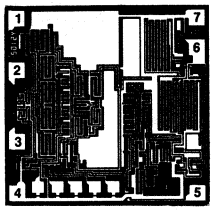
ELECTRICAL CHARACTERISTICS at $V_S = \pm5V$, $V_{CM} = 0V$, $T_A = +25°C$, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	OP-80G MIN	OP-80G TYP	OP-80G MAX	UNITS
Supply Current	I_{SY}	No Load	–	220	325	µA
Input Noise Voltage Density	e_n	$f_O = 1000Hz$	–	70	–	$nV/\sqrt{Hz}$
Output Current	I_{OUT}	Source Sink	25 15	45 22	– –	mA
Slew Rate	SR	$A_V = +1$	0.2	0.4	–	V/µs
Gain-Bandwidth Product	GBW		–	300	–	kHz
Input Resistance		Common-Mode Differential	– –	10^{16} 10^{13}	– –	Ω

ELECTRICAL CHARACTERISTICS at $V_S = \pm5V$, $V_{CM} = 0V$, $-40°C \le T_A \le +85°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-80G MIN	OP-80G TYP	OP-80G MAX	UNITS
Input Offset Voltage	V_{OS}		–	2.0	7.0	mV
Input Bias Current	I_B		–	0.6	50	pA
Common-Mode Rejection	CMR	$V_{CM} = -4.75V, 3.5V$	50	80	–	dB
Power-Supply Rejection	PSR	$V_S = \pm2.25V$ to $\pm8V$	57	80	–	dB
Large-Signal Voltage Gain	A_{VO}	$V_O = -4.5V$ to $+3.25V$, $R_L = 10k\Omega$	50	300	–	V/mV
Output Voltage Swing	V_O	$V_S = \pm5V$, $R_L = 10k\Omega$	+3.25/–4.50	+3.7/–4.9	–	V
	V_{OH}	$V+ = +5V, V- = 0V$, $R_L = 10k\Omega$	+3.25	+3.7	–	V
	V_{OL}	$V+ = +5V, V- = 0V$, $R_L = 10k\Omega$	–	0.2	1	mV
Supply Current	I_{SY}	No Load	–	275	400	µA
Output Current	I_{OUT}	Source Sink	25 15	35 19	– –	mA

DICE CHARACTERISTICS



DIE SIZE 0.070 X 0.069 inch, 4,830 sq. mils
(1.78 X 1.75mm, 3.12 sq. mm)

1. NULL
2. INPUT (–)
3. INPUT (+)
4. V–
5. NULL
6. OUTPUT
7. V+

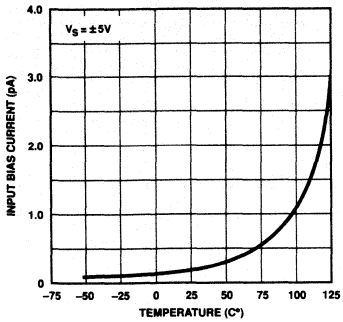
WAFER TEST LIMITS at $V_S = \pm5V$, $V_{CM} = 0V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-80G LIMITS	UNITS
Input Offset Voltage	V_{OS}		2.5	mV MAX
Input Bias Current	I_B		50	pA MAX
Common-Mode Rejection	CMR	$V_{CM} = -4.75V, +3.5$	50	dB MIN
Power-Supply Rejection	PSR	$V_S = \pm2.25V$ to $\pm8V$	60	dB MIN
Large-Signal Voltage Gain	A_{VO}	$V_O = -4.5V$ to $+3.25V$ $R_L = 10k\Omega$	75	V/mV MIN
Output Voltage Swing	V_O	$V_S = \pm5V$, $R_L = 10k\Omega$	+3.5/–4.75	V MIN
	V_{OH}	$V+ = +5V, V- = 0V$, $R_L = 10k\Omega$	+3.5	V MIN
	V_{OL}	$V+ = +5V, V- = 0V$, $R_L = 10k\Omega$	1	mV MAX
Supply Current	I_{SY}	No Load	325	µA MAX
Output Current	I_{OUT}	Source Sink	25 15	mA MIN

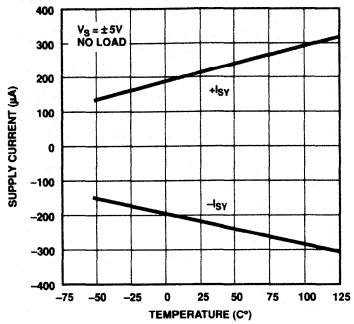
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS

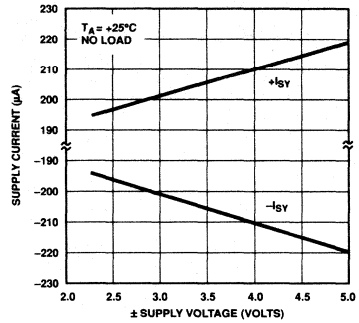
INPUT BIAS CURRENT vs TEMPERATURE



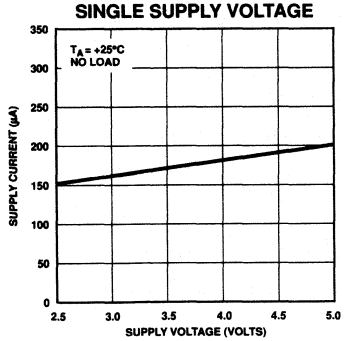
SUPPLY CURRENT vs TEMPERATURE



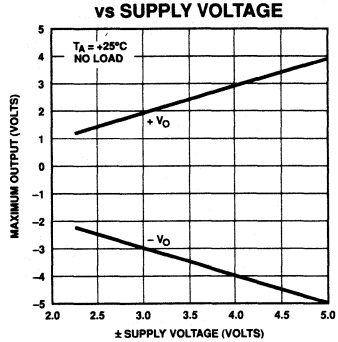
SUPPLY CURRENT vs SUPPLY VOLTAGE



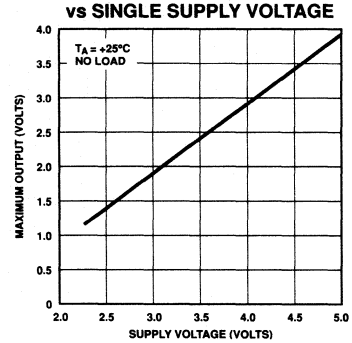
SUPPLY CURRENT vs SINGLE SUPPLY VOLTAGE



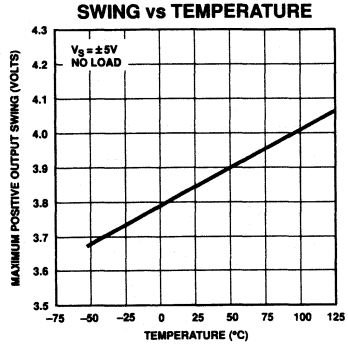
MAXIMUM OUTPUT VOLTAGE vs SUPPLY VOLTAGE



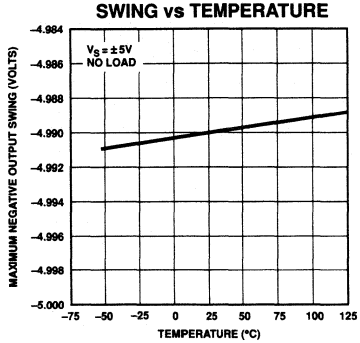
OUTPUT VOLTAGE SWING vs SINGLE SUPPLY VOLTAGE



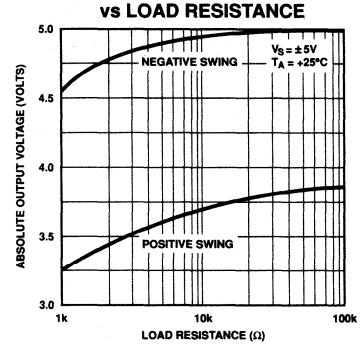
MAXIMUM POSITIVE OUTPUT SWING vs TEMPERATURE



MAXIMUM NEGATIVE OUTPUT SWING vs TEMPERATURE

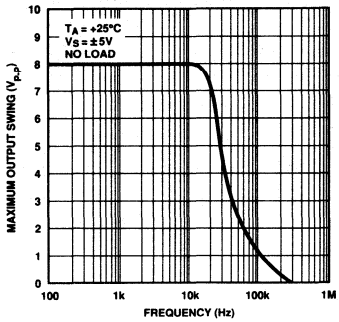


MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE

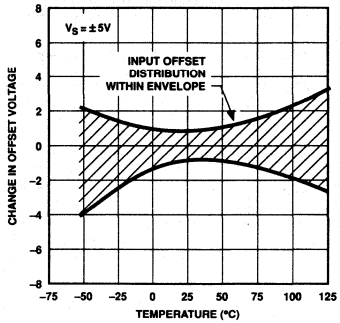


TYPICAL ELECTRICAL CHARACTERISTICS *Continued*

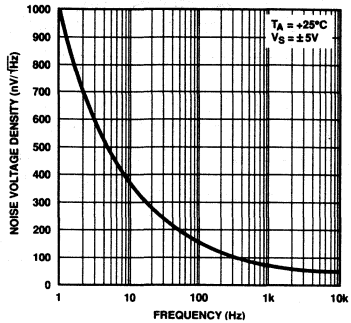
MAXIMUM OUTPUT SWING vs FREQUENCY



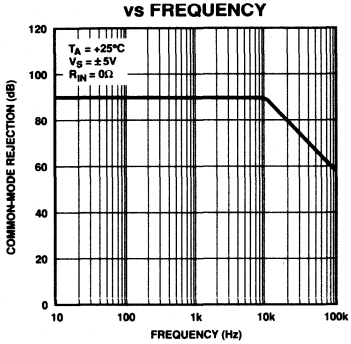
INPUT OFFSET VOLTAGE vs TEMPERATURE



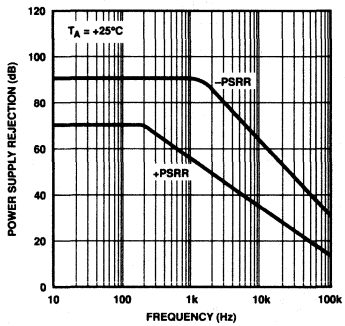
NOISE VOLTAGE DENSITY vs FREQUENCY



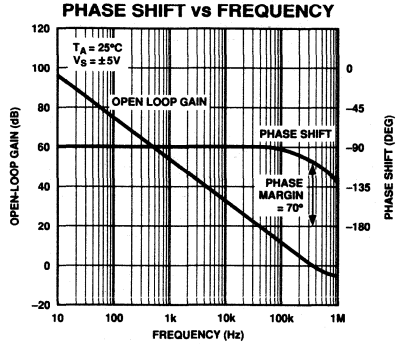
COMMON-MODE REJECTION vs FREQUENCY



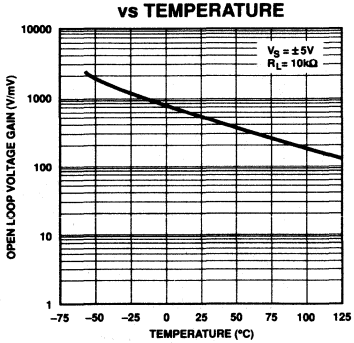
POWER SUPPLY REJECTION vs FREQUENCY



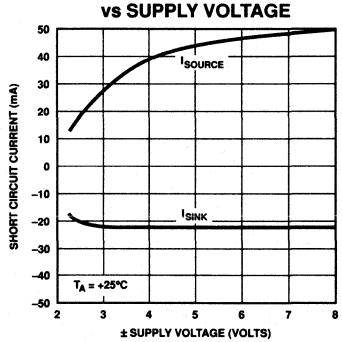
OPEN-LOOP GAIN AND PHASE SHIFT vs FREQUENCY



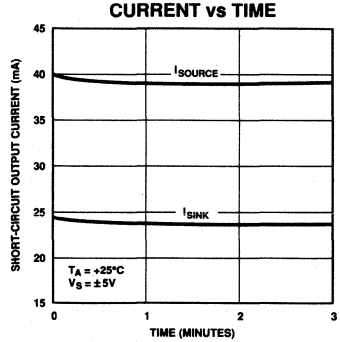
OPEN LOOP GAIN vs TEMPERATURE



SHORT CIRCUIT CURRENT vs SUPPLY VOLTAGE

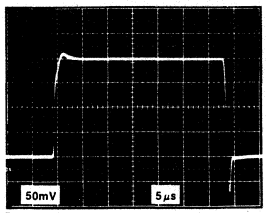


SHORT-CIRCUIT OUTPUT CURRENT vs TIME



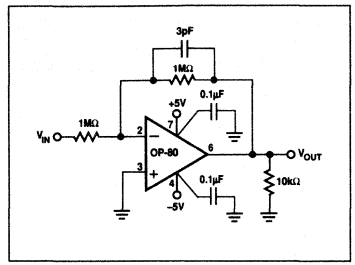
TYPICAL ELECTRICAL CHARACTERISTICS *Continued*

SMALL-SIGNAL TRANSIENT RESPONSE

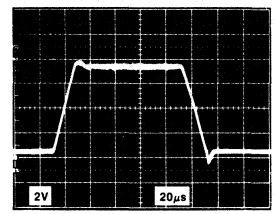


$T_A = +25°C$
$V_S = \pm 5V$
$R_L = 10k\Omega$
$C_L = 100pF$
$A_V = +1$

TEST CIRCUIT FOR LARGE-SIGNAL TRANSIENT RESPONSE



LARGE-SIGNAL TRANSIENT RESPONSE



$T_A = +25°C$
$V_S = \pm 5V$
$R_L = 10k\Omega$
$A_V = -1$

APPLICATIONS INFORMATION

Offering one of the lowest input currents of any monolithic operational amplifier, the OP-80 is ideal for use in applications measuring signals from a very high impedance or a very low current source. Operating from a single +5V supply, common-mode input voltages extend to ground with the output swinging to within 200µV of ground. It is a true "single-supply operational amplifier."

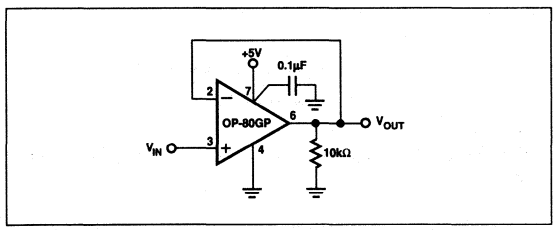


FIGURE 1: *Unity Voltage Gain Follower, Single +5V Supply*

An example of this single-supply operation is illustrated in Figure 1. The OP-80, configured as a unity gain voltage-follower with a single +5V supply, can be operated down to ground, as shown by the 10kHz sinewave output in Figure 2. Typical of CMOS op amp operation, the output stage of the OP-80 requires a output load resistance of 1MΩ or less.

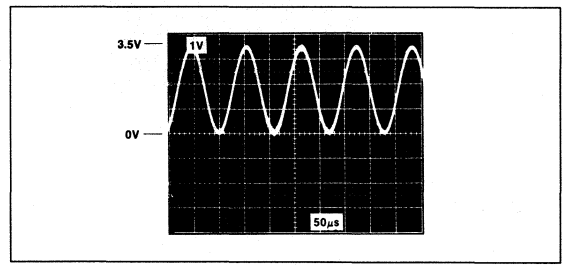


FIGURE 2: *Voltage Follower Response, 10kHz Sine Wave V_S = +5V, R_L = 10kΩ. Note that output extends to ground.*

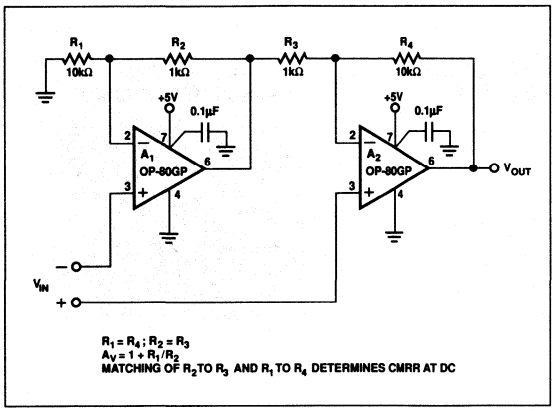


FIGURE 3: *True Single Supply Instrumentation Amplifier*

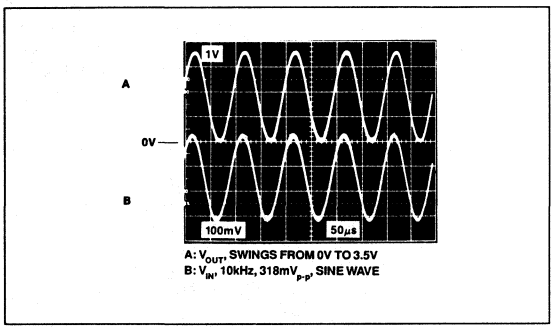


FIGURE 4: *Sine Wave Response*

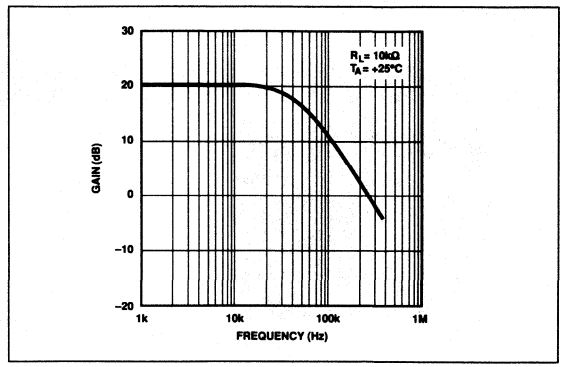


FIGURE 5: *Instrumentation Amplifier Frequency Response*

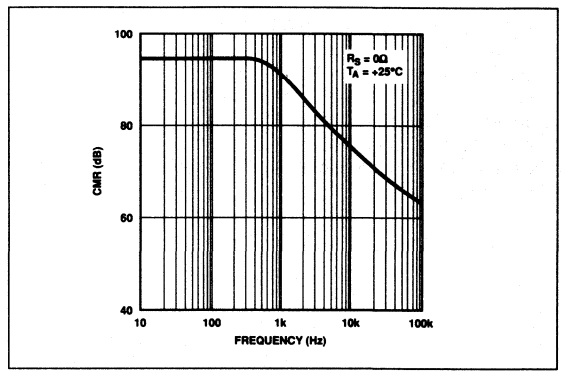


FIGURE 6: *Instrumentation Amplifier Common-Mode Rejection*

A TRUE SINGLE SUPPLY INSTRUMENTATION AMPLIFIER

The circuit in Figure 3 shows an instrumentation amplifier operated from a single +5V supply. This amplifier is quite useful for battery-powered instrument applications since it consumes a supply current of less than 400µA, and the output signal can swing down to ground level, as illustrated in Figure 4.

Although this amplifier topology is not symmetrically balanced, as in a three op-amp instrumentation amplifier, a common-mode rejection of 70dB is still maintained over a signal bandwidth of 20kHz as shown in Figures 5 and 6. Finite open-loop gain of A_1 causes feedthrough of the common-mode input which may be improved by trimming R_1.

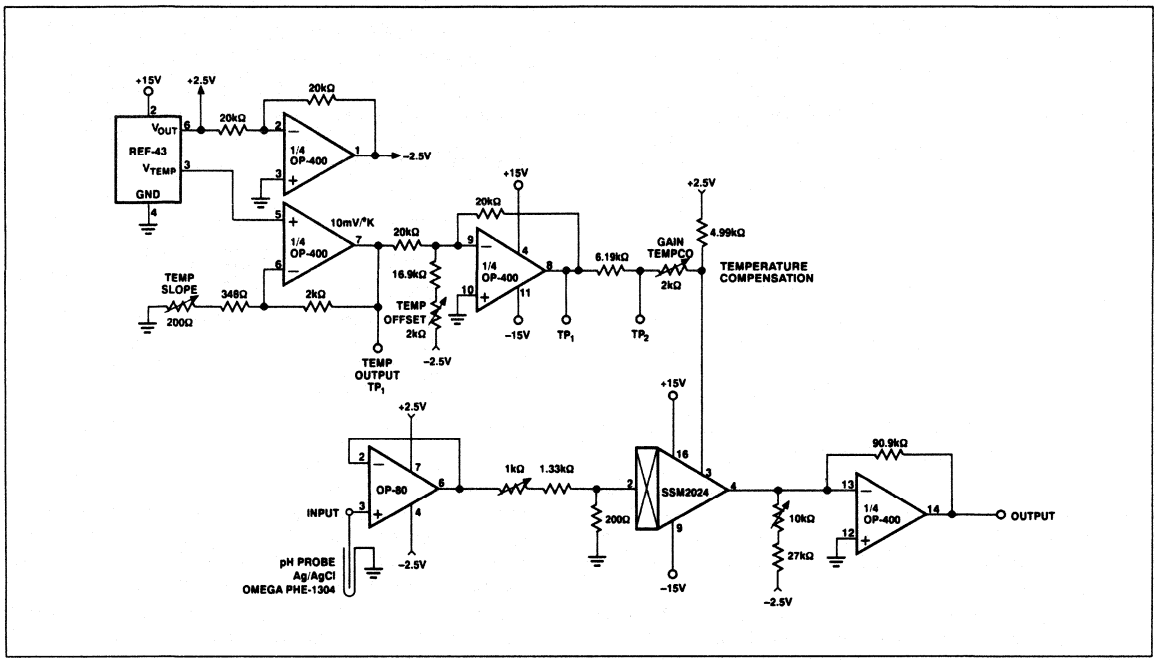


FIGURE 7: *A Complete, Temperature-Compensated pH Meter Design*

IDEAL FOR A pH METER

Since the OP-80 has an extremely high input impedance, it is ideal for pH/Ion sensitive electrode applications. Figure 7 illustrates an OP-80 used to buffer the extremely high impedance of a pH probe. The meter includes a temperature compensation circuit for the probe.

pH Meter Calibration Procedure

1. With T_A = +25°C adjust temperature slope for 2.98V temperature output.
2. Adjust temperature offset @ 25°C for –0.25V at TP_1.
3. Short TP_2 to ground.
4. Apply 0V to input (with pH probe disconnected).
5. Adjust offset for 7V output.
6. Apply +271mV to input; adjust gain trim for 2V output.
7. For improved accuracy, repeat steps 4, 5 and 6 as these adjustments are interactive.
8. Remove ground short from TP_2.
9. With T_A = +25°C, apply +295.6mV to input; adjust gain tempco for 2V output. For highest accuracy, use a buffer solution at a known pH and temperature and set gain tempco for proper output. Remember, to properly set the temperature calibration, the REF-43 must be placed in thermal contact with the solution under test.

The output voltage of the pH probe is linearly dependent on the pH of the sample solution and the sample temperature. A current-controlled amplifier, the SSM2024, is driven by a temperature dependent signal to account for the change in the pH probe's output voltage due to sample temperature variations.

After the pH meter is calibrated, it will have an output of 1V/pH from 2≤ pH ≤ 12 and is accurate to 0.01pH at 25°C and 0.05pH from 0°C to 70°C.

The REF-43's V_{TEMP} output provides an output voltage proportional to a temperature, typically 1.9mV/°C. This temperature dependent signal is conditioned and used to provide the correction signal to the current controlled amplifier.

GUARDING AND SHIELDING

To maintain the extremely high input impedances of the OP-80, care must be taken in circuit board layout and manufacturing. Board surfaces must be kept scrupulously clean and free of moisture. Conformal coating is recommended to provide a humidity barrier. Even a clean PC board can have 100pA of leakage currents between adjacent traces where a potential difference is present, so that guard rings should be used around the inputs. Guard traces should be driven at a voltage equal to or close to that of the inputs, so that leakage currents are kept at a minimum. In noninverting applications, the guard ring should be connected to the common-mode voltage at the inverting input (pin 2).

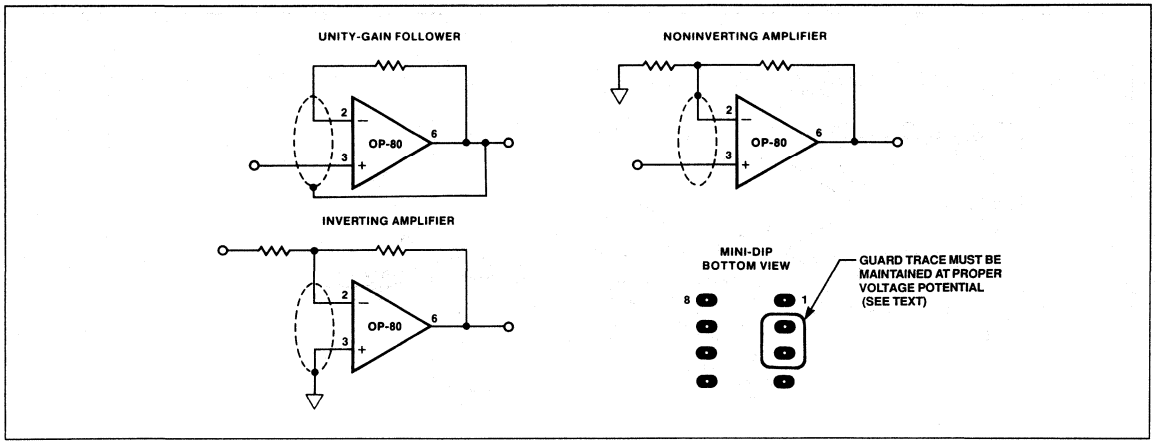


FIGURE 8: *Guard Ring Layout and Connections*

When the OP-80 is operated in the inverting mode, as in Figure 9, the signal traces should have grounded guard traces on both sides of the PC board since both inputs remain at ground voltage potential.

High impedance circuitry is extremely susceptible to RF pickup, line-frequency hum, and radiated noise from switching power-supplies. Enclosing sensitive analog sections within grounded shields is generally necessary to prevent excessive noise pickup. Twisted-pair cable will aid in rejection of line-frequency hum.

The OP-80's AC characteristics are highly stable over a wide range of operating conditions. Due to the extemely high input impedance, the OP-80 can be used with large source impedances, such as I-V converter applications. Input capacitance, with high source impedances, can substantially degrade signal bandwidth and stability margins. Accordingly, guarding the input lines will not only reduce parasitic leakage, but stray capacitance at the input node will also be minimized.

To cancel the effect of the input capacitance, the pole created must be neutralized by a zero that is located at the same frequency. To introduce this zero, place a capacitor, C_F, around the feedback resistor with a value such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_F}$$

or $R_1 C_{IN} \leq R_2 C_F$.

R_1 is modelled as a Thevenin equivalent impedance for I-V converter applications.

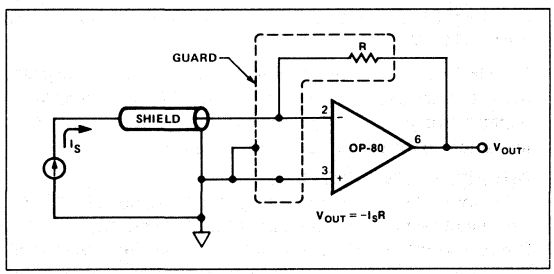


FIGURE 9: *Current-to-Voltage Converter*

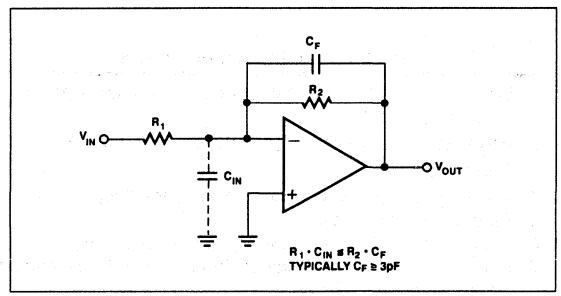


FIGURE 10: *Cancelling the Effect of Input Capacitance*

ANALOG DEVICES

Precision Low-Voltage Micropower Operational Amplifier

OP-90

FEATURES

- **Single/Dual Supply Operation ..... +1.6V to +36V**
  +0.8V to ±18V
- **True Single-Supply Operation; Input and Output Voltage Ranges Include Ground**
- **Low Supply Current ..... 20μA Max**
- **High Output Drive ..... 5mA Min**
- **Low Input Offset Voltage ..... 150μV Max**
- **High Open-Loop Gain ..... 700V/mV Min**
- **Outstanding PSRR ..... 5.6μV/V Max**
- **Standard 741 Pinout with Nulling to V–**
- **Available in Die Form**

GENERAL DESCRIPTION

The OP-90 is a high performance micropower op amp that operates from a single supply of +1.6V to +36V or from dual supplies of ±0.8 to ±18V. Input voltage range includes the negative rail allowing the OP-90 to accommodate input signals down to ground in single supply operation. The OP-90's output swing also includes ground when operating from a single supply, enabling "zero-in, zero-out" operation.

The OP-90 draws less than 20μA of quiescent supply current, while able to deliver over 5mA of output current to a load. Input offset voltage is below 150μV eliminating the need for external nulling. Gain exceeds 700,000 and common-mode rejection is better than 100dB. The power supply-rejection ratio of under 5.6μV/V minimizes offset voltage changes experienced in battery powered systems.

The low offset voltage and high gain offered by the OP-90 bring precision performance to micropower applications. The minimal voltage and current requirements of the OP-90 suit it for battery and solar powered applications, such as portable instruments, remote sensors, and satellites.

ORDERING INFORMATION †

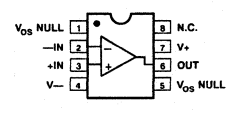
T_A = 25°C V_{OS} MAX (mV)	PACKAGE CERDIP 8-PIN	PACKAGE PLASTIC 8-PIN	PACKAGE LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
150	OP90AZ*	–	OP90ARC/883	MIL
150	OP90EZ	–	–	IND
250	OP90FZ	–	–	IND
450	–	OP90GP	–	XIND
450	–	OP90GS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

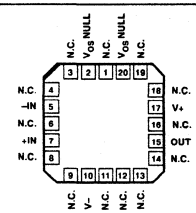
PIN CONNECTIONS



8-PIN HERMETIC DIP (Z-Suffix)

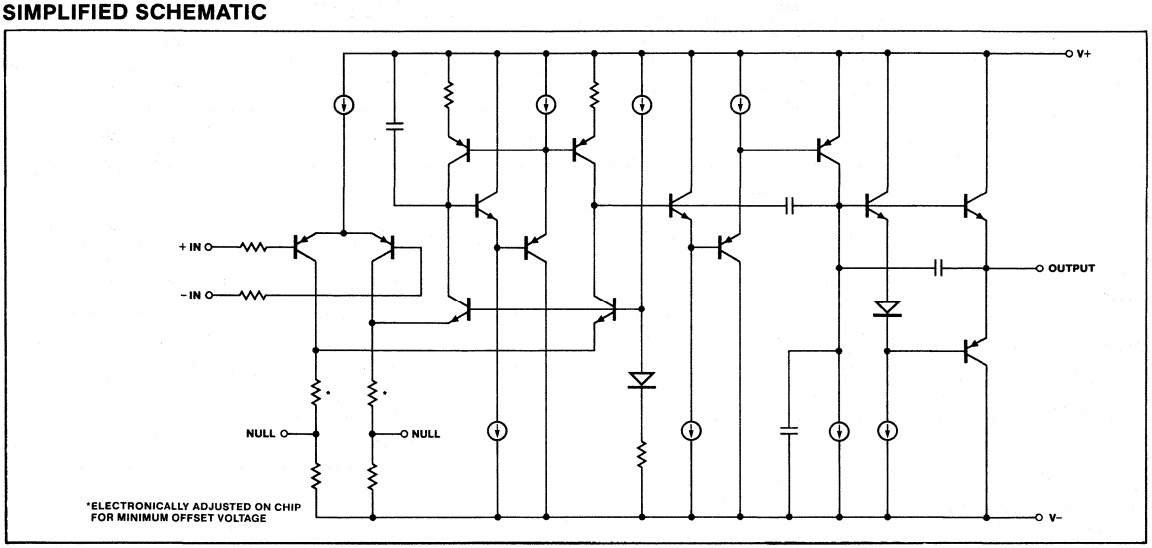
8-PIN EPOXY MINI-DIP (P-Suffix)

8-PIN SO (S-Suffix)



OP-90 ARC/883 LCC (RC-Suffix)

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Differential Input Voltage ..... [(V–) – 20V] to [(V+) + 20V]
Common-Mode Input Voltage
..... [(V–) – 20V] to [(V+) + 20V]
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range
Z Package ..... –65°C to +150°C
P Package ..... –65°C to +150°C
Operating Temperature Range
OP-90A ..... –55°C to +125°C
OP-90E, OP-90F ..... –25°C to +85°C
OP-90G ..... –40°C to +85°C
Junction Temperature (T_J) ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC (RC)	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm1.5V$ to $\pm15V$, $T_A = +25°C$, unless otherwise noted.

			OP-90A/E			OP-90F			OP-90G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	50	150	—	75	250	—	125	450	μV
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	0.4	3	—	0.4	5	—	0.4	5	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	4.0	15	—	4.0	20	—	4.0	25	nA
Large Signal Voltage Gain	A_{VO}	$V_S = \pm15V$, $V_O = \pm10V$										
		$R_L = 100k\Omega$	700	1200	—	500	1000	—	400	800	—	V/mV
		$R_L = 10k\Omega$	350	600	—	250	500	—	200	400	—	
		$R_L = 2k\Omega$	125	250	—	100	200	—	100	200	—	
		V+ = 5V, V– = 0V, $1V < V_O < 4V$										
		$R_L = 100k\Omega$	200	400	—	125	300	—	100	250	—	
		$R_L = 10k\Omega$	100	180	—	75	140	—	70	140	—	
Input Voltage Range	IVR	V+ = 5V, V– = 0V	0/4	—	—	0/4	—	—	0/4	—	—	V
		$V_S = \pm15V$ (Note 2)	−15/13.5	—	—	−15/13.5	—	—	−15/13.5	—	—	
Output Voltage Swing	V_O	$V_S = \pm15V$										
		$R_L = 10k\Omega$	±14	±14.2	—	±14	±14.2	—	±14	±14.2	—	V
		$R_L = 2k\Omega$	±11	±12	—	±11	±12	—	±11	±12	—	
	V_{OH}	V+ = 5V, V– = 0V										V
		$R_L = 2k\Omega$	4.0	4.2	—	4.0	4.2	—	4.0	4.2	—	
	V_{OL}	V+ = 5V, V– = 0V										μV
		$R_L = 10k\Omega$	—	100	500	—	100	500	—	100	500	
Common Mode Rejection	CMR	V+ = 5V, V– = 0V, $0V < V_{CM} < 4V$	90	110	—	80	100	—	80	100	—	dB
		$V_S = \pm15V$, $-15V < V_{CM} < 13.5V$	100	130	—	90	120	—	90	120	—	
Power Supply Rejection Ratio	PSRR		—	1.0	5.6	—	1.0	5.6	—	3.2	10	μV/V
Slew Rate	SR	$V_S = \pm15V$	5	12	—	5	12	—	5	12	—	V/ms
Supply Current	I_{SY}	$V_S = \pm1.5V$	—	9	15	—	9	15	—	9	15	μA
		$V_S = \pm15V$	—	14	20	—	14	20	—	14	20	
Capacitive Load Stability		$A_V = +1$, No Oscillations (Note 1)	250	650	—	250	650	—	250	650	—	pF
Input Noise Voltage	e_{np-p}	$f_O = 0.1Hz$ to 10Hz, $V_S = \pm15V$	—	3	—	—	3	—	—	3	—	μV_{p-p}
Input Resistance Differential Mode	R_{IN}	$V_S = \pm15V$	—	30	—	—	30	—	—	30	—	MΩ
Input Resistance Common Mode	R_{INCM}	$V_S = \pm15V$	—	20	—	—	20	—	—	20	—	GΩ

NOTES:
1. Guaranteed but not 100% tested.
2. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5V$ to $\pm 15V$, $-55°C \leq T_A \leq 125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-90A MIN	OP-90A TYP	OP-90A MAX	UNITS
Input Offset Voltage	V_{OS}		—	80	400	μV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.3	2.5	μV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	1.5	5	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	4.0	20	nA
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_O = \pm 10V$				V/mV
		$R_L = 100k\Omega$	225	400	—	
		$R_L = 10k\Omega$	125	240	—	
		$R_L = 2k\Omega$	50	110	—	
		V+ = 5V, V− = 0V, $1V < V_O < 4V$				
		$R_L = 100k\Omega$	100	200	—	
		$R_L = 10k\Omega$	50	110	—	
Input Voltage Range	IVR	V+ = 5V, V− = 0V (Note 1)	0/3.5	—	—	V
		$V_S = \pm 15V$	−15/13.5	—	—	
Output Voltage Swing	V_O	$V_S = \pm 15V$				V
		$R_L = 10k\Omega$	±13.5	±13.7	—	
		$R_L = 2k\Omega$	±10.5	±11.5	—	
	V_{OH}	V+ = 5V, V− = 0V				V
		$R_L = 2k\Omega$	3.9	4.1	—	
	V_{OL}	V+ = 5V, V− = 0V				μV
		$R_L = 10k\Omega$	—	100	500	
Common Mode Rejection	CMR	V+ = 5V, V− = 0V, $0V < V_{CM} < 3.5V$	85	105	—	dB
		$V_S = \pm 15V$, $-15V < V_{CM} < 13.5V$	95	115	—	
Power Supply Rejection Ratio	PSRR		—	3.2	10	μV/V
Supply Current	I_{SY}	$V_S = \pm 1.5V$	—	15	25	μA
		$V_S = \pm 15V$	—	19	30	

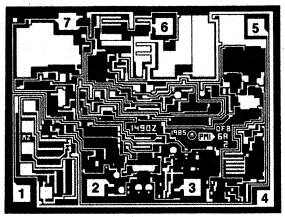
NOTE:
1. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at V_S = ±1.5V to ±15V, −25°C ≤ T_A ≤ +85°C for OP-90E/F, −40°C ≤ T_A ≤ +85°C for OP-90G, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-90E MIN	OP-90E TYP	OP-90E MAX	OP-90F MIN	OP-90F TYP	OP-90F MAX	OP-90G MIN	OP-90G TYP	OP-90G MAX	UNITS
Input Offset Voltage	V_{OS}		—	70	270	—	110	550	—	180	675	µV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.3	2	—	0.6	5	—	1.2	5	µV/°C
Input Offset Current	I_{OS}	V_{CM} = 0V	—	0.8	3	—	1.0	5	—	1.3	7	nA
Input Bias Current	I_B	V_{CM} = 0V	—	4.0	15	—	4.0	20	—	4.0	25	nA
Large Signal Voltage Gain	A_{VO}	V_S = ±15V, V_O = ±10V										V/mV
		R_L = 100kΩ	500	800	—	350	700	—	300	600	—	
		R_L = 10kΩ	250	400	—	175	350	—	150	250	—	
		R_L = 2kΩ	100	200	—	75	150	—	75	125	—	
		V+ = 5V, V− = 0V, 1V < V_O < 4V										
		R_L = 100kΩ	150	280	—	100	220	—	80	160	—	
		R_L = 10kΩ	75	140	—	50	110	—	40	90	—	
Input Voltage Range	IVR	V+ = 5V, V− = 0V	0/3.5	—	—	0/3.5	—	—	0/3.5	—	—	V
		V_S = ±15V (Note 1)	−15/13.5	—	—	−15/13.5	—	—	−15/13.5	—	—	
Output Voltage Swing	V_O	V_S = ±15V										V
		R_L = 10kΩ	±13.5	±14	—	±13.5	±14	—	±13.5	±14	—	
		R_L = 2kΩ	±10.5	±11.8	—	±10.5	±11.8	—	±10.5	±11.8	—	
	V_{OH}	V+ = 5V, V− = 0V										V
		R_L = 2kΩ	3.9	4.1	—	3.9	4.1	—	3.9	4.1	—	
	V_{OL}	V+ = 5V, V− = 0V										µV
		R_L = 10kΩ	—	100	500	—	100	500	—	100	500	
Common Mode Rejection	CMR	V+ = 5V, V− = 0V, 0V < V_{CM} < 3.5V	90	110	—	80	100	—	80	100	—	dB
		V_S = ±15V, −15V < V_{CM} < 13.5V	100	120	—	90	110	—	90	110	—	
Power Supply Rejection Ratio	PSRR		—	1.0	5.6	—	3.2	10	—	5.6	17.8	µV/V
Supply Current	I_{SY}	V_S = ±1.5V	—	13	25	—	13	25	—	12	25	µA
		V_S = ±15V	—	17	30	—	17	30	—	16	30	

NOTE:
1. Guaranteed by CMR test.

DICE CHARACTERISTICS



DIE SIZE 0.086 × 0.067 inch, 5762 sq. mils
(2.18 × 1.70mm, 3.71 sq. mm)

1. V_{OS} NULL
2. −IN
3. +IN
4. V−
5. V_{OS} NULL
6. OUT
7. V+

WAFER TEST LIMITS at $V_S = \pm 1.5V$ to $\pm 15V$, $T_A = 25°C$, unless otherwise noted.

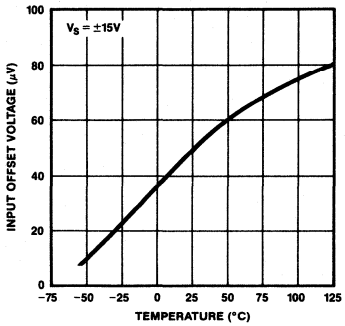
PARAMETER	SYMBOL	CONDITIONS	OP-90GBC LIMIT	UNITS
Input Offset Voltage	V_{OS}		250	μV MAX
Input Offset Current	I_{OS}	$V_{CM} = 0V$	5	nA MAX
Input Bias Current	I_B	$V_{CM} = 0V$	20	nA MAX
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_O = \pm 10V$ $R_L = 100k\Omega$ $R_L = 10k\Omega$	 500 250	V/mV MIN
		V+ = 5V, V− = 0V, $1V < V_O < 4V$ $R_L = 100k\Omega$	 125	V/mV MIN
Input Voltage Range	IVR	V+ = 5V, V− = 0V (Note 1) $V_S = \pm 15V$	0/4 −15/13.5	V MIN
Output Voltage Swing	V_O	$V_S = \pm 15V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	 ±14 ±11	V MIN
	V_{OH}	V+ = 5V, V− = 0V $R_L = 2k\Omega$	 4.0	V MIN
	V_{OL}	V+ = 5V, V− = 0V $R_L = 10k\Omega$	 500	μV MAX
Common Mode Rejection	CMR	V+ = 5V, V− = 0V, $0V < V_{CM} < 4V$ $V_S = \pm 15V$, $-15V < V_{CM} < 13.5V$	80 90	dB MIN
Power Supply Rejection Ratio	PSRR		10	μV/V MAX
Supply Current	I_{SY}	$V_S = \pm 15V$	20	μA MAX

NOTES:
1. Guaranteed by CMR test.

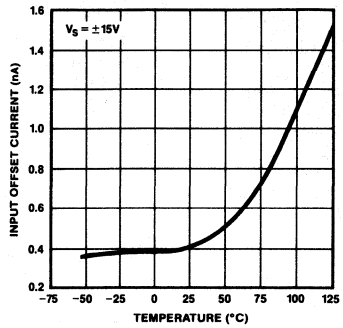
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

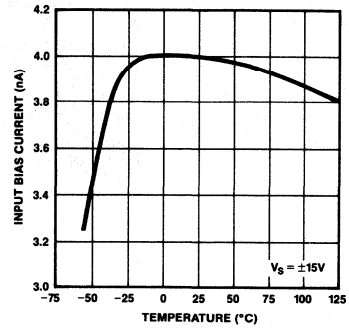
INPUT OFFSET VOLTAGE vs TEMPERATURE



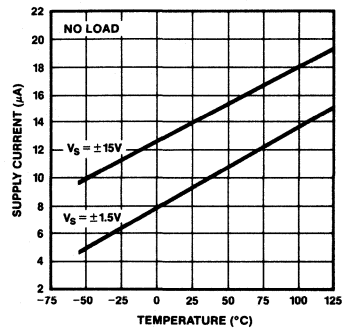
INPUT OFFSET CURRENT vs TEMPERATURE



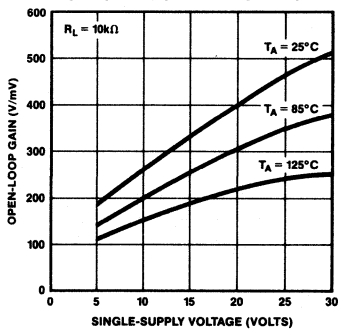
INPUT BIAS CURRENT vs TEMPERATURE



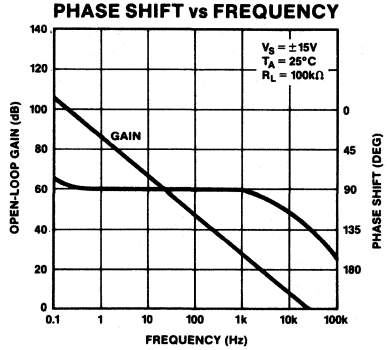
SUPPLY CURRENT vs TEMPERATURE



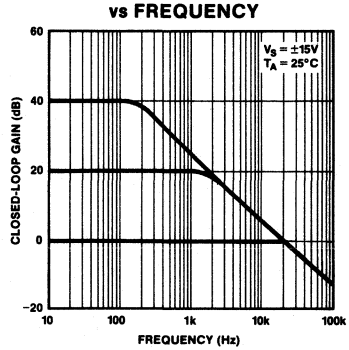
OPEN-LOOP GAIN vs SINGLE-SUPPLY VOLTAGE



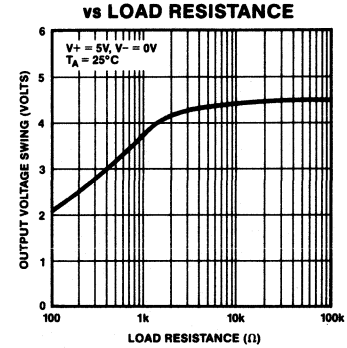
OPEN-LOOP GAIN AND PHASE SHIFT vs FREQUENCY



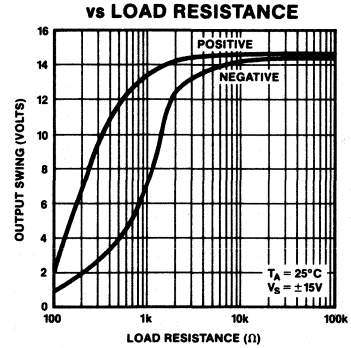
CLOSED-LOOP GAIN vs FREQUENCY



OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

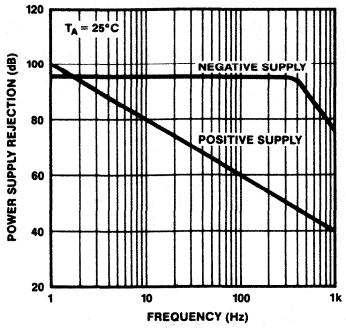


OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

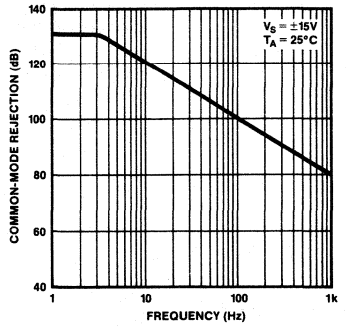


TYPICAL PERFORMANCE CHARACTERISTICS

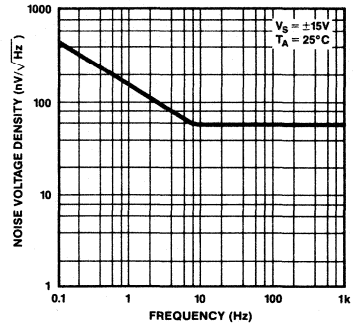
POWER SUPPLY REJECTION vs FREQUENCY



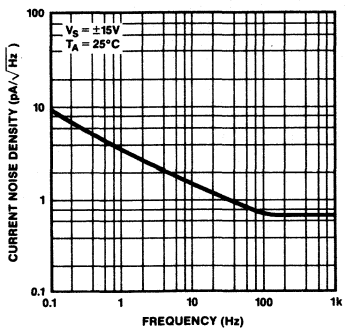
COMMON-MODE REJECTION vs FREQUENCY



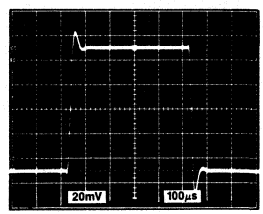
NOISE VOLTAGE DENSITY vs FREQUENCY



CURRENT NOISE DENSITY vs FREQUENCY

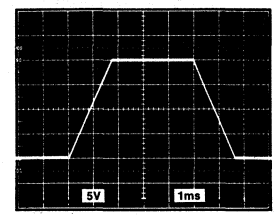


SMALL-SIGNAL TRANSIENT RESPONSE



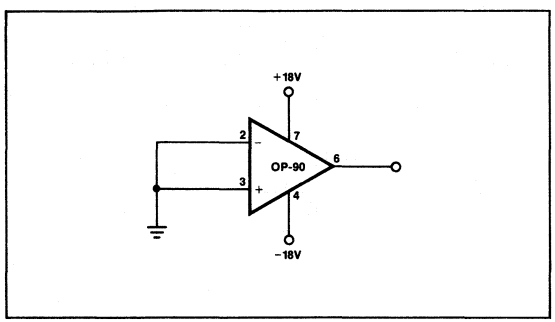
T_A = 25°C
V_S = ±15V
A_V = +1
R_L = 10kΩ
C_L = 500pF

LARGE-SIGNAL TRANSIENT RESPONSE



T_A = 25°C
V_S = ±15V
A_V = +1
R_L = 10kΩ
C_L = 500pF

BURN-IN CIRCUIT



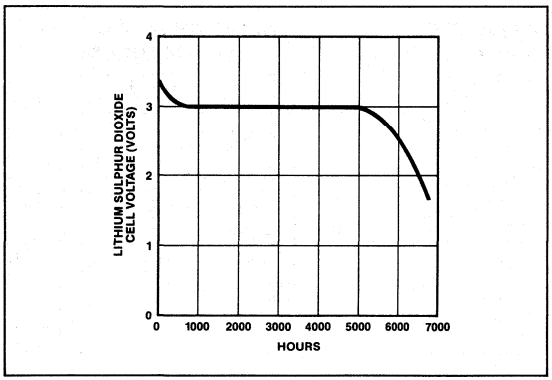
APPLICATIONS INFORMATION

BATTERY-POWERED APPLICATIONS

The OP-90 can be operated on a minimum supply voltage of +1.6V, or with dual supplies ±0.8V, and draws only 14µA of supply current. In many battery-powered circuits, the OP-90 can be continuously operated for thousands of hours before requiring battery replacement, reducing equipment down-time and operating cost.

High-performance portable equipment and instruments frequently use lithium cells because of their long shelf-life, light weight, and high energy density relative to older primary cells. Most lithium cells have a nominal output voltage of 3V and are noted for a flat discharge characteristic. The low supply voltage requirement of the OP-90, combined with the flat discharge characteristic of the lithium cell, indicates that the OP-90 can be operated over the entire useful life of the cell. Figure 1 shows the typical discharge characteristic of a 1Ah lithium cell powering an OP-90 which, in turn, is driving full output swing into a 100kΩ load.

FIGURE 1: Lithium Sulphur Dioxide Cell Discharge Characteristic With OP-90 and 100kΩ Load



INPUT VOLTAGE PROTECTION

The OP-90 uses a PNP input stage with protection resistors in series with the inverting and noninverting inputs. The high breakdown of the PNP transistors coupled with the protection resistors provides a large amount of input protection, allowing the inputs to be taken 20V beyond either supply without damaging the amplifier.

OFFSET NULLING

The offset null circuit of Figure 2 provides 6mV of offset adjustment range. A 100kΩ resistor placed in series with the wiper of the offset null potentiometer, as shown in Figure 3,

FIGURE 2: Offset Nulling Circuit

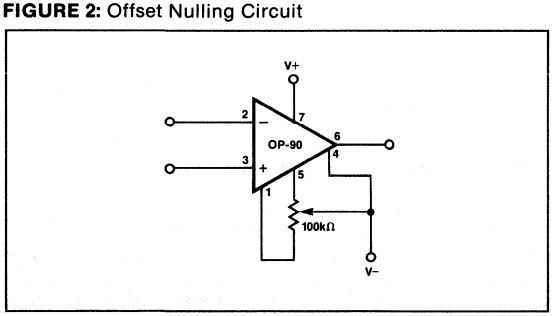
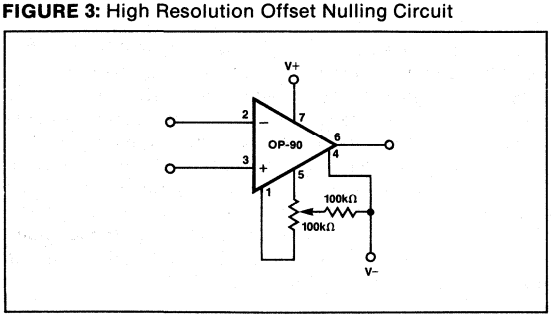


FIGURE 3: High Resolution Offset Nulling Circuit



reduces the offset adjustment range to 400μV and is recommended for applications requiring high null resolution. Offset nulling does not affect TCV_{OS} performance.

SINGLE-SUPPLY OUTPUT VOLTAGE RANGE

In single-supply operation the OP-90's input and output ranges include ground. This allows true "zero-in, zero-out" operation. The output stage provides an active pull-down to around 0.8V above ground. Below this level, a load resistance of up to 1MΩ to ground is required to pull the output down to zero.

In the region from ground to 0.8V the OP-90 has voltage gain equal to the data sheet specification. Output current source capability is maintained over the entire voltage range including ground.

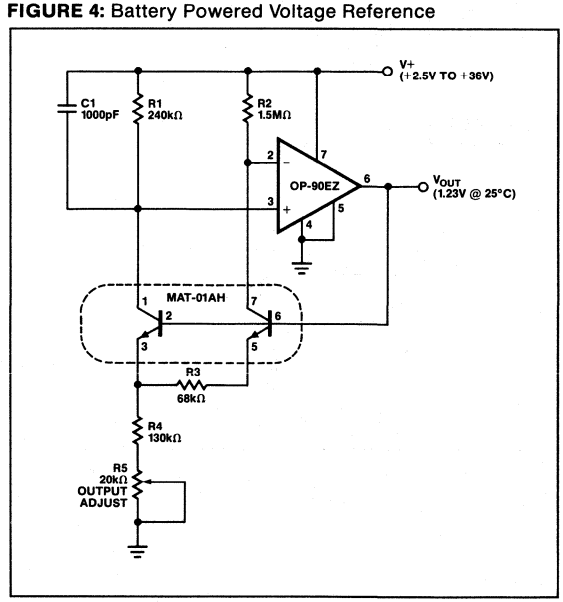
APPLICATIONS

BATTERY-POWERED VOLTAGE REFERENCE

The circuit of Figure 4 is a battery-powered voltage reference that draws only 17μA of supply current. At this level, two AA cells can power this reference over 18 months. At an output voltage of 1.23V @ 25°C, drift of the reference is only 5.5μV/°C over the industrial temperature range. Load regulation is 85μV/mA with line regulation at 120μV/V.

Design of the reference is based on the bandgap technique. Scaling of resistors R1 and R2 produces unequal currents in Q1 and Q2. The resulting V_{BE} mismatch creates a temperature-proportional voltage across R3 which, in turn, produces a larger temperature-proportional voltage across R4 and R5. This voltage appears at the output added to the V_{BE} of Q1, which has an opposite temperature coefficient. Adjusting the

FIGURE 4: Battery Powered Voltage Reference



output to 1.23V at 25°C produces minimum drift over temperature. Bandgap references can have start-up problems. With no current in R1 and R2, the OP-90 is beyond its positive input range limit and has an undefined ouput state. Shorting Pin 5 (an offset adjust pin) to ground forces the output high under these conditions and insures reliable start-up without significantly degrading the OP-90's offset drift.

SINGLE OP AMP FULL-WAVE RECTIFIER

Figure 5 shows a full-wave rectifier circuit that provides the absolute value of input signals up to ±2.5V even though operated from a single 5V supply. For negative inputs, the amplifier acts as an unity gain inverter. Positive signals force the op amp output to ground. The 1N914 diode becomes reversed-biased and the signal passes through R1 and R2 to the output. Since output impedance is dependent on input polarity, load impedances cause an asymmetric output. For constant load impedances, this can be corrected by reducing R2. Varying or heavy loads can be buffered by a second OP-90. Figure 6 shows the output of the full-wave rectifier with a $4V_{p-p}$, 10Hz input signal.

FIGURE 5: Single Op-Amp Full Wave Rectifier

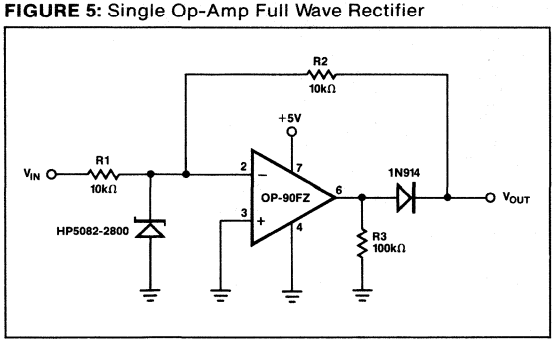
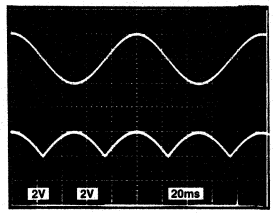


FIGURE 6: Output of Full-Wave Rectifier With $4V_{p-p}$, 10Hz Input



TWO WIRE 4-20mA CURRENT TRANSMITTER

The current transmitter of Figure 7 provides an output of 4mA to 20mA that is linearly proportional to the input voltage. Linearity of the transmitter exceeds 0.004% and line rejection is 0.0005%/volt.

Biasing for the current transmitter is provided by the REF-02EZ. The OP-90EZ regulates the output current to satisfy the current summation at the noninverting node:

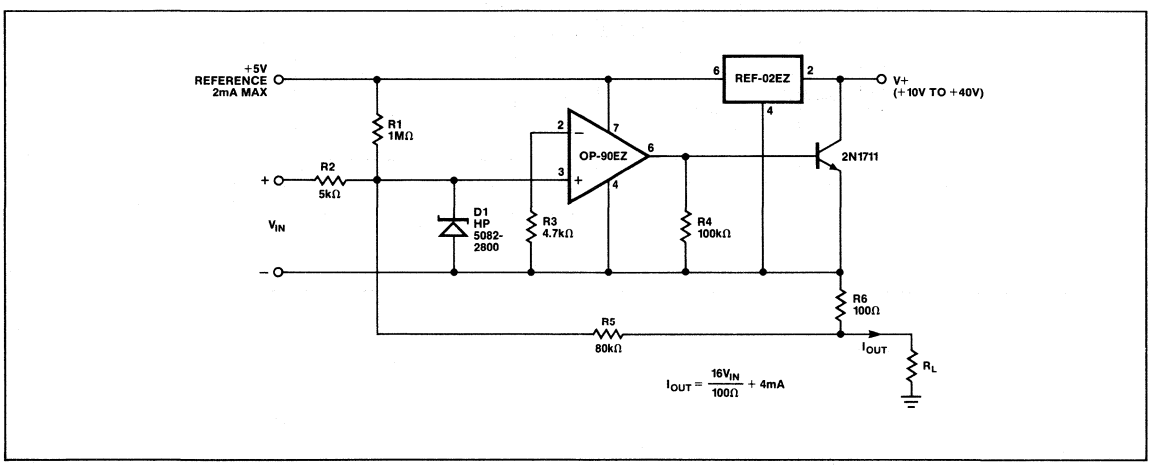
$$I_{OUT} = \frac{1}{R6}\left(\frac{V_{IN}\,R5}{R2} + \frac{5V\,R5}{R1}\right)$$

For the values shown in Figure 7,

$$I_{OUT} = \left(\frac{16}{100\Omega}\right)V_{IN} + 4mA$$

giving a full-scale output of 20mA with a 100mV input. Adjustment of R2 will provide an offset trim and adjustment of R1 will provide a gain trim. These trims do not interact since the noninverting input of the OP-90 is at virtual ground. The Schottky diode, D1, prevents input voltage spikes from pull-

FIGURE 7: Two Wire 4-20mA Transmitter



ing the noninverting input more than 300mV below the inverting input. Without the diode, such spikes could cause phase reversal of the OP-90 and possible latch-up of the transmitter. Compliance of this circuit is from 10V to 40V. The voltage reference output can provide up to 2mA for transducer excitation.

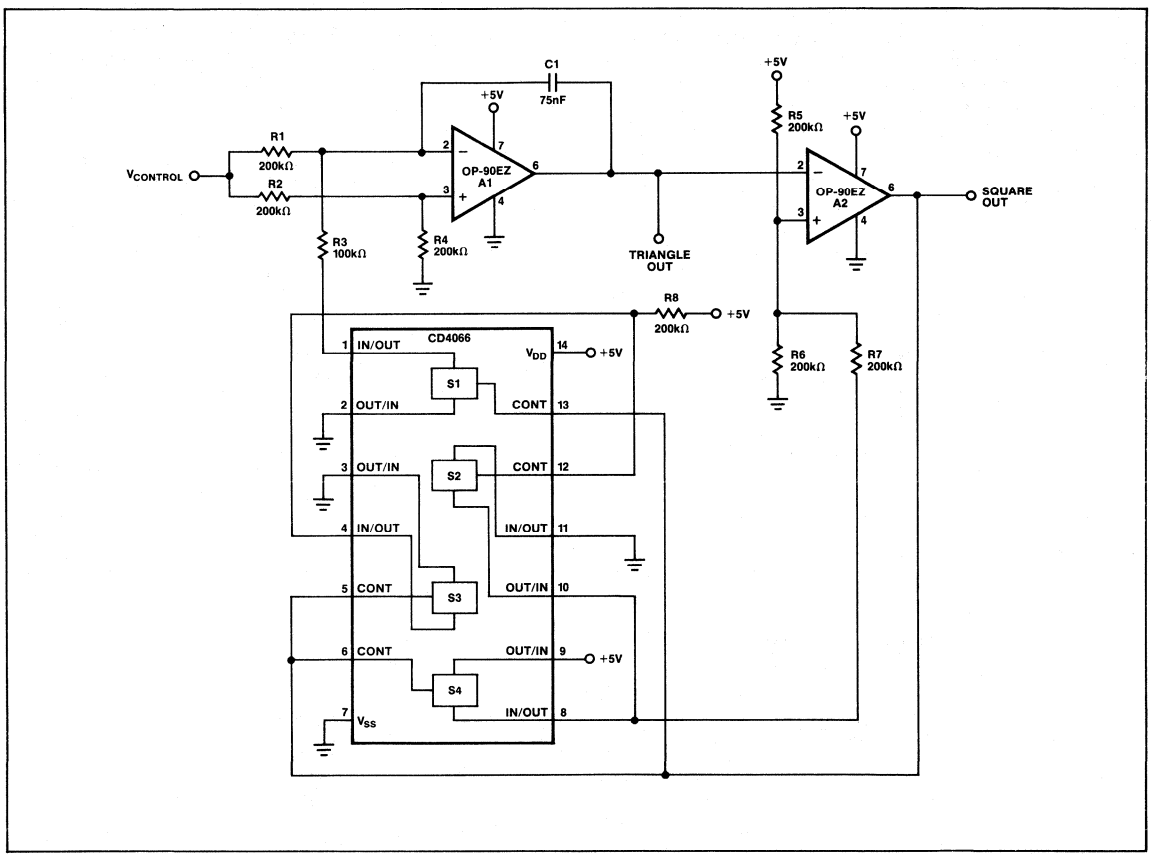
MICROPOWER VOLTAGE-CONTROLLED OSCILLATOR

Two OP-90s in combination with an inexpensive quad CMOS switch comprise the precision VCO of Figure 8. This circuit provides triangle and square wave outputs and draws only 50μA from a single 5V supply. A1 acts as an integrator; S1 switches the charging current symmetrically to yield positive and negative ramps. The integrator is bounded by A2 which acts as a Schmitt trigger with a precise hysteresis of 1.67 volts, set by resistors R5, R6, and R7, and associated CMOS switches. The resulting output of A1 is a triangle wave with upper and lower levels of 3.33 and 1.67 volts. The output of A2 is a square wave with almost rail-to-rail swing. With the components shown, frequency of operation is given by the equation:

$$f_{OUT} = V_{CONTROL}\ (\text{volts}) \times 10\text{Hz/V}$$

but this is easily changed by varying C1. The circuit operates well up to a few hundred hertz.

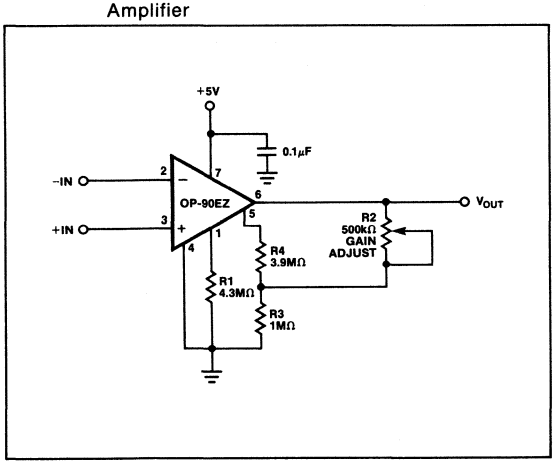
FIGURE 8: Micropower Voltage Controlled Oscillator



MICROPOWER SINGLE-SUPPLY INSTRUMENTATION AMPLIFIER

The simple instrumentation amplifier of Figure 9 provides over 110dB of common-mode rejection and draws only 15μA of supply current. Feedback is to the trim pins rather than to the inverting input. This enables a single amplifier to provide differential to single-ended conversion with excellent common-mode rejection. Distortion of the instrumentation amplifier is that of a differential pair, so the circuit is restricted to high gain applications. Nonlinearity is less than 0.1% for gains of 500 to 1000 over a 2.5V output range. Resistors R3 and R4 set the voltage gain and, with the values shown, yield a gain of 1000. Gain tempco of the instrumentation amplifier is only 50ppm/°C. Offset voltage is under 150μV with drift below 2μV/°C. The OP-90's input and output voltage ranges include the negative rail which allows the instrumentation amplfier to provide true "zero-in, zero-out" operation.

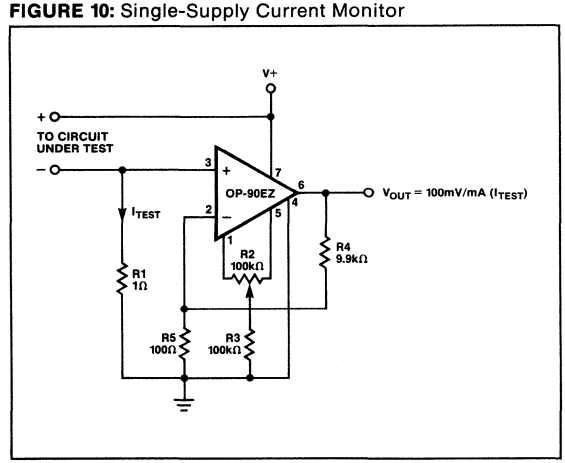
FIGURE 9: Micropower Single-Supply Instrumentation Amplifier



SINGLE-SUPPLY CURRENT MONITOR

Current monitoring essentially consists of amplifying the voltage drop across a resistor placed in series with the current to be measured. The difficulty is that only small voltage drops can be tolerated and with low precision op amps this greatly limits the overall resolution. The single-supply current monitor of Figure 10 has a resolution of 10μA and is capable of monitoring 30mA of current. This range can be adjusted by changing the current sense resistor R1. When measuring total system current, it may be necessary to include the supply current of the current monitor, which bypasses the current sense resistor, in the final result. This current can be measured and calibrated (together with the residual offset) by adjustment of the offset trim potentiometer, R2. This produces a deliberate offset that is temperature dependent. However, the supply current of the OP-90 is also proportional to temperature and the two effects tend to track. Current in R4 and R5, which also bypasses R1, can be accounted for by a gain trim.

FIGURE 10: Single-Supply Current Monitor



ANALOG DEVICES

Low-Power, High-Precision Operational Amplifier

OP-97

FEATURES

- **Low Supply Current ..... 600μA Max**
- **OP-07 Type Performance**
  - **Offset Voltage ..... 20μV Max**
  - **Offset Voltage Drift ..... 0.6μV/°C Max**
- **Very Low Bias Current**
  - **25°C ..... 100pA Max**
  - **–55°C to +125°C ..... 250pA Max**
- **High Common-Mode Rejection ..... 114dB Min**
- **Extended Industrial Temp. Range ..... –40°C to +85°C**
- **Available In Die Form**

ORDERING INFORMATION †

PACKAGE			OPERATING TEMPERATURE RANGE
TO-99	CERDIP	PLASTIC	
OP97AJ*	OP97AZ*	–	MIL
OP97EJ	OP97EZ	OP97EP	XIND
OP97FJ	OP97FZ	OP97FP	XIND
–	–	OP97FS††	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

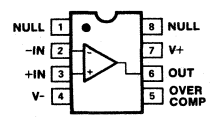
† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

The OP-97 is a low-power alternative to the industry-standard OP-07 precision amplifier. The OP-97 maintains the standards of performance set by the OP-07 while utilizing only 600μA supply current, less than 1/6 that of an OP-07. Offset voltage is an ultra-low 25μV, and drift over temperature is below 0.6μV/°C. External offset trimming is not required in the majority of circuits.

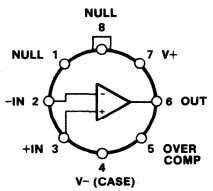
PIN CONNECTIONS



EPOXY MINI-DIP (P-Suffix)

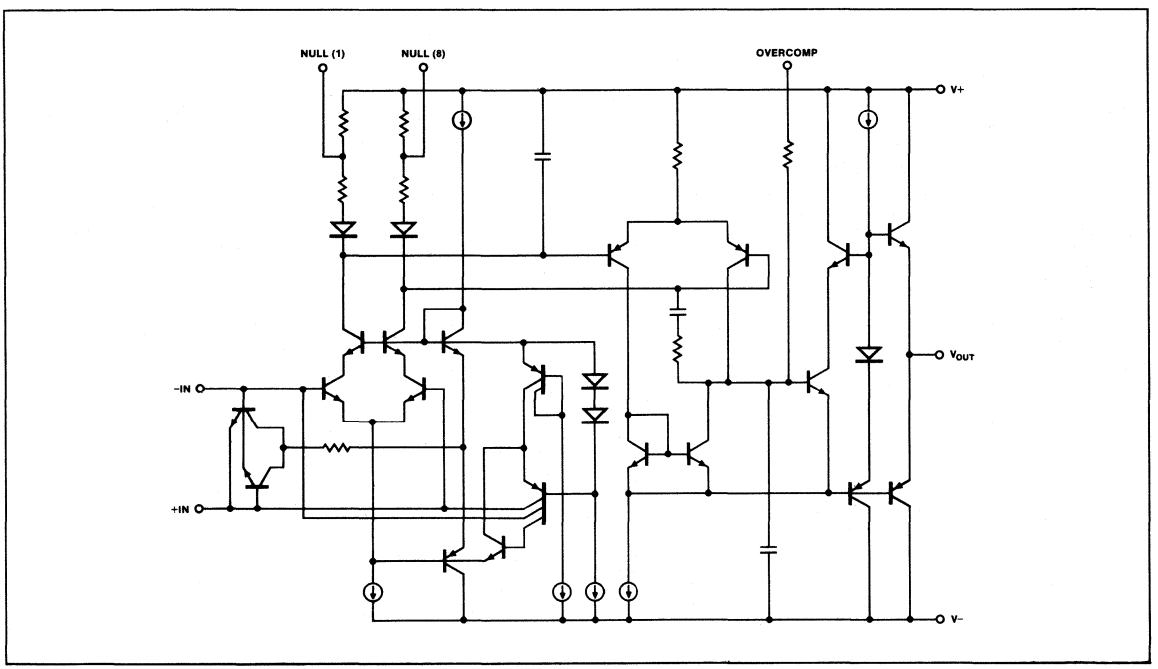
8-PIN CERDIP (Z-Suffix)

EPOXY SO†† (S-Suffix)



TO-99 (J-Suffix)

SIMPLIFIED SCHEMATIC



Improvements have been made over OP-07 specifications in several areas. Notable is bias current, which remains below 250pA over the full military temperature range. The OP-97 is ideal for use in precision long-term integrators or sample-and-hold circuits that must operate at elevated temperatures.

Common-mode rejection and power-supply rejection are also improved with the OP-97, at 114dB minimum over wider ranges of common-mode or supply voltage. Outstanding PSR, a supply range specified from ±2.25V to ±20V and the OP-97's minimal power requirements combine to make the OP-97 a preferred device for portable and battery-powered instruments.

The OP-97 conforms to the OP-07 pinout, with the null potentiometer connected between pins 1 and 8 with the wiper to V+. The OP-97 will upgrade circuit designs using 725, OP05, OP07, OP12, and 1012 type amplifiers. It may replace 741-type amplifiers in circuits without nulling or where the nulling circuitry has been removed.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±20V
Input Voltage (Note 3) ..... ±20V
Differential Input Voltage (Note 4) ..... ±1V
Differential Input Current (Note 4) ..... ±10mA
Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range
OP-97A (J, Z) ..... −55°C to +125°C
OP-97E, F (J, P, Z, S) ..... −40°C to +85°C
Storage Temperature Range ..... −65°C to +150°C
Junction Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP, and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.
3. For supply voltages less than ±20V, the absolute maximum input voltage is equal to the supply voltage.
4. The OP-97's inputs are protected by back-to-back diodes. Current-limiting resistors are not used in order to achieve low noise. Differential input voltages greater than 1V will cause excessive current to flow through the input protection diodes unless limiting resistance is used.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $V_{CM} = 0V$, $T_A = +25°C$, unless otherwise noted.

			OP-97A/E			OP-97F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	10	25	—	30	75	μV
Long-Term Offset Voltage Stability	ΔV_{OS}/Time		—	0.3	—	—	0.3	—	μV/Month
Input Offset Current	I_{OS}		—	30	100	—	30	150	pA
Input Bias Current	I_B		—	±30	±100	—	±30	±150	pA
Input Noise Voltage	$e_{n\ p\text{-}p}$	0.1Hz to 10Hz	—	0.5	—	—	0.5	—	$\mu V_{p\text{-}p}$
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 2) f_O = 1000Hz (Note 3)	— —	17 14	30 22	— —	17 14	30 22	nV/√Hz nV/√Hz
Input Noise Current Density	i_N	f_O = 10Hz	—	20	—	—	20	—	fA/√Hz
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm10V$; $R_L = 2k\Omega$	300	2000	—	200	2000	—	V/mV
Common-Mode Rejection	CMR	$V_{CM} = \pm13.5V$	114	132	—	110	132	—	dB
Power-Supply Rejection	PSR	$V_S = \pm2V$ to ±20V	114	132	—	110	132	—	dB
Input Voltage Range	IVR	(Note 1)	±13.5	±14.0	—	±13.5	±14.0	—	V
Output Voltage Swing	V_O	$R_L = 10k\Omega$	±13	±14	—	±13	±14	—	V
Slew Rate	SR		0.1	0.2	—	0.1	0.2	—	V/μs

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $V_{CM} = 0V$, $T_A = +25°C$, unless otherwise noted. (Continued.)

PARAMETER	SYMBOL	CONDITIONS	OP-97A/E MIN	OP-97A/E TYP	OP-97A/E MAX	OP-97F MIN	OP-97F TYP	OP-97F MAX	UNITS
Differential Input Resistance	R_{IN}	(Note 4)	30	—	—	30	—	—	MΩ
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$	0.4	0.9	—	0.4	0.9	—	MHz
Supply Current	I_{SY}		—	380	600	—	380	600	μA
Supply Voltage	V_S	Operating Range	±2	±15	±20	±2	±15	±20	V

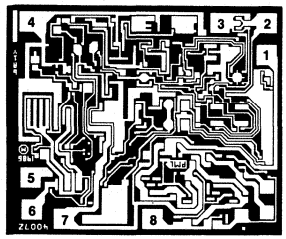
NOTES:
1. Guaranteed by CMR test.
2. 10Hz noise voltage density is sample tested. Devices 100% tested for noise are available on request.
3. Sample tested.
4. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $V_{CM} = 0V$, $-40°C \le T_A \le +85°C$ for the OP-97E/F and $-55°C \le T_A \le +125°C$ for the OP-97A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-97A/E MIN	OP-97A/E TYP	OP-97A/E MAX	OP-97F MIN	OP-97F TYP	OP-97F MAX	UNITS
Input Offset Voltage	V_{OS}		–	25	60	–	60	200	μV
Average Temperature Coefficient of V_{OS}	TCV_{OS}		–	0.2	0.6	–	0.3	2.0	μV/°C
		S-Package	–	–	–	–	0.3	–	
Input Offset Current	I_{OS}		–	60	250	–	80	750	pA
Average Temperature Coefficient of I_{OS}	TCI_{OS}		–	0.4	2.5	–	0.6	7.5	pA/°C
Input Bias Current	I_B		–	±60	±250	–	±80	±750	pA
Average Temperature Coefficient of I_B	TCI_B		–	0.4	2.5	–	0.6	7.5	pA/°C
Large-Signal Voltage Gain	A_{VO}	$V_O = +10V$; $R_L = 2k\Omega$	200	1000	–	150	1000	–	V/mV
Common-Mode Rejection	CMR	$V_{CM} = \pm13.5V$	108	128	–	108	128	–	dB
Power-Supply Rejection	PSR	$V_S = \pm2.5V$ to $\pm20V$	108	126	–	108	128	–	dB
Input Voltage Range	IVR	(Note 1)	±13.5	±14.0	–	±13.5	±14.0	–	V
Output Voltage Swing	V_O	$R_L = 10k\Omega$	±13	±14	–	±13	±14	–	V
Slew Rate	SR		0.05	0.15	–	0.05	0.15	–	V/μs
Supply Current	I_{SY}		–	400	800	–	400	800	μA
Supply Voltage	V_S	Operating Range	±2.5	±15	±20	±2.5	±15	±20	V

NOTES:
1. Guaranteed by CMR test.

DICE CHARACTERISTICS



DIE SIZE 0.063 × 0.074 inch, 4,662 sq. mils
(1.60 × 1.88 mm, 3.01 sq. mm)

1. NULL
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V−
5. OVERCOMPENSATION
6. OUTPUT
7. V+
8. NULL

WAFER TEST LIMITS at $V_S = \pm15V$, $V_{CM} = 0V$, $T_A = +25°C$, unless otherwise noted.

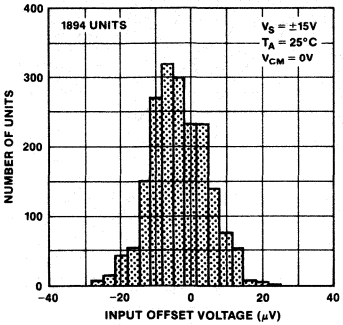
PARAMETER	SYMBOL	CONDITIONS	OP-97N LIMITS	UNITS
Input Offset Voltage	V_{OS}		250	μV MAX
Input Offset Current	I_{OS}		150	pA MAX
Input Bias Current	I_B		±150	pA MAX
Large-Signal Voltage Gain	A_{VO}	$V_{OUT} = \pm10V$, $R_L = 2k\Omega$	120	V/mV MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm13.5$	110	dB MIN
Power-Supply Rejection	PSR	$V_S = \pm2V$ to $\pm20V$	110	dB MIN
Input-Voltage Range	IVR	(Note 1)	±13.5	V MIN
Output Voltage Swing	V_O	$R_L = 10k\Omega$	±13	V MIN
Slew Rate	SR		0.1	V/μs MIN
Supply Current	I_{SY}	No Load	600	μA MAX

NOTES:
1. Guaranteed by CMR test.

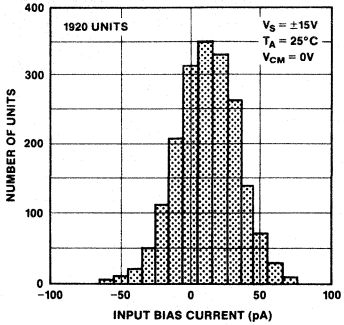
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

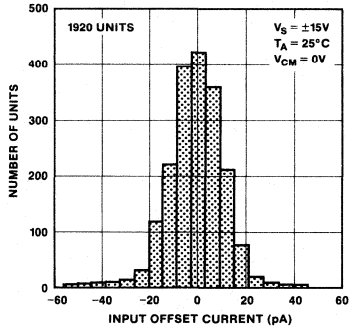
TYPICAL DISTRIBUTION OF INPUT OFFSET VOLTAGE



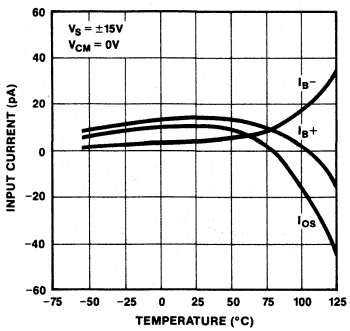
TYPICAL DISTRIBUTION OF INPUT BIAS CURRENT



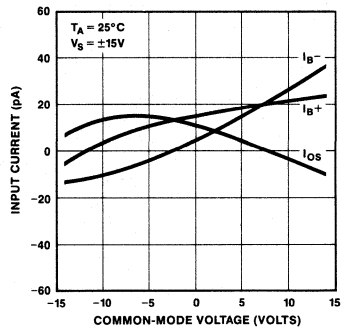
TYPICAL DISTRIBUTION OF INPUT OFFSET CURRENT



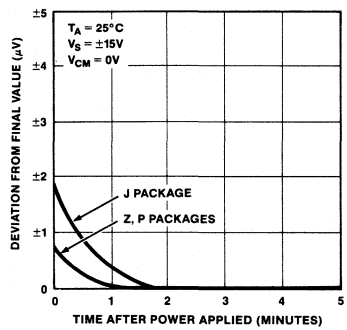
INPUT BIAS, OFFSET CURRENT vs TEMPERATURE



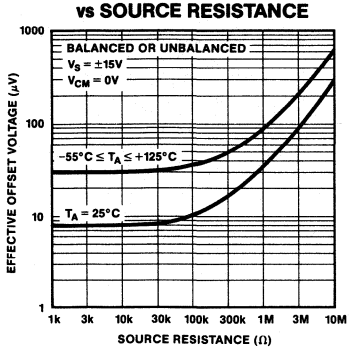
INPUT BIAS, OFFSET CURRENT vs COMMON-MODE VOLTAGE



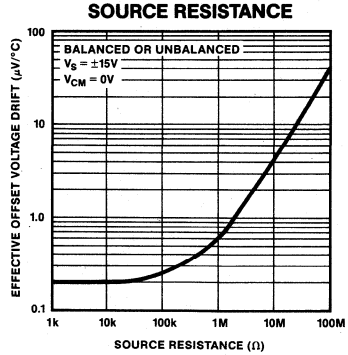
INPUT OFFSET VOLTAGE WARM-UP DRIFT



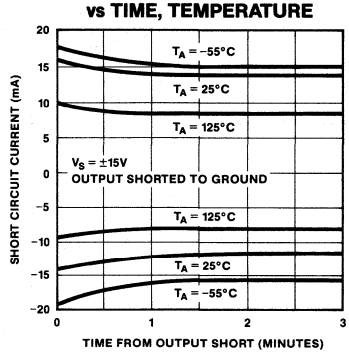
EFFECTIVE OFFSET VOLTAGE vs SOURCE RESISTANCE



EFFECTIVE TCV_{OS} vs SOURCE RESISTANCE

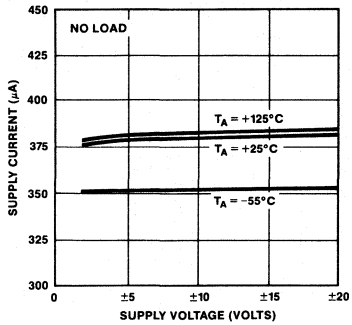


SHORT CIRCUIT CURRENT vs TIME, TEMPERATURE

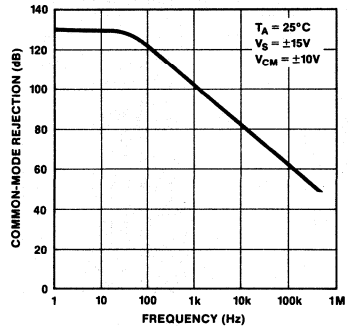


TYPICAL PERFORMANCE CHARACTERISTICS

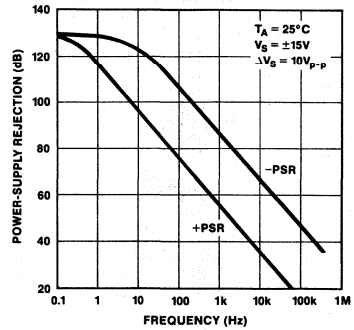
SUPPLY CURRENT vs SUPPLY VOLTAGE



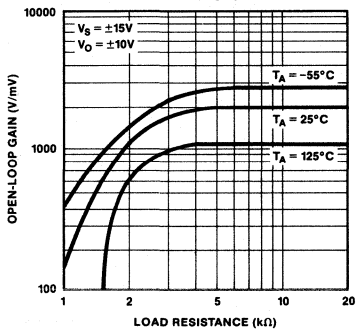
COMMON-MODE REJECTION vs FREQUENCY



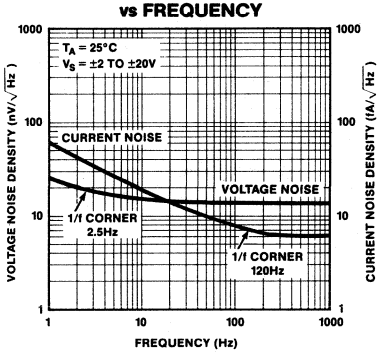
POWER-SUPPLY REJECTION vs FREQUENCY



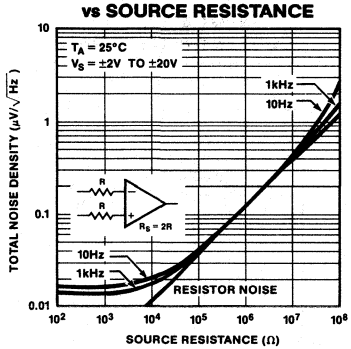
OPEN-LOOP GAIN vs LOAD RESISTANCE



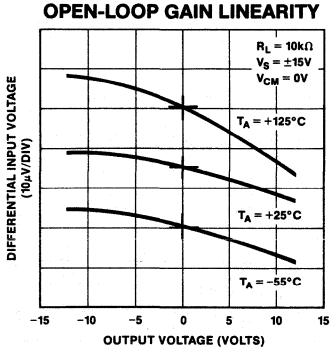
NOISE DENSITY vs FREQUENCY



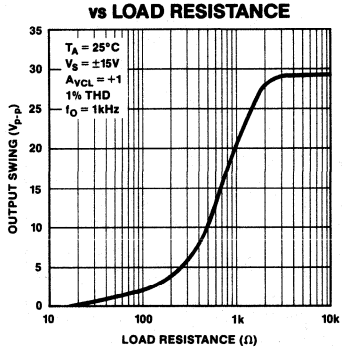
TOTAL NOISE DENSITY vs SOURCE RESISTANCE



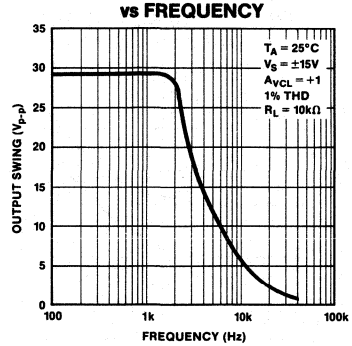
OPEN-LOOP GAIN LINEARITY



MAXIMUM OUTPUT SWING vs LOAD RESISTANCE

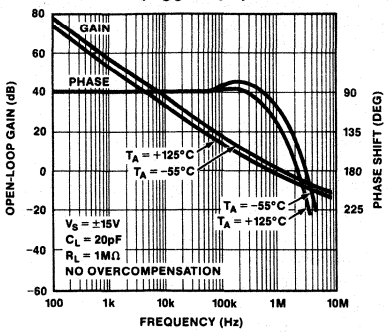


MAXIMUM OUTPUT SWING vs FREQUENCY

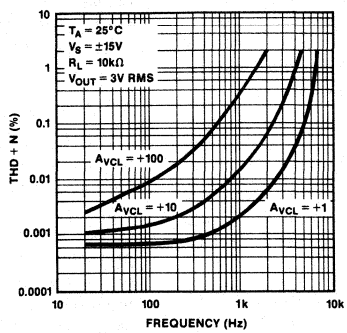


TYPICAL PERFORMANCE CHARACTERISTICS

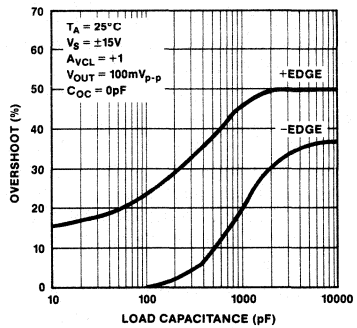
OPEN-LOOP GAIN, PHASE vs FREQUENCY (C_{OC} = 0pF)



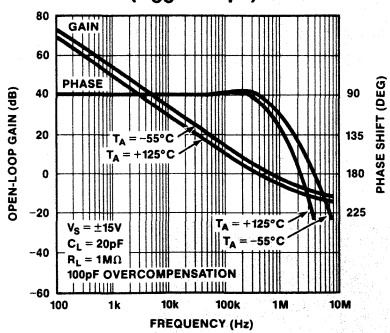
TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY



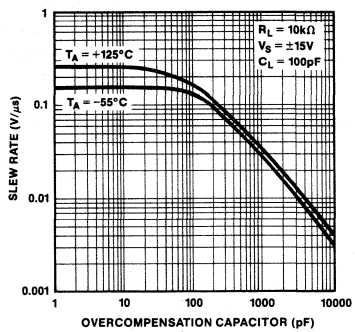
SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD



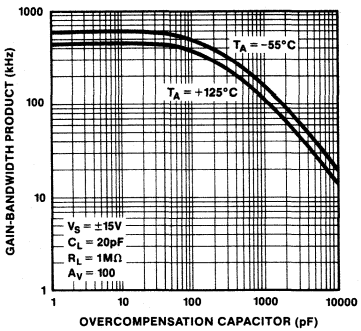
OPEN-LOOP GAIN, PHASE vs FREQUENCY (C_{OC} = 100pF)



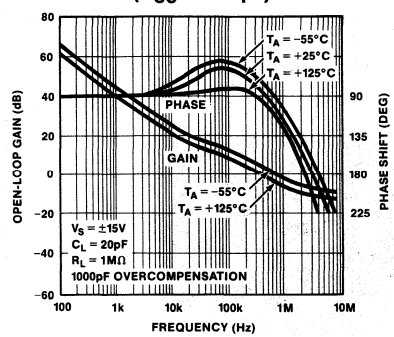
SLEW RATE vs OVERCOMPENSATION



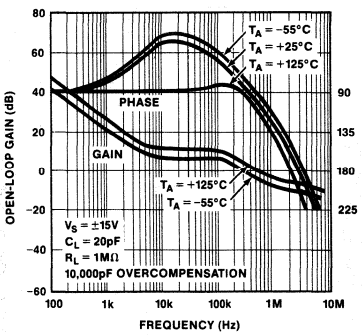
GAIN-BANDWIDTH PRODUCT vs OVERCOMPENSATION



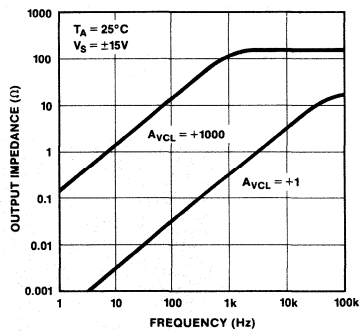
OPEN-LOOP GAIN, PHASE vs FREQUENCY (C_{OC} = 1000pF)



OPEN-LOOP GAIN, PHASE vs FREQUENCY (C_{OC} = 10,000pF)



CLOSED-LOOP OUTPUT RESISTANCE vs FREQUENCY



APPLICATIONS INFORMATION

The OP-97 is a low-power alternative to the industry standard precision op amp, the OP-07. The OP-97 may be substituted directly into OP-07, OP-77, 725, OP-05, 112/312, and 1012 sockets with improved performance and/or less power dissipation, and may be inserted into sockets conforming to the 741 pinout if nulling circuitry is not used. Generally, nulling circuitry used with earlier generation amplifiers is rendered superfluous by the OP-97's extremely low offset voltage, and may be removed without compromising circuit performance.

Extremely low bias current over the full military temperature range makes the OP-97 attractive for use in sample-and-hold amplifiers, peak detectors, and log amplifiers that must operate over a wide temperature range. Balancing input resistances is not necessary with the OP-97. Offset voltage and TCV_{OS} are degraded only minimally by high source resistance, even when unbalanced.

The input pins of the OP-97 are protected against large differential voltage by back-to-back diodes. Current-limiting resistors are not used so that low-noise performance is maintained. If differential voltages above ±1V are expected at the inputs, series resistors must be used to limit the current flow to a maximum of 10mA. Common-mode voltages at the inputs are not restricted, and may vary over the full range of the supply voltages used.

The OP-97 requires very little operating headroom about the supply rails, and is specified for operation with supplies as low as ±2V. Typically, the common-mode range extends to within one volt of either rail. The output typically swings to within one volt of the rails when using a 10kΩ load.

Offset nulling is achieved utilizing the same circuitry as an OP-07. A potentiometer between 5kΩ and 100kΩ is connected between pins 1 and 8 with the wiper connected to the positive supply. The trim range is between 300μV and 850μV, depending upon the internal trimming of the device.

FIGURE 1: Optional Input Offset Voltage Nulling and Overcompensation Circuits

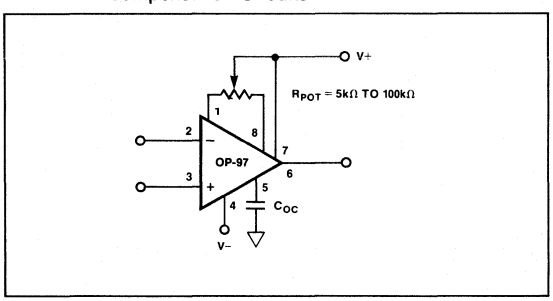
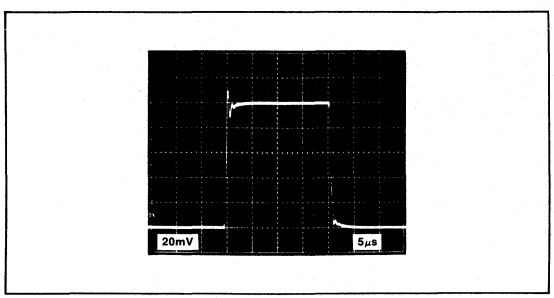


FIGURE 2: Small Signal Transient Response (C_{LOAD} = 100pF, A_{VCL} = +1)



AC PERFORMANCE

The OP-97's AC characteristics are highly stable over its full operating temperature range. Unity-gain small signal response is shown in Figure 2. Extremely tolerant of capacitive loading on the output, the OP-97 displays excellent response even with 1000pF loads (Figure 3). In large-signal applications, the input protection diodes effectively short the input to the output during the transients if the amplifier is connected in the usual unity-gain configuration. The output enters short-circuit current limit, with the flow going through the protection diodes. Improved large-signal transient response is obtained by using a feedback resistor between the output and the inverting input. Figure 4 shows the large-signal response of the OP-97 in unity-gain with a 10kΩ feedback resistor. The unity gain follower circuit is shown in Figure 5.

The overcompensation pin may be used to increase the phase margin of the OP-97, or to decrease gain-bandwidth product at gains greater than 10.

FIGURE 3: Small-Signal Transient Response (C_{LOAD} = 1000pF, A_{VCL} = +1)

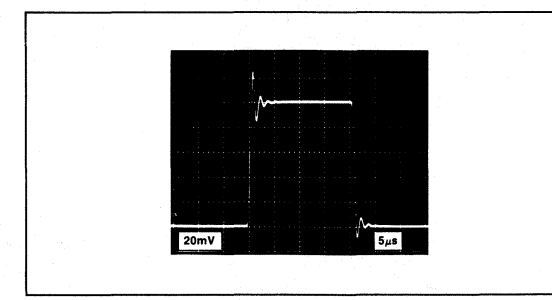


FIGURE 4: Large Signal Transient Response (A_{VCL} = +1)

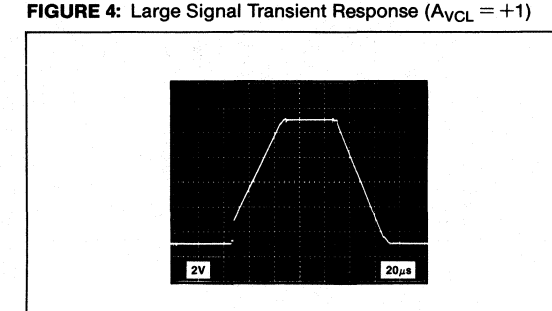


FIGURE 5: Unity-gain Follower

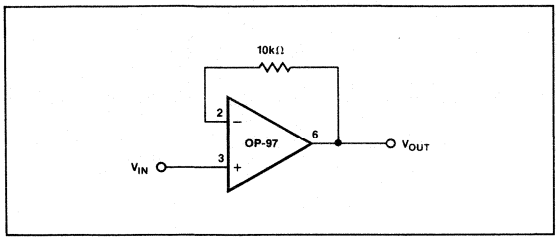
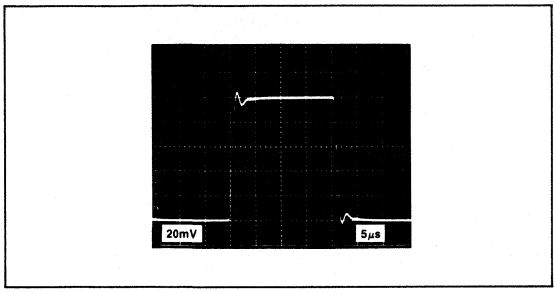


FIGURE 6: Small Signal Transient Response with Overcompensation (C_{LOAD} = 1000pF, A_{VCL} = +1, C_{OC} = 220pF)



GUARDING AND SHIELDING

To maintain the extremely high input impedances of the OP-97, care must be taken in circuit board layout and manufacturing. Board surfaces must be kept scrupulously clean and free of moisture. Conformal coating is recommended to provide a humidity barrier. Even a clean PC board can have 100pA of leakage currents betwen adjacent traces, so that guard rings should be used around the inputs. Guard traces are operated at a voltage close to that on the inputs, so that leakage currents become minimal. In noninverting applications, the guard ring should be connected to the common-mode voltage at the inverting input (pin 2). In inverting applications, both inputs remain at ground, so that the guard trace should be grounded. Guard traces should be made on both sides of the circuit board.

FIGURE 8: DAC Output Amplifier

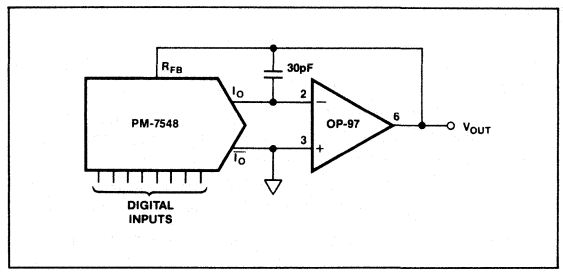


FIGURE 9: Current Monitor

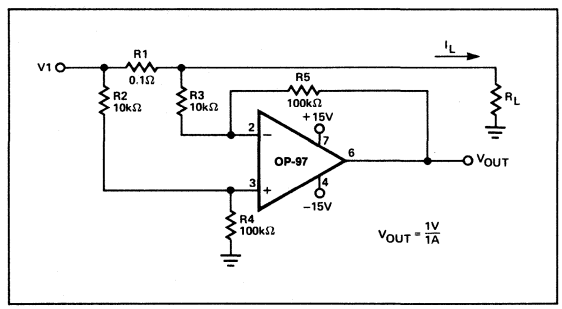
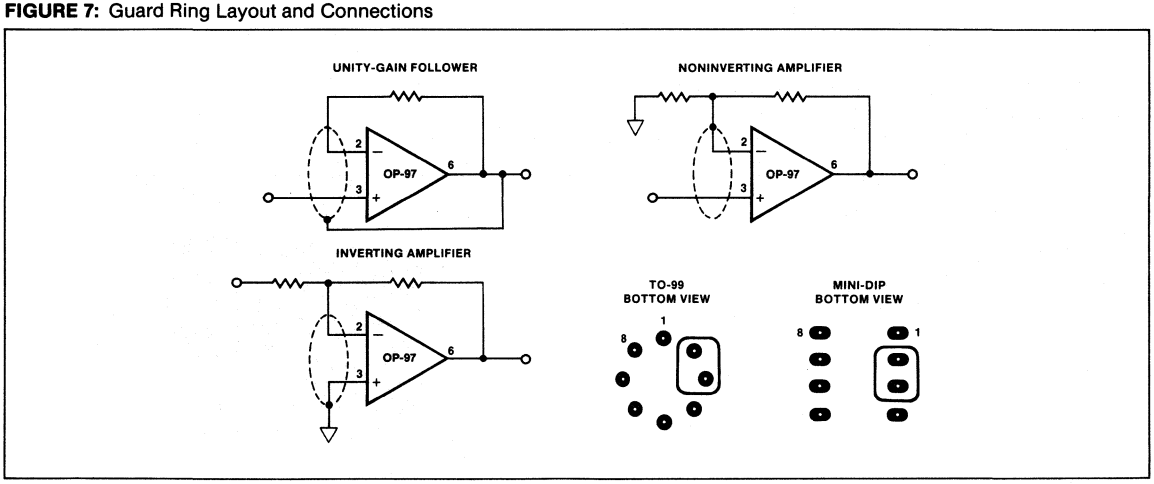


FIGURE 7: Guard Ring Layout and Connections



High impedance circuitry is extremely susceptible to RF pickup, line-frequency hum, and radiated noise from switching power-supplies. Enclosing sensitive analog sections within grounded shields is generally necessary to prevent excessive noise pickup. Twisted-pair cable will aid in rejection of line-frequency hum.

The OP-97 is an excellent choice as an output amplifier for higher resolution CMOS DACs. Its tightly trimmed offset voltage and minimal bias current result in virtually no degradation of linearity, even over wide temperature ranges.

Figure 9 shows a versatile monitor circuit that can typically sense current at any point between the ±15V supplies. This makes it ideal for sensing current in applications such as full bridge drivers where bi-directional current is associated with large common-mode voltage changes. The 114dB CMRR of the OP-97 makes the amplifier's contribution to common-mode error negligible, leaving only the error due to the resistor ratio inequality. Ideally, R2/R4 = R3/R5. This is best trimmed via R4.

The digitally programmable gain amplifier shown in Figure 10 has 12-bit gain resolution with 10-bit gain linearity over the range of −1 to −1024. The low bias current of the OP-97 maintains this linearity, while C1 limits the noise voltage bandwidth allowing accurate measurement down to microvolt levels.

DIGITAL IN	GAIN (A_V)
4095	−1.00024
2048	−2
1024	−4
512	−8
256	−16
128	−32
64	−64
32	−128
16	−256
8	−512
4	−1024
2	−2048
1	−4096
0	OPEN LOOP

Many high-speed amplifiers suffer from less-than-perfect low-frequency performance. A combination amplifier consisting of a high precision, slow device like the OP-97 and a faster device such as the OP-44 results in uniformly accurate performance from DC to the high-frequency limit of the OP-44, which has a gain-bandwidth product of 23MHz. The circuit shown in Figure 11 accomplishes this, with the OP-44 providing high-frequency amplification and the OP-97 operating on low-frequency signals and providing offset correction. Offset voltage and drift of the circuit are controlled by the OP-97.

FIGURE 10: Precision Programmable Gain Amplifier

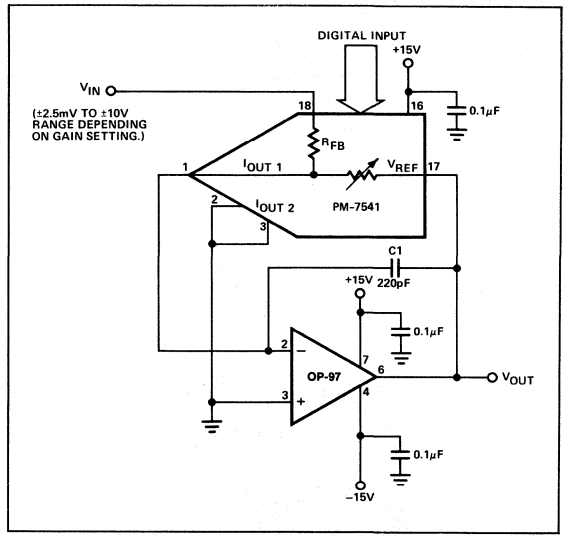


FIGURE 11: Combination High-Speed, Precision Amplifier

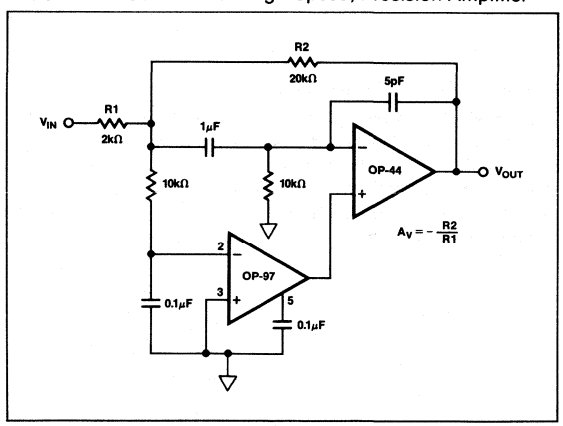
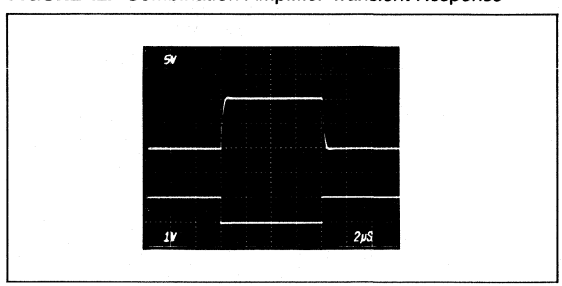


FIGURE 12: Combination Amplifier Transient Response



Low Noise, Low Drift Single-Supply Operational Amplifier

OP-113/OP-213/OP-413

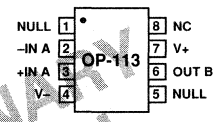
FEATURES
Single-Supply Operation
Low Noise: 6 nV/√Hz @ 1 kHz
Wide Bandwidth: 3 MHz
Low Offset Voltage: 150 μV
Very Low Drift: 0.2 μV/°C
Unity-Gain Stable
No Phase Reversal

APPLICATIONS
Digital Scales
Multimedia
Strain Gages
Battery Powered Instrumentation
Temperature Transducer Amplifier

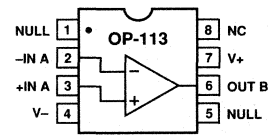
PRELIMINARY TECHNICAL DATA

PIN CONNECTIONS

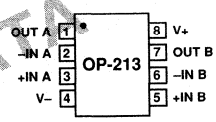
8-Lead Narrow-Body SOIC (S Suffix)



8-Lead Epoxy DIP (P Suffix)



8-Lead Narrow-Body SOIC (S Suffix)



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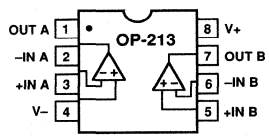
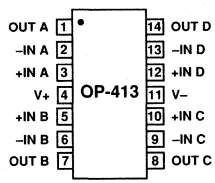
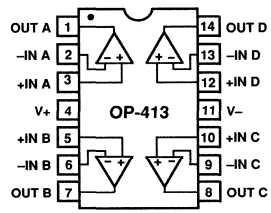


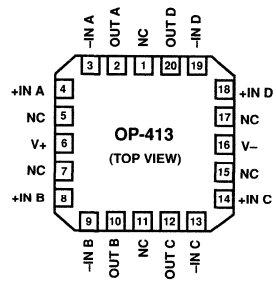
14-Lead Narrow-Body SOIC (S Suffix)



14-Lead Epoxy DIP (P Suffix)



20-Position Chip Carrier (RC Suffix)



GENERAL DESCRIPTION

Designed for systems with internal calibration, the OP-113 single, OP-213 dual and OP-413 quad operational amplifiers feature very low noise and drift. Drift and noise are parameters that are difficult to calibrate out. Most systems with internal calibration use a microprocessor and have +5 V and +12 V supplies, so these amplifiers are designed to be used in single-supply applications. They operate from 4.5 V to 30 V while maintaining precision performance. These unity gain stable amplifiers have a typical gain bandwidth of 3 MHz.

Systems that require low noise and single-supply operation include strain gage applications such as digital scales and multimedia. With a wide common-mode range, that includes the negative supply, and an output that swings from the negative supply to within 1 volt of the positive rail, are other parameters provided for these applications.

The OP-213 is specified over the extended industrial temperature range. Both single, dual and quad amplifiers are available in plastic and ceramic DIP plus SOIC surface mount packages.

Contact your local sales office for MIL-STD-883 data sheet and availability.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

OP-113/OP-213/OP-413—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}				150	μV
Input Bias Current	I_B	V_{CM} = 0 V		500	600	nA
Input Offset Current	I_{OS}	V_{CM} = 0 V			200	nA
Input Voltage Range	V_{CM}		−15		+13	V
Common-Mode Rejection	CMR	V_{CM} = ±12 V	86	106		dB
Large Signal Voltage Gain	A_{VO}	R_L = 600 Ω		200		V/mV
		R_L = 10 kΩ		1500		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			0.2		μV/°C
AUDIO PERFORMANCE						
THD + Noise		V_{IN} = 3 V rms, R_L = 2 kΩ, f = 1 kHz				%
Voltage Noise Density	e_N	f = 10 Hz				nV/√Hz
Voltage Noise Density	e_N	f = 1 kHz		6		nV/√Hz
Voltage Noise	e_N p–p	0.1 Hz to 10 Hz		0.3		μV p–p
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 10 kΩ	−15		+14	V
Short Circuit Limit	I_{SC}			±30		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±15 V		120		dB
Supply Current	I_{SY}	V_O = 0 V, R_L = ∞			4	mA
Supply Voltage Range	V_S		+4.5		±18	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		1		V/μs
Full-Power Bandwidth	BW_p					kHz
Gain Bandwidth Product	GBP			3		MHz
Phase Margin	θ_0					Degrees

PRELIMINARY TECHNICAL DATA

Specifications subject to change without notice.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ELECTRICAL CHARACTERISTICS (@ V_S = +5.0 V, T_A = +25°C unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}				150	μV
Input Bias Current	I_B	V_{CM} = 2.5 V		500	600	nA
Input Offset Current	I_{OS}	V_{CM} = 2.5 V			200	nA
Input Voltage Range	V_{CM}		0		4	V
Common-Mode Rejection	CMR	V_{CM} = ± V	86	106		dB
Large Signal Voltage Gain	A_{VO}	R_L = 600 Ω		200		V/mV
		R_L = 10 kΩ		1500		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			0.2		μV/°C
AUDIO PERFORMANCE						
THD + Noise		V_{IN} = 3 V rms, R_L = 2 kΩ, f = 1 kHz				%
Voltage Noise Density	e_N	f = 10 Hz				nV/√Hz
Voltage Noise Density	e_N	f = 1 kHz		6		nV/√Hz
Voltage Noise	e_N p–p	0.1 Hz to 10 Hz		0.3		μV p–p
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 10 kΩ	0		+4	V
Short Circuit Limit	I_{SC}			±30		mA
POWER SUPPLY						
Supply Current	I_{SY}	V_O = 0 V, R_L = ∞			3.5	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		1		V/μs
Full-Power Bandwidth	BW_p					kHz
Gain Bandwidth Product	GBP			3		MHz
Phase Margin	θ_0					Degrees

PRELIMINARY TECHNICAL DATA

Specifications subject to change without notice.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

WAFER TEST LIMITS (@ V_S = +5.0 V, T_A = +25°C unless otherwise specified.)

Parameter	Symbol	Conditions	Limit	Units
Offset Voltage	V_{OS}		150	mV max
Input Bias Current	I_B	V_{CM} = 0 V	600	nA max
Input Offset Current	I_{OS}	V_{CM} = 0 V	200	nA max
Input Voltage Range[1]				V min
Common-Mode Rejection	CMRR	0 ≤ V_{CM} ≤ 4	86	dB min
Power Supply Rejection Ratio	PSRR	V = ±4.5 V to ±15 V		μV/V
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ	200	V/mV min
Output Voltage Range	V_O	R_L = 2 kΩ	4	V min
Supply Current	I_{SY}	V_O = 0 V, R_L = ∞	3.5	mA max

NOTES
Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on DICE lot qualifications through sample lot assembly and testing.
[1]Guaranteed by CMR test.

PRELIMINARY TECHNICAL DATA

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Input Voltage[2] . . . . . ±18 V
Differential Input Voltage[2] . . . . . 36 V
Output Short-Circuit Duration to GND[3] . . . . . Indefinite
Storage Temperature Range
  Z, RC Package . . . . . −65°C to +175°C
  P, S Package . . . . . −65°C to +150°C
Operating Temperature Range
  OP-213A . . . . . −55°C to +125°C
  OP-213G . . . . . −40°C to +85°C
Junction Temperature Range
  P, S Package . . . . . −65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C

Package Type	θ_{JA}[4]	θ_{JC}	Units
8-Pin Cerdip (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W
14-Pin Cerdip (Y)	108	16	°C/W
14-Pin Plastic DIP (P)	83	39	°C/W
14-Pin SOIC (S)	120	36	°C/W
20-Contact LCC (RC)	98	38	°C/W

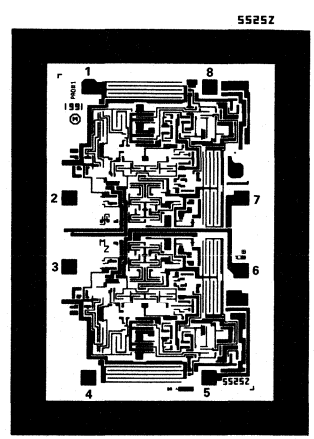
NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.
[3]Shorts to either supply may destroy the device. See data sheet for full details.
[4]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered in circuit board for SOIC package.

ORDERING GUIDE

Model	Temperature Range	Package Option*
OP113AZ/883	−55°C to +125°C	8-Pin Cerdip
OP113GP	−40°C to +85°C	8-Pin Plastic DIP
OP113GS	−40°C to +85°C	8-Pin SOIC
OP113GBC	+25°C	DICE
OP213AZ/883	−55°C to +125°C	8-Pin Cerdip
OP213ARC/883	−55°C to +125°C	20-Contact LCC
OP213GP	−40°C to +85°C	8-Pin Plastic DIP
OP213GS	−40°C to +85°C	8-Pin SOIC
OP213GBC	+25°C	DICE
OP413AZ/883	−55°C to +125°C	14-Pin Cerdip
OP413ARC/883	−55°C to +125°C	20-Contact LCC
OP413GP	−40°C to +85°C	14-Pin Plastic DIP
OP413GS	−40°C to +85°C	14-Pin SOIC
OP413GBC	+25°C	DICE

*For outline information see Package Information section.

DICE CHARACTERISTICS



OP-213 Die Size 0.062 in. × 0.097 in. (6,014 sq. mils.)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ANALOG DEVICES

High-Speed, Current Feedback Operational Amplifier

OP-160

FEATURES

- **Easy To Use – Drives Large Capacitive Loads**
- **Very High Slew Rate (A_V = +1) ..... 1300 V/µs Typ**
- **Bandwidth (A_V = +1) ..... 90MHz Typ**
- **Low Supply Current ..... 6.5mA Typ**
- **Bandwidth Independent of Gain**
- **Unity-Gain Stable**
- **Power Shutdown Pin**

APPLICATIONS

- **High-Speed Data Acquisition**
- **Communication Systems/RF Amplifiers**
- **Video Gain Block**
- **High-Speed Integrators**
- **Driving High-Speed ADCs**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (mV)	PACKAGE CERDIP 8-PIN	PACKAGE PLASTIC 8-PIN	PACKAGE LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
5.0	OP160AZ*	—	OP160ARC/883	MIL
5.0	OP160FZ	OP160GP	—	XIND
5.0	—	OP160GS††	—	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on extended industrial temperature range parts in CerDIP and plastic packages.

†† For availability and burn-in information on SO package, contact your local sales office.

GENERAL DESCRIPTION

The OP-160 is an easy-to-use high-speed, current feedback op amp. Designed to handle large capacitive loads, the OP-160 resists unstable operation. The OP-160 combines PMI's high-speed complementary bipolar process with a current feedback topology for very high slew rate and wide bandwidth performance.

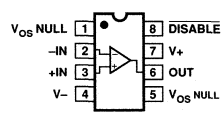
Slew rate of the OP-160 is typically 1300V/µs and is guaranteed to exceed 1000V/µs. In addition, the OP-160's current feedback design has the added advantage of nearly constant bandwidth versus gain. In a gain of +1 the –3dB bandwidth is 90MHz! The OP-160 also requires only 6.5mA of supply current, a considerable power savings over other high-speed amplifiers.

Applications using the OP-160 can be implemented with the same circuit assumptions utilized for conventional voltage feedback op amps. With its high speed and bandwidth, the OP-160 is ideal for a variety of applications including video amplifiers, RF amplifiers, and high-speed data acquisition systems.

The OP-160 is an easy-to-use alternative to the AD844, AD846, EL2020 and EL2030.

For applications requiring a high-speed, wide bandwidth dual amplifier, see the OP-260.

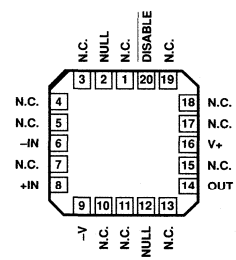
PIN CONNECTIONS



8-PIN EPOXY MINI-DIP (P-Suffix)

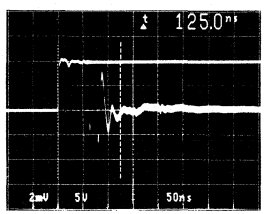
8-PIN CERDIP (Z-Suffix)

8-PIN SO (S-Suffix)



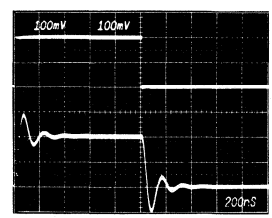
20-CONTACT LCC (RC-Suffix)

FAST SETTLING (0.01%)



A_V = –1, +10V STEP INPUT

DRIVES CAPACITIVE LOADS



A_V = +1, C_L = 1000pF

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Input Voltage ..... Supply Voltage
Differential Input Voltage ..... ±1V
Inverting Input Current ..... ±7mA Continuous
..... ±20mA Peak
Output Short-Circuit Duration ..... 10 sec
Operating Temperature Range
OP-160A (Z, RC) ..... –55°C to +125°C
OP-160A,F (Z) ..... –40°C to +85°C
OP-160G (P,S) ..... –40°C to +85°C
Storage Temperature (Z, RC) ..... –65°C to +175°C
(P, S) ..... –65°C to +150°C
Junction Temperature (Z, RC) ..... –65°C to +175°C
(P, S) ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC (RC)	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, V_{CM} = 0V, R_F = 820Ω, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		OP-160A/F MIN	OP-160A/F TYP	OP-160A/F MAX	OP-160G MIN	OP-160G TYP	OP-160G MAX	UNITS
Input Offset Voltage	V_{IOS}			–	2	5	–	2	5	mV
Input Bias Current	I_{B+} I_{B-}	Noninverting Input Inverting Input		– –	0.2 6	1 20	– –	0.4 10	1.5 30	µA
Input Bias Current Common-Mode Rejection Ratio	$CMRRI_{B+}$ $CMRRI_{B-}$	V_{CM} = ±11V Noninverting Input Inverting Input		– –	40 30	75 75	– –	50 40	125 125	nA/V
Input Bias Current Power Supply Rejection Ratio	$PSRRI_{B+}$ $PSRRI_{B-}$	V_S = ±9V to ±18V Noninverting Input Inverting Input		– –	1 20	5 50	– –	1.5 25	10 75	nA/V
Common-Mode Rejection	CMR	V_{CM} = ±11V		60	65	–	60	65	–	dB
Power Supply Rejection	PSR	V_S = ±9V to ±18V		74	80	–	74	80	–	dB
Open-Loop Transimpedance	R_T	R_L = 500Ω V_O = ±10V		3	4	–	3	4	–	MΩ
Input Voltage Range	IVR	(Note 1)		±11	–	–	±11	–	–	V
Output Voltage Swing	V_O	R_L = 500Ω		±11	–	–	±11	–	–	V
Output Current	I_O	V_O = ±10V		±35	+60/–45	–	±35	+60/–45	–	mA
Supply Current	I_{SY}	No Load		–	6.5	8	–	6.5	8	mA
Slew Rate	SR	A_V = +1, V_O = ±10V, R_L = 500Ω, Test at V_O = ±5V	All Grades	–	1300	–	–	1300	–	V/µs
		A_V = +2, V_O = ±10V, R_L = 500Ω, Test at V_O = ±5V	OP-160A OP-160F OP-160G	1000 800 –	1300 1300 –	– – –	– – 800	– – 1300	– – –	

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $V_{CM} = 0V$, $R_F = 820\Omega$, $T_A = +25°C$, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS		OP-160A/F MIN	OP-160A/F TYP	OP-160A/F MAX	OP-160G MIN	OP-160G TYP	OP-160G MAX	UNITS
Rise Time	t_R	$A_V = +1$	$V_O = \pm100mV$	–	4	–	–	4	–	ns
		$A_V = -1$		–	6.4	–	–	6.4	–	
–3dB Bandwidth	BW	–3dB Point	$A_V = -1$	–	55	–	–	55	–	MHz
		$R_L = 500\Omega$	$A_V = +1$	–	90	–	–	90	–	
			$A_V = +2$	–	65	–	–	65	–	
Settling Time	t_s	$A_V = -1$, 10V Step								ns
		0.01%		–	125	–	–	125	–	
		0.1%		–	75	–	–	75	–	
Input Capacitance	C_{IN}	Noninverting Input		–	4	–	–	4	–	pF
Input Resistance	R_{IN}	Noninverting Input		–	17	–	–	10	–	MΩ
		Inverting Input		–	60	–	–	60	–	Ω
Voltage Noise Density	e_n	$f = 1kHz$		–	5.5	–	–	5.5	–	$nV/\sqrt{Hz}$
Current Noise Density	i_n	$f = 1kHz$								$pA/\sqrt{Hz}$
		Noninverting Input		–	5	–	–	5	–	
		Inverting Input		–	20	–	–	20	–	
Total Harmonic Distortion	THD	$f = 1kHz$, $A_V = +1$, $V_O = 2V_{RMS}$, $R_L = 500\Omega$		–	0.004	–	–	0.004	–	%
Differential Gain		$f = 3.58MHz$ $A_V = +1$, $R_L = 500\Omega$		–	0.04	–	–	0.04	–	%
Differential Phase		$f = 3.58MHz$ $A_V = +1$, $R_L = 500\Omega$		–	0.04	–	–	0.04	–	degrees
Disable Supply Current	$I_{SY\overline{DIS}}$	$\overline{DISABLE} = 0V$ No Load		–	2.3	–	–	2.3	–	mA

NOTE:
1. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $V_{CM} = 0V$, $R_F = 820\Omega$, $-55°C \le T_A \le +125°C$, for the OP-160A, unless otherwise noted.

			OP-160A			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{IOS}		–	3	8	mV
Average Input Offset Voltage Drift	TC_{VOS}		–	10	–	µV/°C
Input Bias Current	I_{B+} I_{B-}	Noninverting Input Inverting Input	– –	0.35 12	2 30	µA
Input Bias Current Common-Mode Rejection		$V_{CM} = \pm 10V$				nA/V
	$CMRRI_{B+}$	Noninverting Input	–	55	150	
	$CMRRI_{B-}$	Inverting Input	–	45	150	
Input Bias Current Power Supply Rejection Ratio		$V_S = \pm 9V$ to $\pm 18V$				nA/V
	$PSRRI_{B+}$	Noninverting Input	–	2	10	
	$PSRRI_{B-}$	Inverting Input	–	40	100	
Common-Mode Rejection	CMR	$V_{CM} = \pm 10V$	56	60	–	dB
Power Supply Rejection	PSR	$V_S = \pm 9V$ to $\pm 18V$	70	76	–	dB
Open-Loop Transimpedance	R_T	$R_L = 500\Omega$ $V_O = \pm 10V$	1.75	3	–	MΩ
Input Voltage Range	IVR	(Note 1)	±10	–	–	V
Output Voltage Swing	V_O	$R_L = 500\Omega$	±10	–	–	V
Supply Current	I_{SY}	No Load	–	6.75	9	mA

NOTE:
1. Guaranteed by CMR test.

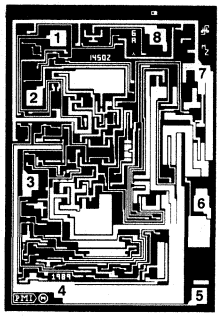
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $V_{CM} = 0V$, $R_F = 820\Omega$, $-40°C \le T_A \le +85°C$, for the OP-160F/G, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-160F MIN	OP-160F TYP	OP-160F MAX	OP-160G MIN	OP-160G TYP	OP-160G MAX	UNITS
Input Offset Voltage	V_{IOS}		–	2.75	8	–	2.75	8	mV
Average Input Offset Voltage	TCV_{OS}		–	10	–	–	10	–	µV/°C
Input Bias Current	I_{B+} I_{B-}	Noninverting Input Inverting Input	– –	0.3 10	2 30	– –	0.5 15	3 40	µA
Input Bias Current Common-Mode Rejection Ratio	$CMRRI_{B+}$ $CMRRI_{B-}$	$V_{CM} = \pm 10V$ Noninverting Input Inverting Input	– –	45 35	150 150	– –	55 45	250 250	nA/V
Input Bias Current Power Supply Rejection Ratio	$PSRRI_{B+}$ $PSRRI_{B-}$	$V_S = \pm 9V$ to $\pm 18V$ Noninverting Input Inverting Input	– –	1.5 30	10 100	– –	2.5 3.5	20 150	nA/V
Common-Mode Rejection	CMR	$V_{CM} = \pm 10V$	56	62	–	56	62	–	dB
Power Supply Rejection	PSR	$V_S = \pm 9V$ to $\pm 18V$	70	80	–	70	80	–	dB
Open-Loop Transimpedance	R_T	$R_L = 500\Omega$ $V_O = \pm 10V$	1.75	3	–	1.75	3	–	MΩ
Input Voltage Range	IVR	(Note 1)	±10	–	–	±10	–	–	V
Output Voltage Swing	V_O	$R_L = 500\Omega$	±10	–	–	±10	–	–	V
Supply Current	I_{SY}	No Load, Both Amplifiers	–	6.75	9	–	6.75	9	mA

NOTE:
1. Guaranteed by CMR test.

OP-160

DICE CHARACTERISTICS



DIE SIZE 0.071 x 0.099 inch, 7,029 sq. mils
(1.80 x 2.52 mm, 4.54 sq. mm)

1. V_{OS} NULL
2. –IN
3. +IN
4. V–
5. V_{OS} NULL
6. OUT
7. V+
8. $\overline{\text{DISABLE}}$

WAFER TEST LIMITS at $V_S = \pm 15V$, $V_{CM} = 0V$, $R_F = 820\Omega$, $T_A = +25°C$, unless otherwise noted.

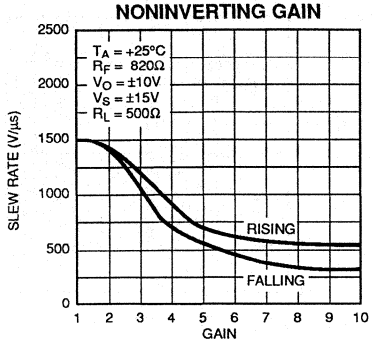
PARAMETER	SYMBOL	CONDITIONS	OP-160GBC LIMITS	UNITS
Input Offset Voltage	V_{IOS}		5	mV MAX
Input Bias Current	I_{B+} I_{B-}	Noninverting Input Inverting Input	1.5 30	µA MAX
Input Bias Current Common-Mode Rejection Ratio	$CMRRI_{B+}$ $CMRRI_{B-}$	$V_{CM} = \pm 11V$ Noninverting Input Inverting Input	125 125	nA/V MAX
Input Bias Current Power Supply Rejection Ratio	$PSRRI_{B+}$ $PSRRI_{B-}$	$V_S = \pm 9V$ to $\pm 18V$ Noninverting Input Inverting Input	10 75	nA/V MAX
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	60	dB MIN
Power Supply Rejection	PSR	$V_S = \pm 9V$ to $\pm 18V$	74	dB MIN
Open-Loop Transimpedance	R_T	$R_L = 500\Omega$ $V_O = \pm 10V$	3	MΩ MIN
Input Voltage Range	IVR		±11	V MIN
Output Voltage Swing	V_O	$R_L = 500\Omega$	±11	V MIN
Supply Current	I_{SY}	No Load	8	mA MAX

NOTES:
1. Guaranteed by CMR test.

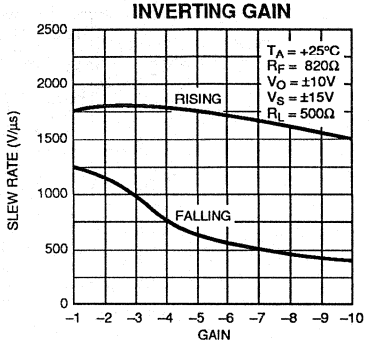
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

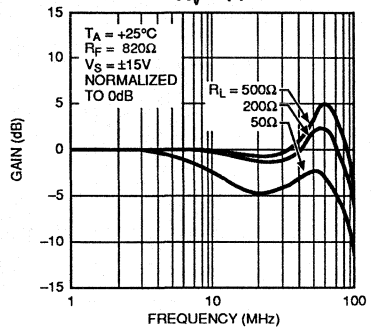
SLEW RATE vs NONINVERTING GAIN



SLEW RATE vs INVERTING GAIN



GAIN vs FREQUENCY A_V = +1



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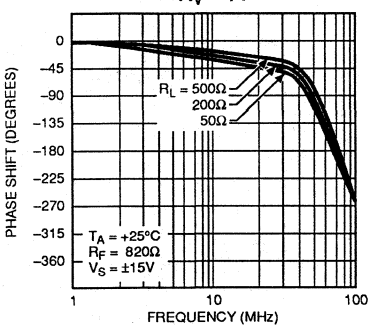
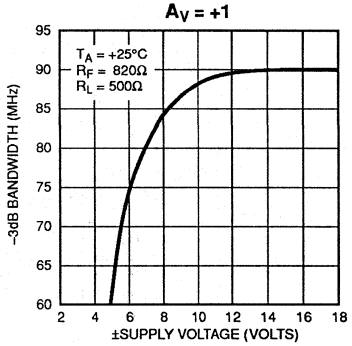
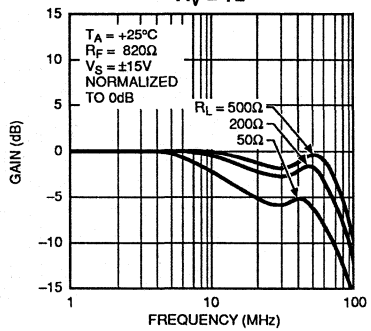


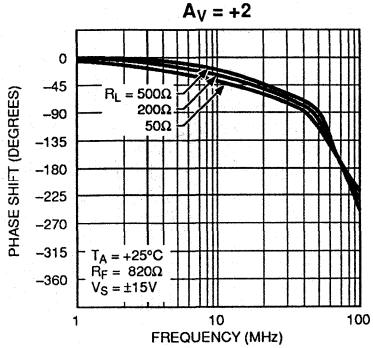
–3dB BANDWIDTH vs SUPPLY VOLTAGE A_V = +1



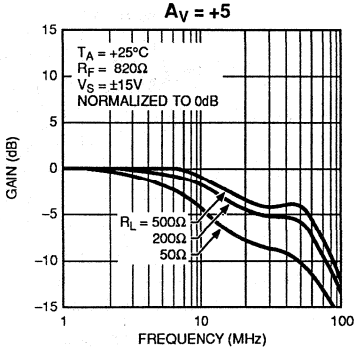
GAIN vs FREQUENCY A_V = +2



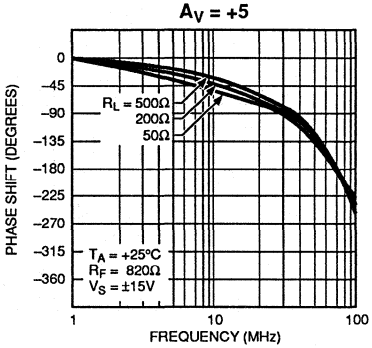
PHASE SHIFT vs FREQUENCY A_V = +2



GAIN vs FREQUENCY A_V = +5



PHASE SHIFT vs FREQUENCY A_V = +5



TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

GAIN vs FREQUENCY
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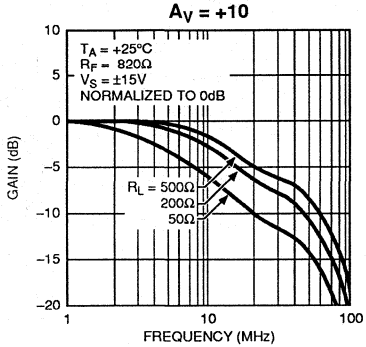
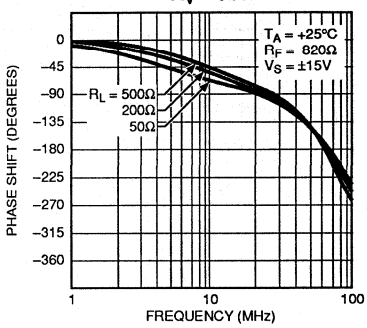


PHASE SHIFT vs FREQUENCY
A_V = +10



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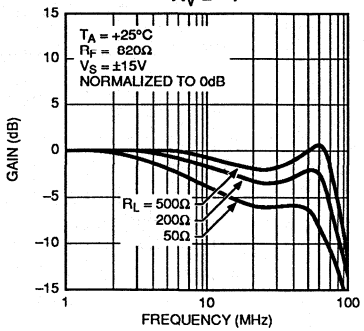

PHASE SHIFT vs FREQUENCY
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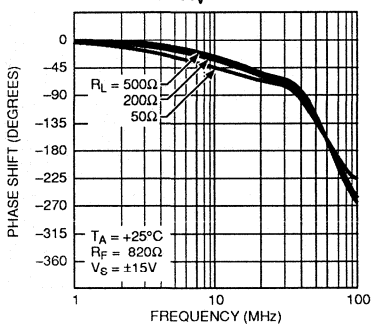

GAIN vs FREQUENCY
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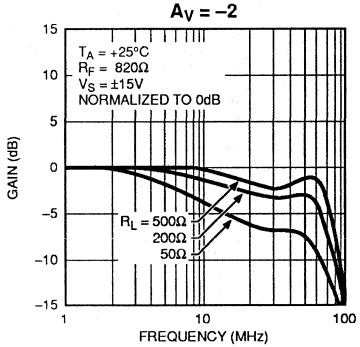
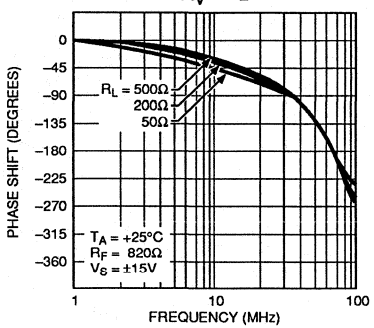


PHASE SHIFT vs FREQUENCY
A_V = –2



GAIN vs FREQUENCY
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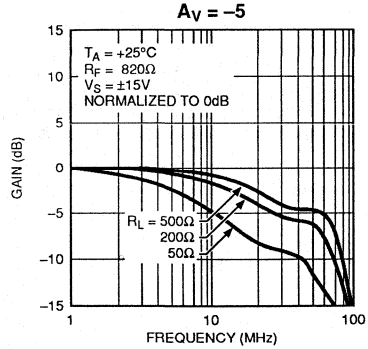
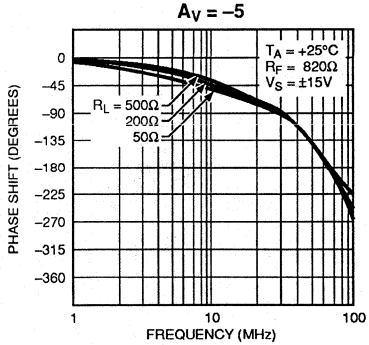
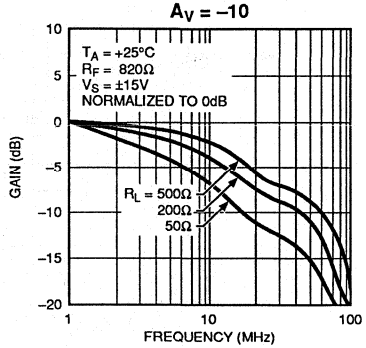


PHASE SHIFT vs FREQUENCY
A_V = –5

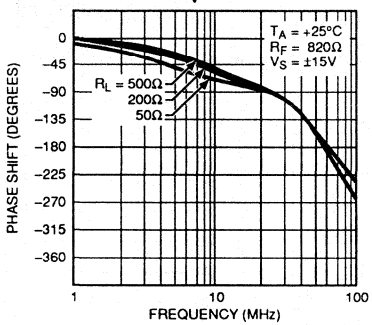


GAIN vs FREQUENCY
A_V = –10

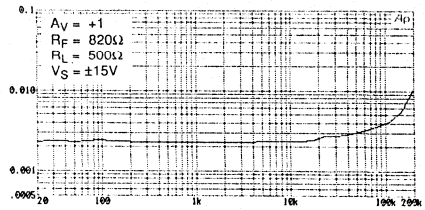


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

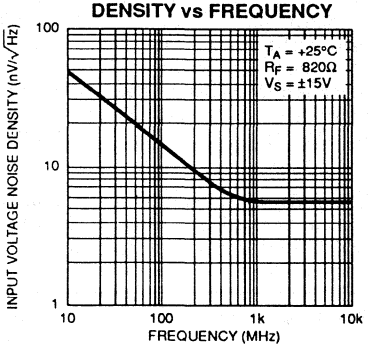
PHASE SHIFT vs FREQUENCY
A_V = –10



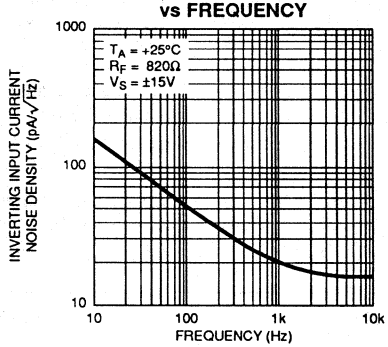
TOTAL HARMONIC DISTORTION vs FREQUENCY



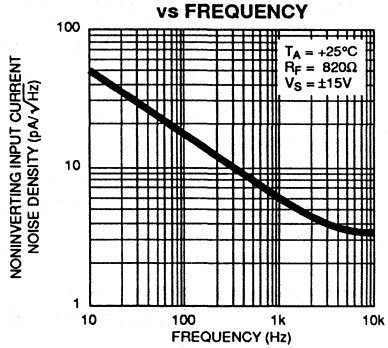
INPUT VOLTAGE NOISE DENSITY vs FREQUENCY



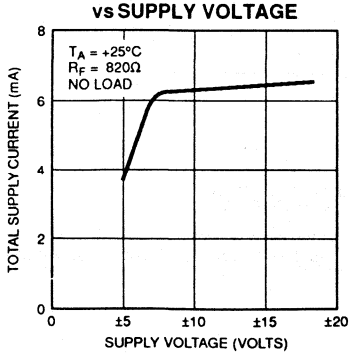
INVERTING INPUT CURRENT NOISE DENSITY vs FREQUENCY



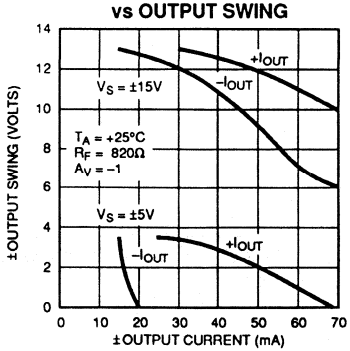
NONINVERTING INPUT CURRENT NOISE DENSITY vs FREQUENCY



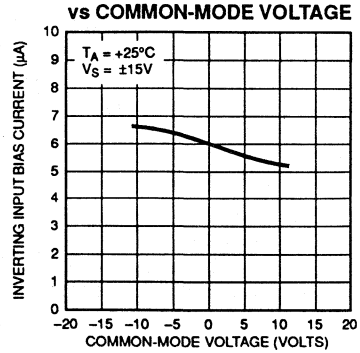
TOTAL SUPPLY CURRENT vs SUPPLY VOLTAGE



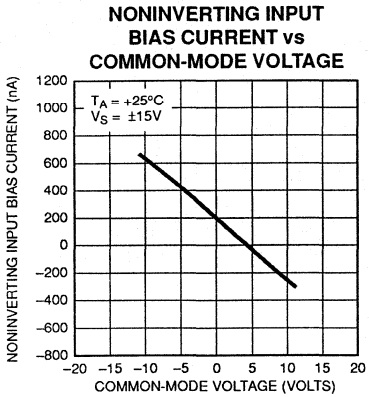
OUTPUT CURRENT vs OUTPUT SWING

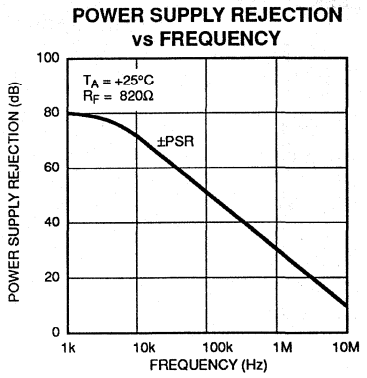


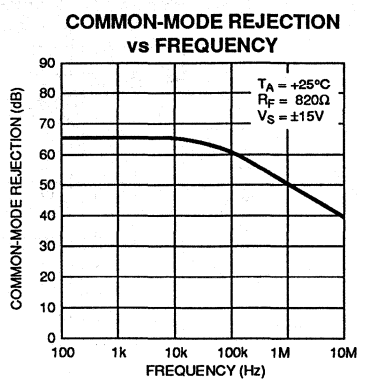
INVERTING INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE



TYPICAL PERFORMANCE CHARACTERISTICS *Continued*







APPLICATIONS INFORMATION

CURRENT VERSUS VOLTAGE FEEDBACK AMPLIFIERS

The OP-160 employs a unique circuit topology that sets it apart from conventional op amps. By using a transimpedance amplifier configuration, the OP-160 provides substantial improvements in bandwidth and slew rate over voltage feedback op amps. Figure 1 compares models of these two different amplifier configurations.

A voltage feedback op amp multiplies the differential voltage at its inputs by its open-loop gain. The feedback loop forces the output to a voltage that, when divided by R_1 and R_2, equalizes the input voltages. Unlike a voltage feedback op amp, which has high impedance inputs, the current feedback amplifier has a high and a low impedance input. The current feedback amplifier's input stage consists of a unity-gain voltage buffer between the noninverting and inverting inputs. The inverting "input" is in reality a low impedance output. Current can flow into or out of the inverting input. A transimpedance stage follows the input buffer that converts the buffer output current into a linearly proportional amplifier output voltage.

The current feedback amplifier loop works in the following fashion (Figure 1b). As the noninverting input voltage rises, the inverting input follows and the buffer sources current through R_1.

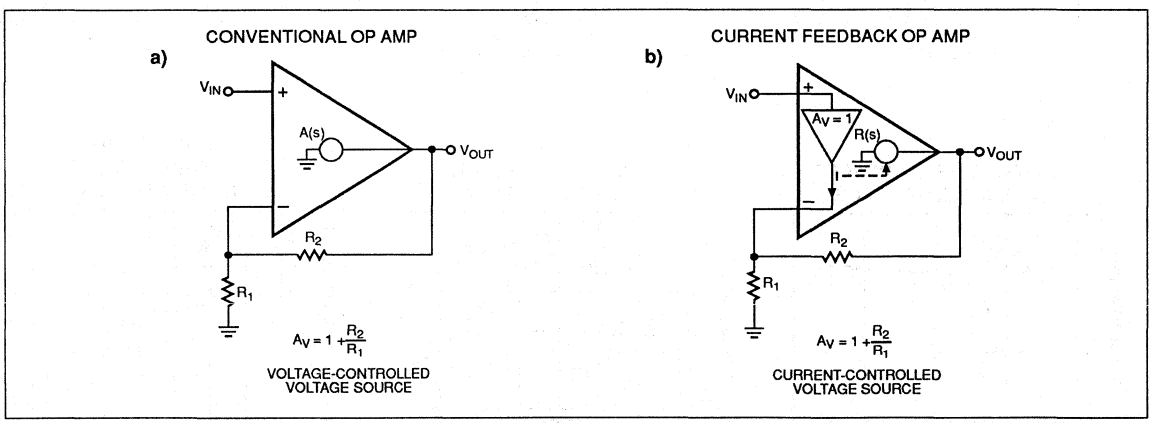


FIGURE 1: *The conventional op amp (a) can be modelled as a voltage-controlled voltage source. In contrast, the current feedback op amp (b), resembles a current-controlled voltage source.*

This current, multiplied by the transimpedance stage, causes the amplifier's output voltage to rise until the current flowing into R_2 from the amplifier's output equalizes the current through R_1, replacing the buffer's output current. At steady state, only a very small buffer output current must flow to sustain the proper output voltage. The ratio $(1 + R_2/R_1)$ determines the closed-loop gain of the circuit. The result is that when designing with current feedback amplifiers the familiar op amp assumptions can still be used for circuit analysis:

1. The voltage across the inputs equals zero.
2. The current into the inputs equals zero.

BANDWIDTH VERSUS GAIN

A unique feature of the current feedback amplifier design is that the closed-loop bandwidth remains relatively constant as a function of closed-loop gain. Voltage feedback op amps suffer from a bandwidth reduction as closed-loop gain increases, as quantified by the gain-bandwidth product (GBWP). This is illustrated in Figure 2 which shows the frequency response of the OP-160 for various closed-loop gains and the frequency response of a voltage feedback op amp with a gain-bandwidth product of 30MHz. The bandwidth of the OP-160 is much less dependent upon closed-loop gain than the voltage feedback op amp.

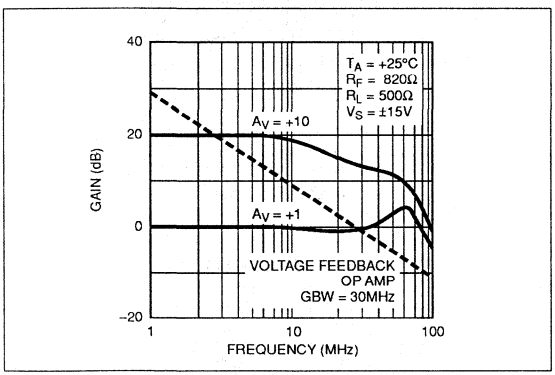


FIGURE 2: *Frequency response of the OP-160 when connected in various closed-loop gains with R_F = 820Ω and R_L = 100Ω. Note that the frequency response of the OP-160 does not follow the asymptotic roll-off characteristic of a voltage feedback op amp.*

FEEDBACK RESISTANCE AND BANDWIDTH

The closed-loop frequency response of the OP-160 shown in Figure 2 applies for a fixed feedback resistor of 820Ω. The frequency response of a current feedback amplifier is primarily dependent on the value of the feedback resistor value. The design of the OP-160 has been optimized for a feedback resistance of 820Ω. By holding the feedback resistor value constant, the –3dB frequency point will also remain constant within a moderate range of closed-loop gain.

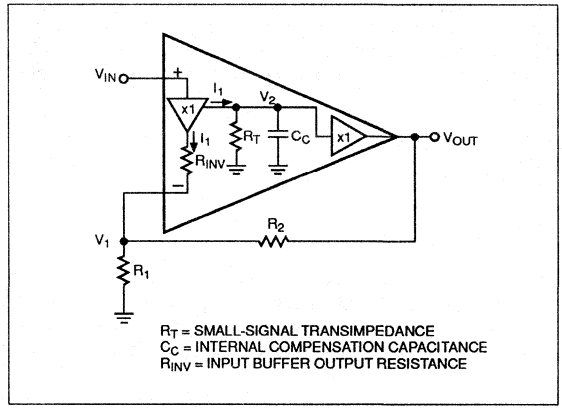


FIGURE 3: *Simple frequency response model of the current feedback amplifier.*

The model shown in Figure 3 can be used to determine the frequency response of a current feedback amplifier. With this model, the frequency response dependency on the value of the feedback resistance is easily seen.

From the model of Figure 3, nodal equations may be written for V_1 and V_2.

$$V_1 = \frac{V_{IN}\left(\frac{R_2}{R_{INV}}\right) + V_{OUT}}{1 + \frac{R_2}{R_1} + \frac{R_2}{R_{INV}}}$$

$$V_2 = \frac{R_T}{1 + sR_T C_C} I_1$$

$$\text{where } I_1 = \frac{V_{IN} - V_1}{R_{INV}} = V_1\left(\frac{1}{R_1} + \frac{1}{R_2}\right) - \frac{V_{OUT}}{R_2}, \text{ and } V_{OUT} = V_2$$

Combining these equations yields:

$$V_{OUT} = \left[\left(\frac{V_{IN}\left(\frac{R_2}{R_{INV}}\right) + V_{OUT}}{1 + \frac{R_2}{R_1} + \frac{R_2}{R_{INV}}}\right)\left(\frac{1}{R_1} + \frac{1}{R_2}\right) - \frac{V_{OUT}}{R_2}\right] \frac{R_T}{1 + sR_T C_C}$$

If the transimpedance of the amplifier, R_T, is » R_2 and R_{INV}, then the transfer function may be simplified to:

$$\frac{V_{OUT}}{V_{IN}} \approx \frac{1 + \frac{R_2}{R_1}}{1 + s\left[R_2 + \left(1 + \frac{R_2}{R_1}\right)R_{INV}\right] C_C}$$

The transfer function shows that the dominant closed-loop pole is mainly dependent on the value of the feedback resistance, R_2, and the internal compensation capacitor, C_C. For example, at unity gain, where R_1 is infinite, R_2 determines the –3dB frequency.

$$\frac{V_{OUT}}{V_{IN}} \approx \frac{1}{1 + sR_2 C_C}$$

$$f_{-3dB} = \frac{1}{2\pi R_2 C_C}$$

where $R_2 \gg R_{INV}$

For higher gains, the –3dB frequency is determined by R_2 plus the output resistance of the buffer, R_{INV} (typically 60Ω), which is multiplied by the closed-loop gain. As the closed-loop gain increases, the multiplying effect on R_{INV} becomes dominant, causing the bandwidth to decrease. However, the closed-loop bandwidth of a current feedback amplifier still far exceeds that of a voltage feedback op amp for moderate values of gain.

Figure 4 shows the effect of the feedback resistance on the bandwidth of the OP-160 for various closed-loop gains.

SLEW RATE AND GAIN

The simplified schematic in Figure 5 shows the three stages of the OP-160. The input stage consists of a unity-gain emitter-follower amplifier. Q_5 and Q_6 form a class AB output stage at the inverting input which can source or sink current. The current flowing through the inverting input is sensed by the top current mirror, formed by Q_7, Q_9, and Q_{10}, or the bottom current mirror, formed by Q_8, Q_{11}, and Q_{12}. When the buffer sources current to a load, current flows out of the inverting input, increasing Q_5's collector current and causing more current to flow through Q_9

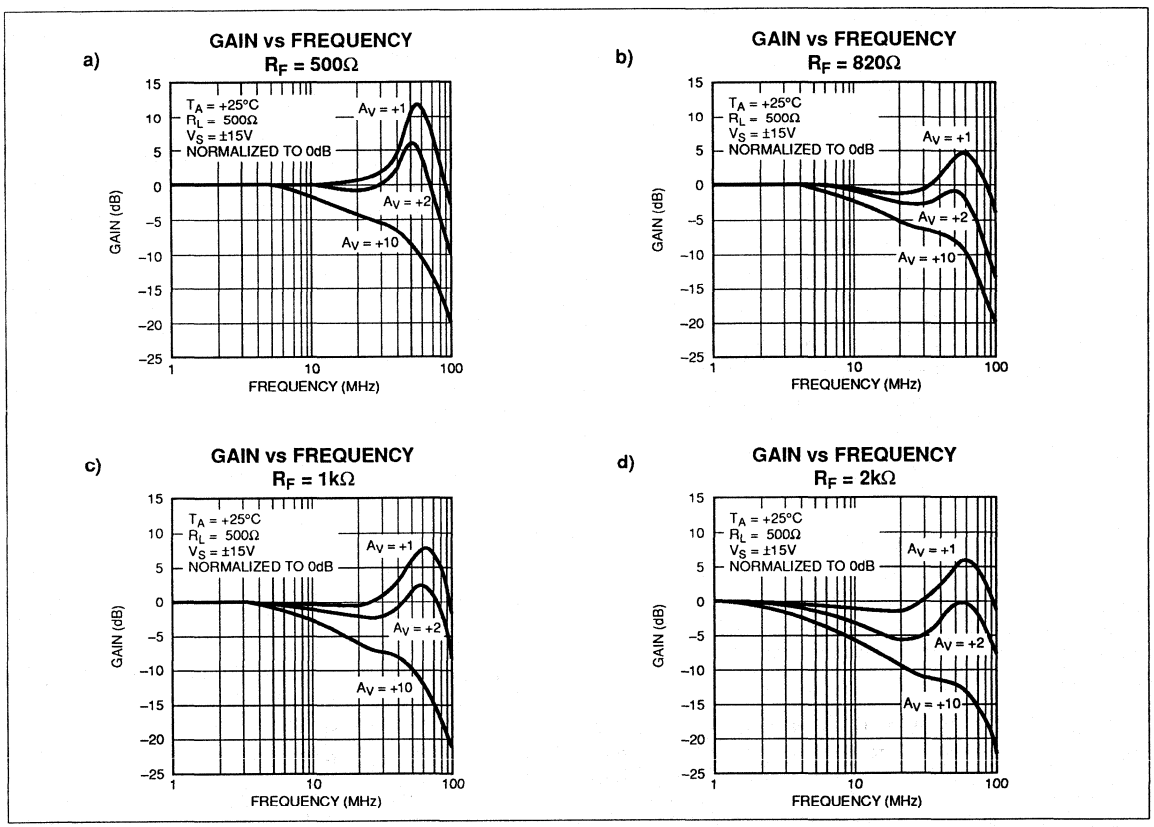


FIGURE 4: *Bandwidth will vary with feedback resistance. Peaking increases as the feedback resistance is decreased. R_F = 820Ω is the recommended value. All graphs are normalized to 0dB.*

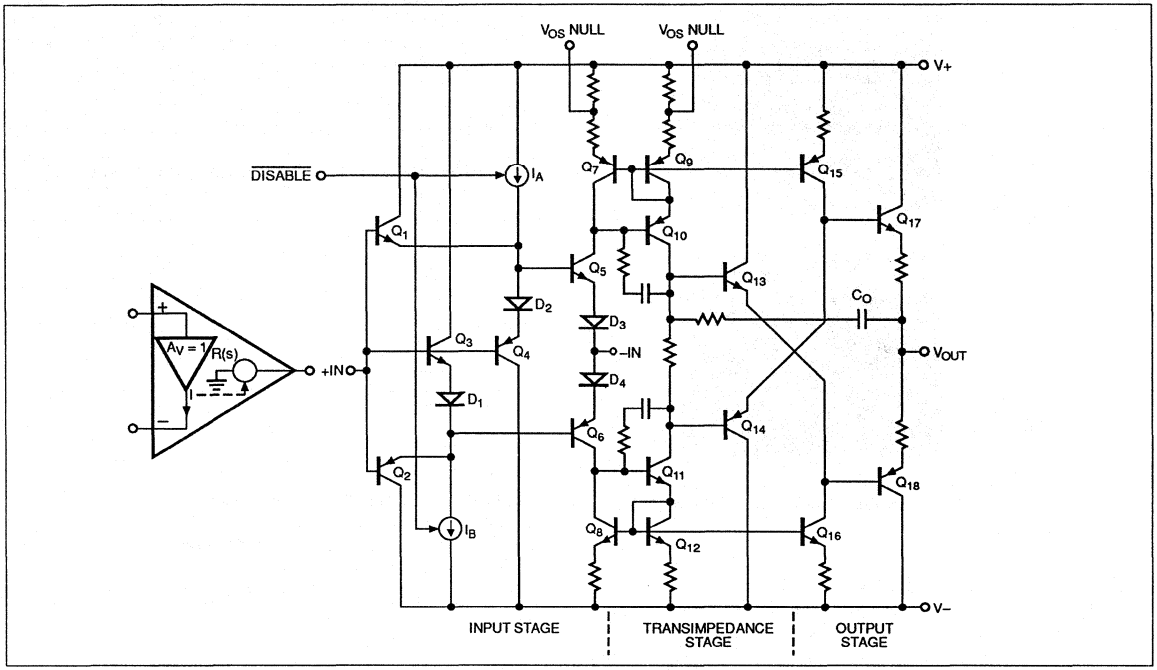


FIGURE 5: *Simplified schematic of the OP-160 showing the three stages of the amplifier.*

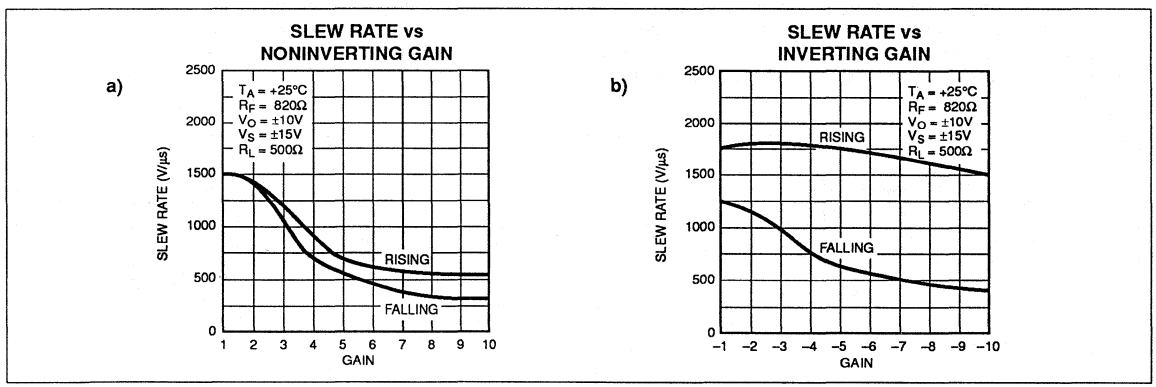


FIGURE 6: *Slew rate of the OP-160 in noninverting (a) and inverting (b) configurations.*

and Q_{15}. This increases the base drive to the output transistor Q_{17}. Simultaneously, the increased current in Q_9 drives Q_{13} which reduces base drive to the complementary output transistor Q_{18}. This push-pull action produces a very fast output slew rate. For a small voltage step, the OP-160's slew rate is dependent on the available current from the two current sources (I_A and I_B) that drive Q_5 and Q_6.

To increase the slew rate, transistors Q_1 and Q_2 have been added to boost the base drive to Q_5 and Q_6. In low gains, a large input step will turn on Q_1 or Q_2 increasing the slew rate dramatically as illustrated in Figure 6.

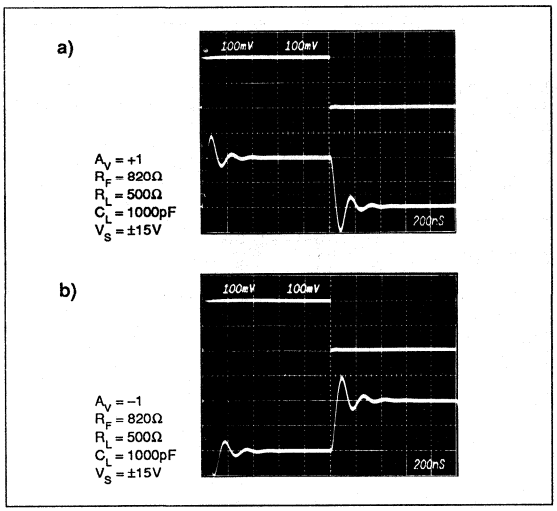


FIGURE 7: *The OP-160 remains stable when driving large capacitive loads.*

DRIVING CAPACITIVE LOADS

The OP-160 is capable of driving capacitive loads at high speed. Output stage compensation is used to reduce the effects of capacitive loading. With low capacitive loads, the gain from the compensation node to the output is unity and C_O does not contribute to the overall compensation. As the load capacitance is increased, a pole is formed with the output resistance of the amplifier. The gain is reduced and C_O begins to contribute to the overall compensation capacitance leading to a reduction in bandwidth. As the load capacitance is increased, the bandwidth is further reduced and the amplifier remains stable. Figure 7 shows the OP-160 in a gain of +1 and –1 driving a 1000pF load without any sign of oscillation. Table 1 shows the effects of capacitive load on the –3dB bandwidth for $A_V = -1$.

TABLE 1: –3dB Bandwidth vs. Capacitive Load; $A_V = -1$, $R_F = 820\Omega$, $R_L = 500\Omega$, $V_S = \pm 15V$.

CAPACITANCE (pF)	–3dB BANDWIDTH (MHz)
0	55
20	55
50	50
75	48
100	40
200	24
500	13
1000	9

AMPLIFIER NOISE PERFORMANCE

Simplified noise models of the OP-160 in the noninverting and inverting amplifier configurations are shown in Figure 8. All resistors are assumed to be noiseless.

For the noninverting amplifier, the equivalent input voltage noise, referred to the input, is:

$$E_N = \sqrt{(R_S\, i_{nn})^2 + e_n^2 + (R_2\, i_{ni})^2 / A_{VCL}}$$

where:

E_N = total input referred noise
e_n = amplifier voltage noise
i_{nn} = noninverting input current noise
i_{ni} = inverting input current noise
R_S = source resistance
A_{VCL} = closed loop gain = $1 + R_2/R_1$

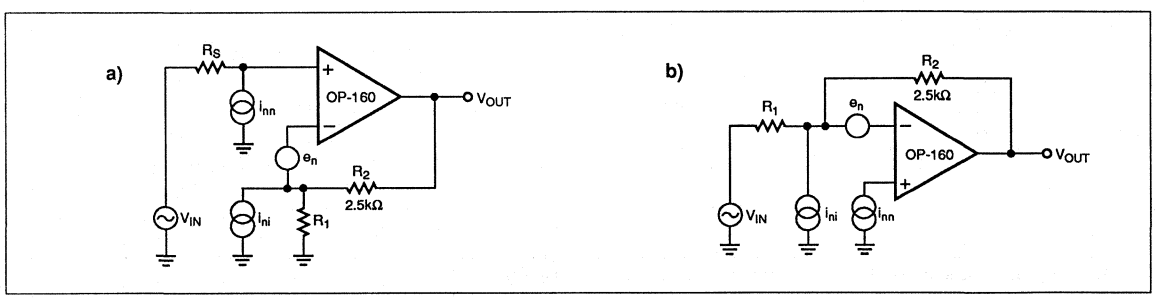


FIGURE 8: *Simplified noise models for the OP-160 in noninverting (a) and inverting (b) gain.*

For the inverting amplifier, the equivalent input voltage noise, referred to the input, is:

$$E_N = \sqrt{e_n^2 \left(\frac{1+|A_{VCL}|}{|A_{VCL}|}\right) + \frac{(R_2\, i_{ni})^2}{|A_{VCL}|}}$$

assuming $R_S \ll R_1$. A_{VCL} = closed-loop gain = $-R_2/R_1$.

Typical values @ 1kHz for the noise parameters of the OP-160 are:

e_n = 5.5nV/√Hz
i_{nn} = 5pA/√Hz
i_{ni} = 20pA/√Hz

SHORT-CIRCUIT PERFORMANCE

To avoid sacrificing bandwidth and slew rate performance the OP-160's output is **not** short-circuit protected. Do not short the amplifier's output to ground or to the supplies. Also, the buffer output current should not exceed a value of ±20mA peak or ±7mA continuous.

POWER SUPPLY BYPASSING AND LAYOUT CONSIDERATIONS

Proper power supply bypassing is critical in all high-frequency circuit applications. For stable operation of the OP-160, the power supplies must maintain a low impedance-to-ground over an extremely wide bandwidth. This is most critical when driving a low resistance or large capacitance, since the current required to drive the load comes from the power supplies. A 10µF and 0.1µF bypass capacitor are recommended for each supply, as shown in Figure 9, and will provide adequate high-frequency bypassing in most applications. The bypass capacitors should be placed at the supply pins of the OP-160. As with all high frequency amplifiers, circuit layout is a critical factor in obtaining optimum performance from the OP-160. Proper high-frequency layout reduces unwanted signal coupling in the circuit. When breadboarding a high-frequency circuit, use direct point-to-point wiring, keeping all lead lengths as short as possible. Do not use wire-wrap boards or "plug-in" prototyping boards.

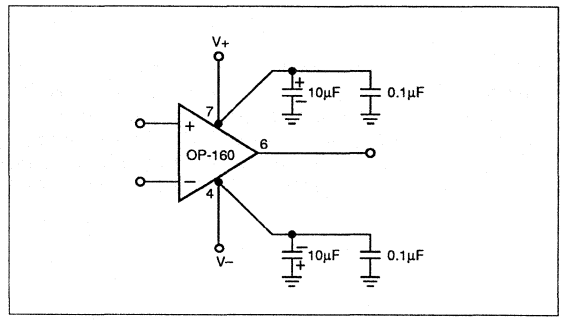


FIGURE 9: *Proper power supplying bypassing is required to obtain optimum performance with the OP-160.*

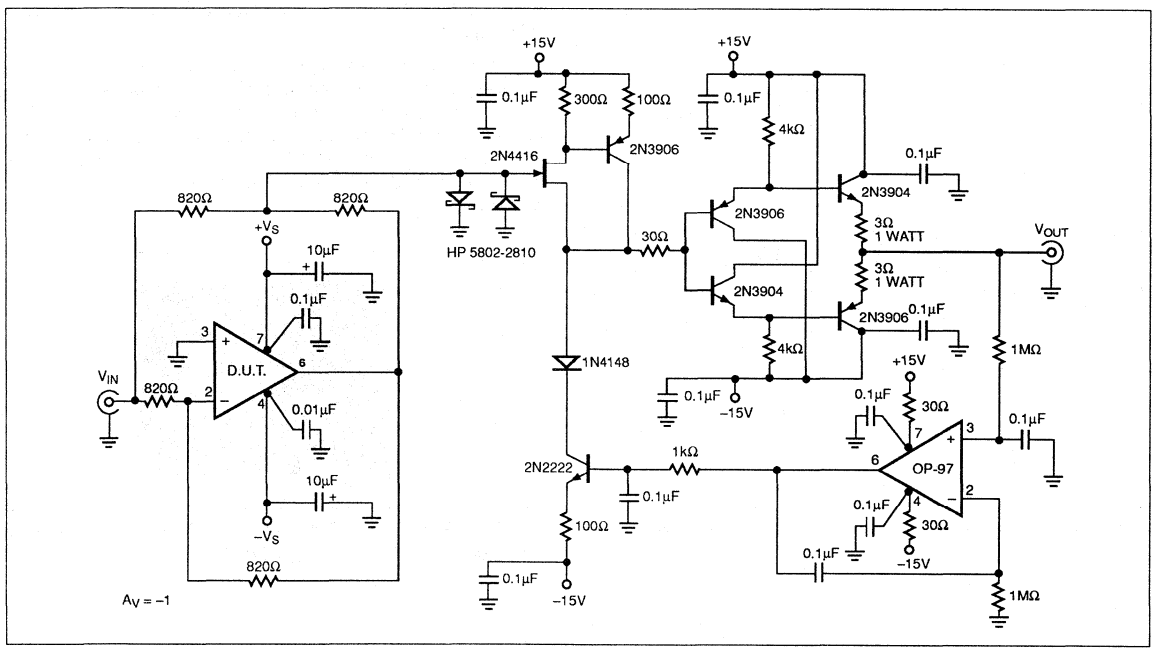


FIGURE 10: *High-Speed Settling Time Fixture (for 0.1 and 0.01%)*

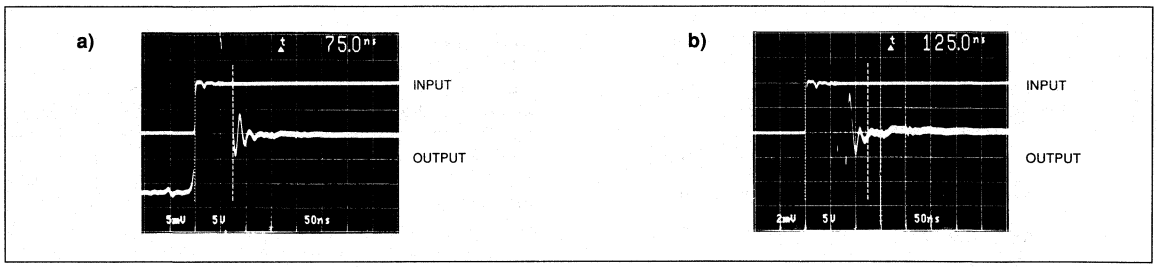


FIGURE 11: *Settling Time Performance of the OP-160 to 0.1% (a) and 0.01% (b) $A_V = -1$*

SETTLING TIME

Settling time is the time between when the input signal begins to change and when the output permanently enters a prescribed error band. Figure 10 illustrates the artificial summing node test configuration, used to characterize the OP-160 settling time. The OP-160 is set in a gain of –1 with a 10V step input. The error bands on the output are 5mV and 0.5mV, respectively, for 0.1% and 0.01% accuracy.

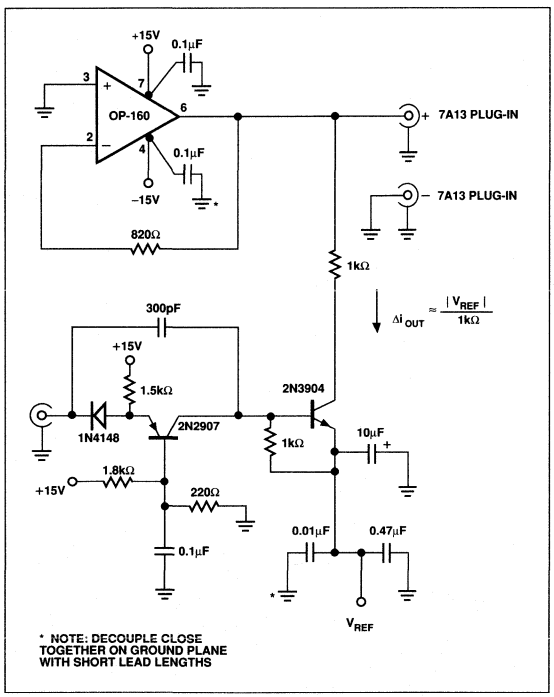


FIGURE 12: *Transient Output Impedance Test Fixture*

The test circuit, built on a copper clad circuit board, has a FET input stage which maintains extremely low loading capacitance at the artificial sum node. Preceding stages are complementary emitter follower stages, providing adequate drive current for a 50Ω oscilloscope input. The OP-97 establishes biasing for the input stage, and eliminates excessive offset voltage errors.

TRANSIENT OUTPUT IMPEDANCE

Settling characteristics of operational amplifiers also includes an amplifier's ability to recover, i.e., settle, from a transient current output load condition. An example of this includes an op amp driving the input from a SAR type A/D converter. Although the comparison point of the converter is usually diode clamped, the input swing of plus-and-minus a diode drop still gives rise to a significant modulation of input current. If the closed-loop output impedance is low enough and bandwidth of the amplifier is sufficiently large, the output will settle before the converter makes a comparison decision which will prevent linearity errors or missing codes.

Figure 12 shows a settling measurement circuit for evaluating recovery from an output current transient. An output disturbing current generator provides the transient change in output load current of 1mA. As seen in Figure 13, the OP-160 has extremely fast recovery of 80ns, (to 0.01%), for a 1mA load transient. The performance makes it an ideal amplifier for data acquisition systems.

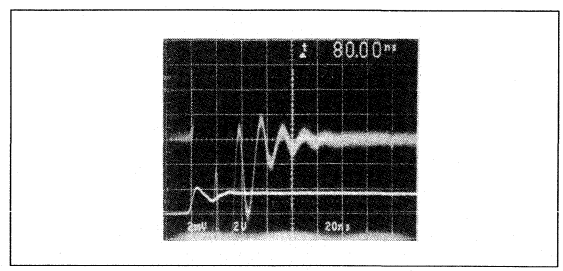


FIGURE 13: *OP-160's Extremely Fast Recovery Time from a 1mA Load Transient to 1mV (0.01%)*

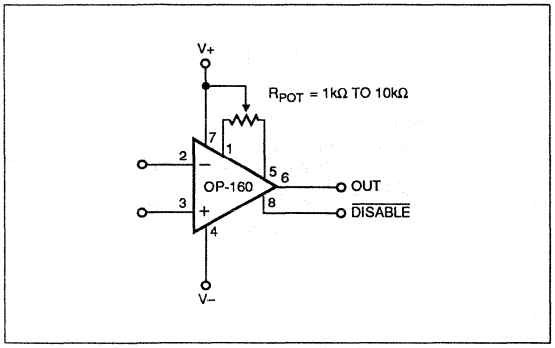


FIGURE 14: *Input Offset Voltage Nulling*

OFFSET VOLTAGE ADJUSTMENT

Offset voltage is adjusted with a 20kΩ potentiometer as shown in Figure 14. The potentiometer should be connected between pins 1 and 5 with its wiper connected to the V+ supply. The typical trim range is ±40mV.

$\overline{\text{DISABLE}}$ AMPLIFIER SHUTDOWN

Pin 8 of the OP-160, $\overline{\text{DISABLE}}$, is an amplifier shutdown control input. The OP-160 operates normally when Pin 8 is left floating. When greater than 1000µA is drawn from the $\overline{\text{DISABLE}}$ pin, the OP-160 is disabled. To draw current from the $\overline{\text{DISABLE}}$ pin, an open collector output logic gate or a discrete NPN transistor can be used as shown in Figure 15. An internal resistor limits the $\overline{\text{DISABLE}}$ current to around 500µA if the $\overline{\text{DISABLE}}$ pin is grounded with the OP-160 powered by ±15V supplies. These logic interface methods have the added advantage of level shifting the TTL signal to whatever supply voltage is used to power the OP-160.

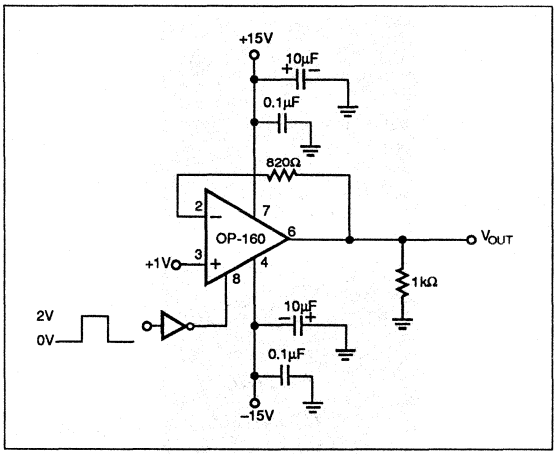


FIGURE 16: *$\overline{\text{DISABLE}}$ Turn-On/Turn-Off Test Circuit*

In the $\overline{\text{DISABLE}}$ mode, the OP-160 maintains 40dB of input-to-output isolation if the input signal remains below ±1.5V. Output resistance is very high, over 100kΩ, if the output is driven by signals of less than ±1.5V. Higher signals will be distorted.

Figure 16 shows a test circuit for measuring the turn-on and turn-off times for the OP-160. The OP-160 is in a gain of +1 with a +1V DC input. As the input pulse to the inverter rises its output falls, drawing current from the $\overline{\text{DISABLE}}$ pin and disabling the

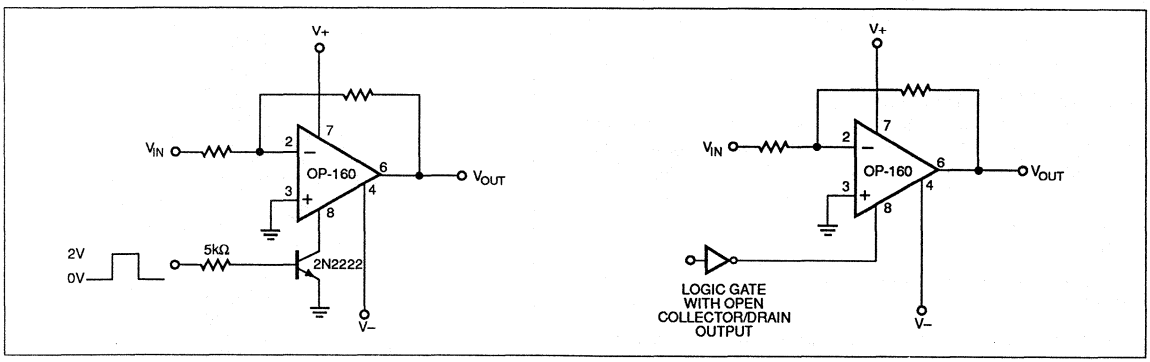


FIGURE 15: *Simple circuits allow the OP-160 to be shut down.*

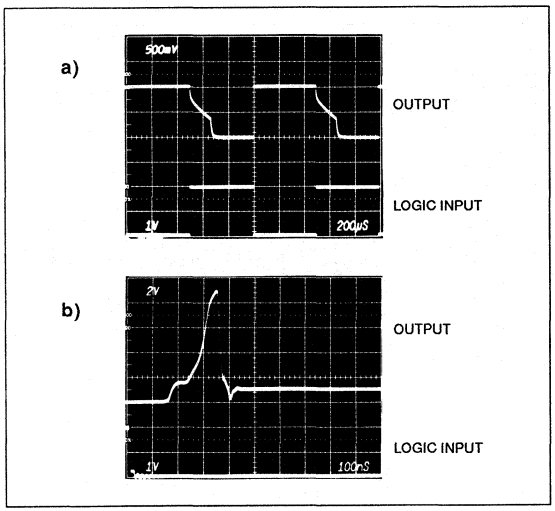


FIGURE 17: *(a) OP-160 turn-on and turn-off performance. (b) Expanded scale showing turn-on performance of the OP-160. Be aware of the high-frequency spike during turn-on.*

amplifier. The output voltage delay is shown in Figure 17 and takes 200µs to reach ground. The turn-on time is much quicker than the turn-off time. In this situation as the input to the inverter falls its output rises, returning the OP-160 to normal operation. The amplifier's output reaches its proper output voltage in 450ns.

OVERDRIVE RECOVERY

Figure 19 shows the overdrive recovery performance of the OP-160. Typical recovery time is 120ns from positive and negative overdrive.

APPLICATIONS

NONINVERTING AMPLIFIER

The OP-160 can be used as a voltage-follower or noninverting amplifier as shown in Figure 20. A current feedback amplifier in this configuration yields the same transfer function as a voltage feedback op amp:

$$\frac{V_{OUT}}{V_{IN}} = 1 + \frac{R_2}{R_1}$$

Remember to use a 820Ω feedback resistor in voltage-follower applications.

In noninverting applications, stray capacitance at the inverting input of a current feedback amplifier will cause peaking which will increase as the closed-loop gain decreases. The gain setting resistor, R_1, is in parallel with this stray capacitance creating a zero in the

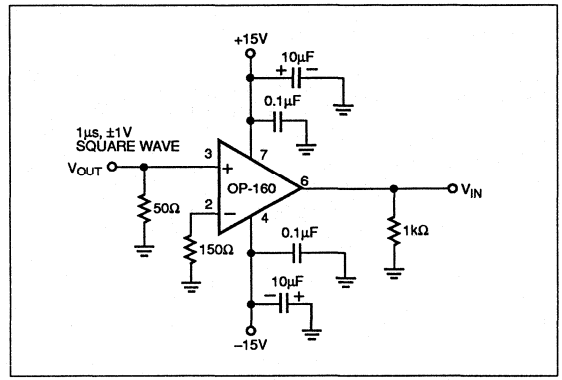


FIGURE 18: *Overdrive Recovery Test Circuit*

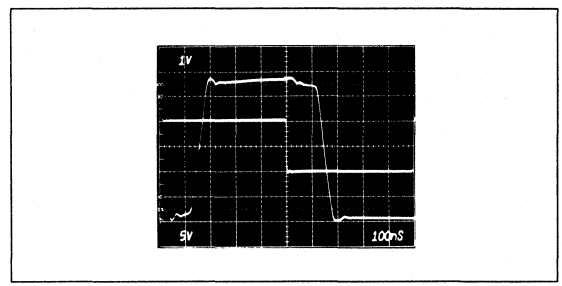


FIGURE 19: *The OP-160 recovers from both positive and negative overdrive in 120ns.*

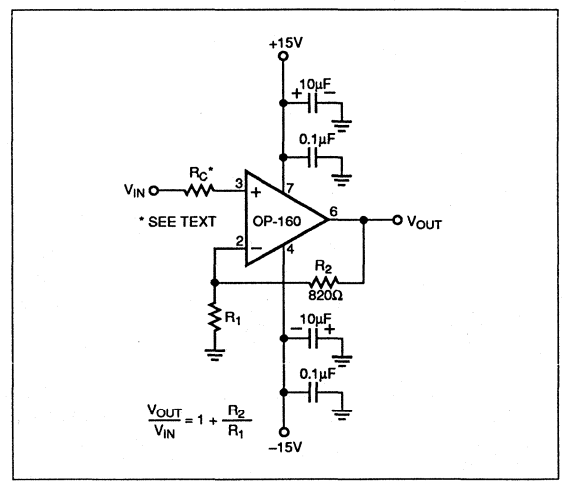


FIGURE 20: *The OP-160 as a voltage follower or noninverting amplifier.*

closed-loop response. For large noninverting gains, R_1 is small, creating a very high-frequency open-loop pole which has limited effect on the closed-loop response. As the noninverting gain is decreased, R_1 becomes larger and the stray zero becomes lower in frequency, having a much greater effect on the closed-loop response. To reduce peaking at low noninverting gains, place a series resistor, R_C, in series with the noninverting input as shown in Figure 20. This resistor combines with the stray capacitance at the noninverting input to form a low-pass filter that will reduce the peaking. The value of R_C should be determined experimentally in the actual PCB layout. Less peaking will occur in inverting gain configurations since the inverting input is a virtual ground which forces a constant voltage across the stray capacitance.

A common practice to stabilize voltage feedback op amps is to use a capacitor across the feedback resistance. This creates a zero in the voltage feedback amplifier response to offset the loss of phase margin due to a parasitic pole. In current feedback amplifiers, this technique will cause the amplifier to become unstable because the closed-loop bandwidth will increase beyond the stable operating frequency.

INVERTING AMPLIFIER

The OP-160 is also capable of operation as an inverting amplifier (see Figure 21). The transfer function of this circuit is identical to that using a voltage feedback op amp:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_2}{R_1}$$

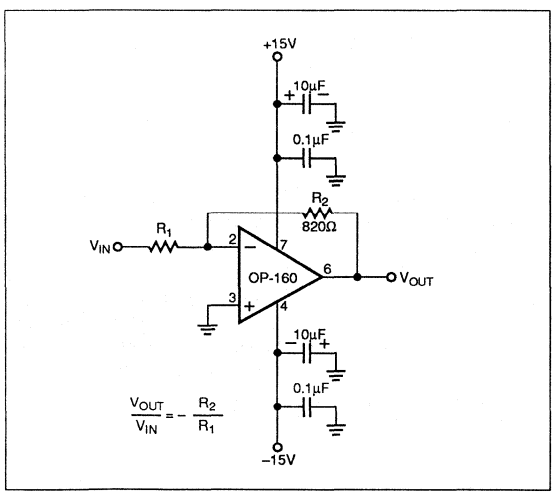


FIGURE 21: *The OP-160 as an inverting amplifier.*

USING CURRENT FEEDBACK OP AMPS IN INTEGRATOR APPLICATIONS

The small-signal model of a current feedback op amp shown earlier in Figure 3 assumes a non-varying value of feedback impedance. A non-varying feedback impedance ensures that the bandwidth of the amplifier does not extend beyond its 180° phase shift point and create unwanted oscillations. In integrator circuits, the feedback element is a capacitor whose impedance does vary with frequency. By definition then, integrator applications using current feedback amplifiers should be unstable. However, a simple trick, shown in Figure 22, enables high-speed, wide bandwidth current feedback op amps to be used in integrator applications.

Resistor R_F is placed between an artificial sum node and the inverting input of the amplifier. This resistor maintains a minimum value of feedback impedance over all frequencies. At high signal frequencies, the integrator capacitor, C_1, is a short circuit; the feedback impedance is equal to R_F only and the amplifier has maximum bandwidth. At low frequencies, C_1 adds to the overall feedback impedance. This lowers the amplifier's bandwidth but not enough to affect the integrator's performance.

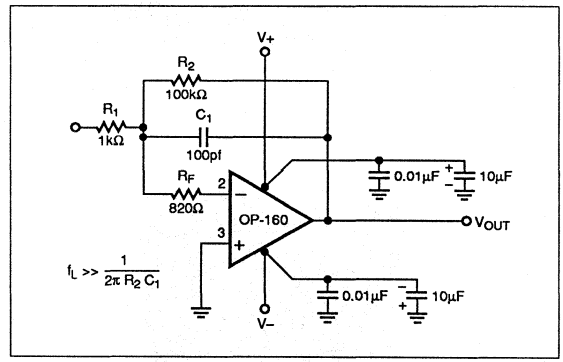


FIGURE 22: *An Integrator Using a Current Feedback Op Amp*

Figure 23 shows the gain and phase performance of the integrator. The integrator has the desired one-pole response for signal frequencies

$f_C >> 1/(2\pi R_2 C_1) \approx 16kHz.$

A more strenuous test of integrator performance is the pulse response. Ideally, this should be a linear ramp. The current feedback integrator's pulse response is exhibited in Figure 24. The response closely approximates the ideal linear ramp.

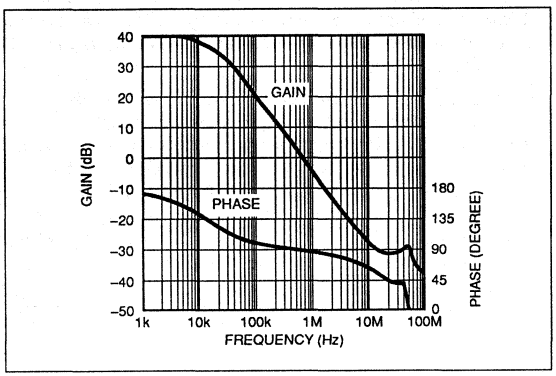


FIGURE 23: *Gain and phase response of the integrator shows a one-pole response.*

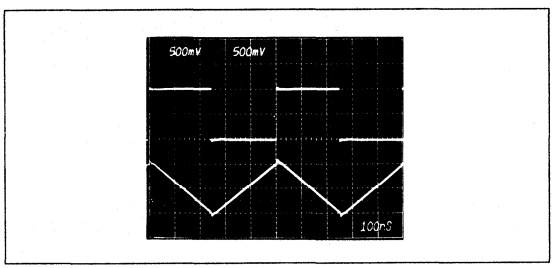


FIGURE 24: *Pulse response of the current feedback integrator. f = 2MHz.*

ACHIEVING FLAT GAIN RESPONSE WITH CURRENT FEEDBACK OP AMPS

In high-performance systems, flat gain response is often required. Current feedback op amps provide wide bandwidth performance but even these may not fulfill the gain flatness requirements of some systems.

Current feedback op amps exhibit both gain roll-off and peaking as shown in Figure 25. Peaking is primarily due to parasitic

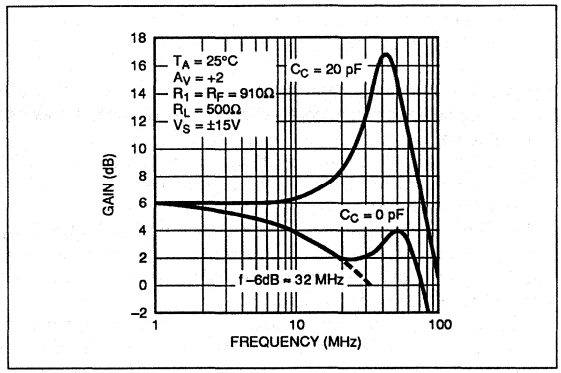


FIGURE 25: *Gain roll-off and peaking of current feedback amplifiers is dependent upon a number of factors including loading and parasitic capacitance.*

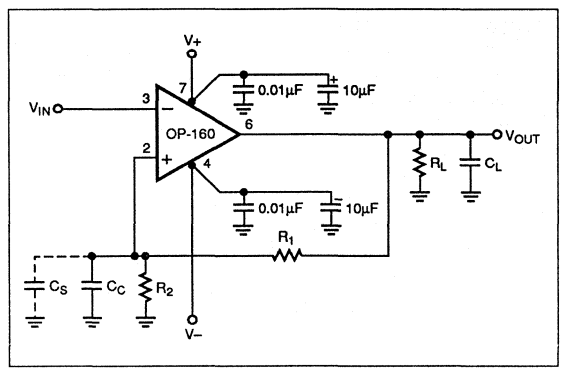


FIGURE 26: *A current feedback op amp configured for noninverting gain. Parasitic capacitances affecting gain are also shown.*

capacitance; gain roll-off is determined by the amount and type of load on the amplifier. Peaking is controlled by careful layout and circuit design; however, its cause can provide a method of improving gain flatness over a desired frequency range.

Consider the noninverting amplifier of Figure 26. The gain equals:

$$1 + \frac{R_2}{R_1 // Z_{(C_C // C_S)}},$$

and at low frequencies

$$A_V = 1 + \frac{R_2}{R_1} = 1 + \frac{910\Omega}{910\Omega} = 2$$

At higher frequencies the gain increases or peaks due to the effect of the parasitic capacitance, C_S, on the gain equation. Any capacitance at the inverting input will create a zero in the amplifier's response. This fact can be used to compensate for gain roll-off due to loading on the amplifier.

Begin by measuring or estimating the amplifier's –6dB point (this is the frequency at which the output signal is half its original amplitude). This can be easily determined from a network analyzer plot of the amplifier's frequency performance. From this the amount of capacitance, C_C, which will double the gain at the –6dB frequency and restore the original gain, can be determined.

From the –6dB frequency, C_C can be calculated:

$$C_C = C_S + \frac{1}{2\pi R_1 f_{-6dB}} + \frac{1}{2\pi R_2 f_{-6dB}}$$

for noninverting configuration, where C_S is the combination of the amplifier's input capacitance and the stray capacitance at the input.

In the example shown,

C_S = 9pF = OP-160 input capacitance (4pF) + stray capacitance (5pF)

$$C_S = 9pF + \frac{1}{2\pi(910\Omega)32MHz} + \frac{1}{2\pi(910\Omega)32MHz}$$

≈ 20pF

Figure 27 is an expanded scale plot of the gain performance of the compensated amplifier at A_V = +2. Gain performance is flat to ±0.1dB out to beyond 9MHz. For low gains ($A_V \leq 5$) peaking will be increased. At higher gains, gain flatness can be significantly improved without gain peaking. Figure 28 depicts the OP-160 with A_V = +10. In this example $f_{-6dB} \approx 22$ MHz so,

$$C_S = 9pF + \frac{1}{2\pi(91\Omega)22MHz} + \frac{1}{2\pi(820\Omega)22MHz}$$

= 97pF

The nearest standard capacitor value is 100pF.

Gain performance is flat to 0.5dB to 30MHz and the amplifier's –3dB point is 38MHz. This gives the amplifier an effective gain-bandwidth of 380MHz! Compensating the OP-160 does not effect the pulse response as shown in Figure 29.

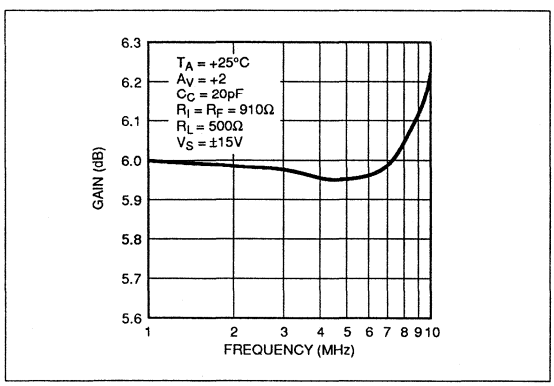


FIGURE 27: *Expanded Gain/Frequency Graph of the Compensated Amplifier, A_V = +2*

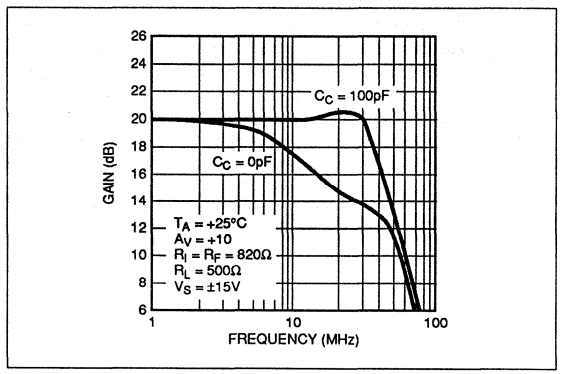


FIGURE 28: *Gain/frequency graph for the compensated amplifier, A_V = +10, showing the effect of the compensation capacitance, C_C, on gain flatness.*

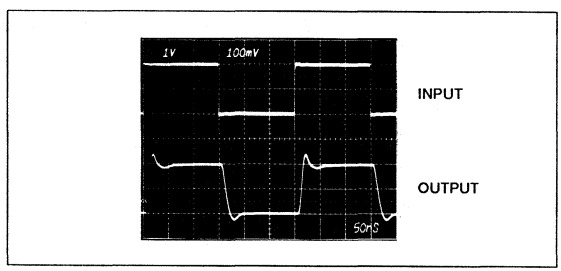


FIGURE 29: *Pulse Response of the OP-160 in a Gain of +10 Compensated for Gain Flatness*

OP-160 SPICE MACRO-MODEL

Figures 30 and 31 show the SPICE macro-model for the OP-160 high-speed, current feedback operational amplifier. This model was tested with, and is compatible with PSpice* and HSpice**. The schematic and net-list are included here so that the model can easily be used. This model uses a unique current feedback topology to accurately model both the AC and DC characteristics of the OP-160. In addition, this model can accommodate any number of poles and zeros to further shape the AC response.

The OP-160 SPICE macro-model uses four BJT transistors to create the input buffer as in the actual device. However, the rest of the model contains only ideal linear elements and ideal diodes to model the OP-160's behavior. Using only four transistors reduces simulation time and simplifies model development. It simulates important DC parameters such as V_{OS}, I_B, CMR, V_O and I_{SY}. AC parameters such as slew rate, open-loop transimpedance and phase response and CMR changes with frequency are also simulated by the model. In addition, the model includes the change in input bias current with varying common-mode and power supply voltages. Both output swing and supply current are accurately modelled.

One aspect of the OP-160's behavior is that slew rate varies with closed-loop gain. Slew rate of the basic model is set to the typical values for the OP-160 in a gain of +1. For other gains, the rising and falling slew rates can be adjusted by varying the values of V_1 and V_2 in the model. Slew rates for various gains can be determined from Figures 6a and 6b.

$$\text{Rising Slew Rate} = \frac{V_1 + 0.6V}{(1k\Omega)(5pF)}$$

$$\text{Falling Slew Rate} = \frac{V_2 + 0.6V}{(1k\Omega)(5pF)}$$

To keep the OP-160 model as simple as possible and thus save computer and development time, not all features of the op amp were modelled as listed below:

- PSR
- Crosstalk
- No limits on power supply voltages
- Maximum input voltage range
- Temperature effects (i.e., model parameters are assumed at 25°C)
- Input noise voltage and current sources
- Parameter variations for Monte Carlo analysis (i.e., all parameters are typical only)

These parameters are considered second-order effects and are not considered necessary for circuit simulation under normal operating conditions. However, users can easily add these functions as needed.

* PSpice is a registered trademark of MicroSim Corporation.
** HSPICE is a tradename of Meta-Software, Inc.

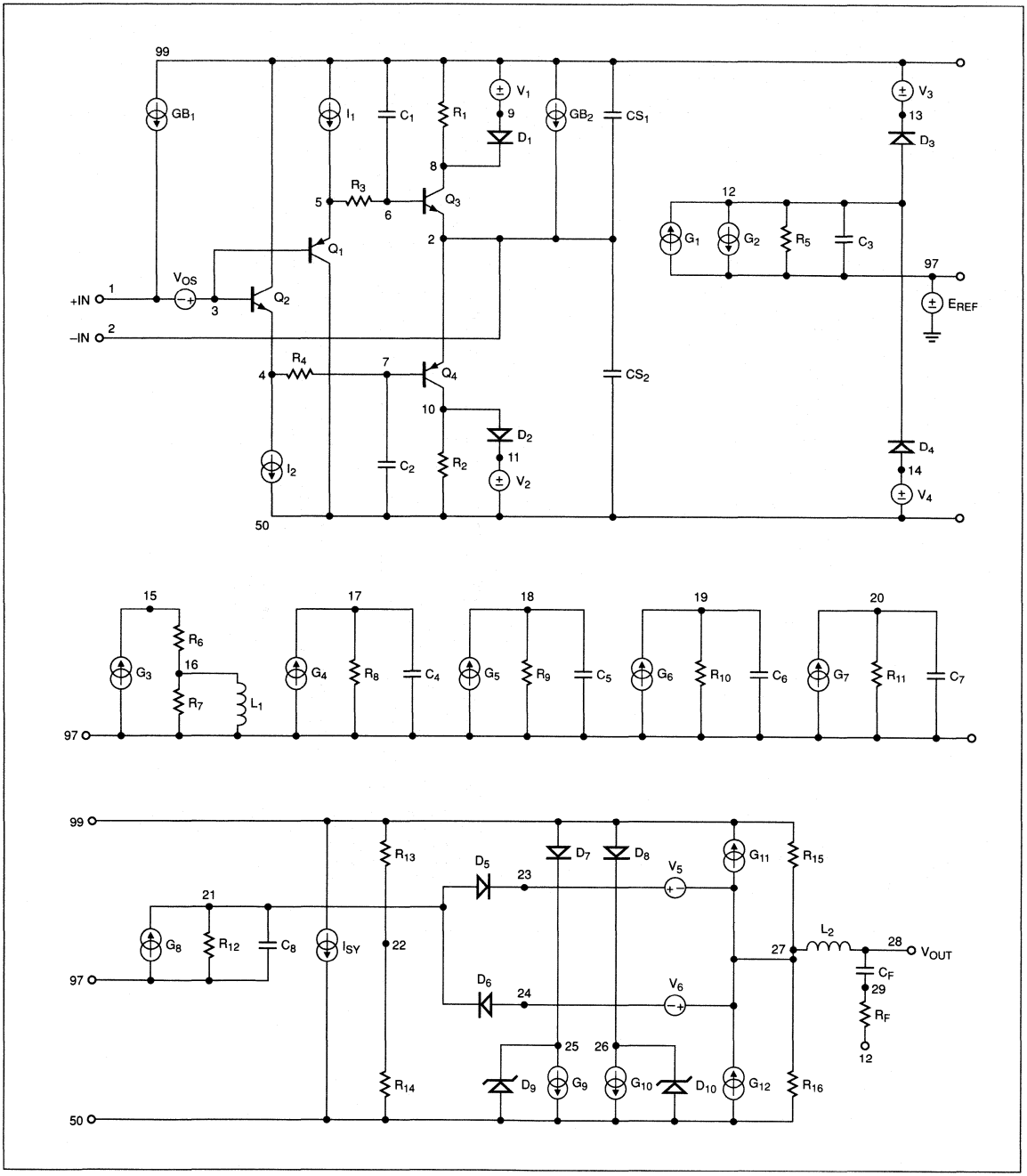


FIGURE 30: *OP-160 SPICE Model*

```
* OP-160 MACRO-MODEL © PMI 1990
*
* NODE ASSIGNMENTS
*                    NONINVERTING INPUT
*                    |  INVERTING INPUT
*                    |  |  OUTPUT
*                    |  |  |  POSITIVE SUPPLY
*                    |  |  |  |  NEGATIVE SUPPLY
*                    |  |  |  |  |
* SUBCKT OP-160  1  2  24  99  50
*
* INPUT STAGE
*
R1    99   8        1K
R2    10   50       1K
V1    99   9        9.4
D1    9    8        DX
V2    11   50       4.4
D2    10   11       DX
I1    99   5        125U
I2    4    50       125U
Q1    50   3    5   QP
Q2    99   3    4   QN
Q3    8    6    2   QN
Q4    10   7    2   QP
R3    5    6        143K
R4    4    7        143K
C1    99   6        0.0133P
C2    50   7        0.0133P
*
* INPUT ERROR SOURCES
*
GB1   99   1        POLY(1) 1  22  2E-7  4E-8
GB2   99   2        POLY(1) 1  22  6E-6  4E-8
VOS   3    1        1E-3
CS1   99   2        2.5E-12
CS2   50   2        2.5E-12
*
EREF  97   0        22  0  1
*
* GAIN STAGE & DOMINANT POLE
*
R5    12   97       5E6
C3    12   97       5P
G1    97   12       99  8  1E-3
G2    12   97       10  50  1E-3
V3    99   13       2.2
V4    14   50       2.2
D3    12   13       DX
D4    14   12       DX
CF    29   28       30P
RF    12   29       300
*
* ZERO/POLE PAIR AT 50MHZ/300MHZ
*
R6    15   16       1E6
L1    16   97       2.65E-3
R7    16   97       5E6
G3    97   15       12  22  1E-6
*
* POLE AT 300MHZ
*
R8    17   97       1E6
C4    17   97       0.531E-15
G4    97   17       15  22  1E-6
*
* POLE AT 300MHZ
*
R9    18   97       1E6
C5    18   97       0.531E-15
G5    97   18       17  22  1E-6
*
* POLE AT 500MHZ
*
R10   19   97       1E6
C6    19   97       0.318E-15
G6    97   19       18  22  1E-6
*
* POLE AT 500MHZ
*
R11   20   97       1E6
C7    20   97       0.318E-15
G7    97   20       19  22  1E-6
*
* POLE AT 500MHZ
*
R12   21   97       1E6
C8    21   97       0.318E-15
G8    97   21       20  22  1E-6
*
* OUTPUT STAGE
*
ISY   99   50       1.75E-3
R13   22   99       3.333E3
R14   22   50       3.333E3
R15   27   99       40
R16   27   50       40
L2    27   28       4E-8
G9    25   50       21  27  25E-3
G10   26   50       27  21  25E-3
G11   27   99       99  21  25E-3
G12   50   27       21  50  25E-3
V5    23   27       1.55
V6    27   24       1.55
D5    21   23       DX
D6    24   21       DX
D7    99   25       DX
D8    99   26       DX
D9    50   25       DY
D10   50   26       DY
*
* MODELS USED
*
.MODEL QN  NPN (BF=1E9 IS=1E-15 VAF=92)
.MODEL QP  PNP (BF=1E9 IS=1E-15 VAF=92)
.MODEL DX  D(IS=1E-15)
.MODEL DY  D(IS=1E-15 BV=50)
.ENDS OP-160
```

FIGURE 31: *OP-160 SPICE Net-List*

ANALOG DEVICES

Bipolar/JFET Audio Operational Amplifier

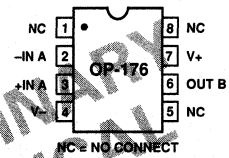
OP-176*

FEATURES
"Excellent Sonic Characteristics"
Low Noise: 5 nV/$\sqrt{Hz}$
Low Distortion: 0.0005%
High Slew Rate: 25 V/μs
Wide Bandwidth: 10 MHz
Low Supply Current: 2 mA/Amplifier
Low Offset Voltage: 1 mV
Unity-Gain Stable

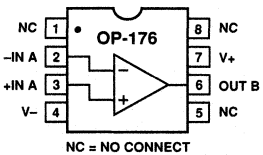
APPLICATIONS
High Performance Audio
Active Filters
Fast Amplifiers
Audio Line Drivers

PIN CONNECTIONS

8-Lead Narow-Body SOIC
(S Suffix)



8-Lead Epoxy DIP
(P Suffix)



PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The OP-176 is similar to the OP-275, but it has improved drive capability, short circuit protection and reduced noise. It features the Butler Amplifier front-end. This new front-end design combines the accuracy and low noise performance of bipolar transistors with the speed and sound quality of JFETs. This yields better THD and noise performance than previous audio amplifiers, at much lower supply currents.

The low offset voltage makes the OP-176 useful in summing applications. Low offsets reduce the need for offset adjust or for settling for limited headroom due to dc offsets. High output drive current with 50 mA short circuit limit is useful for applications that drive cables, especially where the possibility of shorting occurs.

The OP-176 is specified over the extended industrial (−40°C to +85°C) temperature range. OP-176s are available in plastic DIP and SOIC-8 surface mount packages.

*Patents pending.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

OP-176—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}				1	mV
Input Bias Current	I_B	V_{CM} = 0 V		200		nA
Input Offset Current	I_{OS}	V_{CM} = 0 V		10		nA
Input Voltage Range	V_{CM}		−12		+12	V
Common-Mode Rejection	CMR	V_{CM} = ±11 V	86			dB
Large Signal Voltage Gain	A_{VO}	R_L = 600 Ω		200		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			5		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 10 kΩ	−14		14	V
		R_L = 600 Ω, V_S = ±18 V		±17		V
Output Short Circuit Current	ISC			50		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±9 V to ±15 V		80		dB
Supply Current	I_{SY}	V_O = 0 V, R_L = ∞		2.2		mA
Supply Voltage Range	V_S		±4.5		±18	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		25		V/µs
Gain Bandwidth Product	GBP			10		MHz
Total Harmonic Distortion	THD	@ 20 kHz		0.001		%
		@ 1 kHz		0.0006		%
NOISE PERFORMANCE						
Voltage Noise	e_N p–p	0.1 Hz to 10 Hz		1.1		µV p–p
Voltage Noise Density	e_N	f = 30 Hz		6		nV/√Hz
Voltage Noise Density	e_N	f = 1 kHz		5		nV/√Hz
Current Noise Density	i_N	f = 1 kHz		1.1		pA/√Hz
Overshoot Factor		V_{IN} = 100 mV, A_{VD} = 1, R_L = 600 Ω, C_L = 100 pF		10		%

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . +22 V
Input Voltage[2] . . . . . ±18 V
Differential Input Voltage[2] . . . . . 36 V
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range
P, S Package . . . . . −65°C to +150°C
Operating Temperature Range
OP-176G . . . . . −40°C to +85°C
Junction Temperature Range
P, S Package . . . . . −65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C

Package Type	θ_{JA}[3]	θ_{JC}	Units
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.
[3]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered in circuit board for SOIC package.

ORDERING GUIDE

Model	Temperature Range	Package Option*
OP176GP	−40°C to +85°C	8-Pin Plastic DIP
OP176GS	−40°C to +85°C	8-Pin SOIC
OP176GBC	+25°C	DICE

*For outline information see Package Information section.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ANALOG DEVICES

Ultra-Precision Operational Amplifier

OP-177

FEATURES

- **Ultra-Low Offset Voltage**
  - T_A = 25°C ..... 10µV Max
  - −55°C ≤ T_A ≤ 125°C ..... 20µV Max
- **Outstanding Offset Voltage Drift** ..... 0.1µV/°C Max
- **Excellent Open-Loop Gain and Gain Linearity** ..... 12V /µV Typ
- **CMRR** ..... 130dB Min
- **PSRR** ..... 120dB Min
- **Low Supply Current** ..... 2.0 mA Max
- **Fits Industry Standard Precision Op Amp Sockets (OP07/OP77)**

ORDERING INFORMATION †

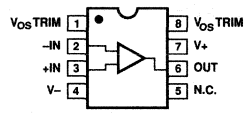
PACKAGE				OPERATING
CERDIP 8-PIN	PLASTIC 8-PIN	LCC 20-PIN	SO 8-PIN	TEMPERATURE RANGE
OP177AZ*	–	–	–	MIL
OP177BZ*	–	OP177BRC/883	–	MIL
OP177EZ	–	–	–	XIND
OP177FZ	OP177FP	–	–	XIND
OP177GZ	OP177GP	–	OP177GS	XIND

MIL = −55°C to +125°C XIND = −40°C to +85°C

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerDIP, plastic DIP, and TO-can packages.

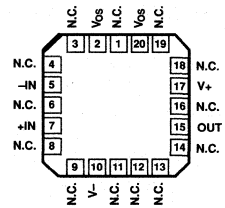
PIN CONNECTIONS



EPOXY MINI-DIP
(P-Suffix)

8-PIN HERMETIC DIP
(Z-Suffix)

8-PIN SO
(S-Suffix)



OP-177BRC/883
LCC
(RC-Suffix)

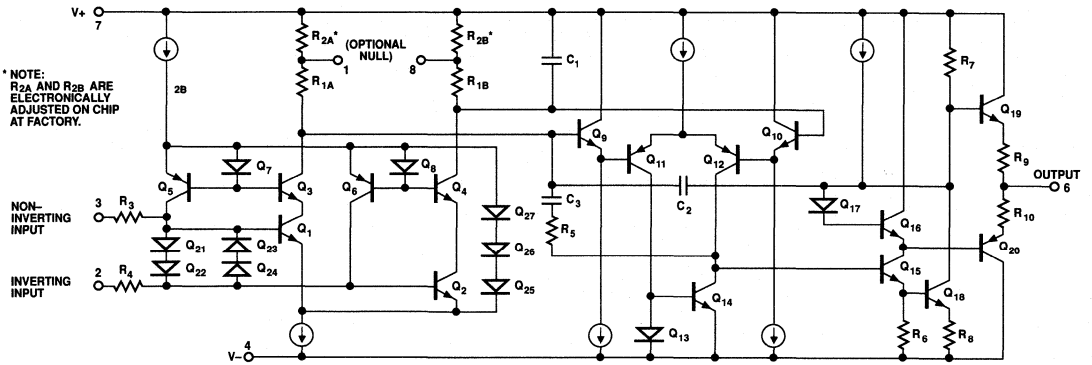
GENERAL DESCRIPTION

The OP-177 features the highest precision performance of any op amp currently available. Offset voltage of the OP-177 is only 10µV MAX at room temperature and 20µV MAX over the full military temperature range of −55°C to +125°C. The ultra-low V_{OS} of the OP-177, combines with its exceptional offset voltage drift (TCV_{OS}) of 0.1µV/°C MAX, to eliminate the need for external V_{OS} adjustment and increases system accuracy over temperature.

The OP-177's open-loop gain of 12V/µV is maintained over the full ±10V output range. CMRR of 130dB MIN, PSRR of 120dB MIN, and maximum supply current of 2mA are just a few examples of the excellent performance of this operational amplifier. The OP-177's combination of outstanding specifications insure accurate performance in high closed-loop gain applications.

This low noise bipolar input op amp is also a cost effective alternative to chopper-stabilized amplifiers. The OP-177 provides chopper-type performance without the usual problems of high noise, low frequency chopper spikes, large physical size, limited common-mode input voltage range, and bulky external storage capacitors.

Continued



GENERAL DESCRIPTION *Continued*

The OP-177 is offered in both the –55°C to +125°C military, and the –40°C to +85°C extended industrial temperature ranges. This product is available in 8-pin ceramic and epoxy DIPs, as well as the space saving 8-pin Small-Outline (SO) and the Leadless Chip Carrier (LCC) packages.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Differential Input Voltage ..... ±30V
Input Voltage (Note 1) ..... ±22V
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range
Z and RC Packages ..... –65°C to +150°C
P Package ..... –65°C to +125°C
Operating Temperature Range
OP-177A, OP-177B ..... –55°C to +125°C
OP-177E, OP-177F, OP-177G ..... –40°C to +85°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature (T_j) ..... –65°C to +150°C

PACKAGE TYPE	Θ_{JA} (NOTE 2)	Θ_{JC}	UNITS
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC (RC)	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-177A MIN	OP-177A TYP	OP-177A MAX	OP-177B MIN	OP-177B TYP	OP-177B MAX	UNITS
Input Offset Voltage	V_{OS}		–	4	10	–	10	25	µV
Long-Term Input Offset Voltage Stability	ΔV_{OS}/Time	(Note 1)	–	0.2	–	–	0.2	–	µV/Mo
Input Offset Current	I_{OS}		–	0.3	1.0	–	0.3	1.5	nA
Input Bias Current	I_B		–0.2	–	1.5	–0.2	–	2.0	nA
Input Noise Voltage	e_n	f_o = 1Hz to 100Hz (Note 2)	–	118	150	–	118	150	nV_{RMS}
Input Noise Current	i_n	f_o = 1Hz to 100Hz (Note 2)	–	3	8	–	3	8	pA_{RMS}
Input Resistance Differential-Mode	R_{IN}	(Note 3)	26	45	–	26	45	–	MΩ
Input Resistance Common-Mode	R_{INCM}		–	200	–	–	200	–	GΩ
Input Voltage Range	IVR	(Note 4)	±13	±14	–	±13	±14	–	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V	130	140	–	130	140	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	120	125	–	115	125	–	dB
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ, V_O = ±10V (Note 5)	5000	12000	–	5000	12000	–	V/mV
Output Voltage Swing	V_O	R_L ≥ 10kΩ R_L ≥ 2kΩ R_L ≥ 1kΩ	±13.5 ±12.5 ±12.0	±14.0 ±13.0 ±12.5	– – –	±13.5 ±12.5 ±12.0	±14.0 ±13.0 ±12.5	– – –	V
Slew Rate	SR	R_L ≥ 2kΩ (Note 2)	0.1	0.3	–	0.1	0.3	–	V/µs
Closed-Loop Bandwidth	BW	A_{VCL} = +1 (Note 2)	0.4	0.6	–	0.4	0.6	–	MHz
Open-Loop Output Resistance	R_O		–	60	–	–	60	–	Ω
Power Consumption	Pd	V_S = ±15V, No Load V_S = ±3V, No Load	– –	50 3.5	60 4.5	– –	50 3.5	60 4.5	mW
Supply Current	I_{SY}	V_S = ±15V, No Load	–	1.6	2.0	–	1.6	2.0	mA
Offset Adjustment Range		Rp = 20kΩ	–	±3	–	–	±3	–	mV

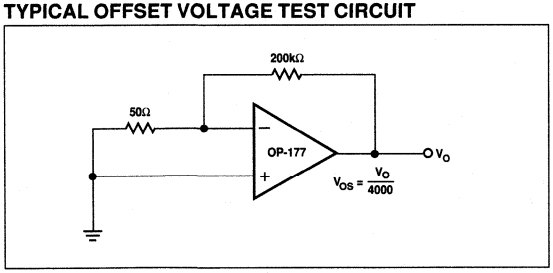
NOTES:
1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically less than 2.0µV.
2. Sample tested.
3. Guaranteed by design.
4. Guaranteed by CMRR test condition.
5. To insure high open-loop gain throughout the ±10V output range, A_{VO} is tested at $-10V \le V_O \le 0V$, $0V \le V_O \le +10V$, and $-10V \le V_O \le +10V$.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $-55°C \le T_A \le +125°C$, unless otherwise noted.

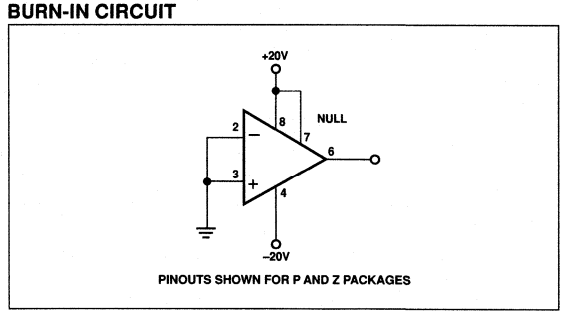
PARAMETER	SYMBOL	CONDITIONS	OP-177A MIN	OP-177A TYP	OP-177A MAX	OP-177B MIN	OP-177B TYP	OP-177B MAX	UNITS
Input Offset Voltage	V_{OS}		–	10	20	–	25	55	µV
Average Input Offset Voltage Drift	TCV_{OS}	(Note 1)	–	0.03	0.1	–	0.1	0.3	µV/°C
Input Offset Current	I_{OS}		–	0.5	1.5	–	0.5	2.0	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	–	1.5	25	–	1.5	25	pA/°C
Input Bias Current	I_B		–0.2	2.4	4	–0.2	2.4	4	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	–	8	25	–	8	25	pA/°C
Input Voltage Range	IVR	(Note 3)	±13	±13.5	–	±13	±13.5	–	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm13V$	120	140	–	120	140	–	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm3V$ to $\pm18V$	120	125	–	110	120	–	dB
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm10V$ (Note 4)	2000	6000	–	2000	6000	–	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12	±13.0	–	±12	±13.0	–	V
Power Consumption	P_d	$V_S = \pm15V$, No Load	–	60	75	–	60	75	mW
Supply Current	I_{SY}	$V_S = \pm15V$, No Load	–	2.0	2.5	–	2.0	2.5	mA

NOTES:
1. TCV_{OS} is 100% tested.
2. Guaranteed by end-point limits.
3. Guaranteed by CMRR test condition.
4. To insure high open-loop gain throughout the ±10V output range, A_{VO} is tested at $-10V \le V_O \le 0V$, $0V \le V_O \le +10V$, and $-10V \le V_O \le +10V$.

TYPICAL OFFSET VOLTAGE TEST CIRCUIT

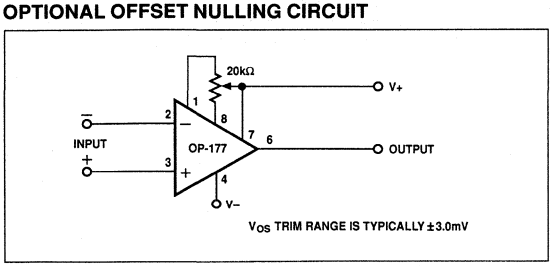


BURN-IN CIRCUIT



PINOUTS SHOWN FOR P AND Z PACKAGES

OPTIONAL OFFSET NULLING CIRCUIT



V_{OS} TRIM RANGE IS TYPICALLY ±3.0mV

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-177E MIN	OP-177E TYP	OP-177E MAX	OP-177F MIN	OP-177F TYP	OP-177F MAX	OP-177G MIN	OP-177G TYP	OP-177G MAX	UNITS
Input Offset Voltage	V_{OS}		–	4	10	–	10	25	–	20	60	µV
Long-Term V_{OS} Stability	V_{OS}/Time	(Note 1)	–	0.2	–	–	0.3	–	–	0.4	–	µV/Mo
Input Offset Current	I_{OS}		–	0.3	1.0	–	0.3	1.5	–	0.3	2.8	nA
Input Bias Current	I_B		–0.2	1.0	1.5	–0.2	1.2	2.0	–0.2	1.2	2.8	nA
Input Noise Voltage	e_n	f_o = 1Hz to 100Hz (Note 2)	–	118	150	–	118	150	–	118	150	nV_{RMS}
Input Noise Current	i_n	f_o = 1Hz to 100Hz (Note 2)	–	3	8	–	3	8	–	3	8	pA_{RMS}
Input Resistance – Differential-Mode	R_{IN}	(Note 3)	26	45	–	26	45	–	18.5	45	–	MΩ
Input Resistance – Common-Mode	R_{INCM}		–	200	–	–	200	–	–	200	–	GΩ
Input Voltage Range	IVR	(Note 4)	±13	±14	–	±13	±14	–	±13	±14	–	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V	130	140	–	130	140	–	115	140	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	120	125	–	115	125	–	110	120	–	dB
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ, V_O = ±10V (Note 5)	5000	12000	–	5000	12000	–	2000	6000	–	V/mV
Output Voltage Swing	V_O	R_L ≥ 10kΩ	±13.5	±14.0	–	±13.5	±14.0	–	±13.5	±14.0	–	V
		R_L ≥ 2kΩ	±12.5	±13.0	–	±12.5	±13.0	–	±12.5	±13.0	–	
		R_L ≥ 1kΩ	±12.0	±12.5	–	±12.0	±12.5	–	±12.0	±12.5	–	
Slew Rate	SR	R_L ≥ 2kΩ (Note 2)	0.1	0.3	–	0.1	0.3	–	0.1	0.3	–	V/µs
Closed-Loop Bandwidth	BW	A_{VCL} = +1 (Note 2)	0.4	0.6	–	0.4	0.6	–	0.4	0.6	–	MHz
Open-Loop Output Resistance	R_O		–	60	–	–	60	–	–	60	–	Ω
Power Consumption	P_d	V_S = ±15V, No Load	–	50	60	–	50	60	–	50	60	mW
		V_S = ±3V, No Load	–	3.5	4.5	–	3.5	4.5	–	3.5	4.5	
Supply Current	I_{SY}	V_S = ±15V, No Load	–	1.6	2.0	–	1.6	2.0	–	1.6	2.0	mA
Offset Adjustment Range		R_P = 20kΩ	–	±3	–	–	±3	–	–	±3	–	mV

NOTES:

1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically less than 2.0µV.
2. Sample tested.
3. Guaranteed by design.
4. Guaranteed by CMRR test condition.
5. To insure high Open-loop gain throughout the ±10V output range, A_{VO} is tested at $-10V \le V_O \le 0V$, $0V \le V_O \le +10V$, and $-10V \le V_O \le +10V$.

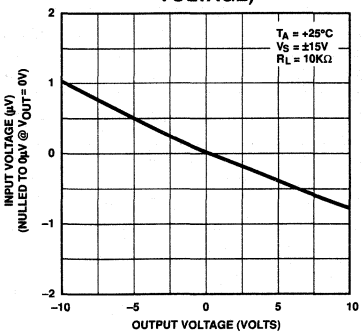
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-40°C \le T_A \le \pm 85°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-177E MIN	OP-177E TYP	OP-177E MAX	OP-177F MIN	OP-177F TYP	OP-177F MAX	OP-177G MIN	OP-177G TYP	OP-177G MAX	UNITS
Input Offset Voltage	V_{OS}		–	10	20	–	15	40	–	20	100	µV
Average Input Offset Voltage Drift	TCV_{OS}	(Note 1)	–	0.03	0.1	–	0.1	0.3	–	0.7	1.2	µV/°C
Input Offset Current	I_{OS}		–	0.5	1.5	–	0.5	2.2	–	0.5	4.5	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	–	1.5	25	–	1.5	40	–	1.5	85	pA/°C
Input Bias Current	I_B		–0.2	2.4	4.0	–0.2	2.4	4.0	–	2.4	±6.0	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	–	8	25	–	8	40	–	15	60	pA/°C
Input Voltage Range	IVR	(Note 3)	±13.0	±13.5	–	±13.0	±13.5	–	±13.0	±13.5	–	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	120	140	–	120	140	–	110	140	–	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	120	125	–	110	120	–	106	115	–	dB
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$ $V_O = \pm 10V$	2000	6000	–	2000	6000	–	1000	4000	–	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12.0	±13.0	–	±12.0	±13.0	–	±12.0	±13.0	–	V
Power Consumption	P_d	$V_S = \pm 15V$, No Load	–	60	75	–	60	75	–	60	75	mW
Supply Current	I_{SY}	$V_S = \pm 15V$, No Load	–	2.0	2.5	–	2.0	2.5	–	2.0	2.5	mA

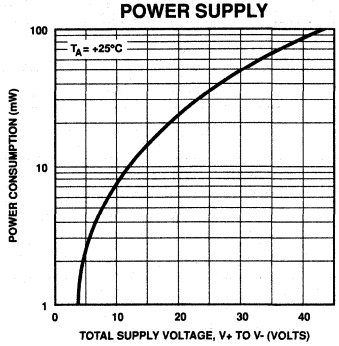
NOTES:
1. OP177E and OP177F: TCV_{OS} is 100% tested.
2. Guaranteed by end-point limits.
3. Guaranteed by CMRR test condition.
4. To insure high open-loop gain throughout the ±10V output range, A_{VO} is tested at $-10V \le V_O \le 0V$, $0V \le V_O \le +10V$, and $-10V \le V_O \le +10V$.

TYPICAL PERFORMANCE CHARACTERISTICS

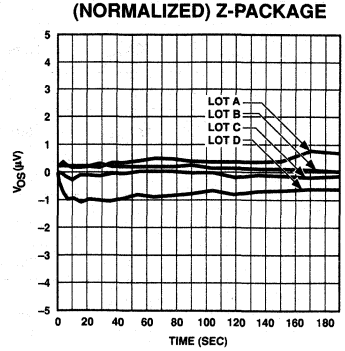
GAIN LINEARITY (INPUT VOLTAGE vs OUTPUT VOLTAGE)



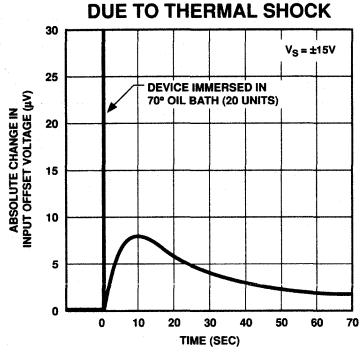
POWER CONSUMPTION vs POWER SUPPLY



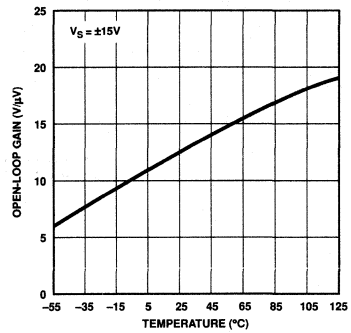
WARM-UP V_{OS} DRIFT (NORMALIZED) Z-PACKAGE



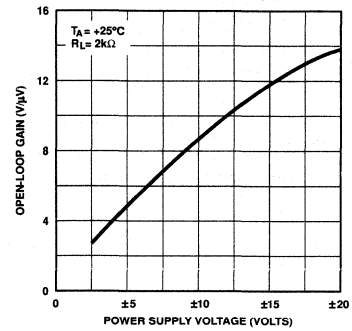
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



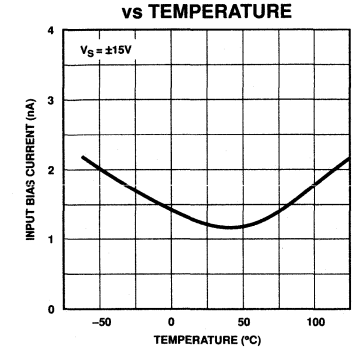
OPEN-LOOP GAIN vs TEMPERATURE



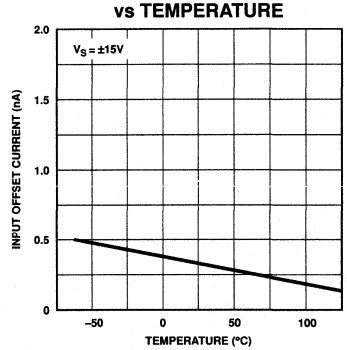
OPEN-LOOP GAIN vs POWER SUPPLY VOLTAGE



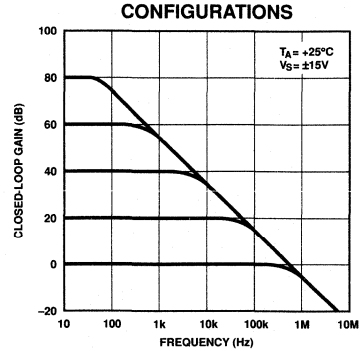
INPUT BIAS CURRENT vs TEMPERATURE



INPUT OFFSET CURRENT vs TEMPERATURE

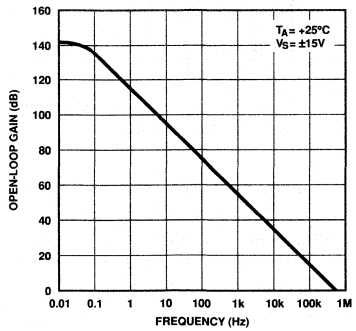


CLOSED-LOOP RESPONSE FOR VARIOUS GAIN CONFIGURATIONS

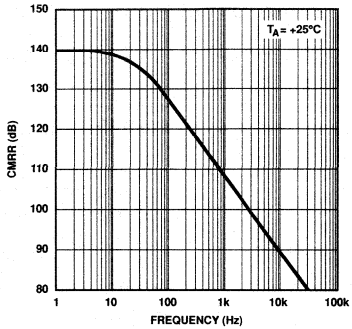


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

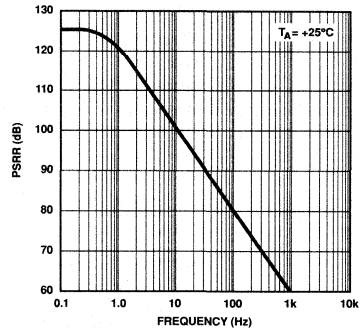
OPEN-LOOP FREQUENCY RESPONSE



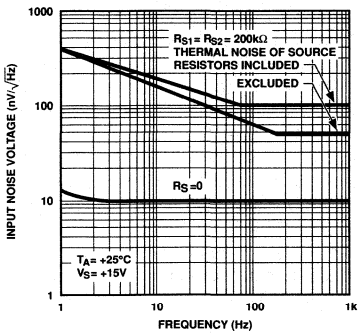
CMRR vs FREQUENCY



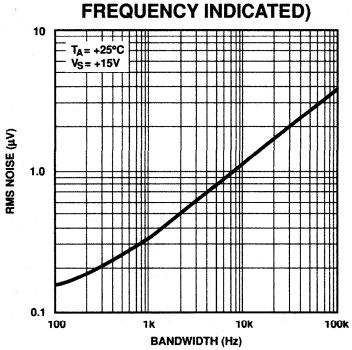
PSRR vs FREQUENCY



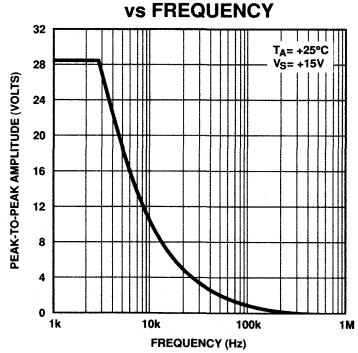
TOTAL INPUT NOISE VOLTAGE vs FREQUENCY



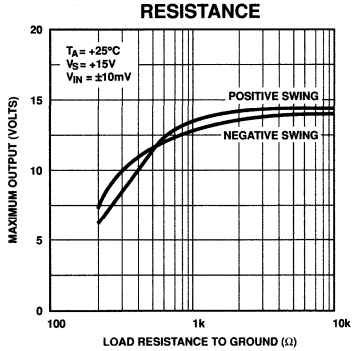
INPUT WIDEBAND NOISE vs BANDWIDTH (0.1 Hz TO FREQUENCY INDICATED)



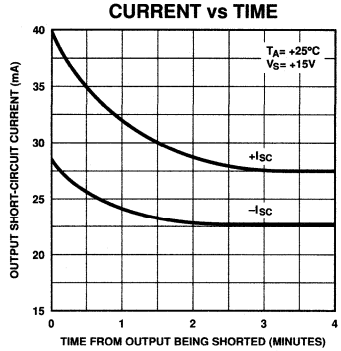
MAXIMUM OUTPUT SWING vs FREQUENCY



MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



OUTPUT SHORT-CIRCUIT CURRENT vs TIME



APPLICATIONS INFORMATION

GAIN LINEARITY

The actual open-loop gain of most monolithic op amps varies at different output voltages. This nonlinearity causes errors in high closed-loop gain circuits.

It is important to know that the manufacturer's A_{VO} specification is only a part of the solution, since all automated testers use end-point testing and therefore only show the average gain. For example, Figure 1 shows a typical precision op amp with a respectable open-loop gain of 650V/mV. However, the gain is not constant through the output voltage range, causing nonlinear errors. An ideal op amp would show a horizontal scope trace.

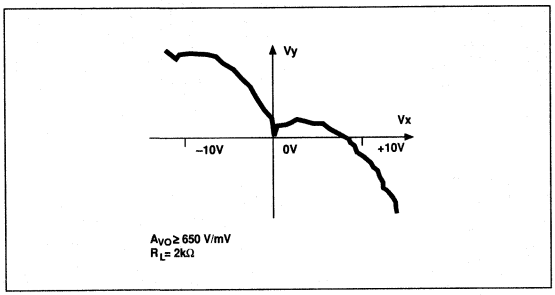


FIGURE 1: *Typical Precision Op-Amp*

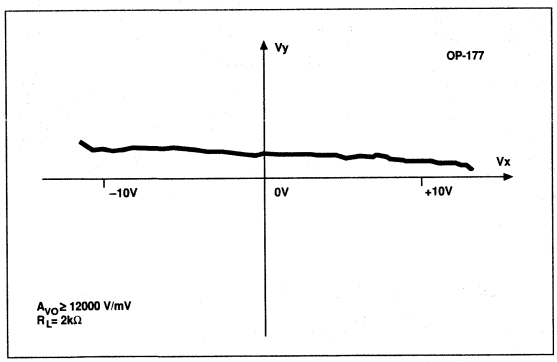


FIGURE 2: *OP-177's Output Gain Linearity Trace*

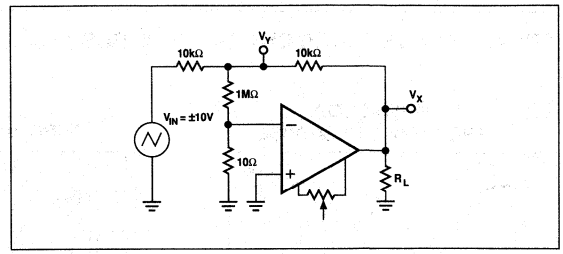


FIGURE 3: *Open-Loop Gain Linearity Test Circuit*

Figure 2 shows the OP-177's output gain linearity trace with its truly impressive average A_{VO} of 12000V/mV. The output trace is virtually horizontal at all points, assuring extremely high gain accuracy. PMI also performs additional testing to insure consistent high open-loop gain at various output voltages.

Figure 3 is a simple open-loop gain test circuit for your own evaluation.

THERMOCOUPLE AMPLIFIER WITH COLD-JUNCTION COMPENSATION

An example of a precision circuit is a thermocouple amplifier that must amplify very low level signals accurately without introducing linearity and offset errors to the circuit. In this circuit, an S-type thermocouple, which has a Seebeck coefficient of 10.3μV/°C, produces 10.3mV of output voltage at a temperature of 1,000°C. The amplifier gain is set at 973.16. Thus, it will produce an output voltage of 10.024V. Extended temperature ranges to beyond 1,500°C can be accomplished by reducing the amplifier gain. The circuit uses a low-cost diode to sense the temperature at the terminating junctions and in turn compensates for any ambient temperature change. The OP-177, with its high open-loop gain, plus low offset voltage and drift combines to yield a very precision temperature sensing circuit. Circuit values for other thermocouple types are shown in Table 1.

TABLE 1

THERMOCOUPLE TYPE	SEEBECK COEFFICIENT	R_1	R_2	R_7	R_9
K	39.2μV/°C	110Ω	5.76kΩ	102kΩ	269kΩ
J	50.2μV/°C	100Ω	4.02kΩ	80.6kΩ	200kΩ
S	10.3μV/°C	100Ω	20.5kΩ	392kΩ	1.07MΩ

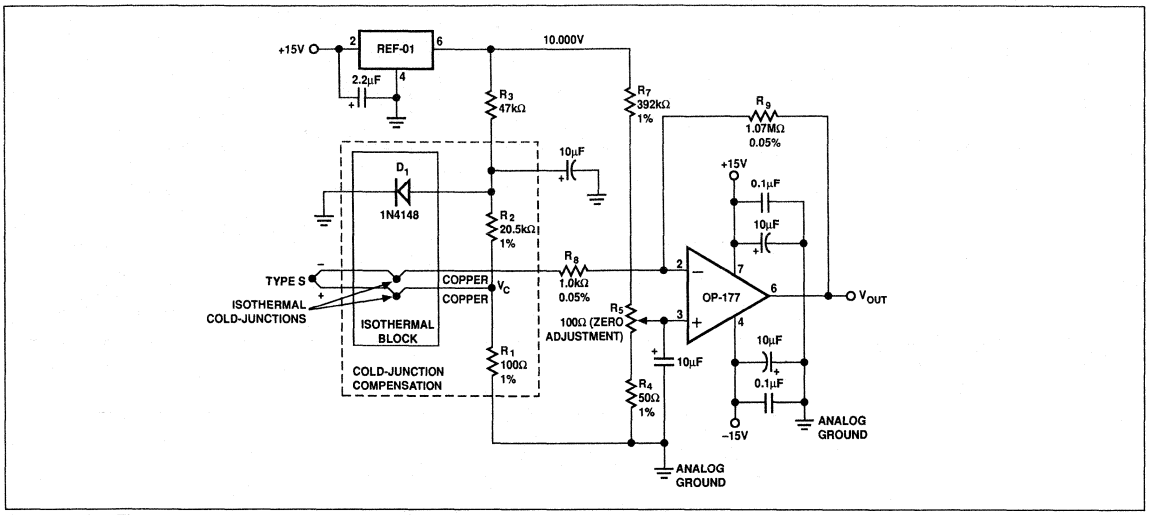


FIGURE 4: *Thermocouple Amplifier with Cold-Junction Compensation*

PRECISION HIGH-GAIN DIFFERENTIAL AMPLIFIER

The high gain, gain linearity, CMRR, and low TCV_{OS} of the OP-177 make it possible to obtain performance not previously available in single stage, very high-gain amplifier applications. See Figure 5.

For best CMR, $\frac{R_1}{R_2}$ must equal $\frac{R_3}{R_4}$. In this example,

with a 10mV differential signal, the maximum errors are as listed in Table 2.

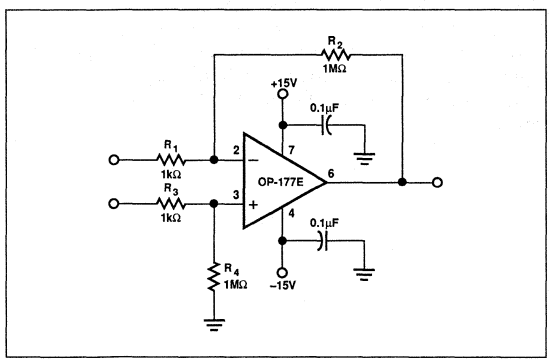


FIGURE 5: *Precision High-Gain Differential Amplifier*

TABLE 2: High Gain Differential Amp Performance

TYPE	AMOUNT
COMMON-MODE VOLTAGE	0.1%/V
GAIN LINEARITY, WORST CASE	0.02%
TCV_{OS}	0.0003%/°C
TCI_{OS}	0.008%/°C

ISOLATING LARGE CAPACITIVE LOADS

The circuit in Figure 6 reduces maximum slew-rate but allows driving capacitive loads of any size without instability. Because the 100Ω resistor is inside the feedback loop, its effect on output impedance is reduced to insignificance by the high open-loop gain of the OP-177.

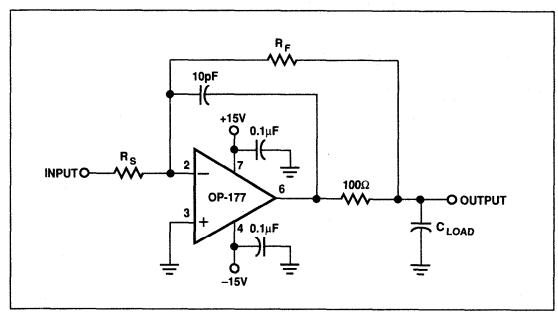


FIGURE 6: *Isolating Capacitive Loads*

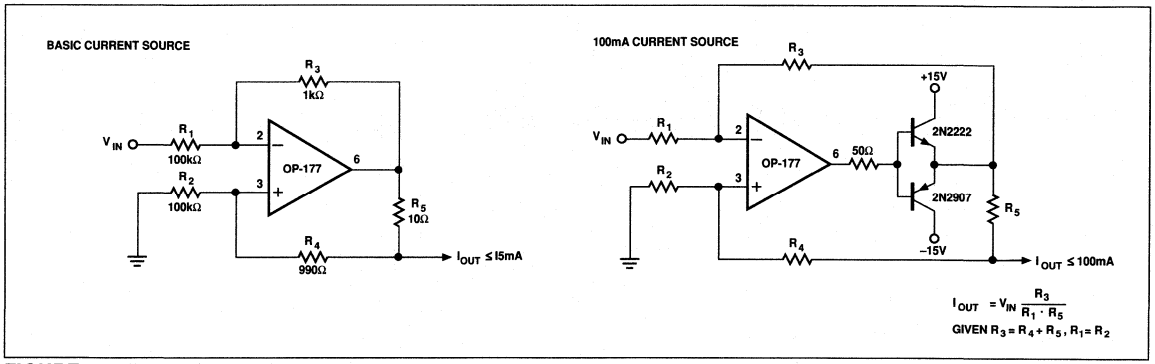


FIGURE 7: *Bilateral Current Source*

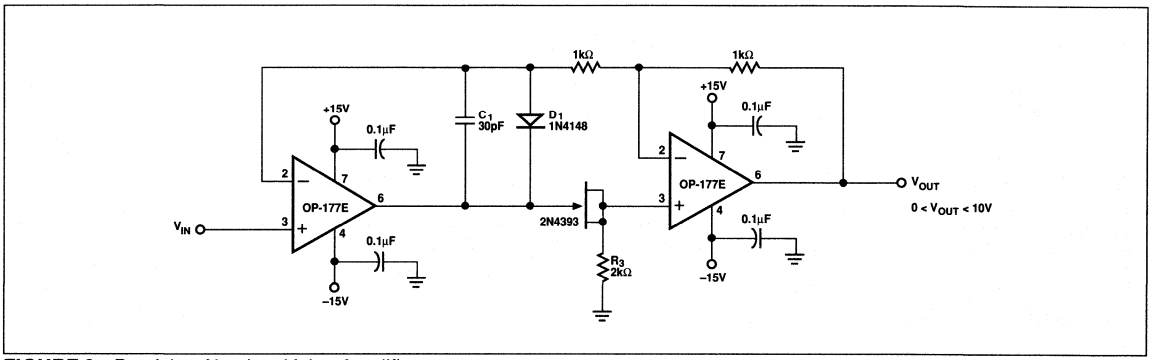


FIGURE 8: *Precision Absolute Value Amplifier*

BILATERAL CURRENT SOURCE

The current sources shown in Figure 7 will supply both positive and negative current into a grounded load.

Note that $Z_O = \dfrac{R_5\left(\dfrac{R_4}{R_2}+1\right)}{\dfrac{R_5+R_4}{R_2}-\dfrac{R_3}{R_1}}$

and that for Z_O to be infinite,

$\dfrac{R_5+R_4}{R_2}$ must $= \dfrac{R_3}{R_1}$

PRECISION ABSOLUTE VALUE AMPLIFIER

The high gain and low TCV_{OS} assure accurate operation with inputs from microvolts to volts. In this circuit, the signal always appears as a common-mode signal to the op amps. The OP-177E CMRR of 140dB assures errors of less than 1ppm. See Figure 8.

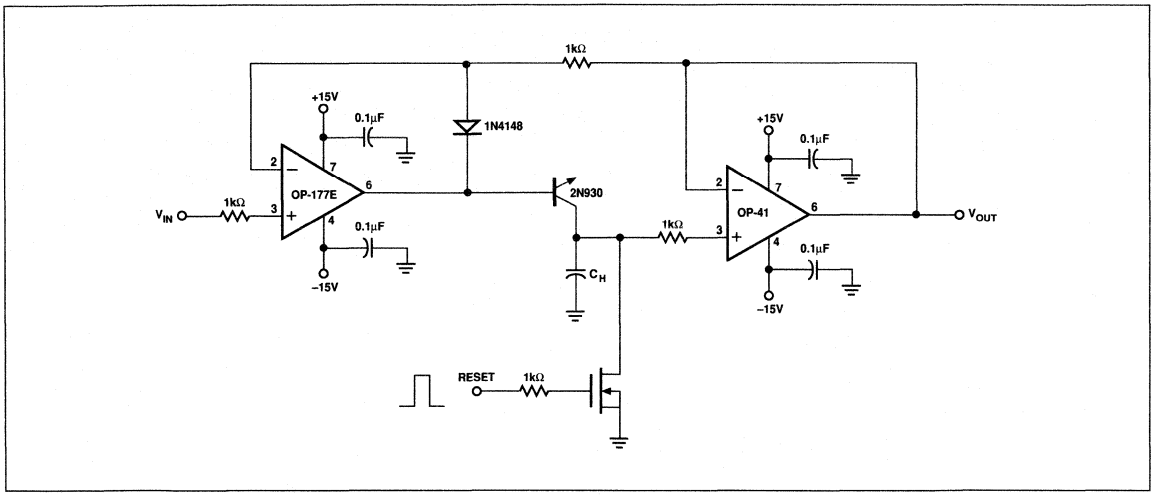


FIGURE 9: *Precision Positive Peak Detector*

PRECISION POSITIVE PEAK DETECTOR

In Figure 9, the C_H must be of polystyrene, Teflon*, or polyethylene to minimize dielectric absorption and leakage. The droop rate is determined by the size of C_H and the bias current of the OP-41.

PRECISION THRESHOLD DETECTOR/AMPLIFIER

In Figure 10, when $V_{IN} < V_{TH}$, amplifier output swings negative, reverse biasing diode D_1. $V_{OUT} = V_{TH}$ if $R_L = \infty$. When $V_{IN} \geq V_{TH}$, the loop closes,

$$V_{OUT} = V_{TH} + (V_{IN} - V_{TH}) \left(1 + \frac{R_F}{R_S}\right)$$

C_C is selected to smooth the response of the loop.

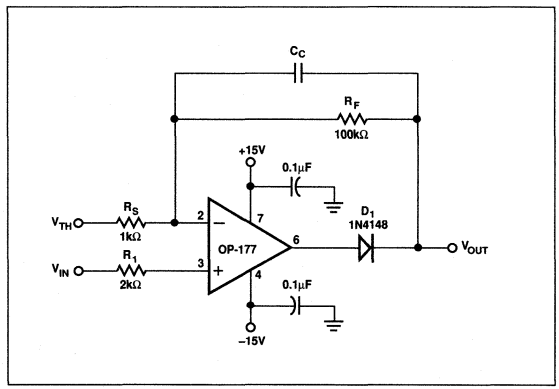


FIGURE 10: *Precision Threshold Detector/Amplifier*

ANALOG DEVICES

Dual Low-Offset, Low-Power Operational Amplifier

OP-200

FEATURES

- **Low Input Offset Voltage ..... 75μV Max**
- **Low Offset Voltage Drift, Over −55°C ≤ T_A ≤ +125°C ..... 0.5μV/°C Max**
- **Low Supply Current (Per Amplifier) ..... 725μA Max**
- **High Open-Loop Gain ..... 5000V/mV Min**
- **Low Input Bias Current ..... 2nA Max**
- **Low Noise Voltage Density ..... 11nV/√Hz at 1kHz**
- **Stable With Large Capacitive Loads ..... 10nF Typ**
- **Pin Compatible to OP-14, OP-221, LM158, MC1458/1558, and LT1013 With Improved Performance**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (μV)	PACKAGE CERDIP 8-PIN	PACKAGE PLASTIC	PACKAGE LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
75	OP200AZ*	–	OP200ARC*	MIL
75	OP200EZ	–	–	XIND
150	OP200FZ	–	–	XIND
200	–	OP200GP	–	XIND
200	–	OP200GS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

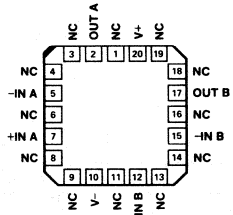
GENERAL DESCRIPTION

The OP-200 is the first monolithic dual operational amplifier to offer OP-77 type precision performance. Available in the industry standard 8-pin pinout, the OP-200 combines precision performance with the space and cost savings offered by a dual amplifier.

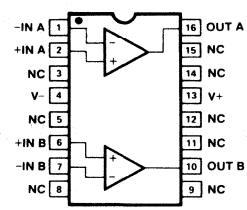
The OP-200 features an extremely low input offset voltage of less than 75μV with a drift below 0.5μV/°C, guaranteed over the

PIN CONNECTIONS

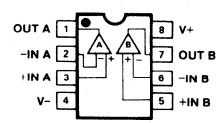
LCC (RC-Suffix)



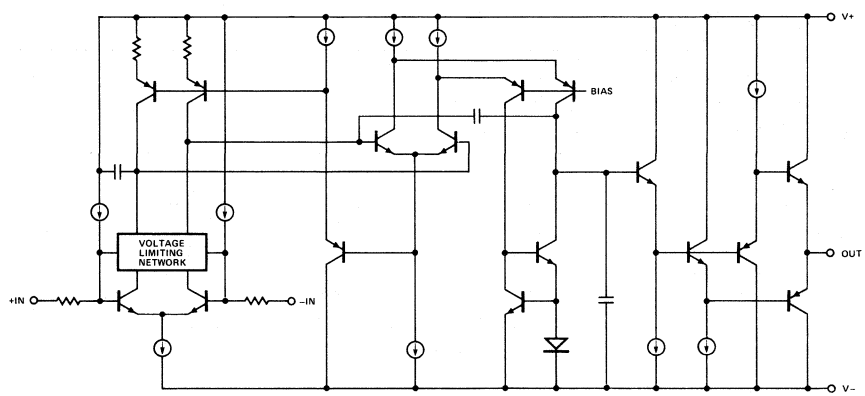
16-PIN SOL (S-Suffix)



EPOXY MINI-DIP (P-Suffix)
8-PIN HERMETIC DIP (Z-Suffix)



SIMPLIFIED SCHEMATIC (One of two amplifiers is shown.)



full military temperature range. Open-loop gain of the OP-200 exceeds 5,000,000 into a 10kΩ load; input bias current is under 2nA; CMR is over 120dB and PSRR below 1.8μV/V. On-chip zener-zap trimming is used to achieve the extremely low input offset voltage of the OP-200 and eliminates the need for offset nulling.

Power consumption of the OP-200 is very low, with each amplifier drawing less than 725μA of supply current. The total current drawn by the dual OP-200 is less than one-half that of a single OP-07, yet the OP-200 offers significant improvements over this industry standard op amp. The voltage noise density of the OP-200, 11nV/$\sqrt{Hz}$ at 1kHz, is half that of most competitive devices.

The OP-200 is pin compatible with the OP-14, OP-221, LM158, MC1458/1558, and LT1013 and can be used to upgrade systems using these devices. The OP-200 is an ideal choice for applications requiring multiple precision op amps and where low power consumption is critical.

For a quad precision op amp, see the OP-400.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±20V
Differential Input Voltage ..... ±30V
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous
Storage Temperature Range
P, RC, S, Z-Package ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature (T_j) ..... –65°C to +150°C
Operating Temperature Range
OP-200A ..... –55°C to +125°C
OP-200E, OP-200F ..... –40°C to +85°C
OP-200G ..... –40°C to +85°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	96	37	°C/W
20-Contact LCC (RC)	88	33	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

			OP-200A/E			OP-200F			OP-200G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	25	75	—	50	150	—	80	200	μV
Long Term Input Voltage Stability			—	0.1	—	—	0.1	—	—	0.1	—	μV/mo
Input Offset Current	I_{OS}	V_{CM} = 0V	—	0.05	1.0	—	0.05	2.0	—	0.05	3.5	nA
Input Bias Current	I_B	V_{CM} = 0V	—	0.1	2.0	—	0.1	4.0	—	0.1	5.0	nA
Input Noise Voltage	$e_{n\ p\text{-}p}$	0.1Hz to 10Hz	—	0.5	—	—	0.5	—	—	0.5	—	$\mu V_{p\text{-}p}$
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 1)	—	22	36	—	22	36	—	22	—	nV/$\sqrt{Hz}$
		f_O = 1000Hz (Note 1)	—	11	18	—	11	18	—	11	—	
Input Noise Current	$i_{n\ p\text{-}p}$	0.1Hz to 10Hz	—	15	—	—	15	—	—	15	—	$pA_{p\text{-}p}$
Input Noise Current Density	i_n	f_O = 10Hz	—	0.4	—	—	0.4	—	—	0.4	—	pA/$\sqrt{Hz}$
Input Resistance Differential Mode	R_{IN}		—	10	—	—	10	—	—	10	—	MΩ
Input Resistance Common Mode	R_{INCM}		—	125	—	—	125	—	—	125	—	GΩ
Large Signal Voltage Gain	A_{VO}	V_O = ±10V										
		R_L = 10kΩ	5000	12000	—	3000	7000	—	3000	7000	—	V/mV
		R_L = 2kΩ	2000	3700	—	1500	3200	—	1500	3200	—	

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $T_A = +25°C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-200A/E MIN	OP-200A/E TYP	OP-200A/E MAX	OP-200F MIN	OP-200F TYP	OP-200F MAX	OP-200G MIN	OP-200G TYP	OP-200G MAX	UNITS
Input Voltage Range	IVR	(Note 3)	±12	±13	—	±12	±13	—	±12	±13	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm12V$	120	135	—	115	135	—	110	130	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm3V$ to $\pm18V$	—	0.4	1.8	—	0.4	3.2	—	0.6	5.6	μV/V
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$	±12 ±11	±12.6 ±12.2	— —	±12 ±11	±12.6 ±12.2	— —	±12 ±11	±12.6 ±12.2	— —	V
Supply Current Per Amplifier	I_{SY}	No Load	—	570	725	—	570	725	—	570	725	μA
Slew Rate	SR		0.1	0.15	—	0.1	0.15	—	0.1	0.15	—	V/μs
Gain Bandwidth Product	GBWP	$A_V = +1$	—	500	—	—	500	—	—	500	—	kHz
Channel Separation	CS	$V_O = 20V_{p-p}$ $f_O = 10Hz$ (Note 2)	123	145	—	123	145	—	123	145	—	dB
Input Capacitance	C_{IN}		—	3.2	—	—	3.2	—	—	3.2	—	pF
Capacitive Load Stability		$A_V = +1$ No Oscillations	—	10	—	—	10	—	—	10	—	nF

NOTES:
1. Sample tested.
2. Guaranteed but not 100% tested.
3. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = +15V$, $-55°C \leq T_A \leq 125°C$ for OP-200A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-200A MIN	OP-200A TYP	OP-200A MAX	UNITS
Input Offset Voltage	V_{OS}		—	45	125	μV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.2	0.5	μV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	0.15	2.5	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	0.9	5.0	nA
Large Signal Voltage Gain	A_{VO}	$V_O = \pm10V$ $R_L = 10\Omega$ $R_L = 2k\Omega$	 3000 1000	 9000 2700	 — —	V/mV
Input Voltage Range	IVR	(Note 1)	±12	±12.5	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm12V$	115	130	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm3V$ to $\pm18V$	—	0.2	3.2	μV/V
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$	±12 ±11	±12.4 ±12	— —	V
Supply Current Per Amplifier	I_{SY}	No Load	—	600	775	μA
Capacitive Load Stability		$A_V = +1$ No Oscillations	—	8	—	nF

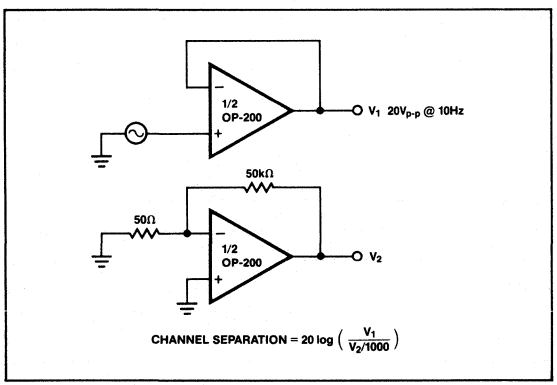
NOTES:
1. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-40°C \le T_A \le +85°C$, unless otherwise noted.

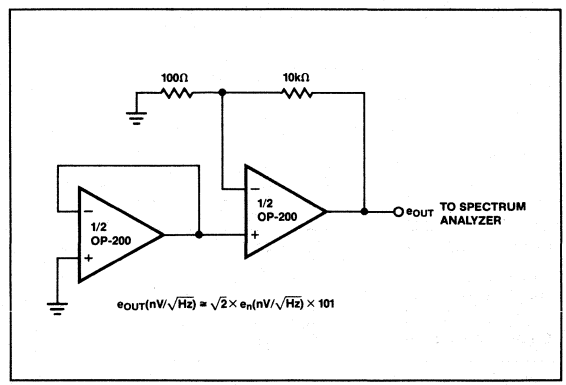
PARAMETER	SYMBOL	CONDITIONS	OP-200E MIN	OP-200E TYP	OP-200E MAX	OP-200F MIN	OP-200F TYP	OP-200F MAX	OP-200G MIN	OP-200G TYP	OP-200G MAX	UNITS
Input Offset Voltage	V_{OS}		—	35	100	—	80	250	—	110	300	μV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.2	0.5	—	0.5	1.5	—	0.6	2.0	μV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	0.08	2.5	—	0.08	3.5	—	0.1	6.0	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	0.3	5.0	—	0.3	7.0	—	0.5	10.0	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	 3000 1500	 10000 3200	 — —	 2000 1000	 5000 2500	 — —	 2000 1000	 5000 2500	 — —	V/mV
Input Voltage Range	IVR	(Note 1)	±12	±12.5	—	±12	±12.5	—	±12	±12.5	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 12V$	115	130	—	110	130	—	105	130	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	0.15	3.2	—	0.15	5.6	—	0.3	10.0	μV/V
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$	±12 ±11	±12.4 ±12	— —	±12 ±11	±12.4 ±12	— —	±12 ±11	±12.4 ±12.2	— —	V
Supply Current Per Amplifier	I_{SY}	No Load	—	600	775	—	600	775	—	600	775	μA
Capacitive Load Stability		$A_V = +1$ No Oscillations	—	10	—	—	10	—	—	10	—	nF

NOTES:
1. Guaranteed by CMR test.

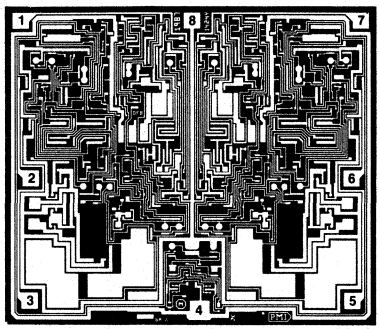
CHANNEL SEPARATION TEST CIRCUIT



NOISE TEST SCHEMATIC



DICE CHARACTERISTICS



DIE SIZE 0.120 × 0.106 inch, 12,720 sq. mils
(3.05 × 2.69 mm, 8.21 sq. mm)

1. **OUT A**
2. **−IN A**
3. **+IN A**
4. **V−**
5. **+IN B**
6. **−IN B**
7. **OUT B**
8. **V+**

2

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

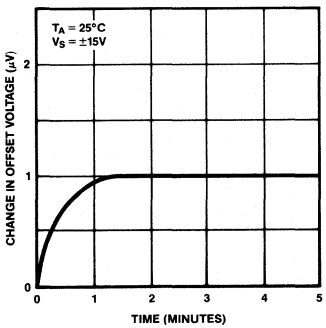
PARAMETER	SYMBOL	CONDITIONS	OP-200GBC LIMIT	UNITS
Input Offset Voltage	V_{OS}		150	μV MAX
Input Offset Current	I_{OS}	$V_{CM} = 0V$	2	nA MAX
Input Bias Current	I_B	$V_{CM} = 0V$	4	nA MAX
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	 3000 1500	 V/mV MIN
Input Voltage Range	IVR	(Note 1)	±12	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 12V$	115	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	3.2	μV/V MAX
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$	±12 ±11	V MIN
Supply Current Per Amplifier	I_{SY}	No Load	725	μA MAX

NOTES:
1. Guaranteed by CMR test.

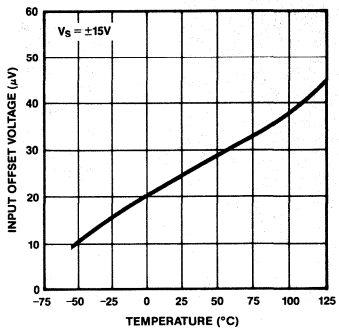
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

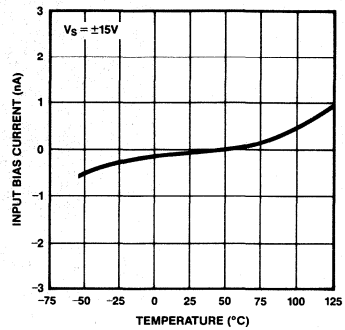
WARM-UP DRIFT



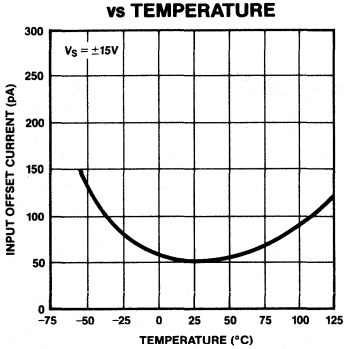
INPUT OFFSET VOLTAGE vs TEMPERATURE



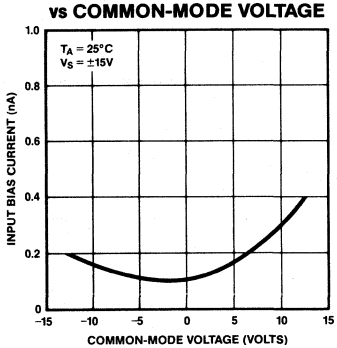
INPUT BIAS CURRENT vs TEMPERATURE



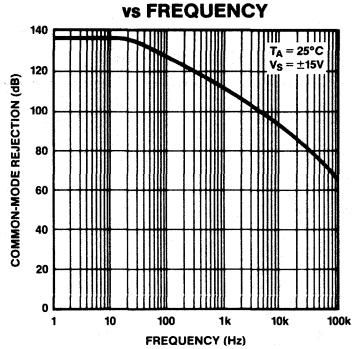
INPUT OFFSET CURRENT vs TEMPERATURE



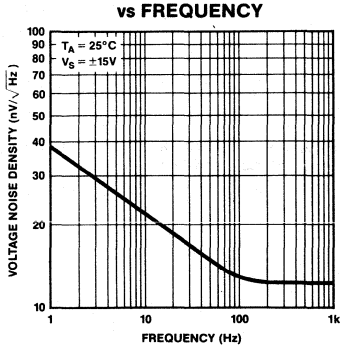
INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE



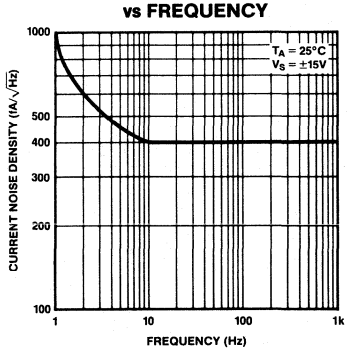
COMMON-MODE REJECTION vs FREQUENCY



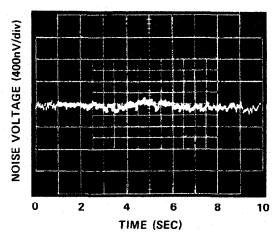
VOLTAGE NOISE DENSITY vs FREQUENCY



CURRENT NOISE DENSITY vs FREQUENCY

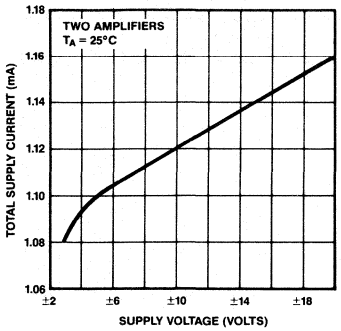


0.1Hz TO 10Hz NOISE

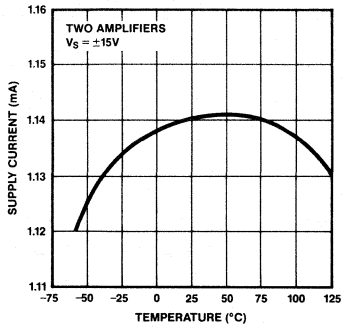


TYPICAL PERFORMANCE CHARACTERISTICS

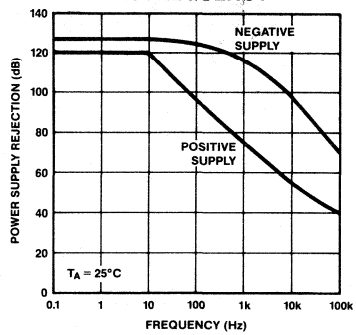
TOTAL SUPPLY CURRENT vs SUPPLY VOLTAGE



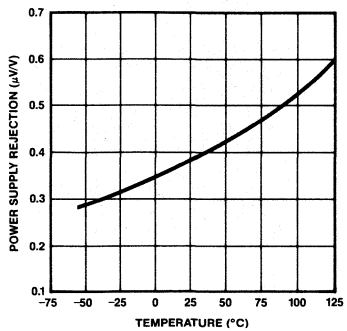
TOTAL SUPPLY CURRENT vs TEMPERATURE



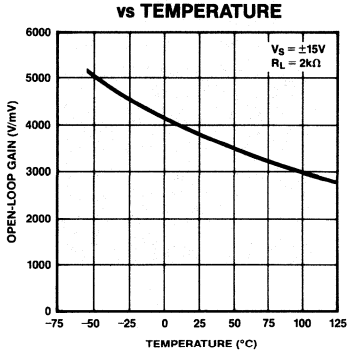
POWER SUPPLY REJECTION vs FREQUENCY



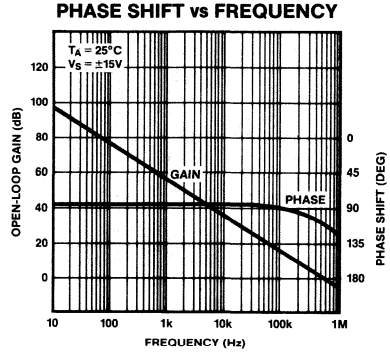
POWER SUPPLY REJECTION vs TEMPERATURE



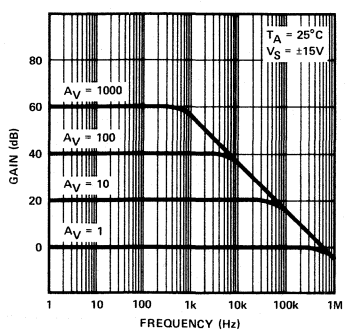
OPEN-LOOP GAIN vs TEMPERATURE



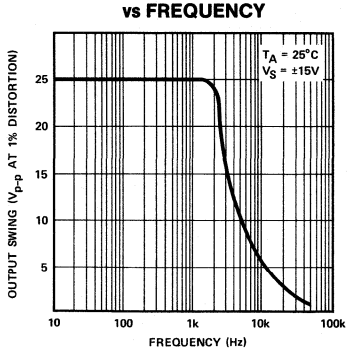
OPEN-LOOP GAIN AND PHASE SHIFT vs FREQUENCY



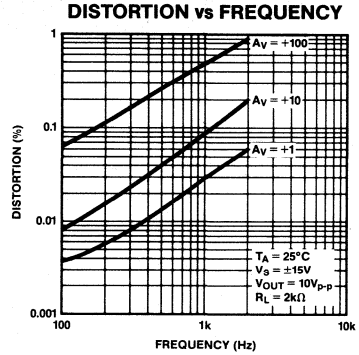
CLOSED-LOOP GAIN vs FREQUENCY



MAXIMUM OUTPUT SWING vs FREQUENCY

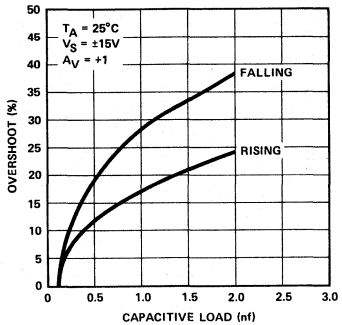


TOTAL HARMONIC DISTORTION vs FREQUENCY

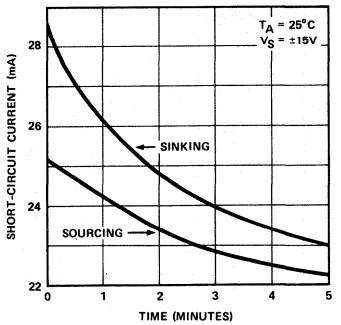


TYPICAL PERFORMANCE CHARACTERISTICS

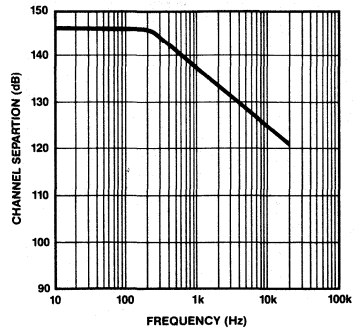
OVERSHOOT vs CAPACITIVE LOAD



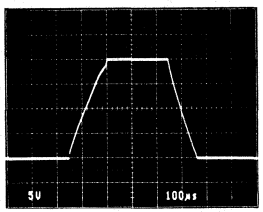
SHORT-CIRCUIT CURRENT vs TIME



CHANNEL SEPARATION vs FREQUENCY

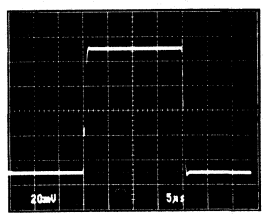


LARGE-SIGNAL TRANSIENT RESPONSE



T_A = 25°C
V_S = ±15V
A_V = +1

SMALL-SIGNAL TRANSIENT RESPONSE



T_A = 25°C
V_S = ±15V
A_V = +1

SMALL-SIGNAL TRANSIENT RESPONSE C_{LOAD} = 1nF

T_A = 25°C
V_S = ±15V
A_V = +1

APPLICATIONS INFORMATION

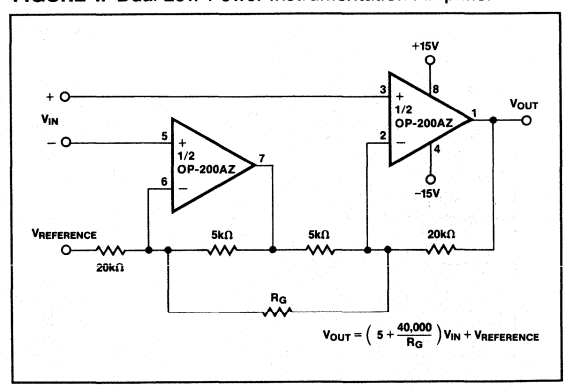
The OP-200 in inherently stable at all gains and is capable of driving large capacitive loads without oscillating. Nonetheless, good supply decoupling is highly recommended. Proper supply decoupling reduces problems caused by supply line noise and improves the capacitive load driving capability of the OP-200.

APPLICATIONS

DUAL LOW-POWER INSTRUMENTATION AMPLIFIER

A dual instrumentation amplifier that consumes less than 33mW of power per channel is shown in Figure 1. The linearity of the instrumentation amplifier exceeds 16 bits in gains of 5 to 200 and is better than 14 bits in gains from 200 to 1000. CMRR is above 115dB (Gain = 1000). Offset voltage drift is typically 0.2µV/°C over the military temperature range which is comparable to the best monolithic instrumentation amplifiers. The

FIGURE 1: Dual Low-Power Instrumentation Amplifier



bandwidth of the low-power instrumentation amplifier is a function of gain and is shown below:

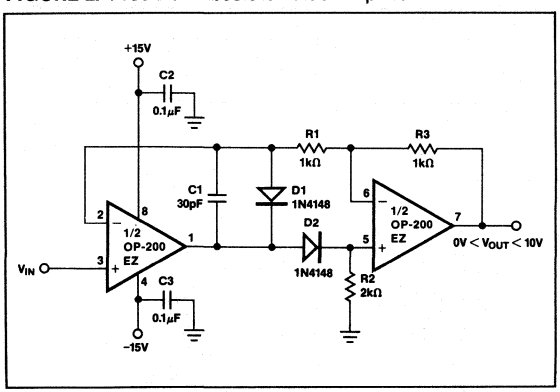
GAIN	BANDWIDTH
5	150kHz
10	67kHz
100	7.5kHz
1000	500Hz

The output signal is specified with respect to the reference input, which is normally connected to analog ground. The reference input can be used to offset the output from −10V to +10V if required.

PRECISION ABSOLUTE VALUE AMPLIFIER

The circuit of Figure 2 is a precision absolute value amplifier with an input impedance of 10MΩ. The high gain and low TCV_{OS} of the OP-200 insure accurate operation with microvolt input signals. In this circuit, the input always appears as a common-mode signal to the op amps. The CMR of the OP-200 exceeds 120dB, yielding an error of less than 2ppm.

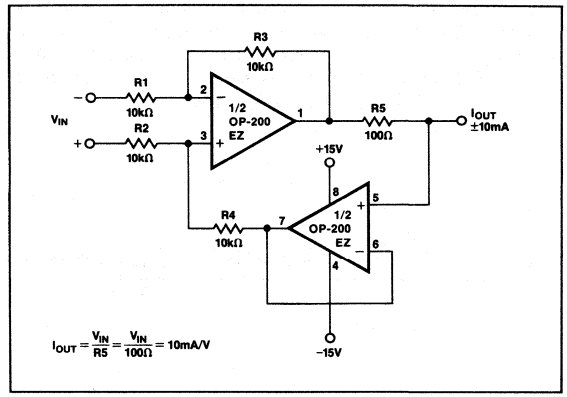
FIGURE 2. Precision Absolute Value Amplifier



PRECISION CURRENT PUMP

Maximum output current of the precision current pump shown in Figure 3 is ±10mA. Voltage compliance is ±10V with ±15V supplies. Output impedance of the current transmitter exceeds 3MΩ with linearity better than 16 bits.

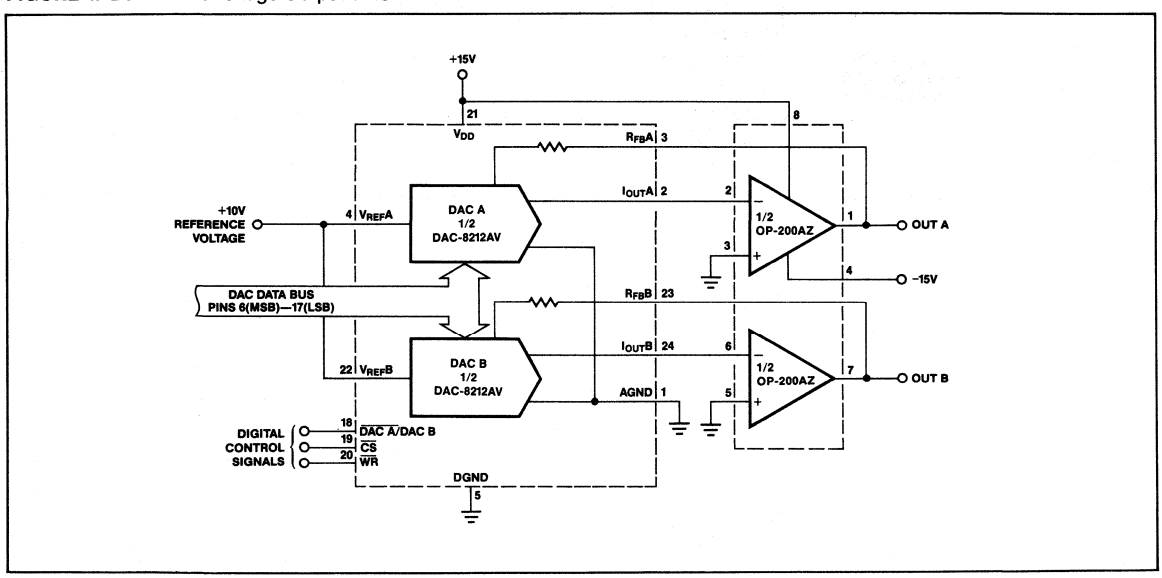
FIGURE 3. Precision Current Pump



DUAL 12-BIT VOLTAGE OUTPUT DAC

The dual output DAC shown in Figure 4 is capable of providing untrimmed 12-bit accurate operation over the entire military temperature range. Offset voltage, bias current and gain errors of the OP-200 contribute less than 1/10 of an LSB error at 12 bits over the military temperature range.

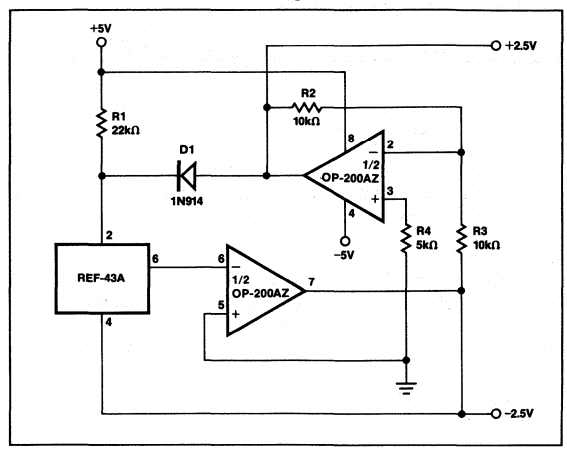
FIGURE 4. Dual 12-Bit Voltage Output DAC



DUAL PRECISION VOLTAGE REFERENCE

A dual OP-200 and a REF-43, a 2.5V voltage reference, can be used to build a ±2.5V precision voltage reference. Maximum output current from each reference is ±10mA with load regulation under 25μV/mA. Line regulation is better than 15μV/V and output voltage drift is under 20μV/°C. Output voltage noise from 0.1Hz to 10Hz is typically 75μV_{p-p}. R1 and D1 insure correct start-up.

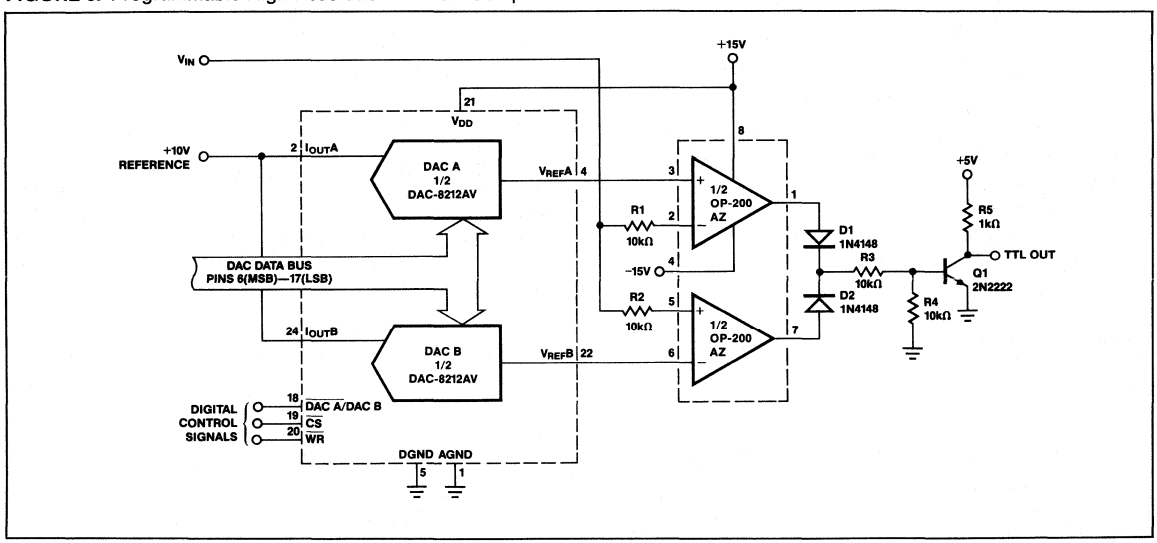
FIGURE 5. Dual Precision Voltage Reference



PROGRAMMABLE HIGH RESOLUTION WINDOW COMPARATOR

The programmable window comparator shown in Figure 6 is easily capable of 12-bit accuracy over the full military temperature range. A dual CMOS 12-bit DAC, the DAC-8212, is used in the voltage switching mode to set the upper and lower thresholds (DAC A and DAC B, respectively).

FIGURE 6. Programmable High Resolution Window Comparator



ANALOG DEVICES

Dual Ultralow V_{OS} Matched Operational Amplifier

OP-207

FEATURES

- **Low V_{OS} ..... 100μV Max**
- **Offset Voltage Match ..... 90μV Max**
- **Offset Voltage Match vs. Temp. ..... 1.0μV/°C Max**
- **Common-Mode Rejection Match ..... 103dB Min**
- **Bias Current Match ..... 3.5nA Max**
- **Low Noise ..... 0.6μV_{p-p} Max**
- **Low Bias Current ..... 3.0nA Max**
- **High Channel Separation ..... 126dB Min**

ORDERING INFORMATION†

T_A = 25°C V_{OS} MAX (μV)	HERMETIC DIP 14-PIN	OPERATING TEMPERATURE RANGE
100	OP207AY*	MIL
100	OP207EY	COM
200	OP207FY	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

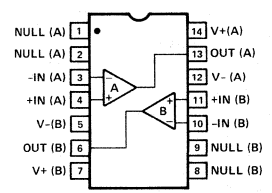
GENERAL DESCRIPTION

The OP-207 series of dual matched operational amplifiers consists of two independent OP-07 high performance operational amplifiers in a single 14-pin dual-in-line package. Exceptionally low offset voltage and tight matching of critical parameters is provided between the channels of this dual operational amplifier.

The excellent specifications of the individual amplifiers combined with the tight matching and temperature tracking between channels provide high performance in instrumentation amplifier designs. The individual amplifiers feature very low input offset voltage, low offset voltage drift, low noise voltage, and low bias current. Each amplifier is fully compensated and protected.

Matching between channels is provided on all critical parameters including offset voltage, tracking of offset voltage vs. temperature, noninverting bias currents, and common-mode rejection.

PIN CONNECTIONS

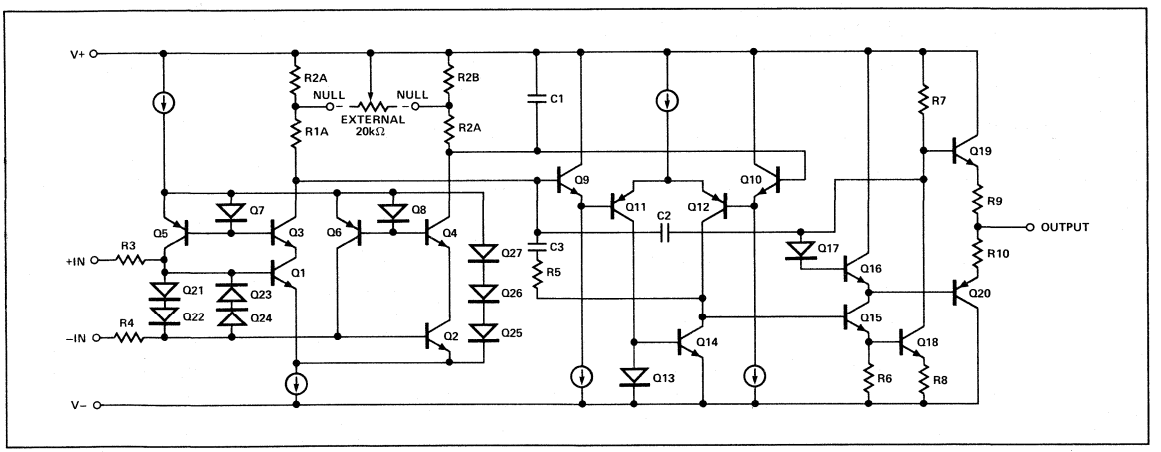


14-PIN HERMETIC DIP (Y-Suffix)

NOTES:

1. Device may be operated even if insertion is reversed; this is due to inherent symmetry of pin locations of amplifiers A and B.
2. V-(A) and V-(B) are internally connected via substrate resistance.

SIMPLIFIED SCHEMATIC (1/2 OP-207)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Differential Input Voltage ..... ±30V
Input Voltage (Note 1) ..... ±22V
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range ..... –65°C to 150°C
Operating Temperature Range
OP-207A ..... –55°C to +125°C
OP-207E, OP-207F ..... 0°C to +70°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
14-Pin Hermetic DIP (Y)	108	16	°C/W

NOTES:
1. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP package.

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-207A/E MIN	OP-207A/E TYP	OP-207A/E MAX	OP-207F MIN	OP-207F TYP	OP-207F MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}	$R_S = 100\Omega$	—	30	90	—	50	280	µV
Average Noninverting Bias Current	I_{B^+}		—	±1.5	±3.5	—	±1.5	±6.0	nA
Noninverting Offset Current	I_{OS^+}		—	±0.7	±3.5	—	±1.0	±6.0	nA
Inverting Offset Current	I_{OS^-}		—	±0.7	±3.5	—	±1.0	±6.0	nA
Common-Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm 13V$	103	120	—	96	114	—	dB
Power Supply Rejection Ratio Match	ΔPSRR	$V_S = \pm 3V$ to $\pm 18V$	—	7	32	—	10	51	µV/V
Channel Separation			126	140	—	126	140	—	dB

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq 125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-207A MIN	OP-207A TYP	OP-207A MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}	$R_S = 100\Omega$	—	70	180	µV
Input Offset Voltage Tracking						
Without External Trim	$TC\Delta V_{OS}$	(Note 1)	—	0.5	1.0	µV/°C
With External Trim	$TC\Delta V_{OSn}$	$R_P = 20k\Omega$ (Note 1)	—	0.3	1.0	µV/°C
Average Noninverting Bias Current	I_{B^+}		—	±2	±6	nA
Average Drift of Non-inverting Bias Current	TCI_{B^+}		—	10	—	pA/°C
Noninverting Offset Current	I_{OS^+}		—	2	6.5	nA
Average Drift of Non-inverting Offset Current	TCI_{OS^+}		—	12	—	pA/°C
Inverting Offset Current	I_{OS^-}		—	2	6.5	nA
Common-Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm 13V$	100	117	—	dB
Power Supply Rejection Ratio Match	ΔPSRR	$V_S = \pm 3V$ to $\pm 18V$	—	10	51	µV/V

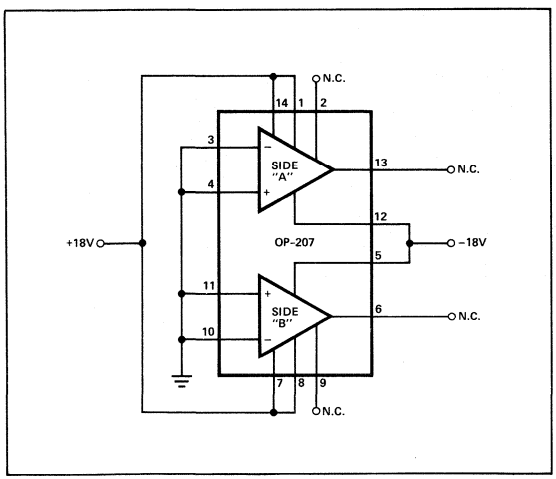
NOTE:
1. Sample tested.

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $0°C \leq T_A \leq 70°C$, unless otherwise noted.

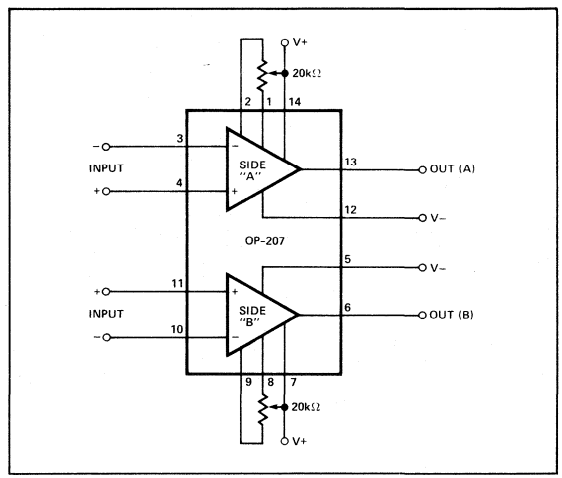
			OP-207E			OP-207F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage Match	ΔV_{OS}	$R_S = 100\Omega$	—	60	150	—	120	350	μV
Input Offset Voltage Tracking									
Without External Trim	$TC\Delta V_{OS}$	(Note 1)	—	0.5	1.0	—	0.9	1.5	μV/°C
With External Trim	$TC\Delta V_{OSn}$	$R_P = 20k\Omega$ (Note 1)	—	0.3	1.0	—	0.4	1.3	
Average Noninverting Bias Current	I_{B^+}		—	±2	±5	—	±3	±10	nA
Average Drift of Non-inverting Bias Current	TCI_{B^+}		—	10	—	—	12	—	pA/°C
Noninverting Offset Current	I_{OS^+}		—	2	5	—	3	10	nA
Average Drift of Non-inverting Offset Current	TCI_{OS^+}		—	12	—	—	15	—	pA/°C
Inverting Offset Current	I_{OS^-}		—	2	5	—	3	10	nA
Common-Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm 13V$	100	117	—	94	114	—	dB
Power Supply Rejection Ratio Match	ΔPSRR	$V_S = \pm 3V$ to $\pm 18V$	—	10	51	—	16	100	μV/V

NOTE:
1. Sample tested.

BURN-IN CIRCUIT



OFFSET NULLING CIRCUIT



INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-207A/E MIN	OP-207A/E TYP	OP-207A/E MAX	OP-207F MIN	OP-207F TYP	OP-207F MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 100\Omega$	—	35	100	—	60	200	μV
Input Offset Voltage Stability	$\Delta V_{OS}/Time$	(Note 1)	—	0.3	1.5	—	0.4	2.0	$\mu V/Mo$
Input Offset Current	I_{OS}		—	0.9	2.8	—	1.5	6.0	nA
Input Bias Current	I_B		—	±1	±3	—	±2	±7	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 2)	—	0.35	0.6	—	0.35	0.6	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$ (Note 2)	—	10.3	18.0	—	10.3	18.0	$nV/\sqrt{Hz}$
		$f_O = 100Hz$ (Note 2)	—	10.0	13.0	—	10.0	13.0	
		$f_O = 1000Hz$ (Note 2)	—	9.6	—	—	9.6	—	
Input Noise Current	I_{np-p}	0.1Hz to 10Hz (Note 2)	—	14	30	—	14	30	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10Hz$ (Note 2)	—	0.32	0.80	—	0.32	0.80	$pA/\sqrt{Hz}$
		$f_O = 100Hz$ (Note 2)	—	0.14	0.23	—	0.14	0.23	
		$f_O = 1000Hz$ (Note 2)	—	0.12	—	—	0.12	—	
Input Resistance — Differential Mode	R_{IN}	(Note 3)	20	60	—	8	30	—	MΩ
Input Resistance — Common-Mode	$R_{IN\,CM}$		—	200	—	—	120	—	GΩ
Input Voltage Range	IVR		±13	±14	—	±13	±14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	106	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	7	32	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	200	500	—	150	400	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	±12.5	±13.0	—	±12.5	±13.0	—	V
		$R_L \geq 2k\Omega$	±12.0	±12.8	—	±12.0	±12.8	—	
		$R_L \geq 1k\Omega$	±10.0	±12.0	—	±10.0	±12.0	—	
Slew Rate	SR	$R_L \geq 2k\Omega$	—	0.2	—	—	0.2	—	$V/\mu s$
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$	—	0.6	—	—	0.6	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	60	—	—	60	—	Ω
Power Consumption	P_d	No Load, Both Amplifiers	—	180	240	—	200	300	mW
Offset Adjustment Range		$R_P = 20k\Omega$	—	±4	—	—	±4	—	mV
Input Capacitance	C_{IN}		—	8	—	—	8	—	pF

NOTES:

1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically $2.5\mu V$. Parameter is sample tested.
2. Sample tested.
3. Guaranteed by design.

INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq 125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-207A MIN	OP-207A TYP	OP-207A MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 100\Omega$	—	75	230	μV
Average Input Offset Voltage Drift						
Without External Trim	TCV_{OS}	$R_P = 20k\Omega$ (Notes 1, 2)	—	0.4	1.3	μV/°C
With External Trim	TCV_{OSn}		—	0.4	—	
Input Offset Current	I_{OS}		—	1.8	5.6	nA
Average Input Offset Current Drift	TCI_{OS}		—	10	—	pA/°C
Input Bias Current	I_B		—	±3.0	±5.6	nA
Average Input Bias Current Drift	TCI_B		—	12	—	pA/°C
Input Voltage Range	IVR		±13	±13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	103	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	7	32	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	150	400	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.0	±12.8	—	V

INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm 15V$, $0°C \leq T_A \leq 70°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-207E MIN	OP-207E TYP	OP-207E MAX	OP-207F MIN	OP-207F TYP	OP-207F MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 100\Omega$	—	60	200	—	90	350	μV
Average Input Offset Voltage Drift									
Without External Trim	TCV_{OS}	$R_P = 20k\Omega$ (Notes 1, 2)	—	0.4	1.3	—	0.7	1.8	μV/°C
With External Trim	TCV_{OSn}		—	0.4	—	—	0.7	—	
Input Offset Current	I_{OS}		—	1.4	5	—	2.5	10	nA
Average Input Offset Current Drift	TCI_{OS}		—	10	—	—	12	—	pA/°C
Input Bias Current	I_B		—	±2	±5	—	±3	±11	nA
Average Input Bias Current Drift	TCI_B		—	12	—	—	18	—	pA/°C
Input Voltage Range	IVR		±13	±13.5	—	±13	±13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	103	120	—	97	117	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	7	32	—	10	51	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	150	400	—	120	350	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.0	±12.8	—	±12.0	±12.8	—	V

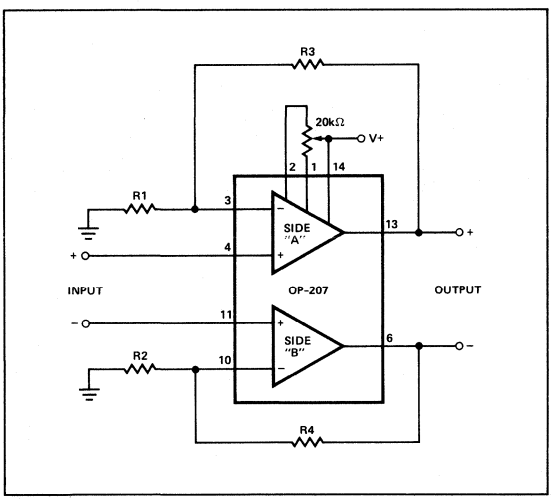
NOTES:
1. Exclude first hour of operation to allow for stabilization of external circuitry.
2. Sample tested.

APPLICATION OF DUAL MATCHED OPERATIONAL AMPLIFIERS

ADVANTAGES OF DUAL MATCHED OPERATIONAL AMPLIFIERS

Dual matched operational amplifiers provide a powerful tool for the solution of some difficult circuit design problems. Circuits include true instrumentation amplifiers, extremely low drift, high common-mode rejection DC amplifiers, low DC drift active filters, dual tracking voltage references, and many other demanding applications. These designs all require good matching between two operational amplifiers.

The circuit below, a differential-in, differential-out amplifier, shows how errors can be reduced. Assuming the resistors used are matched, the gain of each side will be identical; if the offset voltage of each amplifier is matched, then the net differential voltage at the amplifiers output will be zero. Note that the output offset error of this amplifier is not a function of the offset voltage of the individual amplifiers, but only a function of the *difference* between the amplifiers' offset voltages. This error-cancellation principle holds for a number of input-referred error parameters — offset voltage, offset voltage drift, inverting and noninverting bias currents, common-mode and power supply rejection ratios. Note also that the impedances of each input, both common-mode and differential-mode, are extremely high, an important feature not possible with single operational amplifier circuits. Common-mode rejection can be made exceptionally high; this is very important in instrumentation amplifiers where errors due to large common-mode voltages can be far greater than errors due to noise or drift with temperature. For example, consider the case of two op amps, each with 80dB (100μV/V) CMRR. If the CMRR of one device is +100μV/V CMRR and the other is −100μV/V, then the net CMRR will be 200μV/V, a 6dB degradation. The matching of CMRR increases the effective CMRR when used as an instrumentation input stage.



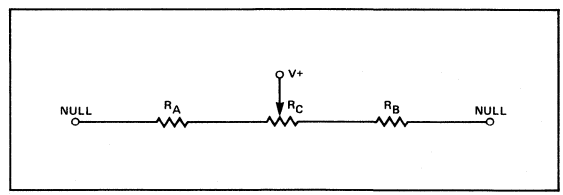
POWER SUPPLIES

The V+ supply terminals are completely independent and may be powered by separate supplies if desired. However, this approach would sacrifice the advantages of the power-supply-rejection-ratio matching. The V− supply terminals are both connected to the common substrate and must be tied to the same voltage.

OFFSET TRIMMING

Offset voltage trimming is provided for each amplifier. Guaranteed performance over temperature is obtained by trimming one side (side A) to match the offset of the other. A net differential offset of zero results. This procedure is used during factory testing of the devices. The same results are obtained by trimming side B to match side A or by nulling each side individually.

The OP-207 is designed to provide best drift performance when trimmed with a 20kΩ potentiometer; this value provides about ±4mV of adjustment range which is adequate for most applications. Trimming resolution can be increased by use of the circuit shown below.



ANALOG DEVICES

Dual Precision JFET-Input Operational Amplifier

OP-215

FEATURES

- **High Slew Rate** ..... **10V/μs Min**
- **Fast Settling Time** ..... **0.9μs to 0.1% Typ**
- **Low Input Offset Voltage Drift** ..... **10μV/°C Max**
- **Wide Bandwidth** ..... **3.5MHz Min**
- **Temperature-Compensated Input Bias Currents**
- **Guaranteed Input Bias Current** ..... **18nA Max (125°C)**
- **Bias Current Specified Warmed-Up Over Temperature**
- **Low Input Noise Current** ..... **0.01pA/$\sqrt{Hz}$ Typ**
- **High Common-Mode Rejection Ratio** ..... **86dB Min**
- **Pin Compatible With Standard Dual Pinouts**
- **125°C Temperature Tested DICE**
- **Models With MIL-STD-883 Class B Processing Available**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = 25°C V_{os} MAX (mV)	PACKAGE TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
1.0	OP215AJ*	OP215AZ*	–	–	MIL
1.0	OP215EJ	OP215EZ	OP215EP	–	COM
2.0	OP215BJ/883	OP215BZ/883	–	OP215BRC/883	MIL
2.0	OP215FJ	OP215FZ	OP215FP	–	COM
4.0	OP215CJ/883	OP215CZ/883	–	–	MIL
6.0	–	OP215GZ	OP215GP	–	XIND
6.0	–	–	OP215GS	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

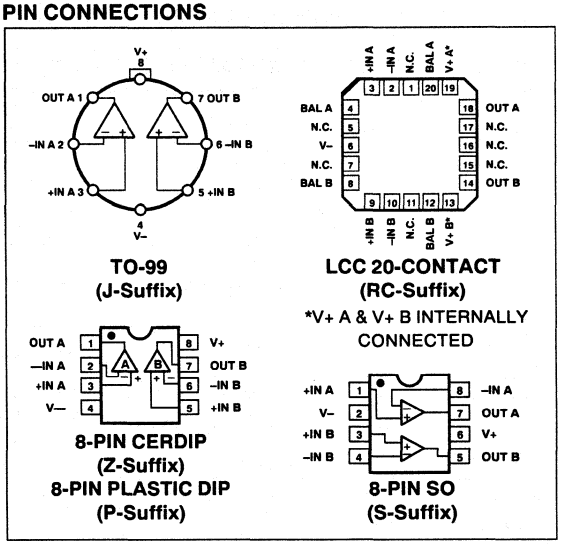
The OP-215 offers the proven JFET-input performance advantages of high speed and low input bias current with the tracking and convenience advantages of a dual op-amp configuration.

Low input offset voltages, low input currents, and low drift are featured in these high-speed amplifiers.

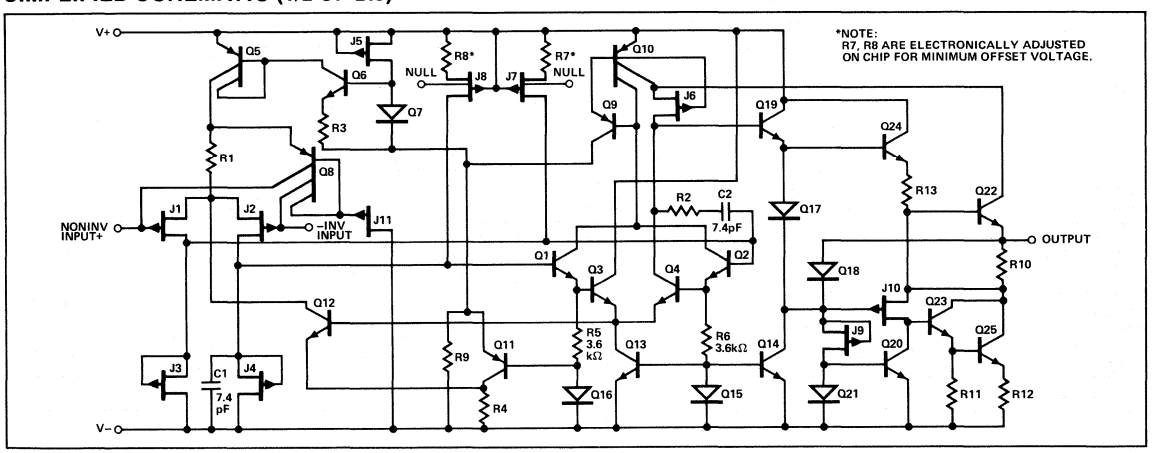
On-chip zener-zap trimming is used to achieve low V_{OS} while a bias-current compensation scheme gives a low input bias current at elevated temperatures. Thus the OP-215 features an input bias current of 18nA at 125°C ambient (not junction) temperature which greatly extends the application usefulness of this device.

Applications include high-speed amplifiers for current output DACs, active filters, sample-and-hold buffers, and photocell

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC (1/2 OP-215)



GENERAL DESCRIPTION *Continued*

amplifiers. For additional precision JFET op amps, see the OP-15/16/17 data sheet.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage
- OP-215A, OP-215B, OP-215E, OP-215F (All DICE Except GR) ..... ±22V
- OP-215C, OP-215G (GR DICE Only) ..... ±18V

Operating Temperature Range
- OP-215A, OP-215B, OP-215C ..... −55°C to +125°C
- OP-215E, OP215F ..... 0°C to + 70°C
- OP-215G ..... −40°C to +85°C

Maximum Junction Temperature (T_j) ..... +150°C

Differential Input Voltage
- OP-215A, OP-215B, (All DICE Except GR) ..... ±40V
- OP-215E, OP-215F, (All DICE Except GR) ..... ±40V
- OP-215C, OP-215G, (GR DICE Only) ..... ±30V

Input Voltage
- OP-215A, OP-215B, (All DICE Except GR) ..... ±20V
- OP-215E, OP-215F, (All DICE Except GR) ..... ±20V
- OP-215C, OP-215G, (GR DICE Only) ..... ±16V

(Unless otherwise specified, the absolute maximum negative input voltage is equal to one volt more positive than the negative power supply voltage.)

Output Short-Circuit Duration ..... Indefinite

Storage Temperature Range ..... −65°C to +150°C

Lead Temperature (Soldering, 60 sec) ..... 300°C

Junction Temperature (T_j) ..... −65°C to +150°C

PACKAGE TYPE	Θ_{JA} (NOTE 2)	Θ_{JC}	UNITS
TO-99 (J)	145	16	°C/W
8-Pin Hermetic DIP (Z)	134	12	°C/W
8-Pin Plastic DIP (P)	96	37	°C/W
20-Contact LCC (RC)	88	33	°C/W
8-Pin SO (S)	150	41	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-215A/E MIN	OP-215A/E TYP	OP-215A/E MAX	OP-215B/F MIN	OP-215B/F TYP	OP-215B/F MAX	OP-215C/G MIN	OP-215C/G TYP	OP-215C/G MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	0.2	1.0	—	0.8	2.0	—	2.0	4.0	mV
		'G' Grade	—	—	—	—	—	—	—	2.5	6.0	
Input Offset Current	I_{OS}	$T_j = 25°C$ (Note 1)	—	3	50	—	3	50	—	3	100	pA
		Device Operating	—	5	100	—	5	100	—	5	200	
Input Bias Current	I_B	$T_j = 25°C$ (Note 1)	—	±15	±100	—	±15	±200	—	±15	±300	pA
		Device Operating	—	±18	±300	—	±18	±400	—	±18	±600	
Input Resistance	R_{IN}		—	10^{12}	—	—	10^{12}	—	—	10^{12}	—	Ω
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	150	500	—	75	220	—	50	200	—	V/mV
Output Voltage Swing	V_O	$R_L = 10k\Omega$	±12	±13	—	±12	±13	—	±12	±13	—	V
		$R_L = 2k\Omega$	±11	±12.7	—	±11	±12.7	—	±11	±12.7	—	
Supply Current	I_{SY}		—	6.0	8.5	—	6.0	8.5	—	7.0	10.0	mA
		'G' Grade	—	—	—	—	—	—	—	7.0	12.0	
Slew Rate	SR	$A_{VCL} = +1$	10	18	—	7.5	18	—	5	15	—	V/μs
Gain Bandwidth Product	GBW	(Note 3)	3.5	5.7	—	3.5	5.7	—	3.0	5.4	—	MHz
Closed-Loop Bandwidth	CLBW	$A_{VCL} = +1$	—	13	—	—	13	—	—	12	—	MHz
Settling Time	t_S	to 0.01%	—	2.3	—	—	2.3	—	—	2.4	—	μs
		to 0.05% (Note 2)	—	1.1	—	—	1.1	—	—	1.2	—	
		to 0.10%	—	0.9	—	—	0.9	—	—	1.0	—	
Input Voltage Range	IVR		+10.2	+14.8	—	+10.2	+14.8	—	+10.1	+14.8	—	V
			−10.2	−11.5	—	−10.2	−11.5	—	−10.1	−11.5	—	
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm IVR$ A, B, C Grades	86	100	—	86	100	—	82	96	—	dB
		E, F, G Grades	82	100	—	82	100	—	80	96	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 16V$	—	10	51	—	10	80	—	—	—	μV/V
		$V_S = \pm 10V$ to $\pm 15V$	—	—	—	—	—	—	—	16	100	
Input Noise Voltage Density	e_n	$f_O = 100Hz$	—	20	—	—	20	—	—	20	—	$nV/\sqrt{Hz}$
		$f_O = 1000Hz$	—	15	—	—	15	—	—	15	—	
Input Noise Current Density	i_n	$f_O = 100Hz$	—	0.01	—	—	0.01	—	—	0.01	—	$pA/\sqrt{Hz}$
		$f_O = 1000Hz$	—	0.01	—	—	0.01	—	—	0.01	—	
Input Capacitance	C_{IN}		—	3	—	—	3	—	—	3	—	pF

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-215A MIN	OP-215A TYP	OP-215A MAX	OP-215B MIN	OP-215B TYP	OP-215B MAX	OP-215C MIN	OP-215C TYP	OP-215C MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	0.5	2.0	—	1.5	3.0	—	3.0	6.0	mV
Average Input Offset Voltage Drift												
Without External Trim	TCV_{OS}	(Note 3)	—	3	10	—	3	10	—	6	—	µV/°C
With External Trim	TCV_{OSn}	$R_P = 100k\Omega$	—	3	—	—	3	—	—	4	—	
Input Offset Current (Note 1)	I_{OS}	$T_j = +125°C$	—	0.8	8	—	0.8	8	—	1.0	12	nA
		$T_A = +125°C$, Device Operating	—	1.2	14	—	1.2	14	—	1.5	22	
Input Bias Current (Note 1)	I_B	$T_j = +125°C$	—	±1.5	±10	—	±1.5	±10	—	±1.8	±15	nA
		$T_A = +125°C$, Device Operating	—	±2.2	±18	—	±2.2	±18	—	±2.7	±28	
Input Voltage Range	IVR		+10.2	+14.6	—	+10.2	+14.6	—	+10.1	+14.6	—	V
			−10.2	−11.3	—	−10.2	−11.3	—	−10.1	−11.3	—	
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm IVR$	82	97	—	82	97	—	80	93	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 16V$	—	10	100	—	15	100	—	—	—	µV/V
		$V_S = \pm 10V$ to $\pm 15V$	—	—	—	—	—	—	—	23	126	
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	30	110	—	30	110	—	25	100	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	±12	±13	—	±12	±13	—	±12	±13	—	V

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0°C \leq T_A \leq +70°C$ for E/F Grades, $-40°C \leq T_A \leq +85°C$ for G Grade, unless otherwise noted.

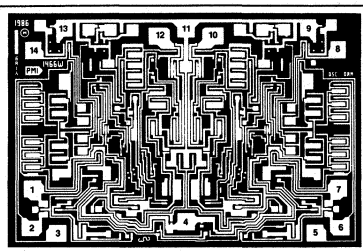
PARAMETER	SYMBOL	CONDITIONS	OP-215E MIN	OP-215E TYP	OP-215E MAX	OP-215F MIN	OP-215F TYP	OP-215F MAX	OP-215G MIN	OP-215G TYP	OP-215G MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	0.4	1.65	—	1.4	2.65	—	3.5	8.0	mV
Average Input Offset Voltage Drift												
Without External Trim	TCV_{OS}	(Note 3)	—	3	15	—	3	15	—	6	—	µV/°C
With External Trim	TCV_{OSn}	$R_P = 100k\Omega$	—	3	—	—	3	—	—	4	—	
Input Offset Current (Note 1)	I_{OS}	$T_j = +70°C$	—	0.06	0.45	—	0.06	0.45	—	0.08	0.65	nA
		$T_A = +70°C$, Device Operating	—	0.08	0.80	—	0.08	0.80	—	0.10	1.2	
Input Bias Current (Note 1)	I_B	$T_j = +70°C$	—	±0.12	±0.70	—	±0.12	±0.70	—	±0.14	±0.9	nA
		$T_A = +70°C$, Device Operating	—	±0.16	±1.40	—	±0.16	±1.40	—	±0.19	±1.8	
Input Voltage Range	IVR		+10.2	+14.7	—	+10.2	+14.7	—	+10.1	+14.7	—	V
			−10.2	−11.4	—	−10.2	−11.4	—	−10.1	−11.3	—	
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm IVR$	80	98	—	80	98	—	76	94	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 16V$	—	13	100	—	13	100	—	—	—	µV/V
		$V_S = \pm 10V$ to $\pm 15V$	—	—	—	—	—	—	—	20	159	
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	50	180	—	50	180	—	35	130	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	±12	±13	—	±12	±13	—	±12	±13	—	V

NOTES:

1. Input bias current is specified for two different conditions. The $T_j = 25°C$ specification is with the junction at ambient temperature; the Device Operating specification is with the device operating in a warmed-up condition at 25°C ambient. The warmed-up bias current value is correlated to the junction temperature value via the curves of I_B vs. T_j and I_B vs. T_A. PMI has a bias current compensation circuit which gives improved bias current and bias current over temperature vs. standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
2. Settling time is defined here for a unity gain inverter connection using 2kΩ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within a specified percent of its final value from the time a 10V step input is applied to the inverter. See settling time test circuit.
3. Sample tested.

OP-215

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



1. INVERTING INPUT (A)
2. NONINVERTING INPUT (A)
3. NULL (A)
4. V–
5. NULL (B)
6. NONINVERTING INPUT (B)
7. INVERTING INPUT (B)
8. NULL (B)
9. V+
10. V_O (B)
11. V+
12. V_O (A)
13. V+
14. NULL (A)

ALL V+ PADS ARE INTERNALLY CONNECTED.

DIE SIZE 0.110 × 0.075 inch, 8250 sq. mils
(2.79 × 1.91 mm, 5.33 sq. mm)

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$ for OP-215N, OP-215G and OP-215GR devices; $T_A = 125°C$ for OP-215NT and OP-215GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-215NT LIMIT	OP-215N LIMIT	OP-215GT LIMIT	OP-215G LIMIT	OP-215GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	2	1	3	2	6	mV MAX
Input Bias Current	I_B		±18	—	±18	—	—	nA MAX
Input Offset Current	I_{OS}		14	—	14	—	—	nA MAX
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$, $R_L = 2k\Omega$	30	150	30	75	50	V/mV MIN
Input Voltage Range	IVR		±10.2	±10.2	±10.2	±10.2	±10.1	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm IVR$	82	86	82	86	82	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10$ to $\pm 16V$ $V_S = \pm 10$ to $\pm 15V$	100 —	51 —	100 —	80 —	— 100	µV/V MAX
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$	±12 —	±12 ±11	±12 —	±12 ±11	±12 ±11	V MIN
Supply Current	I_{SY}		—	8.5	—	8.5	12.0	mA MAX

NOTES:
For 25°C characteristics of NT & GT devices, see N & G characteristics respectively.

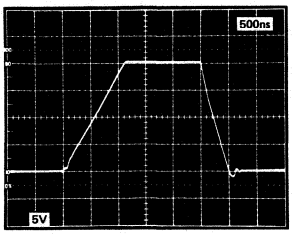
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

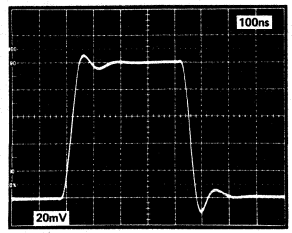
PARAMETER	SYMBOL	CONDITIONS	OP-215NT TYPICAL	OP-215N TYPICAL	OP-215GT TYPICAL	OP-215G TYPICAL	OP-215GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	Unnulled $R_P = 100k\Omega$	2	2	3	3	4	µV/°C
Average Input Offset Voltage Drift	TCV_{OSn}	Nulled $R_P = 100k\Omega$	0.5	0.5	1	1	2	µV/°C
Input Offset Current	I_{OS}		3	3	3	3	3	pA
Input Bias Current	I_B		±15	±15	±15	±15	±15	pA
Slew Rate	SR	$A_{VCL} = +1$	17	17	16	16	15	V/µs
Settling Time	t_S	to 0.01% to 0.05% to 0.10%	2.2 1.1 0.9	2.2 1.1 0.9	2.3 1.1 0.9	2.3 1.1 0.9	2.4 1.2 1.0	µs
Gain Bandwidth Product	GBW		6.0	6.0	5.7	5.7	5.4	MHz
Closed-Loop Bandwidth	CLBW	$A_{VCL} = +1$	14	14	13	13	12	MHz
Input Noise Voltage Density	e_n	$f_O = 100Hz$ $f_O = 1000Hz$	20 15	20 15	20 15	20 15	20 15	$nV/\sqrt{Hz}$
Input Noise Current Density	i_n	$f_O = 100Hz$ $f_O = 1000Hz$	0.01	0.01	0.01	0.01	0.01	$pA/\sqrt{Hz}$
Input Capacitance	C_{IN}		3	3	3	3	3	pF

TYPICAL PERFORMANCE CHARACTERISTICS

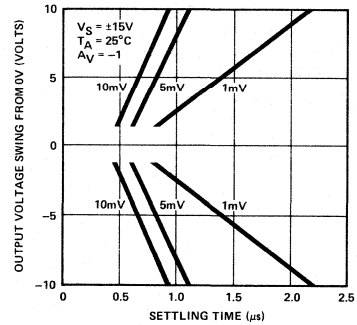
LARGE-SIGNAL TRANSIENT RESPONSE



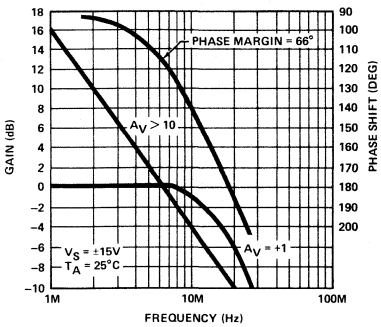
SMALL-SIGNAL TRANSIENT RESPONSE



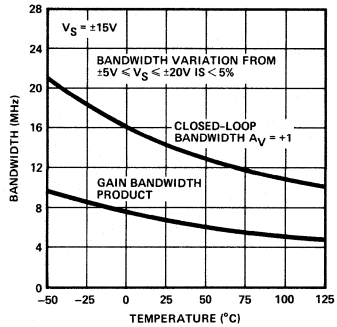
SETTLING TIME



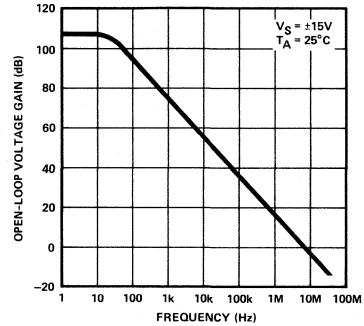
CLOSED-LOOP BANDWIDTH AND PHASE SHIFT vs FREQUENCY



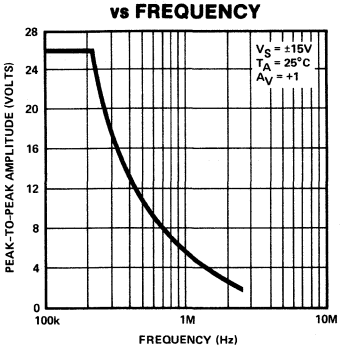
BANDWIDTH vs TEMPERATURE



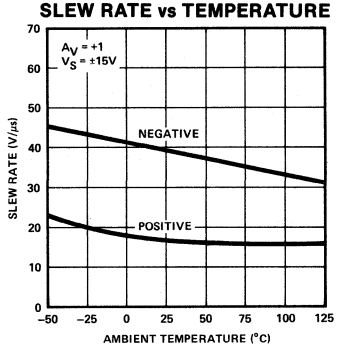
OPEN-LOOP FREQUENCY RESPONSE



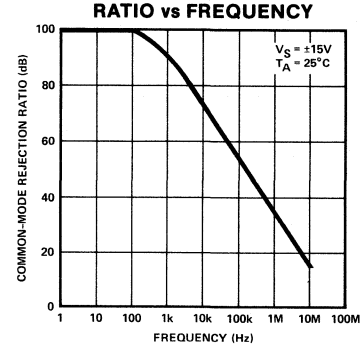
MAXIMUM OUTPUT SWING vs FREQUENCY



SLEW RATE vs TEMPERATURE



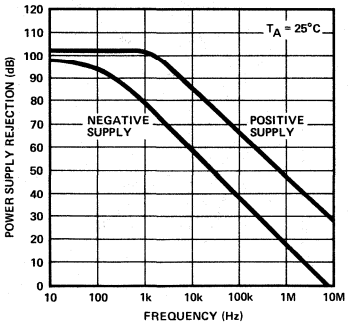
COMMON-MODE REJECTION RATIO vs FREQUENCY



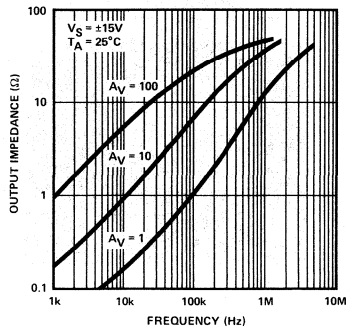
OP-215

TYPICAL PERFORMANCE CHARACTERISTICS

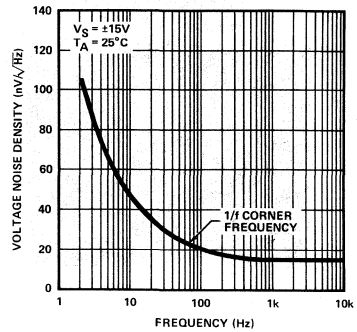
POWER SUPPLY REJECTION vs FREQUENCY



OUTPUT IMPEDANCE vs FREQUENCY

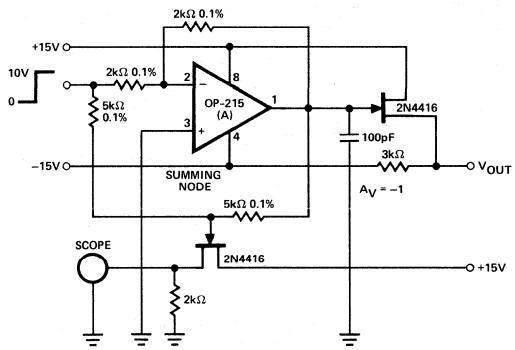


VOLTAGE NOISE DENSITY vs FREQUENCY



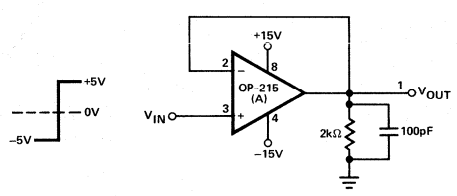
BASIC CONNECTIONS

SETTLING TIME TEST CIRCUIT



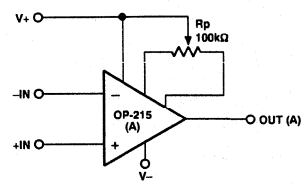
(PINOUT FOR "J," "Z" AND "P" PACKAGES ONLY)

SLEW RATE TEST CIRCUIT



(PINOUT FOR "J," "Z" AND "P" PACKAGES ONLY)

INPUT OFFSET VOLTAGE NULLING

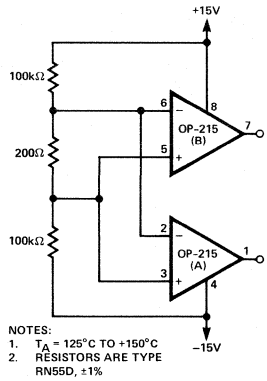


NOTE:
V_{OS} CAN BE TRIMMED WITH POTENTIOMETERS RANGING FROM 10kΩ TO 1MΩ. FOR MOST UNITS TCV_{OS} WILL BE MINIMUM WHEN V_{OS} IS ADJUSTED WITH A 100kΩ POTENTIOMETER.

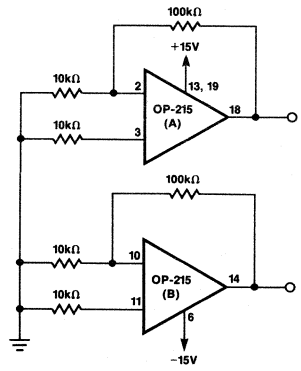
(DICE ONLY)

BASIC CONNECTIONS

BURN-IN CIRCUIT



("J," "Z" AND "P" PACKAGES ONLY)



("RC" PACKAGE)

APPLICATIONS INFORMATION

DYNAMIC OPERATING CONSIDERATIONS

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground sets the frequency of the pole. In many instances, the frequency of this pole is much greater than the expected 3dB frequency of the closed-loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3dB frequency, a lead capacitor should be placed from the output to the negative input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than, or equal to, the original feedback-pole time constant.

ANALOG DEVICES

Dual Micropower Operational Amplifier

OP-220

FEATURES

- **Excellent TCV_{OS} Match** ..... **2μV/°C Max**
- **Low Input Offset Voltage** ..... **150μV Max**
- **Low Supply Current** **100μA**
- **Single-Supply Operation** ..... **+5V to +30V**
- **Low Input Offset Voltage Drift** ..... **0.75μV/°C**
- **High Open-Loop Gain** **2000V/mV**
- **High PSRR** **3μV/V**
- **Low Input Bias Current** **12nA**
- **Wide Common-Mode Voltage Range** ..... **V− to within 1.5V of V+**
- **Pin Compatible with 1458, LM158, LM2904**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (μV)	PACKAGE TO-99	PACKAGE CERDIP 8-PIN	PACKAGE PLASTIC 8-PIN	OPERATING TEMPERATURE RANGE
150	OP220AJ*	OP220AZ	—	MIL
150	—	OP220EZ	—	IND
300	—	OP220FZ	—	IND
750	OP220CJ*	OP220CZ	—	MIL
750	OP220GJ	OP220GZ	OP220GP	XIND
750	—	—	OP220GS	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

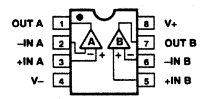
GENERAL DESCRIPTION

The OP-220 is a monolithic dual operational amplifier that can be used either in single or dual supply operation. The low offset voltage, and input offset voltage tracking as low as 1.0μV/°C, make this the first micropower precision dual operational amplifier.

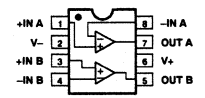
The excellent specifications of the individual amplifiers combined with the tight matching and temperature tracking between channels provides high performance in instrumentation amplifier designs. The individual amplifiers feature extremely low input offset voltage, low offset voltage drift, low noise voltage, and low bias current. They are fully compensated and protected.

Matching between channels is provided on all critical parameters including input offset voltage, tracking of offset voltage vs. temperature, non-inverting bias currents, and common-mode rejection ratios.

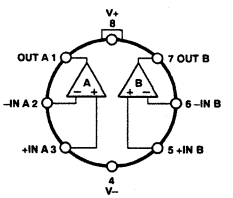
PIN CONNECTIONS



8-PIN HERMETIC DIP
(Z-Suffix)
8-PIN PLASTIC DIP
(P-Suffix)

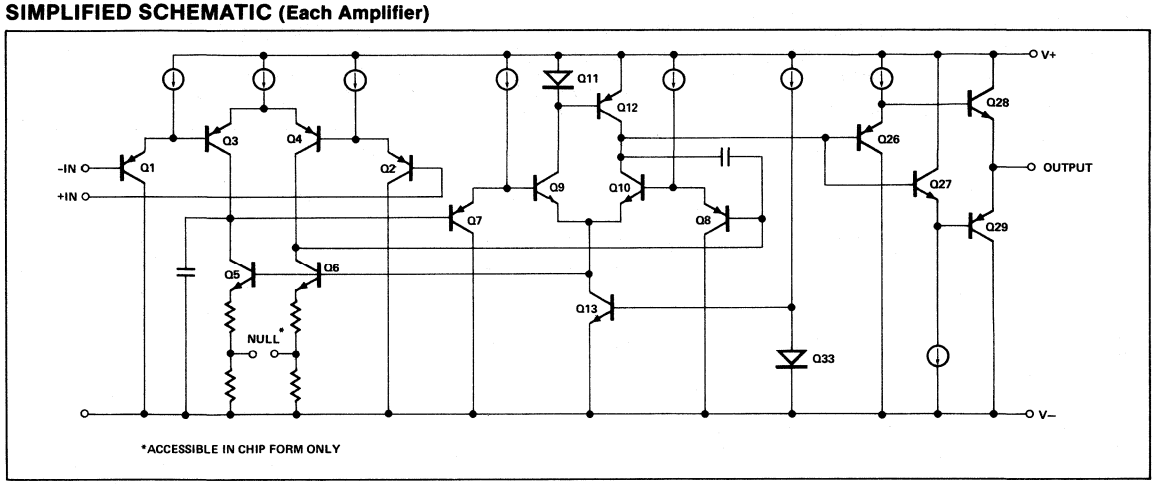


8-PIN SO
(S-Suffix)



TO-99
(J-Suffix)

SIMPLIFIED SCHEMATIC (Each Amplifier)



*ACCESSIBLE IN CHIP FORM ONLY

OP-220

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Differential Input Voltage ..... 30V or Supply Voltage
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range ..... –65°C to +150°C
Operating Temperature Range
OP-220A, C ..... –55°C to +125°C
OP-220E, F ..... –25°C to +85°C
OP-220G ..... –40°C to +85°C
Lead Temperature (Soldering, 60 sec) ..... +300°C
Junction Temperature (T_j) ..... –65°C to +150°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $T_A = +25°C$, unless otherwise noted.

			OP-220A/E			OP-220F			OP-220C/G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	120	150	—	250	300	—	500	750	µV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	0.15	1.5	—	0.2	2	—	0.2	3.5	nA
Input Bias Current	I_B	$V_{CM} = 0$	—	12	20	—	13	25	—	14	30	nA
Input Voltage Range	IVR	V+ = 5V, V– = 0V, $V_S = \pm 15V$	0/3.5 –15/13.5	—	—	0/3.5 –15/13.5	—	—	0/3.5 –15/13.5	—	—	V
Common-Mode Rejection Ratio	CMRR	V+ = 5V, V– = 0V, $0V \le V_{CM} \le 3.5V$ $V_S = \pm 15V$, $-15V \le V_{CM} \le 13.5V$	90 95	100 100	—	85 90	90 95	—	75 80	85 90	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ V– = 0V, V+ = 5V to 30V	—	3 6	10 18	—	10 18	32 57	—	32 57	100 180	µV/V
Large-Signal Voltage Gain	A_{VO}	V+ = 5V, V– = 0V, $R_L = 100k\Omega$ $1V \le V_O \le 3.5V$ $V_S = \pm 15V$, $R_L = 25k\Omega$ $V_O = \pm 10V$	500 1000	1000 2000	—	500 1000	800 2000	—	300 800	500 1600	—	V/mV
Output Voltage Swing	V_O	V+ = 5V, V– = 0V, $R_L = 10k\Omega$ $V_S = \pm 15V$, $R_L = 25k\Omega$	0.7/4 ±14	—	—	0.7/4 ±14	—	—	0.8/4 ±14	—	—	V
Slew Rate	SR	$R_L = 25k\Omega$, (Note 1)	—	0.05	—	—	0.05	—	—	0.05	—	V/µs
Bandwidth	BW	$A_{VCL} = +1$, $R_L = 25k\Omega$	—	200	—	—	200	—	—	200	—	kHz
Supply Current (Both Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load $V_S = \pm 15V$, No Load	—	100 140	115 170	—	115 150	125 190	—	125 205	135 220	µA

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $-55°C \le T_A \le +125°C$ for OP-220A and C, $-25°C \le T_A \le +85°C$ for OP-220E and F, $-40°C \le T_A \le +85°C$ for OP-220G, unless otherwise noted.

			OP-220A/E			OP-220F			OP-220C/G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	$V_S = \pm 15V$	—	0.75	1.5	—	1.2	2	—	2	3	µV/°C
Input Offset Voltage	V_{OS}		—	200	300	—	400	500	—	1000	1300	µV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	0.5	2	—	0.6	2.5	—	0.8	5	nA
Input Bias Current	I_B	$V_{CM} = 0$	—	12	25	—	13	30	—	14	40	nA
Input Voltage Range	IVR	V+ = 5V, V– = 0V, $V_S = \pm 15V$	0/3.2 –15/13.2	—	—	0/3.2 –15/13.2	—	—	0/3.2 –15/13.2	—	—	V
Common-Mode Rejection Ratio	CMRR	V+ = 5V, V– = 0V, $0V \le V_{CM} \le 3.2V$ $V_S = \pm 15V$ $-15V \le V_{CM} \le 13.2V$	85 90	90 95	—	80 85	85 90	—	70 75	80 85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ V– = 0V, V+ = 5V to 30V	—	6 10	18 32	—	18 32	57 100	—	57 100	180 320	µV/V

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $-55°C \le T_A \le +125°C$ for OP-220A and C, $-25°C \le T_A \le +85°C$ for OP-220E and F, $-40°C \le T_A \le +85°C$ for OP-220G, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	OP-220A/E MIN	OP-220A/E TYP	OP-220A/E MAX	OP-220F MIN	OP-220F TYP	OP-220F MAX	OP-220C/G MIN	OP-220C/G TYP	OP-220C/G MAX	UNITS
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 50k\Omega$ $V_O = \pm 10V$	500	1000	—	500	800	—	400	500	—	V/mV
Output Voltage Swing	V_O	$V+ = 5V$, $V- = 0V$, $R_L = 20k\Omega$	0.9/3.8	—	—	0.9/3.8	—	—	1/3.8	—	—	V
		$V_S = \pm 15V$, $R_L = 50k\Omega$	± 13.8	—	—	± 13.8	—	—	± 13.8	—	—	
Supply Current (Both Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load	—	135	170	—	155	185	—	170	210	μA
		$V_S = \pm 15V$, No Load	—	190	250	—	200	280	—	275	330	

NOTE: 1. Sample tested.

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-220A/E MIN	OP-220A/E TYP	OP-220A/E MAX	OP-220F MIN	OP-220F TYP	OP-220F MAX	OP-220C/G MIN	OP-220C/G TYP	OP-220C/G MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}		—	150	300	—	250	500	—	300	600	μV
Average Noninverting Bias Current	I_B+	$V_{CM} = 0$	—	10	20	—	15	25	—	20	30	nA
Noninverting Offset Current	$I_{OS}+$	$V_{CM} = 0$	—	0.7	1.5	—	1	2	—	1.4	2.5	nA
Common-Mode Rejection Ratio Match (Note 1)	ΔCMRR	$V_{CM} = -15V$ to $+13.5V$	92	100	—	87	95	—	72	85	—	dB
Power Supply Rejection Ratio Match (Note 2)	ΔPSRR	$V_S = \pm 2.5V$ to $\pm 15V$	—	6	14	—	18	44	—	57	140	μV/V

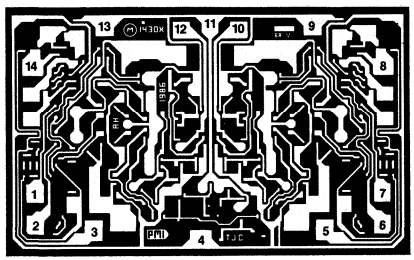
MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$ for OP-220A and C; $-25°C \le T_A \le +85°C$ for OP-220E and F; $-40°C \le T_A \le +85°C$ for OP-220G, unless otherwise noted. Grades E, F are sample tested.

PARAMETER	SYMBOL	CONDITIONS	OP-220A/E MIN	OP-220A/E TYP	OP-220A/E MAX	OP-220F MIN	OP-220F TYP	OP-220F MAX	OP-220C/G MIN	OP-220C/G TYP	OP-220C/G MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}		—	250	500	—	400	800	—	800	1800	μV
Input Offset Voltage Tracking	$TC\Delta V_{OS}$	(Note 3)	—	1	2	—	1.5	3	—	1.5	5	μV/°C
Average Noninverting Bias Current	I_B+	$V_{CM} = 0$	—	10	25	—	15	30	—	22	40	nA
Average Drift of Noninverting Bias Current	TCI_B+	$V_{CM} = 0$ (Note 3)	—	15	25	—	15	30	—	30	50	pA/°C
Noninverting Offset Current	$I_{OS}+$	$V_{CM} = 0$	—	0.7	2	—	1	2.5	—	2.5	5	nA
Average Drift of Noninverting Offset Current	$TCI_{OS}+$	$V_{CM} = 0$ (Note 3)	—	7	15	—	12	22.5	—	15	30	pA/°C
Common-Mode Rejection Ratio Match (Note 1)	ΔCMRR	$V_{CM} = -15V$ to $+13V$	87	98	—	82	96	—	72	80	—	dB
Power Supply Rejection Ratio Match (Note 2)	ΔPSRR	$V_S = \pm 2.5V$ to $\pm 15V$	—	10	26	—	30	78	—	57	250	μV/V

NOTES:
1. ΔCMRR is $20 \log_{10} V_{CM}/\Delta CME$, where V_{CM} is the voltage applied to both noninverting inputs and ΔCME is the difference in common-mode input-referred error.
2. ΔPSRR is: $\frac{\text{Input-referred differential error}}{\Delta V_S}$
3. Sample tested.

OP-220

DICE CHARACTERISTICS



DIE SIZE 0.097 × 0.063 inch, 6111 sq. mils
(2.464 × 1.600 mm, 3.94 sq. mm)

NOTE: All V+ PADS ARE INTERNALLY CONNECTED.

1. **INVERTING INPUT (A)**
2. **NONINVERTING INPUT (A)**
3. **BALANCE (A)**
4. **V−**
5. **BALANCE (B)**
6. **NONINVERTING INPUT (B)**
7. **INVERTING INPUT (B)**
8. **BALANCE (B)**
9. **V+**
10. **OUT (B)**
11. **V+**
12. **OUT (A)**
13. **V+**
14. **BALANCE (A)**

WAFER TEST LIMITS at $V_S = \pm 2.5V$ to $\pm 15V$, $T_A = 25°C$ for OP-220N, OP-220G and OP-220GR devices; $T_A = 125°C$ for OP-221NT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-220NT LIMIT	OP-220N LIMIT	OP-220G LIMIT	OP-220GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		350	200	500	1000	μV MAX
Input Offset Voltage Match	ΔV_{OS}		500	300	500	600	μV MAX
Input Offset Current	I_{OS}	$V_{CM} = 0$	2.5	2	3.5	5	nA MAX
Input Bias Current	I_B	$V_{CM} = 0$	30	25	30	40	nA MAX
Input Voltage Range	IVR	$V_S = \pm 15V$	−15/13.5	−15/13.5	−15/13.5	−15/13.5	V MIN
Common-Mode Rejection Ratio	CMRR	V− = 0V, V+ = 5V, $0V \le V_{CM} \le 3.5V$ $-15V \le V_{CM} \le 13.5V$, $V_S = \pm 15V$	83 88	88 93	83 88	75 80	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ V− = 0V, V+ = 5V to 30V	22 36	12.5 22.5	40 70	100 180	μV/V MAX
Large-Signal Voltage Gain	A_{VO}	$R_L = 25k\Omega$, $V_S = \pm 15V$ $V_O = \pm 10V$	—	1000	800	500	V/mV MIN
		$V_S = \pm 15V$, $R_L = 50k\Omega$ $V_O = \pm 10V$	500	—	—	—	
Output Voltage Swing	V_O	V+ = 5V, V− = 0V, $R_L = 10k\Omega$	—	0.7/4	0.8/4	0.8/3.8	V MIN
		$V_S = \pm 15V$, $R_L = 25k\Omega$	—	±14	±14	±13.8	
		V+ = 5V, V− = 0V, $R_L = 20k\Omega$	0.9/3.8	—	—	—	
		$V_S = \pm 15V$, $R_L = 50k\Omega$	±13.8	—	—	—	
Supply Current (Both Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load $V_S = \pm 15V$, No Load	170 250	125 190	135 220	170 300	μA MAX

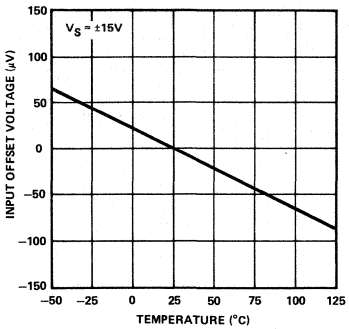
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

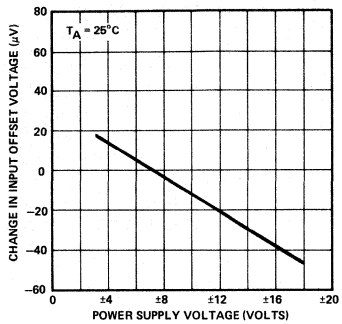
PARAMETER	SYMBOL	CONDITIONS	OP-220NT TYPICAL	OP-220N TYPICAL	OP-220G TYPICAL	OP-220GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}		1.5	1.5	2	3	μV/°C
Large-Signal Voltage Gain	A_{VO}	$R_L = 25k\Omega$	2000	2000	1600	800	V/mV

TYPICAL PERFORMANCE CHARACTERISTICS

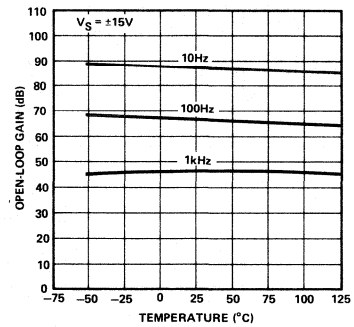
NORMALIZED OFFSET VOLTAGE vs TEMPERATURE



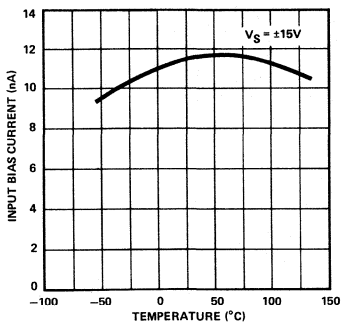
INPUT OFFSET VOLTAGE vs POWER SUPPLY VOLTAGE



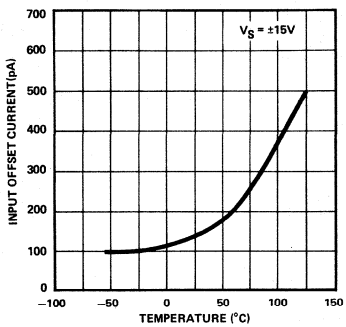
OPEN-LOOP GAIN vs TEMPERATURE



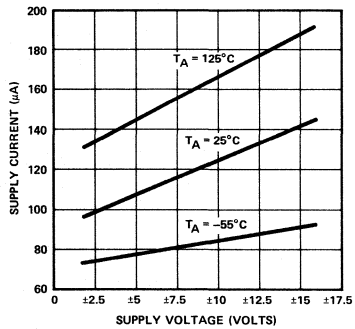
INPUT BIAS CURRENT vs TEMPERATURE



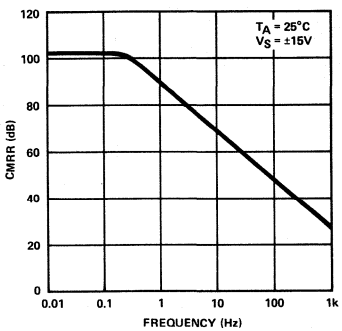
INPUT OFFSET CURRENT vs TEMPERATURE



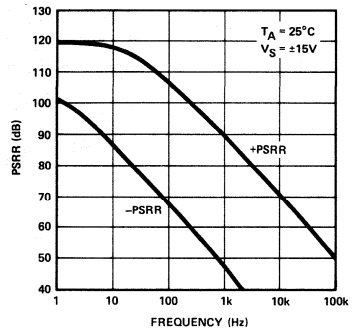
SUPPLY CURRENT vs SUPPLY VOLTAGE



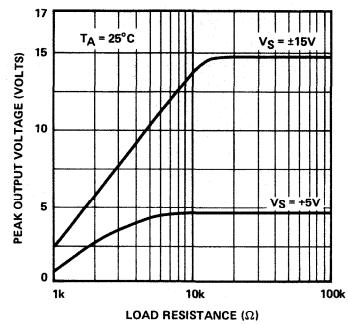
CMRR vs FREQUENCY



PSRR vs FREQUENCY



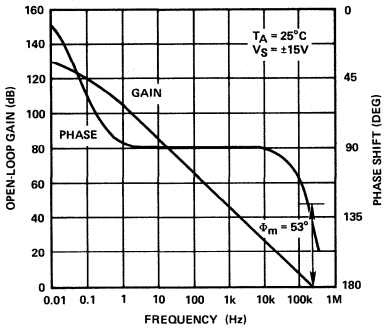
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



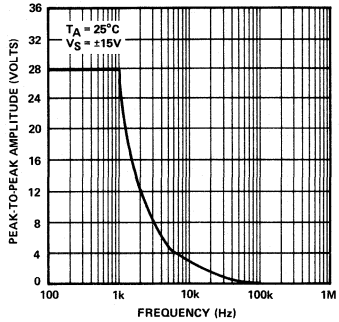
2

TYPICAL PERFORMANCE CHARACTERISTICS

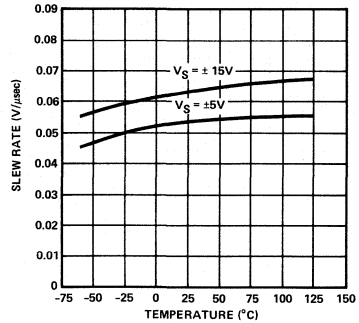
OPEN-LOOP VOLTAGE GAIN AND PHASE vs FREQUENCY



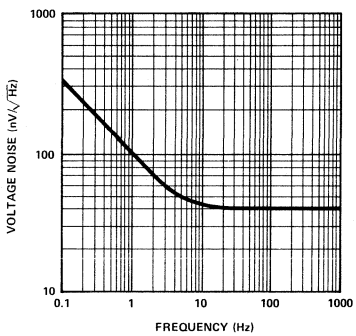
MAXIMUM OUTPUT SWING vs FREQUENCY



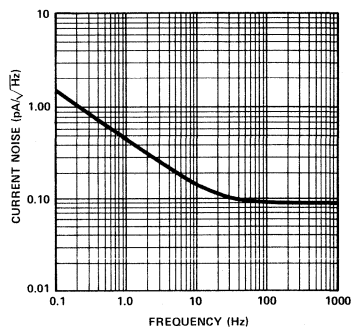
SLEW RATE vs TEMPERATURE



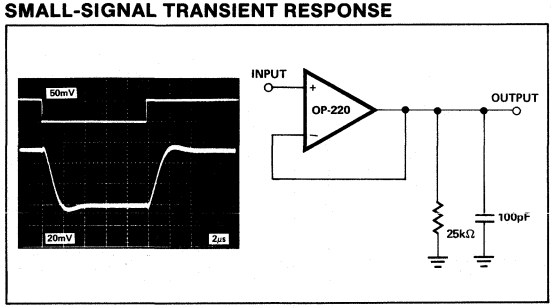
VOLTAGE NOISE DENSITY (e_n) vs FREQUENCY



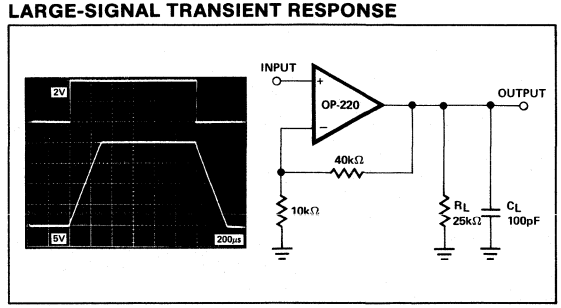
CURRENT NOISE DENSITY (i_n) vs FREQUENCY



SMALL-SIGNAL TRANSIENT RESPONSE



LARGE-SIGNAL TRANSIENT RESPONSE



INSTRUMENTATION AMPLIFIER APPLICATIONS OF THE OP-220

TWO-OP-AMP CONFIGURATION

The excellent input characteristics of the OP-220 make it ideal for use in *instrumentation amplifier* configurations where low-level differential signals are to be amplified. The low-noise, low input offsets, low drift, and high gain combined with excellent CMRR provide the characteristics needed for high-performance instrumentation amplifiers. In addition, the power supply current drain is very low.

The circuit of Figure 1 is recommended for applications where the common-mode input range is relatively low and differential gain will be in the range of 10 to 1000. This two-op-amp instrumentation amplifier features *independent* adjustment of common-mode rejection and differential gain. Input impedance is very high since both inputs are applied to noninverting op amp inputs.

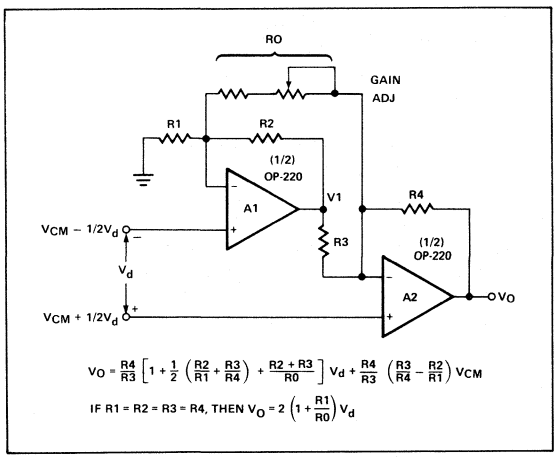


Figure 1. Two-Op-Amp Instrumentation Amplifier Configuration

The input voltages are represented as a common-mode input V_{CM} plus a differential input V_d. The ratio R_3/R_4 is made equal to the ratio R_2/R_1 to reject the common-mode input V_{CM}. The differential signal V_d is then amplified according to:

$$V_O = \frac{R_4}{R_3}\left(1 + \frac{R_3}{R_4} + \frac{R_2 + R_3}{R_O}\right) V_d, \text{ where } \frac{R_3}{R_4} = \frac{R_2}{R_1}$$

Note that gain can be independently varied by adjusting R_O. From considerations of dynamic range, resistor tempco matching, and matching of amplifier response, it is generally best to make R_1, R_2, R_3, and R_4 approximately equal. Designating R_1, R_2, R_3, and R_4 as R_N allows the output equation to be further simplified:

$$V_O = 2\left(1 + \frac{R_N}{R_O}\right) V_d, \text{ where } R_N = R_1 = R_2 = R_3 = R_4$$

Dynamic range is limited by A1 as well as A2; the output of A1 is:

$$V_1 = -\left(1 + \frac{R_N}{R_O}\right) V_d + 2\,V_{CM}$$

If the instrumentation amplifier were designed for a gain of 10 and maximum V_d of ±1V, then R_N/R_O would need to be four and V_O would be a maximum of ±10V. Amplifier A1 would have a maximum output of ±5V plus $2V_{CM}$, thus a limit of ±10V on the output of A1 would imply a limit of ±2.5V on V_{CM}.

A nominal value of 100kΩ for R_N is suitable for most applications. A range of 200Ω to 25kΩ for R_O will then provide a gain range of 10 to 1000. The current through R_O is V_d/R_O, so the amplifiers must supply ±10mV/200Ω when the gain is at the maximum value of 1000 and V_d is at ±10mV.

Rejecting common-mode inputs is most important in accurately amplifying low-level differential signals. Two factors determine the CMR of this instrumentation amplifier configuration (assuming infinite gain):

(1) CMRR of the op amps
(2) Matching of the resistor network ($R_3/R_4 = R_2/R_1$)

In this instrumentation amplifier configuration, error due to CMRR effect is directly proportional to the *differential* CMRR of the op amps. For the OP-220A/E, this combined CMRR is a minimum of 98dB. A combined CMRR value of 100dB and common-mode input range of ±2.5V indicates a peak input-referred error of only ±25μV.

Resistor matching is the other factor affecting CMRR. Defining A_d as the differential gain of the instrumentation amplifier and assuming that R_1, R_2, R_3 and R_4 are approximately equal (R_N will be the nominal value), then CMRR will be approximately A_d divided by $4\Delta R/R_N$. CMRR at differential gain of 100 would be 88dB with resistor matching of 0.1%. Trimming R_1 to make the ratio R_3/R_4 equal to R_2/R_1 will directly raise the CMRR until it is limited by linearity and resistor stability considerations.

The high open-loop gain of the OP-220 is very important in achieving high accuracy in the two-op-amp instrumentation amplifier configuration. Gain error can be approximated by:

$$\text{Gain Error} \sim \frac{1}{1 + \frac{A_d}{A_{02}}}, \quad \frac{A_d}{2\,A_{01}\,A_{02}} \ll 1$$

where A_d is the instrumentation amplifier differential gain and A_{02} is the open-loop gain of op amp A2. This analysis assumes equal values of R_1, R_2, R_3, and R_4. For example, consider an OP-220 with A_{02} of 700V/mV. If the differential gain A_d were set to 700, the gain error would be 1/1.001 which is approximately 0.1%.

Another effect of finite op amp gain is undesired feedthrough of common-mode input. Defining A_{01} as the open-loop gain of op amp A1, then the common-mode error (CME) at the output due to this effect will be approximately

$$\text{CME} \sim \frac{2\,A_d}{1 + \frac{A_d}{A_{01}}} \frac{1}{A_{01}} V_{CM}$$

For $A_d/A_{01}, \ll 1$, this simplifies to $(2\,A_d/A_{01}) \times V_{CM}$. If the op amp gain is 700V/mV, V_{CM} is 2.5V, and A_d is set to 700, then the error at the output due to this effect will be approximately 5mV.

The OP-220 offers a unique combination of excellent dc performance, wide input range, and low supply current drain that is particularly attractive for instrumentation amplifier design.

THREE-OP-AMP CONFIGURATION

A three-op-amp instrumentation amplifier configuration using the OP-220 and OP-22 is recommended for applications requiring high accuracy over a wide gain range. This circuit provides excellent CMR over a wide input range. As with the two-op-amp instrumentation amplifier circuits, tight matching of the two op amps provides a real boost in performance. The OP-22 is a micropower op-amp featuring programmable supply current.

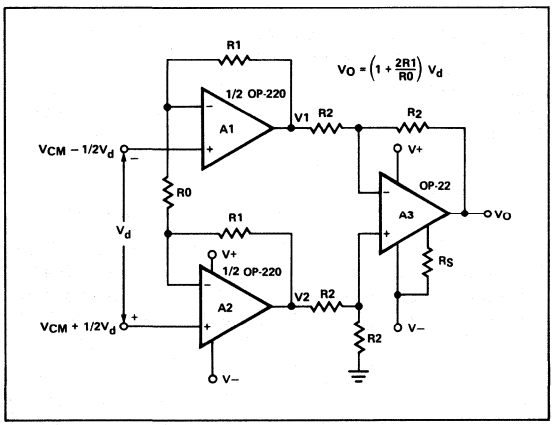


Figure 2. Three-Op-Amp Instrumentation Amplifier Using OP-220 and OP-22

A simplified schematic is shown in Figure 2. The input stage (A1 and A2) serves to amplify the differential input V_d without amplifying the common-mode voltage V_{CM}. The output stage then rejects the common-mode input. With ideal op-amps and no resistor matching errors, the outputs of each amplifier will be:

$$V_1 = -\left(1 + \frac{2R_1}{R_O}\right)\frac{V_d}{2} + V_{CM}$$

$$V_2 = \left(1 + \frac{2R_1}{R_O}\right)\frac{V_d}{2} + V_{CM}$$

$$V_O = V_2 - V_1 = \left(1 + \frac{2R_1}{R_O}\right)V_d$$

$$V_O = A_d\,V_d$$

The differential gain A_d is $1 + 2R_1/R_O$ and the common-mode input V_{CM} is rejected.

This three-op-amp instrumentation amplifier configuration using an OP-220 at the input and an OP-22 at the output provides excellent performance over a wide gain range with very low power consumption. A gain range of 1 to 2000 is practical and CMR of over 120dB is readily achievable.

ANALOG DEVICES

Dual Low-Power Operational Amplifier, Single or Dual Supply

OP-221

FEATURES

- **Excellent TCV_{OS} Match ..... 2μV/°C Max**
- **Low Input Offset Voltage ..... 150μV Max**
- **Low Supply Current ..... 550μA Max**
- **Single Supply Operation ..... +5V to +30V**
- **Low Input Offset Voltage Drift ..... 0.75μV/°C**
- **High Open-Loop Gain ..... 1500V/mV Min**
- **High PSRR 3μV/V**
- **Wide Common-Mode Voltage Range ..... V− to within 1.5V of V+**
- **Pin Compatible with 1458, LM158, LM2904**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (μV)	PACKAGE TO-99	PACKAGE CERDIP 8-PIN	PACKAGE PLASTIC 8-PIN	OPERATING TEMPERATURE RANGE
150	OP-221AJ/883	OP221AZ*	–	MIL
150	–	OP221EZ	–	IND
300	OP221BJ	–	–	MIL
500	OP221CJ	–	–	MIL
500	OP221GJ	OP221GZ	OP221GP	XIND
500	–	–	OP221GS	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

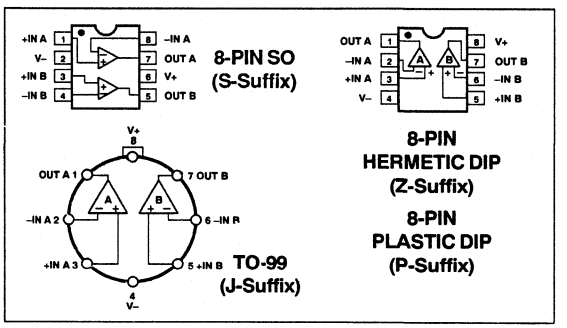
GENERAL DESCRIPTION

The OP-221 is a monolithic dual operational amplifier that can be used either in single or dual supply operation. The wide supply voltage range, wide input voltage range, and low supply current drain of the OP-221 make it well-suited for operation from batteries or unregulated power supplies.

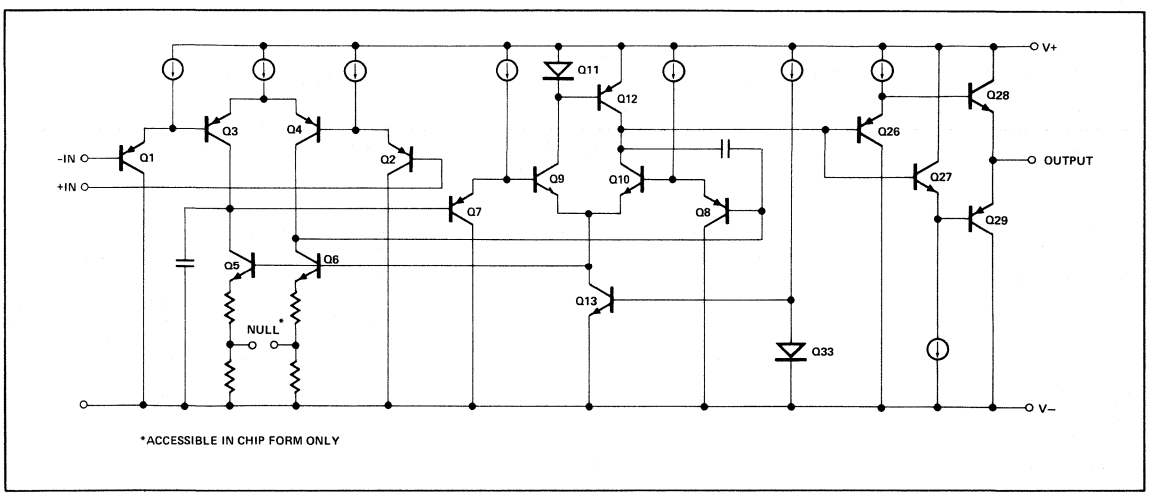
The excellent specifications of the individual amplifiers combined with the tight matching and temperature tracking between channels provide high performance in instrumentation amplifier designs. The individual amplifiers feature very low input offset voltage, low offset voltage drift, low noise voltage, and low bias current. They are fully compensated and protected.

Matching between channels is provided on all critical parameters including input offset voltage, tracking of offset voltage vs. temperature, non-inverting bias currents, and common-mode rejection.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC (Each Amplifier)



OP-221

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Differential Input Voltage ..... 30V or Supply Voltage
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range ..... –65°C to +150°C
Operating Temperature Range
OP-221A, B, C ..... –55°C to +125° C
OP-221E ..... –25°C to +85°C
OP-221G ..... –40°C to +85°C
Lead Temperature (Soldering, 60 sec) ..... +300°C
Junction Temperature (T_j) ..... –65°C to +150°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-221A/E MIN	OP-221A/E TYP	OP-221A/E MAX	OP-221B MIN	OP-221B TYP	OP-221B MAX	OP-221C/G MIN	OP-221C/G TYP	OP-221C/G MAX	UNITS
Input Offset Voltage	V_{OS}		—	75	150	—	150	300	—	250	500	µV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	0.5	3	—	1	5	—	1.5	7	nA
Input Bias Current	I_B	$V_{CM} = 0$	—	50	80	—	60	100	—	70	120	nA
Input Voltage Range	IVR	V+ = 5V, V– = 0V (Note 2)	0/3.5	—	—	0/3.5	—	—	0/3.5	—	—	V
		$V_S = \pm 15V$	–15/13.5	—	—	–15/13.5	—	—	–15/13.5	—	—	
Common-Mode Rejection Ratio	CMRR	V+ = 5V, V– = 0V $0V \le V_{CM} \le 3.5V$	90	100	—	85	90	—	75	85	—	dB
		$V_S = \pm 15V$ $-15V \le V_{CM} \le 13.5V$	95	100	—	90	95	—	80	90	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$	—	3	10	—	10	32	—	32	100	µV/V
		V– = 0V, V+ = 5V to 30V	—	6	18	—	18	57	—	57	180	
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 10k\Omega$ $V_O = \pm 10V$	1500	—	—	1000	—	—	800	—	—	V/mV
Output Voltage Swing	V_O	V+ = 5V, V– = 0V, $R_L = 10k\Omega$	0.7/4.1	—	—	0.7/4.1	—	—	0.8/4	—	—	V
		$V_S = \pm 15V$, $R_L = 10k\Omega$	±13.8	—	—	±13.8	—	—	±13.5	—	—	
Slew Rate	SR	$R_L = 10k\Omega$, (Note 1)	0.2	0.3	—	0.2	0.3	—	0.2	0.3	—	V/µs
Bandwidth	BW		—	600	—	—	600	—	—	600	—	kHz
Supply Current (Both Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load	—	450	550	—	500	600	—	550	650	µA
		$V_S = \pm 15V$, No Load	—	600	800	—	800	850	—	850	900	

NOTES:
1. Sample tested.
2. Guaranteed by CMRR test limits.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $-55°C \le T_A \le +125°C$ for OP-221A, B, and C, $-25°C \le T_A \le +85°C$ for OP-221E, $-40°C \le T_A \le +85°C$ for OP-221G, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-221A/E MIN	OP-221A/E TYP	OP-221A/E MAX	OP-221B MIN	OP-221B TYP	OP-221B MAX	OP-221C/G MIN	OP-221C/G TYP	OP-221C/G MAX	UNITS
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}		—	0.75	1.5	—	1.2	2	—	2	3	µV/°C
Input Offset Voltage	V_{OS}		—	150	300	—	250	450	—	400	700	µV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	1	5	—	1.5	7	—	2	10	nA
Input Bias Current	I_B	$V_{CM} = 0$	—	55	100	—	65	120	—	80	140	nA
Input Voltage Range	IVR	V+ = 5V, V– = 0V (Note 2)	0/3.2	—	—	0/3.2	—	—	0/3.2	—	—	V
		$V_S = \pm 15V$	–15/13.2	—	—	–15/13.2	—	—	–15/13.2	—	—	
Common-Mode Rejection Ratio	CMRR	V+ = 5V, V– = 0V $0V \le V_{CM} \le 3.2V$	85	90	—	80	85	—	70	80	—	dB
		$V_S = \pm 15V$ $-15V \le V_{CM} \le 13.2V$	90	95	—	85	90	—	75	85	—	

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $-55°C \le T_A \le +125°C$ for OP-221A, B, and C, $-25°C \le T_A \le +85°C$ for OP-221E, $-40°C \le T_A \le +85°C$ for OP-221G, unless otherwise noted. *(Continued)*

PARAMETER	SYMBOL	CONDITIONS	OP-221A/E MIN	OP-221A/E TYP	OP-221A/E MAX	OP-221B MIN	OP-221B TYP	OP-221B MAX	OP-221C/G MIN	OP-221C/G TYP	OP-221C/G MAX	UNITS
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$	—	6	18	—	18	57	—	57	180	μV/V
		$V- = 0V$, $V+ = 5V$ to $30V$	—	10	32	—	32	100	—	100	320	
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 10k\Omega$, $V_O = \pm 10V$	1000	—	—	800	—	—	600	—	—	V/mV
Output Voltage Swing	V_O	$V+ = 5V$, $V- = 0V$, $R_L = 10k\Omega$	0.8/3.8	—	—	0.8/3.8	—	—	0.9/3.7	—	—	V
		$V_S = \pm 15V$, $R_L = 10k\Omega$	±13.5	±14	—	±13.5	±14	—	±13.2	—	—	
Supply Current (Both Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load	—	500	650	—	550	700	—	600	750	μA
		$V_S = \pm 15V$, No Load	—	700	900	—	900	950	—	950	1000	

NOTES:
1. Sample tested.
2. Guaranteed by CMRR test limits.

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-221A/E MIN	OP-221A/E TYP	OP-221A/E MAX	OP-221B MIN	OP-221B TYP	OP-221B MAX	OP-221C/G MIN	OP-221C/G TYP	OP-221C/G MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}		—	50	200	—	150	400	—	250	600	μV
Average Noninverting Bias Current	I_B+		—	—	80	—	—	100	—	—	120	nA
Noninverting Input Offset Current	$I_{OS}+$		—	2	5	—	2	5	—	4	10	nA
Common-Mode Rejection Ratio Match (Note 1)	ΔCMRR	$V_{CM} = -15V$ to $+13.5V$	92	—	—	87	—	—	72	—	—	dB
Power Supply Rejection Ratio Match (Note 2)	ΔPSRR	$V_S = \pm 2.5V$ to $\pm 15V$	—	—	14	—	—	44	—	—	140	μV/V

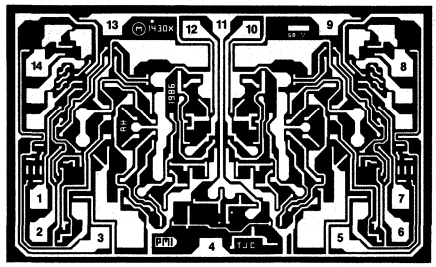
MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$ for OP-221A, B, and C, $-25°C \le T_A \le +85°C$ for OP-221E, $-40°C \le T_A \le +85°C$ for OP-221G, unless otherwise noted. Grades E and G are sample tested.

PARAMETER	SYMBOL	CONDITIONS	OP-221A/E MIN	OP-221A/E TYP	OP-221A/E MAX	OP-221B MIN	OP-221B TYP	OP-221B MAX	OP-221C/G MIN	OP-221C/G TYP	OP-221C/G MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}		—	100	400	—	250	600	—	400	800	μV
Average Noninverting Bias Current	I_B+	$V_{CM} = 0$	—	—	100	—	—	120	—	—	140	nA
Input Offset Voltage Tracking	$TC\Delta V_{OS}$		—	1	2	—	1	3	—	3	5	μV/°C
Noninverting Input Offset Current	$I_{OS}+$	$V_{CM} = 0$	—	3	7	—	3	7	—	6	12	nA
Common-Mode Rejection Ratio Match (Note 1)	ΔCMRR	$V_{CM} = -15V$ to $+13.2V$	87	90	—	82	85	—	72	80	—	dB
Power Supply Rejection Ratio Match (Note 2)	ΔPSRR		—	—	26	—	—	78	—	—	250	μV/V

NOTES:
1. ΔCMRR is $20 \log_{10} V_{CM}/\Delta CME$, where V_{CM} is the voltage applied to both noninverting inputs and ΔCME is the difference in common-mode input-referred error.
2. ΔPSRR is: $\frac{\text{Input-Referred Differential Error}}{\Delta V_S}$

OP-221

DICE CHARACTERISTICS



DIE SIZE 0.097 × 0.063 inch, 6111 sq. mils
(2.464 × 1.600 mm, 3.94 sq. mm)

NOTE: All V+ PADS ARE INTERNALLY CONNECTED.

1. INVERTING INPUT (A)
2. NONINVERTING INPUT (A)
3. BALANCE (A)
4. V−
5. BALANCE (B)
6. NONINVERTING INPUT (B)
7. INVERTING INPUT (B)
8. BALANCE (B)
9. V+
10. OUT (B)
11. V+
12. OUT (A)
13. V+
14. BALANCE (A)

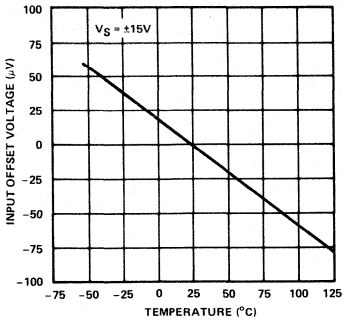
WAFER TEST LIMITS at $V_S = \pm 2.5V$ to $\pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-221N LIMIT	OP-221G LIMIT	OP-221GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		200	350	500	μV MAX
Input Offset Current	I_{OS}	$V_{CM} = 0$	3.5	5.5	7	nA MAX
Input Bias Current	I_B	$V_{CM} = 0$	85	105	120	nA MAX
Input Voltage Range	IVR	V+ = 5V, V− = 0V	0/3.5	0/3.5	0/3.5	V MIN/MAX
		$V_S = \pm 15V$	−15/13.5	−15/13.5	−15/13.5	V MIN
Common-Mode Rejection Ratio	CMRR	V− = 0V, V+ = 5V, $0V \le V_{CM} \le 3.5V$	88	83	75	dB MIN
		$V_S = \pm 15V$, $-15V \le V_{CM} \le 13.5V$	93	88	80	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$	12.5	40	100	μV/V MAX
		V− = 0V, V+ = 5V to 30V	22.5	70	180	
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 10k\Omega$	1500	1000	800	V/mV MIN
Output Voltage Swing	V_O	V+ = 5V, V− = 0V, $R_L = 10k\Omega$	0.7/4.1	0.7/4.1	0.8/4	V MIN/MAX
		$V_S = \pm 15V$, $R_L = 10k\Omega$	±13.8	±13.8	±13.5	V MIN
Supply Current (Both Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load	560	610	650	μA MAX
		$V_S = \pm 15V$, No Load	810	860	900	

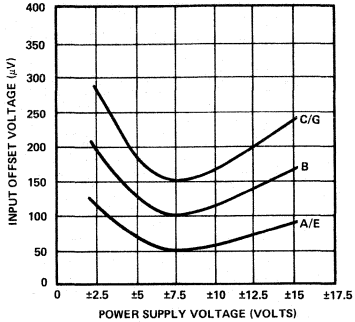
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

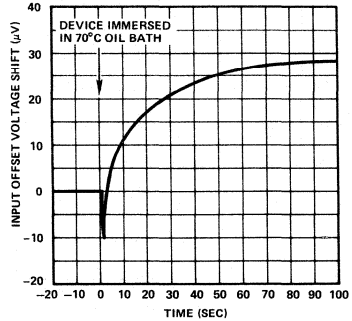
NORMALIZED INPUT OFFSET VOLTAGE vs TEMPERATURE



INPUT OFFSET VOLTAGE vs SUPPLY VOLTAGE

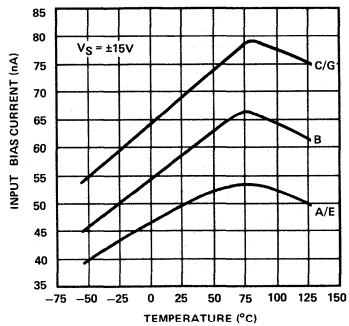


OFFSET VOLTAGE SHIFT DUE TO THERMAL SHOCK

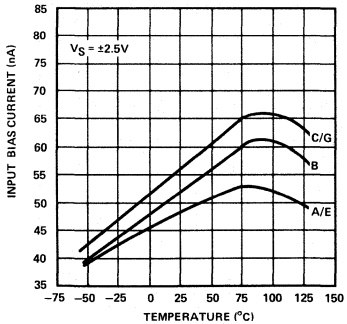


2

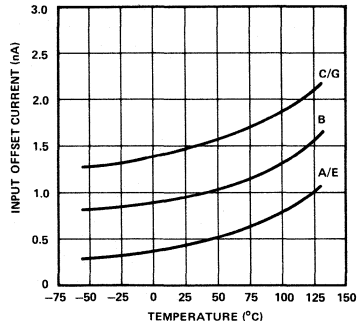
INPUT BIAS CURRENT vs TEMPERATURE



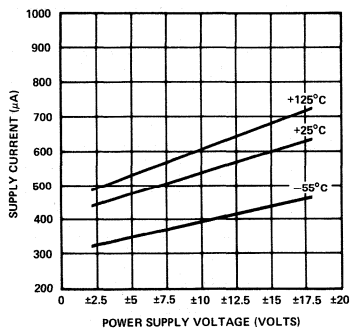
INPUT BIAS CURRENT vs TEMPERATURE



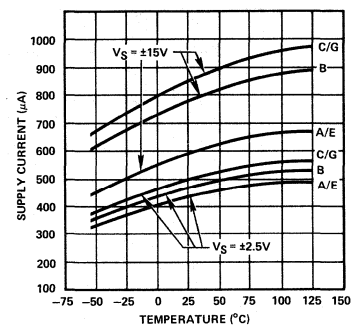
INPUT OFFSET CURRENT vs TEMPERATURE



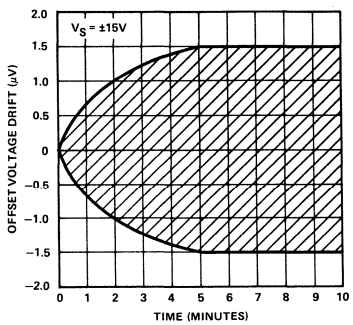
SUPPLY CURRENT vs SUPPLY VOLTAGE FOR OP-221A/E



SUPPLY CURRENT vs TEMPERATURE AT $V_S = \pm 15V$ AND $\pm 2.5V$



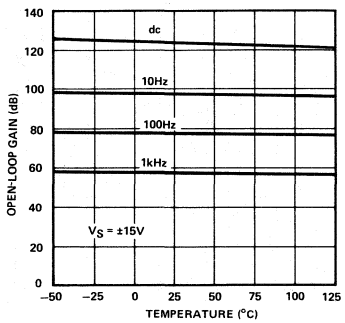
INITIAL OFFSET VOLTAGE DRIFT vs TIME



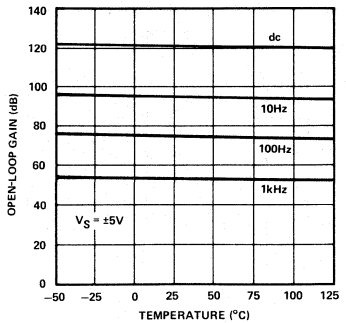
OP-221

TYPICAL PERFORMANCE CHARACTERISTICS

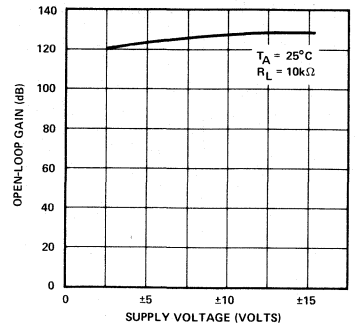
OPEN-LOOP GAIN AT ±15V vs TEMPERATURE



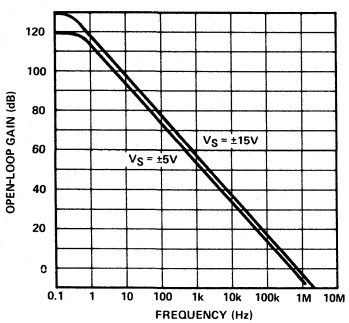
OPEN-LOOP GAIN AT ±5V vs TEMPERATURE



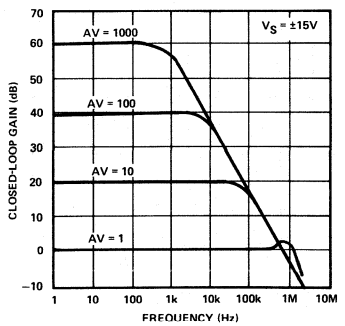
OPEN-LOOP GAIN vs SUPPLY VOLTAGE



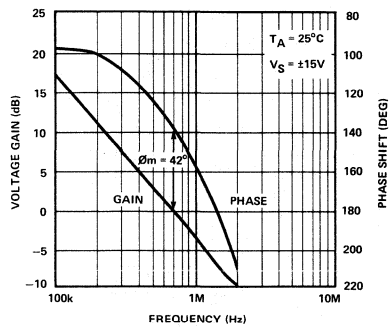
OPEN-LOOP GAIN vs FREQUENCY



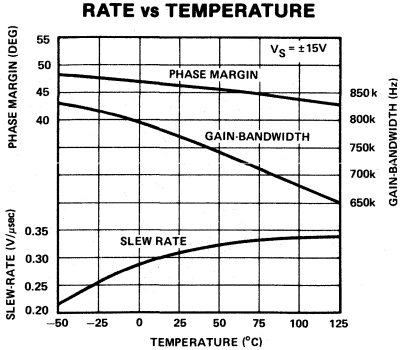
CLOSED-LOOP GAIN vs FREQUENCY



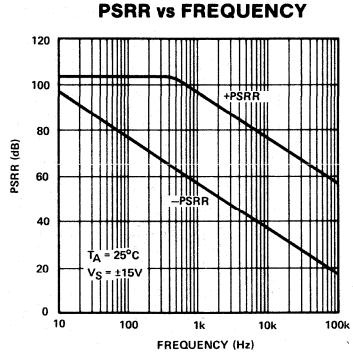
GAIN AND PHASE SHIFT vs FREQUENCY



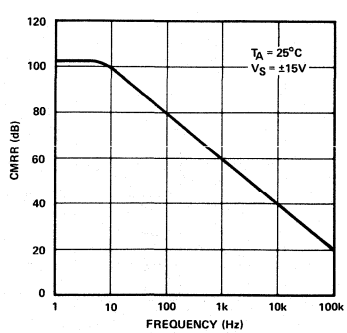
PHASE MARGIN, GAIN-BANDWIDTH, AND SLEW RATE vs TEMPERATURE



PSRR vs FREQUENCY

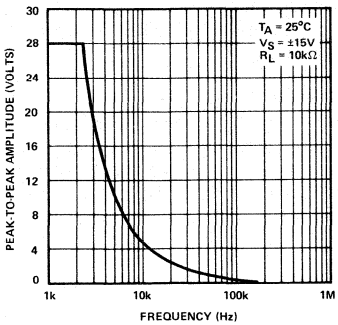


CMRR vs FREQUENCY

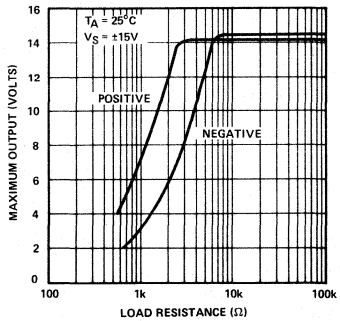


TYPICAL PERFORMANCE CHARACTERISTICS

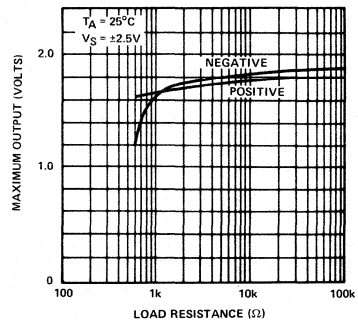
MAXIMUM OUTPUT SWING vs FREQUENCY



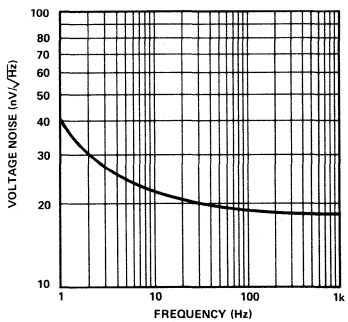
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



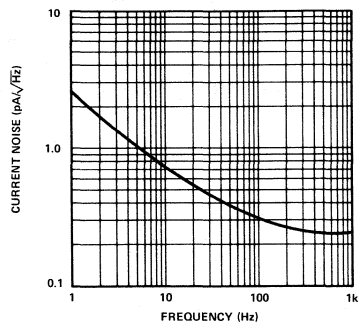
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



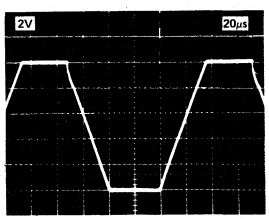
VOLTAGE NOISE DENSITY (e_n) vs FREQUENCY

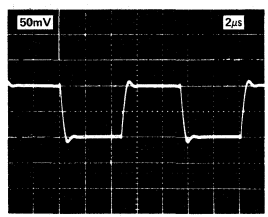


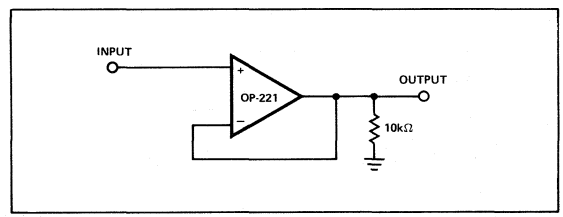
CURRENT NOISE DENSITY (i_n) vs FREQUENCY



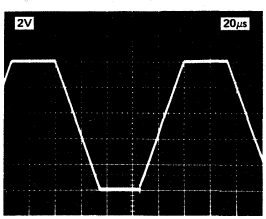
NONINVERTING STEP RESPONSE

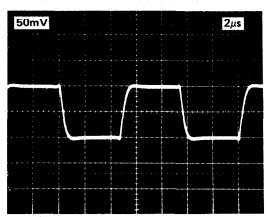


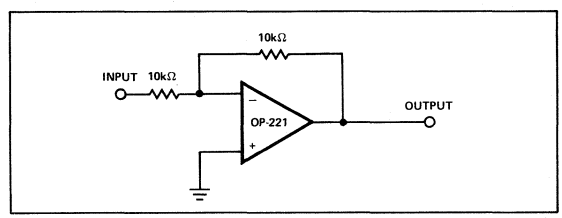




INVERTING STEP RESPONSE







SPECIAL NOTES ON THE APPLICATION OF DUAL MATCHED OPERATIONAL AMPLIFIERS

ADVANTAGES OF DUAL MONOLITHIC OPERATIONAL AMPLIFIERS

Dual matched operational amplifiers provide the engineer with a powerful tool for designing instrumentation amplifiers and many other differential-input circuits. These designs are based on the principle that careful matching between two operational amplifiers can minimize the effect of DC errors in the individual amplifiers.

Reference to the circuit shown in Figure 1, a differential-in, differential-out amplifier, shows how the reductions in error can be accomplished. Assuming the resistors used are ideally matched, the gain of each side will be identical. If the offset voltages of each amplifier are perfectly matched, then the net differential voltage at the amplifier's output will be zero. Note that the output offset error of this amplifier is not a function of the offset voltage of the individual amplifiers, but only a function of the *difference* (degree of matching) between the amplifiers' offset voltages. This error-cancellation principle holds for a considerable number of input referred error parameters — offset voltage, offset voltage drift, inverting and noninverting bias currents, common-mode and power supply rejection ratios. Note also that the impedances of each input, both common-mode and differential-mode, are high and tightly matched, an important feature not practical with single operational amplifier circuits.

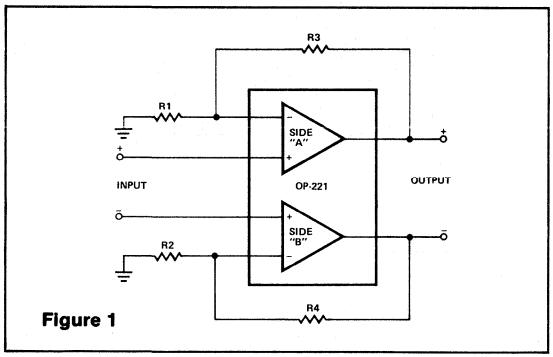


Figure 1

INSTRUMENTATION AMPLIFIER APPLICATIONS

Two-Op-Amp Configuration

The two-op-amp circuit (Figure 2), is recommended where the common-mode input voltage range is relatively limited; the common-mode and differential voltage both appear at V1.

The high open-loop gain of the OP-221 is very important in achieving good CMRR in this configuration. Finite open-loop gain of A1 (A_{01}) causes undesired feedthrough of the common-mode input. For $A_d/A_{01} << 1$, the common-mode error (CME) at the output due to this effect is approximately $(2\ A_d/A_{01}) \times V_{CM}$. This circuit features independent adjustment of CMRR and differential gain.

Three-Op-Amp Configuration

The three-op-amp circuit (Figure 3), has increased common-mode voltage range because the common-mode voltage is not amplified as it is in Figure 2. The CMR of this amplifier is directly proportional to the match of the CMR of the input op amps. CMRR can be raised even further by trimming the output stage resistors.

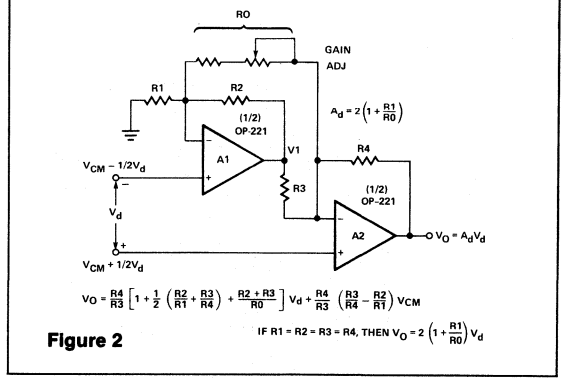


Figure 2

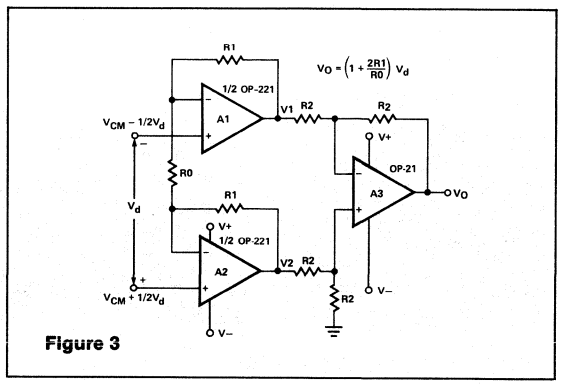


Figure 3

ANALOG DEVICES

Dual, Low-Noise Low-Offset Instrumentation Operational Amplifier

OP-227

FEATURES

- **Excellent Individual Amplifier Parameters**
- **Low V_{OS} ..... 80μV Max**
- **Offset Voltage Match ..... 80μV Max**
- **Offset Voltage Match vs Temperature ..... 1μV/°C Max**
- **Stable V_{OS} vs Time ..... 1μV/Mo Max**
- **Low Voltage Noise ..... 3.9nV/$\sqrt{Hz}$ Max**
- **Fast ..... 2.8V/μs Typ**
- **High Gain ..... 1.8 Million Typ**
- **High Channel Separation ..... 154dB Typ**

ORDERING INFORMATION†

T_A = 25°C V_{OS} MAX (μV)	HERMETIC DIP 14-PIN	OPERATING TEMPERATURE RANGE
80	OP227AY*	MIL
80	OP227EY	IND
120	OP227BY/883	MIL
120	OP227FY	IND
180	OP227GY	IND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

The OP-227 is the first dual amplifier to offer a combination of low offset, low noise, high speed and guaranteed amplifier matching characteristics in one device. The OP-227 with a V_{OS} match of 25μV typical, a TCV_{OS} match of 0.3μV/°C typical, and a 1/f corner of only 2.7Hz is an excellent choice for precision low noise designs. These D.C. characteristics, coupled with a slew rate of 2.8V/μs typical and a small-signal bandwidth of 8MHz typical, allow the designer to achieve AC performance previously unattainable with op-amp-based instrumentation designs.

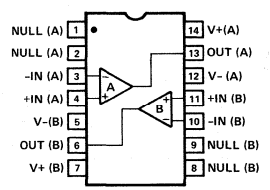
When used in a three-op-amp instrumentation amplifier configuration, the OP-227 can achieve a CMRR in excess of 100dB at 10kHz. In addition, this device has an open-loop gain of 1.5M typical with a 1kΩ load. The OP-227 also features an I_B of ±10nA typical, an I_{OS} of 7nA typical, and guaranteed matching of input currents between amplifiers. These outstanding input current specifications are realized through the use of a unique input current-cancellation-circuit which typically holds I_B and I_{OS} to ±20nA and 15nA respectively over the full military temperature range.

Other sources of input-referred errors, such as PSRR and CMRR, are reduced by factors in excess of 120dB for the individual amplifiers. D.C. stability is assured by a long-term drift specification of 1.0μV/month.

Matching between channels is provided on all critical parameters including offset voltage, tracking of offset voltage vs. temperature, noninverting bias current, CMRR, and power supply rejection ratio. This unique dual amplifier allows the elimination of external components for offset nulling and frequency compensation.

The OP-227 is pin compatible with the OP-10 and OP-207.

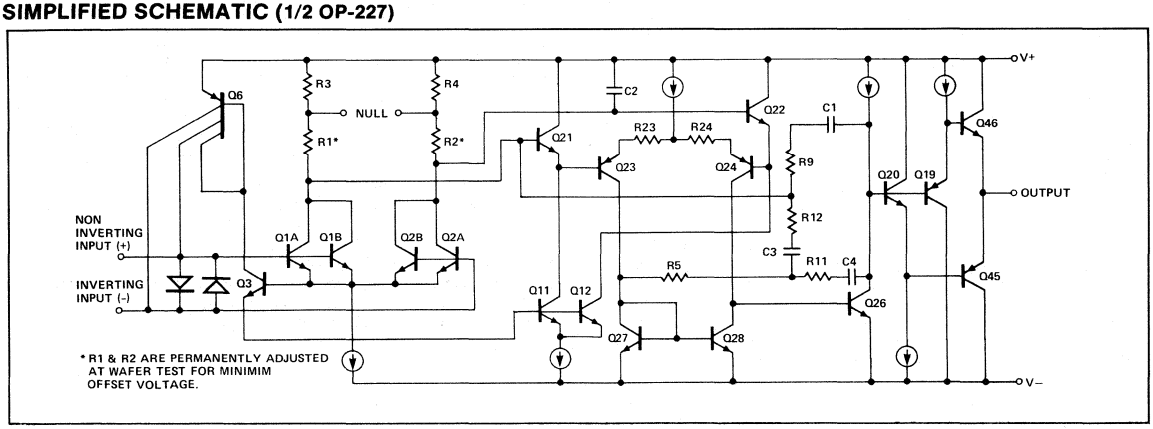
PIN CONNECTIONS



14-PIN CERAMIC DIP (Y-Suffix)

NOTES:
1. Device may be operated even if insertion is reversed; this is due to inherent symmetry of pin locations of amplifiers A and B.
2. V-(A) and V-(B) are internally connected via substrate resistance.

SIMPLIFIED SCHEMATIC (1/2 OP-227)



OP-227

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Input Voltage (Note 1) ..... ±22V
Output Short-Circuit Duration ..... Indefinite
Differential Input Voltage (Note 2) ..... ±0.7V
Differential Input Current (Note 2) ..... ±25mA
Storage Temperature Range ..... –65°C to +150°C
Operating Temperature Range
OP-227A, OP-227B ..... –55°C to +125°C
OP-227E, OP-227F, OP-227G ..... –25°C to +85°C
Lead Temperature (Soldering 60 sec) ..... 300°C

PACKAGE TYPE	Θ_{JA} (Note 3)	Θ_{JC}	UNITS
14-Pin Hermetic DIP (Y)	108	16	°C/W

NOTES:
1. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
2. The OP-227's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP package.

INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-227A/E			OP-227F			OP-227G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	20	80	—	40	120	—	60	180	μV
Long-Term V_{OS} Stability	V_{OS}/Time	(Notes 2, 4)	—	0.2	1.0	—	0.3	1.5	—	0.4	2.0	μV/Mo
Input Offset Current	I_{OS}		—	7	35	—	9	50	—	12	75	nA
Input Bias Current	I_B		—	±10	±40	—	±12	±55	—	±15	±80	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Notes 3, 5)	—	0.08	0.20	—	0.08	0.20	—	0.09	0.28	μV_{p-p}
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 3)	—	3.5	6.0	—	3.5	6.0	—	3.8	9.0	$nV/\sqrt{Hz}$
		f_O = 30Hz (Note 3)	—	3.1	4.7	—	3.1	4.7	—	3.3	5.9	
		f_O = 1000Hz (Note 3)	—	3.0	3.9	—	3.0	3.9	—	3.2	4.6	
Input Noise Current Density	i_n	f_O = 10Hz (Notes 3, 6)	—	1.7	4.5	—	1.7	4.5	—	1.7	—	$pA/\sqrt{Hz}$
		f_O = 30Hz (Notes 3, 6)	—	1.0	2.5	—	1.0	2.5	—	1.0	—	
		f_O = 1000Hz (Notes 3, 6)	—	0.4	0.7	—	0.4	0.7	—	0.4	0.7	
Input Resistance — Differential-Mode	R_{IN}	(Note 7)	1.3	6	—	0.94	5	—	0.7	4	—	MΩ
Input Resistance — Common-Mode	R_{INCM}		—	3	—	—	2.5	—	—	2	—	GΩ
Input Voltage Range	IVR		±11.0	±12.3	—	±11.0	±12.3	—	±11.0	±12.3	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 11V$	114	126	—	106	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4V$ to $\pm 18V$	—	1	10	—	1	10	—	2	20	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	1000	1800	—	1000	1800	—	700	1500	—	V/mV
		$R_L \geq 600\Omega$, $V_O = \pm 10V$	800	1500	—	800	1500	—	600	1500	—	
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.0	±13.8	—	±12.0	±13.8	—	±11.5	±13.5	—	V
		$R_L \geq 600\Omega$	±10.0	±11.5	—	±10.0	±11.5	—	±10.0	±11.5	—	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 4)	1.7	2.8	—	1.7	2.8	—	1.7	2.8	—	V/μs
Gain Bandwidth Prod.	GBW	(Note 4)	5	8	—	5	8	—	5	8	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $i_O = 0$	—	70	—	—	70	—	—	70	—	Ω
Power Consumption	P_d	Each Amplifier	—	90	140	—	90	140	—	100	170	mW
Offset Adjustment Range		$R_P = 10k\Omega$	—	±4	—	—	±4	—	—	±4	—	mV

NOTES:
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E grade specifications are guaranteed fully warmed up.
2. Long-Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5μV — refer to typical performance curve.
3. Sample tested.
4. Parameter is guaranteed by design.
5. See test circuit and frequency response curve for 0.1Hz to 10Hz tester.
6. See test circuit for current noise measurement.
7. Guaranteed by input bias current.

INDIVIDUAL AMPLIFIER CHARACTERISTICS for $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-227A MIN	OP-227A TYP	OP-227A MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	60	180	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSn}	(Notes 2, 3)	—	0.3	1.0	μV/°C
Input Offset Current	I_{OS}		—	15	50	nA
Input Bias Current	I_B		—	±20	±60	nA
Input Voltage Range	IVR		±10.0	±11.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	108	122	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	16	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	600	1200	—	V
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±11.5	±13.5	—	V

INDIVIDUAL AMPLIFIER CHARACTERISTICS for $V_S = \pm 15V$, $-25°C \le T_A \le 85°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-227E MIN	OP-227E TYP	OP-227E MAX	OP-227F MIN	OP-227F TYP	OP-227F MAX	OP-227G MIN	OP-227G TYP	OP-227G MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	40	140	—	60	200	—	85	280	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSn}	(Note 2)	—	0.5	1.0	—	0.4	1.5	—	0.5	1.8	μV/°C
Input Offset Current	I_{OS}		—	10	50	—	14	85	—	20	135	nA
Input Bias Current	I_B		—	±14	±60	—	±18	±95	—	±25	±150	nA
Input Voltage Range	IVR		±10.0	±11.8	—	±10.0	±11.8	—	±10.0	±11.8	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	110	124	—	102	121	—	96	118	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	15	—	2	16	—	2	32	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm 10V$	750	1500	—	700	1300	—	450	1000	—	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±11.7	±13.6	—	±11.4	±13.5	—	±11.0	±13.3	—	V

MATCHING CHARACTERISTICS for $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-227A/E MIN	OP-227A/E TYP	OP-227A/E MAX	OP-227F MIN	OP-227F TYP	OP-227F MAX	OP-227G MIN	OP-227G TYP	OP-227G MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}		—	25	80	—	35	150	—	55	300	μV
Average Noninverting Bias Current	I_B^+	$I_B^+ = \frac{I_B^+{}_A + I_B^+{}_B}{2}$	—	±10	±40	—	±12	±55	—	±15	±90	nA
Noninverting Offset Current	I_{OS}^+	$I_{OS}^+ = I_B^+{}_A - I_B^+{}_B$	—	±12	±60	—	±15	±80	—	±20	±130	nA
Inverting Offset Current	I_{OS}^-	$I_{OS}^- = I_B^-{}_A - I_B^-{}_B$	—	±12	±60	—	±15	±80	—	±20	±130	nA
Common-Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm 11V$	110	123	—	103	120	—	97	117	—	dB
Power Supply Rejection Ratio Match	ΔPSRR	$V_S = \pm 4V$ to $\pm 18V$	—	2	10	—	2	10	—	2	20	μV/V
Channel Separation	CS	(Note 1)	126	154	—	126	154	—	126	154	—	dB

NOTES:

1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. The TCV_{OS} performance is within the specifications unnulled or when nulled with $R_P = 8k\Omega$ to $20k\Omega$, optimum performance is obtained with $R_P = 8k\Omega$.
3. Sample tested.

MATCHING CHARACTERISTICS for $V_S = \pm 15V$, $T_A = -55°C$ to $+125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-227A MIN	OP-227A TYP	OP-227A MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}		—	55	180	μV
Input Offset Voltage Tracking	$TC\Delta V_{OS}$	Nulled or Unnulled (Note 2)	—	0.3	1.0	μV/°C
Average Noninverting Bias Current	I_B+	$I_B+ = \frac{I_B+_A + I_B+_B}{2}$	—	±20	±60	nA
Average Drift of Non-inverting Bias Current	TCI_B+		—	100	—	pA/°C
Noninverting Offset Current	$I_{OS}+$	$I_{OS}+ = I_B+_A - I_B+_B$	—	±25	±90	nA
Average Drift of Non-inverting Offset Current	$TCI_{OS}+$		—	130	—	pA/°C
Inverting Offset Current	$I_{OS}-$	$I_{OS}- = I_B-_A - I_B-_B$	—	±25	±90	nA
Common-Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm 10V$	105	118	—	dB
Power Supply Rejection Ratio Match	ΔPSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	16	μV/V

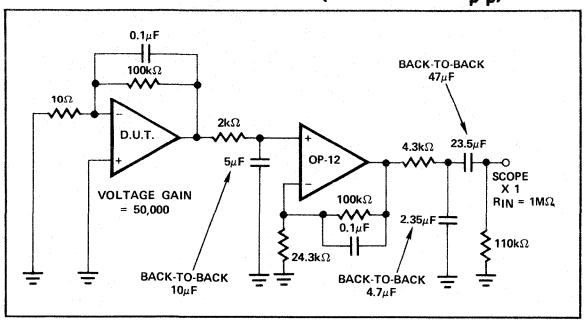
MATCHING CHARACTERISTICS for $V_S = \pm 15V$, $T_A = -25°C$ to $+85°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-227E MIN	OP-227E TYP	OP-227E MAX	OP-227F MIN	OP-227F TYP	OP-227F MAX	OP-227G MIN	OP-227G TYP	OP-227G MAX	UNITS
Input Offset Voltage Match	ΔV_{OS}		—	40	140	—	65	210	—	90	400	μV
Input Offset Voltage Tracking	$TC\Delta V_{OS}$	Nulled or Unnulled (Note 1)	—	0.3	1.0	—	0.4	1.5	—	0.5	1.8	μV/°C
Average Noninverting Bias Current	I_B+	$I_B+ = \frac{I_B+_A + I_B+_B}{2}$	—	±14	±60	—	±18	±95	—	±25	±170	nA
Average Drift of Non-inverting Bias Current	TCI_B+		—	80	—	—	140	—	—	180	—	pA/°C
Noninverting Offset Current	$I_{OS}+$	$I_{OS}+ = I_B+_A - I_B+_B$	—	±20	±90	—	±25	±140	—	±35	±250	nA
Average Drift of Non-inverting Offset Current	$TCI_{OS}+$		—	130	—	—	200	—	—	250	—	pA/°C
Inverting Offset Current	$I_{OS}-$	$I_{OS}- = I_B-_A - I_B-_B$	—	±20	±90	—	±25	±140	—	±35	±250	nA
Common-Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm 10V$	106	120	—	98	117	—	90	112	—	dB
Power Supply Rejection Ratio Match	ΔPSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	15	—	2	16	—	3	32	μV/V

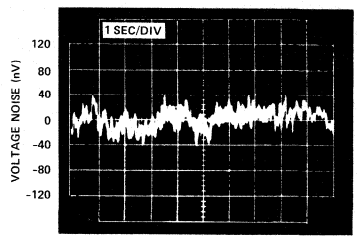
NOTES:
1. Sample tested.
2. Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

VOLTAGE NOISE TEST CIRCUIT (0.1Hz-TO-10Hz$_{p-p}$)



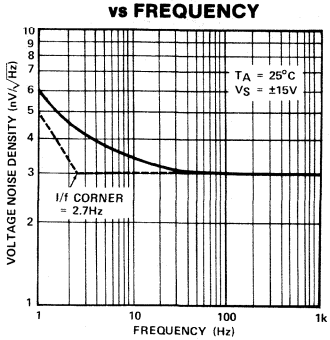
LOW-FREQUENCY NOISE



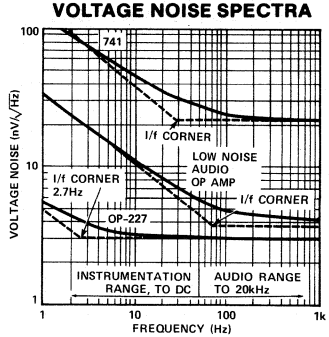
0.1Hz TO 10Hz PEAK-TO-PEAK NOISE

NOTE: OBSERVATION TIME MUST BE LIMITED TO 10 SECONDS TO ENSURE 0.1Hz CUTOFF.

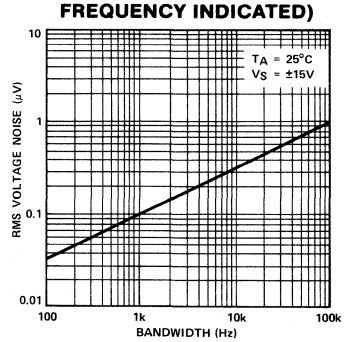
VOLTAGE NOISE DENSITY vs FREQUENCY



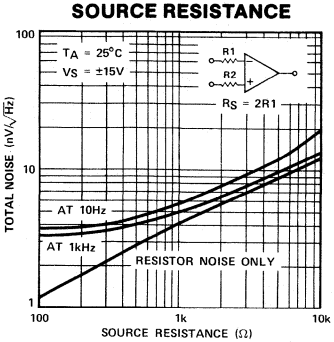
COMPARISON OF OP-AMP VOLTAGE NOISE SPECTRA



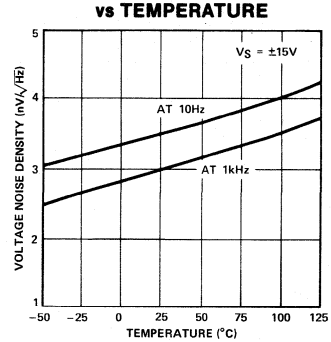
INPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



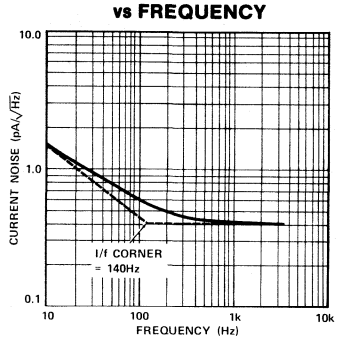
TOTAL NOISE vs SOURCE RESISTANCE



VOLTAGE NOISE DENSITY vs TEMPERATURE



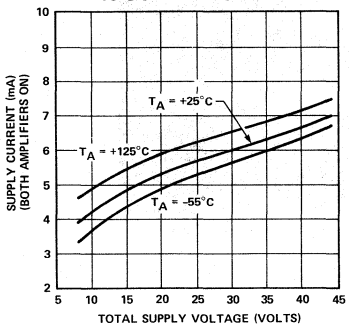
CURRENT NOISE DENSITY vs FREQUENCY



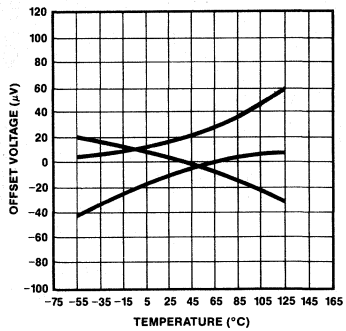
OP-227

TYPICAL PERFORMANCE CHARACTERISTICS

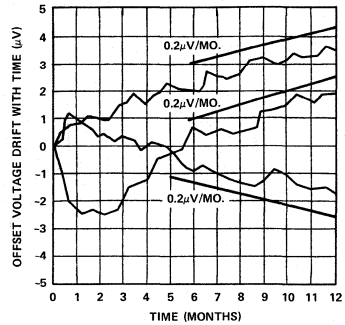
SUPPLY CURRENT vs SUPPLY VOLTAGE



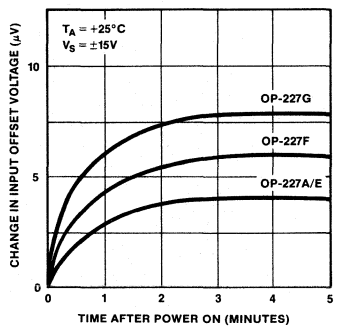
OFFSET VOLTAGE DRIFT OF REPRESENTATIVE UNITS



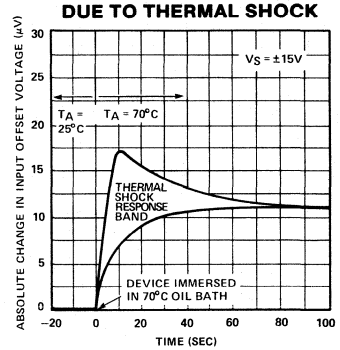
OFFSET VOLTAGE STABILITY WITH TIME



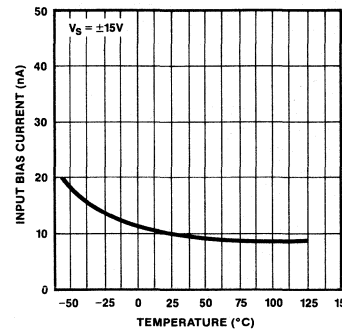
WARM-UP DRIFT



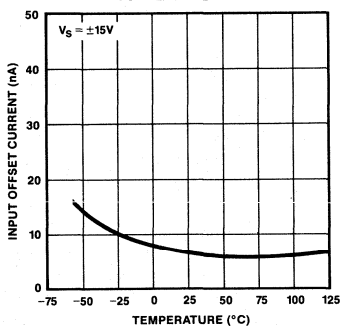
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



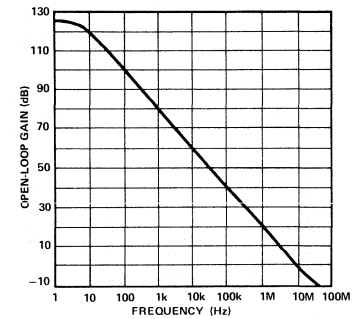
INPUT BIAS CURRENT vs TEMPERATURE



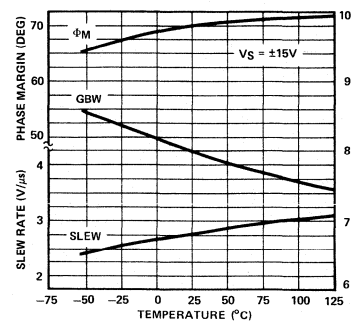
INPUT OFFSET CURRENT vs TEMPERATURE



OPEN-LOOP GAIN vs FREQUENCY

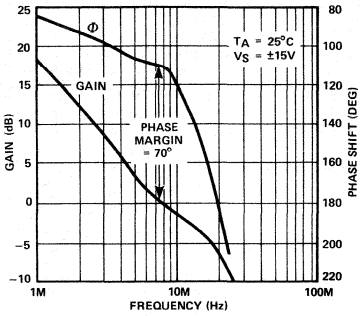


SLEW RATE, GAIN-BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE

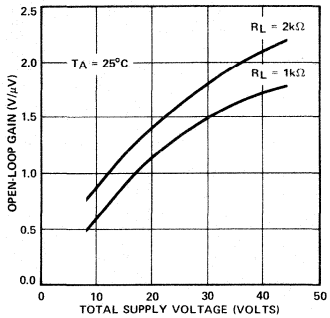


TYPICAL PERFORMANCE CHARACTERISTICS

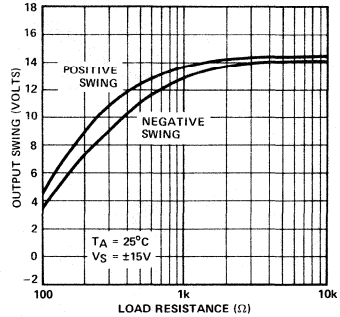
GAIN, PHASE SHIFT vs FREQUENCY



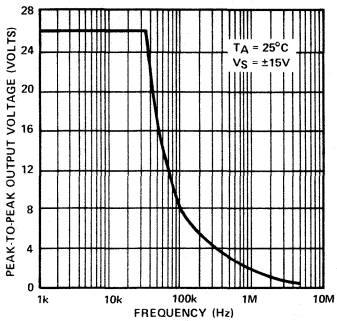
OPEN-LOOP GAIN vs SUPPLY VOLTAGE



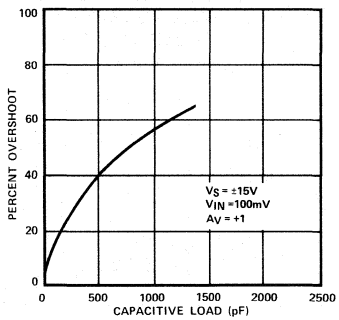
OUTPUT SWING vs RESISTIVE LOAD



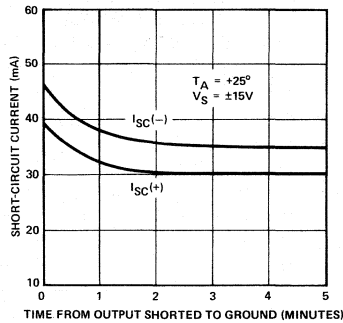
MAXIMUM UNDISTORTED OUTPUT vs FREQUENCY



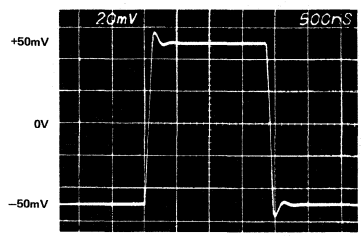
SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD



SHORT-CIRCUIT CURRENT vs TIME

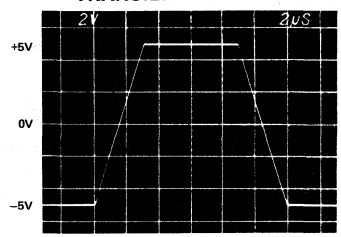


SMALL-SIGNAL TRANSIENT RESPONSE



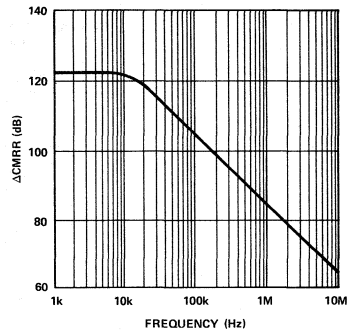
A_{VCL} = +1, C_L = 15pF
V_S = ±15V
T_A = 25°C

LARGE-SIGNAL TRANSIENT RESPONSE



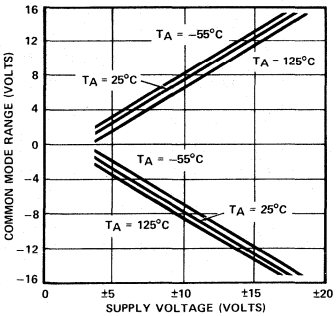
A_{VCL} = +1
V_S = ±15V
T_A = 25°C

MATCHING CHARACTERISTIC CMRR MATCH vs FREQUENCY

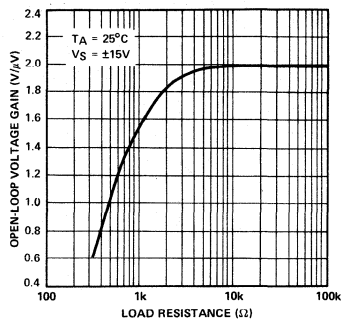


TYPICAL PERFORMANCE CHARACTERISTICS

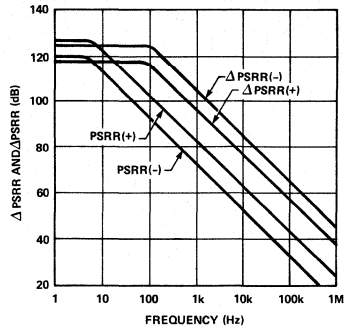
COMMON-MODE INPUT RANGE vs SUPPLY VOLTAGE



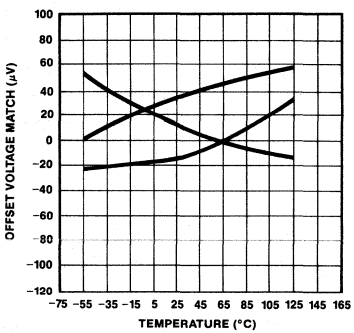
OPEN-LOOP VOLTAGE GAIN vs LOAD RESISTANCE



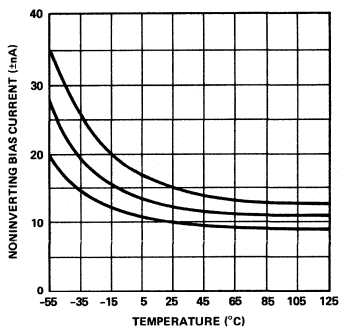
PSRR AND ΔPSRR vs FREQUENCY



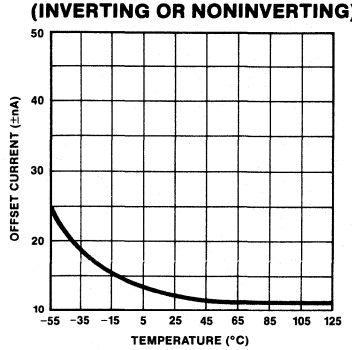
MATCHING CHARACTERISTIC; DRIFT OF OFFSET VOLTAGE MATCH OF REPRESENTATIVE UNITS



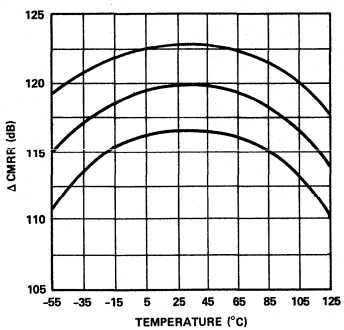
MATCHING CHARACTERISTIC; AVERAGE NONINVERTING BIAS CURRENT vs TEMPERATURE



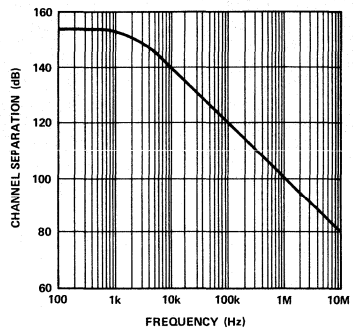
MATCHING CHARACTERISTIC; AVERAGE OFFSET CURRENT vs TEMPERATURE (INVERTING OR NONINVERTING)



MATCHING CHARACTERISTIC; CMRR MATCH vs TEMPERATURE

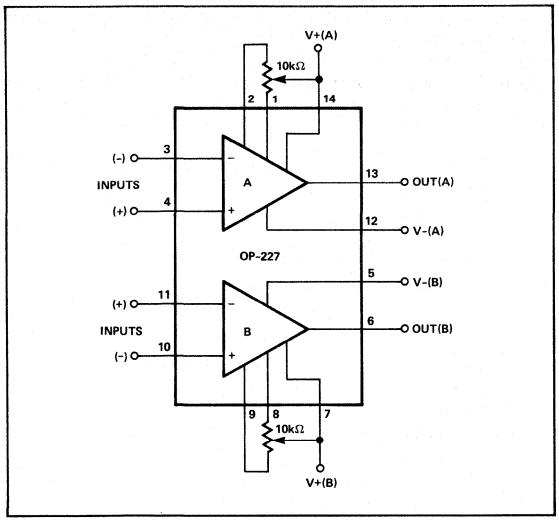


CHANNEL SEPARATION vs FREQUENCY



BASIC CONNECTIONS

OFFSET NULLING CIRCUIT



APPLICATIONS INFORMATION

NOISE MEASUREMENTS

To measure the 80nV peak-to-peak noise specification of the OP-227 in the 0.1Hz to 10Hz range, the following precautions must be observed:

(1) The device has to be warmed-up for at least five minutes. As shown in the warm-up drift curve, the offset voltage typically changes 4μV due to increasing chip temperature after power-up. In the 10-second measurement interval these temperature-induced effects can exceed tens-of-nanovolts.

(2) For similar reasons, the device has to be well-shielded from air currents. Shielding minimizes thermocouple effects.

(3) Sudden motion in the vicinity of the device can also "feedthrough" to increase the observed noise.

(4) The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds. As shown in the noise-tester frequency-response curve, the 0.1Hz corner is defined by only one zero. The test time of 10 seconds acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

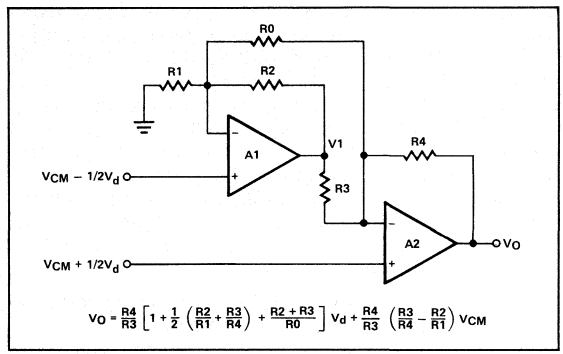
(5) A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage-density measurement will correlate well with a 0.1Hz-to-10Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the 1/f corner frequency.

INSTRUMENTATION AMPLIFIER APPLICATIONS OF THE OP-227

The excellent input characteristics of the OP-227 make it ideal for use in *instrumentation amplifier* configurations where low-level differential signals are to be amplified. The low-noise, low input offsets, low drift, and high gain combined with excellent CMR provides the characteristics needed for high-performance instrumentation amplifiers. In addition, CMR vs. frequency is very good due to the wide gain-bandwidth of these op amps.

The circuit of Figure 1 is recommended for applications where the common-mode input range is relatively low and differential gain will be in the range of 10 to 1000. This two-op-amp instrumentation amplifier features *independent* adjustment of common-mode rejection and differential gain. Input impedance is very high since both inputs are applied to non-inverting op amp inputs.

FIGURE 1: Two-Op-Amp Instrumentation Amplifier Configuration



The output voltage V_O, assuming ideal op amps, is given in Fig. 1. The input voltages are represented as a common-mode input V_{CM} plus a differential input V_d. The ratio R_3/R_4 is made equal to the ratio R_2/R_1 to reject the common-mode input V_{CM}. The differential signal V_d is then amplified according to:

$$V_O = \frac{R_4}{R_3}\left(1 + \frac{R_3}{R_4} + \frac{R_2 + R_3}{R_O}\right) V_d, \text{ where } \frac{R_3}{R_4} = \frac{R_2}{R_1}$$

Note that gain can be independently varied by adjusting R_O. From considerations of dynamic range, resistor tempco matching, and matching of amplifier response, it is generally best to make R_1, R_2, R_3, and R_4 approximately equal. Designating R_1, R_2, R_3, and R_4 as R_N allows the output equation to be further simplified:

$$V_O = 2\left(1 + \frac{R_N}{R_O}\right) V_d, \text{ where } R_N = R_1 = R_2 = R_3 = R_4$$

Dynamic range is limited by A1 as well as A2; the output of A1 is:

$$V_1 = -\left(1 + \frac{R_N}{R_O}\right) V_d + 2\,V_{CM}$$

If the instrumentation amplifier were designed for a gain of 10 and maximum V_d of ±1V, then R_N/R_O would need to be four and V_O would be a maximum of ±10V. Amplifier A1 would have a maximum output of ±5V plus $2V_{CM}$, thus a limit of ±10V on the output of A1 would imply a limit of ±2.5V on V_{CM}. A nominal value of 10kΩ for R_N is suitable for most applications. A range of 20Ω to 2.5kΩ for R_O will then provide a gain range of 10 to 1000. The current through R_O is V_d/R_O, so the amplifiers must supply ±10mV/20Ω (or ±0.5mA) when the gain is at the maximum value of 1000 and V_d is at ±10mV.

Rejecting common-mode inputs is important in accurately amplifying low-level differential signals. Two factors determine the CMR in this instrumentation amplifier configuration (assuming infinite gain):

(1) CMR of the op amps
(2) Matching of the resistor network ratios ($R_3/R_4 = R_2/R_1$)

In this instrumentation amplifier configuration, error due to CMR effect is directly proportional to the CMR match of the op amps. For the OP-227 this ΔCMR is a minimum of 97dB for the "G" and 110dB for the "E" grade. A ΔCMR value of 100dB and common-mode input range of ±2.5V indicates a peak input-referred error of only ±25μV. Resistor matching is the other factor affecting CMR. Defining A_d as the differential gain of the instrumentation amplifier and assuming that R_1, R_2, R_3 and R_4 are approximately equal (R_N will be the nominal value), then CMR for this instrumentation amplifier configuration will be approximately A_d divided by $4\Delta R/R_N$. CMR at differential gain of 100 would be 88dB with resistor matching of 0.1%. Trimming R_1 to make the ratio R_3/R_4 equal to R_2/R_1 will raise the CMR until limited by linearity and resistor stability considerations.

The high open-loop gain of the OP-227 is very important to achieving high accuracy in the two op-amp instrumentation amplifier configuration. Gain error can be approximated by

$$\text{Gain Error} \sim \frac{1}{1+\frac{A_d}{A_{O2}}}, \quad \frac{A_d}{2\,A_{O1}\,A_{O2}} \ll 1$$

where A_d is the instrumentation amplifier differential gain and A_{O2} is the open-loop gain of op amp A2. This analysis assumes equal values of R_1, R_2, R_3, and R_4. For example, consider an OP-227 with A_{02} of 700V/mV. If the differential gain A_d were set to 700, then the gain error would be 1/1.001 which is approximately 0.1%.

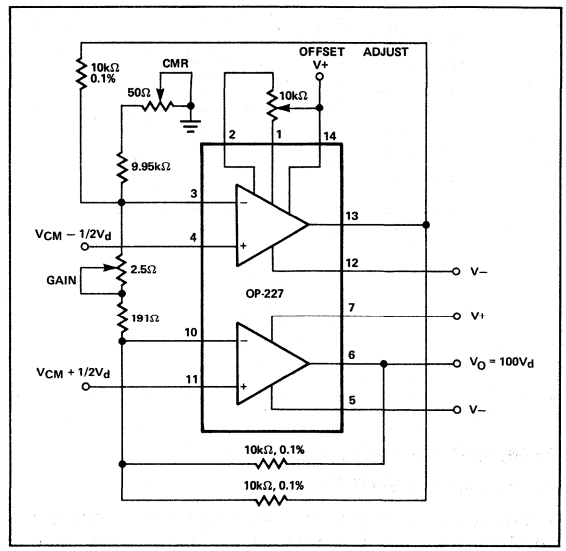
Another effect of finite op amp gain is undesired feedthrough of common-mode input. Defining A_{01} as the open-loop gain of op amp A1, then the common-mode error (CME) at the output due to this effect will be approximately

$$\text{CME} \sim \frac{2\,A_d}{1+\frac{A_d}{A_{O1}}} \quad \frac{1}{A_{O1}} \; V_{CM}$$

For $A_d/A_{O1} \ll 1$, this simplifies to $(2\,A_d/A_{O1}) \times V_{CM}$. If the op amp gain is 700V/mV, V_{CM} is 2.5V, and A_d is set to 700, then the error at the output due to this effect will be approximately 5mV.

A complete instrumentation amplifier designed for a gain of 100 is shown in Figure 2. It has provision for trimming of input offset voltage, CMR, and gain. Performance is excellent due to the high gain, high CMR, and low noise of the individual amplifiers combined with the tight matching characteristics of the OP-227 dual.

FIGURE 2: Two-Op-Amp Instrumentation Amplifier Using OP-227 Dual



A three-op-amp instrumentation amplifier configuration using the OP-227 and OP-27 is recommended for applications requiring high accuracy over a wide gain range. This circuit provides excellent CMR over a wide frequency range. As with the two-op-amp instrumentation amplifier circuits, the tight matching of the two op-amps within the OP-227 package provides a real boost in performance. Also, the low-noise, low offset, and high gain of the individual op-amps minimize errors.

A simplified schematic is shown in Figure 3. The input stage (A1 and A2) serves to amplify the differential input V_d without amplifying the common-mode voltage V_{CM}. The output stage then rejects the common-mode input. With ideal op-amps and no resistor matching errors, then the outputs of each amplifier will be:

$$V_1 = -\left(1+\frac{2R_1}{R_O}\right)\frac{V_d}{2} + V_{CM}$$

$$V_2 = \left(1+\frac{2R_1}{R_O}\right)\frac{V_d}{2} + V_{CM}$$

$$V_O = V_2 - V_1 = \left(1+\frac{2R_1}{R_O}\right)V_d$$

$$V_O = A_d\,V_d$$

The differential gain A_d is $1 + 2R_1/R_O$ and the common-mode input V_{CM} is rejected.

While output error due to input offsets and noise are easily determined, the effects of finite gain and common-mode rejection are more subtle. CMR of the complete instrumentation amplifier is directly proportioned to the *match* in CMR of the input op-amps. This match varies from 97dB to 110dB minimum for the OP-227. Using 100dB, then the output response to a common-mode input V_{CM} would be:

$$[V_O]_{CM} = A_d\, V_{CM} \times 10^{-5}$$

CMRR of the instrumentation amplifier, which is defined as $20 \log_{10} A_d/A_{CM}$, is simply equal to the ΔCMRR of the OP-227. While this ΔCMRR is already high, overall CMRR of the complete amplifier can be raised by trimming the output stage resistor network.

Finite gain of the input op-amps causes a scale factor error and a small degradation in CMR. Designating the open-loop gain of op-amp A_1 as A_{O1}, and op-amp A_2 as A_{O2}, then the following equation approximates the output:

$$V_O \sim \frac{1}{1 + \frac{R_1}{R_O}\left(\frac{1}{A_{O1}} + \frac{1}{A_{O2}}\right)} \left(A_d\, V_d + \frac{2R_1}{R_O}\left(\frac{1}{A_{O1}} - \frac{1}{A_{O2}}\right) V_{CM}\right)$$

This can be simplified by defining A_O as the nominal open-loop gain and ΔA_O as the differential open-loop gain. Then

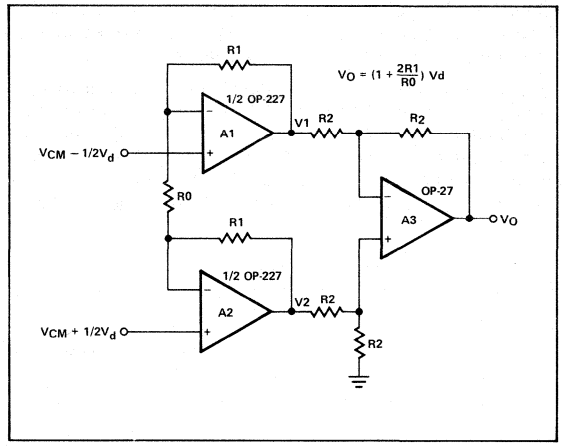
$$V_O \sim \frac{1}{1 + \frac{2R_1}{R_O}\frac{1}{A_O}} \left(A_d\, V_d + \frac{2R_1}{R_O}\frac{\Delta A_O}{A_O^2} V_{CM}\right)$$

The high open-loop gain of each amplifier within the OP-227 (700,000 minimum at 25° C into $R_L \geq 2k$) assures good gain accuracy even at high values of A_d. The effect of finite open-loop gain on CMR can be approximated by:

$$CMRR \sim \frac{A_O^2}{\Delta A_O}$$

If $\Delta A_O/A_O$ were 6% and A_O were 600,000, then the CMRR due to finite gain of the input op-amps would be approximately 140dB.

FIGURE 3: Three-Op-Amp Instrumentation Amplifier Using OP-227 and OP-27



The unity-gain output stage contributes negligible error to the overall amplifier. However, matching of the four-resistor R_2–network is critical to achieving high CMR. Consider a worst-case situation where each R_2 resistor has an error of $\pm\Delta R_2$. If the resistor ratio is high on one side and low on the other, then the common-mode gain will be $2\Delta R_2/R_2$. Since the output stage gain is unity, CMRR will then be $R_2/2\Delta R_2$. It is common practice to trim the R_2 resistor connected to ground to maximize overall CMRR for the total instrumentation amplifier circuit.

This three-op-amp instrumentation amplifier configuration provides excellent performance over a wide gain range. A gain range of 1 to 2000 is practical and CMR of over 120dB is achievable.

HIGH SPEED PRECISION RECTIFIER

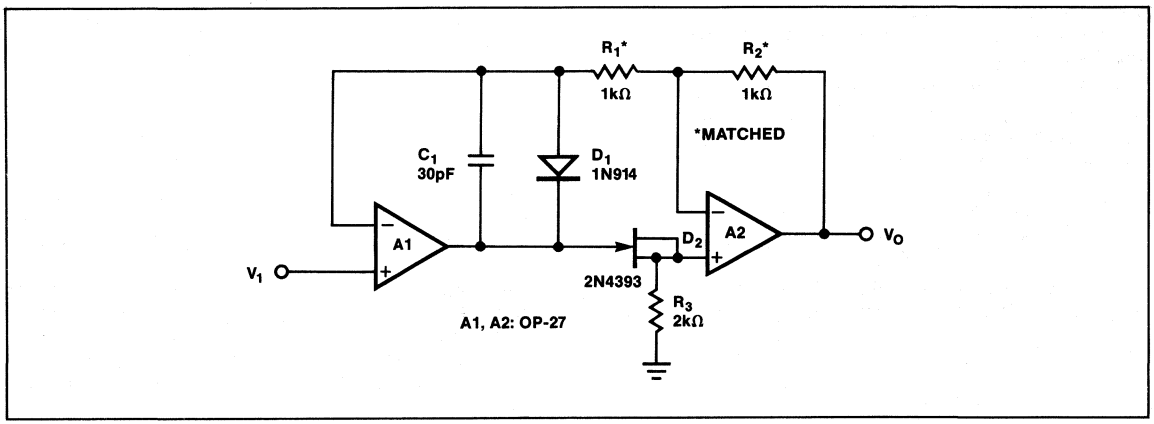
The low offsets and excellent load driving capability of the OP-27 are key advantages in this precision rectifier circuit. The summing impedances can be as low as 1kΩ which helps to reduce the effects of stray capacitance.

For positive inputs, D2 conducts and D1 is biased OFF. Amplifiers A1 and A2 act as a follower with output-to-input feedback and the R1 resistors are no critical. For negative inputs, D1 conducts and D2 is biased OFF. A1 acts as a follower and A2 serves as a precision inverter. In this mode, matching of the two R1 resistors is critical to gain accuracy.

Typical component values are 30pF for C1 and 2kΩ for R3. The drop across D1 must be less than the drop across the FET diode D2. A 1N914 for D1 and a 2N4393 for the JFET were used successfully.

The circuit provides full-wave rectification for inputs of up to ±10V and up to 20kHz in frequency. To assure frequency stability, be sure to decouple the power supply inputs and minimize any capacitive loading. An OP-227, which is two OP-27 amplifiers in a single package, can be used to improve packaging density.

FIGURE 4: High Speed Precision Rectifier



Dual, Precision JFET High-Speed Operational Amplifier

OP-249

FEATURES

- **Fast Slew Rate ..... 22V/μs Typ**
- **Settling Time (0.01%) ..... 1.2μs Max**
- **Offset Voltage ..... 300μV Max**
- **High Open-Loop Gain ..... 1000V/mV Min**
- **Low Total Harmonic Distortion ..... 0.002% Typ**
- **Improved Replacement for AD712, LT1057, OP-215, TL072, and MC34082**
- **Available in Die Form**

APPLICATIONS

- **Output Amplifier for Fast D/As**
- **Signal Processing**
- **Instrumentation Amplifiers**
- **Fast Sample/Holds**
- **Active Filters**
- **Low Distortion Audio Amplifiers**
- **Input Buffer for A/D Converters**
- **Servo Controllers**

GENERAL DESCRIPTION

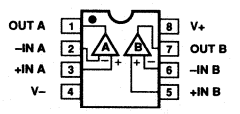
The OP-249 is a high-speed, precision dual JFET op amp, similar to the popular single op amp, the OP-42. The OP-249 outperforms available dual amplifiers by providing superior speed with excellent DC performance. Ultra-high open-loop gain (1kV/mV minimum), low offset voltage, and superb gain linearity, makes the OP-249 the industry's first true precision, dual high-speed amplifier.

With a slew rate of 22V/μs typical, and a fast settling time of less than 1.2μs maximum to 0.01%, the OP-249 is an ideal choice for high-speed bipolar D/A and A/D converter applications. The excellent DC performance of the OP-249 allows the full accuracy of high-resolution CMOS D/As to be realized.

Symmetrical slew rate, even when driving large loads, such as 600Ω, or 200pF of capacitance, and ultra-low distortion, make the OP-249 ideal for professional audio applications, active filters, high-speed integrators, servo systems, and buffer amplifiers.

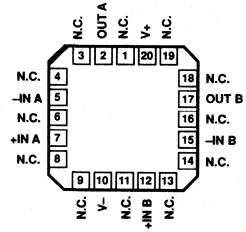
The OP-249 provides significant performance upgrades to the TL072, AD712, OP-215, MC34082 and the LT1057.

PIN CONNECTIONS

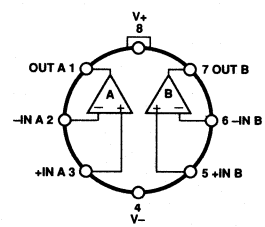


8-PIN CERDIP
(Z-Suffix)

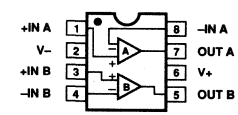
8-PIN EPOXY MINI-DIP
(P-Suffix)



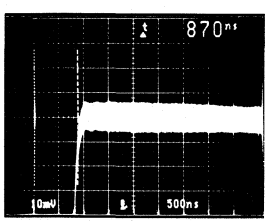
20-CONTACT LCC
(RC-Suffix)



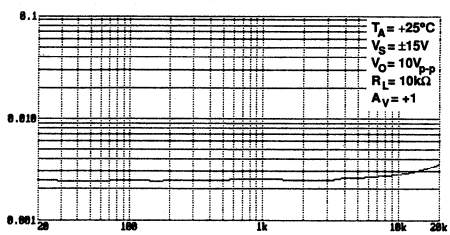
TO-99
(J-Suffix)



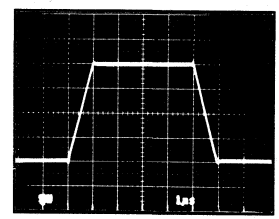
8-PIN SO
(S-Suffix)



FAST SETTLING
(0.01%)



LOW DISTORTION
A_V = +1, R_L = 10kΩ



EXCELLENT OUTPUT DRIVE
R_L = 600Ω

ORDERING INFORMATION †

PACKAGE				OPERATING TEMPERATURE RANGE
TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	LCC 20-CONTACT	
OP249AJ*	OP249AZ*	–	OP249ARC/883	MIL
OP249EJ	–	–	–	XIND
OP249FJ	OP249FZ	–	–	XIND
–	–	OP249GP	–	XIND
–	–	OP249GS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Input Voltage (Note 2) ..... ±18V
Differential Input Voltage (Note 2) 36V
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range ..... –65°C to +175°C

Operating Temperature Range
OP-249A (J, Z, RC) ..... –55°C to +125°C
OP-249E,F (J, Z) ..... –40°C to +85°C
OP-249G (P, S) ..... –40°C to +85°C
Junction Temperature
OP-249 (J, Z, RC) ..... –65°C to +175°C
OP-249 (P, S) ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C

PACKAGE TYPE	θ_{JA} (Note 3)	θ_{JC}	UNITS
TO-99 (J)	145	16	°C/W
8-Pin Hermetic DIP (Z)	134	12	°C/W
8-Pin Plastic DIP (P)	96	37	°C/W
20-Contact LCC (RC)	88	33	°C/W
8-Pin SO (S)	150	41	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.
3. θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

			OP-249A			OP-249E			OP-249F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Offset Voltage	V_{OS}		–	0.2	0.5	–	0.1	0.3	–	0.2	0.7	mV
Long Term Offset Voltage	V_{OS}	(Note 1)	–	–	0.8	–	–	0.6	–	–	1.0	mV
Offset Stability			–	1.5	–	–	1.5	–	–	1.5	–	µV/Month
Input Bias Current	I_B	V_{CM} = 0V, T_J = +25°C	–	30	75	–	20	50	–	30	75	pA
Input Offset Current	I_{OS}	V_{CM} = 0V, T_J = +25°C	–	6	25	–	4	15	–	6	25	pA
Input Voltage Range	IVR	(Note 2)	±11	+12.5 –12.5	–	±11	+12.5 –12.5	–	±11	+12.5 –12.5	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	80	90	–	86	95	–	80	90	–	dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	–	12	31.6	–	9	31.6	–	12	50	µV/V
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V R_L = 2kΩ	1000	1400	–	1000	1400	–	500	1200	–	V/mV
Output Voltage Swing	V_O	R_L = 2kΩ	±12.0	+12.5 –12.5	–	±12.0	+12.5 –12.5	–	±12.0	+12.5 –12.5	–	V
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	±20	+36 –33	±50	±20	+36 –33	±50	±20	+36 –33	±50	mA
Supply Current	I_{SY}	No Load V_O = 0V	–	5.6	7.0	–	5.6	7.0	–	5.6	7.0	mA
Slew Rate	SR	R_L = 2kΩ, C_L = 50pF	18	22	–	18	22	–	18	22	–	V/µs
Gain-Bandwidth Product	GBW	(Note 4)	3.5	4.7	–	3.5	4.7	–	3.5	4.7	–	MHz
Settling Time	t_s	10V Step 0.01% (Note 3)	–	0.9	1.2	–	0.9	1.2	–	0.9	1.2	µs
Phase Margin	θ_0	0dB Gain	–	55	–	–	55	–	–	55	–	Deg

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	OP-249A MIN	OP-249A TYP	OP-249A MAX	OP-249E MIN	OP-249E TYP	OP-249E MAX	OP-249F MIN	OP-249F TYP	OP-249F MAX	UNITS
Differential Input Impedance	Z_{IN}		–	10^{12}||6	–	–	10^{12}||6	–	–	10^{12}||6	–	Ω||pF
Open-Loop Output Resistance	R_O		–	35	–	–	35	–	–	35	–	Ω
Voltage Noise	$e_{n\ p\text{-}p}$	0.1Hz to 10Hz	–	2	–	–	2	–	–	2	–	$\mu V_{p\text{-}p}$
Voltage Noise Density	e_n	f_O = 10Hz	–	75	–	–	75	–	–	75	–	nV/√Hz
		f_O = 100Hz	–	26	–	–	26	–	–	26	–	
		f_O = 1kHz	–	17	–	–	17	–	–	17	–	
		f_O = 10kHz	–	16	–	–	16	–	–	16	–	
Current Noise Density	i_n	f_O = 1kHz	–	0.003	–	–	0.003	–	–	0.003	–	pA/√Hz
Voltage Supply Range	V_S		±4.5	±15	±18	±4.5	±15	±18	±4.5	±15	±18	V

NOTES:
1 Long term offset voltage is guaranteed by a 1000 HR life test performed on 3 independent wafer lots at +125°C with a LTPD of 3.
2. Guaranteed by CMR test.
3. Settling-time is statistically tested.
4. Guaranteed by design and by inference from the slew rate measurement.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-249G MIN	OP-249G TYP	OP-249G MAX	UNITS
Offset Voltage	V_{OS}		–	0.4	2.0	mV
Input Bias Current	I_B	V_{CM} = 0V, T_J = +25°C	–	40	75	pA
Input Offset Current	I_{OS}	V_{CM} = 0V, T_J = +25°C	–	10	25	pA
Input Voltage Range	IVR	(Note 1)	±11	+12.5 –12.0	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	76	90	–	dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	–	12	50	μV/V
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V R_L = 2kΩ	500	1100	–	V/mV
Output Voltage Swing	V_O	R_L = 2kΩ	±12.0	+12.5 –12.5	–	V
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	±20	+36 –33	±50	mA
Supply Current	I_{SY}	No Load V_O = 0V	–	5.6	7.0	mA
Slew Rate	SR	R_L = 2kΩ, C_L = 50pF	18	22	–	V/μs
Gain-Bandwidth Product	GBW		–	4.7	–	MHz
Settling Time	t_s	10V Step 0.01%	–	0.9	–	μs
Phase Margin	Θ_0	0dB Gain	–	55	–	Deg

NOTES:
1. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	OP-249G MIN	OP-249G TYP	OP-249G MAX	UNITS
Differential Input Impedance	Z_{IN}		–	10^{12}||6	–	Ω||pF
Open-Loop Output Resistance	R_O		–	35	–	Ω
Voltage Noise	$e_{n\ p\text{-}p}$	0.1Hz to 10Hz	–	2	–	$\mu V_{p\text{-}p}$
Voltage Noise Density	e_n	f_O = 10Hz	–	75	–	nV/√Hz
		f_O = 100Hz	–	26	–	
		f_O = 1kHz	–	17	–	
		f_O = 10kHz	–	16	–	
Current Noise Density	i_n	f_O = 1kHz	–	0.003	–	pA/√Hz
Voltage Supply Range	V_S		±4.5	±15	±18	V

ELECTRICAL CHARACTERISTICS at V_S = ±15V, –40°C ≤ T_A ≤ +85°C for E/F grades, and –55°C ≤ T_A ≤ +125°C for A grade, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-249A MIN	OP-249A TYP	OP-249A MAX	OP-249E MIN	OP-249E TYP	OP-249E MAX	OP-249F MIN	OP-249F TYP	OP-249F MAX	UNITS
Offset Voltage	V_{OS}		–	0.12	1.0	–	0.1	0.5	–	0.5	1.1	mV
Offset Voltage Temperature Coefficient	TCV_{OS}		–	1	5	–	1	3	–	1.2	6	µV/°C
Input Bias Current	I_B	(Note 1)	–	4	20	–	0.25	3.0	–	0.3	4.0	nA
Input Offset Current	I_{OS}	(Note 1)	–	0.04	4	–	0.01	0.7	–	0.02	1.2	nA
Input Voltage Range	IVR	(Note 2)	±11	+12.5 –12.5	–	±11	+12.5 –12.5	–	±11	+12.5 –12.5	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	76	110	–	86	100	–	76	95	–	dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	–	5	50	–	5	50	–	7	100	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L = 2kΩ V_O = ±10V	500	1400	–	750	1400	–	250	1200	–	V/mV
Output Voltage Swing	V_O	R_L = 2kΩ	±12.0	+12.5 –12.5	–	±12.0	+12.5 –12.5	–	±12.0	+12.5 –12.5	–	V
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	±10	–	±60	±18	–	±60	±18	–	±60	mA
Supply Current	I_{SY}	No Load V_O = 0V	–	5.6	7.0	–	5.6	7.0	–	5.6	7.0	mA

NOTES:

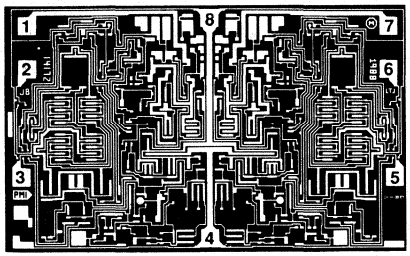
1. T_J = 85°C for E/F Grades; T_J = 125°C for A Grade.
2. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, –40°C ≤ T_A ≤ +85°C, unless otherwise noted.

			OP-249G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Offset Voltage	V_{OS}		–	1.0	3.6	mV
Offset Voltage Temperature Coefficient	TCV_{OS}		–	6	25	µV/°C
Input Bias Current	I_B	(Note 1)	–	0.5	4.5	nA
Input Offset Current	I_{OS}	(Note 1)	–	0.04	1.5	nA
Input Voltage Range	IVR	(Note 2)	±11.0	+12.5 –12.5	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	76	95	–	dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	–	10.0	100	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L = 2kΩ V_O = ±10V	250	1200	–	V/mV
Output Voltage Swing	V_O	R_L = 2kΩ	±12.0	+12.5 –12.5	–	V
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	±18	–	±60	mA
Supply Current	I_{SY}	No Load V_O = 0V	–	5.6	7.0	mA

NOTES:
1. T_j = 85°C.
2. Guaranteed by CMR test.

DICE CHARACTERISTICS



DIE SIZE 0.072 x 0.112 inch, 8,064 sq. mils
(1.83 x 2.84 mm, 5.2 sq. mm)

1. OUT (A)
2. –IN (A)
3. +IN (A)
4. V–
5. +IN (B)
6. –IN (B)
7. OUT (B)
8. V+

WAFER TEST LIMITS at V_S = ±15V, T_j = +25°C, unless otherwise noted.

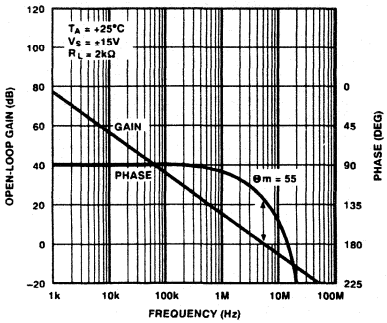
PARAMETER	SYMBOL	CONDITIONS	OP-249GBC LIMITS	UNITS
Offset Voltage	V_{OS}		0.5	mV MAX
Offset Voltage Temperature Coefficient	TCV_{OS}	–40°C ≤ T_j ≤ 85°C	6.0	µV/°C MAX
Input Bias Current	I_B	V_{CM} = 0V	225	pA MAX
Input Offset Current	I_{OS}	V_{CM} = 0V	75	pA MAX
Input Voltage Range	IVR	(Note 1)	±11	V MIN
Common-Mode Rejection	CMR	V_{CM} = ±11V	76	dB MIN
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	100	µV/V MAX
Large-Signal Voltage Gain	A_{VO}	R_L = 2kΩ	250	V/mV MIN
Output Voltage Swing	V_O	R_L = 2kΩ	±12.0	V MIN
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	±20/±60	mA MIN/MAX
Supply Current	I_{SY}	No Load V_O = 0V	7.0	mA MAX
Slew Rate	SR	R_L = 2kΩ, C_L = 50pF	16.5	V/µs MIN

NOTES:
1. Guaranteed by CMR test.

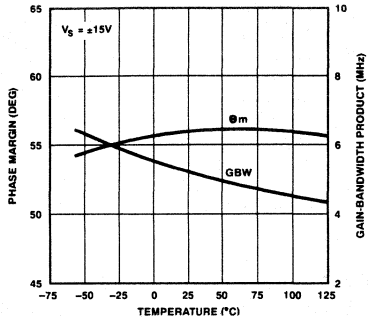
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

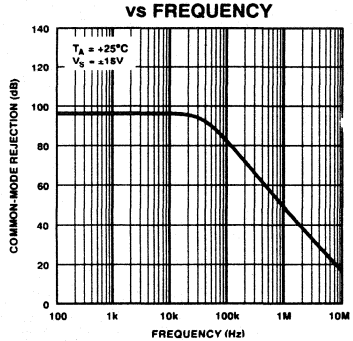
OPEN-LOOP GAIN, PHASE vs FREQUENCY



GAIN-BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE

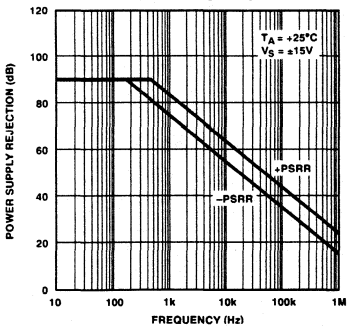


COMMON-MODE REJECTION vs FREQUENCY

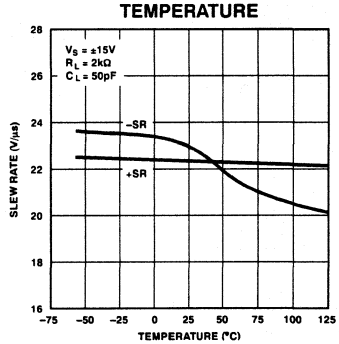


2

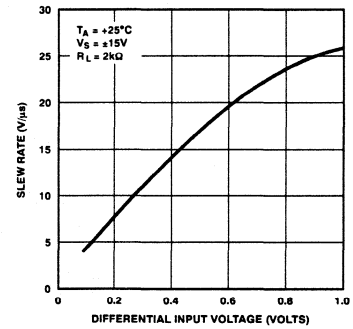
POWER SUPPLY REJECTION vs FREQUENCY



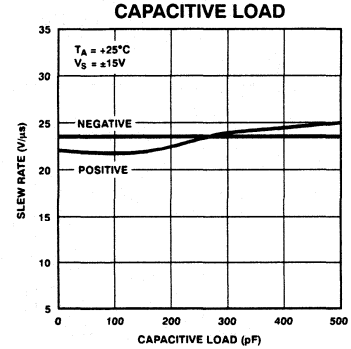
SLEW RATE vs TEMPERATURE



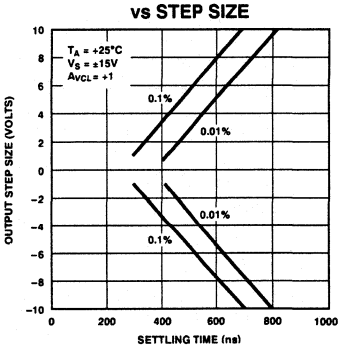
SLEW RATE vs DIFFERENTIAL INPUT VOLTAGE



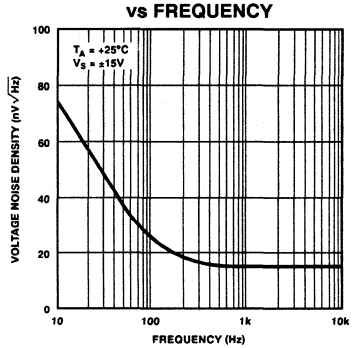
SLEW RATE vs CAPACITIVE LOAD



SETTLING TIME vs STEP SIZE

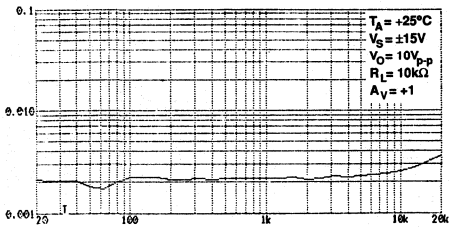


VOLTAGE NOISE DENSITY vs FREQUENCY

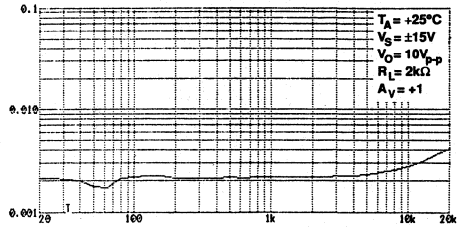


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

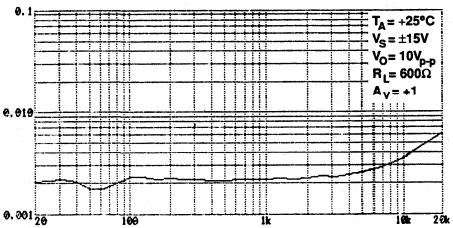
DISTORTION vs FREQUENCY



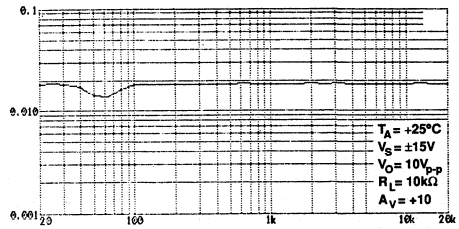
DISTORTION vs FREQUENCY



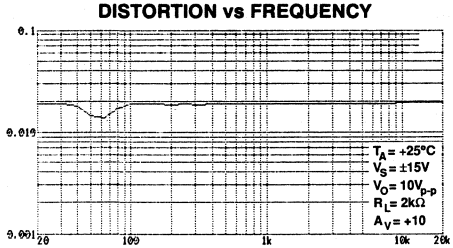
DISTORTION vs FREQUENCY



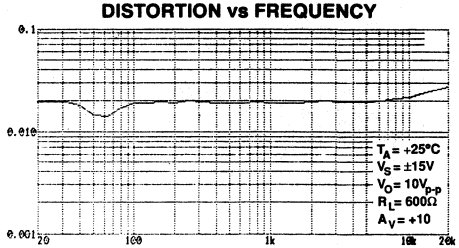
DISTORTION vs FREQUENCY



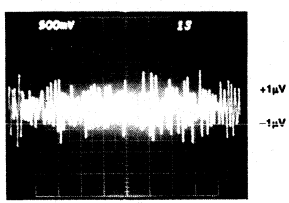
DISTORTION vs FREQUENCY



DISTORTION vs FREQUENCY



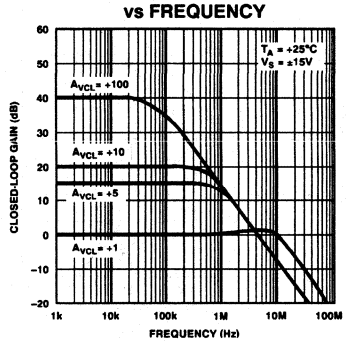
LOW FREQUENCY NOISE



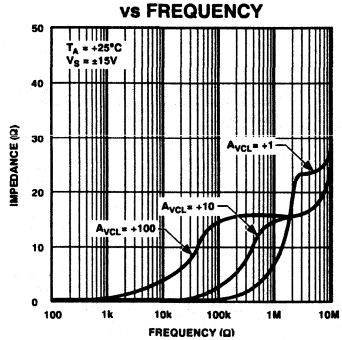
BANDWIDTH (0.1Hz TO 10Hz)

T_A = +25°C V_S = ±15V

CLOSED-LOOP GAIN vs FREQUENCY

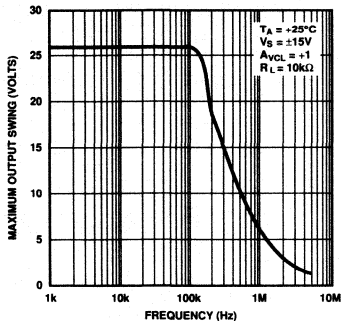


CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

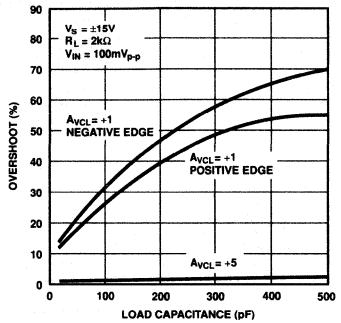


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

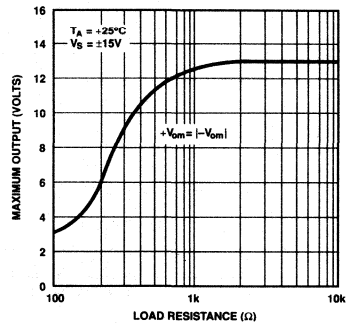
MAXIMUM OUTPUT SWING vs FREQUENCY



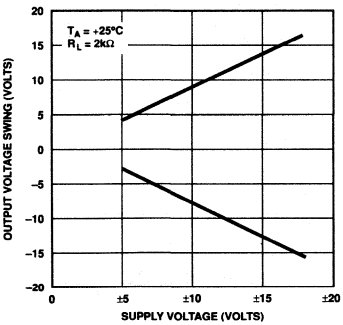
SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE



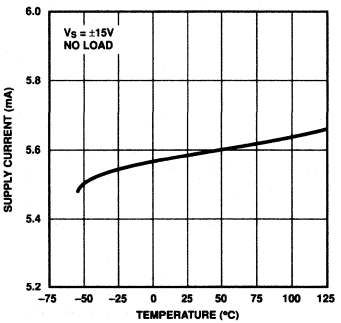
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



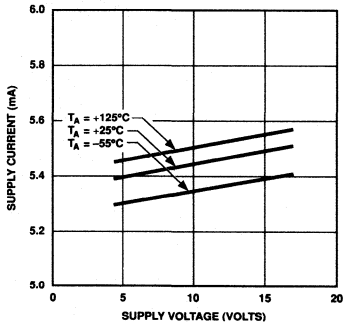
OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE



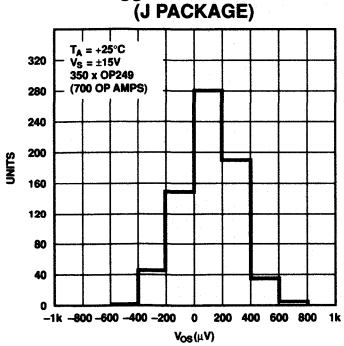
SUPPLY CURRENT vs TEMPERATURE



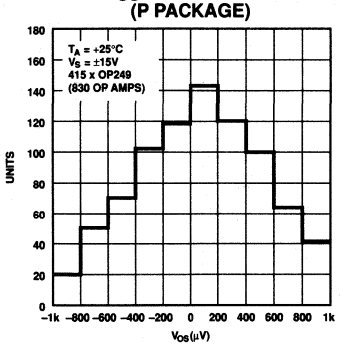
SUPPLY CURRENT vs SUPPLY VOLTAGE



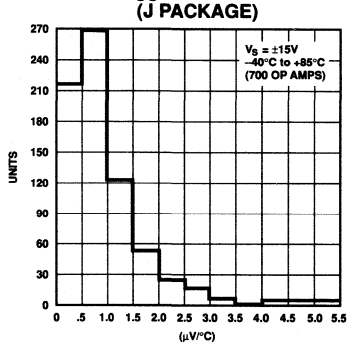
V_{OS} DISTRIBUTION (J PACKAGE)



V_{OS} DISTRIBUTION (P PACKAGE)

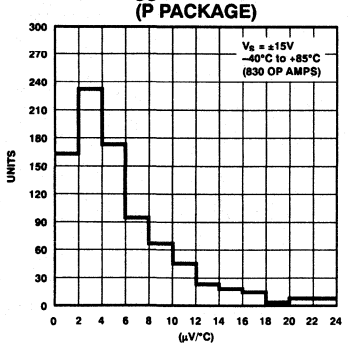


TCV_{OS} DISTRIBUTION (J PACKAGE)

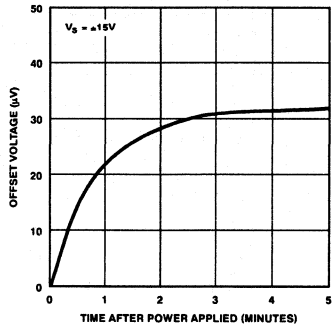


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

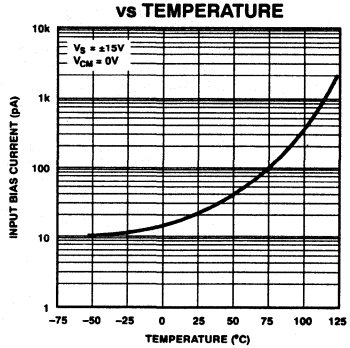
TCV$_{OS}$ DISTRIBUTION (P PACKAGE)



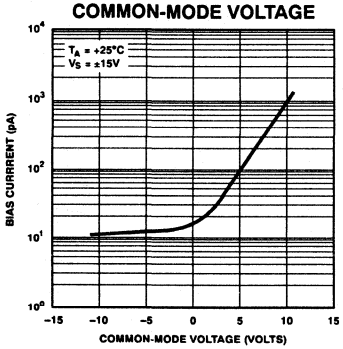
OFFSET VOLTAGE WARM-UP DRIFT



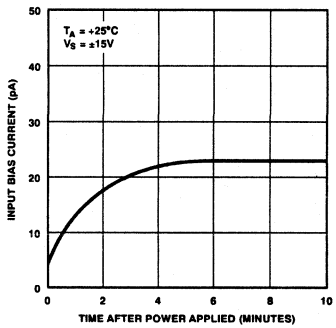
INPUT BIAS CURRENT vs TEMPERATURE



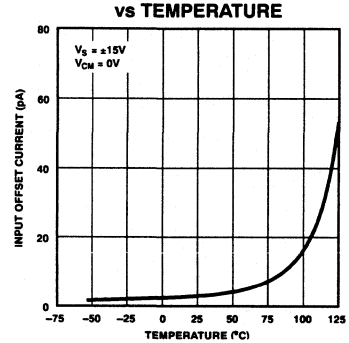
BIAS CURRENT vs COMMON-MODE VOLTAGE



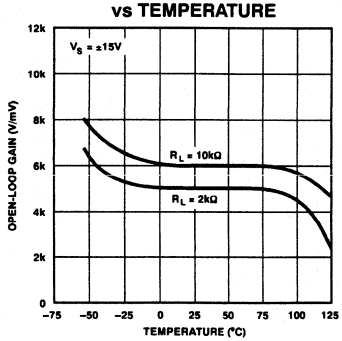
BIAS CURRENT WARM-UP DRIFT



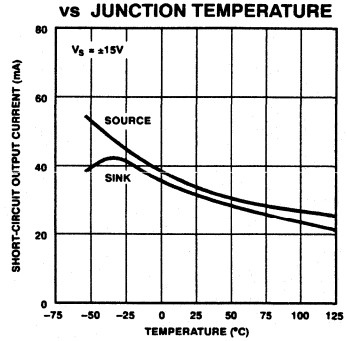
INPUT OFFSET CURRENT vs TEMPERATURE



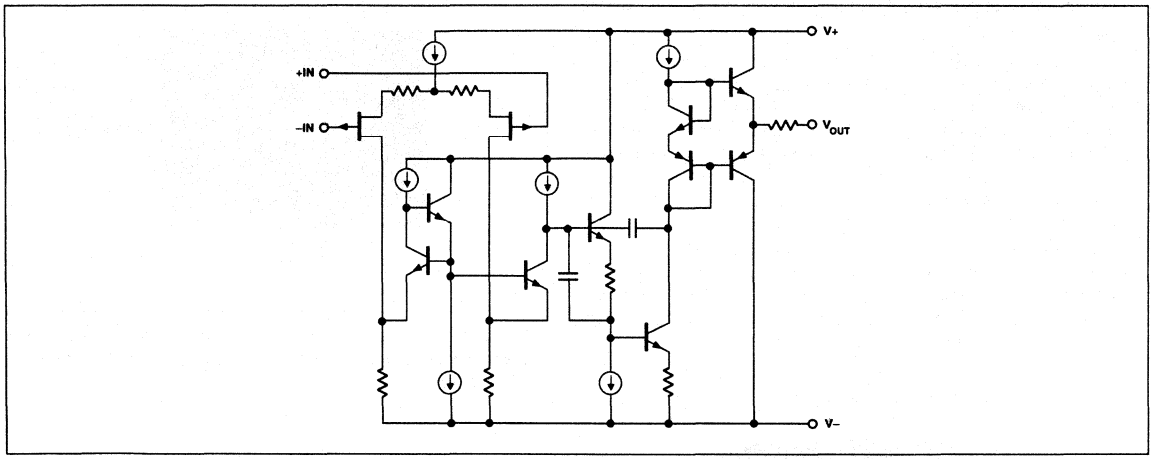
OPEN-LOOP GAIN vs TEMPERATURE



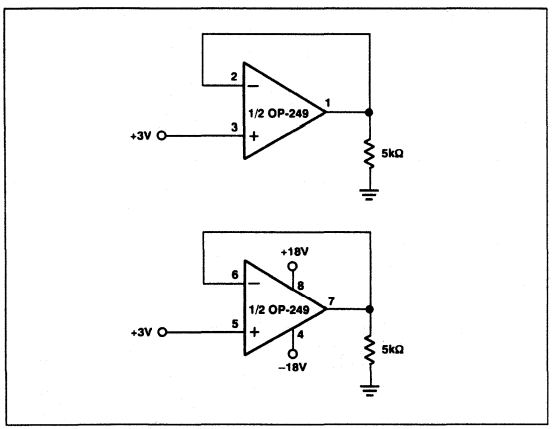
SHORT-CIRCUIT OUTPUT CURRENT vs JUNCTION TEMPERATURE



SIMPLIFIED SCHEMATIC (1/2 OP-249)



BURN-IN CIRCUIT



APPLICATIONS INFORMATION

The OP-249 represents a reliable JFET amplifier design, featuring an excellent combination of DC precision and high speed. A rugged output stage provides the ability to drive a 600Ω load and still maintain a clean AC response. The OP-249 features a large-signal response that is more linear and symmetric than previously available JFET input amplifiers – compare the OP-249's large-signal reponse, as illustrated in Figure 1, to other industry standard dual JFET amplifiers.

Typically, JFET amplifier's slewing performance is simply specified as just a number of volts/μs. There is no discussion on the quality, i.e., linearity, symmetry, etc. of the slewing response.

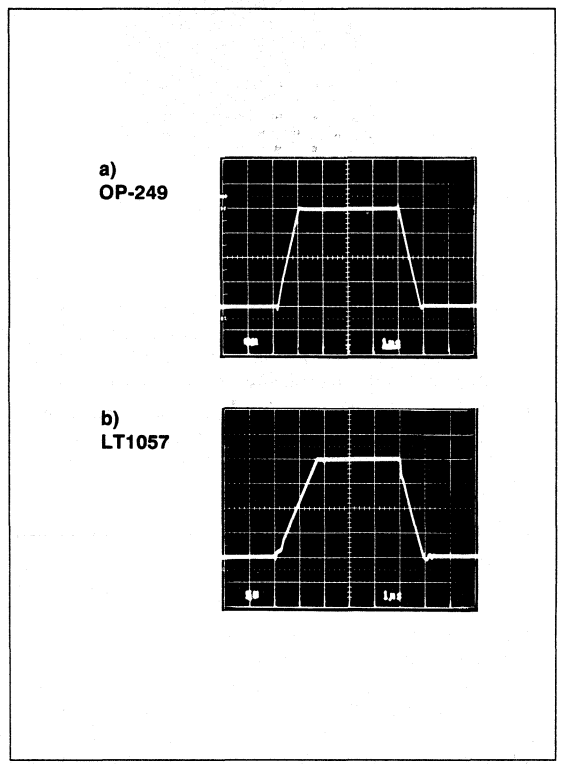


FIGURE 1: *Large-Signal Transient Response, A_V = +1, V_{IN} = 20V_{p-p}, Z_L = 2kΩ||200pF, V_S = ±15V*

The OP-249 was carefully designed to provide symmetrically matched slew characteristics in both the negative and positive directions, even when driving a large output load.

An amplifier's slewing limitation determines the maximum frequency at which a sinusoidal output can be obtained without significant distortion. It is, however, important to note that the nonsymmetric slewing typical of previously available JFET amplifiers adds a higher series of harmonic energy content to the resulting response – and an additional DC output component. Examples of potential problems of nonsymmetric slewing behaviour could be in audio amplifier applications, where a natural, low-distortion sound quality is desired, and in servo or signal processing systems where a net DC offset cannot be tolerated. The linear and symmetric slewing feature of the OP-249 makes it an ideal choice for applications that will exceed the full-power-bandwidth range of the amplifier.

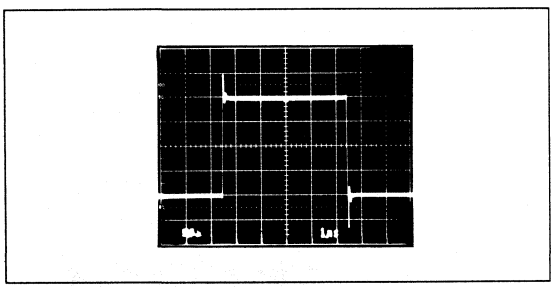


FIGURE 2: *Small-Signal Transient Response, A_V = +1, Z_L = 2kΩ||100pF, No Compensation, V_S = ±15V*

As with most JFET-input amplifiers, the output of the OP-249 may undergo phase inversion if either input exceeds the specified input voltage range. Phase inversion will not damage the amplifier, nor will it cause an internal latch-up condition.

Supply decoupling should be used to overcome inductance and resistance associated with supply lines to the amplifier. A 0.1μF and a 10μF capacitor should be placed between each supply pin and ground.

OPEN-LOOP GAIN LINEARITY

The OP-249 has both an extremely high open-loop gain of 1kV/mV minimum and constant gain linearity. This feature of the OP-249 enhances its DC precision, and provides superb accuracy in high closed-loop gain applications. Figure 3 illustrates the typical open-loop gain linearity – high gain accuracy is assured, even when driving a 600Ω load.

OFFSET VOLTAGE ADJUSTMENT

The inherent low offset voltage of the OP-249 will make offset adjustments unnecessary in most applications. However, where a lower offset error is required, balancing can be performed with simple external circuitry, as illustrated in Figures 4 and 5.

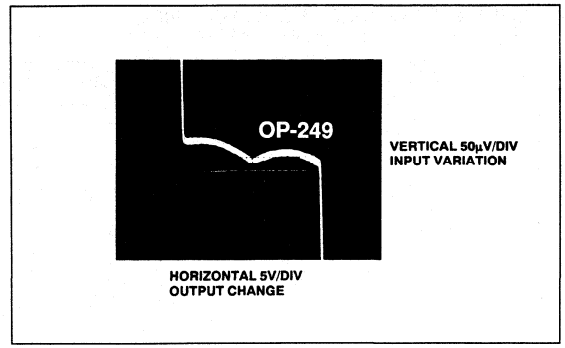


FIGURE 3: *Open-Loop Gain Linearity. Variation in Open-Loop Gain Results in Errors in High Closed-Loop Gain Circuits. R_L = 600Ω, V_S = ±15V*

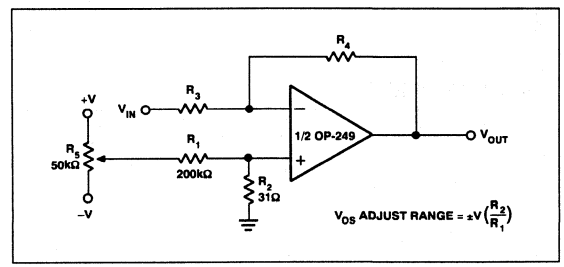


FIGURE 4: *Offset Adjust for Inverting Amplifier Configuration*

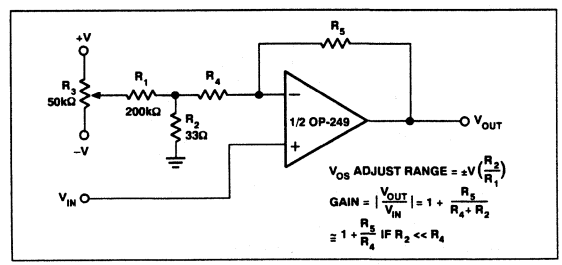


FIGURE 5: *Offset Adjust for Noninverting Amplifier Configuration*

In Figure 4, the offset adjustment is made by supplying a small voltage at the noninverting input of the amplifier. Resistors R_1 and R_2 attenuates the pot voltage, providing a ±2.5mV (with V_S = ±15V) adjustment range, referred to the input. Figure 5 illustrates offset adjust for the noninverting amplifier configuration, also providing a ±2.5mV adjustment range. As indicated in the equations in Figure 5, if R_4 is not much greater than R_2, there will be a resulting closed-loop gain error that must be accounted for.

Settling time is the time between when the input signal begins to change and when the output permanently enters a prescribed error band. The error bands on the output are 5mV and 0.5mV, respectively, for 0.1% and 0.01% accuracy.

Figure 6 illustrates the OP-249's typical settling time of 870ns. Moreover, problems in settling response, such as thermal tails and long-term ringing are nonexistent.

DAC OUTPUT AMPLIFIER

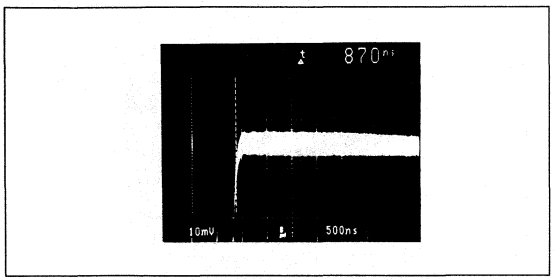


FIGURE 6: *Settling Characteristics of the OP-249 to 0.01%.*

Unity-gain stability, a low offset voltage of 300μV typical, and a fast settling time of 870ns to 0.01%, makes the OP-249 an ideal amplifier for fast digital-to-analog converters.

For CMOS DAC applications, the low offset voltage of the OP-249 results in excellent linearity performance. CMOS DACs, such as the PM-7545, will typically have a code-dependent output resistance variation between 11kΩ and 33kΩ. The change in output resistance, in conjunction with the 11kΩ feedback resistor, will result in a noise gain change. This causes variations in the offset error, increasing linearity errors. The OP-249 features low offset voltage error, minimizing this effect and maintaining 12-bit linearity performance over the full scale range of the converter.

Since the DAC's output capacitance appears at the operational amplifiers inputs, it is essential that the amplifier is adequately compensated. Compensation will increase the phase margin, and ensure an optimal overall settling response. The required lead compensation is achieved with capacitor C in Figure 7.

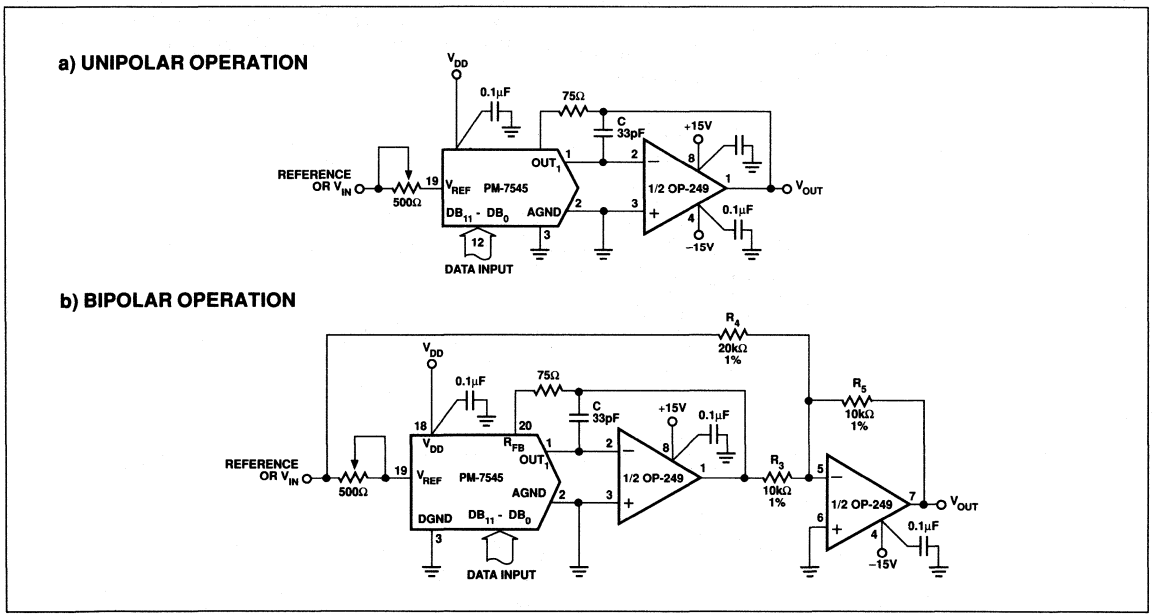


FIGURE 7: *Fast Settling and Low Offset Error of the OP-249 Enhances CMOS DAC Performance*

Figure 8 illustrates the effect of altering the compensation on the output response of the circuit in Figure 6a. Compensation is required to address the combined effect of the DAC's output capacitance, the op amp's input capacitance, and any stray capacitance. Slight adjustments to the compensation capacitor may be required to optimize settling response for any given application.

The settling time of the combination of the current output DAC and the op amp can be approximated by:

$$t_{S\ TOTAL} = \sqrt{(t_{S\ DAC})^2 + (t_{S\ AMP})^2}$$

The actual overall settling time is affected by the noise gain of the amplifier, the applied compensation, and the equivalent input capacitance at the amplifier's input.

DISCUSSION ON DRIVING A/D CONVERTERS

Settling characteristics of operational amplifiers also include an amplifier's ability to recover, i.e., settle, from a transient current output load condition. An example of this includes an op amp driving the input from a SAR type A/D converter. Although the comparison point of the converter is usually diode clamped, the input swing of plus-and-minus a diode drop still gives rise to a significant modulation of input current. If the closed-loop output impedance is low enough and bandwidth of the amplifier is sufficiently large, the output will settle before the converter makes a comparison decision which will prevent linearity errors or missing codes.

Figure 9 shows a settling measurement circuit for evaluating recovery from an output current transient. An output disturbing

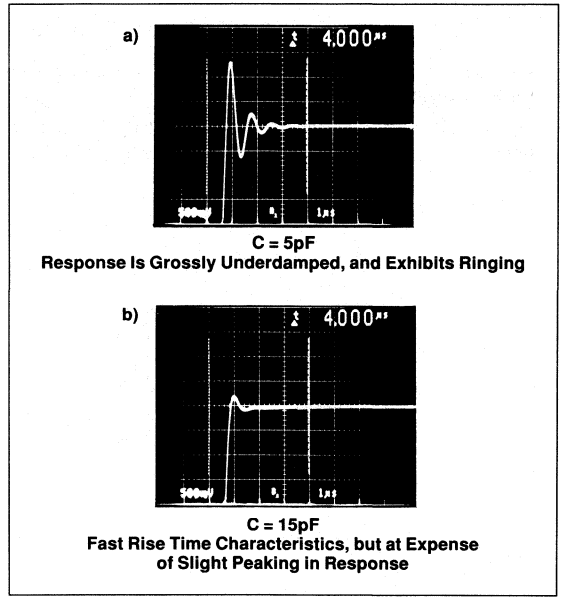


FIGURE 8: *Effect of Altering Compensation from Circuit in Figure 7a – PM-7545 CMOS DAC with 1/2 OP-249, Unipolar Operation. Critically Damped Response Will Be Obtained with C ≈ 33pF*

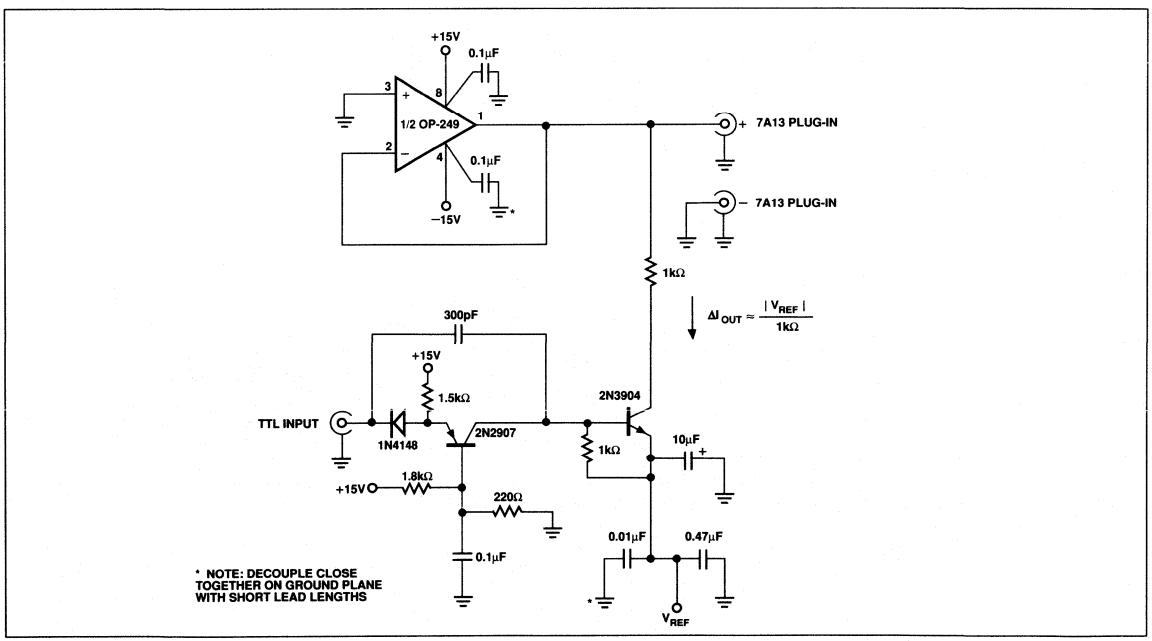


FIGURE 9: *Transient Output Impedance Test Fixture*

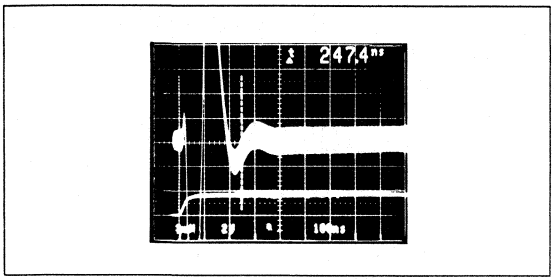


FIGURE 10: *OP-249's Transient Recovery Time from a 1mA Load Transient to 0.01%*

current generator provides the transient change in output load current of 1mA. As seen in Figure10, the OP-249 has extremely fast recovery of 274ns (to 0.01%), for a 1mA load transient. The performance makes it an ideal amplifier for data acquisition systems.

The combination of high speed and excellent DC performance of the OP-249 makes it an ideal amplifier for 12-bit data acquisition systems. Examining the circuit in Figure 11, one amplifier in the OP-249 provides a stable –5V reference voltage for the V_{REF} input of the ADC-912. The other amplifier in the OP-249 performs high-speed buffering of the A/D's input.

Examining the worst case transient voltage error (Figure 12) at the Analog In node of the A/D converter: the OP-249 recovers in less than 100ns. The fast recovery is due to both the OP-249's wide bandwidth and low DC output impedance.

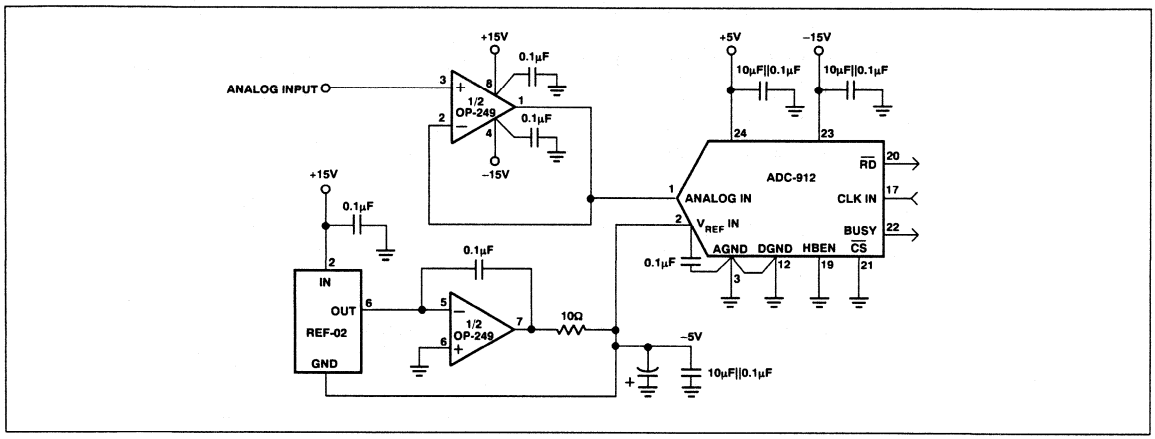


FIGURE 11: *OP-249 Dual Amplifiers Provide Both Stable –5V Reference Input, and Buffers Input to ADC-912*

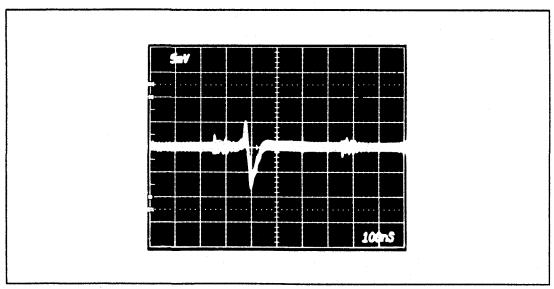


FIGURE 12: *Worst Case Transient Voltage, at Analog In, Occurs at the Half-Scale Point of the A/D. OP-249 Buffers the A/D Input from Figure 11, and Recovers in Less than 100ns*

OP-249 SPICE MACRO-MODEL

Figures 13 and 14 show the node and net list for a SPICE macromodel of the OP-249. The model is a simplified version of the actual device and simulates important DC parameters such as V_{OS}, I_{OS}, I_B, A_{VO}, CMR, V_O and I_{SY}. AC parameters such as slew rate, gain and phase reponse and CMR change with frequency are also simulated by the model.

The model uses typical parameters for the OP-249. The poles and zeros in the model were determined from the actual open and closed-loop gain and phase reponse of the OP-249. In this way the model presents an accurate AC representation of the actual device. The model assumes an ambient temperature of 25°C.

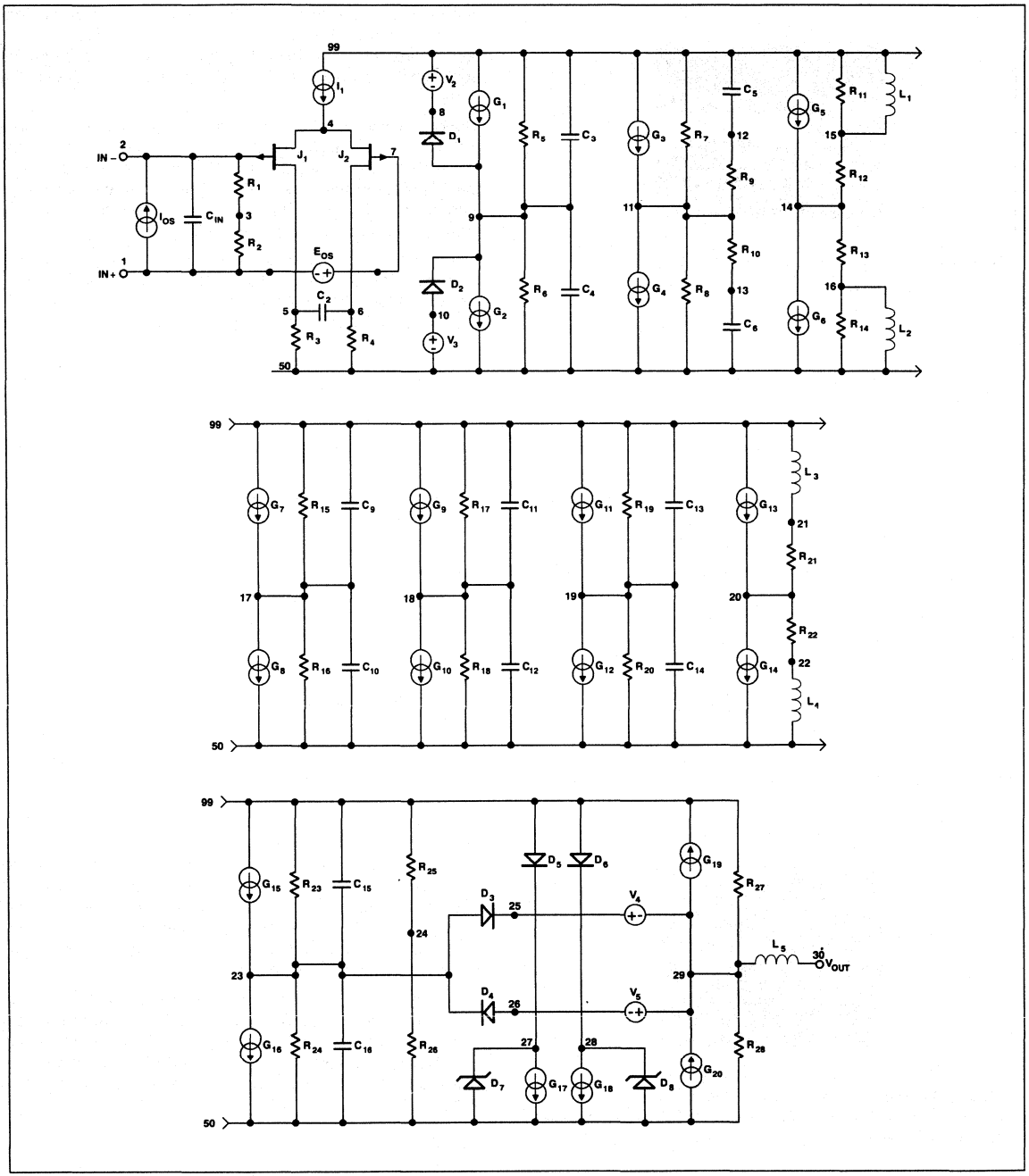


FIGURE 13: *OP-249 Macro-Model*

```
OP-249 MACRO-MODEL    © PMI 1989
*
* subckt OP-249 1  2 30 99 50
*
INPUT STAGE & POLE AT 100MHz
*
r1   2   3        5E11
r2   1   3        5E11
r3   5   50       652.3
r4   6   50       652.3
cin  1   2        5E-12
c2   5   6        1.22E-12
i1   99  4        1E-3
ios  1   2        3.1E-12
eos  7   1        poly(1) 20 24 150E-6 1
j1   5   2   4    jx
j2   6   7   4    jx
*
* SECOND STAGE & POLE AT 12.2Hz
*
r5   9   99       326.1E6
r6   9   50       326.1E6
c3   9   99       40E-12
c4   9   50       40E-12
g1   99  9        poly(1) 5 6 4.25E-3 1.533E-3
g2   9   50       poly(1) 6 5 4.25E-3 1.533E-3
v2   99  8        2.9
v3   10  50       2.9
d1   9   8        dx
d2   10  9        dx
*
* POLE-ZERO PAIR AT 2MHz/4.0MHz
*
r7   11  99       1E6
r8   11  50       1E6
r9   11  12       1E6
r10  11  13       1E6
c5   12  99       37.79E-15
c6   13  50       37.79E-15
g3   99  11       9  24 1E-6
g4   11  50       24 9  1E-6
*
* ZERO-POLE PAIR AT 4MHz/8MHz
*
r11  99  15       1E6
r12  14  15       1E6
r13  14  16       1E6
r14  50  16       1E6
l1   99  15       19.89E-3
l2   50  16       19.89E-3
g5   99  14       11 24 1E-6
g6   14  50       24 11 1E-6
*
* POLE AT 20MHz
*
r15  17  99       1E6
r16  17  50       1E6
c9   17  99       7.96E-15
c10  17  50       7.96E-15
g7   99  17       14 24 1E-6
g8   17  50       24 14 1E-6
*
* POLE AT 50MHz
*
r17  18  99       1E6
r18  18  50       1E6
c11  18  99       3.18E-15
c12  18  50       3.18E-15
g9   99  18       17 24 1E-6
g10  18  50       24 17 1E-6
*
* POLE AT 50MHz
*
r19  19  99       1E6
r20  19  50       1E6
c13  19  99       3.18E-15
c14  19  50       3.18E-15
g11  99  19       18 24 1E-6
g12  19  50       24 18 1E-6
*
* COMMON-MODE GAIN NETWORK WITH ZERO AT 60kHz
*
r21  20  21       1E6
r22  20  22       1E6
l3   21  99       2.65
l4   22  50       2.65
g13  99  20       3  24 1.78E-11
g14  20  50       24 3  1.78E-11
*
* POLE AT 50MHz
*
r23  23  99       1E6
r24  23  50       1E6
c15  23  99       3.18E-15
c16  23  50       3.18E-15
g15  99  23       19 24 1E-6
g16  23  50       24 19 1E-6
*
* OUTPUT STAGE
*
r25  24  99       135E3
r26  24  50       135E3
r27  29  99       70
r28  29  50       70
l5   29  30       4E-7
g17  27  50       23 29 14.3E-3
g18  28  50       29 23 14.3E-3
g19  29  99       99 23 14.3E-3
g20  50  29       23 50 14.3E-3
v4   25  29       .4
v5   29  26       .4
d3   23  25       dx
d4   26  23       dx
d5   99  27       dx
d6   99  28       dx
d7   50  27       dy
d8   50  28       dy
*
* MODELS USED
*
• model jx PJF(BETA=1.175E-3 VTO=-2.000 IS=21E-12)
• model dx   D(IS=1E-15)
• model dy   D(IS=1E-15 BV=50)
• ends OP-249
```

FIGURE 14: *OP-249 SPICE Net List*

* PSpice is a registered trademark of MicroSim Corporation.
** HSPICE is a tradename of Meta-Software, Inc.

Dual, High-Speed, Current Feedback Operational Amplifier

OP-260

FEATURES

- Very High Slew Rate ..... 550V/μs Typ
- -3dB Bandwidth (A_V=+10) ..... 40MHz Typ
- Bandwidth Independent of Gain
- Unity-Gain Stable
- Low Supply Current ..... 4.5mA per amp Typ

ORDERING INFORMATION†

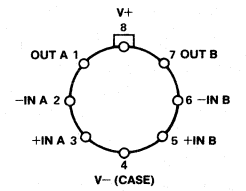
T_A = 25°C V_{IOS} MAX (mV)	PACKAGE			OPERATING TEMPERATURE RANGE
	TO-99 8-PIN	PLASTIC	LCC 20-CONTACT	
3.5	OP260AJ*	–	OP260ARC/883	MIL
3.5	OP260EJ	–	–	XIND
5.0	OP260FJ	–	–	XIND
7.0	–	OP260GP	–	XIND
7.0	–	OP260GS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

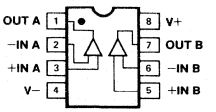
† Burn-in is available on commercial and industrial temperature range parts in cerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO packages, contact your local sales office.

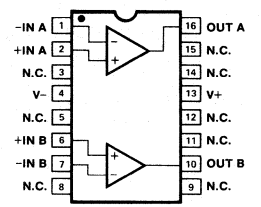
PIN CONNECTIONS



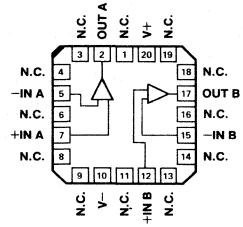
TO-99
(J-Suffix)



EPOXY MINI-DIP
(P-Suffix)
CERDIP
(Z-Suffix)



16-PIN SOL
(S-Suffix)



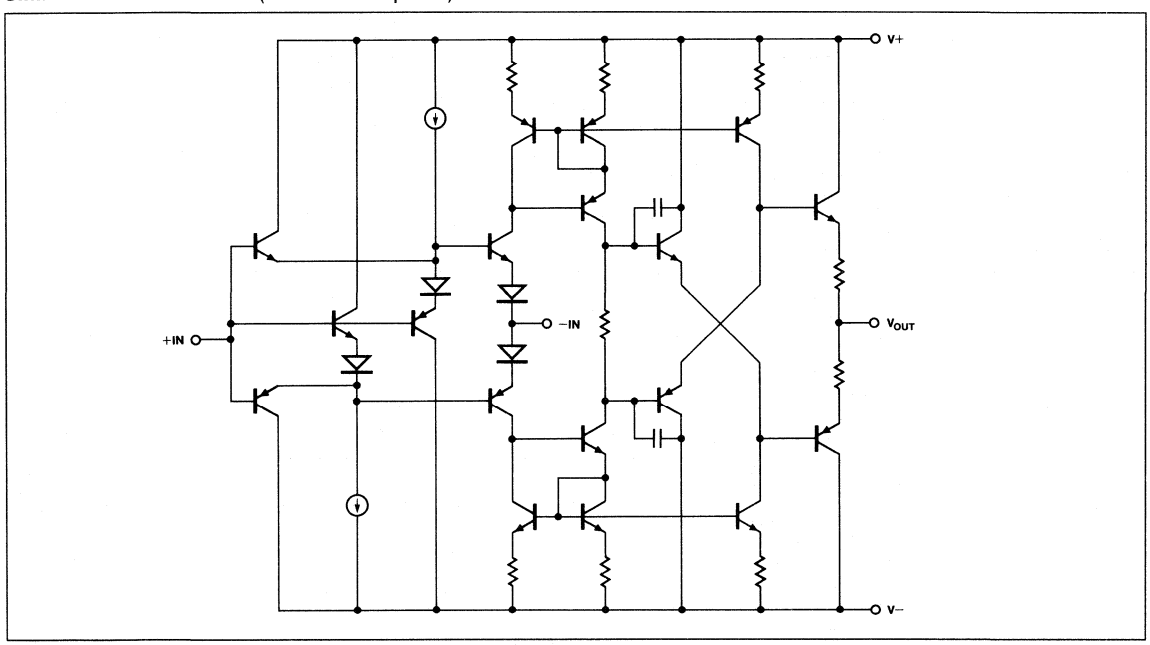
20-CONTACT
HERMETIC LCC
(RC-Suffix)

GENERAL DESCRIPTION

The dual OP-260 represents a new concept in monolithic operational amplifiers. Built on PMI's high-speed bipolar process, the OP-260

continued

SIMPLIFIED SCHEMATIC (One of Two Amplifiers)



GENERAL DESCRIPTION *Continued*

employs current feedback to provide consistently wideband operation regardless of gain. The OP-260's –3dB bandwidth of 90MHz at A_V=+1 combines with a slew rate of 1000V/µs for extremely high-speed operation. For its high-speed bandwidth, the OP-260 requires only 4.5mA of supply current per amplifier, a considerable power savings over other high-speed operational amplifiers.

The OP-260 is easy to design with, since most of the circuit assumptions for voltage feedback amplifiers can also be used for current feedback amplifiers. The two independent amplifiers of the OP-260 allow two channel amplification with matched AC performance. It is also ideal for high-speed instrumentation amplifiers. Other applications for the OP-260 include ultrasound and sonar systems, video amplifiers and high-speed data acquisition systems.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Input Voltage ..... Supply Voltage
Differential Input Voltage ..... ±1V
Inverting Input Current ..... ±7mA Continuous
..... ±20mA Peak
Output Short-Circuit Duration ..... 10 sec
Operating Temperature Range
OP-260A, (J, RC, Z) ..... –55°C to +125°C
OP-260E/F (J, Z) ..... –40°C to +85°C
OP-260G (P, S) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +175°C
Junction Temperature Range (J, RC) ..... –65°C to +175°C
Junction Temperature Range (P, S) ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
TO-99 (J)	145	16	°C/W
8-Pin Hermetic DIP (Z)	134	12	°C/W
8-Pin Plastic DIP (P)	96	37	°C/W
20-Contact LCC (RC)	88	33	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, V_{CM} = 0V, R_F = 2.5kΩ, T_A = +25°C, unless otherwise noted.

			OP-260A/E			OP-260F			OP-260G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{IOS}		–	1	3.5	–	2	5	–	3	7	mV
Input Bias Current	I_{B+} I_{B-}	Noninverting Input Inverting Input	– –	0.2 3	1 8	– –	0.3 4	2 10	– –	0.5 5	3 15	µA
Input Bias Current Common-Mode Rejection Ratio	$CMRRI_{B-}$	Inverting Input V_{CM} = ±11V	–	0.04	0.1	–	0.06	0.2	–	0.1	0.5	µA/V
Input Bias Current Power Supply Rejection Ratio	$PSRRI_{B-}$ $PSRRI_{B+}$	Inverting Input Noninverting Input V_S = ±9V to ±18V	– –	0.02 0.002	0.1 0.02	– –	0.04 0.004	0.2 0.04	– –	0.05 0.01	0.5 0.1	µA/V
Common-Mode Rejection	CMR	V_{CM} = ±11V	56	62	–	50	60	–	50	60	–	dB
Power Supply Rejection	PSR	V_S = ±9V to ±18V	66	72	–	60	66	–	60	66	–	dB
Open-Loop Transimpedance	R_T	R_L = 1kΩ V_O = ±10V	5	7	–	4	5	–	4	5	–	MΩ
Input Voltage Range	IVR		±11	–	–	±11	–	–	±11	–	–	V
Output Voltage Swing	V_O	R_L = 1kΩ I_{OUT} = ±20mA	±12 ±11	±12.6 ±11.5	– –	±12 ±11	±12.6 ±11.5	– –	±12 ±11	±12.6 ±11.5	– –	V
Supply Current	I_{SY}	No Load, Both Amplifiers	–	9	10.5	–	9	10.5	–	9	10.5	mA
Slew Rate	SR	A_V = +1, V_O = ±10V, R_L = 1kΩ, Test at V_O = ±5V	–	1000	–	–	1000	–	–	1000	–	V/µs
		A_V = +10, V_O = ±10V, R_L = 1kΩ, Test at V_O = ±5V	375	550	–	300	550	–	300	550	–	
		A_V = +10, V_O = ±10V, R_L = 1kΩ, Test at V_O = ±5V 8-pin Hermetic DIP (Z) Package	300	–	–	300	–	–	–	–	–	

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $V_{CM} = 0V$, $R_F = 2.5k\Omega$, $T_A = 25°C$, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	OP-260A/E MIN	OP-260A/E TYP	OP-260A/E MAX	OP-260F MIN	OP-260F TYP	OP-260F MAX	OP-260G MIN	OP-260G TYP	OP-260G MAX	UNITS
–3dB Bandwidth	BW	–3dB point $A_V = -1$ $R_L = 500\Omega$ $A_V = +1$ $A_V = +10$	– – –	55 90 40	– – –	– – –	55 90 40	– – –	– – –	55 90 40	– – –	MHz
Settling Time	t_S	$A_V = -1$, 10V step, 0.1%	–	250	–	–	250	–	–	250	–	ns
Input Capacitance	C_{IN}	Noninverting and Inverting Inputs	–	4.5	–	–	4.5	–	–	4.5	–	pF
Channel Separation	CS	$f_O = 100kHz$, $V_O = 10Vp\text{-}p$, $R_L = 100\Omega$	–	100	–	–	100	–	–	100	–	dB

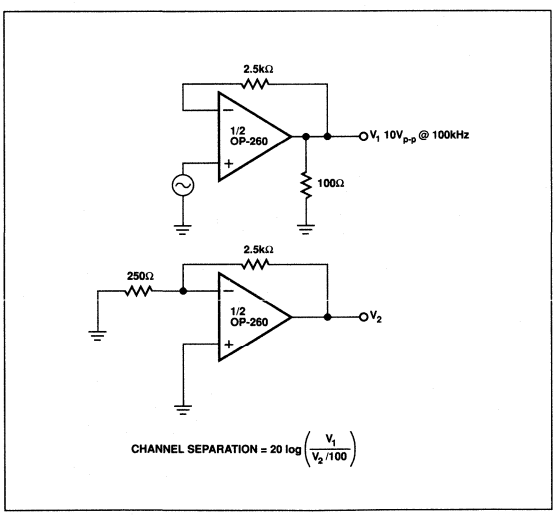
ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $V_{CM} = 0V$, $R_F = 2.5k\Omega$, $-55°C \le T_A \le +125°C$, for the OP-260A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-260A MIN	OP-260A TYP	OP-260A MAX	UNITS
Input Offset Voltage	V_{IOS}		–	1.8	6	mV
Average Input Offset Voltage Drift	TCV_{IOS}		–	8	–	µV/°C
Input Bias Current	I_{B+} I_{B-}	Noninverting Input Inverting Input	– –	0.3 4	2 12	µA
Input Bias Current Common Mode Rejection Ratio	$CMRRI_{B-}$	Inverting Input $V_{CM} = \pm11V$	–	0.05	0.2	µA/V
Input Bias Current Power Supply Rejection Ratio	$PSRRI_{B-}$ $PSRRI_{B+}$	Inverting Input Noninverting Input $V_S = \pm9V$ to $\pm18V$	– –	0.03 0.003	0.2 0.05	µA/V
Common Mode Rejection	CMR	$V_{CM} = \pm11V$	52	58	–	dB
Power Supply Rejection	PSR	$V_S = \pm9V$ to $\pm18V$	62	70	–	dB
Open-Loop Transimpedance	R_T	$R_L = 1k\Omega$, $V_O = \pm10V$	3	4.8	–	MΩ
Input Voltage Range	IVR		±11	–	–	V
Output Voltage Swing	V_O	$R_L = 1k\Omega$ $I_{OUT} = \pm20mA$	±11.5 ±10.5	±12.4 ±11.1	– –	V
Supply Current	I_{SY}	No load, Both Amplifiers	–	9	11.5	mA

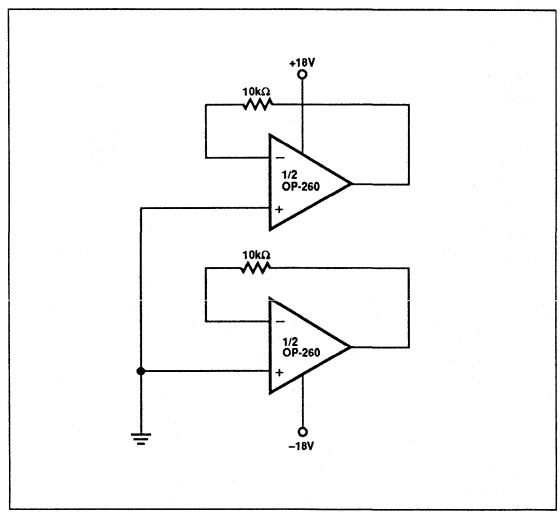
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $V_{CM} = 0V$, $R_F = 2.5k\Omega$, $-40°C \leq T_A \leq +85°C$ for the OP-260E/F/G, unless otherwise noted.

			OP-260E			OP-260F			OP-260G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{IOS}		–	1.4	6	–	2.5	8	–	3.7	10	mV
Average Input Offset Voltage Drift	TCV_{IOS}		–	6	–	–	8	–	–	10	–	µV/°C
Input Bias Current	I_{B+} I_{B-}	Noninverting Input Inverting Input	– –	0.3 4	2 12	– –	0.4 5	3 15	– –	0.6 7	5 20	µA
Input Bias Current Common Mode Rejection Ratio	$CMRRI_{B-}$	Inverting Input $V_{CM} = \pm 11V$	–	0.05	0.2	–	0.7	0.4	–	0.15	1.0	µA/V
Input Bias Current Power Supply Rejection Ratio	$PSRRI_{B-}$ $PSRRI_{B+}$	Inverting Input Noninverting Input	– –	0.03 0.003	0.2 0.05	– –	0.05 0.005	0.4 0.1	– –	0.1 0.01	1.0 0.2	µA/V
Common Mode Rejection	CMR	$V_{CM} = \pm 11V$	52	60	–	50	58	–	50	58	–	dB
Power Supply Rejection	PSR	$V_S = \pm 9V$ to $\pm 15V$	62	70	–	60	64	–	60	64	–	dB
Open-Loop Transimpedance	R_T	$R_L = 1k\Omega$, $V_O = \pm 10V$	3	5	–	2	4	–	2	4	–	MΩ
Input Voltage Range	IVR		±11	–	–	±11	–	–	±11	–	–	V
Output Voltage Swing	V_O	$R_L = 1k\Omega$ $I_{OUT} = \pm 20mA$	±11.5 ±10.5	±12.5 ±11.1	–	±11.5 ±10.5	±12.5 ±11.1	–	±11.5 ±10.5	±12.5 ±11.1	–	V
Supply Current	I_{SY}	No Load, Both Amplifiers	–	9	11.5	–	9	11.5	–	9	11.5	mA

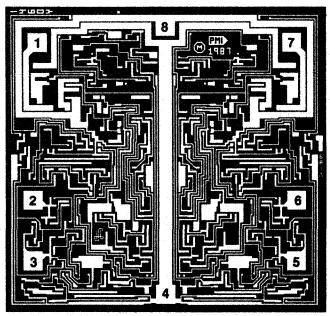
CHANNEL SEPARATION TEST CIRCUIT



BURN-IN CIRCUIT



DICE CHARACTERISTICS



DIE SIZE 0.089 x 0.086 inch, 7,654 sq. mils
(2.26 x 2.18 mm, 4.93 sq. mm)

1. OUT A
2. - IN A
3. + IN A
4. V-
5. + IN B
6. - IN B
7. OUT B
8. V +

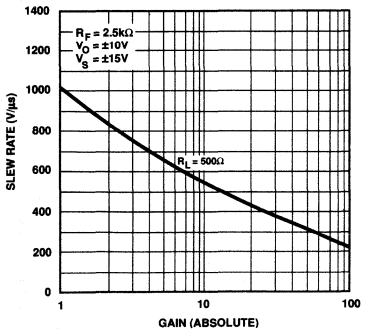
WAFER TEST LIMITS at $V_S = \pm 15V$, $V_{CM} = 0V$, $R_F = 2.5k\Omega$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-260GBC LIMITS	UNITS
Input Offset Voltage	V_{IOS}		5	mV MAX
Input Bias Current	I_{B+} I_{B-}	Noninverting Input Inverting Input	2 10	µA MAX
Input Bias Current Common Mode Rejection Ratio	$CMRRI_B$	Inverting Input $V_{CM} = +11V$	0.2	µA/V MAX
Input Bias Current Power Supply Rejection Ratio	$PSRRI_{B-}$ $PSRRI_{B+}$	Inverting Input Noninverting Input $V_S = \pm 9V$ to $\pm 18V$	0.2 0.04	µA/V MAX
Common Mode Rejection	CMR	$V_{CM} = \pm 11V$	50	dB MIN
Power Supply Rejection	PSR	$V_S = \pm 9V$ to $\pm 18V$	60	dB MIN
Open-Loop Transimpedance	R_T	$R_L = 1k\Omega$, $V_O = \pm 10V$	4	MΩ MIN
Input Voltage Range	IVR		±11	V MIN
Output Voltage Swing	V_O	$R_L = 1k\Omega$ $I_{OUT} = \pm 20mA$	±12 ±11	V MIN
Supply Current	I_{SY}	No Load, Both Amplifiers	10.5	mA MAX

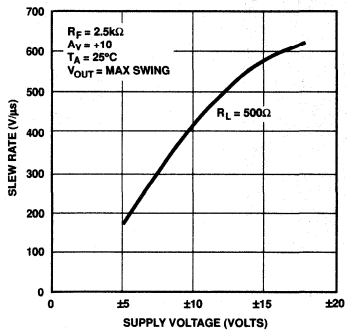
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS

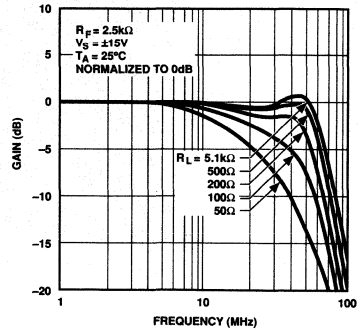
SLEW RATE vs GAIN



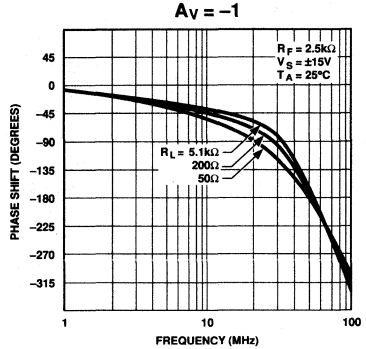
SLEW RATE vs SUPPLY VOLTAGE



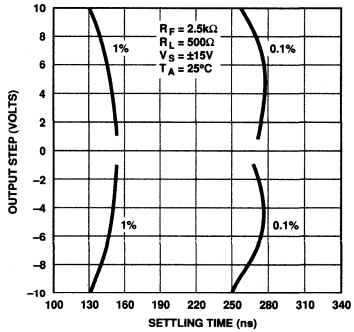
GAIN vs FREQUENCY A_V = –1



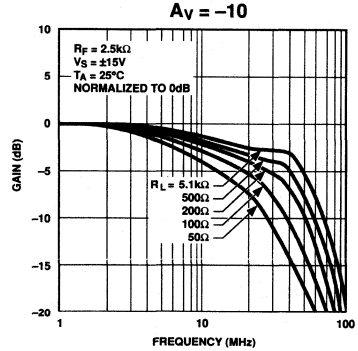
PHASE SHIFT vs FREQUENCY A_V = –1



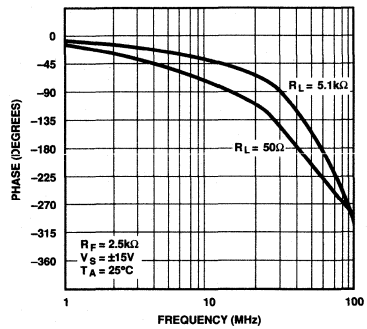
SETTLING TIME vs OUTPUT STEP A_V = –1



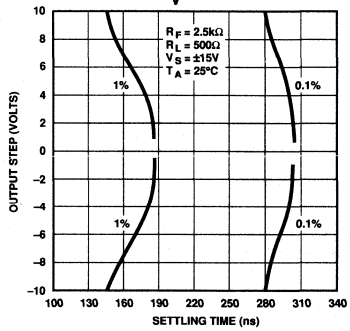
GAIN vs FREQUENCY A_V = –10



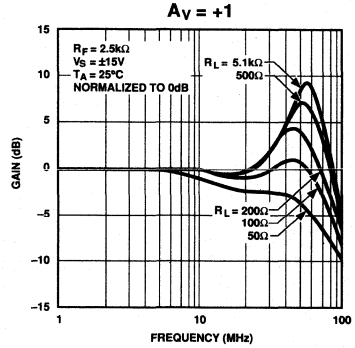
PHASE vs FREQUENCY A_V = –10



SETTLING TIME vs OUTPUT STEP A_V = –10

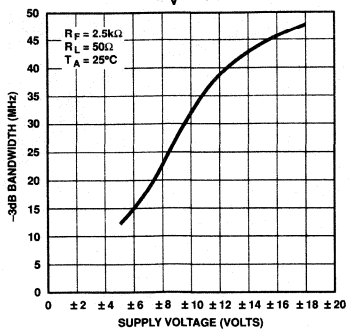


GAIN vs FREQUENCY A_V = +1

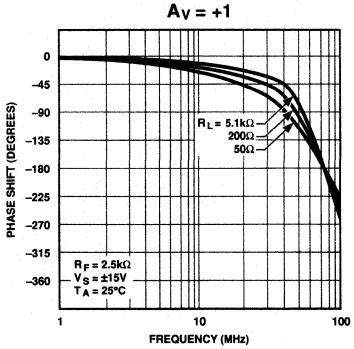


TYPICAL ELECTRICAL CHARACTERISTICS *Continued*

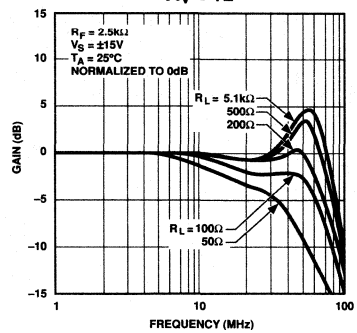
SMALL-SIGNAL –3dB BANDWIDTH vs SUPPLY VOLTAGE A_V = +1



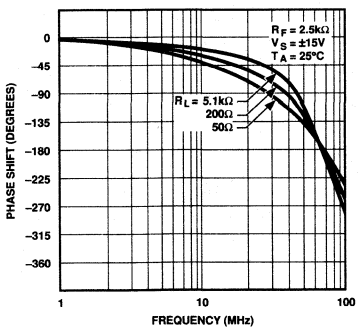
PHASE SHIFT vs FREQUENCY A_V = +1



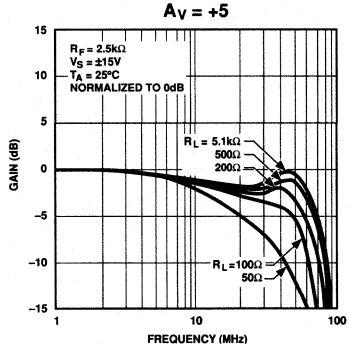
GAIN vs FREQUENCY A_V = +2



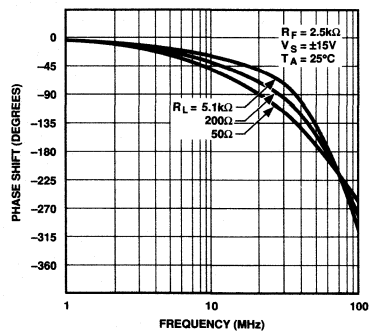
PHASE SHIFT vs FREQUENCY A_V = +2



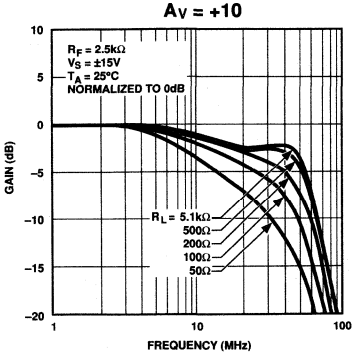
GAIN vs FREQUENCY A_V = +5



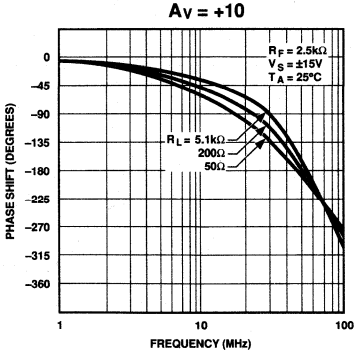
PHASE SHIFT vs FREQUENCY A_V = +5



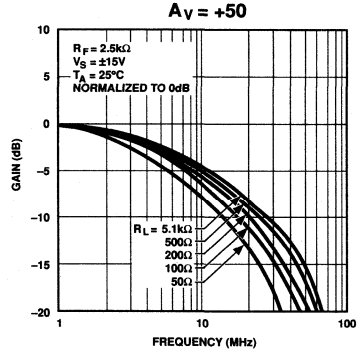
GAIN vs FREQUENCY A_V = +10



PHASE SHIFT vs FREQUENCY A_V = +10

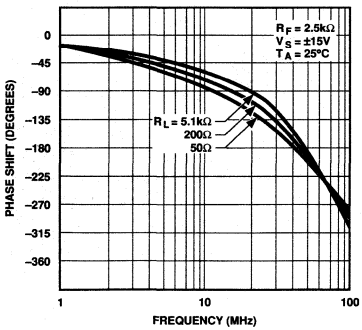


GAIN vs FREQUENCY A_V = +50

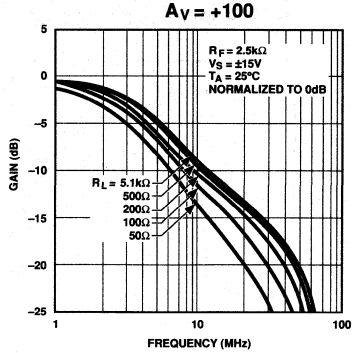


TYPICAL ELECTRICAL CHARACTERISTICS *Continued*

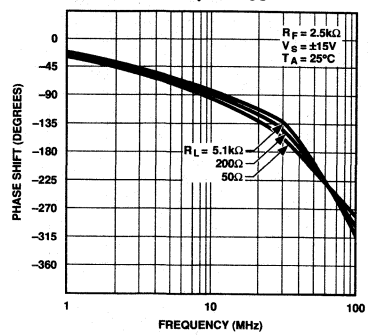
PHASE SHIFT vs FREQUENCY
A_V = +50



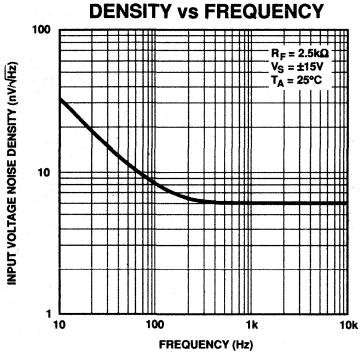
GAIN vs FREQUENCY
A_V = +100



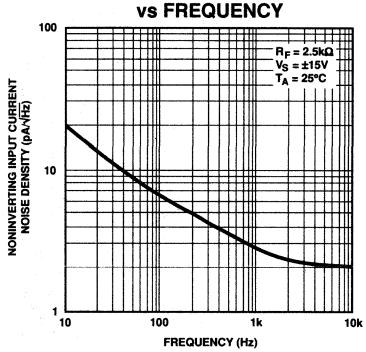
PHASE SHIFT vs FREQUENCY
A_V = +100



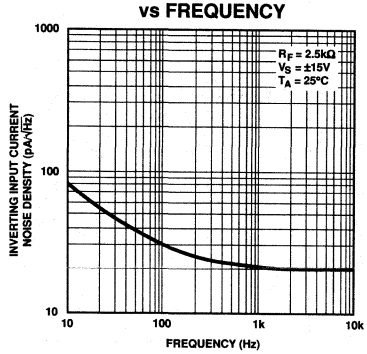
INPUT VOLTAGE NOISE DENSITY vs FREQUENCY



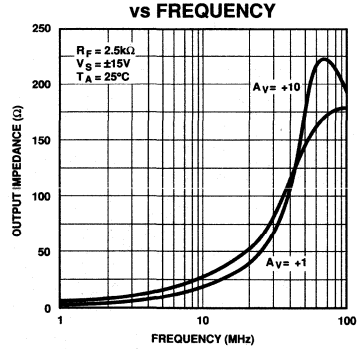
NONINVERTING INPUT CURRENT NOISE DENSITY vs FREQUENCY



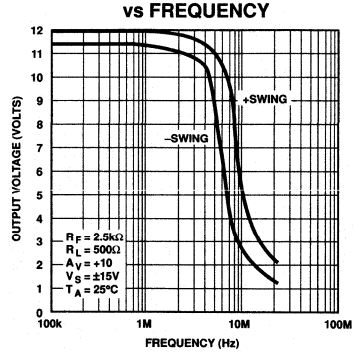
INVERTING INPUT CURRENT NOISE DENSITY vs FREQUENCY



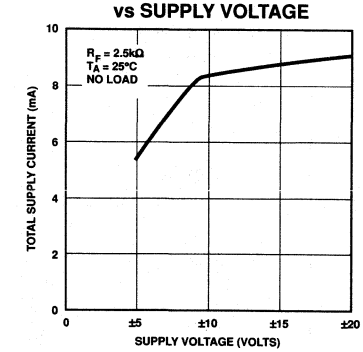
OUTPUT IMPEDANCE vs FREQUENCY



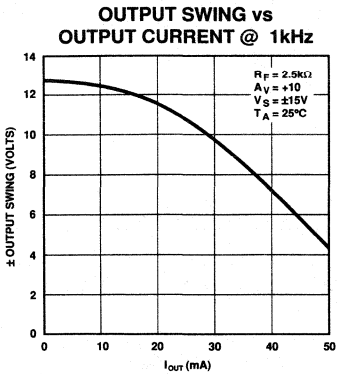
MAXIMUM OUTPUT SWING vs FREQUENCY

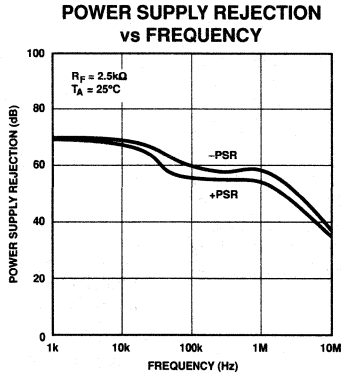


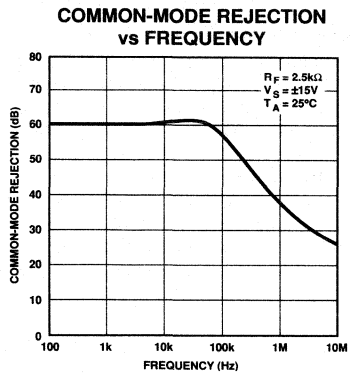
TOTAL SUPPLY CURRENT vs SUPPLY VOLTAGE



TYPICAL ELECTRICAL CHARACTERISTICS *Continued*







2

APPLICATIONS INFORMATION

CURRENT VERSUS VOLTAGE FEEDBACK AMPLIFIERS

The dual OP-260 employs a unique circuit topology that sets it apart from conventional op amps. By using a transimpedance amplifier configuration, the OP-260 provides substantial improvements in bandwidth and slew rate over voltage feedback op amps. Figure 1 compares models of these two different amplifier configurations.

A voltage feedback op amp multiplies the differential voltage at its inputs by its open-loop gain. The feedback loop forces the output to a voltage that, when divided by R_1 and R_2, equalizes the input voltages. Unlike a voltage feedback op amp, which has high impedance inputs, the current feedback amplifier has a high and a low impedance input. The current feedback amplifier's input stage consists of a unity-gain voltage buffer between the noninverting and inverting inputs. The inverting "input" is in reality a low impedance output. Current can flow into or out of the inverting input. A transimpedance stage follows the input buffer that converts the buffer output current into a linearly proportional amplifier output voltage.

The current feedback amplifier loop works in the following fashion (Figure 1b). As the noninverting input voltage rises, the inverting input follows and the buffer sources current through R_1. This current, multiplied by the transimpedance stage, causes the amplifier's output voltage to rise until the current flowing into R_2 from the amplifier's output equalizes the current through R_1, replacing the buffer's output current. At steady state, only a very small buffer output current must flow to sustain the proper output voltage. The ratio $(1 + R_2/R_1)$ determines the

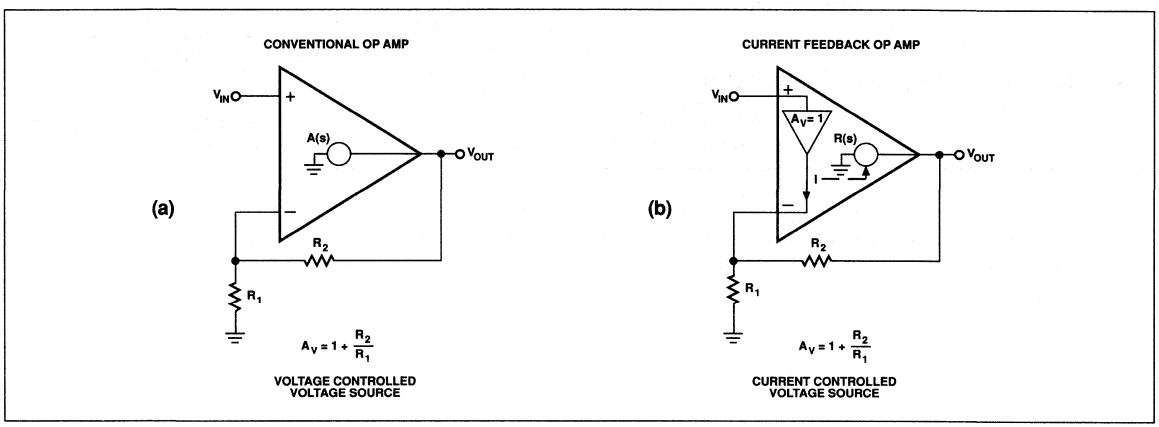


FIGURE 1: *The conventional op amp (a) can be modelled as a voltage-controlled voltage source. In contrast, the current feedback op amp (b), resembles a current-controlled voltage source.*

closed-loop gain of the circuit. The result is that when designing with current feedback amplifiers the familiar op amp assumptions can still be used for circuit analysis:

1. The voltage across the inputs equals zero.
2. The current into the inputs equals zero.

BANDWIDTH VERSUS GAIN

A unique feature of the current feedback amplifier design is that the closed-loop bandwidth remains relatively constant as a function of closed-loop gain. Voltage feedback op amps suffer from a bandwidth reduction as closed-loop gain increases, as quantified by the gain-bandwidth product (GBWP). This is illustrated in Figure 2 which shows the frequency response of the OP-260 for various closed-loop gains and the frequency response of a voltage feedback op amp with a gain-bandwidth product of 30MHz. The bandwidth of the OP-260 is much less dependent upon closed-loop gain than the voltage feedback op amp.

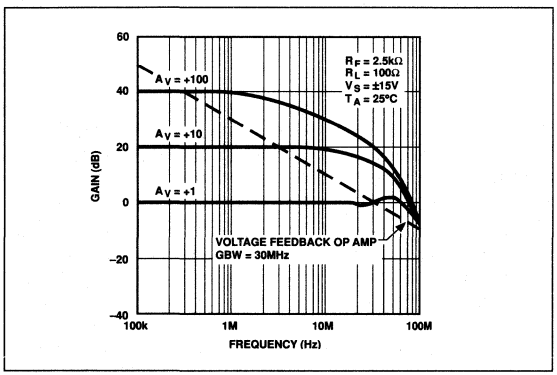


FIGURE 2: *Frequency response of the OP-260 when connected in various closed-loop gains with R_F = 2.5kΩ and R_L = 100Ω. Note that the frequency response of the OP-260 does not follow the asymptotic roll-off characteristic of a voltage feedback op-amp.*

FEEDBACK RESISTANCE AND BANDWIDTH

The closed-loop frequency response of the OP-260 shown in Figure 2 applies for a fixed feedback resistor of 2.5kΩ. The frequency response of a current feedback amplifier is primarily dependent on the value of the feedback resistor. The design of the OP-260 has been optimized for a feedback resistance of 2.5kΩ. By holding the feedback resistor value constant, the –3dB frequency point will also remain constant within a moderate range of closed-loop gain.

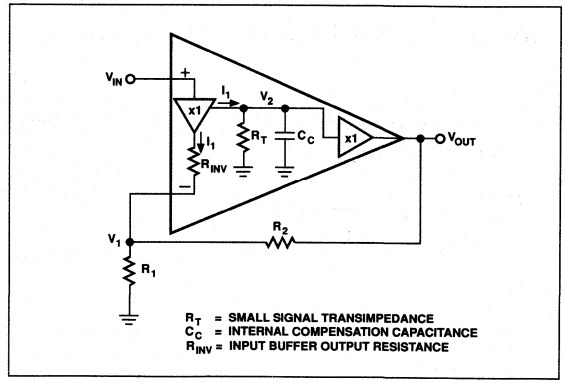


FIGURE 3: *Simple frequency response model of the current feedback amplifier.*

The model shown in Figure 3 can be used to determine the frequency response of a current feedback amplifier. With this model, the frequency response dependency on the value of the feedback resistance is easily seen.

From the model of Figure 3, nodal equations may be written for V_1 and V_2.

$$V_1 = \frac{V_{IN}\left(\frac{R_2}{R_{INV}}\right) + V_{OUT}}{1 + \frac{R_2}{R_1} + \frac{R_2}{R_{INV}}}$$

$$V_2 = \frac{R_T}{1 + sR_TC_C} I_1$$

where $I_1 = \frac{V_{IN} - V_1}{R_{INV}} = V_1\left(\frac{1}{R_1} + \frac{1}{R_2}\right) - \frac{V_{OUT}}{R_2}$, and $V_{OUT} = V_2$.

Combining these equations yields:

$$V_{OUT} = \left[\left(\frac{V_{IN}\left(\frac{R_2}{R_{INV}}\right) + V_{OUT}}{1 + \frac{R_2}{R_1} + \frac{R_2}{R_{INV}}}\right)\left(\frac{1}{R_1} + \frac{1}{R_2}\right) - \frac{V_{OUT}}{R_2}\right] \frac{R_T}{1 + sR_TC_C}$$

If the transimpedance of the amplifier, R_T, is » R_2 and R_{INV}, then the transfer function may be simplified to:

$$\frac{V_{OUT}}{V_{IN}} \approx \frac{1 + \frac{R_2}{R_1}}{1 + s\left[R_2 + \left(1 + \frac{R_2}{R_1}\right)R_{INV}\right]C_C}$$

The transfer function shows that the dominant closed-loop pole is mainly dependent on the value of the feedback resistance, R_2, and the internal compensation capacitor, C_C. For example, at unity gain, where R_1 is infinite, R_2 determines the –3dB frequency.

$$\frac{V_{OUT}}{V_{IN}} \approx \frac{1}{1 + sR_2C_C}$$

$$f_{-3dB} = \frac{1}{2\pi R_2 C_C}$$

where $R_2 \gg R_{INV}$.

For higher gains, the –3dB frequency is determined by R_2 plus the output resistance of the buffer, R_{INV} (typically 100Ω), which is multiplied by the closed-loop gain. As the closed-loop gain increases, the multiplying effect on R_{INV} becomes dominant, causing the bandwidth to decrease. However, the closed-loop bandwidth of a current feedback amplifier still far exceeds that of a voltage feedback op amp for moderate values of gain.

Figure 4 shows the effect of the feedback resistance on the bandwidth of the OP-260 for various closed-loop gains.

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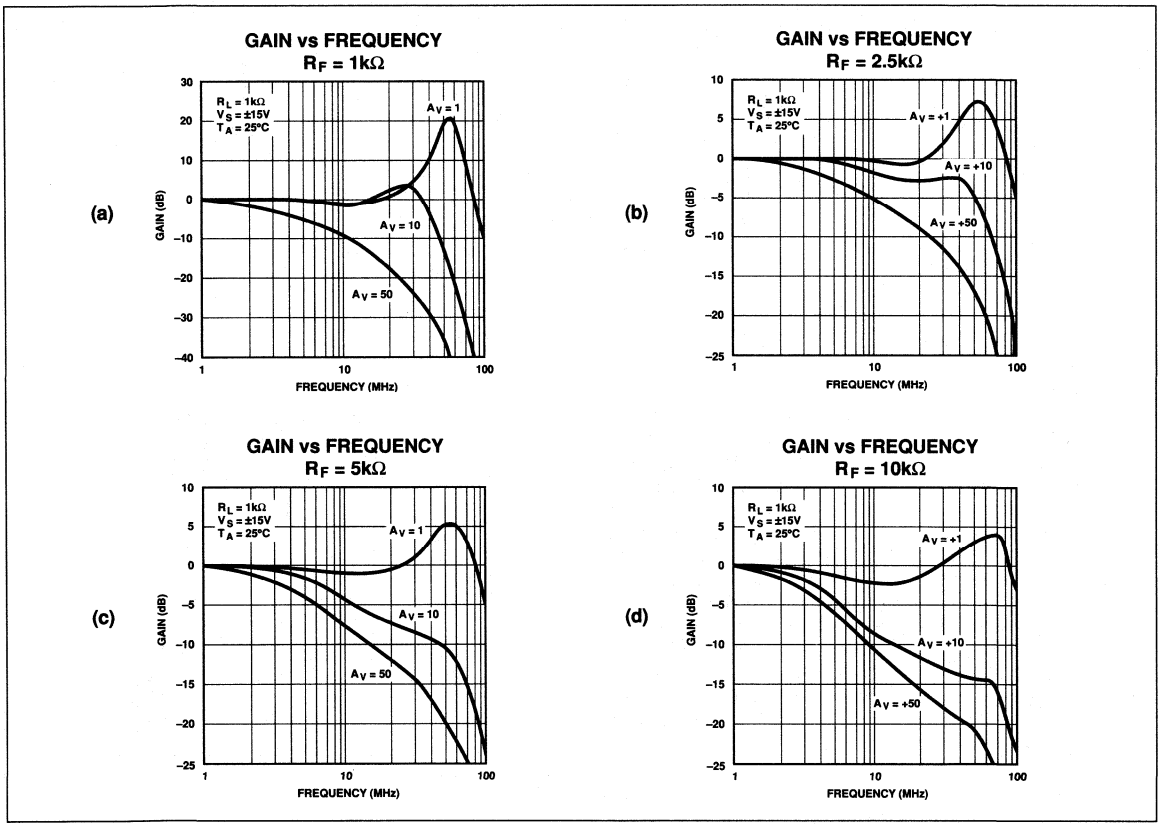

FIGURE 4: *Bandwidth will vary with feedback resistance. Peaking increases as the feedback resistance is decreased. R_F = 2.5kΩ is the recommended value. All graphs are normalized to 0dB.*

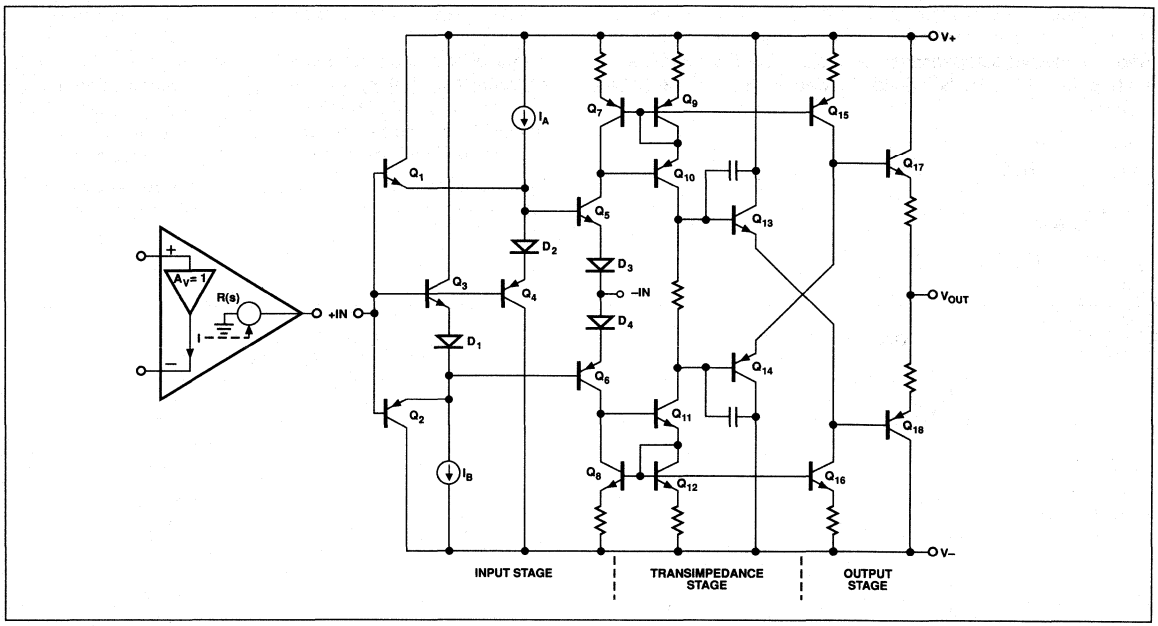

FIGURE 5: *Simplified schematic of the OP-260 showing the three stages of the amplifier.*

SLEW RATE AND GAIN

The simplified schematic in Figure 5 shows the three stages of the OP-260. The input stage consists of a unity-gain emitter-follower amplifier. Q_5 and Q_6 form a class AB output stage at the inverting input which can source or sink current. The current flowing through the inverting input is sensed by the top current mirror, formed by Q_7, Q_9, and Q_{10}, or the bottom current mirror, formed by Q_8, Q_{11}, and Q_{12}. When the buffer sources current to a load, current flows out of the inverting input, increasing Q_5's collector current and causing more current to flow through Q_9 and Q_{15}. This increases the base drive to the output transistor Q_{17}. Simultaneously, the increased current in Q_9 drives Q_{13} which reduces base drive to the complementary output transistor Q_{18}. This push-pull action produces a very fast output slew rate. For a small voltage step, the OP-260's slew rate is dependent on the available current from the two current sources (I_A and I_B) that drive Q_5 and Q_6.

To increase the slew rate, transistors Q_1 and Q_2 have been added to boost the base drive to Q_5 and Q_6. In closed-loop gains below 10, a large input step will turn on Q_1 or Q_2 increasing the slew rate dramatically as illustrated in Figure 6.

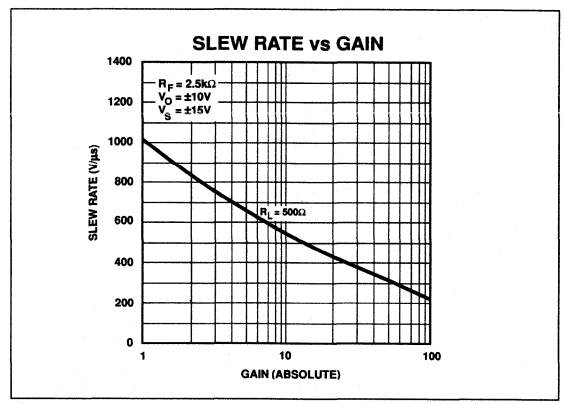

FIGURE 6: *Slew rate of the OP-260 is highest in gains below ±10.*

AMPLIFIER NOISE PERFORMANCE

Simplified noise models of the OP-260 in the noninverting and inverting amplifier configurations are shown in Figure 7. All resistors are assumed to be noiseless.

For the noninverting amplifier, the equivalent input voltage noise, referred to the input, is:

$$E_n = \sqrt{(R_S\, i_{nn})^2 + e_n^2 + \frac{(R_2\, i_{ni})^2}{(A_{VLC})^2}}$$

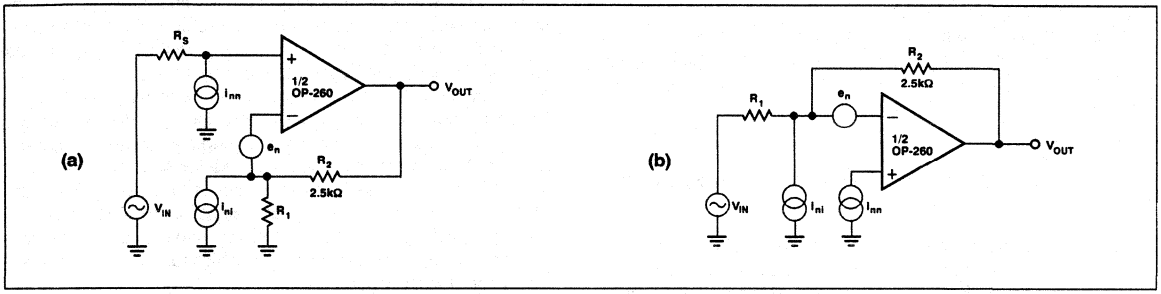

FIGURE 7: *Simplified noise models for the OP-260 in noninverting (a) and inverting (b) gain.*

where:

E_N = total input referred noise
e_n = amplifier voltage noise
i_{nn} = noninverting input current noise
i_{ni} = inverting input current noise
R_S = source resistance
A_{VCL} = closed loop gain = $1 + R_2/R_1$

For the inverting amplifier, the equivalent input voltage noise, referred to the input, is:

$$E_n = \sqrt{e_n^2 \left(\frac{1 + |A_{VLC}|}{|A_{VLC}|}\right)^2 + \frac{(R_2\, i_{ni})^2}{(|A_{VLC}|)^2}}$$

assuming $R_S \ll R_1$. A_{VCL} = closed loop gain = $-R_2/R_1$.

Typical values @ 1kHz for the noise parameters of the OP-260 are:

e_n = 5.0nV/$\sqrt{Hz}$
i_{nn} = 3.0pA/$\sqrt{Hz}$
i_{ni} = 20.0pA/$\sqrt{Hz}$

SHORT CIRCUIT PERFORMANCE

To avoid sacrificing bandwidth and slew rate performance the OP-260's output is **not** short circuit protected. Do not short the amplifier's output to ground or to the supplies. Also, the buffer output current should not exceed a value of ±20mA peak or ±7mA continuous.

POWER SUPPLY BYPASSING AND LAYOUT CONSIDERATIONS

Proper power supply bypassing is critical in all high-frequency circuit applications. For stable operation of the OP-260, the power supplies must maintain a low impedance-to-ground over an extremely wide bandwidth. This is most critical when driving a low resistance or large capacitance, since the current required to drive the load comes from the power supplies. A 10µF and 0.1µF bypass capacitor are recommended for each supply, as shown in Figure 8, and will provide adequate high-frequency bypassing in most applications. The bypass capacitors should be placed at the supply pins of the OP-260. As with all high frequency amplifiers, circuit layout is a critical factor in obtaining optimum performance from the OP-260. Proper high frequency layout reduces unwanted signal coupling in the circuit. When breadboarding a high frequency circuit, use direct point-to-point wiring, keeping all lead lengths as short as possible. Do not use wire-wrap boards or "plug-in" prototyping boards.

During PC board layout, keep all lead lengths and traces as short as possible to minimize inductance. The feedback and gain-setting resistors should be as close as possible to the inverting input to reduce stray capacitance at that point. To further reduce stray capacitance, remove the ground plane from the area around the inputs of the OP-260. Elsewhere, the use of a solid unbroken ground plane will insure a good high-frequency ground.

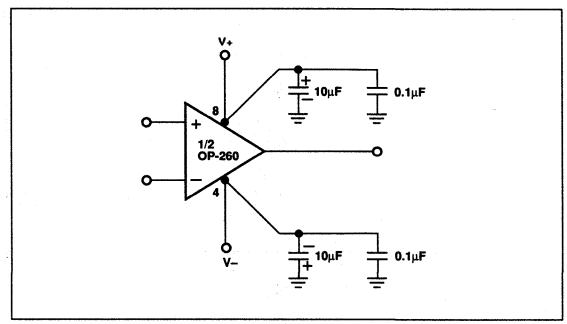

FIGURE 8: *Proper power supplying bypassing is required to obtain optimum performance with the OP-260.*

APPLICATIONS

NONINVERTING AMPLIFIER

The OP-260 can be used as a voltage-follower or noninverting amplifier as shown in Figure 9. A current feedback amplifier in this configuration yields the same transfer function as a voltage feedback op amp:

$$\frac{V_{OUT}}{V_{IN}} = 1 + \frac{R_2}{R_1}.$$

Remember to use a 2.5kΩ feedback resistor in voltage-follower application.

In noninverting applications, stray capacitance at the inverting input of a current feedback amplifier will cause peaking which will increase as the closed-loop gain decreases. The gain setting resistor, R_1, is in parallel with this stray capacitance creating a zero in the closed-loop response. For large noninverting gains, R_1 is small, creating a very high frequency open-loop pole which has limited effect on the closed-loop response. As the noninverting gain is decreased, R_1 becomes larger and the stray zero becomes lower in frequency, having a much greater effect on the closed-loop response. To reduce peaking at low noninverting gains, place a series resistor, R_C, in series with the noninverting input as shown in Figure 9. This resistor combines with the stray capacitance at the noninverting input to form a low-pass filter that will reduce the peaking. The value of R_C should be determined experimentally in the actual PCB layout. Less peaking will occur in inverting gain configurations since the inverting input is a virtual ground which forces a constant voltage across the stray capacitance.

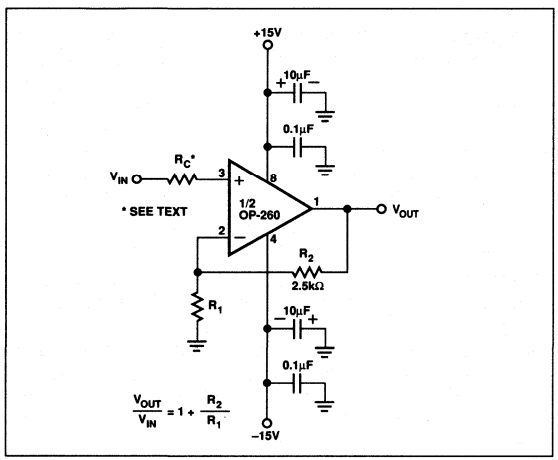

FIGURE 9: *The OP-260 as a voltage follower or noninverting amplifier.*

A common practice to stabilize voltage feedback op amps is to use a capacitor across the feedback resistance. This creates a zero in the voltage feedback amplifier response to offset the loss of phase margin due to a parasitic pole. In current feedback amplifiers, this technique will cause the amplifier to become unstable because the closed-loop bandwidth will increase beyond the stable operating frequency. For the same reason, current feedback amplifiers will not be stable in integrator applications.

INVERTING AMPLIFIER

The OP-260 is also capable of operation as an inverting amplifier (see Figure 10). The transfer function of this circuit is identical to that using a voltage feedback op amp:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_2}{R_1}.$$

An optional offset voltage trim is shown in Figure 11.

AUTOMATIC GAIN CONTROL AMPLIFIER

One of the shortcomings of using voltage feedback op amps in an Automatic-Gain-Control amplifier is that its bandwidth drops off rapidly as gain increases, limiting the useful bandwidth. However, for current feedback amplifiers, bandwidth is relatively independent of gain,

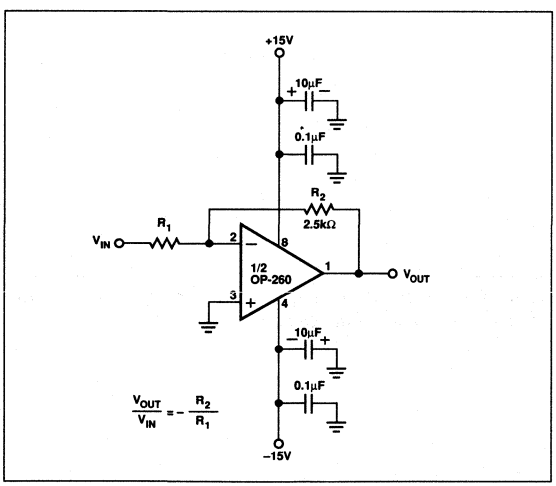

FIGURE 10: *The OP-260 as an inverting amplifier.*

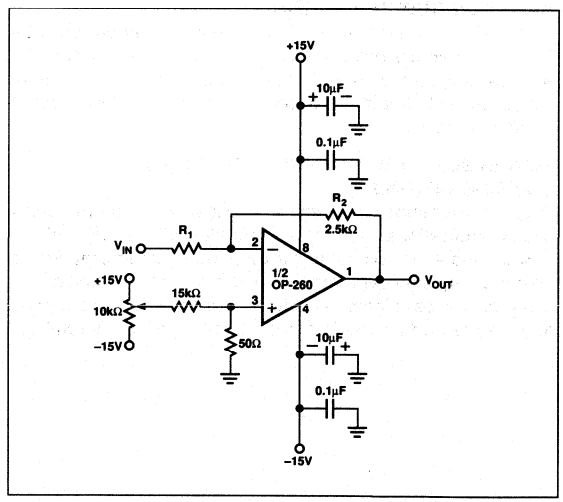

FIGURE 11: *Optional offset voltage trim circuit for the OP-260.*

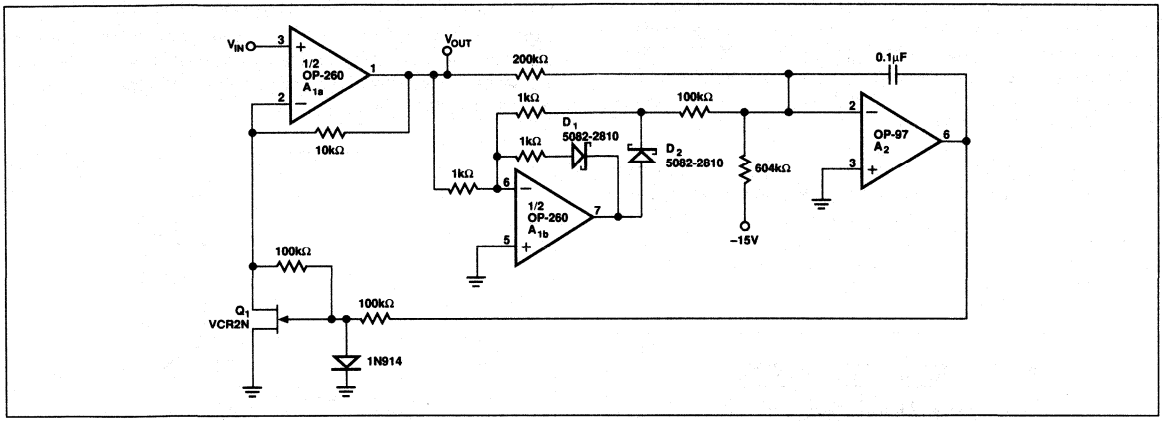

FIGURE 12: *The OP-260 eliminates the problem of variable bandwidth in AGC amplifiers using voltage feedback op amps.*

eliminating this problem. Figure 12 shows a simple AGC amplifier design using the OP-260. Amplifier A_{1a} is used as the gain stage. Its output is rectified by the second amplifier A_{1b}. If the output voltage swings more negative, diode D_2 forward biases and D_1 reverse biases, closing the loop on amplifier A_{1b}. A positive voltage appears on the anode of D_2; but, if the output voltage swings positive, D_2 reverse biases and D_1 forward biases, keeping the loop closed on A_{1b}. This prevents the amplifier from saturating to the negative rail. The result is an accurate positive rectification of the output signal.

The output of the rectifier is then compared with a reference current set up by the 604kΩ resistor which is biased to −15V. The output of the error amplifier A_2 will drive the FET (Q_1) to the proper voltage necessary to achieve a zero voltage at the inverting input of A_2. If there is insufficient signal, the error amplifier will detect an imbalance. This causes the error amp to drive more positive, turning FET Q_1 on harder, reducing the channel resistance and increasing the gain. Figure 13 shows the pulse response of the AGC amplifier. The AGC loop maintains a constant peak output amplitude for a square wave input signal range of $\pm 20mV_{p-p}$ to $\pm 6.0V_{p-p}$.

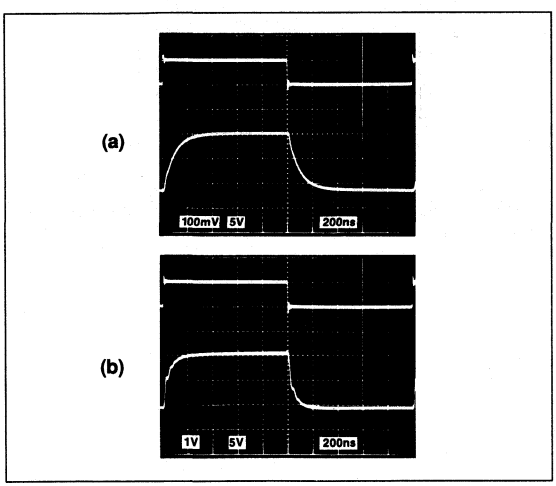

FIGURE 13: *Pulse response of the AGC amplifier at (a) low level input signal, and (b) large input signal.*

LOW PHASE ERROR AMPLIFIER

The simple amplifier depicted in Figure 14 utilizes the monolithic dual OP-260 and a few resistors to substantially reduce phase error over a wide frequency range compared to conventional amplifier

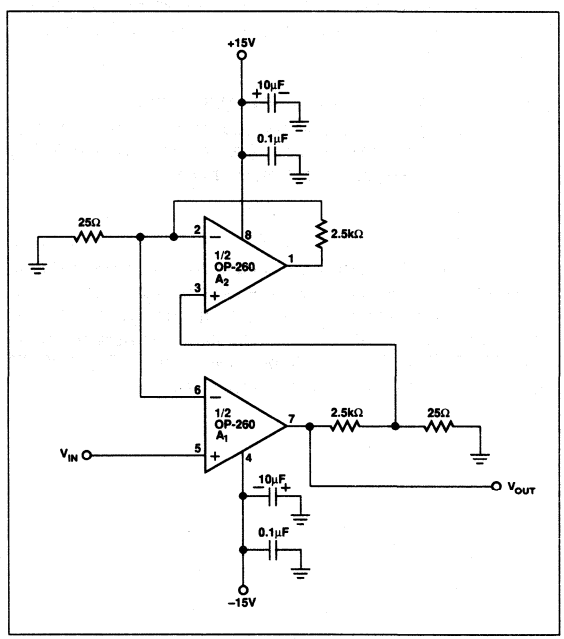

FIGURE 14: *Active feedback allows cancellation of the dominant pole, therefore reducing the phase shift significantly.*

designs. This technique relies on the matched frequency characteristics of the two current feedback amplifiers in the OP-260. Referring to the circuit, notice that each amplifier has the same feedback resistor network, corresponding to a gain of 100. Since these two amplifiers are set at equal gain and are matched due to the monolithic construction of the OP-260, they will have an identical frequency response. A pole in the feedback loop of an amplifier becomes a zero in the closed loop response. With one amplifier in the feedback loop of the other, the pole and zero are at the same frequency, thus cancelling and reducing low phase error. Figure 15 shows that the low phase error amplifier at a gain of 100 exhibits 1° of phase error up to a frequency of 1MHz. For a single voltage feedback op amp to match this performance, it would require a gain-bandwidth product exceeding 10GHz!

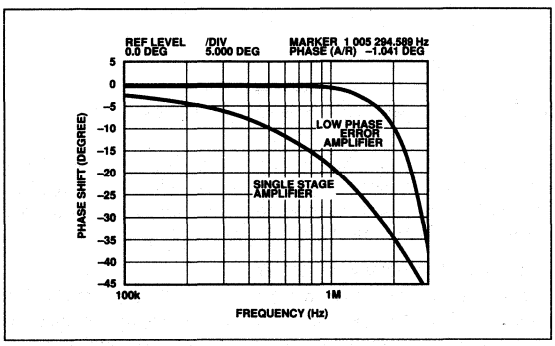

FIGURE 15: *Phase response of the ultra-low phase error amplifier compared to that of a single current feedback amplifier. Note that there is only one degree of phase error over a 1MHz bandwidth at a gain of 100.*

HIGH-SPEED INSTRUMENTATION AMPLIFIER

The circuit of Figure 16 is a high-speed instrumentation amplifier constructed with a single OP-260. Gain of the amplifier is set by resistor R_G according to the following formula:

$$\frac{V_{OUT}}{V_{IN}} = \frac{10k\Omega}{R_G} + 2.$$

The advantages of the two op amp instrumentation amplifier is that the errors in the individual amplifiers tend to cancel one another. Common-mode rejection is limited by the matching of resistors R_1 to R_4. For the best CMR performance, these resistors should be matched to 0.01% or a CMR trim can be performed on R_1. A CMRR of 90dB (measured at 60Hz) is achievable at all gains. Input offset voltage of the instrumentation amplifier is determined by the V_{IOS} matching of the OP-260, which is typically under 0.5mV.

Figure 17 shows the relationship between gain and bandwidth for the instrumentation amplifier. Reducing resistors R_1 to R_4 to 2.5kΩ increases the bandwidth but makes circuit performance more dependent on board layout.

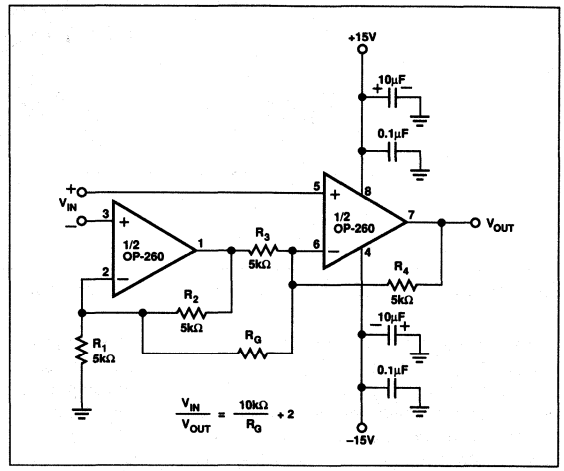

FIGURE 16: *High Speed Instrumentation Amplifier*

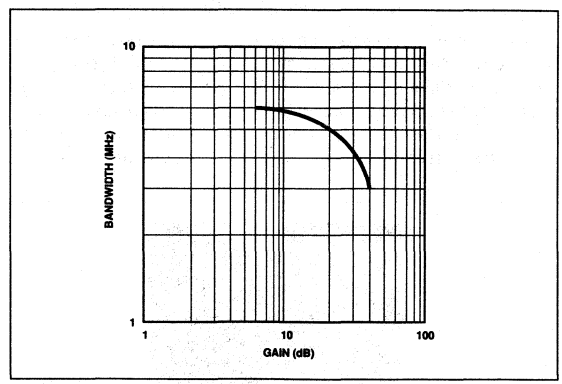

FIGURE 17: *Bandwidth versus gain for the high speed instrumentation amplifier.*

* PSpice is a registered trademark of MicroSim Corporation.
** HSpice is a tradename of Meta-Software, Inc.

OP-260 SPICE MACRO-MODEL

Figure 18 shows the SPICE macro-model for the OP-260 dual, high-speed, current feedback operational amplifier. This model was tested with, and is compatible with PSpice* and HSpice**. The schematic and net-list are included here so that the model can easily be used. This model uses a unique current feedback topology to accurately model both the AC and DC characteristics of the OP-260. In addition, this model can accommodate any number of poles and zeros to further shape the AC response.

This model consists of one of the op amps in the dual OP-260 package. To use this model as a dual, just call up the model twice and specify the same power supplies for each op amp. The OP-260 SPICE macro-model uses four BJT transistors to create the input buffer just as the actual device does. However, the rest of the model contains only ideal linear elements and ideal diodes to model the OP-260's behavior. Using only four transistors reduces simulation time and simplifies model development. It simulates important DC parameters such as V_{OS}, I_B, CMR, V_O and I_{SY}. AC parameters such as slew rate, open-loop transimpedance and phase response and CMR changes with frequency are also simulated by the model. In addition, the model includes the change in input bias current with varying common-mode and power supply voltages. Both output swing and supply current are accurately modelled.

To keep the OP-260 model as simple as possible and thus save computer and development time, not all features of the op amp were modelled as listed below:

- PSR
- Crosstalk
- Varying slew rate with closed-loop gain
- No limits on power supply voltages
- Maximum input voltage range
- Temperature effects (i.e., model parameters are assumed at 25°C)
- Input noise voltage and current sources
- Parameter variations for Monte Carlo analysis (i.e., all parameters are typical only)

These parameters are considered second-order effects and are not considered necessary for circuit simulation under normal operating conditions. However, users can easily add these functions as needed.

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* PSpice is a registered trademark of MicroSim Corporation.
** HSpice is a tradename of Meta-Software, Inc.

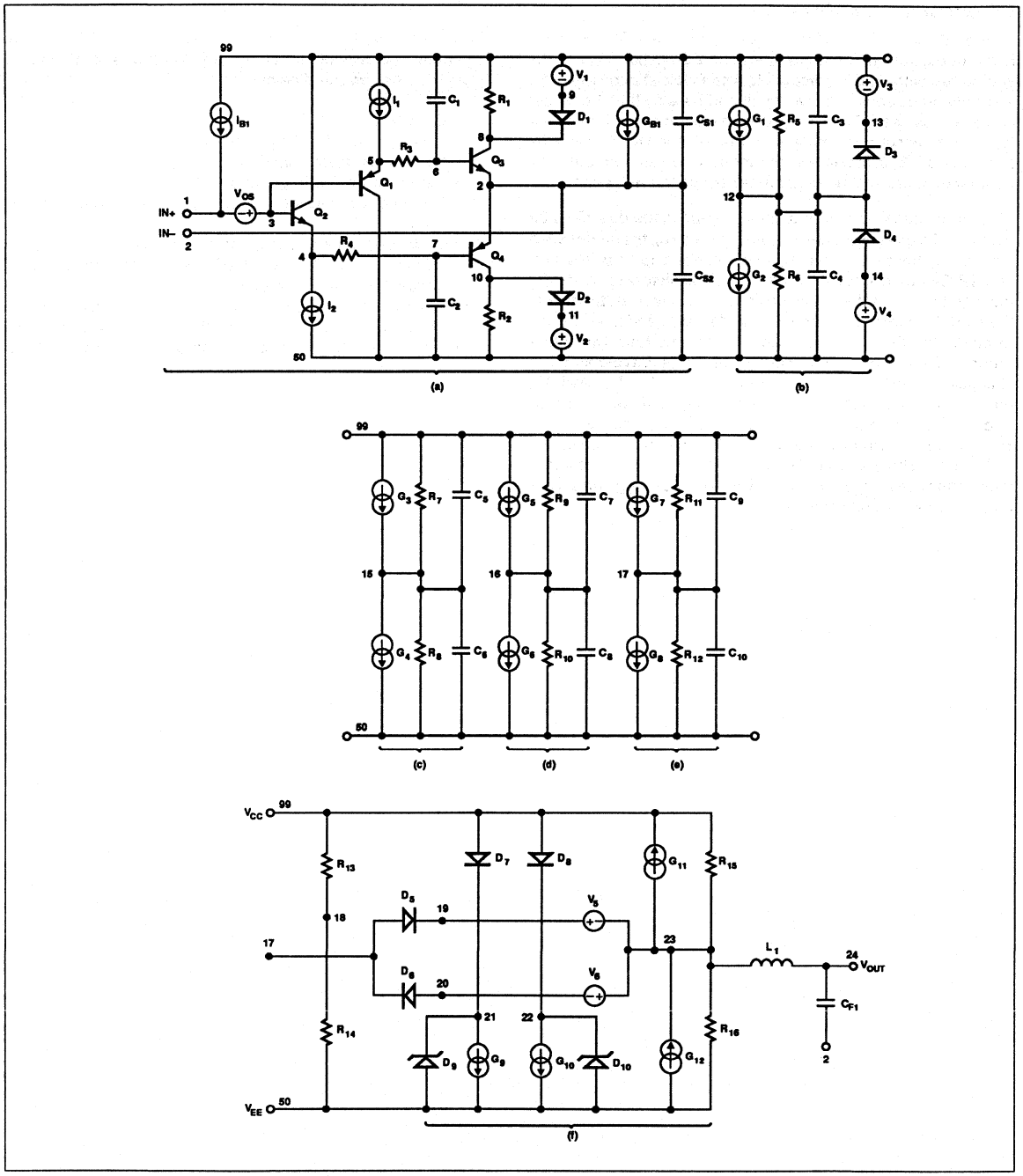


FIGURE 18: *OP-260 Macro-Model Schematic*

```
OP-260 MACRO-MODEL © PMI 1989
*
* SUBCKT OP-260 1  2 24 99 50
*
* INPUT STAGE
*
R1    99   8        4K
R2    10   50       4K
V1    99   9        1.1
D1    9    8        DX
V2    11   50       1.1
D2    10   11       DX
I1    99   5        15OU
I2    4    50       15OU
Q1    50   3    5   QP
Q2    99   3    4   QN
Q3    8    6    2   QN
Q4    10   7    2   QP
R3    5    6        14.3K
R4    4    7        14.3K
C1    99   6        0.133P
C2    50   7        0.133P
*
* INPUT ERROR SOURCES
*
GB1   99   2        POLY(1)  1  18  3E-6  4E-8
IB1   99   1        2E-7
VOS   3    1        1E-3
CS1   99   2        0.8E-12
CS2   50   2        0.8E-12
*
* GAIN STAGE & DOMINANT POLE
*
R5    12   99       10E6
R6    12   50       10E6
C3    12   99       0.6P
C4    12   50       0.6P
G1    99   12       POLY (1)  99  8   4E-3    0.25E-3
G2    12   50       POLY (1)  10  50  4E-3    0.25E-3
V3    99   13       2.2
V4    14   50       2.2
D3    12   13       DX
D4    14   12       DX
*
* POLE AT 64 MHz
*
R7    15   99       1E6
R8    15   50       1E6
C5    15   99       2.5E-15
C6    15   50       2.5E-15
G3    99   15       12  18   1E-6
G4    15   50       18  12   1E-6
*
* POLE AT 72 MHz
*
R9    16   99       1E6
R10   16   50       1E6
C7    16   99       2.2E-15
C8    16   50       2.2E-15
G5    99   16       15  18   1E-6
G6    16   50       18  15   1E-6
*
* POLE  AT 80 MHz
*
R11   17   99       1E6
R12   17   50       1E6
C9    17   99       2E-15
C10   17   50       2E-15
G7    99   17       16  18   1E-6
G8    17   50       18  16   1E-6
*
* OUTPUT STAGE
*
R13   18   99       3.333E3
R14   18   50       3.333E3
R15   23   99       150
R16   23   50       150
L1    23   24       1.5E-8
CF1   24   2        1.8P
G9    21   50       17  23   6.66667E-3
G10   22   50       23  17   6.66667E-3
G11   23   99       99  17   6.66667E-3
G12   50   23       17  50   6.66667E-3
V5    19   23       1.55
V6    23   20       1.55
D5    17   19       DX
D6    20   17       DX
D7    99   21       DX
D8    99   22       DX
D9    50   21       DY
D10   50   22       DY
*
*MODELS USED
*
.MODEL   QN  NPN (BF = 1E9   IS = 1E-15   VAF = 150)
.MODEL   QP  PNP (BF = 1E9   IS = 1E-15   VAF = 150)
.MODEL   DX  D (IS = 1E-15)
.MODEL   DY  D (IS = 1E-15    BV =50)
.ENDS OP-260
```

FIGURE 19: *OP-260 SPICE Net-List*

ANALOG DEVICES

Dual Very Low-Noise Precision Operational Amplifier

OP-270

FEATURES

- **Very Low Noise** ..... 5nV/$\sqrt{Hz}$ @ 1kHz Max
- **Excellent Input Offset Voltage** ..... 75μV Max
- **Low Offset Voltage Drift** ..... 1μV/°C Max
- **Very High Gain** ..... 1500V/mV Min
- **Outstanding CMR** ..... 106dB Min
- **Slew Rate** ..... 2.4V/μs Typ
- **Gain-Bandwidth Product** ..... 5MHz Typ
- **Industry Standard 8-Pin Dual Pinout**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (μV)	PACKAGE CERDIP 8-PIN	PLASTIC	LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
75	OP270AZ*	–	OP270ARC/883	MIL
75	OP270EZ	–	–	XIND
150	OP270FZ	–	–	XIND
250	–	OP270GP	–	XIND
250	–	OP270GS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

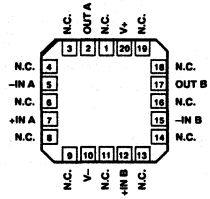
†† For availability and burn-in information on SO and PLCC packages, contact you local sales office.

GENERAL DESCRIPTION

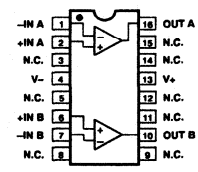
The OP-270 is a high-performance monolithic dual operational amplifier with exceptionally low voltage noise, 5nV/$\sqrt{Hz}$ at 1kHz Max, offering comparable performance to PMI's industry standard OP-27.

The OP-270 features an input offset voltage below 75μV and an offset drift under 1μV/°C, guaranteed over the full military temperature range. Open-loop gain of the OP-270 is over 1,500,000 into a 10kΩ load insuring excellent gain accuracy and linearity, even in high-gain applications. Input bias current is under 20nA which reduces errors due to signal source resistance. The OP-270's CMR of over 106dB and PSRR of less than 3.2μV/V significantly reduce errors due to

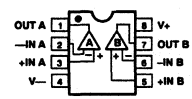
PIN CONNECTIONS



LCC
(RC-Suffix)

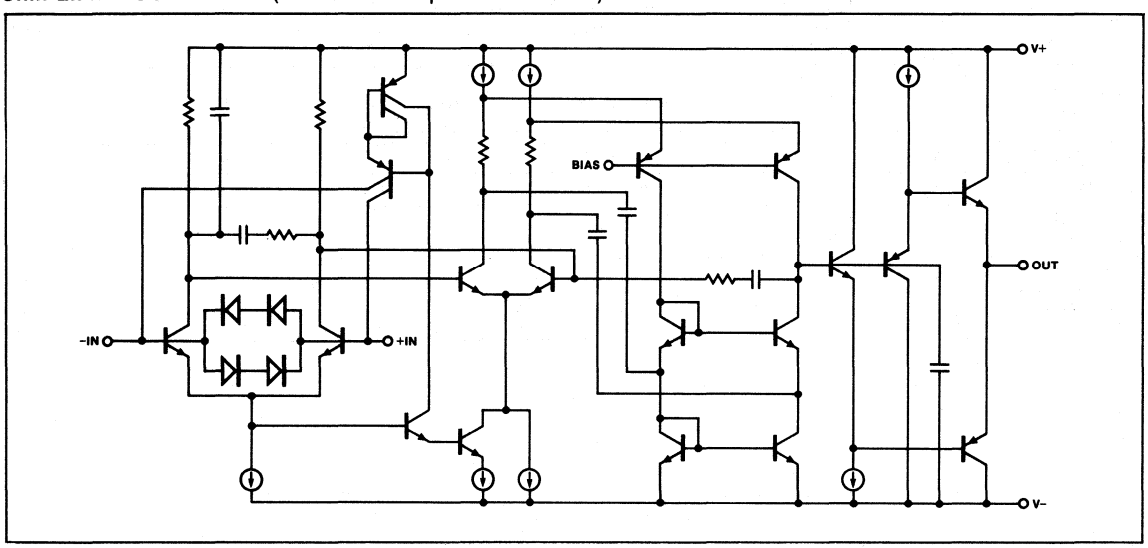


16-PIN SOL
(S-Suffix)



EPOXY MINI-DIP (P-Suffix)
8-PIN HERMETIC DIP
(Z-Suffix)

SIMPLIFIED SCHEMATIC (One of two amplifiers is shown.)



ground noise and power supply fluctuations. Power consumption of the dual OP-270 is one-third less than two OP-27s, a significant advantage for power conscious applications. The OP-270 is unity-gain stable with a gain-bandwidth product of 5MHz and a slew rate of 2.4V/μs.

The OP-270 offers excellent amplifier matching which is important for applications such as multiple gain blocks, low-noise instrumentation amplifiers, dual buffers, and low-noise active filters.

The OP-270 conforms to the industry standard 8-pin DIP pinout. It is pin compatible with the MC1458/1558, SE5532/A, RM4558 and HA5102 dual op amps and can be used to upgrade systems using these devices.

For higher speed applications the OP-271, with a slew rate of 8V/μs, is recommended. For a quad op amp, see the OP-470.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Differential Input Voltage (Note 2) ..... ±1.0V
Differential Input Current (Note 2) ..... ±25mA
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous

Storage Temperature Range
P, RC, S, Z-Package ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature (T_j) ..... –65°C to +150°C
Operating Temperature Range
OP-270A ..... –55°C to +125°C
OP-270E, OP-270F, OP-270G ..... –40°C to +85°C

PACKAGE TYPE	Θ_{JA} (Note 3)	Θ_{JC}	UNITS
8-Pin Hermetic DIP (Z)	134	12	°C/W
8-Pin Plastic DIP (P)	96	37	°C/W
20-Contact LCC (RC)	88	33	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. The OP-270's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise performance. If differential voltage exceeds ±10V, the input current should be limited to ±25mA.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

			OP-270A/E			OP-270F			OP-270G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	–	–	10	75	–	20	150	–	50	250	μV
Input Offset Current	I_{OS}	V_{CM} = 0V	–	1	10	–	3	15	–	5	20	nA
Input Bias Current	I_B	V_{CM} = 0V	–	5	20	–	10	40	–	15	60	nA
Input Noise Voltage	$e_{n\ p\text{-}p}$	0.1Hz to 10Hz (Note 1)	–	80	200	–	80	200	–	80	–	nVp-p
Input Noise Voltage Density	e_n	f_O = 10Hz	–	3.6	6.5	–	3.6	6.5	–	3.6	–	nV/√Hz
		f_O = 100Hz	–	3.2	5.5	–	3.2	5.5	–	3.2	–	
		f_O = 1kHz (Note 2)	–	3.2	5.0	–	3.2	5.0	–	3.2	–	
Input Noise Current Density	i_n	f_O = 10Hz	–	1.1	–	–	1.1	–	–	1.1	–	pA/√Hz
		f_O = 100Hz	–	0.7	–	–	0.7	–	–	0.7	–	
		f_O = 1kHz	–	0.6	–	–	0.6	–	–	0.6		
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V										V/mV
		R_L = 10kΩ	1500	2300	–	1000	1700	–	750	1500	–	
		R_L = 2kΩ	750	1200	–	500	900	–	350	700	–	
Input Voltage Range	IVR	(Note 3)	±12	±12.5	–	±12	±12.5	–	±12	±12.5	–	V
Output Voltage Swing	V_O	R_L ≥ 2kΩ	±12	±13.5	–	±12	±13.5	–	±12	±13.5	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	106	125	–	100	120	–	90	110	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	–	0.56	3.2	–	1.0	5.6	–	1.5	6	μV/V
Slew Rate	SR		1.7	2.4	–	1.7	2.4	–	1.7	2.4	–	V/μs

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $T_A = +25°C$, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	OP-270A/E MIN	OP-270A/E TYP	OP-270A/E MAX	OP-270F MIN	OP-270F TYP	OP-270F MAX	OP-270G MIN	OP-270G TYP	OP-270G MAX	UNITS
Supply Current (All Amplifiers)	I_{SY}	No Load	–	4	6.5	–	4	6.5	–	4	6.5	mA
Gain Bandwidth Product	GBW		–	5	–	–	5	–	–	5	–	MHz
Channel Separation	CS	$V_O = 20V_{p-p}$ $f_O = 10Hz$ (Note 1)	125	175	–	125	175	–	–	175	–	dB
Input Capacitance	C_{IN}		–	3	–	–	3	–	–	3	–	pF
Input Resistance Differential-Mode	R_{IN}		–	0.4	–	–	0.4	–	–	0.4	–	MΩ
Input Resistance Common-Mode	R_{INCM}		–	20	–	–	20	–	–	20	–	GΩ
Settling Time	t_s	$A_V = +1$, 10V Step to 0.01%	–	5	–	–	5	–	–	5	–	μs

NOTES:
1. Guaranteed by not 100% tested.
2. Sample tested.
3. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $-55°C \le T_A \le +125°C$ for OP-270A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-270A MIN	OP-270A TYP	OP-270A MAX	UNITS
Input Offset Voltage	V_{OS}		–	30	175	μV
Average Input Offset Voltage Drift	TCV_{OS}		–	0.2	1	μV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	–	2	30	nA
Input Bias Current	I_B	$V_{CM} = 0V$	–	6	60	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	750 400	1600 800	– –	V/mV
Input Voltage Range	IVR	(Note 1)	±12	±12.5	–	V
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12	±13	–	V
Common-Mode Rejection	CMR	$V_{CM} = \pm11V$	100	120	–	dB
Power Supply Rejection Ration	PSRR	$V_S = \pm4.5V$ to ±18V	–	1.0	5.6	μV/V
Supply Current (All Amplifiers)	I_{SY}	No Load	–	4.5	7.5	mA

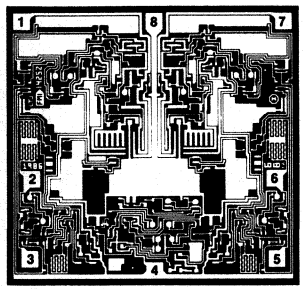
NOTE:
1. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-40°C \le T_A \le +85°C$, unless otherwise noted.

			OP-270E			OP-270F			OP-270G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}		–	25	150	–	45	275	–	100	400	µV
Average Input Offset Voltage Drift	TCV_{OS}		–	0.2	1	–	0.4	2	–	0.7	3	µV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	–	1.5	30	–	5	40	–	15	50	nA
Input Bias Current	I_B	$V_{CM} = 0V$	–	6	60	–	15	70	–	19	80	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	 1000 500	 1800 900	 – –	 600 300	 1400 700	 – –	 400 225	 1250 670	 – –	V/mV
Input Voltage Range	IVR	(Note 1)	±12	±12.5	–	±12	±12.5	–	±12	±12.5	–	V
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12	±13	–	±12	±13	–	±12	±13	–	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	100	120	–	94	115	–	90	100	–	dB
Power Supply Rejection Ration	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	–	0.7	5.6	–	1.8	10	–	2.0	15	µV/V
Supply Current (All Amplifiers)	I_{SY}	No Load	–	4.4	7.2	–	4.4	7.2	–	4.4	7.2	mA

NOTE:
1. Guaranteed by CMR test.

DICE CHARACTERISTICS



DIE SIZE 0.094 × 0.092 inch, 8,648 sq. mils
(2.39 × 2.34 mm, 5.60 sq. mm)

1. OUT A
2. −IN A
3. +IN A
4. V−
5. +IN B
6. −IN B
7. OUT B
8. V+

Substrate is internally connected to V−.

2

WAFER TEST LIMITS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-270G LIMIT	TYP
Input Offset Voltage	V_{OS}		150	µV MAX
Input Offset Current	I_{OS}	V_{CM} = 0V	15	nA MAX
Input Bias Current	I_B	V_{CM} = 0V	40	nA MAX
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V R_L = 2kΩ	500	V/mV MIN
Input Voltage Range	IVR	(Note 1)	±12	V MIN
Output Voltage Swing	V_O	R_L ≥ 2kΩ	±12	V MIN
Common-Mode Rejection	CMR	V_{CM} = ±12V	100	dB MIN
Power Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	5.6	µV/V MAX
Supply Current (All Amplifiers)	I_{SY}	No Load	6.5	mA MAX

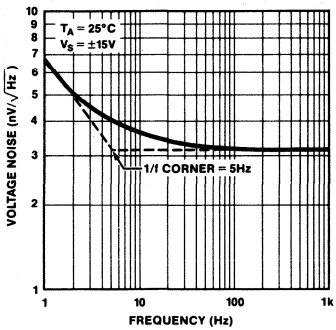
NOTE:
1. Guaranteed by CMR test.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yields loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

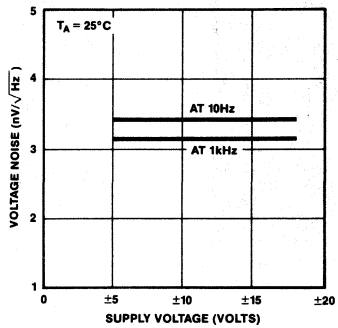
OP-270

TYPICAL PERFORMANCE CHARACTERISTICS

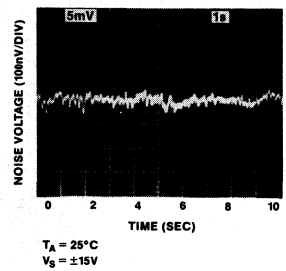
VOLTAGE NOISE DENSITY vs FREQUENCY



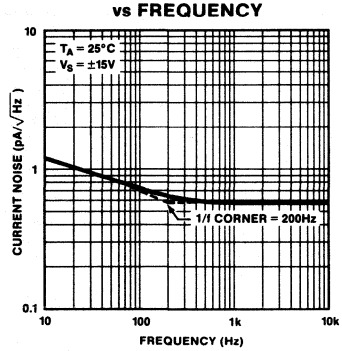
VOLTAGE NOISE DENSITY vs SUPPLY VOLTAGE



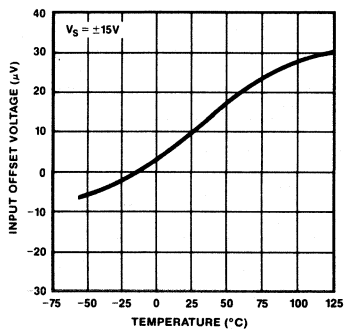
0.1Hz TO 10Hz NOISE



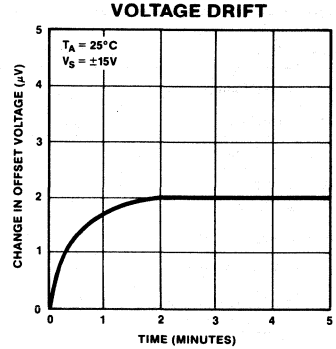
CURRENT NOISE DENSITY vs FREQUENCY



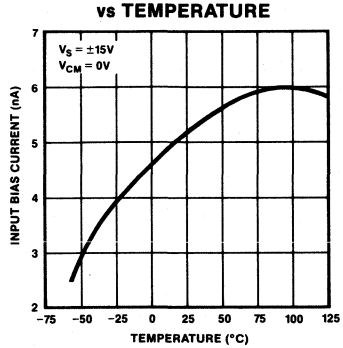
INPUT OFFSET VOLTAGE vs TEMPERATURE



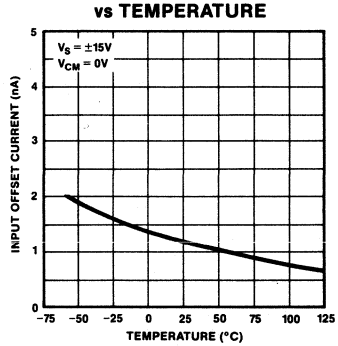
WARM-UP OFFSET VOLTAGE DRIFT



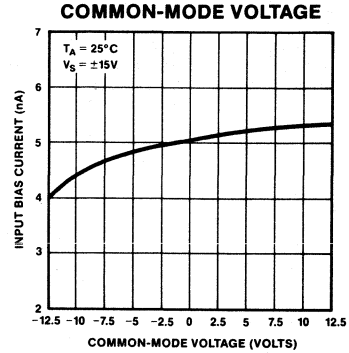
INPUT BIAS CURRENT vs TEMPERATURE



INPUT OFFSET CURRENT vs TEMPERATURE

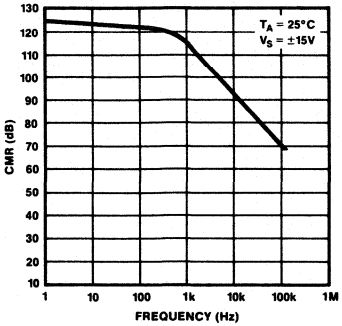


INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

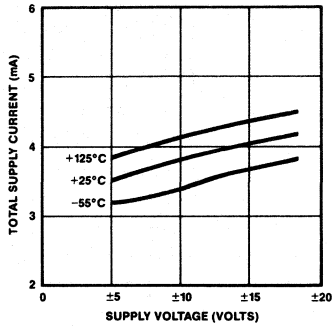


TYPICAL PERFORMANCE CHARACTERISTICS

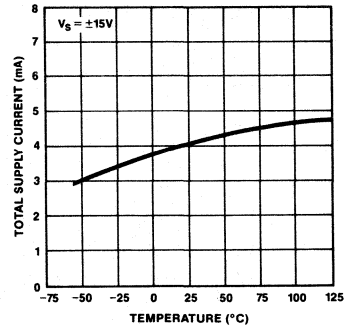
CMR vs FREQUENCY



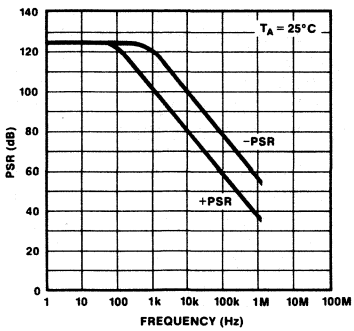
TOTAL SUPPLY CURRENT vs SUPPLY VOLTAGE



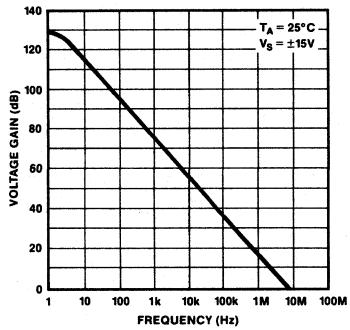
TOTAL SUPPLY CURRENT vs TEMPERATURE



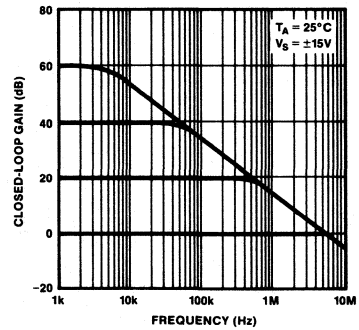
PSR vs FREQUENCY



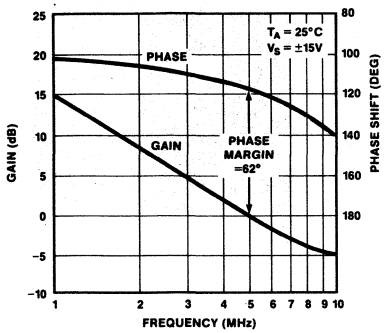
OPEN-LOOP GAIN vs FREQUENCY



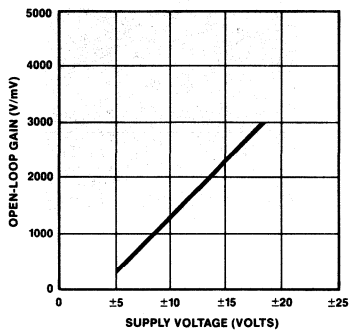
CLOSED-LOOP GAIN vs FREQUENCY



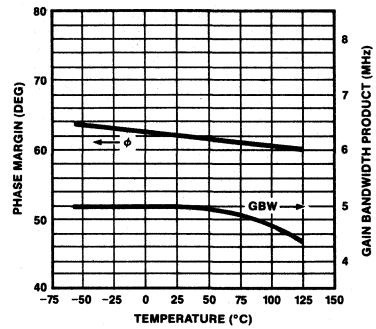
OPEN-LOOP GAIN, PHASE SHIFT vs FREQUENCY



OPEN-LOOP GAIN vs SUPPLY VOLTAGE



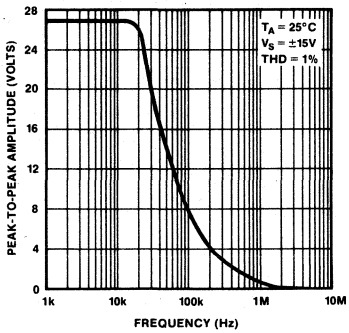
GAIN-BANDWIDTH, PHASE MARGIN vs TEMPERATURE



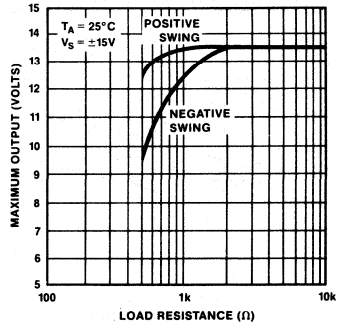
OP-270

TYPICAL PERFORMANCE CHARACTERISTICS

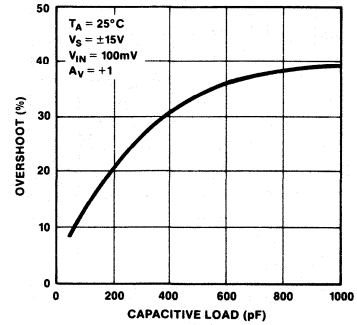
MAXIMUM OUTPUT SWING vs FREQUENCY



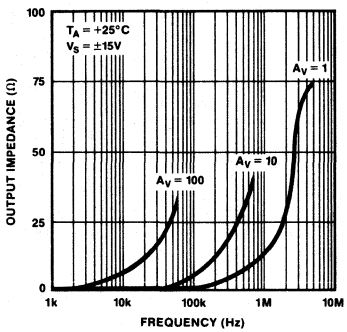
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



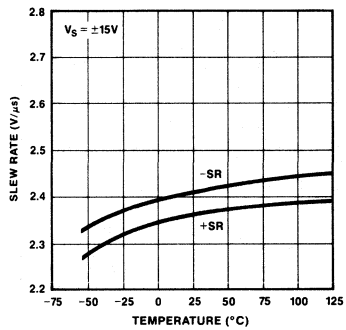
SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD



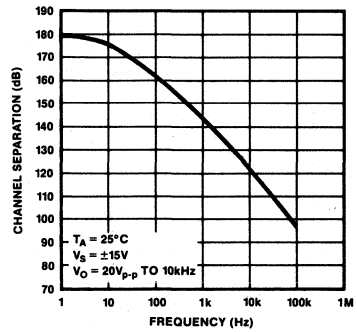
OUTPUT IMPEDANCE vs FREQUENCY



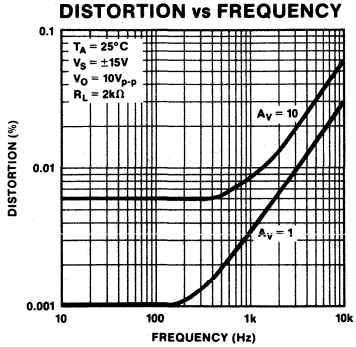
SLEW RATE vs TEMPERATURE



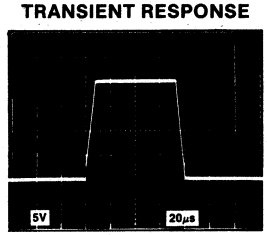
CHANNEL SEPARATION vs FREQUENCY



TOTAL HARMONIC DISTORTION vs FREQUENCY

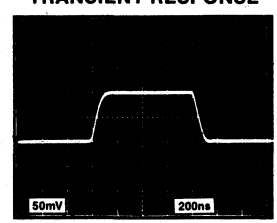


LARGE-SIGNAL TRANSIENT RESPONSE



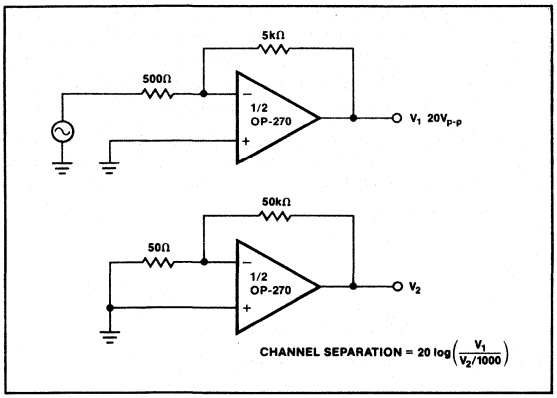
T_A = 25°C
V_S = ±15V
A_V = +1
R_L = 2kΩ

SMALL-SIGNAL TRANSIENT RESPONSE

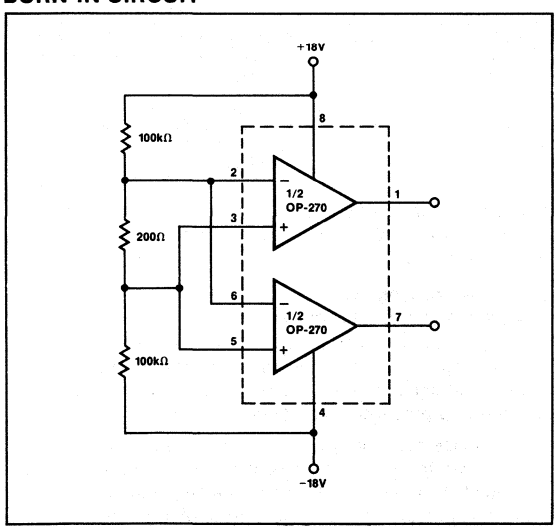


T_A = 25°C
V_S = ±15V
A_V = +1
R_L = 2kΩ

CHANNEL SEPARATION TEST CIRCUIT



BURN-IN CIRCUIT



APPLICATIONS INFORMATION

VOLTAGE AND CURRENT NOISE

The OP-270 is a very low-noise dual op amp, exhibiting a typical voltage noise of only 3.2nV/$\sqrt{Hz}$ @ 1kHz. The exceptionally low noise characteristics of the OP-270 is in part achieved by operating the input transistors at high collector currents since the voltage noise is inversely proportional to the square root of the collector current. Current noise, however, is directly proportional to the square root of the collector current. As a result, the outstanding voltage noise performance of the OP-270 is gained at the expense of current noise performance, which is normal for low noise amplifiers.

To obtain the best noise performance in a circuit it is vital to understand the relationship between voltage noise (e_n), current noise (i_n), and resistor noise (e_t).

TOTAL NOISE AND SOURCE RESISTANCE

The total noise of an op amp can be calculated by:

$$E_n = \sqrt{(e_n)^2 + (i_n R_S)^2 + (e_t)^2}$$

where:

E_n = total input referred noise

e_n = op amp voltage noise

i_n = op amp current noise

e_t = source resistance thermal noise

R_S = source resistance

The total noise is referred to the input and at the output would be amplified by the circuit gain.

Figure 1 shows the relationship between total noise at 1kHz and source resistance. For $R_S < 1k\Omega$ the total noise is dominated by the voltage noise of the OP-270. As R_S rises above 1kΩ, total noise increases and is dominated by resistor noise rather than by voltage or current noise of the OP-270. When R_S exceeds 20kΩ, current noise of the OP-270 becomes the major contributor to total noise.

FIGURE 1: Total Noise vs Source Resistance (Including Resistor Noise) at 1kHz

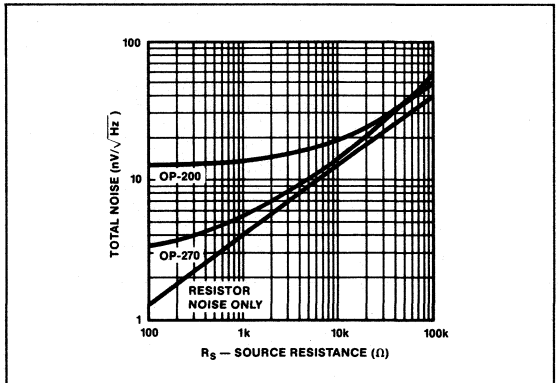


Figure 2 also shows the relationship between total noise and source resistance, but at 10Hz. Total noise increases more quickly than shown in Figure 1 because current noise is inversely proportional to the square root of frequency. In Figure 2, current noise of the OP-270 dominates the total noise when $R_S > 5k\Omega$.

From Figures 1 and 2 it can be seen that to reduce total noise, source resistance must be kept to a minimum. In applications with a high source resistance, the OP-200, with lower current noise than the OP-270, will provide lower total noise.

FIGURE 2: Total Noise vs Source Resistance (Including Resistor Noise) at 10Hz

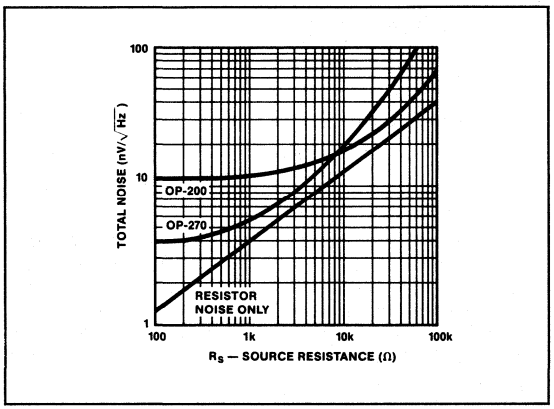


FIGURE 3: Peak-To-Peak Noise (0.1Hz To 10Hz) vs Source Resistance (Includes Resistor Noise)

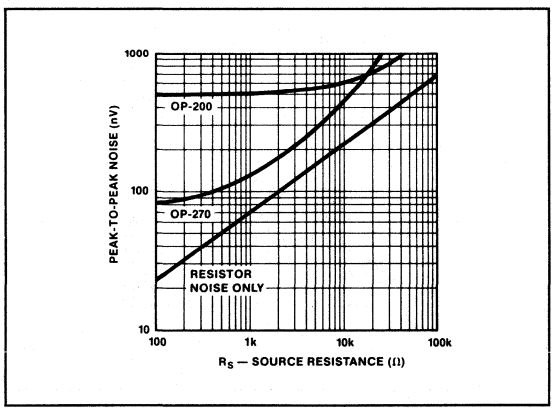


Figure 3 shows peak-to-peak noise versus source resistance over the 0.1Hz to 10Hz range. Once again, at low values of R_S, the voltage noise of the OP-270 is the major contributor to peak-to-peak noise with current noise the major contributor as R_S increases. The crossover point between the OP-270 and the OP-200 for peak-to-peak noise is at $R_S = 17k\Omega$.

The OP-271 is a higher speed version of the OP-270, with a slew rate of $8V/\mu s$. Noise of the OP-271 is slightly higher than the OP-270. Like the OP-270, the OP-271 is unity-gain stable.

For reference, typical source resistances of some signal sources are listed in Table 1.

TABLE 1

DEVICE	SOURCE IMPEDANCE	COMMENTS
Strain gauge	<500Ω	Typically used in low-frequency applications.
Magnetic tapehead, microphone	<1500Ω	Low I_B very important to reduce self-magnetization problems when direct coupling is used. OP-270 I_B can be neglected.
Magnetic phonograph cartridge	<1500Ω	Similar need for low I_B in direct coupled applications. OP-270 will not introduce any self-magnetization problem.
Linear variable differential transformer	<1500Ω	Used in rugged servo-feedback applications. Bandwidth of interest is 400Hz to 5kHz.

For further information regarding noise calculations, see "Minimization of Noise in Op-Amp Applications", Application Note AN-15.

NOISE MEASUREMENTS — PEAK-TO-PEAK VOLTAGE NOISE

The circuit of Figure 4 is a test setup for measuring peak-to-peak voltage noise. To measure the 200nV peak-to-peak noise specification of the OP-270 in the 0.1Hz to 10Hz range, the following precautions must be observed:

1. The device has to be warmed-up for at least five minutes. As shown in the warm-up drift curve, the offset voltage typically changes $2\mu V$ due to increasing chip temperature after power-up. In the 10-second measurement interval, these temperature-induced effects can exceed tens-of-nanovolts.
2. For similar reasons, the device has to be well-shielded from air currents. Shielding also minimizes thermocouple effects.
3. Sudden motion in the vicinity of the device can also "feed-through" to increase the observed noise.
4. The test time to measure 0.1Hz-to-10Hz noise should not exceed 10 seconds. As shown in the noise-tester frequency-response curve of Figure 5, the 0.1Hz corner is defined by only one pole. The test time of 10 seconds acts

FIGURE 4: Peak-To-Peak Voltage Noise Test Circuit (0.1Hz To 10Hz)

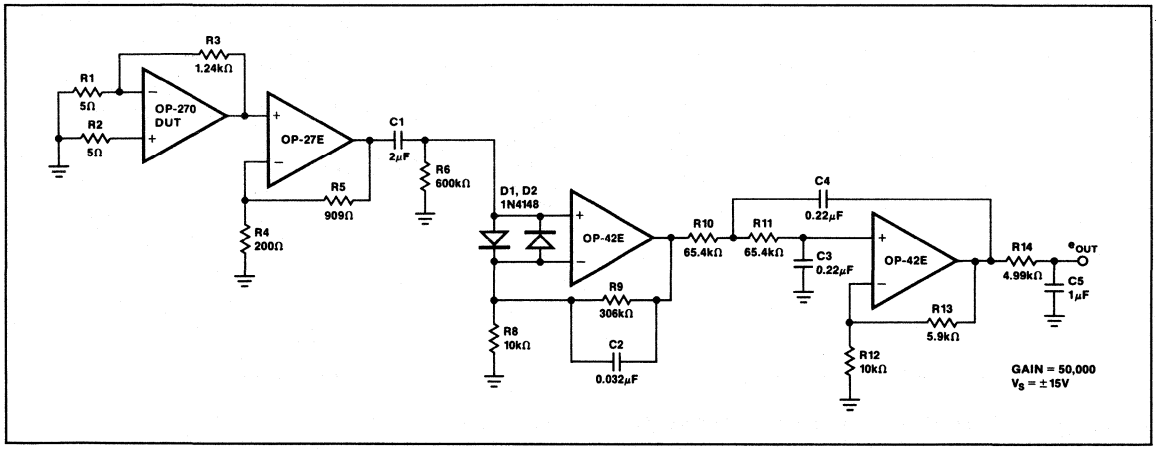
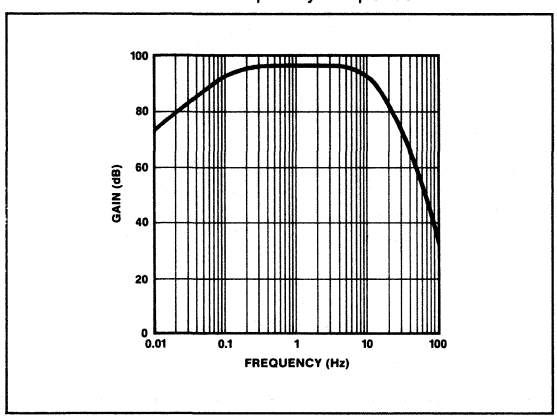


FIGURE 5: 0.1Hz To 10Hz Peak-To-Peak Voltage Noise Test Circuit Frequency Response



as an additional pole to eliminate noise contribution from the frequency band below 0.1Hz.

5. A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage-density measurement will correlate well with a 0.1Hz-to-10Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the 1/f corner frequency.
6. Power should be supplied to the test circuit by well bypassed low-noise supplies, e.g. batteries. These will minimize output noise introduced via the amplifier supply pins.

NOISE MEASUREMENT — NOISE VOLTAGE DENSITY

The circuit of Figure 6 shows a quick and reliable method of measuring the noise voltage density of dual op amps. The first amplifier is in unity-gain, with the final amplifier in a noninverting gain of 101. Since the ac noise voltages of each amplifier are uncorrelated, they add in rms fashion to yield:

$$e_{OUT} = 101 \left(\sqrt{e_{nA}^2 + e_{nB}^2} \right)$$

The OP-270 is a monolithic device with two identical amplifiers. The noise voltage density of each individual amplifier will match, giving:

$$e_{OUT} = 101 \left(\sqrt{2e_n^2} \right) = 101 \left(\sqrt{2}e_n \right)$$

FIGURE 6: Noise Voltage Density Test Circuit

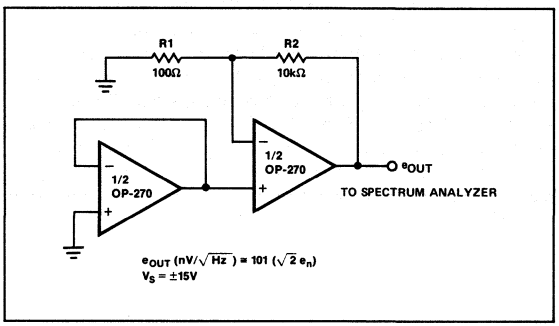
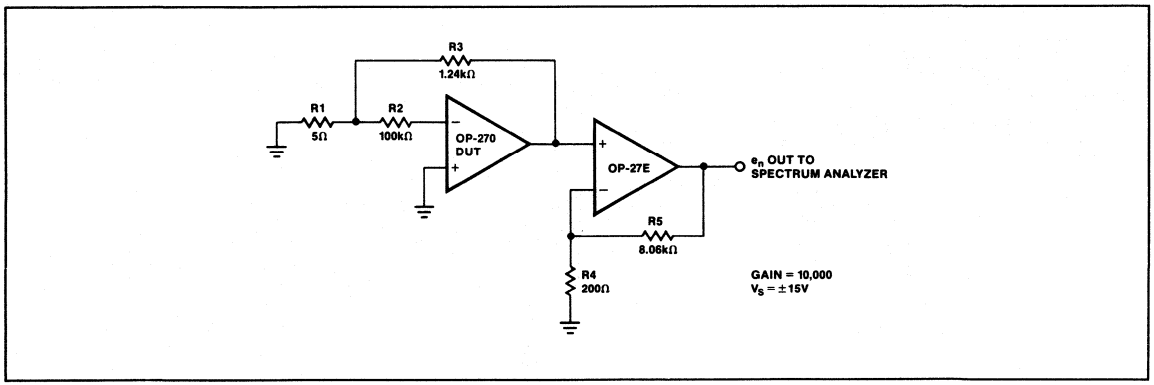


FIGURE 7: Current Noise Density Test Circuit



NOISE MEASUREMENT — CURRENT NOISE DENSITY

The test circuit shown in Figure 7 can be used to measure current noise density. The formula relating the voltage output to current noise density is:

$$i_n = \frac{\sqrt{\left(\frac{e_{nOUT}}{G}\right)^2 - \left(40nV/\sqrt{Hz}\right)^2}}{R_S}$$

where:

G = gain of 10000

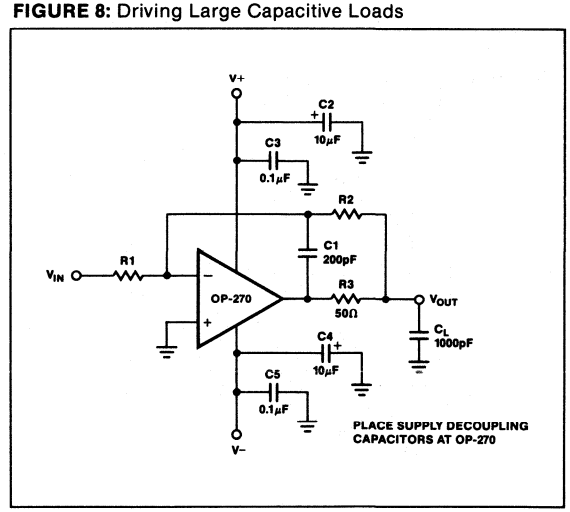
R_S = 100kΩ source resistance

CAPACITIVE LOAD DRIVING AND POWER SUPPLY CONSIDERATIONS

The OP-270 is unity-gain stable and is capable of driving large capacitive loads without oscillating. Nonetheless, good supply bypassing is highly recommended. Proper supply bypassing reduces problems caused by supply line noise and improves the capacitive load driving capability of the OP-270.

In the standard feedback amplifier, the op amp's output resistance combines with the load capacitance to form a low-pass filter that adds phase shift in the feedback network and reduces stability. A simple circuit to eliminate this effect is shown in Figure 8. The added components, C1 and R3, decouple the amplifier from the load capacitance and provide additional stability. The values of C1 and R3 shown in Figure 8 are for a load capacitance of up to 1000pF when used with the OP-270.

FIGURE 8: Driving Large Capacitive Loads



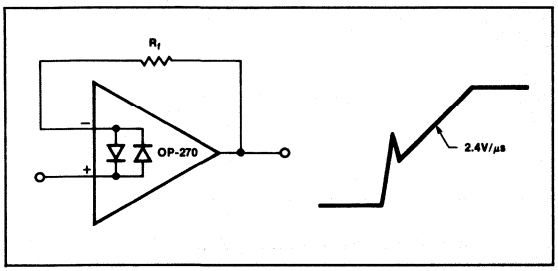
UNITY-GAIN BUFFER APPLICATIONS

When $R_f \leq 100\Omega$ and the input is driven with a fast, large-signal pulse (>1V), the output waveform will look as shown in Figure 9.

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input, and a current, limited only by the output short-circuit protection, will be drawn by the signal generator. With $R_f \geq 500\Omega$, the output is capable of handling the current requirements ($I_L \leq 20mA$ at 10V); the amplifier will stay in its active mode and a smooth transition will occur.

When $R_f > 3k\Omega$, a pole created by R_f and the amplifier's input capacitance (3pF) creates additional phase shift and reduces phase margin. A small capacitor (20 to 50pF) in parallel with R_f helps eliminate this problem.

FIGURE 9: Pulsed Operation



APPLICATIONS

LOW PHASE ERROR AMPLIFIER

The simple amplifier depicted in Figure 10 utilizes a monolithic dual operational amplifier and a few resistors to substantially reduce phase error compared to conventional amplifier designs. At a given gain, the frequency range for a specified phase accuracy is over a decade greater than for a standard single op amp amplifier.

The low phase error amplifier performs second-order frequency compensation through the response of op amp A2 in the feedback loop of A1. Both op amps must be extremely well matched in frequency response. At low frequencies, the A1 feedback loop forces $V_2/(K1 + 1) = V_{IN}$. The A2 feedback loop forces $V_O/(K1 + 1) = V_2/(K1 + 1)$ yielding an overall transfer function of $V_O/V_{IN} = K1 + 1$. The DC gain is determined by the resistor divider at the output, V_O, and is not directly affected by the resistor divider around A2. Note, that like a conventional single op amp amplifier, the DC gain is set by resistor ratios only. Minimum gain for the low phase error amplifier is 10.

FIGURE 10: Low Phase Error Amplifier

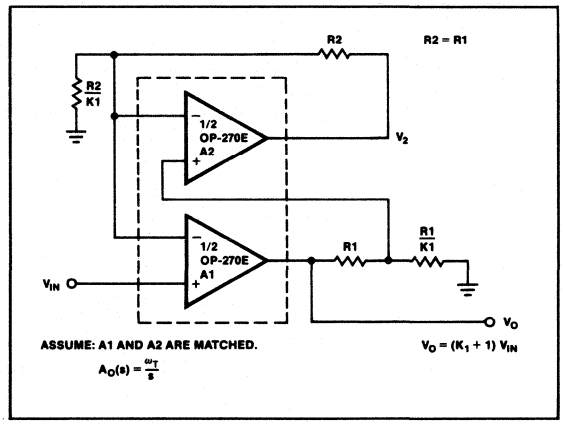


Figure 11 compares the phase error performance of the low phase error amplifier with a conventional single op amp amplifier and a cascaded two-stage amplifier. The low phase error amplifier shows a much lower phase error, particularly for frequencies where $\omega/\beta\omega_T < 0.1$. For example, phase error of −0.1° occurs at $0.002\ \omega/\beta\omega_T$ for the single op amp amplifier, but at $0.11\ \omega/\beta\omega_T$ for the low phase error amplifier.

For more detailed information on the low phase error amplifier, see Application Note AN-107.

FIGURE 11: Phase Error Comparison

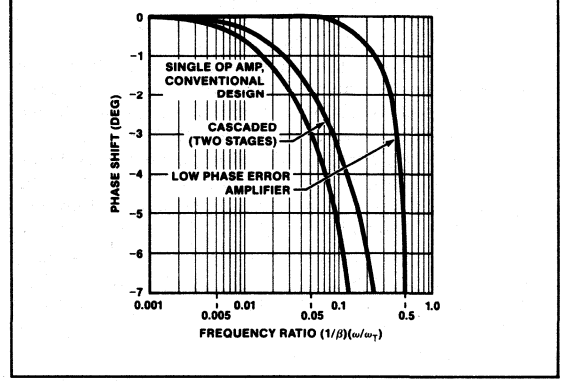
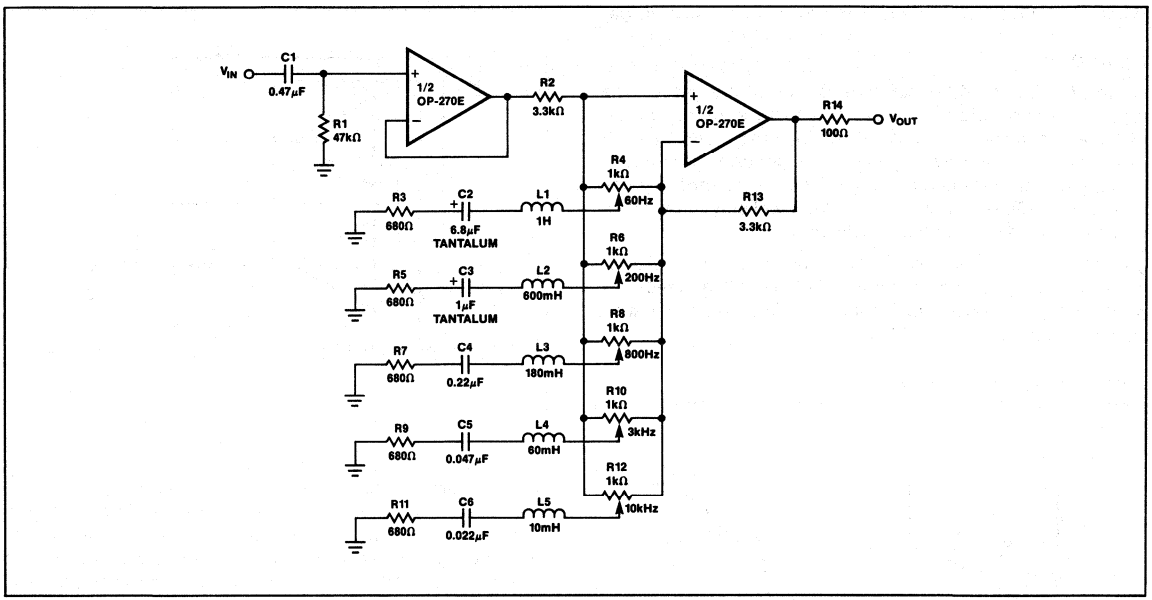


FIGURE 12: 5-Band Low Noise Graphic Equalizer



FIVE-BAND LOW NOISE STEREO GRAPHIC EQUALIZER

The graphic equalizer circuit shown in Figure 12 provides 15dB of boost or cut over a 5-band range. Signal-to-noise ratio over a 20kHz bandwidth is better than 100dB referred to a 3V rms input. Larger inductors can be replaced by active inductors but this reduces the signal-to-noise ratio.

DIGITAL PANNING CONTROL

Figure 13 uses a DAC-8221, a dual 12-bit CMOS DAC, to pan a signal between two channels. One channel is formed by the current output of DAC A driving one-half of an OP-270 in a current-to-voltage converter configuration. The other channel is formed by the complementary output current of DAC A which normally flows to ground though the AGND pin. This complementary current is converted to a voltage by the other half of the OP-270 which also holds AGND at virtual ground.

Gain error due to mismatching between the internal DAC ladder resistors and the current-to-voltage feedback resistors is eliminated by using feedback resistors internal to the DAC-8221. Only DAC A passes a signal; DAC B provides the second feedback resistor. With $V_{REF}B$ unconnected, the current-to-voltage converter, using $R_{FB}B$, is accurate and not influenced by digital data reaching DAC B. Distortion of the digital panning control is less than 0.002% over the 20Hz-20kHz audio range. Figure 14 shows the complementary outputs for a 1kHz input signal and a digital ramp applied to the DAC data input.

DUAL PROGRAMMABLE GAIN AMPLIFIER

The dual OP-270 and the DAC-8221, a dual 12-bit CMOS DAC, can be combined to form a space-saving dual programmable amplifier. The digital code present at the DAC, which is easily set by a microprocessor, determines the ratio between the internal feedback resistor and the resistance the DAC ladder presents to the op amp feedback loop. Gain of each amplifier is:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{4096}{n}$$

where n equals the decimal equivalent of the 12-bit digital code present at the DAC. If the digital code present at the DAC consists of all zeros, the feedback loop will open causing the op amp output to saturate. A 20MΩ resistor placed in parallel with the DAC feedback loop eliminates this problem with only a very small reduction in gain accuracy.

FIGURE 13: Digital Panning Control

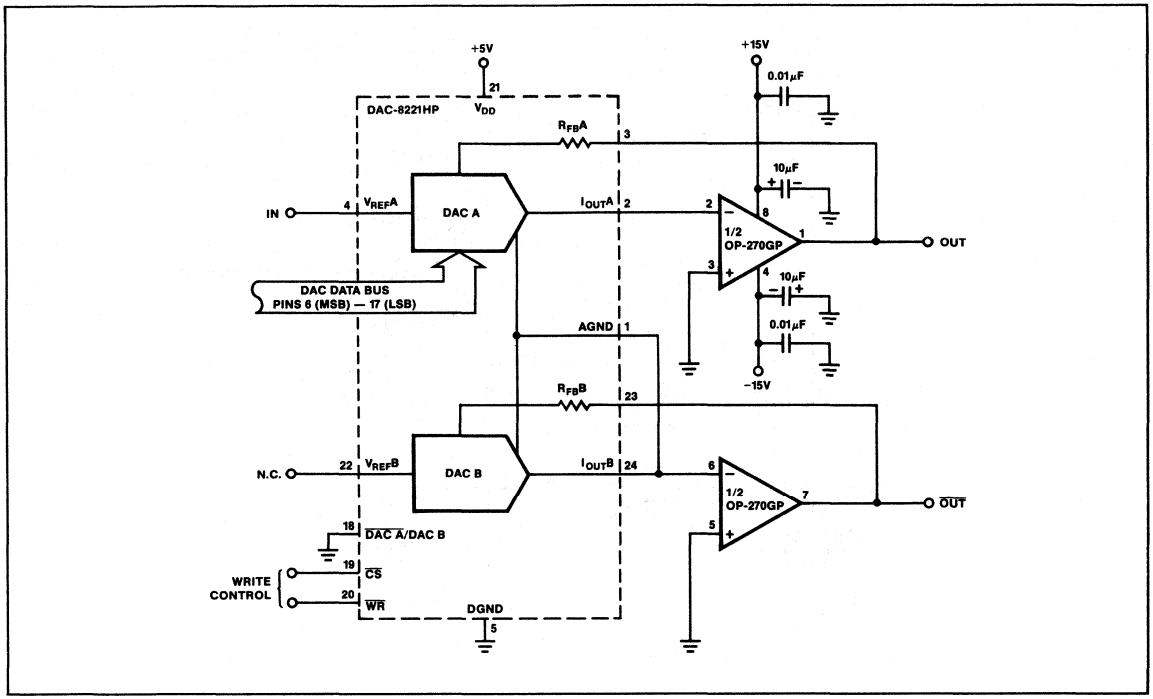


FIGURE 14: Digital Panning Control Output

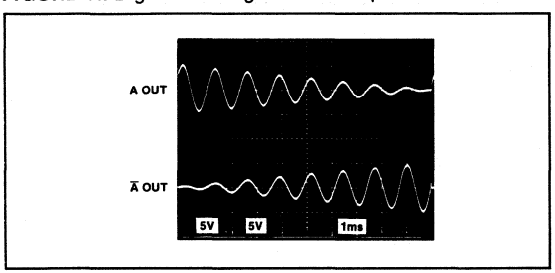
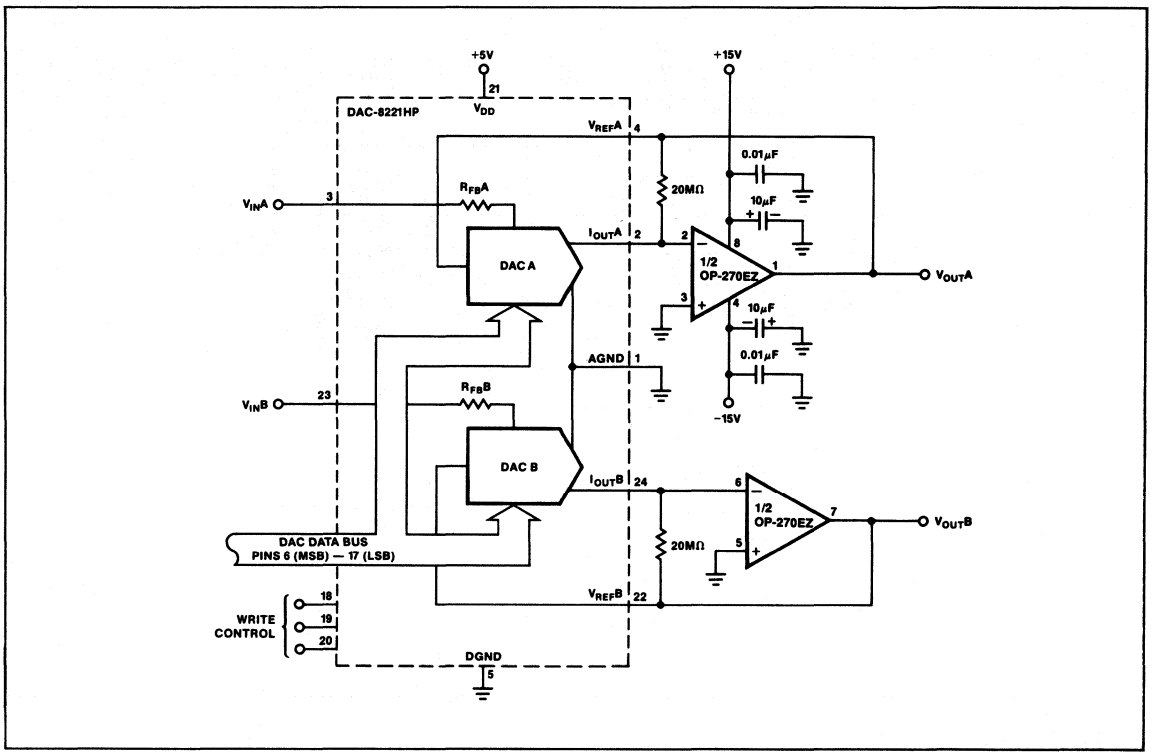


FIGURE 15: Dual Programmable Gain Amplifier



ANALOG DEVICES

High Speed Dual Operational Amplifier

OP-271

FEATURES

- **Excellent Speed ..... 8.5V/μs Typ**
- **Fast Settling (0.01%) ..... 2μs Typ**
- **Unity-Gain Stable**
- **High Gain-Bandwidth ..... 5MHz Typ**
- **Low Input Offset Voltage ..... 200μV Max**
- **Low Offset Voltage Drift ..... 2μV/°C Max**
- **High Gain ..... 400V/mV Min**
- **Outstanding CMR ..... 106 dB Min**
- **Industry Standard 8-Pin Dual Pinout**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (μV)	PACKAGE CERDIP 8-PIN	PACKAGE PLASTIC	PACKAGE LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
200	OP271AZ*	–	OP271ARC/883	MIL
200	OP271EZ	–	–	XND
300	OP271FZ	–	–	XND
400	–	OP271GP	–	XND
400	–	OP271GS††	–	XND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

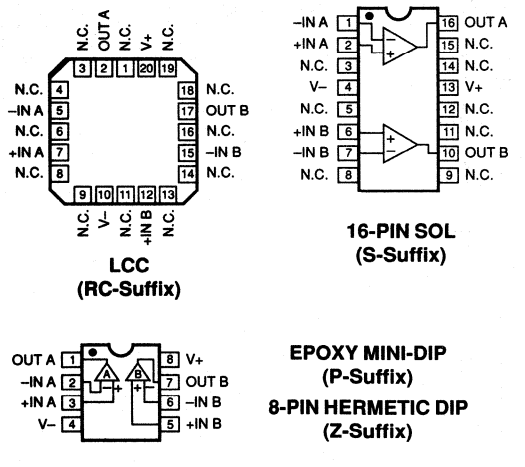
GENERAL DESCRIPTION

The OP-271 is a unity-gain stable monolithic dual op amp featuring excellent speed, 8.5V/μs typical, and fast settling time, 2μs typical to 0.01%. The OP-271 has a gain-bandwidth of 5MHz with a high phase margin of 62°.

Input offset voltage of the OP-271 is under 200μV with input offset voltage drift below 2μV/°C, guaranteed over the full military temperature range. Open-loop gain exceeds 400,000 into a 10kΩ load ensuring outstanding gain accuracy and linearity. The input bias current is under 20nA limiting errors due to source resistance. The OP-271's outstanding CMR, over 106dB, and low PSRR, under 5.6μV/V, reduce errors caused by ground noise and power supply fluctuations. In addition, the OP-271 exhibits high CMR and PSRR over a wide frequency range, further improving system accuracy.

Continued

PIN CONNECTIONS



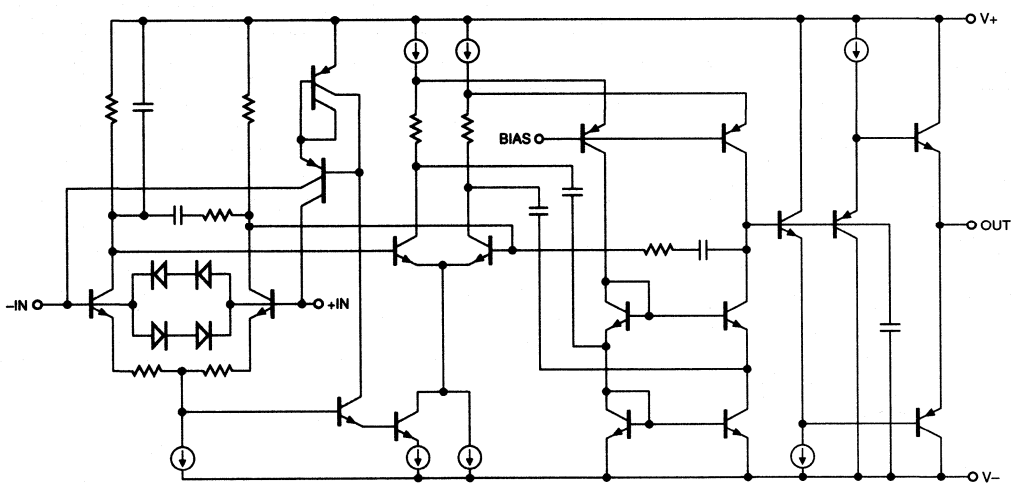
LCC (RC-Suffix)

16-PIN SOL (S-Suffix)

EPOXY MINI-DIP (P-Suffix)

8-PIN HERMETIC DIP (Z-Suffix)

SIMPLIFIED SCHEMATIC (One of the two amplifiers is shown.)



The OP-271 offers outstanding DC and AC matching between channels. This is especially valuable for applications such as multiple gain blocks, high-speed instrumentation and amplifiers, buffers and active filters.

The OP-271 conforms to the industry standard 8-pin dual op amp pinout. It is pin compatible with the TL072, TL082, LF412, and 1458/1558 dual op amps and can be used to significantly improve systems using these devices.

For applications requiring lower voltage noise, see the OP-270. For a quad version of the OP-271, see the OP-471.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Differential Input Voltage (Note 2) ..... ±1.0V
Differential Input Current (Note 2) ..... ±25mA
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C
Junction Temperature (T_J) ..... –65°C to +150C
Operating Temperature Range
OP-271A ..... –55°C to +125°C
OP-271E, OP-271F, OP-271G ..... –40°C to +85°C

PACKAGE TYPE	Θ_{JA} (Note 3)	Θ_{JC}	UNITS
8-Pin Hermetic DIP (Z)	134	12	°C/W
8-Pin Plastic DIP (P)	96	37	°C/W
20-Contact LCC (RC)	88	33	°C/W
8-Pin SO (S)	92	27	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. The OP-271's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise performance. If differential voltage exceeds ±1.0V, the input current should be limited to ±25mA.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

			OP-271A/E			OP-271F			OP-271G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		–	75	200	–	150	300	–	200	400	µV
Input Offset Current	I_{OS}	V_{CM} = 0V	–	1	10	–	4	15	–	7	20	nA
Input Bias Current	I_B	V_{CM} = 0V	–	4	20	–	6	40	–	12	60	nA
Input Noise Voltage Density	e_n	f_O = 1kHz	–	7.6	–	–	7.6	–	–	7.6	–	nV/ Hz
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V R_L = 10kΩ R_L = 2kΩ	400 300	650 500	– –	300 200	500 300	– –	250 175	400 250	– –	V/mV
Input Voltage Range	IVR	(Note 1)	±12	±12.5	–	±12	±12.5	–	±12	±12.5	–	V
Output Voltage Swing	V_O	R_L ≥ 2kΩ	±12	±13	–	±12	±13	–	±12	±13	–	V
Common-Mode Rejection	CMR	V_{CM} = ±12V	106	120	–	100	115	–	90	105	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	–	0.6	3.2	–	1.8	5.6	–	2.4	7.0	µV/V
Slew Rate	SR		5.5	8.5	–	5.5	8.5	–	5.5	8.5	–	V/µs
Phase Margin	$ø_m$	A_V = +1	–	62	–	–	62	–	–	62	–	deg
Supply Current (All Amplifiers)	I_{SY}	No Load	–	4.5	6.5	–	4.5	6.5	–	4.5	6.5	mA
Gain Bandwidth Product	GBW		–	5	–	–	5	–	–	5	–	MHz
Channel Separation	CS	V_O = 20V_{p-p} f_O = 10Hz (Note 2)	125	175	–	125	175	–	–	175	–	dB
Input Capacitance	C_{IN}		–	3	–	–	3	–	–	3	–	pF
Input Resistance Differential-Mode	R_{IN}		–	0.4	–	–	0.4	–	–	0.4	–	MΩ
Input Resistance Common-Mode	R_{INCM}		–	20	–	–	20	–	–	20	–	GΩ
Settling Time	t_s	A_V = +1, 10V Step to 0.01%	–	2	–	–	2	–	–	2	–	µs

NOTES:
1. Guaranteed by CMR test.
2. Guaranteed but not 100% tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $-55°C \leq T_A \leq 125°C$ for OP-271A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-271A MIN	OP-271A TYP	OP-271A MAX	UNITS
Input Offset Voltage	V_{OS}		—	115	400	µV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.4	2	µV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	1.5	30	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	7	60	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	 300 200	 600 500	 — —	V/mV
Input Voltage Range	IVR	(Note 1)	±12	±12.5	—	V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm12V$	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm4.5V$ to $\pm18V$	—	1.0	5.6	µV/V
Supply Current (All Amplifiers)	I_{SY}	No Load	—	5.3	7.5	mA

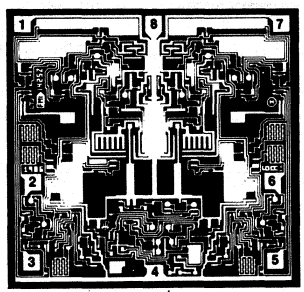
NOTE:
1. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $-40°C \leq T_A \leq +85°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-271A/E MIN	OP-271A/E TYP	OP-271A/E MAX	OP-271F MIN	OP-271F TYP	OP-271F MAX	OP-271G MIN	OP-271G TYP	OP-271G MAX	UNITS
Input Offset Voltage	V_{OS}		–	100	330	–	215	560	–	300	700	µV
Average Input Offset Voltage Drift	TCV_{OS}		–	0.4	2	–	1	4	–	2.0	5	µV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	–	1	30	–	5	40	–	15	50	nA
Input Bias Current	I_B	$V_{CM} = 0V$	–	6	60	–	10	70	–	15	80	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	 300 200	 600 500	 – –	 200 100	 500 400	 – –	 150 90	 400 300	 – –	V/mV
Input Voltage Range	IVR	(Note 1)	±12	±12.5	–	±12	±12.5	–	±12	±12.5	–	V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	–	±12	±13	–	±12	±13	–	V
Common-Mode Rejection	CMR	$V_{CM} = \pm12V$	100	120	–	94	115	–	90	100	–	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm4.5V$ to $\pm18V$	–	0.7	5.6	–	51.8	10	–	2.0	15	µV/V
Supply Current (All Amplifiers)	I_{SY}	No Load	–	5.2	7.2	–	5.2	7.2	–	5.2	7.2	mA

NOTE:
1. Guaranteed by CMR test.

DICE CHARACTERISTICS



DIE SIZE 0.094 × 0.092 inch, 8,648 sq. mils
(2.39 × 2.34 mm, 5.60 sq. mm)

1. OUT A
2. −IN A
3. +IN A
4. V−
5. +IN B
6. −IN B
7. OUT B
8. V+

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

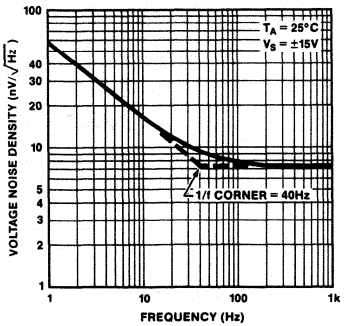
PARAMETER	SYMBOL	CONDITIONS	OP-271GBC LIMIT	UNITS
Input Offset Voltage	V_{OS}		300	µV MAX
Input Offset Current	I_{OS}	$V_{CM} = 0V$	15	nA MAX
Input Bias Current	I_B	$V_{CM} = 0V$	40	nA MAX
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	 300 200	V/mV MIN
Input Voltage Range	IVR	(Note 1)	±12	V MIN
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 12V$	100	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	5.6	µV/V MAX
Supply Current (All Amplifiers)	I_{SY}	No Load	6.5	mA MAX

NOTES:
1. Guaranteed by CMR test.

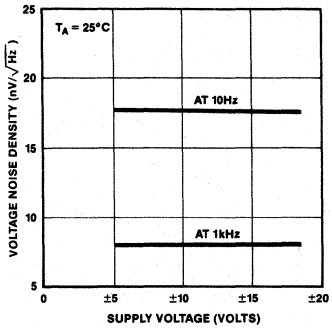
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

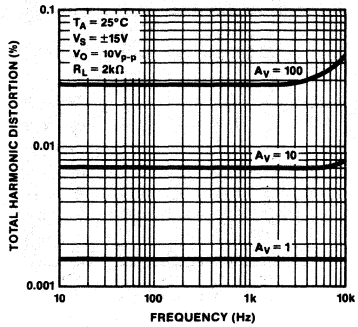
VOLTAGE NOISE DENSITY vs FREQUENCY



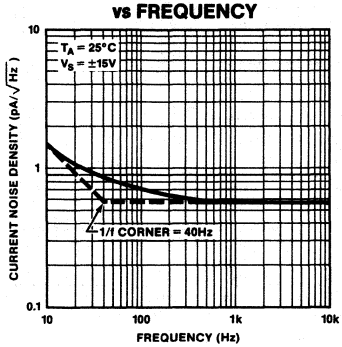
VOLTAGE NOISE DENSITY vs SUPPLY VOLTAGE



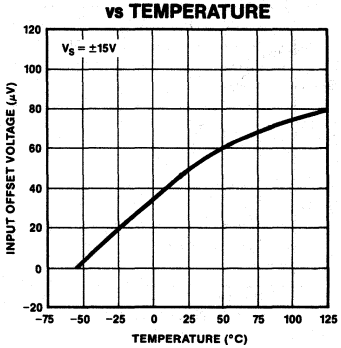
TOTAL HARMONIC DISTORTION vs FREQUENCY



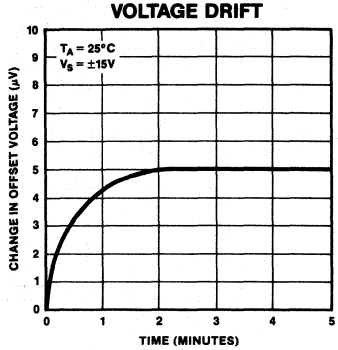
CURRENT NOISE DENSITY vs FREQUENCY



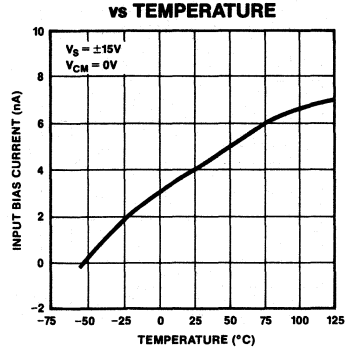
INPUT OFFSET VOLTAGE vs TEMPERATURE



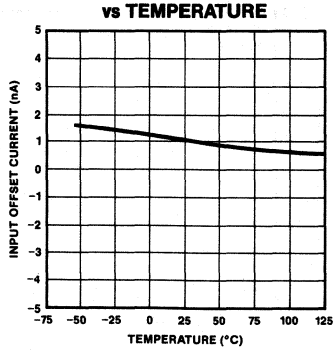
WARM-UP OFFSET VOLTAGE DRIFT



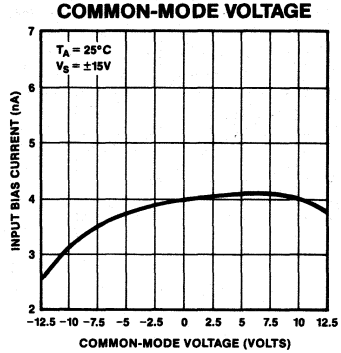
INPUT BIAS CURRENT vs TEMPERATURE



INPUT OFFSET CURRENT vs TEMPERATURE

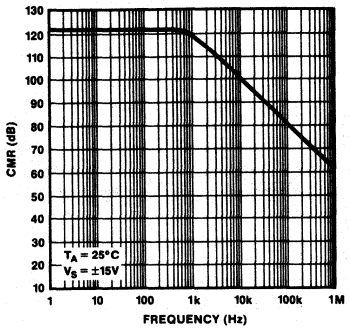


INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

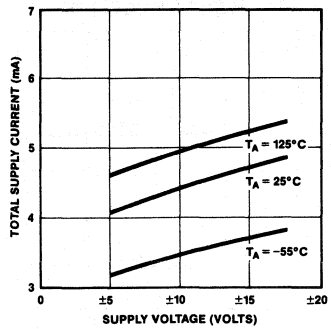


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

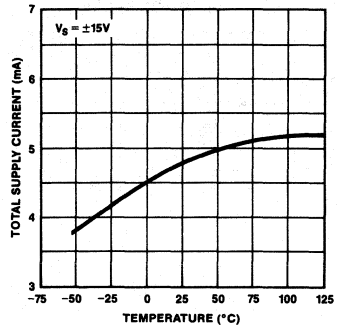
CMR vs FREQUENCY



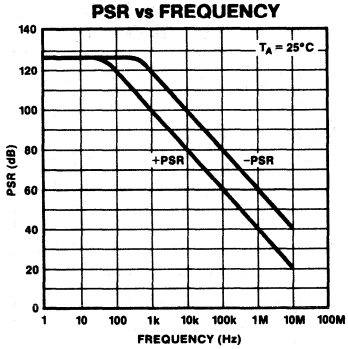
TOTAL SUPPLY CURRENT vs SUPPLY VOLTAGE



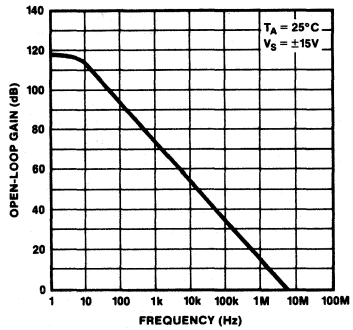
TOTAL SUPPLY CURRENT vs TEMPERATURE



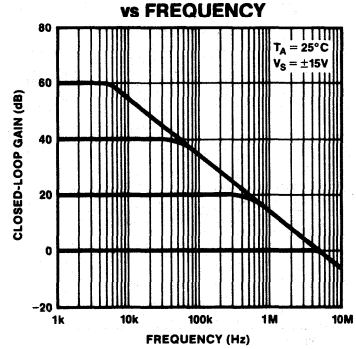
PSR vs FREQUENCY



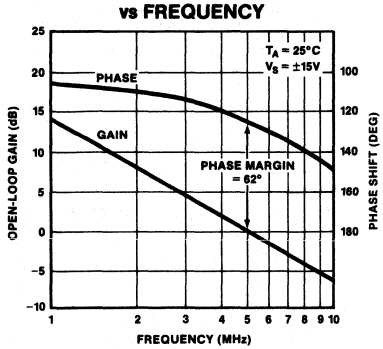
OPEN-LOOP GAIN vs FREQUENCY



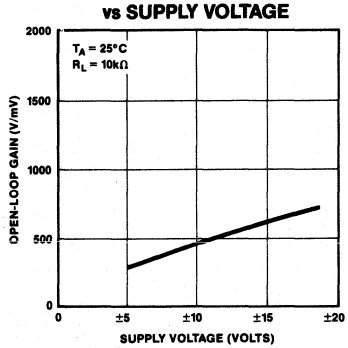
CLOSED-LOOP GAIN vs FREQUENCY



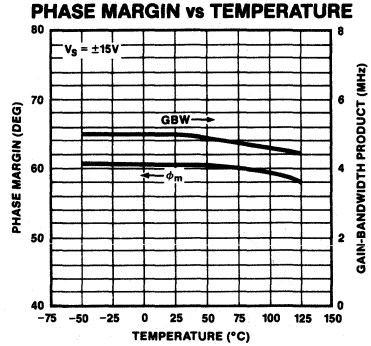
OPEN-LOOP GAIN, PHASE SHIFT vs FREQUENCY



OPEN-LOOP GAIN vs SUPPLY VOLTAGE

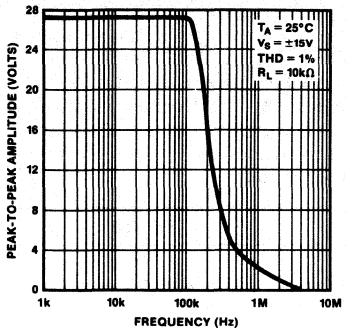


GAIN-BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE

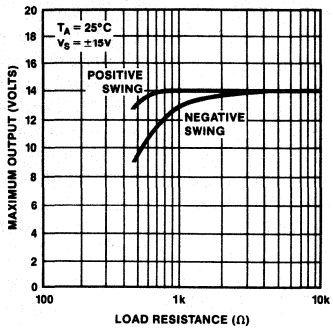


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

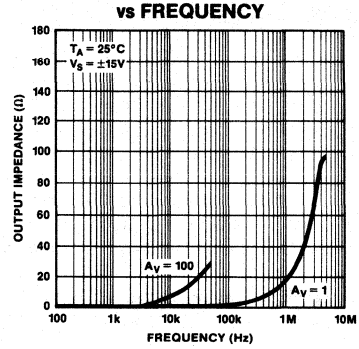
MAXIMUM OUTPUT SWING vs FREQUENCY



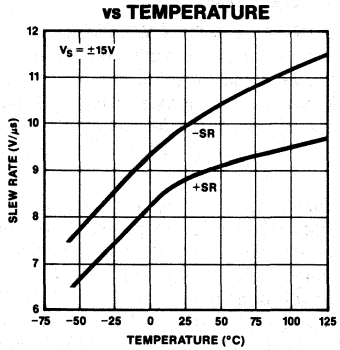
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



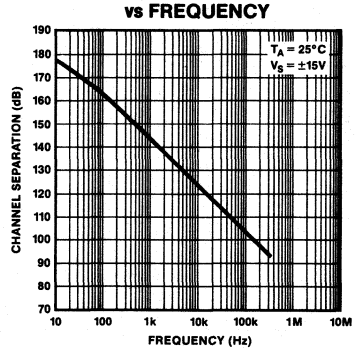
OUTPUT IMPEDANCE vs FREQUENCY



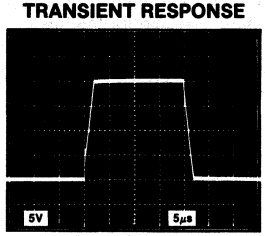
SLEW RATE vs TEMPERATURE



CHANNEL SEPERATION vs FREQUENCY

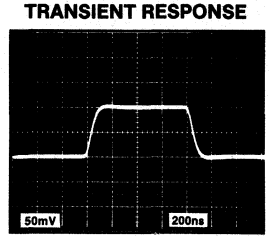


LARGE-SIGNAL TRANSIENT RESPONSE



T_A = 25°C
V_S = ±15V
A_V = +1

SMALL-SIGNAL TRANSIENT RESPONSE



T_A = 25°C
V_S = ±15V
A_V = +1

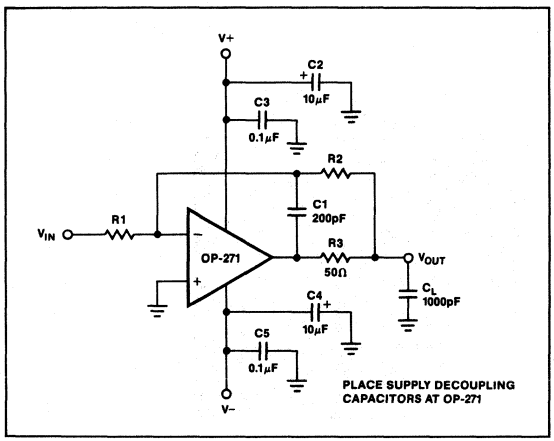
APPLICATIONS INFORMATION

CAPACITIVE LOAD DRIVING AND POWER SUPPLY CONSIDERATIONS

The OP-271 is unity-gain stable and is capable of driving large capacitive loads without oscillating. Nonetheless, good supply bypassing is highly recommended. Proper supply bypassing reduces problems caused by supply line noise and improves the capacitive load driving capability of the OP-271.

In the standard feedback amplifier, the op amp's output resistance combines with the load capacitance to form a low-pass filter that adds phase shift in the feedback network and reduces stability. A simple circuit to eliminate this effect is shown in Figure 1. The added components, C1 and R3, decouple the amplifier from the load capacitance and provide additional stability. The values of C1 and R3 shown in Figure 8 are for a load capacitance of up to 1000pF when used with the OP-271.

FIGURE 1: Driving Large Capacitive Loads

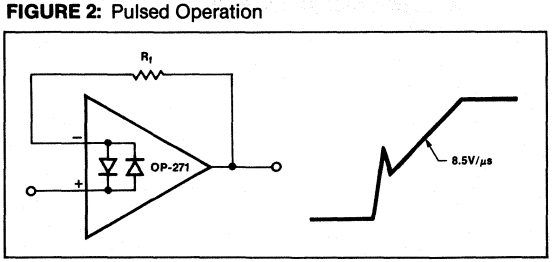


UNITY-GAIN BUFFER APPLICATIONS

When $R_f \leq 100\Omega$ and the input is driven with a fast, large-signal pulse (>1V), the output waveform will look as shown in Figure 2.

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input, and a current, limited only by the output short-circuit protection, will be drawn by the signal generator. With $R_f \geq 500\Omega$, the output is capable of handling the current requirements ($I_L \leq 20mA$ at 10V); the amplifier will stay in its active mode and a smooth transition will occur.

FIGURE 2: Pulsed Operation



When $R_f > 3k\Omega$, a pole created by R_f and the amplifier's input capacitance (3pF) creates additional phase shift and reduces phase margin. A small capacitor in parallel with R_f helps eliminate this problem.

COMPUTER SIMULATIONS

Many electronic design and analysis programs include models for op amps which calculate AC performance from the location of poles and zeros. As an aid to designers utilizing such a program, major poles and zeros of the OP-271 are listed below. Their location will vary slightly between production lots. Typically, they will be within ±15% of the frequency listed. Use of this data will enable the designer to evaluate gross circuit performance quickly, but should not supplant rigorous characterization of a breadboarded circuit.

POLES	ZEROS
15 Hz	2.5 MHz
1.2 MHz	4 × 23 MHz
2 × 32 MHz	—
8 × 40 MHz	—

APPLICATIONS

LOW PHASE ERROR AMPLIFIER

The simple amplifier depicted in Figure 3 utilizes a monolithic dual operational amplifier and a few resistors to substantially reduce phase error compared to conventional amplifier designs. At a given gain, the frequency range for a specified phase accuracy is over a decade greater than for a standard single op amp amplifier.

The low phase error amplifier performs second-order frequency compensation through the response of op amp A2 in the feedback loop of A1. Both op amps must be extremely well matched in frequency response. At low frequencies, the A1 feedback loop forces $V_2/(K1+1) = V_{IN}$. The A2 feedback loop forces $V_O/(K1+1) = V_2/(K1+1)$ yielding an overall transfer function of $V_O/V_{IN} = K1+1$. The DC gain is determined by the resistor divider at the output, V_O, and is not directly affected by the resistor divider around A2. Note that, like a conventional single op amp amplifier, the DC gain is set by resistor ratios only. Minimum gain for the low phase error amplifier is 10.

FIGURE 3: Low Phase Error Amplifier

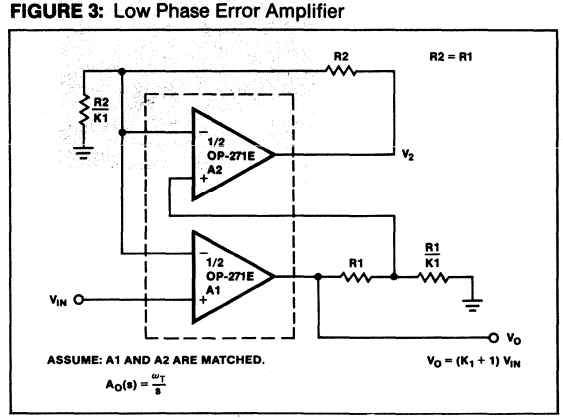


FIGURE 4: Phase Error Comparison

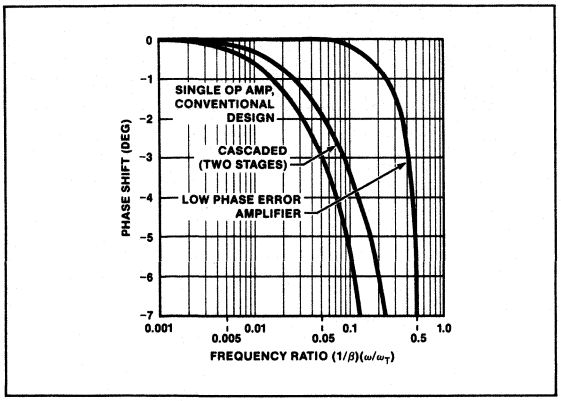


Figure 4 compares the phase error performance of the low phase error amplifier with a conventional single op amp amplifier and a cascaded two-stage amplifier. The low phase error amplifier shows a much lower phase error, particularly for frequencies where $\omega/\beta\omega_T < 0.1$. For example, phase error of $-0.1°$ occurs at 0.002 $\omega/\beta\omega_T$ for the single op amp amplifier, but at 0.11 $\omega/\beta\omega_T$ for the low phase error amplifier.

For more detailed information on the low phase error amplifier, see Application Note AN-107.

DUAL 12-BIT VOLTAGE OUTPUT DAC

The dual voltage output DAC shown in Figure 5 will settle to 12-bit accuracy from zero to full scale in 2μs typically. The CMOS DAC-8222 utilizes a 12-bit, double-buffered input structure allowing faster digital throughput and minimizing digital feedthrough.

FAST CURRENT PUMP

Maximum output current of the fast current pump shown in Figure 6 is ±11mA. Voltage compliance exceeds ±10V with ±15V supplies. The current pump has an output resistance of over 3MΩ and maintains 12-bit linearity over its entire output range.

2

FIGURE 6: Fast Current Pump

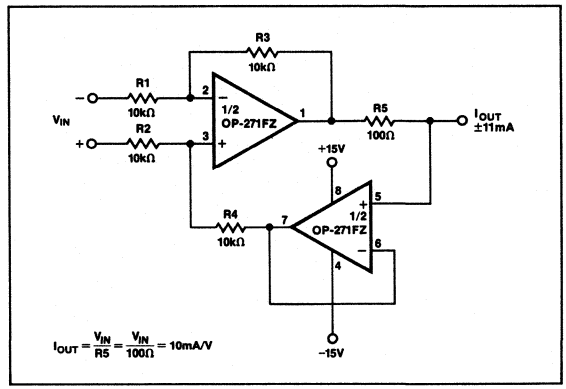
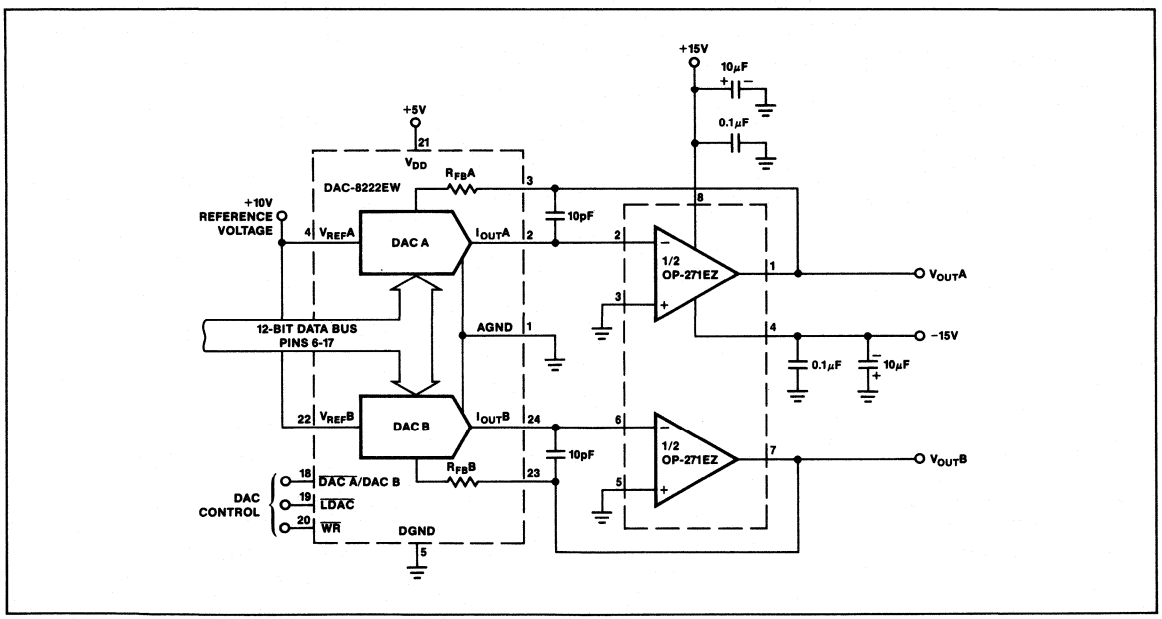


FIGURE 5: Dual 12-Bit Voltage Output DAC



ANALOG DEVICES

Dual Bipolar/JFET, Audio Operational Amplifier

OP-275*

FEATURES

Excellent Sonic Characteristics
Low Noise: 6 nV/$\sqrt{Hz}$
Low Distortion: 0.0006%
High Slew Rate: 22 V/μs
Wide Bandwidth: 9 MHz
Low Supply Current: 5 mA
Low Offset Voltage: 1 mV
Low Offset Current: 2 nA
Unity Gain Stable
SOIC-8 Package

APPLICATIONS

High Performance Audio
Active Filters
Fast Amplifiers
Integrators

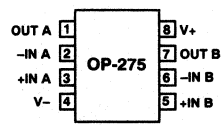
GENERAL DESCRIPTION

The OP-275 is the first amplifier to feature the Butler Amplifier front-end. This new front-end design combines both bipolar and JFET transistors to attain amplifiers with the accuracy and low noise performance of bipolar transistors, and the speed and sound quality of JFETs. Total Harmonic Distortion plus Noise equals previous audio amplifiers, but at much lower supply currents.

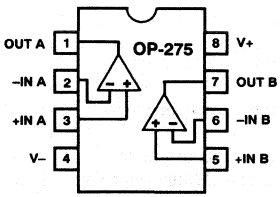
A very low 1/f corner of below 6 Hz maintains a flat noise density response. Whether noise is measured at either 30 Hz or 1 kHz, it is only 6 nV/$\sqrt{Hz}$. The JFET portion of the input stage gives the OP-275 its high slew rates to keep distortion low, even when large output swings are required, and the 22 V/μs slew rate of the OP-275 is the fastest of any standard audio amplifier. Best of all, this low noise and high speed are accomplished using less than 5 mA of supply current, lower than any standard audio amplifier.

PIN CONNECTIONS

8-Lead Narrow Body SOIC (S Suffix)



8-Lead Epoxy DIP (P Suffix)



Improved dc performance is also provided with bias and offset currents greatly reduced over purely bipolar designs. Input offset voltage is guaranteed at 1 mV and is typically less than 200 μV. This allows the OP-275 to be used in many dc coupled or summing applications without the need for special selections or the added noise of additional offset adjustment circuitry.

The output is capable of driving 600 Ω loads to 10 V rms while maintaining low distortion. THD + Noise at 3 V rms is a low 0.0006%.

The OP-275 is specified over the extended industrial (−40°C to +85°C) temperature range. OP-275s are available in both plastic DIP and SOIC-8 packages. SOIC-8 packages are available in 2500 piece reels. Many audio amplifiers are not offered in SOIC-8 surface mount packages for a variety of reasons, however the OP-275 was designed so that it would offer full performance in surface mount packaging.

*Patent pending.

OP-275—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
AUDIO PERFORMANCE						
THD + Noise		V_{IN} = 3 V rms, R_L = 2 kΩ, f = 1 kHz		0.0006		%
Voltage Noise Density	e_n	f = 30 Hz		7		nV/√Hz
		f = 1 kHz		6		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		1.5		pA/√Hz
Headroom		THD + Noise ≤ 0.01%, R_L = 2 kΩ, V_S = ±18 V		>12.9		dBu
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}				1	mV
		−40°C≤T_A≤+85°C			1.25	mV
Input Bias Current	I_B	V_{CM} = 0 V		100	350	nA
		V_{CM} = 0 V, −40°C≤T_A≤+85°C		100	400	nA
Input Offset Current	I_{OS}	V_{CM} = 0 V		2	±50	nA
		V_{CM} = 0 V, −40°C≤T_A≤+85°C		2	±100	nA
Input Voltage Range	V_{CM}		−10.5		+10.5	V
Common-Mode Rejection	CMR	V_{CM} = ±10.5 V, −40°C≤T_A≤+85°C	80	106		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ	250			V/mV
		R_L = 2 kΩ, −40°C≤T_A≤+85°C	175			V/mV
		R_L = 600 Ω		200		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			5		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 2 kΩ	−13.5	±13.9	+13.5	V
		R_L = 2 kΩ, −40°C≤T_A≤+85°C	−13	±13.9	+13	V
		R_L = 600 Ω, V_S = ±18 V		±16		V
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V	85	111		dB
		V_S = ±4.5 V to ±18 V, −40°C≤T_A≤+85°C	80			dB
Supply Current	I_{SY}	V_S = ±4.5 V to ±18 V, V_O = 0 V, R_L = ∞, −40°C≤T_A≤+85°C		4	5	mA
		V_S = ±22 V, V_O = 0 V, R_L = ∞, −40°C≤T_A≤+85°C			5.5	mA
Supply Voltage Range	V_S		±4.5		±22	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	15	22		V/µs
Full-Power Bandwidth	BW_P					kHz
Gain Bandwidth Product	GBP			9		MHz
Phase Margin	∅o			62		Degrees
Overshoot Factor		V_{IN} = 100 mV, A_V = +1, R_L = 600 Ω, C_L = 100 pF		10		%

Specifications subject to change without notice.

WAFER TEST LIMITS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Conditions	Limit	Units
Offset Voltage	V_{OS}		1	mV max
Input Bias Current	I_B	V_{CM} = 0 V	350	nA max
Input Offset Current	I_{OS}	V_{CM} = 0 V	±50	nA max
Input Voltage Range[1]			±10.5	V min
Common-Mode Rejection	CMRR	V_{CM} = ±10.5 V	80	dB min
Power Supply Rejection Ratio	PSRR	V = ±4.5 V to ±18 V	85	dB min
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ	250	V/mV min
Output Voltage Range	V_O	R_L = 10 kΩ	±13.5	V min
Supply Current	I_{SY}	V_O = 0 V, R_L = ∞	5	mA max

NOTES

Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

[1]Guaranteed by CMR test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±22 V
Input Voltage[2] . . . . . ±18 V
Differential Input Voltage[2] . . . . . ±7.5 V
Output Short-Circuit Duration to GND[3] . . . . . Indefinite
Storage Temperature Range
(P, S) Package . . . . . −65°C to +150°C
Operating Temperature Range
OP-275G . . . . . −40°C to +85°C
Junction Temperature Range
(P, S) Package . . . . . −65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C

Package Type	θ_{JA}[4]	θ_{JC}	Units
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W

NOTES

[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

[2]For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.

[3]Shorts to either supply may destroy the device. See data sheet for full details.

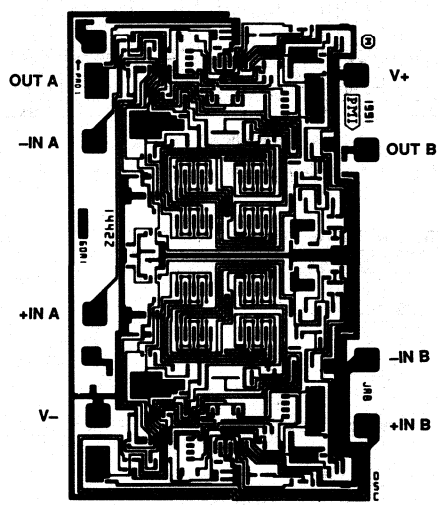
[4]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered in circuit board for SOIC package.

ORDERING GUIDE

Model	Temperature Range	Package Option*
OP275GP	−40°C to +85°C	8-Pin Plastic DIP
OP275GS	−40°C to +85°C	8-Pin SOIC
OP275GSR	−40°C to +85°C	SOIC-8 Reel, 2500 pcs.
OP275GBC	+25°C	DICE

*For outline information see Package Information section.

DICE CHARACTERISTICS



OP-275 Die Size 0.070 × 0.108 in. (7,560 sq. mils)

APPLICATIONS

Short Circuit Protection

The OP-275 has been designed with inherent output short circuit protection to ground.

However shorts to either supply may destroy the device when excessive voltages or currents are applied. For safe operation the output current of the OP-275 should be design limited to ±30 mA.

Total Harmonic Distortion

Total Harmonic Distortion + Noise (THD + N) of the OP-275 is well below 0.001% with any load down to 600 Ω. However, this is dependent upon the peak output swing. In Figure 1 it is seen that the THD + Noise with 3 V rms output is below 0.001%. In the following Figure 2, THD + Noise is below 0.001% for the 10 kΩ and 2 kΩ loads but increases to above 0.1% for the 600 Ω load condition. This is a result of the output swing capability of the OP-275. Notice the results in Figure 3, showing THD vs. V_{IN} (V rms). This figure shows that the THD + Noise remains very low until the output reaches 9.5 volts rms. This performance is similar to competitive products.

The output of the OP-275 is designed to maintain low harmonic distortion while driving 600 Ω loads. However, driving 600 Ω loads with very high output swings results in higher distortion if clipping occurs. A common example of this is in attempting to drive 10 V rms into any load with ±15 volt supplies. Clipping will occur and distortion will be very high.

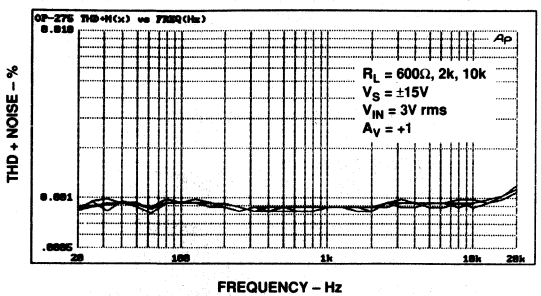


Figure 1. THD + Noise vs. Frequency vs. R_{LOAD}

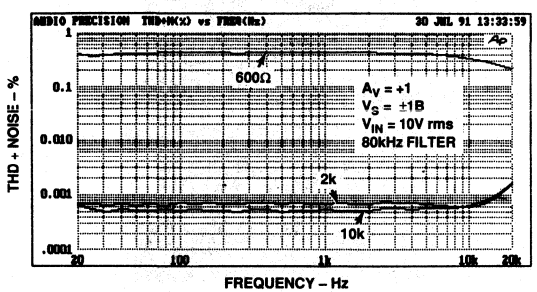


Figure 2. THD + Noise vs. R_{LOAD}; V_{IN} = 10 V rms, ±18 V Supplies

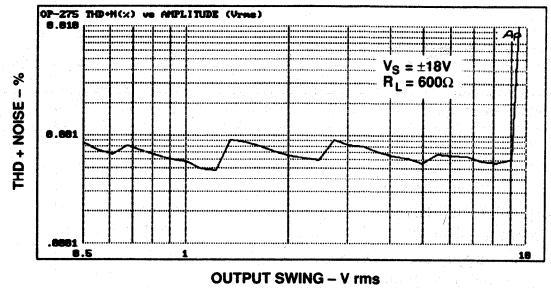


Figure 3. Headroom, THD + Noise vs. Output Amplitude (V rms); R_{LOAD} = 600 Ω, V_{SUP} = ±18 V

To attain low harmonic distortion with large output swings, supply voltages may be increased. Figure 4 shows the performance of the OP-275 driving 600 Ω loads with supply voltages varying from ±18 to ±20 volts. Notice that with ±18 volt supplies the distortion is fairly high, while with ±20 volt supplies it is a very low 0.0007%.

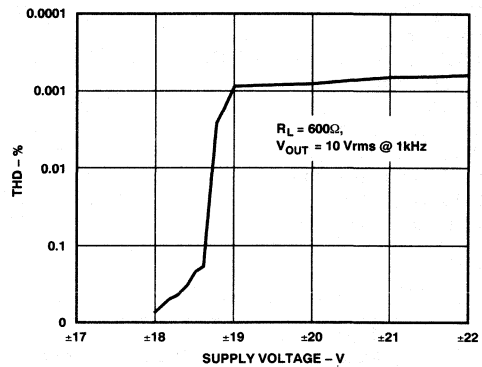


Figure 4. THD + Noise vs. Supply Voltage

Noise

The voltage noise density of the OP-275 is below 7 nV/$\sqrt{\text{Hz}}$ from 30 Hz. This enables low noise designs to have good performance throughout the full audio range. Figure 5 shows a typical OP-275 with a 1/f corner at 5.2 Hz.

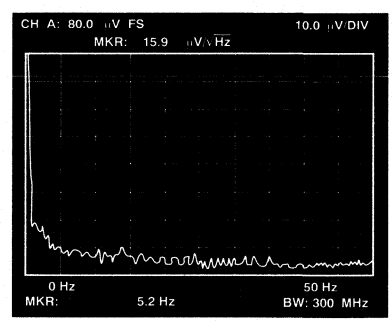


Figure 5. 1/f Noise Corner, V_s = ±15 V, A_V = 1000

Noise Testing

For audio applications the noise density is usually the most important noise parameter. For characterization the OP-275 is tested using an Audio Precision, System One. The input signal to the Audio Precision must be amplified enough to measure accurately. For the OP-275 the noise is gained by approximately 1020 using the circuit shown in Figure 6. Any readings on the Audio Precision must then be divided by the gain. In implementing this test fixture, good supply bypassing is essential.

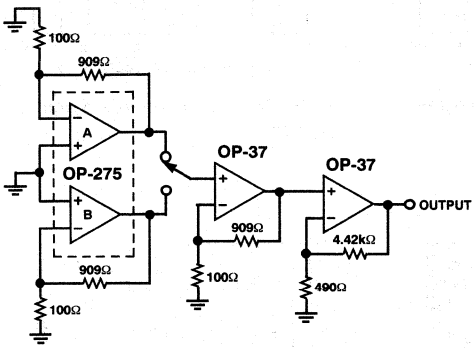


Figure 6. Noise Test Fixture

Driving Capacitive Loads

The OP-275 was designed to drive both resistive loads to 600 Ω and capacitive loads of over 1000 pF and maintain stability. While there is a degradation in bandwidth when driving capacitive loads, the designer need not worry about device stability. The graph in Figure 7 shows the 0 dB bandwidth of the OP-275 with capacitive loads from 10 pF to 1000 pF.

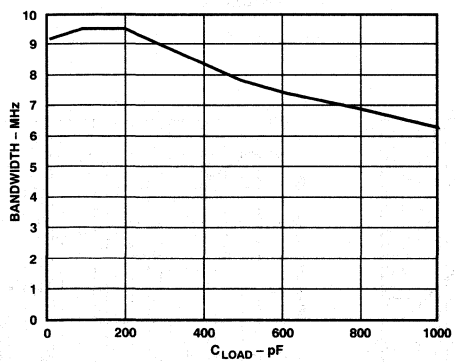


Figure 7. Bandwidth vs. C_{LOAD}

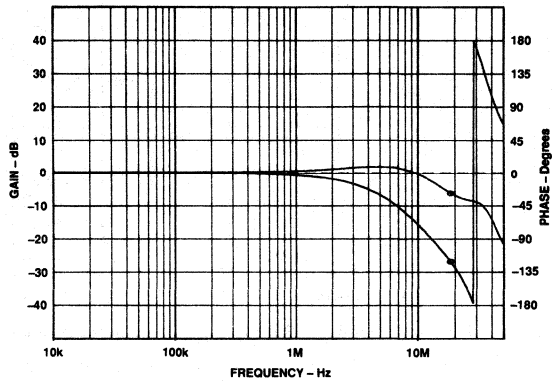


Figure 8. Closed-Loop Gain and Phase, A_V = +1

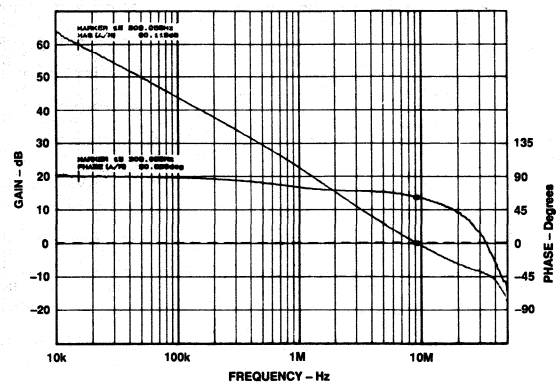
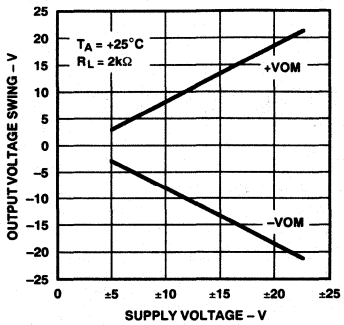
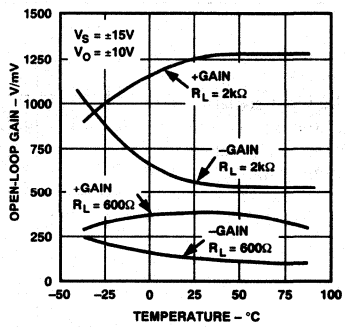


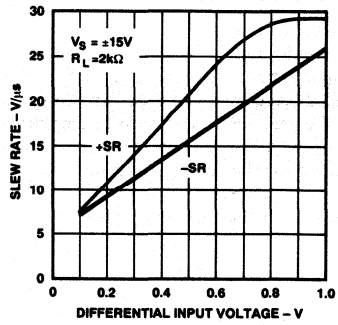
Figure 9. Open-Loop Gain and Phase



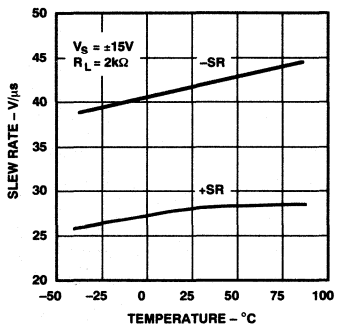
Output Voltage Swing vs. Supply Voltage



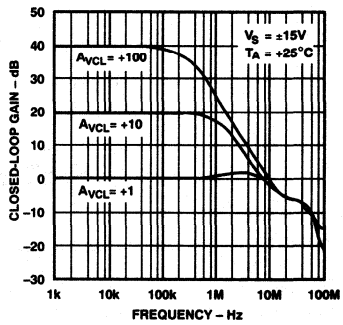
Open-Loop Gain vs. Temperature



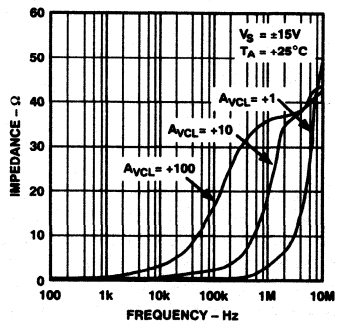
Slew Rate vs. Differential Input Voltage



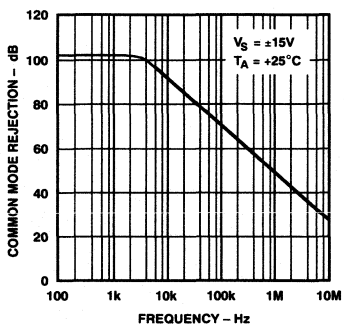
Slew Rate vs. Temperature



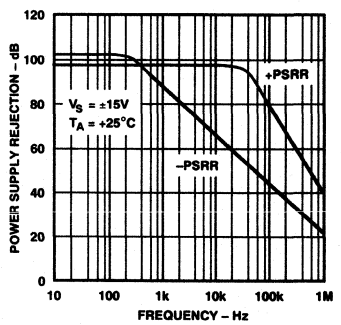
Closed-Loop Gain vs. Frequency



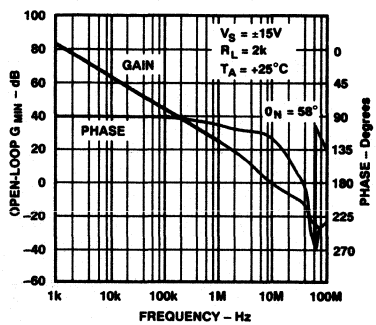
Closed-Loop Output Impedance vs. Frequency



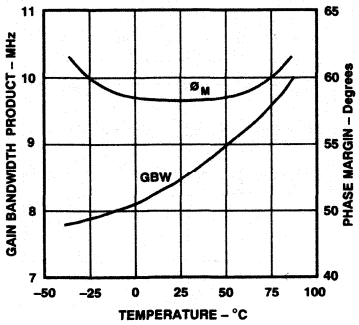
Common-Mode Rejection vs. Frequency



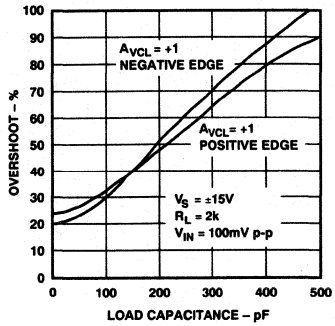
Power Supply Rejection vs. Frequency



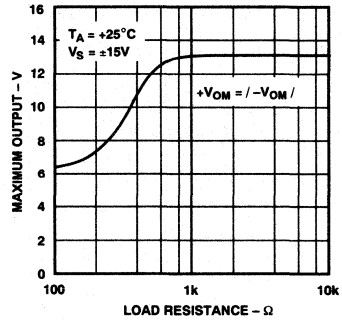
Open-Loop Gain, Phase vs. Frequency



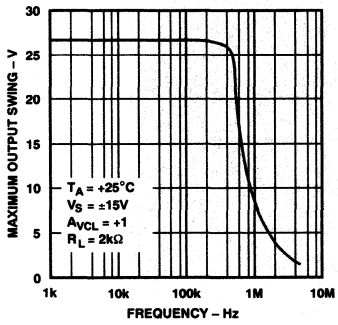
Gain Bandwidth Product, Phase Margin vs. Temperature



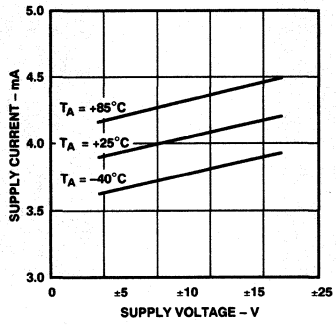
Small-Signal Overshoot vs. Load Capacitance



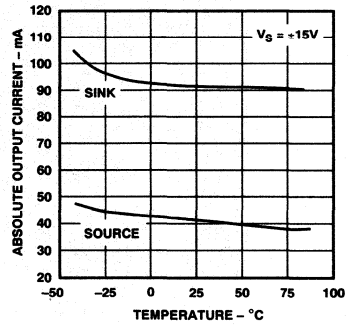
Maximum Output Voltage vs. Load Resistance



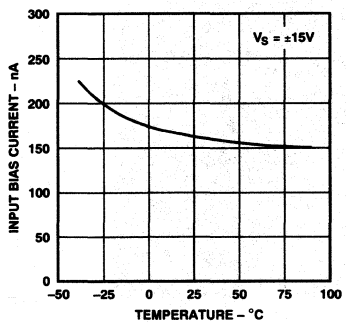
Maximum Output Swing vs. Frequency



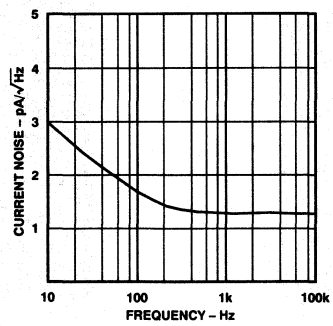
Supply Current vs. Supply Voltage



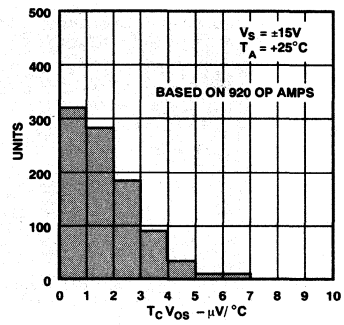
Short Circuit Current vs. Temperature



Input Bias Current vs. Temperature

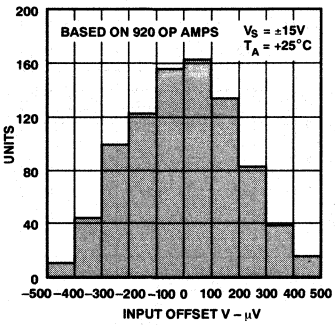


Current Noise Density vs. Frequency

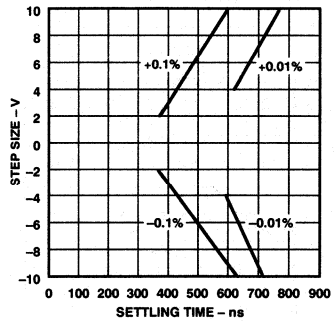


t_C V_{OS} Distribution

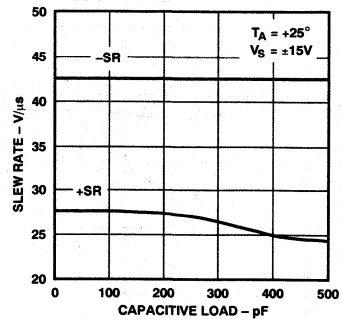
OP-275—Typical Performance



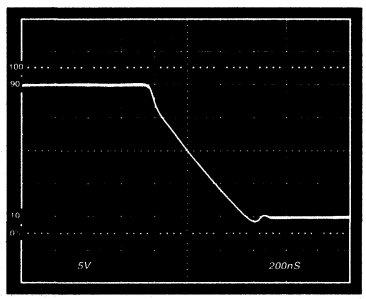
Input Offset (V_{OS}) Distribution



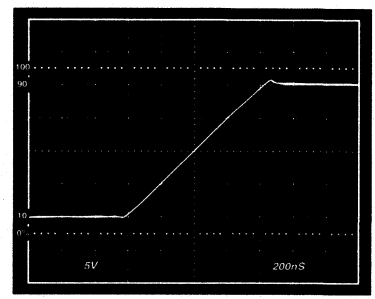
Settling Time vs. Step Size



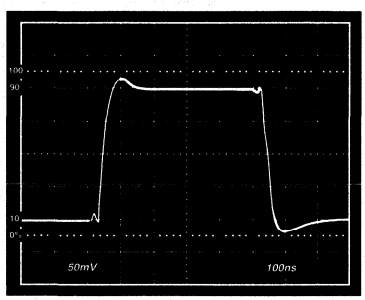
Slew Rate vs. Capacitive Load



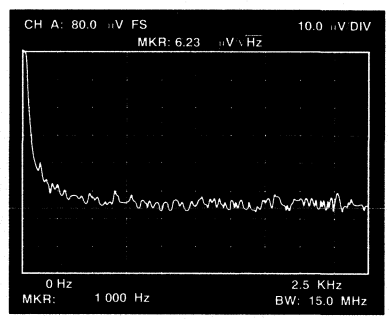
Negative Slew Rate
R_L = 2 kΩ, V_S = ±15 V, A_V = +1



Positive Slew Rate
R_L = 2 kΩ, V_S = ±15 V, A_V = +1



Small Signal Response
R_L = 2 kΩ, V_S = ±15 V, A_V = +1



OP-275 Voltage Noise Density vs. Frequency V_S = ±15 V, A_V = 1000

Dual/Quad Low Power, High Speed JFET Operational Amplifier

OP-282/OP-482

FEATURES
- High Slew Rate: 9 V/μs
- Wide Bandwidth: 4 MHz
- Low Supply Current: 250 μA/Amplifier
- Low Offset Voltage: 3 mV
- Low Bias Current: 100 pA
- Fast Settling Time
- Common-Mode Range Includes V+
- Unity Gain Stable

APPLICATIONS
- Active Filters
- Fast Amplifiers
- Integrators
- Supply Current Monitoring

GENERAL DESCRIPTION

The OP-282/OP-482 dual and quad operational amplifiers feature excellent speed at exceptionally low supply currents. Slew rate exceeds 7 V/μs with supply current under 250 μA per amplifier. These unity gain stable amplifiers have a typical gain-bandwidth of 4 MHz.

The JFET input stage of the OP-282/OP-482 insures bias current is typically a few picoamps and below 500 pA over the full temperature range. Offset voltage is under 3 mV for the dual and under 4 mV for the quad.

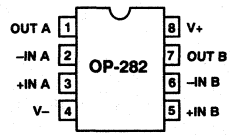
With a wide output swing, within 1.5 volts of each supply, low power consumption and high slew rate, the OP-282/OP-482 are ideal for battery-powered systems or power restricted applications. An input common-mode range that includes the positive supply makes the OP-282/OP-482 an excellent choice for high-side signal conditioning.

The OP-282/OP-482 are specified over the extended industrial temperature range. Both dual and quad amplifiers are available in plastic and ceramic DIP plus SOIC surface mount packages.

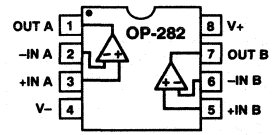
Contact your local sales office for MIL-STD-883 data sheet and availability.

PIN CONNECTIONS

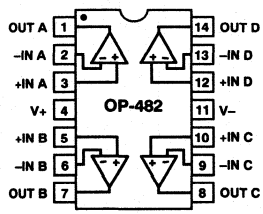
8-Lead Narrow-Body SOIC (S Suffix)



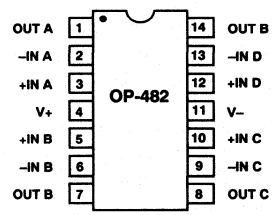
8-Lead Epoxy DIP (P Suffix)



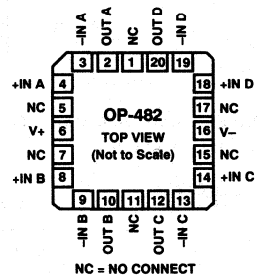
14-Lead Epoxy DIP (P Suffix)



14-Lead Narrow-Body SOIC (S Suffix)



20-Position Chip Carrier (RC Suffix)



OP-282/OP-482—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	OP-282		0.2	3	mV
		OP-282, $-40 \le T_A \le +85°C$			4.5	mV
Offset Voltage	V_{OS}	OP-482		0.2	4	mV
		OP-482, $-40 \le T_A \le +85°C$			6	mV
Input Bias Current	I_B	V_{CM} = 0 V		3	100	pA
		V_{CM} = 0 V, Note 1			500	pA
Input Offset Current	I_{OS}	V_{CM} = 0 V		1	50	pA
		V_{CM} = 0 V, Note 1			250	pA
Input Voltage Range			−11		+15	V
Common-Mode Rejection	CMR	$-11V \le V_{CM} \le +15$ V, $-40 \le T_A \le +85°C$	70	90		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ	20			V/mV
		R_L = 10 kΩ, $-40 \le T_A \le +85°C$	15			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			10		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			8		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 10 kΩ	−13.5	±13.9	13.5	V
Short Circuit Limit	I_{SC}	Source	3	10		mA
		Sink	−8	−12		mA
Open-Loop Output Impedance	Z_{OUT}	f = 1 MHz		200		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V,				
		$-40 \le T_A \le +85°C$		25	316	µV/V
Supply Current/Amplifier	I_{SY}	V_O = 0 V, $40 \le T_A \le +85°C$		210	250	µA
Supply Voltage Range	V_S		±4.5		±18	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ	7	9		V/µs
Full-Power Bandwidth	BW_P	1% Distortion		125		kHz
Settling Time	t_S	To 0.01%		1.6		µs
Gain Bandwidth Product	GBP			4		MHz
Phase Margin	∅o			55		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p–p	0.1 Hz to 10 Hz		1.3		µVp–p
Voltage Noise Density	e_n	f = 1 kHz		36		nV/√Hz
Current Noise Density	i_n			0.01		pA/√Hz

NOTE

[1]The input bias and offset currents are tested at $T_A = T_J$ = +85°C. Bias and offset currents are guaranteed but not tested at −40°C.

Specifications subject to change without notice.

WAFER TEST LIMITS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Limit	Units
Offset Voltage	V_{OS}	OP-282	3	mV max
Offset Voltage	V_{OS}	OP-482	4	mV max
Input Bias Current	I_B	V_{CM} = 0 V	100	pA max
Input Offset Current	I_{OS}	V_{CM} = 0 V	50	pA max
Input Voltage Range[1]			−11, +15	V min/max
Common-Mode Rejection	CMRR	$-11V \le V_{CM} \le +15$ V	70	dB min
Power Supply Rejection Ratio	PSRR	V = ±4.5 V to ±18 V	316	µV/V
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ	20	V/mV min
Output Voltage Range	V_O	R_L = 10 kΩ	±13.5	V min
Supply Current/Amplifier	I_{SY}	V_O = 0 V, R_L = ∞	250	µA max

NOTES

Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

[1]Guaranteed by CMR test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply voltage . . . . . ±18 V
Input Voltage[2] . . . . . ±18 V
Differential Input Voltage[2] . . . . . 36 V
Output Short-Circuit Duration . . . . . Indefinite
Storage Temperature Range
  Y, Z, RC Package . . . . . −65°C to +175°C
  P, S Package . . . . . −65°C to +150°C
Operating Temperature Range
  OP-282A, OP-482A . . . . . −55°C to +125°C
  OP-282G, OP-482G . . . . . −40°C to +85°C
Junction Temperature Range
  Y, Z, RC Package . . . . . −65°C to +125°C
  P, S Package . . . . . −65°C to +125°C
Lead Temperature Range (Soldering, 60 Sec) . . . . . +300°C

Package Type	θ_{JA}[3]	θ_{JC}	Units
8-Pin Cerdip (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W
14-Pin Cerdip (Y)	108	16	°C/W
14-Pin Plastic DIP (P)	83	39	°C/W
14-Pin SOIC (S)	120	36	°C/W
20-Contact LCC (RC)	98	38	°C/W

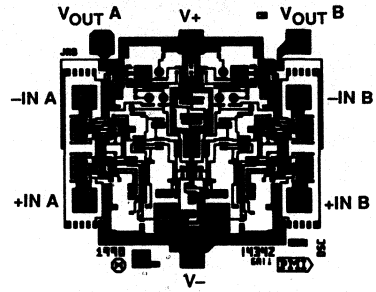
NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.
[3]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered in circuit board for SOIC package.

ORDERING GUIDE

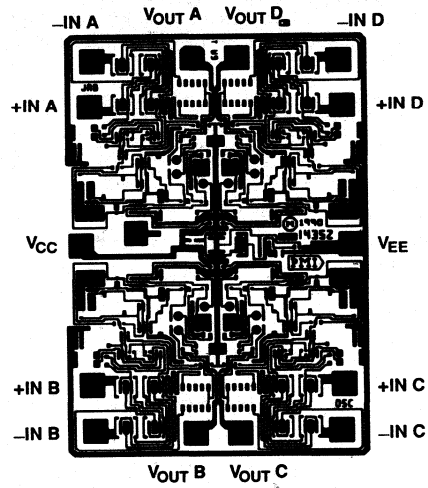
Model	Temperature Range	Package Option*
OP282AZ/883	−55°C to +125°C	14-Pin Cerdip
OP482AY/883	−55°C to +125°C	14-Pin Cerdip
OP482ARC/883	−55°C to +125°C	20-Contact LCC
OP282GP	−40°C to +85°C	8-Pin Plastic DIP
OP282GS	−40°C to +85°C	8-Pin SOIC
OP482GP	−40°C to +85°C	14-Pin Plastic DIP
OP482GS	−40°C to +85°C	14-Pin SOIC
OP282GBC	+25°C	DICE
OP482GBC	+25°C	DICE

*For outline information see Package Information section.

DICE CHARACTERISTICS



OP-282 Die Size 0.063 × 0.060 Inch, 3,780 Sq. Mils



OP-482 Die Size 0.070 × 0.098 Inch, 6,860 Sq. Mils

2

APPLICATIONS INFORMATION

The OP-282 and OP-482 are single and dual JFET op amps that have been optimized for high speed at low power. This combination makes these amplifiers excellent choices for battery powered or low power applications requiring above average performance. Applications benefiting from this performance combination include telecom, geophysical exploration, portable medical equipment and navigational instrumentation.

HIGH SIDE SIGNAL CONDITIONING

There are many applications that require the sensing of signals near the positive rail. OP-282s and OP-482s have been tested and guaranteed over a common-mode range ($-11\ V \leq V_{CM} \leq +15\ V$) that includes the positive supply.

One application where this is commonly used is in the sensing of power supply currents. This enables it to be used in current sensing applications such as the partial circuit shown in Figure 1. In this circuit, the voltage drop across a low value resistor, such as the 0.1 Ω shown here, is amplified and compared to 7.5 volts. The output can then be used for current limiting.

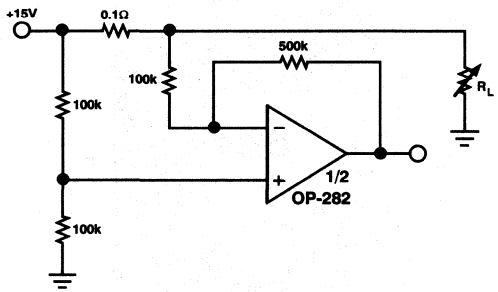


Figure 1. Phase Inversion

PHASE INVERSION

Most JFET-input amplifiers will invert the phase of the input signal if either input exceeds the input common-mode range. For the OP-282 and OP-482 negative signals in excess of approximately 14 volts will cause phase inversion. The cause of this effect is saturation of the input stage leading to the forward-biasing of a drain-gate diode. A simple fix for this in non-inverting applications is to place a resistor in series with the noninverting input. This limits the amount of current through the forward-biased diode and prevents the shutting down of the output stage. For the OP-282/OP-482, a value of 200 kΩ has been found to work. However, this adds a significant amount of noise.

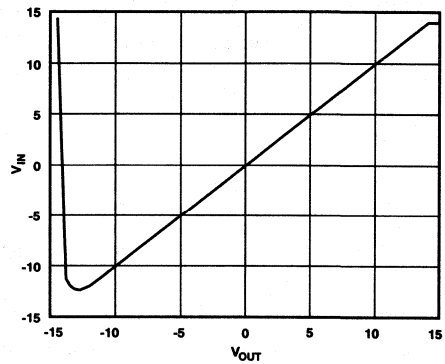


Figure 2. OP-282 Phase Reversal

ACTIVE FILTERS

The OP-282 and OP-482's wide bandwidth and high slew rates make either an excellent choice for many filter applications.

There are many types of active filter configurations, but the four most popular configurations are Butterworth, elliptical, Bessel, and Chebyshev. Each type has a response that is optimized for a given characteristic as shown in Table I.

Table I.

Type	Selectivity	Overshoot	Phase	Amplitude (Pass Band)	Amplitude (Stop Band)
Butterworth	Moderate	Good		Max Flat	
Chebyshev	Good	Moderate	Nonlinear	Equal Ripple	
Elliptical	Best	Poor		Equal Ripple	Equal Ripple
Bessel (Thompson)	Poor	Best	Linear		

PROGRAMMABLE STATE-VARIABLE FILTER

The circuit shown in Figure 3 can be used to accurately program the "Q," the cutoff frequency f_C, and the gain of a two-pole state-variable filter. OP-482s have been used in this design because of their high bandwidths, low power and low noise. This circuit takes only three packages to build because of the quad configuration of the op amps and DACs.

The DACs shown are all used in the voltage mode so all values are dependent only on the accuracy of the DAC and not on the absolute values of the DAC's resistive ladders. This make this circuit unusually accurate for a programmable filter.

Adjusting DAC 1 changes the signal amplitude across R1; therefore, the DAC attenuation times R1 determines the amount of signal current that charges the integrating capacitor, C1. This cutoff frequency can now be expressed as:

$$f_C = \frac{1}{2\pi R_1 C_1}\left(\frac{D_1}{256}\right)$$

where D_1 is the digital code for the DAC.

Gain of this circuit is set by adjusting D3. The gain equation is:

$$Gain = \frac{R_4}{R_5}\left(\frac{D_3}{256}\right)$$

DAC 2 is used to set the "Q" of the circuit. Adjusting this DAC controls the amount of feedback from the bandpass node to the input summing node. Note that the digital value of the DAC is in the numerator, therefore zero code is not a valid operating point.

$$Q = \frac{R_2}{R_3}\left(\frac{256}{D_2}\right)$$

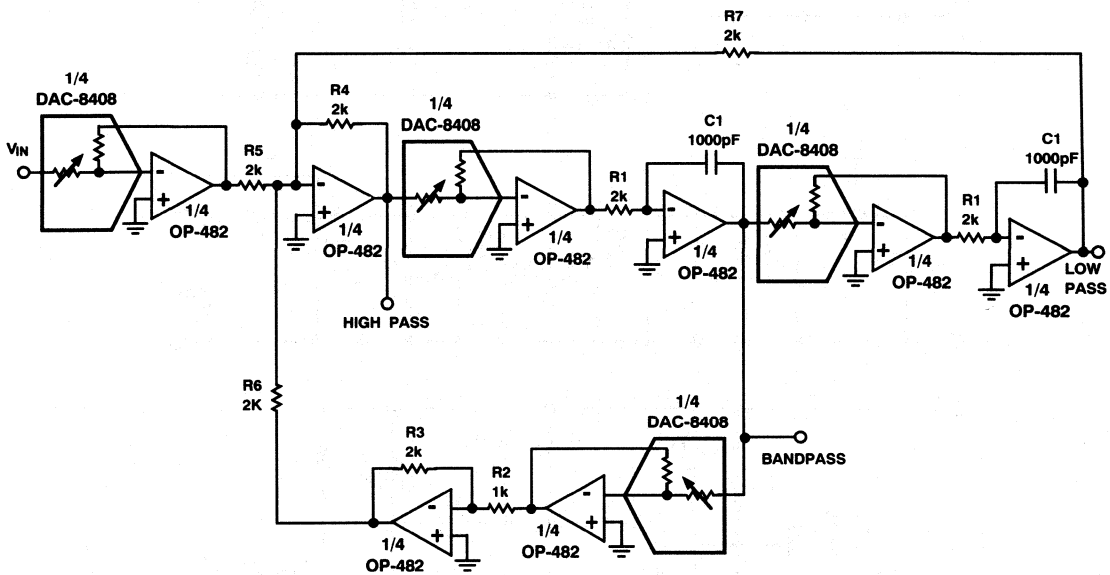


Figure 3.

OP-282/OP-482 SPICE MACRO MODEL

Figure 4 shows the OP-282 SPICE macro model. The model for the OP-482 is similar to that of the OP-282, but there are some minor changes in the circuit values. Contact ADI for a copy of the latest SPICE model diskette for both listings.

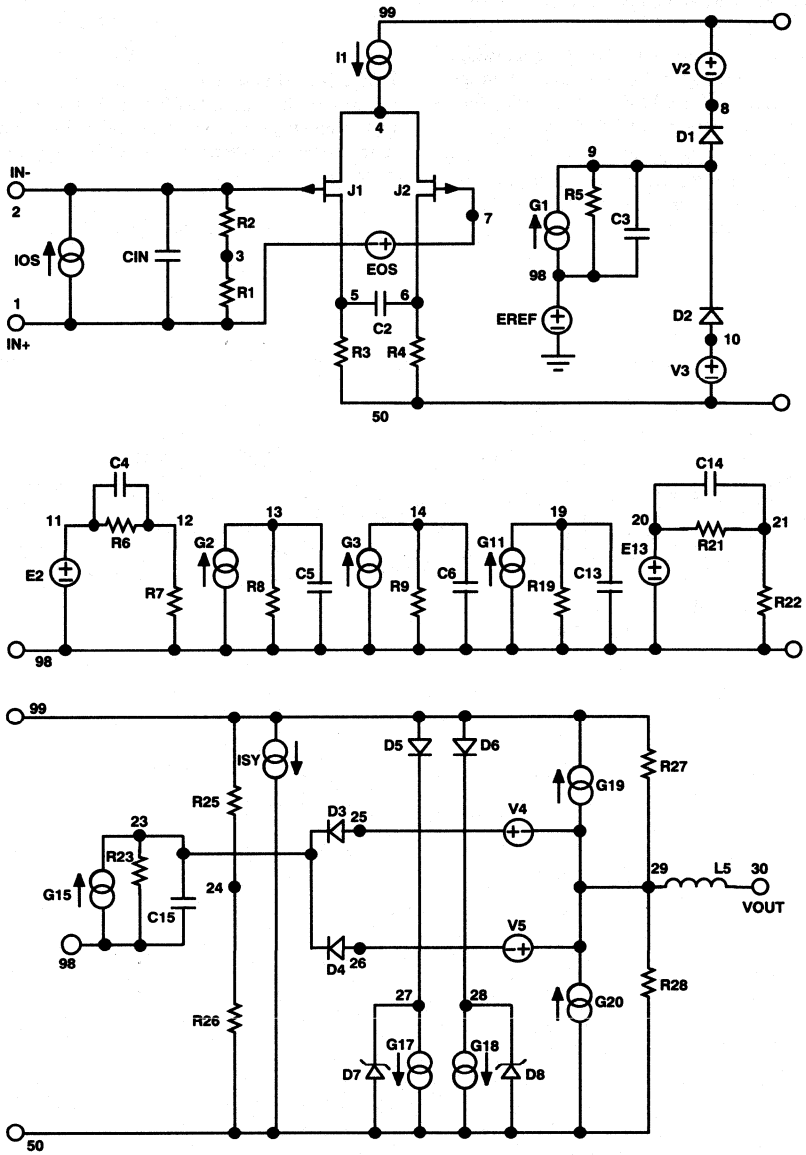


Figure 4.

OP-282 SPICE MACRO MODEL

```
* Node assignments
*                  noninverting input
*                  |  inverting input
*                  |  |  positive supply
*                  |  |  |  negative supply
*                  |  |  |  |  output
*                  |  |  |  |  |
.SUBCKT OP282      1  2  99 50 30
*
* INPUT STAGE & POLE AT 15 MHZ
*
R1      1   3   5E11
R2      2   3   5E11
R3      5   50  3871.3
R4      6   50  3871.3
CIN     1   2   5E-12
C2      5   6   1.37E-12
I1      99  4   0.1E-3
IOS     1   2   5E-13
EOS     7   1   POLY(1) 21 24 200E-6 1
J1      5   2   4          JX
J2      6   7   4          JX
*
EREF    98  0   24         0 1
*
* GAIN STAGE & POLE AT 124 HZ
*
R5      9   98  1.16E8
C3      9   98  1.11E-11
G1      98  9   5 6        2.58E-4
V2      99  8   1.2
V3      10  50  1.2
D1      9   8   DX
D2      10  9   DX
*
* NEGATIVE ZERO AT 4 MHZ
*
R6      11  12  1E6
R7      12  98  1
C4      11  12  39.8E-15
E2      11  98  9          24 1E6
*
* POLE AT 15 MHZ
*
R8      13  98  1E6
C5      13  98  10.6E-15
G2      98  13  12         24 1E-6
*
* POLE AT 15 MHZ
*
R9      14  98  1E6
C6      14  98  10.6E-15
G3      98  14  13         24 1E-6
*
* POLE AT 15 MHZ
*
R19     19  98  1E6
C13     19  98  10.6E-15
G11     98  19  14         24 1E-6
*
* COMMON-MODE GAIN NETWORK
WITH ZERO AT 11 KHZ
*
R21     20  21  1E6
R22     21  98  1
C14     20  21  14.38E-12
E13     98  20  3          24 31.62
*
* POLE AT 15 MHZ
*
R23     23  98  1E6
C15     23  98  10.6E-15
G15     98  23  19         24 1E-6
*
* OUTPUT STAGE
*
R25     24  99  5E6
R26     24  50  5E6
ISY     99  50  107E-6
R27     29  99  700
R28     29  50  700
L5      29  30  1E-8
G17     27  50  23         29 1.43E-3
G18     28  50  29         23 1.43E-3
G19     29  99  99         23 1.43E-3
G20     50  29  23         50 1.43E-3
V4      25  29  2.8
V5      29  26  3.5
D3      23  25  DX
D4      26  23  DX
D5      99  27  DX
D6      99  28  DX
D7      50  27  DY
D8      50  28  DY
*
* MODELS USED
*
.MODEL JX PJF(BETA = 3.34E-4
VTO = -2.000 IS = 3E-12)
.MODEL DX D(IS = 1E-15)
.MODEL DY D(IS = 1E-15 BV = 50)
.ENDS OP282
```

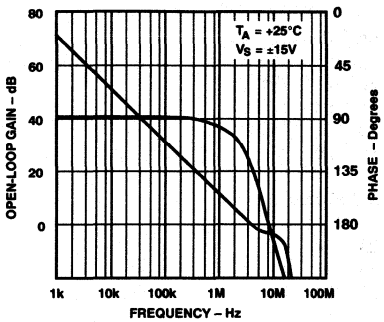


Figure 5. Open-Loop Gain, Phase vs. Frequency

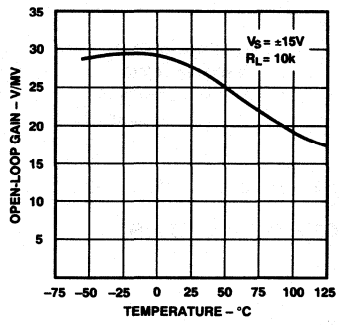


Figure 8. Open-Loop Gain (V/mV)

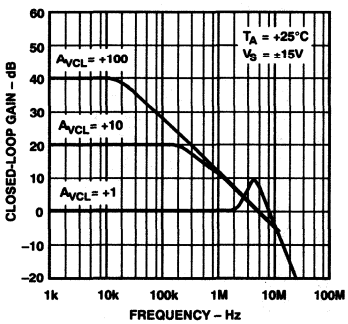


Figure 6. Closed-Loop Gain vs. Frequency

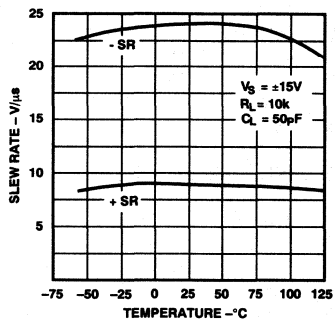


Figure 9. OP-282/OP-482 Slew Rate vs. Temperature

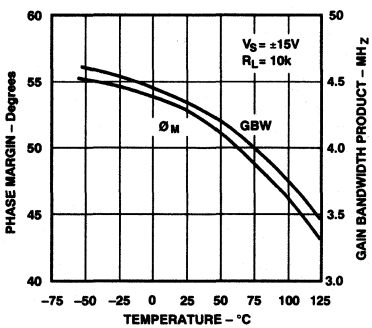


Figure 7. OP-482 Phase Margin and Gain Bandwidth Product vs. Temperature

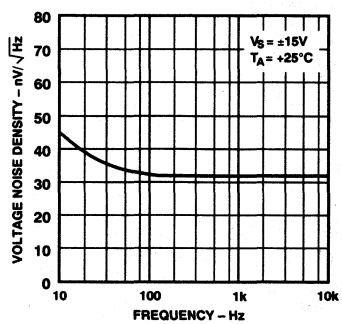


Figure 10. Voltage Noise Density vs. Frequency

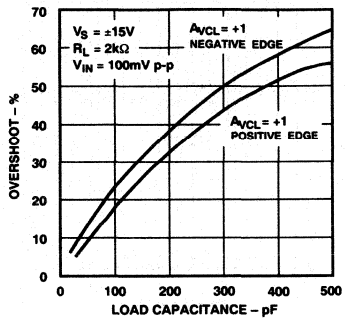


Figure 11. Small Signal Overshoot vs. Load Capacitance

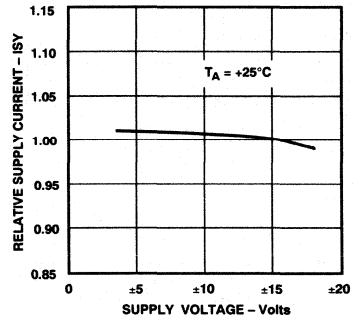


Figure 14. Relative Supply Current vs. Supply Voltage

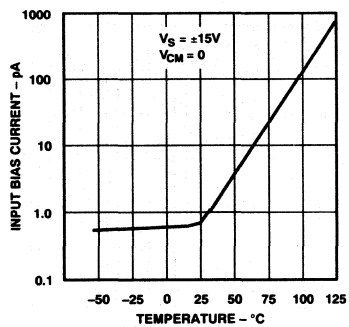


Figure 12. OP-282 Input Bias Current vs. Temperature

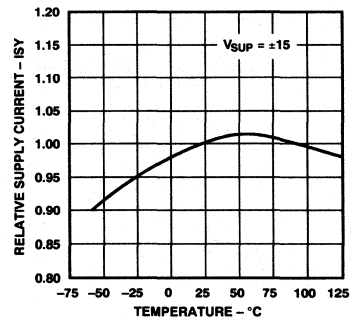


Figure 15. Relative Supply Current vs. Temperature

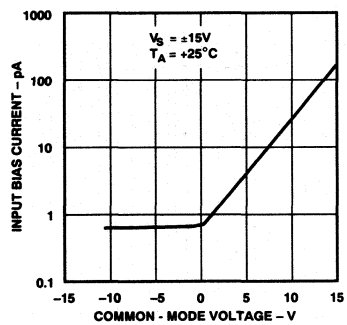


Figure 13. OP-282 Input Bias Current vs. Common-Mode Voltage

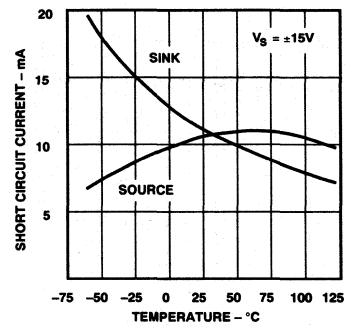


Figure 16. OP-282/OP-482 Short Circuit Current vs. Temperature

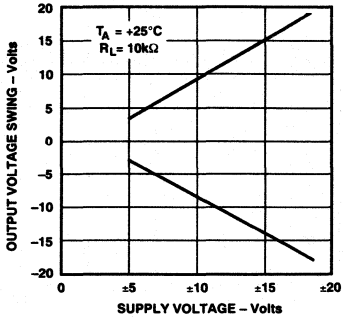


Figure 17. Output Voltage Swing vs. Supply Voltage

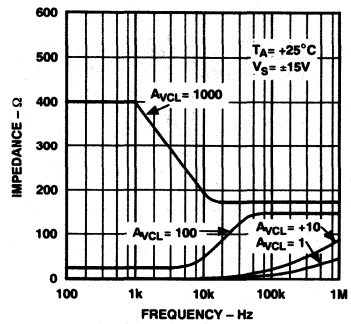


Figure 20. OP-482 Closed-Loop Output Impedance vs. Frequency

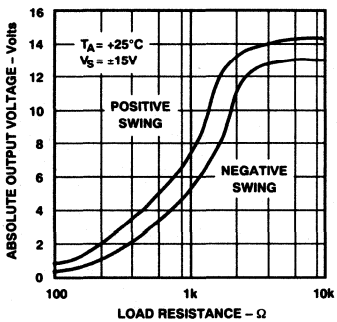


Figure 18. Maximum Output Voltage vs. Load Resistance

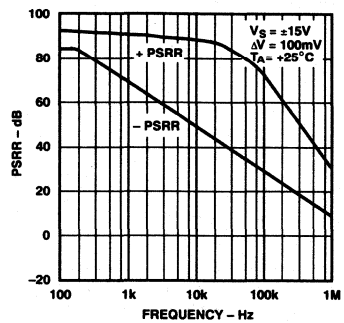


Figure 21. OP-282 Power Supply Rejection Ratio (PSRR) vs. Frequency

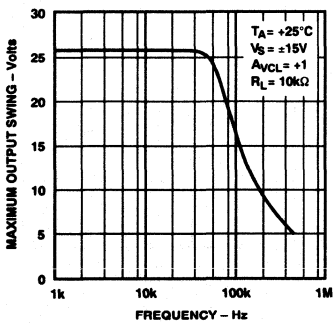


Figure 19. Maximum Output Swing vs. Frequency

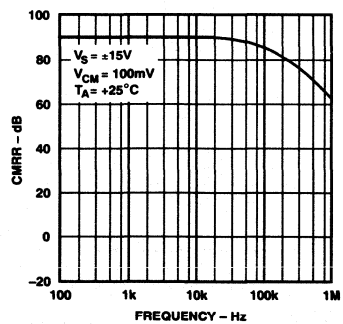


Figure 22. OP-282 Common-Mode Rejection Ratio (CMRR) vs. Frequency

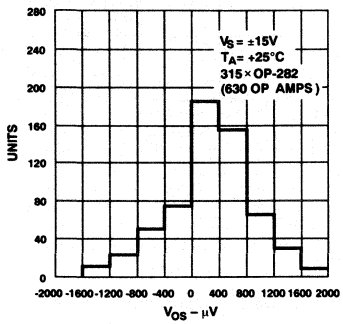


Figure 23. V_{OS} Distribution "P" Package

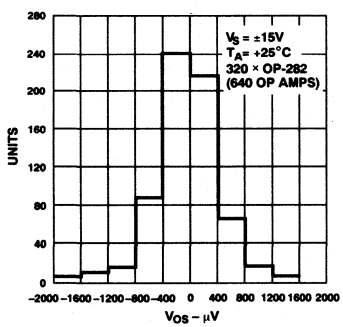


Figure 24. V_{OS} Distribution "Z" Package

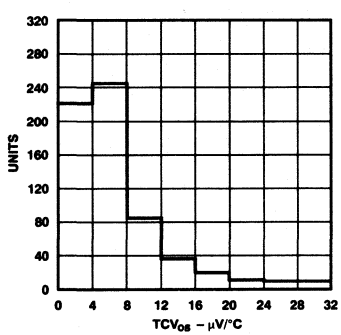


Figure 25. OP-282 TCV_{OS} (µV/°C) Distribution "P" Package

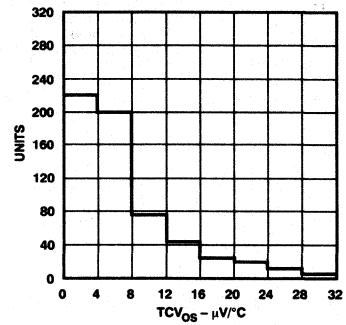


Figure 26. OP-282 TCV_{OS} (µV/°C) Distribution "Z" Package

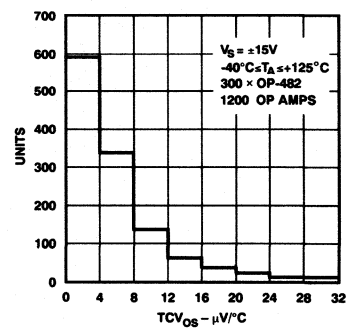


Figure 27. OP-482 TCV_{OS} Distribution "Z" Package

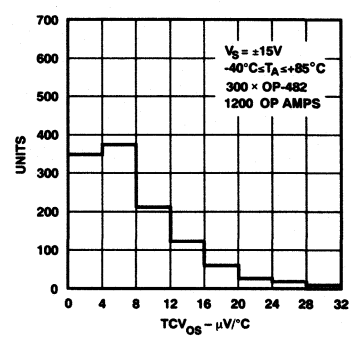


Figure 28. TCV_{OS} Distribution "P" Package

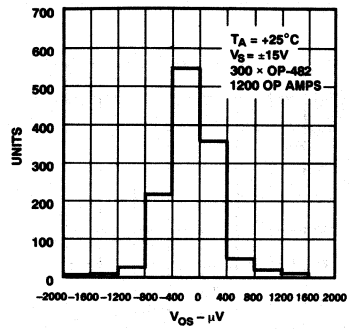


Figure 29. OP-482 V_{OS} Distribution "Z" Package

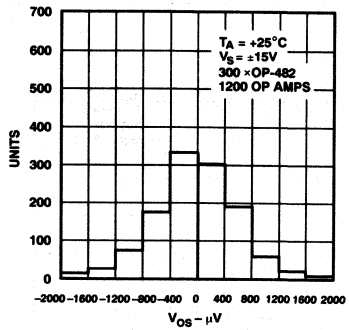


Figure 30. OP-482 V_{OS} Distribution "P" Package

Dual Bipolar/JFET, Precision Operational Amplifier

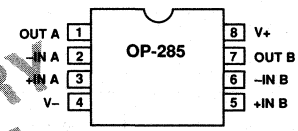
OP-285*

FEATURES
Low Offset Voltage: 250 μV
Wide Bandwidth: 8 MHz
High Slew Rate: 20 V/μs
Low Noise: 6 nV/√Hz
Low Distortion: 0.001%
Low Supply Current: 5 mA
Low Offset Current: 2 nA
Unity-Gain Stable

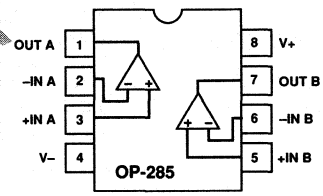
APPLICATIONS
Active Filters
Fast Amplifiers
Integrators

PIN CONNECTIONS

8-Lead Narrow-Body SOIC
(S Suffix)



8-Lead Epoxy DIP
(P Suffix)



PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The OP-285 is a precision high speed amplifier featuring the Butler Amplifier front-end. This new front-end design combines the accuracy and low noise performance of bipolar transistors with the speed of JFETs. This yields an amplifier with high slew rates, low offset and good noise performance at low supply currents. Bias currents are also low compared to bipolar designs.

The OP-285 is specified over the extended industrial (−40°C to +85°C) temperature range. OP-285s are available in plastic DIP plus SO-8 surface mount packages.

*Patents pending.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

OP-285—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			125	250	μV
Input Bias Current	I_B	V_{CM} = 0 V		150		nA
Input Offset Current	I_{OS}	V_{CM} = 0 V		2		nA
Input Voltage Range	V_{CM}		−10.5		+10.5	V
Common-Mode Rejection	CMR	V_{CM} = ±10.5 V	86			dB
Large Signal Voltage Gain	A_{VO}	R_L = 600 Ω		200		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			5		μV/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 10 kΩ	−13	±14.1	+13	V
Open Loop Output Resistance	R_{OUT}					Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ± 4.5 V to ±15 V		80		dB
Supply Current	I_{SY}	V_O = 0 V, R_L = ∞		4	5	mA
Supply Voltage Range	V_S		±4.5		±18	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		20		V/μs
Full-Power Bandwidth	BWp					kHz
Settling Time	t_S					μs
Gain Bandwidth Product	GBP			8		MHz
Total Harmonic Distortion	THD	@ 20 kHz		0.002		%
		@ 1 kHz		0.0006		%
Phase Margin	θ_0			62		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p–p	0.1 Hz to 10 Hz		1.1		μV p–p
Voltage Noise Density	e_n	f = 1 kHz		6		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		1.5		pA/√Hz

PRELIMINARY TECHNICAL DATA

Specifications subject to change without notice.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

WAFER TEST LIMITS @ V_S = ±15.0 V, T_A = +25°C unless otherwise specified.)

Parameter	Symbol	Conditions	Limit	Units
Offset Voltage	V_{OS}		250	mV max
Input Bias Current	I_B	V_{CM} = 0 V	200	nA max
Input Offset Current	I_{OS}	V_{CM} = 0 V	50	nA max
Input Voltage Range[1]			±10.5	V min
Common-Mode Rejection	CMRR	V_{CM} = ±10.5 V	86	dB min
Power Supply Rejection Ratio	PSRR	V = ±4.5 V to ±15 V	80	dB min
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ	100	V/mV min
Output Voltage Range	V_O	R_L = 10 kΩ	±13	V min
Supply Current	I_{SY}	V_O = 0 V, R_L = ∞	5	mA max

NOTE
Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.
[1]Guaranteed by CMR test.

PRELIMINARY TECHNICAL DATA

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Input Voltage[2] . . . . . ± 18 V
Differential Input Voltage[2] . . . . . ±7.5 V
Output Short-Circuit Duration . . . . . Limited
Storage Temperature Range
P, S Package . . . . . −65°C to +150°C
Operating Temperature Range
OP-285E, F . . . . . −40°C to +85°C
Junction Temperature Range
P, S Package . . . . . −65°C to +150°C
Lead Temperature Range (Soldering, 60 Sec) . . . . . +300°C

Package Type	θ_{JA}[3]	θ_{JC}	Units
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W

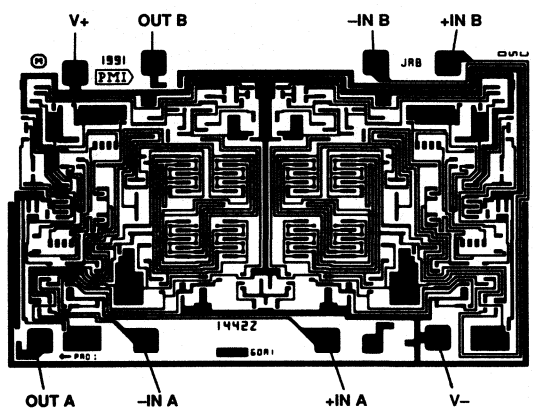
NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.
[3]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered in circuit board for SOIC package.

ORDERING GUIDE

Model	Temperature Range	Package Option*
OP285EP	−40°C to +85°C	8-Pin Plastic DIP
OP285ES	−40°C to +85°C	8-Pin SOIC
OP285FP	−40°C to +85°C	8-Pin Plastic DIP
OP285FS	−40°C to +85°C	8-Pin SOIC
OP285GBC	+25°C	DICE

*For outline information see Package Information section.

DICE CHARACTERISTICS



OP-285 Die Size 0.070 in. × 0.108 in. (7,560 sq. mils)

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ANALOG DEVICES

Precision Low-Power Micropower Dual Operational Amplifier

OP-290

FEATURES

- **Single/Dual Supply Operation ..... +1.6V to +36V**
  ..... ±0.8V to ±18V
- **True Single-Supply Operation; Input and Output Voltage Ranges Include Ground**
- **Low Supply Current (per amplifier) ..... 20μA Max**
- **High Output Drive ..... 5mA Min**
- **Low Input Offset Voltage ..... 200μV Max**
- **High Open-Loop Gain ..... 700V/mV Min**
- **Outstanding PSRR ..... 5.6μV/V Max**
- **Industry Standard 8-Pin Dual Pinout**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (mV)	PACKAGE CERDIP 8-PIN	PACKAGE PLASTIC	PACKAGE LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
200	OP290AZ*	–	OP290ARC/883	MIL
200	OP290EZ	–	–	XIND
300	OP290FZ	–	–	XIND
500	–	OP290GP	–	XIND
500	–	OP290GS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

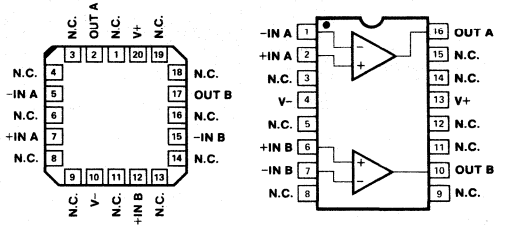
GENERAL DESCRIPTION

The OP-290 is a high performance micropower dual op amp that operates from a single supply of +1.6V to +36V or from dual supplies of ±0.8V to ±18V. Input voltage range includes the negative rail allowing the OP-290 to accommodate input signals down to ground in single supply operation. The OP-290's output swing also includes ground when operating from a single supply, enabling "zero-in, zero-out" operation.

The OP-290 draws less than 20μA of quiescent supply current per amplifier, while able to deliver over 5mA of output current to a load. Input offset voltage is below 200μV eliminating the need for external nulling. Gain exceeds 700,000 and common-mode rejection is better than 100dB. The power

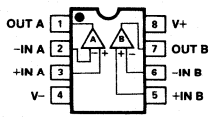
Continued

PIN CONNECTIONS



LCC (RC-Suffix)

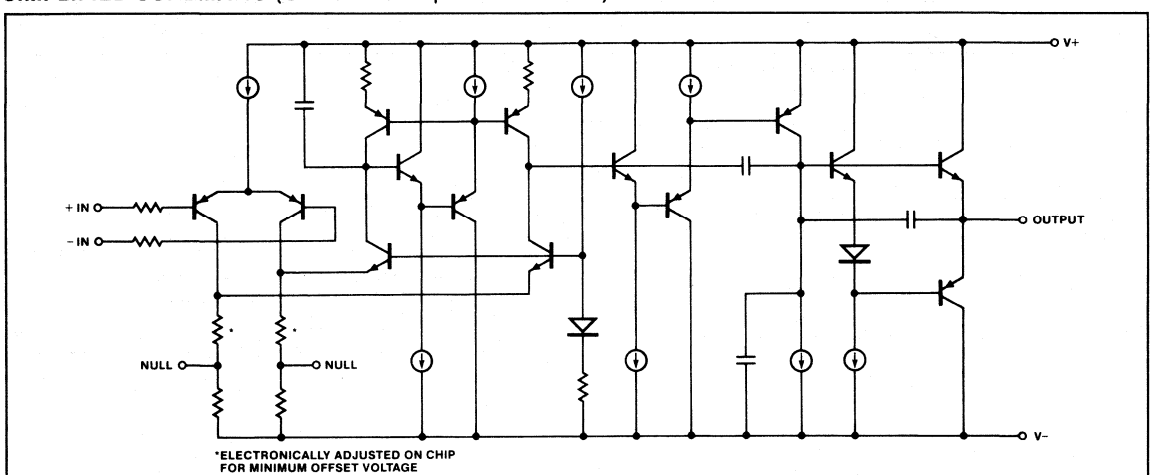
16-PIN SOL (S-Suffix)



EPOXY MINI-DIP (P-Suffix)

8-PIN HERMETIC DIP (Z-Suffix)

SIMPLIFIED SCHEMATIC (One of two amplifiers is shown.)



GENERAL DESCRIPTION *Continued*

supply rejection ratio of under 5.6μV/V minimizes offset voltage changes experienced in battery powered systems. The low offset voltage and high gain offered by the OP-290 bring precision performance to micropower applications. The minimal voltage and current requirements of the OP-290 suit it for battery and solar powered applications, such as portable instruments, remote sensors, and satellites. For a single op amp, see the OP-90; for a quad, see the OP-490.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Differential Input Voltage ..... [(V–) – 20V] to [(V+) + 20V]
Common-Mode Input Voltage
..... [(V–) – 20V] to [(V+) + 20V]
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range
P, RC, S, Z Package ..... –65°C to +150°C
Operating Temperature Range
OP-290A ..... –55°C to +125°C
OP-290E, OP-290F, OP-290G ..... –40°C to +85°C
Junction Temperature (T_J) ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
8-Pin Hermetic DIP (Z)	134	12	°C/W
8-Pin Plastic DIP (P)	96	37	°C/W
20-Contact LCC (RC)	88	33	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm1.5V$ to $\pm15V$, $T_A = +25°C$, unless otherwise noted.

			OP-290A/E			OP-290F			OP-290G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	50	200	—	75	300	—	125	500	μV
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	0.1	3	—	0.1	5	—	0.1	5	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	4.0	15	—	4.0	20	—	4.0	25	nA
Large Signal Voltage Gain	A_{VO}	$V_S = \pm15V$, $V_O = \pm10V$										
		$R_L = 100k\Omega$	700	1200	—	500	1000	—	400	800	—	V/mV
		$R_L = 10k\Omega$	350	600	—	250	500	—	200	400	—	
		$R_L = 2k\Omega$	125	250	—	100	200	—	100	200	—	
		V+ = 5V, V– = 0V, $1V < V_O < 4V$										
		$R_L = 100k\Omega$	200	400	—	125	300	—	100	250	—	
		$R_L = 10k\Omega$	100	180	—	75	140	—	70	140	—	
Input Voltage Range	IVR	V+ = 5V, V– = 0V	0/4	—	—	0/4	—	—	0/4	—	—	V
		$V_S = \pm15V$ (Note 1)	–15/13.5	—	—	–15/13.5	—	—	–15/13.5	—	—	
Output Voltage Swing	V_O	$V_S = \pm15V$										
		$R_L = 10k\Omega$	±13.5	±14.2	—	±13.5	±14.2	—	±13.5	±14.2	—	V
		$R_L = 2k\Omega$	±10.5	±11.5	—	±10.5	±11.5	—	±10.5	±11.5	—	
	V_{OH}	V+ = 5V, V– = 0V, $R_L = 2k\Omega$	4.0	4.2	—	4.0	4.2	—	4.0	4.2	—	V
	V_{OL}	V+ = 5V, V– = 0V, $R_L = 10k\Omega$	—	10	50	—	10	50	—	10	50	μV
Common-Mode Rejection	CMR	V+ = 5V, V– = 0V, $0V < V_{CM} < 4V$	90	115	—	80	100	—	80	100	—	dB
		$V_S = \pm15V$, $-15V < V_{CM} < 13.5V$	100	120	—	90	120	—	90	120	—	
Power Supply Rejection Ratio	PSRR		—	1.0	5.6	—	1.0	5.6	—	3.2	10	μV/V
Supply Current (All Amplifiers)	I_{SY}	$V_S = \pm1.5V$	—	19	30	—	19	30	—	19	30	μA
		$V_S = \pm15V$	—	25	40	—	25	40	—	25	40	
Capacitive Load Stability		$A_V = +1$, No Oscillations	—	650	—	—	650	—	—	650	—	pF
Input Noise Voltage	e_{np-p}	$f_O = 0.1Hz$ to 10Hz, $V_S = \pm15V$	—	3	—	—	3	—	—	3	—	μV_{p-p}

ELECTRICAL CHARACTERISTICS at $V_S = \pm1.5V$ to $\pm15V$, $T_A = +25°C$, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	OP-290A/E MIN	OP-290A/E TYP	OP-290A/E MAX	OP-290F MIN	OP-290F TYP	OP-290F MAX	OP-290G MIN	OP-290G TYP	OP-290G MAX	UNITS
Input Resistance Differential-Mode	R_{IN}	$V_S = \pm15V$	—	30	—	—	30	—	—	30	—	MΩ
Input Resistance Common-Mode	R_{INCM}	$V_S = \pm15V$	—	20	—	—	20	—	—	20	—	GΩ
Slew Rate	SR	$A_V = +1$ $V_S = \pm15V$	5	12	—	5	12	—	5	12	—	V/ms
Gain Bandwidth Product	GBWP	$A_V = +1$ $V_S = \pm15V$	—	20	—	—	20	—	—	20	—	kHz
Channel Separation	CS	$f_O = 10Hz$ $V_O = 20V_{p-p}$ $V_S = \pm15V$ (Note 2)	120	150	—	120	150	—	120	150	—	dB

NOTES:
1. Guaranteed by CMR test.
2. Guaranteed but not 100% tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm1.5V$ to $\pm15V$, $-55°C \le T_A \le 125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-290A MIN	OP-290A TYP	OP-290A MAX	UNITS
Input Offset Voltage	V_{OS}		—	80	500	μV
Average Input Offset Voltage Drift	TCV_{OS}	$V_S = \pm15V$	—	0.3	3	μV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	0.1	5	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	4.2	20	nA
Large Signal Voltage Gain	A_{VO}	$V_S = \pm15V$, $V_O = \pm10V$ $R_L = 100k\Omega$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	225 125 50	400 240 110	— — —	V/mV
		V+ = 5V, V− = 0V, $1V < V_O < 4V$ $R_L = 100k\Omega$ $R_L = 10k\Omega$	100 50	200 110	— —	
Input Voltage Range	IVR	V+ = 5V, V− = 0V (Note 1) $V_S = \pm15V$	0/3.5 −15/13.5	— —	— —	V
Output Voltage Swing	V_O	$V_S = \pm15V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	±13 ±10	±14.1 ±11	— —	V
	V_{OH}	V+ = 5V, V− = 0V $R_L = 2k\Omega$	3.9	4.1	—	V
	V_{OL}	V+ = 5V, V− = 0V $R_L = 10k\Omega$	—	10	100	μV
Common-Mode Rejection	CMR	V+ = 5V, V− = 0V, $0V < V_{CM} < 3.5V$ $V_S = \pm15V$, $-15V < V_{CM} < 13.5V$	80 90	105 115	— —	dB
Power Supply Rejection Ratio	PSRR		—	3.2	10	μV/V
Supply Current (All Amplifiers)	I_{SY}	$V_S = \pm1.5V$ $V_S = \pm15V$	— —	30 38	50 60	μA

NOTE:
1. Guaranteed by CMR test.

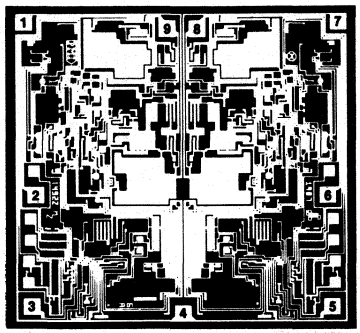
OP-290

ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5V$ to $\pm 15V$, $-40°C \leq T_A \leq 85°C$ for OP-290E/F/G, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-290E MIN	OP-290E TYP	OP-290E MAX	OP-290F MIN	OP-290F TYP	OP-290F MAX	OP-290G MIN	OP-290G TYP	OP-290G MAX	UNITS
Input Offset Voltage	V_{OS}		—	70	400	—	115	600	—	200	750	μV
Average Input Offset Voltage Drift	TCV_{OS}	$V_S = \pm 15V$	—	0.3	3	—	0.6	5	—	1.2	—	μV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	0.1	3	—	0.1	5	—	0.1	7	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	4.2	15	—	4.2	20	—	4.2	25	nA
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_O = \pm 10V$										V/mV
		$R_L = 100k\Omega$	500	800	—	350	700	—	300	600	—	
		$R_L = 10k\Omega$	250	400	—	175	350	—	150	250	—	
		$R_L = 2k\Omega$	100	200	—	75	150	—	75	125	—	
		V+ = 5V, V− = 0V, $1V < V_O < 4V$										
		$R_L = 100k\Omega$	150	280	—	100	220	—	80	160	—	
		$R_L = 10k\Omega$	75	140	—	50	110	—	40	90	—	
Input Voltage Range	IVR	V+ = 5V, V− = 0V	0/3.5	—	—	0/3.5	—	—	0/3.5	—	—	V
		$V_S = \pm 15V$ (Note 1)	−15/13.5	—	—	−15/13.5	—	—	−15/13.5	—	—	
Output Voltage Swing	V_O	$V_S = \pm 15V$										V
		$R_L = 10k\Omega$	±13	±14	—	±13	±14	—	±13	±14	—	
		$R_L = 2k\Omega$	±10	±11	—	±10	±11	—	±10	±11	—	
	V_{OH}	V+ = 5V, V− = 0V, $R_L = 2k\Omega$	3.9	4.1	—	3.9	4.1	—	3.9	4.1	—	V
	V_{OL}	V+ = 5V, V− = 0V, $R_L = 10k\Omega$	—	10	100	—	10	100	—	10	100	μV
Common-Mode Rejection	CMR	V+ = 5V, V− = 0V, $0V < V_{CM} < 3.5V$	85	105	—	80	100	—	80	100	—	dB
		$V_S = \pm 15V$, $-15V < V_{CM} < 13.5V$	95	115	—	90	110	—	90	110	—	
Power Supply Rejection Ratio	PSRR		—	3.2	7.5	—	5.6	10	—	5.6	15	μV/V
Supply Current (All Amplifiers)	I_{SY}	$V_S = \pm 1.5V$	—	24	50	—	24	50	—	24	50	μA
		$V_S = \pm 15V$	—	31	60	—	31	60	—	31	60	

NOTE:
1. Guaranteed by CMR test.

DICE CHARACTERISTICS



DIE SIZE 0.109 × 0.104 inch, 11,336 sq. mils
(2.77 × 1.70mm, 4.71 sq. mm)

1. OUT A
2. −IN A
3. +IN A
4. V−
5. +IN B
6. −IN B
7. OUT B
8. V+ B
9. V+ A

2

WAFER TEST LIMITS at $V_S = \pm 1.5V$ to $\pm 15V$, $T_A = 25°C$, unless otherwise noted.

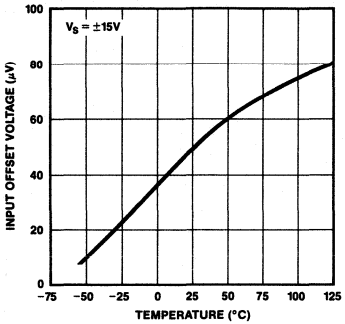
PARAMETER	SYMBOL	CONDITIONS	OP-290GBC LIMIT	UNITS
Input Offset Voltage	V_{OS}		300	μV MAX
Input Offset Current	I_{OS}	$V_{CM} = 0V$	5	nA MAX
Input Bias Current	I_B	$V_{CM} = 0V$	20	nA MAX
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_O = \pm 10V$ $R_L = 100k\Omega$ $R_L = 10k\Omega$	500 250	V/mV MIN
		V+ = 5V, V− = 0V, $1V < V_O < 4V$ $R_L = 100k\Omega$	125	V/mV MIN
Input Voltage Range	IVR	V+ = 5V, V− = 0V $V_S = \pm 15V$ (Note 1)	0/4 −15/13.5	V MIN
Output Voltage Swing	V_O	$V_S = \pm 15V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	±13.5 ±10.5	V MIN
	V_{OH}	V+ = 5V, V− = 0V $R_L = 2k\Omega$	4.0	V MIN
	V_{OL}	V+ = 5V, V− = 0V $R_L = 10k\Omega$	50	μV MAX
Common-Mode Rejection	CMR	V+ = 5V, V− = 0V, $0V < V_{CM} < 4V$ $V_S = \pm 15V$, $-15V < V_{CM} < 13.5V$	80 90	dB MIN
Power Supply Rejection Ratio	PSRR		5.6	μV/V MAX
Supply Current (All Amplifiers)	I_{SY}	$V_S = \pm 15V$	40	μA MAX

NOTES:
1. Guaranteed by CMR test.

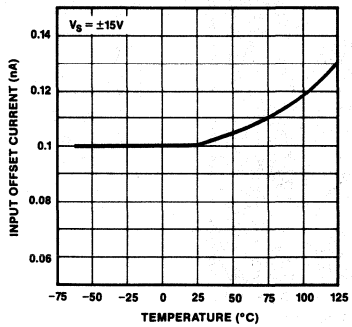
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

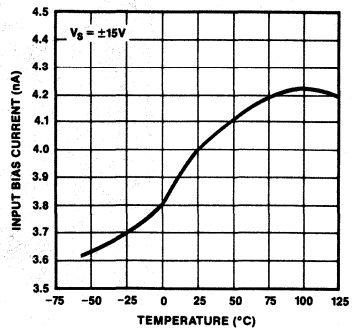
INPUT OFFSET VOLTAGE vs TEMPERATURE



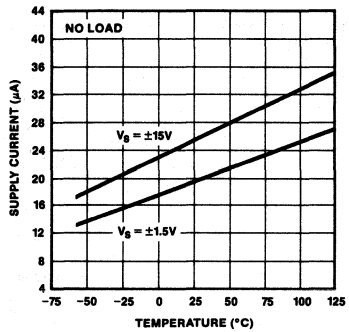
INPUT OFFSET CURRENT vs TEMPERATURE



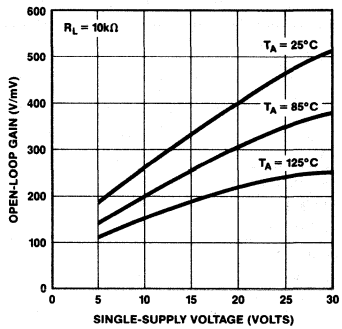
INPUT BIAS CURRENT vs TEMPERATURE



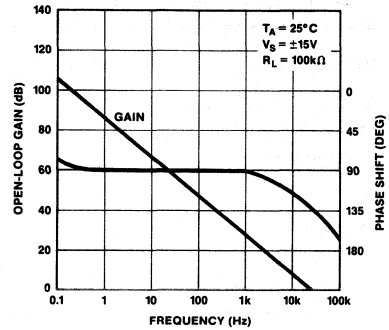
SUPPLY CURRENT vs TEMPERATURE



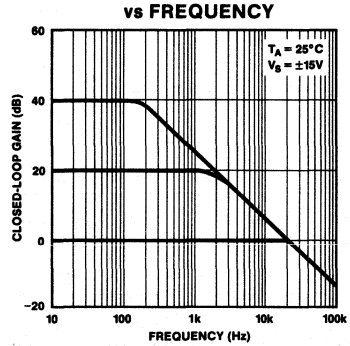
OPEN-LOOP GAIN vs SINGLE-SUPPLY VOLTAGE



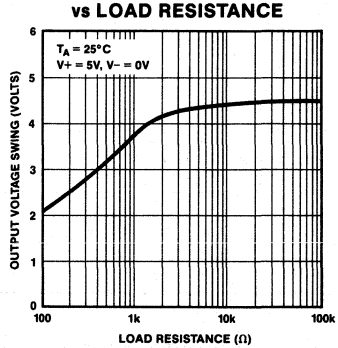
OPEN-LOOP GAIN AND PHASE SHIFT vs FREQUENCY



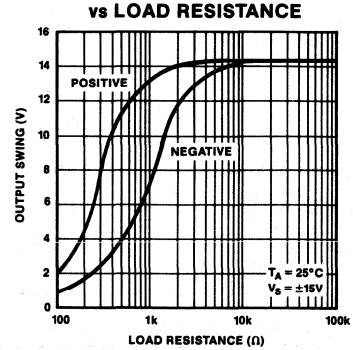
CLOSED-LOOP GAIN vs FREQUENCY



OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

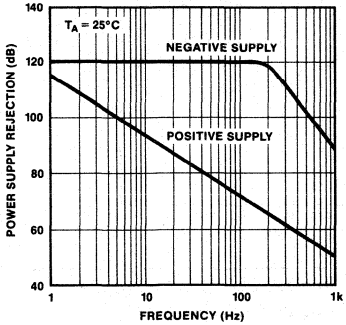


OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

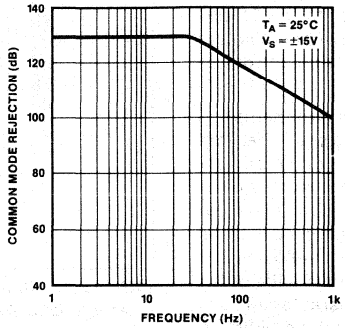


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

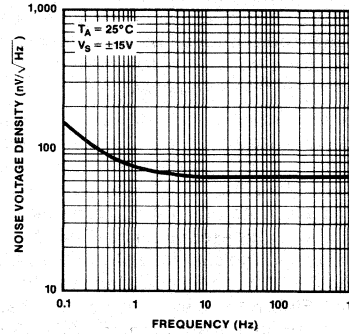
POWER SUPPLY REJECTION vs FREQUENCY



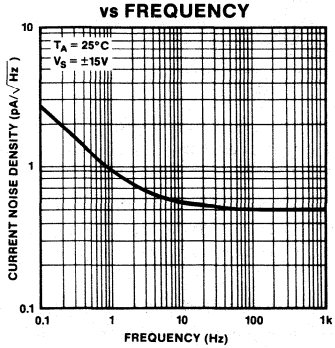
COMMON-MODE REJECTION vs FREQUENCY



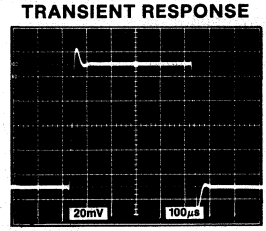
NOISE VOLTAGE DENSITY vs FREQUENCY



CURRENT NOISE DENSITY vs FREQUENCY

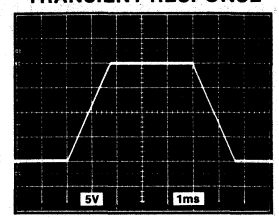


SMALL-SIGNAL TRANSIENT RESPONSE



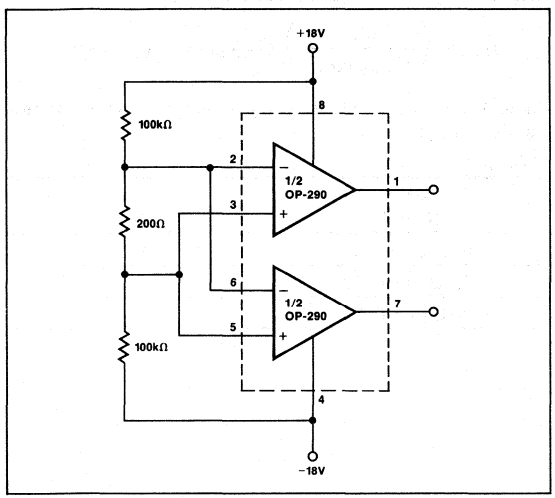
T_A = 25°C
V_S = ±15V
A_V = +1
R_L = 10kΩ
C_L = 500pF

LARGE-SIGNAL TRANSIENT RESPONSE

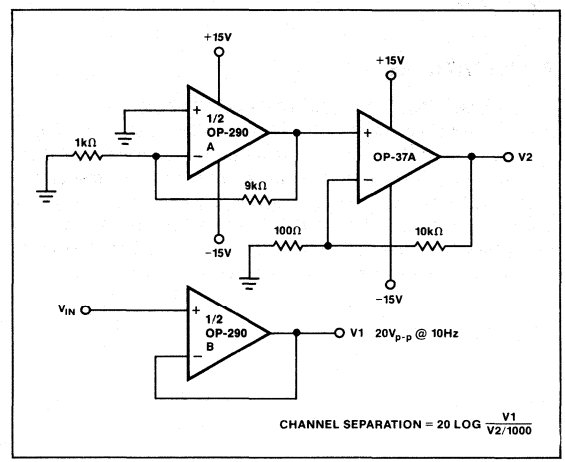


T_A = 25°C
V_S = ±15V
A_V = +1
R_L = 10kΩ
C_L = 500pF

BURN-IN CIRCUIT



CHANNEL SEPARATION TEST CIRCUIT



APPLICATIONS INFORMATION

BATTERY-POWERED APPLICATIONS

The OP-290 can be operated on a minimum supply voltage of +1.6V, or with dual supplies of ±0.8V, and draws only 19μA of supply current. In many battery-powered circuits, the OP-290 can be continuously operated for thousands of hours before requiring battery replacement, reducing equipment downtime and operating cost.

High-performance portable equipment and instruments frequently use lithium cells because of their long shelf-life, light weight, and high energy density relative to older primary cells. Most lithium cells have a nominal output voltage of 3V and are noted for a flat discharge characteristic. The low supply voltage requirement of the OP-290, combined with the flat discharge characteristic of the lithium cell, indicates that the OP-290 can be operated over the entire useful life of the cell. Figure 1 shows the typical discharge characteristic of a 1Ah lithium cell powering an OP-290 with each amplifier, in turn, driving full output swing into a 100kΩ load.

INPUT VOLTAGE PROTECTION

The OP-290 uses a PNP input stage with protection resistors in series with the inverting and noninverting inputs. The high breakdown of the PNP transistors coupled with the protection resistors provides a large amount of input protection, allowing the inputs to be taken 20V beyond either supply without damaging the amplifier.

SINGLE-SUPPLY OUTPUT VOLTAGE RANGE

In single-supply operation the OP-290's input and output ranges include ground. This allows true "zero-in, zero-out" operation. The output stage provides an active pull-down to around 0.8V above ground. Below this level, a load resistance of up to 1MΩ to ground is required to pull the output down to zero.

In the region from ground to 0.8V the OP-290 has voltage gain equal to the data sheet specification. Output current source capability is maintained over the entire voltage range including ground.

APPLICATIONS

TEMPERATURE TO 4-20mA TRANSMITTER

A simple temperature to 4-20mA transmitter is shown in Figure 2. After calibration, the transmitter is accurate to ±0.5°C over the −50°C to +150°C temperature range. The transmitter operates from +8V to +40V with supply rejection better than 3ppm/V. One half of the OP-290 is used to buffer the V_{TEMP} pin, while the other half regulates the output current to satisfy the current summation at its noninverting input:

$$I_{OUT} = \frac{V_{TEMP}(R_6 + R_7)}{R_2 R_{10}} - V_{SET}\left(\frac{R_2 + R_6 + R_7}{R_2 R_{10}}\right)$$

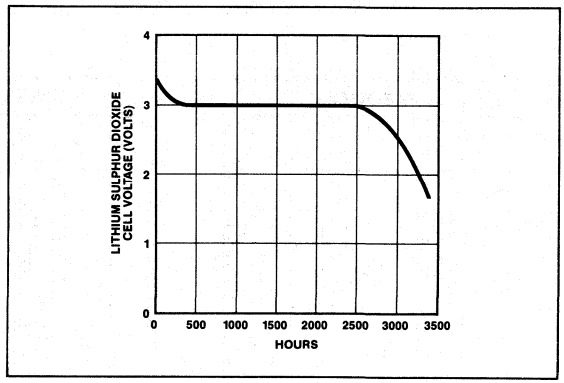


FIGURE 1: *Lithium Sulphur Dioxide Cell Discharge Characteristic With OP-290 and 100kΩ Loads*

The change in output current with temperature is the derivative of the transfer function:

$$\frac{\Delta I_{OUT}}{\Delta T} = \frac{\frac{\Delta V_{TEMP}}{\Delta T}(R_6 + R_7)}{R_2 R_{10}}$$

From the formulas, it can be seen that if the span trim is adjusted before the zero trim, the two trims are not interactive, which greatly simplifies the calibration procedure.

Calibration of the transmitter is simple. First, the slope of the output current versus temperature is calibrated by adjusting the span trim, R_7. A couple of iterations may be required to be sure the slope is correct.

Once the span trim has been completed, the zero trim can be made. Remember, that adjusting the offset trim will not affect the gain.

The offset trim can be set at any known temperature by adjusting R_5 until the output current equals:

$$I_{OUT} = \left(\frac{\Delta I_{FS}}{\Delta T_{OPERATING}}\right)(T_{AMBIENT} - T_{MIN}) + 4mA$$

Table 1 shows the values of R_6 required for various temperature ranges.

TABLE 1

TEMP RANGE	R_6
0°C to +70°C	10k
−40°C to +85°C	6.2k
−55°C to +150°C	3k

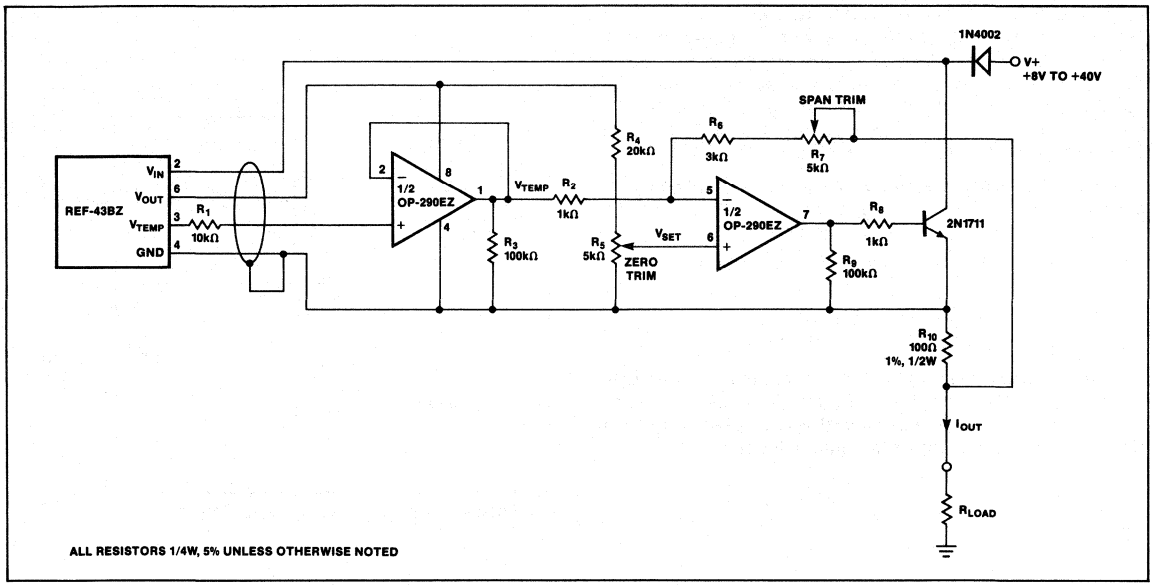


FIGURE 2: *Temperature to 4-20mA Transmitter*

VARIABLE SLEW RATE FILTER

The circuit shown in Figure 3 can be used to remove pulse noise from an input signal without limiting the response rate to a genuine signal. The non-linear filter has use in applications where the input signal of interest is known to have physical limitations. An example of this is a transducer output where a change of temperature or pressure cannot exceed a certain rate due to physical limitations of the environment. The filter consists of a comparator which drives an integrator. The comparator compares the input voltage to the output voltage and forces the integrator output to equal the input voltage. A_1 acts as a comparator with its output high or low. Diodes D_1 and D_2 clamp the voltage across R_3 forcing a constant current to flow in or out of C_2. R_3, C_2 and A_2 form an integrator with A_2's output slewing at a maximum rate of:

$$\text{Maximum slew rate} = \frac{V_D}{R_3C_2} \approx \frac{0.6V}{R_3C_2}$$

For an input voltage slewing at a rate under this maximum slew rate, the output simply follows the input with A_1 operating in its linear region.

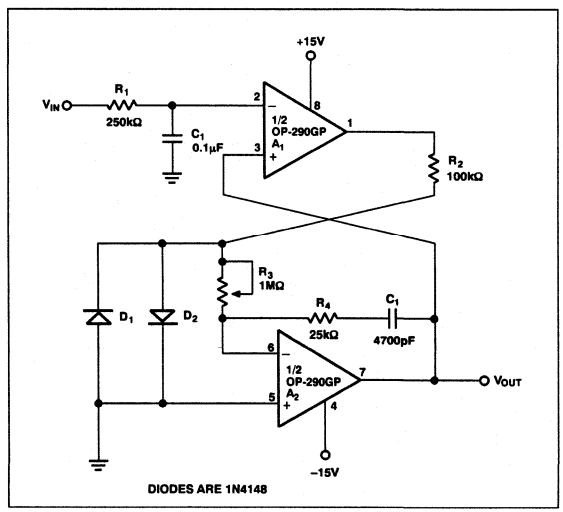


FIGURE 3: *Variable Slew Rate Filter*

LOW OVERHEAD VOLTAGE REFERENCE

Figure 4 shows a voltage reference which requires only 0.1V of overhead voltage. As shown, the reference provides a stable +4.5V output with a +4.6V to +36V supply. Output voltage drift is only 12ppm/°C. Line regulation of the reference is under 5μV/V with load regulation better than 10μV/mA with up to 50mA of output current.

The REF-43 provides a stable 2.5V which is multiplied by the OP-290. The PNP output transistor enables the output voltage to approach the supply voltage.

Resistors R_1 and R_2 determine the output voltage:

$$V_{OUT} = 2.5V\left(1 + \frac{R_2}{R_1}\right)$$

The 200Ω variable resistor is used to trim the output voltage. For the lowest temperature drift, parallel resistors can be used in place of the variable resistor and taken out of the circuit as required to adjust the output voltage.

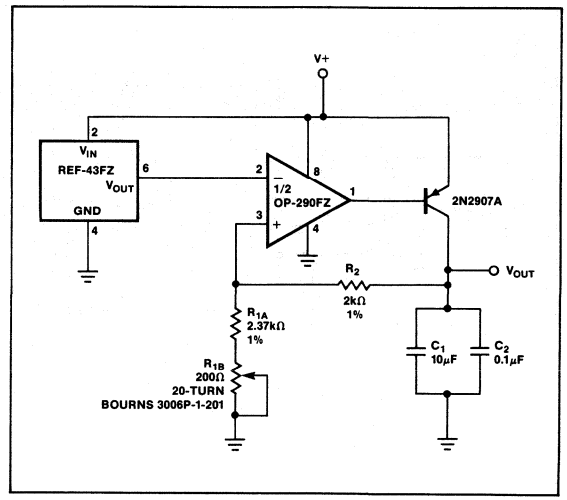


FIGURE 4: *Low Overhead Voltage Reference*

ANALOG DEVICES

Rail-to-Rail Operational Amplifier

OP-295/OP-495

FEATURES

Rail-to-Rail Output Swing
Single Supply Operation, +3 V to 36 V
Low Offset Voltage: 200 μV
Gain Bandwidth Product: 80 kHz
High Open-Loop Gain: 1000 V/mV
Unity Gain Stable
Low Power

APPLICATIONS

Battery Operated Instrumentation
Servo Amplifiers
Actuator Drives
Sensor Conditioners
Power Supply Control

PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

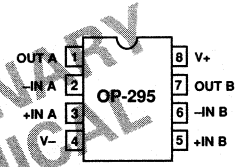
Rail-to-rail output swing is the key feature of the OP-295 BiCMOS dual operational amplifier. A quad version, the OP-495, is also available. A bipolar front end gives improved noise performance over CMOS designs. Both input and output ranges include the negative supply providing the user "zero-in/zero-out" capability. For users of 3 volt systems such as lithium batteries, the OP-295/OP-495 is specified for three volt operation.

Maximum offset voltage is specified at 200 μV for +5 volt operation, and the open-loop gain is a minimum of 500 V/mV, giving the user performance that can be used to implement high accuracy systems even in single supply designs.

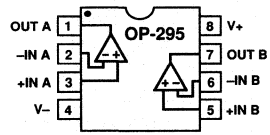
The ability to swing rail-to-rail and supply ±15 mA to the load makes the OP-295 an ideal driver for power transistors and "H" bridges. This allows designs to achieve higher efficiencies and transfer more power to the load than previously possible without the use of discrete components. For applications that require driving inductive loads, such as transformers, increases in efficiency are also possible. Stability while driving capacitive loads is another benefit of this design over CMOS rail-to-rail amplifiers.

PIN CONNECTIONS

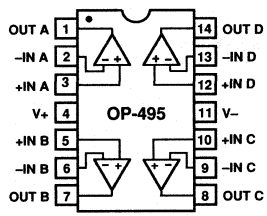
8-Lead Narrow-Body SOIC (S Suffix)



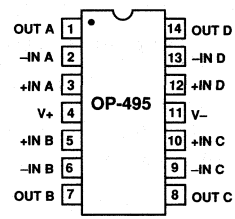
8-Lead Epoxy DIP (P Suffix)



14-Lead Epoxy DIP (P Suffix)



14-Lead Narrow-Body SOIC (S Suffix)



The OP-295/OP-495 is specified over the extended industrial (−40°C to +85°C) temperature range. OP-295s are available in 8-pin plastic and ceramic DIP plus SOIC-8 surface mount packages, and the OP-495 is available in similar 14-pin packages. Contact your local sales office for MIL-STD-883 data sheet.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

OP-295/OP-495—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			300	500	μV
Input Bias Current	I_B	V_{CM} = 0V		6	15	nA
Input Offset Current	I_{OS}	V_{CM} = 0V		1	2	nA
Input Voltage Range	V_{CM}		−15		+13.5	V
Common-Mode Rejection	CMR	−15 V ≤ V_{CM} ≤ 13.5 V	86	100		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ	500	1000		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			<10		μV/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = ∞	−15		15	V
Output Voltage Swing	V_O	R_L = 100 kΩ	−14.95		14.95	V
Output Voltage Swing	V_O	R_L = 10 kΩ	−14.85		14.85	V
Output Current	I_{OUT}		−15	±23	+15	mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±3 V to ±15 V	86	100		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V, R_L = ∞		125	175	μA
Supply Voltage Range	V_S		+3		+36	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		0.04		V/μs
Full-Power Bandwidth	FPBW					kHz
Gain Bandwidth Product	GBP			80		kHz
Phase Margin	θ_O			70		Degrees

PRELIMINARY TECHNICAL DATA

ELECTRICAL CHARACTERISTICS (@ V_S = +5.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			50	200	μV
Input Bias Current	I_B	V_{CM} = 0 V		7	15	nA
Input Offset Current	I_{OS}	V_{CM} = 0 V		0.7	2	nA
Input Voltage Range	V_{CM}		0		+4	V
Common-Mode Rejection	CMR	0 V ≤ V_{CM} ≤ 3.5 V	86			dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ		5000		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$					μV/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = ∞	−0		5	V
Output Voltage Swing	V_O	R_L = 100 kΩ	−0	5.0	4.98	V
Output Voltage Swing	V_O	R_L = 10 kΩ	−0	4.95	4.85	V
Output Current	I_{OUT}		−10	+15/−18	+10	mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = +5 V ≤ V_S ≤ +30 V	86	100		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V, R_L = ∞		100	150	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		0.03		V/μs
Full-Power Bandwidth	FPBW					kHz
Gain Bandwidth Product	GBP			85		kHz
Phase Margin	θ_O					Degrees
NOISE PERFORMANCE						
Voltage Noise	e_N p–p	0.1 Hz to 10 Hz				μV p–p
Voltage Noise Density	e_N	f = 1 kHz				nV/√Hz
Current Noise Density	i_N	f = 1 kHz				pA/√Hz

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ELECTRICAL CHARACTERISTICS (@ V_S = +3.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			200	500	μV
Input Bias Current	I_B	V_{CM} = 0 V		10		nA
Input Offset Current	I_{OS}	V_{CM} = 0 V		2		nA
Input Voltage Range	V_{CM}		0		+2	V
Common-Mode Rejection	CMR	0 V ≤ V_{CM} ≤ 1.5 V	86			dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ		2000		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$					μV/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = ∞	−0		3	V
Output Voltage Swing	V_O	R_L = 100 kΩ	−0		2.98	V
Output Voltage Swing	V_O	R_L = 10 kΩ	−0		2.85	V
Output Current	I_{OUT}		−10		+10	mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = +3 V ≤ V_S ≤ +5 V		100		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V, R_L = ∞		400		μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		0.03		V/μs
Full-Power Bandwidth	FPBW					kHz
Gain Bandwidth Product	GBP			85		kHz
Phase Margin	θ_O					Degrees
NOISE PERFORMANCE						
Voltage Noise	e_N p–p	0.1 Hz to 10 Hz				μV p–p
Voltage Noise Density	e_N	f = 1 kHz				nV/√Hz
Current Noise Density	i_N	f = 1 kHz				pA/√Hz

PRELIMINARY TECHNICAL DATA

WAFER TEST LIMITS (@ V_S = ±5.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Limit	Units
Offset Voltage	V_{OS}		250	μV max
Input Bias Current	I_B	V_{CM} = 0 V	15	nA max
Input Offset Current	I_{OS}	V_{CM} = 0 V	2	nA max
Input Voltage Range[1]			0 to +4	V min
Common-Mode Rejection	CMRR	V_{CM} = ±11 V	86	dB min
Power Supply Rejection Ratio	PSRR	V = ±3 to ±15 V	86	μV/V
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ	500	V/mV min
Output Voltage Range	V_O	R_L = 10 kΩ	4.85	V min
Supply Current/Amplifier	I_{SY}	V_O = 0 V, R_L = ∞	150	μA max

NOTES
Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.
[1]Guaranteed by CMR test.

Specifications subject to change without notice.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

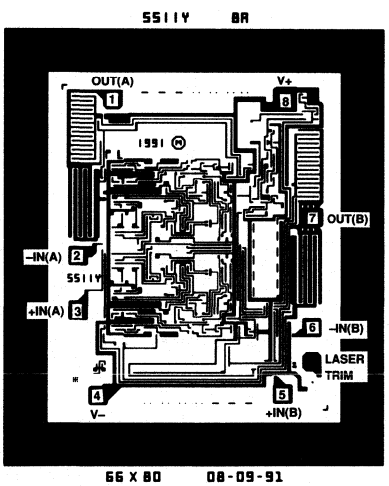
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Input Voltage[2] . . . . . ±18 V
Differential Input Voltage[2] . . . . . 36 V
Output Short-Circuit Duration . . . . . Indefinite
Storage Temperature Range
  Y Package . . . . . −65°C to +175°C
  P, S Package . . . . . −65°C to +150°C
Operating Temperature Range
  OP-295A . . . . . −55°C to +125°C
  OP-295G . . . . . −40°C to +85°C
Junction Temperature Range
  Z Package . . . . . −65°C to +175°C
  P, S Package . . . . . −65°C to +150°C
Lead Temperature Range (Soldering, 60 Sec) . . . . . +300°C

Package Type	θ_{JA}[3]	θ_{JC}	Units
8-Pin Cerdip (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W
14-Pin Cerdip (Y)	108	16	°C/W
14-Pin Plastic DIP (P)	83	39	°C/W
14-Pin SOIC (S)	120	36	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.
[3]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered in circuit board for SOIC package.

DICE CHARACTERISTICS



OP-295 Die Size 0.066 × 0.080 inch, 5,280 sq. mils

ORDERING GUIDE

Model	Temperature Range	Package Option*
OP295AZ/883	−55°C to +125°C	8-Pin Cerdip
OP295GP	−40°C to +85°C	8-Pin Plastic DIP
OP295GS	−40°C to +85°C	8-Pin SOIC
OP295GBC	+25°C	DICE
OP495AZ/883	−55°C to +125°C	14-Pin Cerdip
OP495GP	−40°C to +85°C	14-Pin Plastic DIP
OP495GS	−40°C to +85°C	14-Pin SOIC
OP495GBC	+25°C	DICE

*For outline information see Package Information section.

PRELIMINARY TECHNICAL DATA

APPLICATIONS

Low Drop-out Reference

The OP-295 can be used to gain up a 2.5 V or other low voltage reference to 4.5 volts for use with high resolution A/D converters that operate from +5 volt only supplies. The circuit in Figure 1 will supply up to 10 mA. Its no-load drop-out voltage is only 20 mV. This circuit will supply over 3.5 mA with a +5 volt supply.

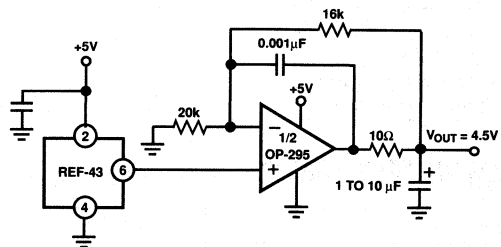
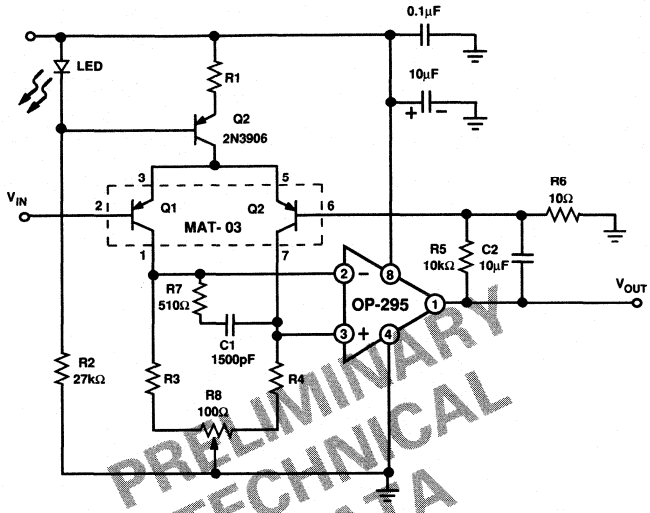


Figure 1. 4.5 V Low Drop-Out Reference

Low Noise, Single Supply Preamplifier

The characteristics of low noise and single supply are not easily available together in a monolithic op amp. If a device has single supply operation, its noise is typically on the order of 30 to 60 nV/$\sqrt{\text{Hz}}$. On the other hand, if the part has noise on the order of 5 nV/$\sqrt{\text{Hz}}$ or less, then its input voltage range and output voltage range are typically at least a few volts from the negative supply. The circuit in Figure 2 uses a single supply op amp (OP-295) and a discrete PNP matched transistor pair (MAT-03) to achieve true zero-in/zero-out single supply operation with an input voltage noise of 3.1 nV/$\sqrt{\text{Hz}}$ at 100 Hz. R5 and R6 yield a gain of 1000, making this circuit ideal for maximizing dynamic range when amplifying low level signals in single supply. The OP-295 provides rail-to-rail output swings allowing this circuit to operate with 0 V to 5 V outputs. Only half of the OP-295 is used leaving an additional op amp to be used elsewhere.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.



PRELIMINARY TECHNICAL DATA

Figure 2. Low Noise Single Supply Preamplifier

The input noise is controlled by the MAT-03 transistor pair and its collector current level. Increasing the collector current reduces the voltage noise. This particular circuit was tested with 1.85 mA and 0.5 mA of current. Under these two cases, the input voltage noise was 3.1 nV/$\sqrt{Hz}$ and 10 nV/$\sqrt{Hz}$, respectively. The high collector currents do lead to a trade-off in supply current, bias current, and current noise. All of these parameters will increase with increasing collector current. For example, typically the MAT-03 has an h_{FE} = 165. This leads to bias current of 11 μA and 3 μA, respectively. Based on high bias currents, this circuit is best suited for applications with low source impedances such as magnetic pickups or low impedance strain gages. Furthermore, a high source impedance will degrade the noise performance. For example, a 1 kΩ resistor generates 4 nV/$\sqrt{Hz}$ of broadband noise, which is already greater than the preamp.

The collector current is set by R1 in combination with the LED and Q2. The LED is a 1.6 V "Zener" that has temperature coefficient close to that of Q2's base-emitter junction, which provides a constant 1.0 V drop across R1. With R1 equal to 270 Ω, the tail current is 3.7 mA, and the collector current is half that or 1.85 mA. The value of R1 can be altered to adjust the collector current. Whenever R1 is changed, R3 and R4 should also be adjusted. To maintain a common-mode input range that includes ground, the collectors of the Q1 and Q2 should not go above 0.5 V, otherwise they could saturate. Thus, R3 and R4 must be small enough to prevent this condition. Their values and the overall performance for two different values of R1 are summarized in Table I. Lastly, the potentiometer, R8, is needed to adjust the offset voltage to null it to zero. Similar performance can be obtained using an OP-90 as the output amplifier with a savings of about 185 μA of supply current. However, the output swing will not include the positive rail, and the bandwidth will reduce to approximately 250 Hz.

Table I. Preamplifier Performance

	I_C 1.85 mA	0.5 mA
R1	270Ω	1.0 kΩ
R3, R4	200 Ω	910 Ω
e_N 100 Hz	3.15 nV/$\sqrt{Hz}$	8.6 nV/$\sqrt{Hz}$
e_N 10 Hz	4.2 nV/$\sqrt{Hz}$	10.2 nV/$\sqrt{Hz}$
I_{S4}	4.0 mA	1.3 mA
I_B	11 μA	3 μA
BW	1 kHz	1 kHz
A_{CL}	1000	1000

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Dual Low Bias Current Precision Operational Amplifier

OP-297

FEATURES

- Precision Performance in Standard SO-8 Pinout
- Low Offset Voltage ..... 50μV Max
- Low Offset Voltage Drift ..... 0.6μV/°C Max
- Very Low Bias Current
  - +25°C ..... 100pA Max
  - –55°C to +125°C ..... 450pA Max
- Very High Open-Loop Gain ..... 2000V/mV Min
- Low Supply Current (Per Amplifier) ..... 625μA Max
- Operates From ±2V to ±20V Supplies
- High Common-Mode Rejection ..... 120dB Min
- Pin Compatible to LT1013, AD706, AD708, OP-221, LM158, and MC1458/1558 with Improved Performance

APPLICATIONS

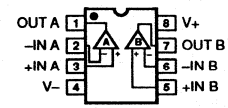
- Strain Guage and Bridge Amplifiers
- High Stability Thermocouple Amplifiers
- Instrumentation Amplifiers
- Photo-Current Monitors
- High-Gain Linearity Amplifiers
- Long-Term Integrators/Filters
- Sample-and-Hold Amplifiers
- Peak Detectors
- Logarithmic Amplifiers
- Battery-Powered Systems

GENERAL DESCRIPTION

The OP-297 is the first dual op amp to pack precision performance into the space-saving, industry standard 8-pin SO package. Its combination of precision with low power and extremely low input bias current makes the dual OP-297 useful in a wide variety of applications.

Precision performance of the OP-297 includes very low offset, under 50μV, and low drift, below 0.6μV/°C. Open-loop gain exceeds 2000V/mV insuring high linearity in every application. Errors due to common-mode signals are eliminated by the OP-297's common-mode rejection of over 120dB. The OP-297's power supply rejection of over 120dB minimizes offset voltage changes experienced in battery powered systems. Supply current of the OP-297 is under 625μA per amplifier and it can operate with supply voltages as low as ±2V. *Continued*

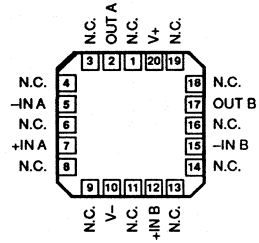
PIN CONNECTIONS



PLASTIC MINI-DIP (P-Suffix)

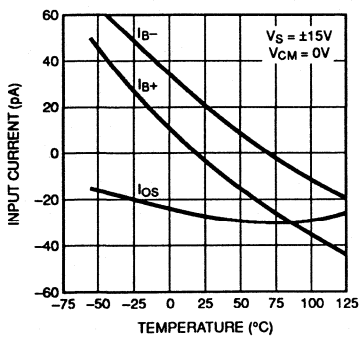
8-PIN CERDIP (Z-Suffix)

8-PIN SO (S-Suffix)

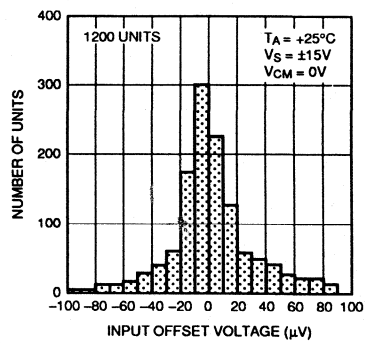


LCC (RC-Suffix)

LOW BIAS CURRENT OVER TEMPERATURE



VERY LOW OFFSET



GENERAL DESCRIPTION *Continued*

The OP-297 utilizes a super-beta input stage with bias current cancellation to maintain picoamp bias currents at all temperatures. This is in contrast to FET input op amps whose bias currents start in the picoamp range at 25°C, but double for every 10°C rise in temperature, to reach the nanoamp range above 85°C. Input bias current of the OP-297 is under 100pA at 25°C and is under 450pA over the military temperature range.

Combining precision, low power and low bias current, the OP-297 is ideal for a number of applications including instrumentation amplifiers, log amplifiers, photo-diode preamplifiers and long-term integrators. For a single device, see the OP-97; for a quad, see the OP-497.

ORDERING INFORMATION†

T_A = +25°C V_{OS} MAX (μV)	PACKAGE CERDIP 8-PIN	PACKAGE PLASTIC 8-PIN	PACKAGE LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
50	OP297AZ/883*	—	OP297ARC/883*	MIL
50	OP297AZ	—	—	MIL
50	OP297EZ	—	—	MIL
100	OP297FZ	OP297FP	—	XIND
200	—	OP297GP	—	XIND
200	—	OP297GS††	—	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on extended industrial temperature range parts in CerDIP, and plastic DIP packages.

†† For availability and burn-in information on SO packages, contact your local sales office.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±20V
Input Voltage (Note 2) ..... ±20V
Differential Input Voltage (Note 2) 40V
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range
  Z, RC-Package ..... –65°C to +175°C
  P, S-Package ..... –65°C to 150°C
Operating Temperature Range
  OP-297A (Z, RC) ..... –55°C to +125°C
  OP-297E, F (Z) ..... –40°C to +85°C
  OP-297F, G (P, S) ..... –40°C to +85°C
Junction Temperature
  Z, RC-Package ..... –65°C to +175°C
  P, S-Package ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C

PACKAGE TYPE	Θ_{JA} (Note 3)	Θ_{JC}	UNITS
8-Pin CerDIP (Z)	134	12	°C/W
8-Pin Plastic DIP (P)	96	37	°C/W
20-Contact LCC (RC)	88	33	°C/W
8-Pin SO (S)	150	41	°C/W

NOTES:

1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. For supply voltages less than ±20V, the absolute maximum input voltage is equal to the supply voltage.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-297A/E MIN	OP-297A/E TYP	OP-297A/E MAX	OP-297F MIN	OP-297F TYP	OP-297F MAX	OP-297G MIN	OP-297G TYP	OP-297G MAX	UNITS
Input Offset Voltage	V_{OS}		–	25	50	–	50	100	–	80	200	μV
Long-Term Input Voltage Stability			–	0.1	–	–	0.1	–	–	0.1	–	μV/mo
Input Offset Current	I_{OS}	V_{CM} = 0V	–	20	100	–	35	150	–	50	200	pA
Input Bias Current	I_B	V_{CM} = 0V	–	20	±100	–	35	±150	–	50	±200	pA
Input Noise Voltage	$e_{n\,p\text{-}p}$	0.1Hz to 10Hz	–	0.5	–	–	0.5	–	–	0.5	–	$\mu V_{p\text{-}p}$
Input Noise Voltage Density	e_n	f_O = 10Hz f_O = 1000Hz	– –	20 17	– –	– –	20 17	– –	– –	20 17	– –	$nV/\sqrt{Hz}$
Input Noise Current Density	i_n	f_O = 10Hz	–	20	–	–	20	–	–	20	–	$fA/\sqrt{Hz}$
Input Resistance Differential Mode	R_{IN}		–	30	–	–	30	–	–	30	–	MΩ
Input Resistance Common-Mode	R_{INCM}		–	500	–	–	500	–	–	500	–	GΩ
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V R_L = 2kΩ	2000	4000	–	1500	3200	–	1200	3200	–	V/mV

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $T_A = +25°C$, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	OP-297A/E MIN	OP-297A/E TYP	OP-297A/E MAX	OP-297F MIN	OP-297F TYP	OP-297F MAX	OP-297G MIN	OP-297G TYP	OP-297G MAX	UNITS
Input Voltage Range	IVR	(Note 1)	±13	±14	–	±13	±14	–	±13	±14	–	V
Common-Mode Rejection	CMR	$V_{CM} = \pm13V$	120	140	–	114	135	–	114	135	–	dB
Power Supply Rejection	PSR	$V_S = \pm2V$ to $\pm20V$	120	130	–	114	125	–	114	125	–	dB
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$	±13 ±13	±14 ±13.7	– –	±13 ±13	±14 ±13.7	– –	±13 ±13	±14 ±13.7	– –	V
Supply Current Per Amplifier	I_{SY}	No Load	–	525	625	–	525	625	–	525	625	µA
Supply Voltage	V_S	Operating Range	±2	–	±20	±2	–	±20	±2	–	±20	V
Slew Rate	SR		0.05	0.15	–	0.05	0.15	–	0.05	0.15	–	V/µs
Gain Bandwith Product	GBWP	$A_V = +1$	–	500	–	–	500	–	–	500	–	kHz
Channel Separation	CS	$V_O = 20V_{p-p}$ $f_O = 10Hz$	–	150	–	–	150	–	–	150	–	dB
Input Capacitance	C_{IN}		–	3	–	–	3	–	–	3	–	pF

NOTE:
1. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $-55°C \le T_A \le +125°C$ for OP-297A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-297A MIN	OP-297A TYP	OP-297A MAX	UNITS
Input Offset Voltage	V_{OS}		–	45	100	µV
Average Input Offset Voltage Drift	TCV_{OS}		–	0.2	0.6	µV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	–	60	450	pA
Input Bias Current	I_B	$V_{CM} = 0V$	–	60	±450	pA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm10V$, $R_L = 2k\Omega$	1200	2700	–	V/mV
Input Voltage Range	IVR	(Note 1)	±13	±13.5	–	V
Common-Mode Rejection	CMR	$V_{CM} = \pm13$	114	130	–	dB
Power Supply Rejection	PSR	$V_S = \pm2.5V$ to $\pm20V$	114	125	–	dB
Output Voltage Swing	V_O	$R_L = 10k\Omega$	±13	±13.4	–	V
Supply Current Per Amplifier	I_{SY}	No Load	–	575	750	µA
Supply Voltage	V_S	Operating Range	±2.5	–	±20	V

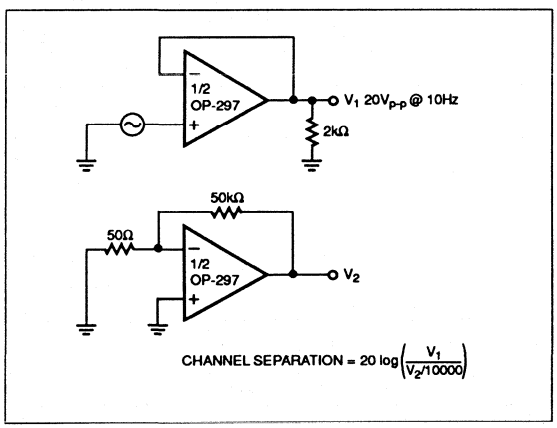
NOTE:
1. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-40°C \le T_A \le +85°C$ for OP-297E/F/G, unless otherwise noted.

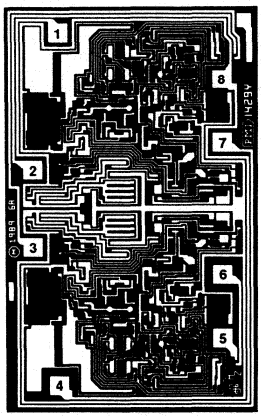
PARAMETER	SYMBOL	CONDITIONS	OP-297E			OP-297F			OP-297G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		–	35	100	–	80	300	–	110	400	µV
Average Input Offset Voltage Drift	TCV_{OS}		–	0.2	0.6	–	0.5	2.0	–	0.6	2.0	µV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	–	50	450	–	80	750	–	80	750	pA
Input Bias Current	I_B	$V_{CM} = 0V$	–	50	±450	–	80	±750	–	80	±750	pA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$, $R_L = 2k\Omega$	1200	3200	–	1000	2500	–	800	2500	–	V/mV
Input Voltage Range	IVR	(Note 1)	±13	±13.5	–	±13	±13.5	–	±13	±13.5	–	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 13V$	114	130	–	108	130	–	108	130	–	dB
Power Supply Rejection	PSR	$V_S = \pm 2.5V$ to $\pm 20V$	114	0.15	–	108	0.15	–	108	0.3	–	dB
Output Voltage Swing	V_O	$R_L = 10k\Omega$	±13	±13.4	–	±13	±13.4	–	±13	±13.4	–	V
Supply Current Per Amplifier	I_{SY}	No Load	–	550	750	–	550	750	–	550	750	µA
Supply Voltage	V_S	Operating Range	±2.5	–	±20	±2.5	–	±20	±2.5	–	±20	V

NOTE:
1. Guaranteed by CMR test.

CHANNEL SEPARATION TEST CIRCUIT



DICE CHARACTERISTICS



1. OUT A
2. –IN A
3. +IN A
4. V–
5. +IN B
6. –IN B
7. OUT B
8. V+

DIE SIZE 0.071 x 0.114 inch, 8,094 sq. mils
(1.80 x 2.90 mm, 5.22 sq. mm)

2

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

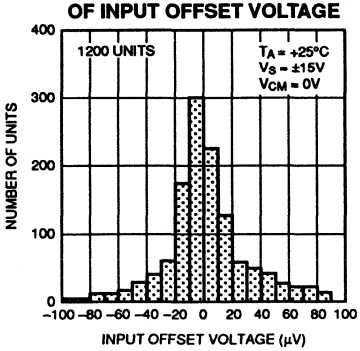
PARAMETER	SYMBOL	CONDITIONS	OP-297GBC LIMIT	UNITS
Input Offset Voltage	V_{OS}		200	µV MAX
Input Offset Current	I_{OS}	$V_{CM} = 0V$	200	pA MAX
Input Bias Current	I_B	$V_{CM} = 0V$	±200	pA MAX
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$, $R_L = 2k\Omega$	1200	V/mV MIN
Input Voltage Range	IVR	(Note 1)	±13	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 13V$	114	dB MIN
Power Supply Rejection	PSR	$V_S = \pm 2V$ to $\pm 18V$	114	dB MIN
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$	±13 ±13	V MIN
Supply Current Per Amplifier	I_{SY}	No Load	625	µA MAX

NOTES:
1. Guaranteed by CMR test.

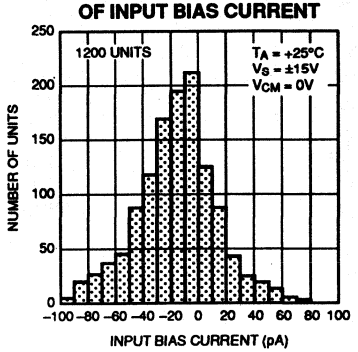
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

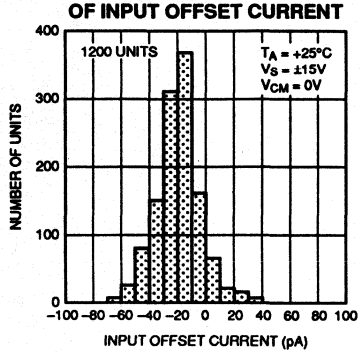
TYPICAL DISTRIBUTION OF INPUT OFFSET VOLTAGE



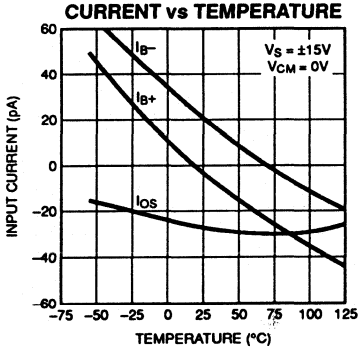
TYPICAL DISTRIBUTION OF INPUT BIAS CURRENT



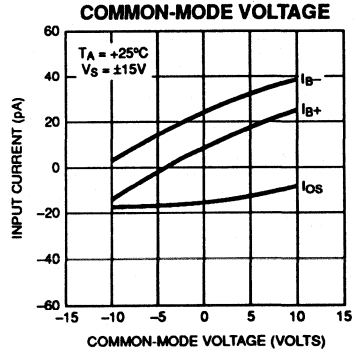
TYPICAL DISTRIBUTION OF INPUT OFFSET CURRENT



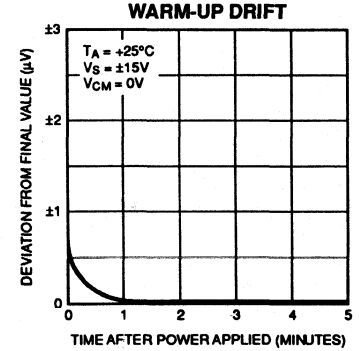
INPUT BIAS, OFFSET CURRENT vs TEMPERATURE



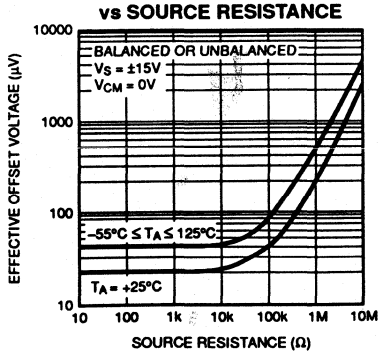
INPUT-BIAS, OFFSET CURRENT vs COMMON-MODE VOLTAGE



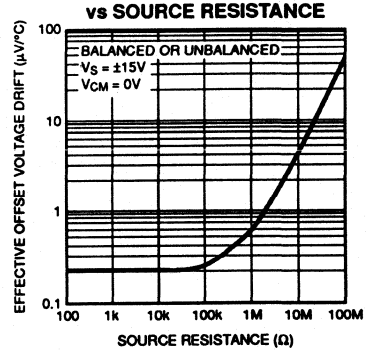
INPUT OFFSET VOLTAGE WARM-UP DRIFT



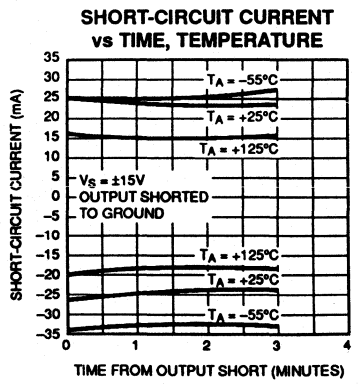
EFFECTIVE OFFSET VOLTAGE vs SOURCE RESISTANCE



EFFECTIVE TCVOS vs SOURCE RESISTANCE

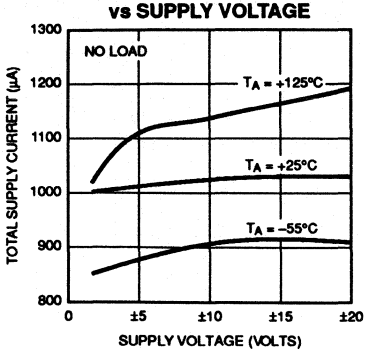


SHORT-CIRCUIT CURRENT vs TIME, TEMPERATURE

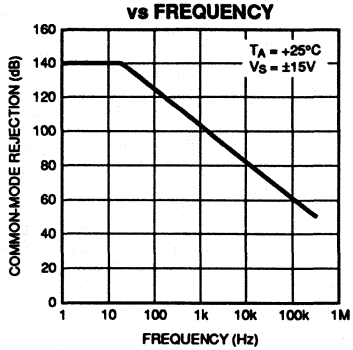


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

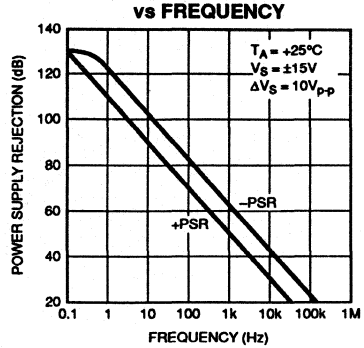
TOTAL SUPPLY CURRENT vs SUPPLY VOLTAGE



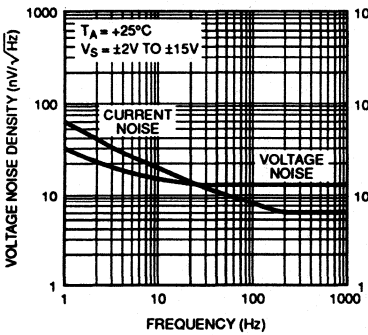
COMMON-MODE REJECTION vs FREQUENCY



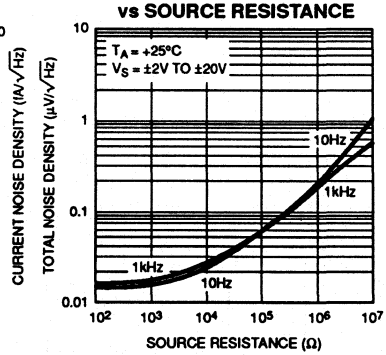
POWER SUPPLY REJECTION vs FREQUENCY



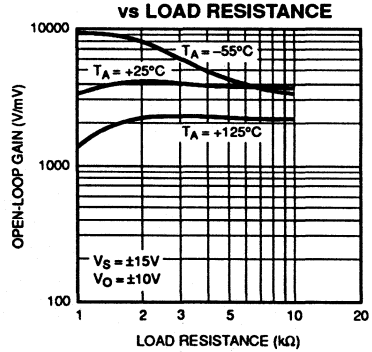
NOISE DENSITY vs FREQUENCY



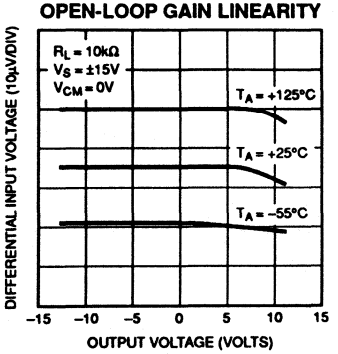
TOTAL NOISE DENSITY vs SOURCE RESISTANCE



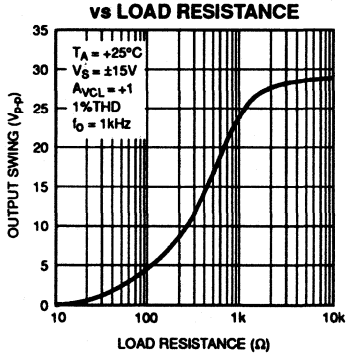
OPEN-LOOP GAIN vs LOAD RESISTANCE



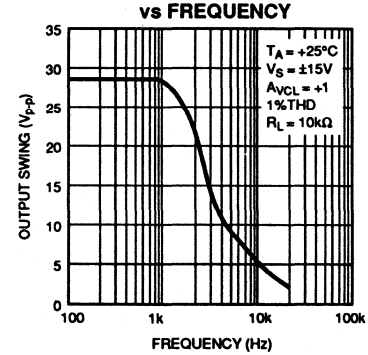
OPEN-LOOP GAIN LINEARITY



MAXIMUM OUTPUT SWING vs LOAD RESISTANCE

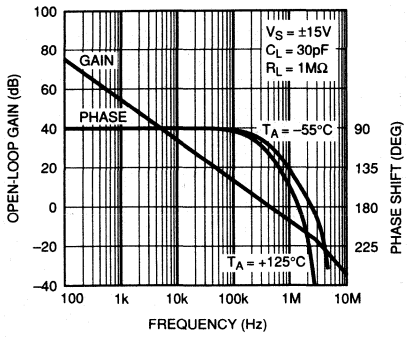


MAXIMUM OUTPUT SWING vs FREQUENCY

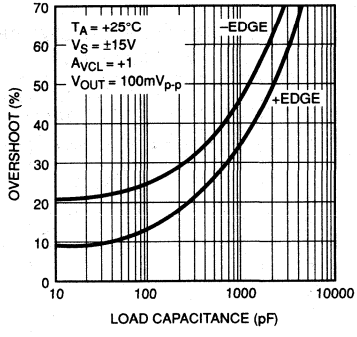


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

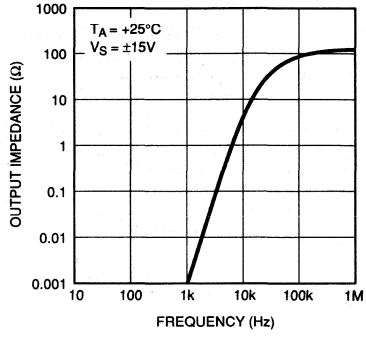
OPEN-LOOP GAIN, PHASE vs FREQUENCY



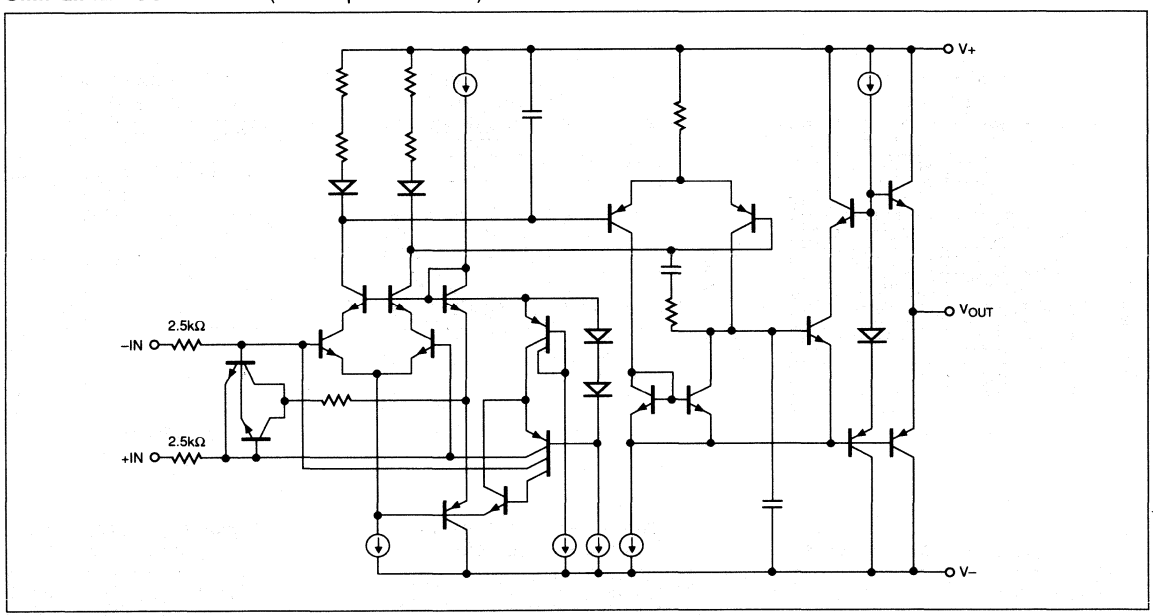
SMALL-SIGNAL OVERSHOOT vs CAPACITANCE LOAD



OPEN-LOOP OUTPUT IMPEDANCE vs FREQUENCY



SIMPLIFIED SCHEMATIC (One Amplifier is Shown)



APPLICATIONS INFORMATION

Extremely low bias current over the full military temperature range makes the OP-297 attractive for use in sample-and-hold amplifiers, peak detectors, and log amplifiers that must operate over a wide temperature range. Balancing input resistances is not necessary with the OP-297. Offset voltage and TCV_{OS} are degraded only minimally by high source resistance, even when unbalanced.

The input pins of the OP-297 are protected against large differential voltage by back-to-back diodes and current-limiting resistors. Common-mode voltages at the inputs are not restricted, and may vary over the full range of the supply voltages used.

The OP-297 requires very little operating headroom about the supply rails, and is specified for operation with supplies as low as ±2V. Typically, the common-mode range extends to within one volt of either rail. The output typically swings to within one volt of the rails when using a 10kΩ load.

AC PERFORMANCE

The OP-297'S AC characteristics are highly stable over its full operating temperature range. Unity-gain small-signal response is shown in Figure 1. Extremely tolerant of capacitive loading on the output, the OP-297 displays excellent response even with 1000pF loads (Figure 2).

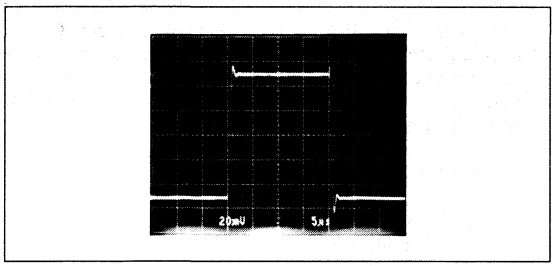


FIGURE 1: *Small-Signal Transient Response (C_{LOAD} = 100pF, A_{VCL} = +1)*

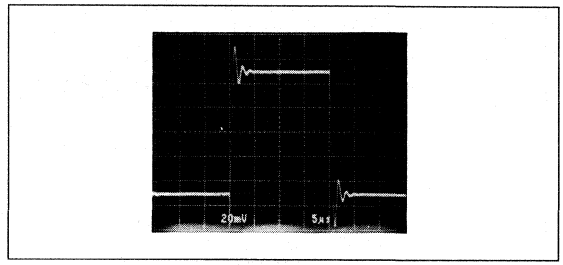


FIGURE 2: *Small-Signal Transient Response (C_{LOAD} = 1000pF, A_{VCL} = +1)*

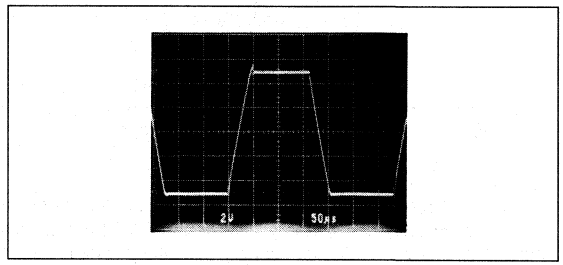


FIGURE 3: *Large-Signal Transient Response (A_{VCL} = +1)*

GUARDING AND SHIELDING

To maintain the extremely high input impedances of the OP-297, care must be taken in circuit board layout and manufacturing. Board surfaces must be kept scrupulously clean and free of moisture. Conformal coating is recommended to provide a humidity barrier. Even a clean PC board can have 100pA of leakage currents between adjacent traces, so guard rings should be used around the inputs. Guard traces are operated at a voltage close to that on the inputs, as shown in Figure 4, so that leakage currents become minimal. In noninverting applications, the guard ring should be connected to the common-mode voltage at the inverting input. In inverting applications, both inputs remain at ground, so the guard trace should be grounded. Guard traces should be on both sides of the circuit board.

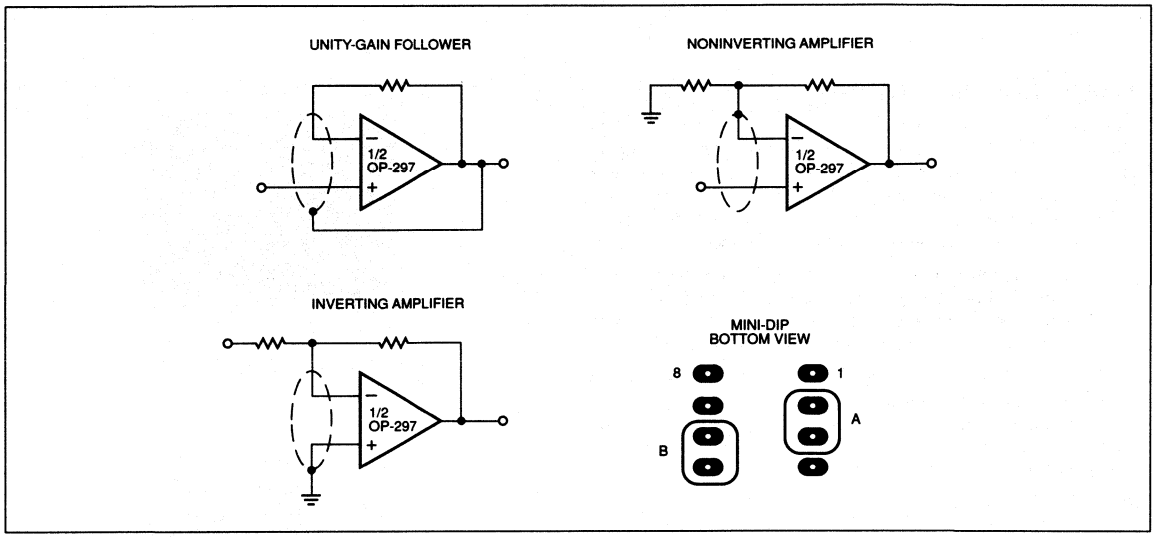


FIGURE 4: *Guard Ring Layout and Connections*

OPEN-LOOP GAIN LINEARITY

The OP-297 has both an extremely high gain of 2000V/mV minimum and constant gain linearity. This enhances the precision of the OP-297 and provides for very high accuracy in high closed-loop gain applications. Figure 5 illustrates the typical open-loop gain linearity of the OP-297 over the military temperature range.

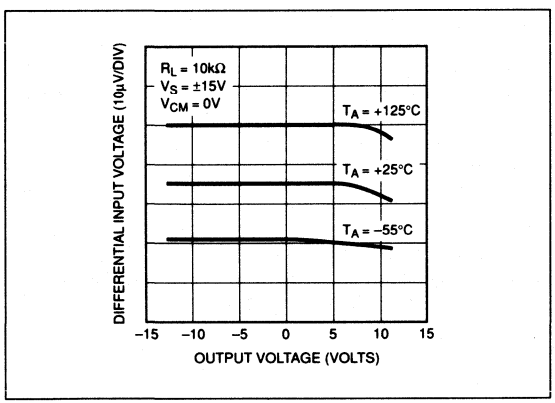


FIGURE 5: *Open-Loop Linearity of the OP-297*

APPLICATIONS

PRECISION ABSOLUTE VALUE AMPLIFIER

The circuit of Figure 6 is a precision absolute value amplifier with an input impedance of 30MΩ. The high gain and low TCV_{OS} of the OP-297 insure accurate operation with microvolt input signals. In this circuit, the input always appears as a common-mode signal to the op amps. The CMR of the OP-297 exceeds 120dB, yielding an error of less than 2ppm.

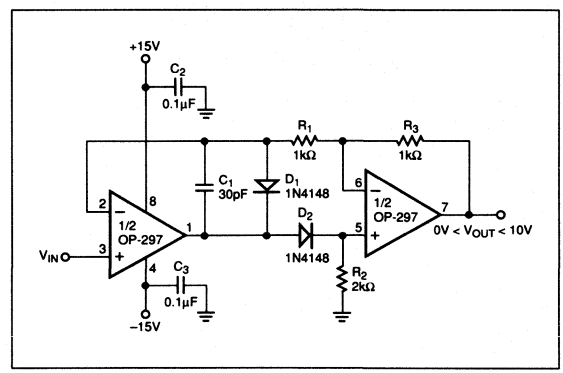


FIGURE 6: *Precision Absolute Value Amplifier*

PRECISION CURRENT PUMP

Maximum output current of the precision current pump shown in Figure 7 is ±10mA. Voltage compliance is ±10V with ±15V supplies. Output impedance of the current transmitter exceeds 3MΩ with linearity better than 16 bits.

PRECISION POSITIVE PEAK DETECTOR

In Figure 8, the C_H must be of polystyrene, Teflon*, or polyethylene to minimize dielectric absorption and leakage. The droop rate is determined by the size of C_H and the bias current of the OP-297.

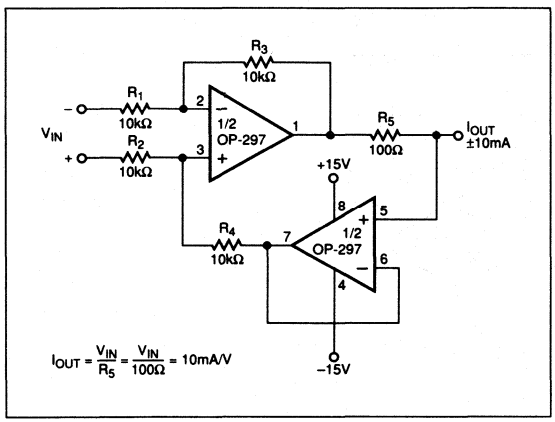


FIGURE 7: *Precision Current Pump*

SIMPLE BRIDGE CONDITIONING AMPLIFIER

Figure 9 shows a simple bridge conditioning amplifier using the OP-297. The transfer function is:

$$V_{OUT} = V_{REF}\left(\frac{\Delta R}{R + \Delta R}\right)\frac{R_F}{R}$$

The REF-43 provides an accurate and stable reference voltage for the bridge. To maintain the highest circuit accuracy, R_F should be 0.1% or better with a low temperature coefficient.

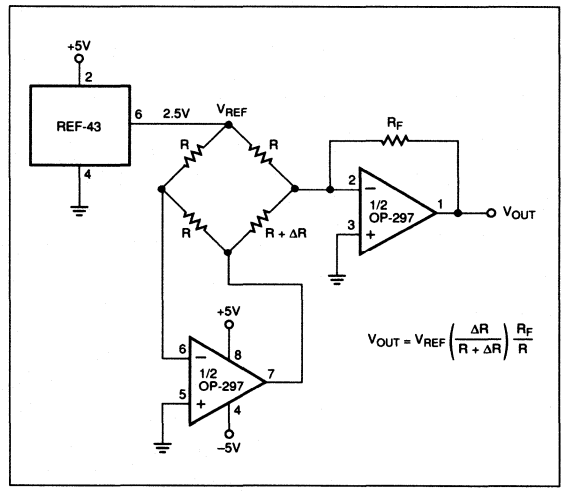


FIGURE 9: *A simple bridge conditioning amplifier using the OP-297.*

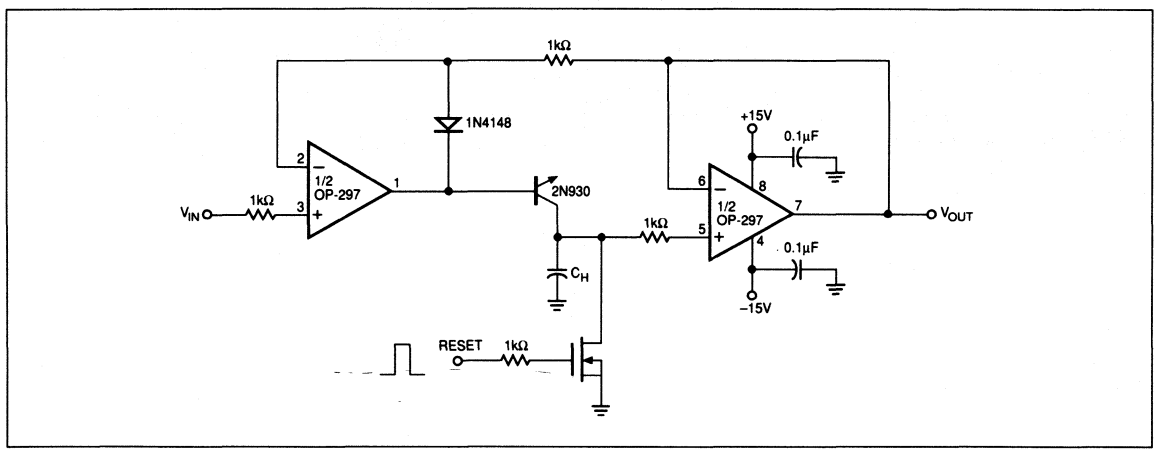


FIGURE 8: *Precision Positive Peak Detector*

*Teflon is a registered trademark of the Dupont Company

NONLINEAR CIRCUITS

Due to its low input bias currents, the OP-297 is an ideal log amplifier in nonlinear circuits such as the square and square-root circuits shown in Figures 10 and 11. Using the squaring circuit of Figure 10 as an example, the analysis begins by writing a voltage loop equation across transistors Q_1, Q_2, Q_3 and Q_4.

$$V_{T1} \ln\left(\frac{I_{IN}}{I_{S1}}\right) + V_{T2} \ln\left(\frac{I_{IN}}{I_{S2}}\right) = V_{T3} \ln\left(\frac{I_O}{I_{S3}}\right) + V_{T4} \ln\left(\frac{I_{REF}}{I_{S4}}\right)$$

All the transistors of the MAT-04 are precisely matched and at the same temperature, so the I_S and V_T terms cancel, giving:

$$2 \ln I_{IN} = \ln I_O + \ln I_{REF} = \ln (I_O \times I_{REF})$$

Exponentiating both sides of the equation leads to:

$$I_O = \frac{(I_{IN})^2}{I_{REF}}$$

Op amp A_2 forms a current-to-voltage converter which gives $V_{OUT} = R_2 \times I_O$. Substituting (V_{IN}/R_1) for I_{IN} and the above equation for I_O yields:

$$V_{OUT} = \left(\frac{R_2}{I_{REF}}\right)\left(\frac{V_{IN}}{R_1}\right)^2$$

A similar analysis made for the square-root circuit of Figure 11 leads to its transfer function:

$$V_{OUT} = R_2 \sqrt{\frac{(V_{IN})(I_{REF})}{R_1}}$$

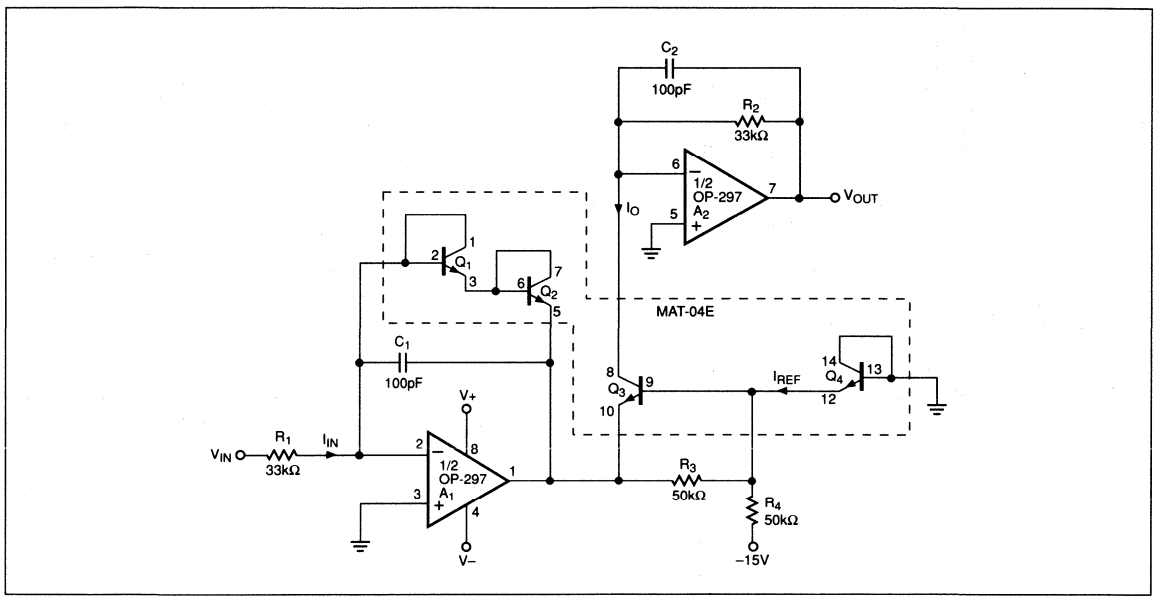


FIGURE 10: *Squaring Amplifier*

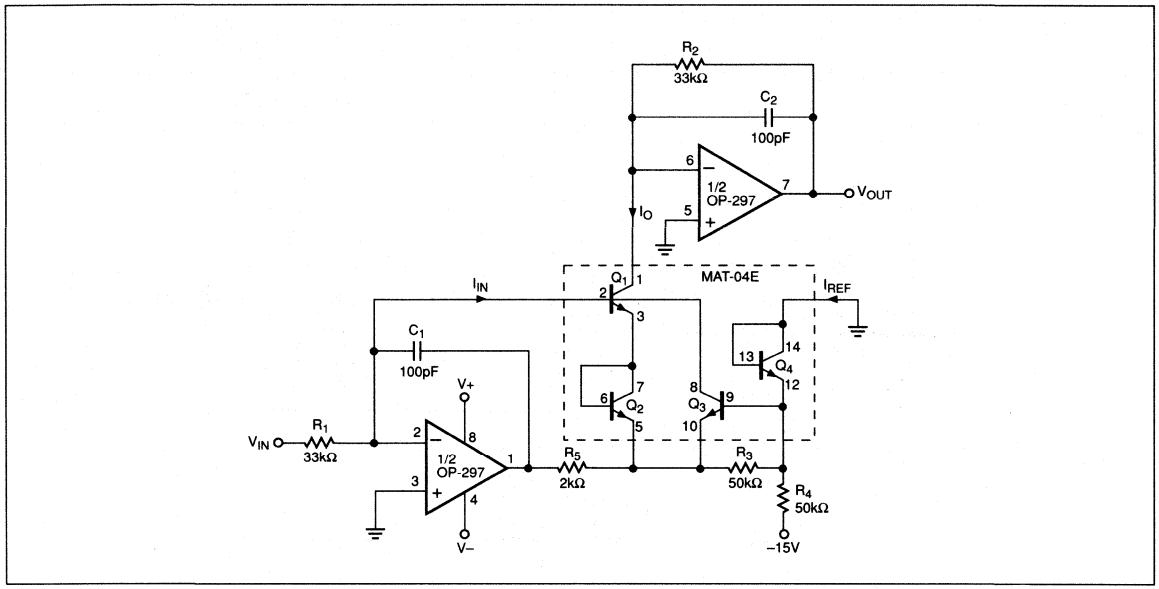


FIGURE 11: *Square-Root Amplifier*

In these circuits, I_{REF} is a function of the negative power supply. To maintain accuracy, the negative supply should be well regulated. For applications where very high accuracy is required, a voltage reference may be used to set I_{REF}. An important consideration for the squaring circuit is that a sufficiently large input voltage can force the output beyond the operating range of the output op amp. Resistor R_4 can be changed to scale I_{REF}, or R_1 and R_2 can be varied to keep the output voltage within the usable range.

Unadjusted accuracy of the square-root circuit is better than 0.1% over an input voltage range of 100mV to 10V. For a similar input voltage range, the accuracy of the squaring circuit is better than 0.5%.

OP-297 SPICE MACRO-MODEL

Figures 12 and 13 show the node and net list for a SPICE macromodel of the OP-297. The model is a simplified version of the actual device and simulates important DC parameters such as V_{OS}, I_{OS}, I_B, A_{VO}, CMR, V_O and I_{SY}. AC parameters such as slew rate, gain and phase response and CMR change with frequency are also simulated by the model.

The model uses typical parameters for the OP-297. The poles and zeros in the model were determined from the actual open and closed-loop gain and phase response of the OP-297. In this way, the model presents an accurate AC representation of the actual device. The model assumes an ambient temperature of 25°C.

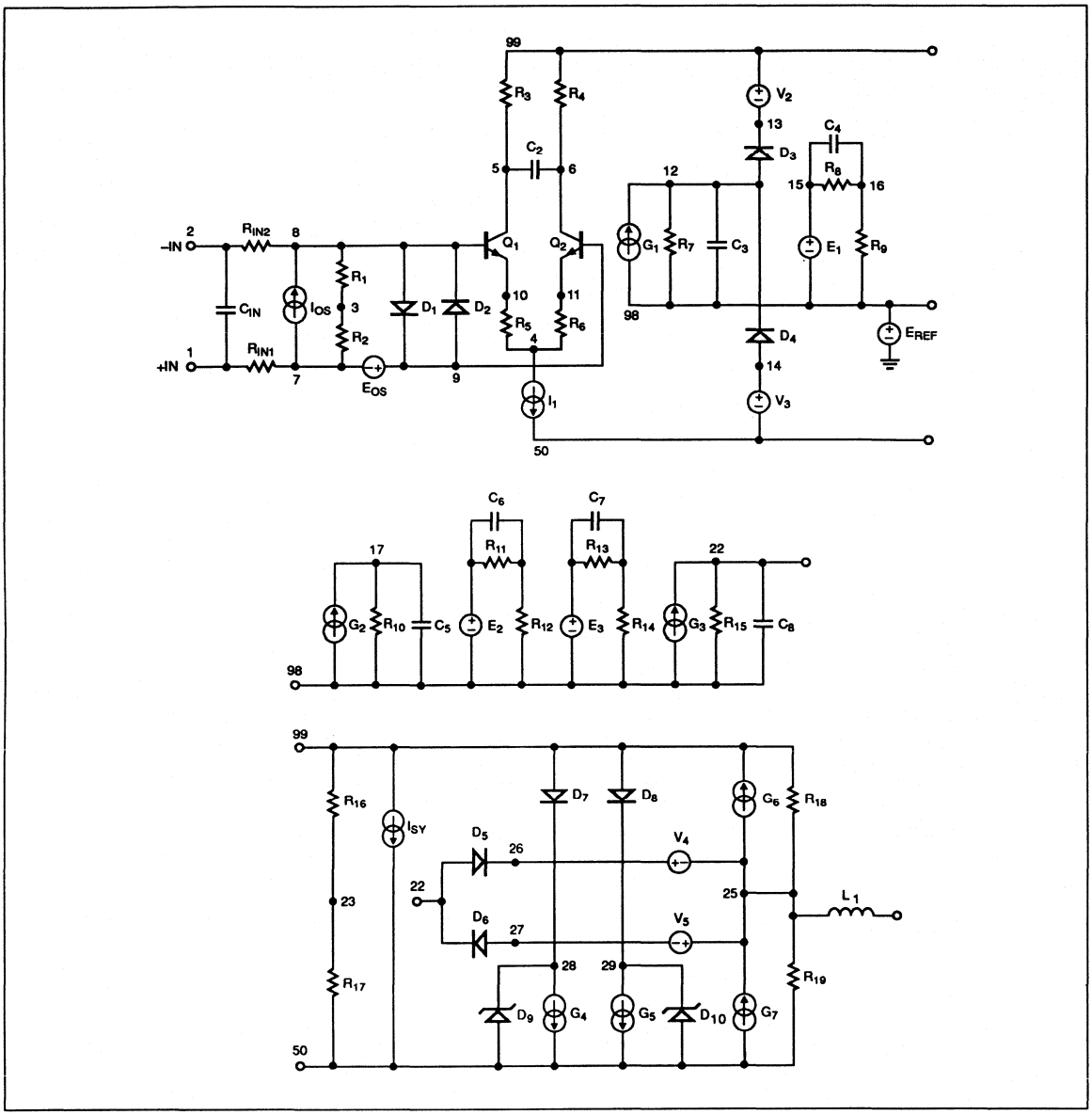


FIGURE 12: *OP-297 Macro-Model*

```
* OP-297 SPICE MACRO-MODEL © PMI 1990
*
* NODE ASSIGNMENTS
*                    NONINVERTING INPUT
*                    | INVERTING INPUT
*                    | | OUTPUT
*                    | | | POSITIVE SUPPLY
*                    | | | | NEGATIVE SUPPLY
*                    | | | | |
.SUBCKT OP-297  1  2  30  99  50
*
* INPUT STAGE & POLE AT 6 MHZ
*
RIN1   1   7        2500
RIN2   2   8        2500
R1     8   3        5E11
R2     7   3        5E11
R3     5   99       612
R4     6   99       612
CIN    7   8        3E-12
C2     5   6        21.67E-12
I1     4   50       0.1E-3
IOS    7   8        20E-12
EOS    9   7        POLY(1) 19 23 25E-6 1
Q1     5   8   10   QX
Q2     6   9   11   QX
R5     10  4        96
R6     11  4        96
D1     8   9        DX
D2     9   8        DX
*
EREF   98  0        23 0 1
*
*GAIN STAGE & DOMINANT POLE AT 0.13 HZ
*
R7     12  98       2.45E9
C3     12  98       500E-12
G1     98  12       5 6 1.634E-3
V2     99  13       1.5
V3     14  50       1.5
D3     12  13       DX
D4     14  12       DX
*
*NEGATIVE ZERO AT –1.8 MHZ
*
R8     15  16       1E6
C4     15  16       –88.4E-15
R9     16  98       1
E1     15  98       12 23 1E6
*
*POLE AT 1.8 MHZ
*
R10    17  98       1E6
C5     17  98       88.4E-15
G2     98  17       16 23 1E-6
*
*COMMON-MODE GAIN NETWORK WITH ZERO AT 50 HZ
*
R11    18  19       1E6
C6     18  19       3.183E-9
R12    19  98       1
E2     18  98       3 23 100E-3
*
*POLE AT 6 MHZ
*
R15    22  98       1E6
C8     22  98       26.53E-15
G3     98  22       17 23 1E-6
*
*OUTPUT STAGE
*
R16    23  99       160K
R17    23  50       160K
ISY    99  50       331E-6
R18    25  99       200
R19    25  50       200
L1     25  30       1E-7
G4     28  50       22 25 5E-3
G5     29  50       25 22 5E-3
G6     25  99       99 22 5E-3
G7     50  25       22 50 5E-3
V4     26  25       1.8
V5     25  27       1.3
D5     22  26       DX
D6     27  22       DX
D7     99  28       DX
D8     99  29       DX
D9     50  28       DY
D10    50  29       DY
*
*MODELS USED
*
.MODEL QX NPN (BF=2.5E6)
.MODEL DX     D (IS=1E-15)
.MODEL DY     D (IS=1E-15 BV=50)
.ENDS OP-297
```

FIGURE 13: *OP-297 SPICE Net-List*

ANALOG DEVICES

Quad Low-Offset, Low-Power Operational Amplifier

OP-400

FEATURES

- **Low Input Offset Voltage ..... 150μV Max**
- **Low Offset Voltage Drift, Over –55°C to +125°C ..... 1.2μV/°C Max**
- **Low Supply Current (Per Amplifier) ..... 725μA Max**
- **High Open-Loop Gain ..... 5000V/mV Min**
- **Input Bias Current ..... 3nA Max**
- **Low Noise Voltage Density ..... 11nV/$\sqrt{Hz}$ at 1kHz**
- **Stable With Large Capacitive Loads ..... 10nF Typ**
- **Pin Compatible to OP-11, LM148, HA4741, RM4156, and LT1014 With Improved Performance**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (mV)	PACKAGE CERDIP 14-PIN	PACKAGE PLASTIC	PACKAGE LCC 28-CONTACT	OPERATING TEMPERATURE RANGE
150	OP400AY*	–	OP400ATC/883	MIL
150	OP400EY	–	–	IND
230	OP400FY	–	–	IND
300	–	OP400GP	–	COM
300	–	OP400GS††	–	COM
300	–	OP400HP	–	XIND
300	–	OP400HS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

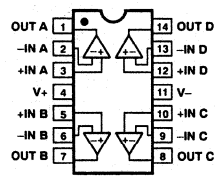
†† For availablity and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

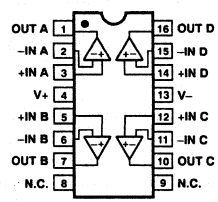
The OP-400 is the first monolithic quad operational amplifier that features OP-77 type performance. Precision performance no longer has to be sacrificed to obtain the space and cost savings offered by quad amplifiers.

The OP-400 features an extremely low input offset voltage of less than 150μV with a drift of under 1.2μV/°C, guaranteed

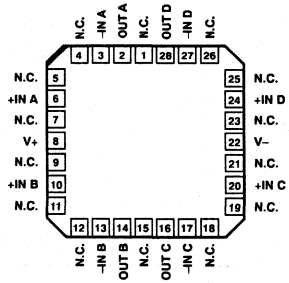
PIN CONNECTIONS



14-PIN HERMETIC DIP (Y-Suffix)
14-PIN PLASTIC DIP (P-Suffix)

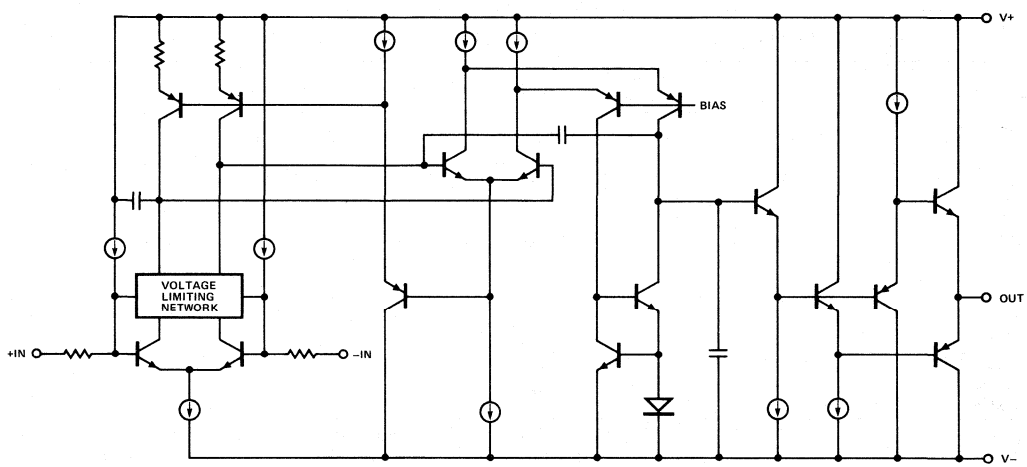


16-PIN SOL (S-Suffix)



28-LEAD LCC (TC-Suffix)

SIMPLIFIED SCHEMATIC (One of four amplifiers is shown.)



over the full military temperature range. Open-loop gain of the OP-400 is over 5,000,000 into a 10kΩ load; input bias current is under 3nA; CMR is above 120dB and PSRR below 1.8μV/V. On-chip zener-zap trimming is used to achieve the low input offset voltage of the OP-400 and eliminates the need for offset nulling. (The OP-400 conforms to the industry-standard quad pinout which does not have null terminals.)

The OP-400 features low power consumption, drawing less than 725μA per amplifier. The total current drawn by this quad amplifier is less than that of a single OP-07, yet the OP-400 offers significant improvements over this industry-standard op amp. Voltage noise density of the OP-400 is a low $11nV/\sqrt{Hz}$ at 10Hz which is half that of most competitive devices.

The OP-400 is pin compatible with the OP-11, LM148, HA4741, RM4156, and LT1014 operational amplifiers and can be used to upgrade systems using these devices. The OP-400 is an ideal choice for applications requiring multiple precision operational amplifiers and where low power consumption is critical.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage ..... ±20V
Differential Input Voltage ..... ±30V
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous
Storage Temperature Range
P, TC, Y-Package ..... –65°C to +150°C
Lead Temperature Range (Soldering 60 sec) ..... 300°C
Junction Temperature (T_J) ..... –65°C to +150°C
Operating Temperature Range
OP-400A ..... –55°C to +125°C
OP-400E, OP-400F ..... –25°C to +85°C
OP-400G ..... 0°C to +70°C
OP-400H ..... –40°C to +85°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
14-Pin Hermetic DIP (Y)	94	10	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
28-Contact LCC (TC)	70	28	°C/W
16-Pin SOL (S)	88	23	°C/W

NOTES:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.
2. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $T_A = +25°C$, unless otherwise noted.

			OP-400A/E			OP-400F			OP-400G/H			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	40	150	—	60	230	—	80	300	μV
Long Term Input Voltage Stability			—	0.1	—	—	0.1	—	—	0.1	—	μV/mo
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	0.1	1.0	—	0.1	2.0	—	0.1	3.5	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	0.75	3.0	—	0.75	6.0	—	0.75	7.0	nA
Input Noise Voltage	$e_{n\ p-p}$	0.1Hz to 10Hz	—	0.5	—	—	0.5	—	—	0.5	—	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$ (Note 1)	—	22	36	—	22	36	—	22	—	$nV/\sqrt{Hz}$
		$f_O = 1000Hz$ (Note 1)	—	11	18	—	11	18	—	11	—	
Input Noise Current	$i_{n\ p-p}$	0.1Hz to 10Hz	—	15	—	—	15	—	—	15	—	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10Hz$	—	0.6	—	—	0.6	—	—	0.6	—	$pA/\sqrt{Hz}$
Input Resistance Differential Mode	R_{IN}		—	10	—	—	10	—	—	10	—	MΩ
Input Resistance Common Mode	R_{INCM}		—	200	—	—	200	—	—	200	—	GΩ
Large Signal Voltage Gain	A_{VO}	$V_O = \pm10V$ $R_L = 10k\Omega$	5000	12000	—	3000	7000	—	3000	7000	—	V/mV
		$R_L = 2k\Omega$	2000	3500	—	1500	3000	—	1500	3000	—	

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $T_A = +25°C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-400A/E MIN	OP-400A/E TYP	OP-400A/E MAX	OP-400F MIN	OP-400F TYP	OP-400F MAX	OP-400G/H MIN	OP-400G/H TYP	OP-400G/H MAX	UNITS
Input Voltage Range	IVR	Note 3	±12	±13	—	±12	±13	—	±12	±13	—	V
Common Mode Rejection	CMR	$V_{CM} = \pm12V$	120	140	—	115	140	—	110	135	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm3V$ to $\pm18V$	—	0.1	1.8	—	0.1	3.2	—	0.2	5.6	μV/V
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$	±12 ±11	±12.6 ±12.2	— —	±12 ±11	±12.6 ±12.2	— —	±12 ±11	±12.6 ±12.2	— —	V
Supply Current Per Amplifier	I_{SY}	No Load	—	600	725	—	600	725	—	600	725	μA
Slew Rate	SR		0.1	0.15	—	0.1	0.15	—	0.1	0.15	—	V/μs
Gain Bandwidth Product	GBWP	$A_V = +1$	—	500	—	—	500	—	—	500	—	kHz
Channel Separation	CS	$V_O = 20V_{p-p}$ $f_O = 10Hz$ (Note 2)	123	135	—	123	135	—	123	135	—	dB
Input Capacitance	C_{IN}		—	3.2	—	—	3.2	—	—	3.2	—	pF
Capacitive Load Stability		$A_V = +1$ No Oscillations	—	10	—	—	10	—	—	10	—	nF

NOTES:
1. Sample tested.
2. Guaranteed but not 100% tested.
3. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $-55°C \leq T_A \leq 125°C$ for OP-400A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-400A MIN	OP-400A TYP	OP-400A MAX	UNITS
Input Offset Voltage	V_{OS}		—	70	270	μV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.3	1.2	μV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	0.1	2.5	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	1.3	5.0	nA
Large Signal Voltage Gain	A_{VO}	$V_O = \pm10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	3000 1000	9000 2300	— —	V/mV
Input Voltage Range	IVR	Note 1	±12	±12.5	—	V
Common Mode Rejection	CMR	$V_{CM} = \pm12V$	115	130	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm3V$ to $\pm18V$	—	0.2	3.2	μV/V
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$	±12 ±11	±12.4 ±12	— —	V
Supply Current Per Amplifier	I_{SY}	No Load	—	600	775	μA
Capacitive Load Stability		$A_V = +1$ No Oscillations	—	8	—	nF

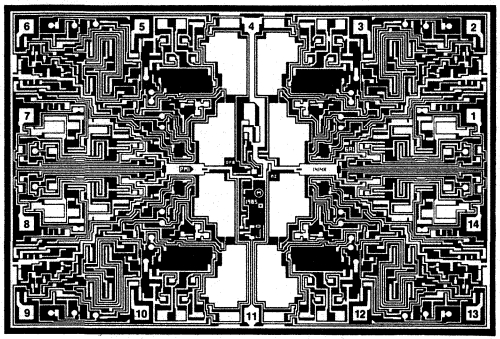
NOTE:
1. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-25°C \le T_A \le \pm 85°C$ for OP-400E/F, $0°C \le T_A \le +70°C$ for OP-400G, $-40°C \le T_A \le +85°C$ for OP-400H, unless otherwise noted.

			OP-400E			OP-400F			OP-400G/H			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}		–	60	220	–	80	350	–	110	400	µV
Average Input Offset Voltage Drift	TCV_{OS}		–	0.3	1.2	–	0.3	2.0	–	0.6	2.5	µV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$ E, F, G Grades H Grade	– –	0.1 –	2.5 –	– –	0.1 –	3.5 –	– –	0.2 0.2	6.0 12.0	nA
Input Bias Current	I_B	$V_{CM} = 0V$ E, F, G Grades H Grade	– –	0.9 –	5.0 –	– –	0.9 –	10.0 –	– –	1.0 1.0	12.0 20.0	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	3000 1500	10000 2700	– –	2000 1000	5000 2000	– –	2000 1000	5000 2000	– –	V/mV
Input Voltage Range	IVR	(Note 1)	±12	±12.5	–	±12	±12.5	–	±12	±12.5	–	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 12V$	115	135	–	110	135	–	105	130	–	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	–	0.15	3.2	–	0.15	5.6	–	0.3	10.0	µV/V
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$	±12 ±11	±12.4 ±12	– –	±12 ±11	±12.4 ±12	– –	±12 ±11	±12.6 ±12.2	– –	V
Supply Current Per Amplifier	I_{SY}	No Load	–	600	775	–	600	775	–	600	775	µA
Capacitive Load Stability		$A_V = +1$ No Oscillations	–	10	–	–	10	–	–	10	–	nF

NOTE:
1. Guaranteed by CMR test.

DICE CHARACTERISTICS



DIE SIZE 0.181 × 0.123 inch, 22,263 sq. mils
(4.60 × 3.12 mm, 14.35 sq. mm)

1. OUT A
2. −IN A
3. +IN A
4. V+
5. +IN B
6. −IN B
7. OUT B
8. OUT C
9. −IN C
10. +IN C
11. V−
12. +IN D
13. −IN D
14. OUT D

2

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-400GBC LIMIT	UNITS
Input Offset Voltage	V_{OS}		230	μV MAX
Input Offset Current	I_{OS}	$V_{CM} = 0V$	2	nA MAX
Input Bias Current	I_B	$V_{CM} = 0V$	6	nA MAX
Large Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	3000 1500	V/mV MIN
Input Voltage Range	IVR	Note 1	±12	V MIN
Common Mode Rejection	CMR	$V_{CM} = \pm 12V$	115	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	3.2	μV/V MAX
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$	±12 ±11	V MIN
Supply Current Per Amplifier	I_{SY}	No Load	725	μA MAX

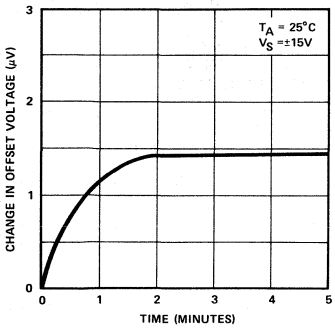
NOTES:
1. Guaranteed by CMR test.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

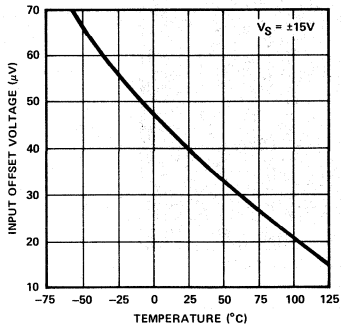
OP-400

TYPICAL PERFORMANCE CHARACTERISTICS

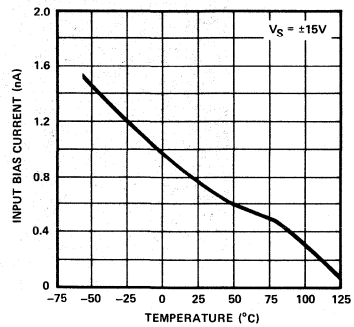
WARM-UP DRIFT



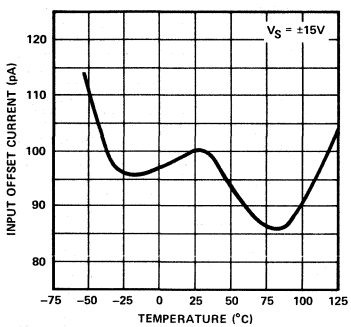
INPUT OFFSET VOLTAGE vs TEMPERATURE



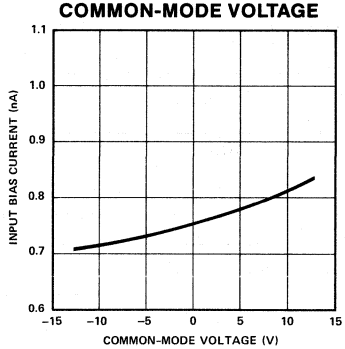
INPUT BIAS CURRENT vs TEMPERATURE



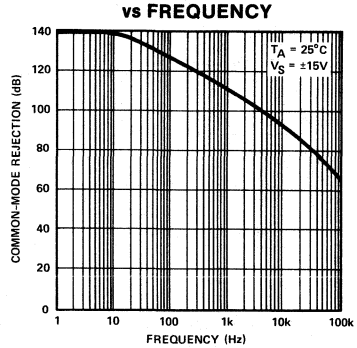
INPUT OFFSET CURRENT vs TEMPERATURE



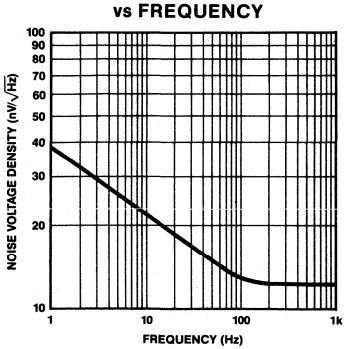
INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE



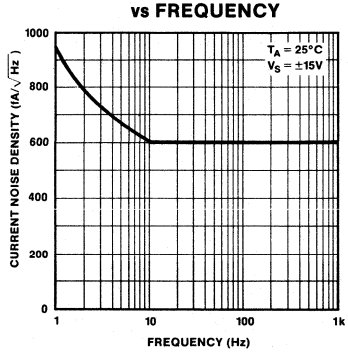
COMMON-MODE REJECTION vs FREQUENCY



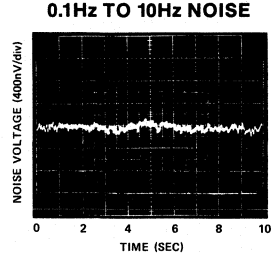
NOISE VOLTAGE DENSITY vs FREQUENCY



CURRENT NOISE DENSITY vs FREQUENCY

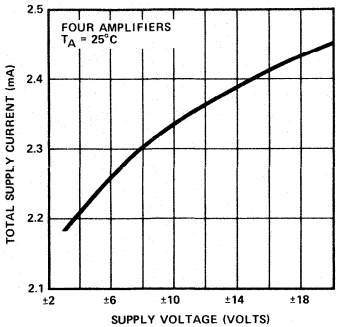


0.1Hz TO 10Hz NOISE

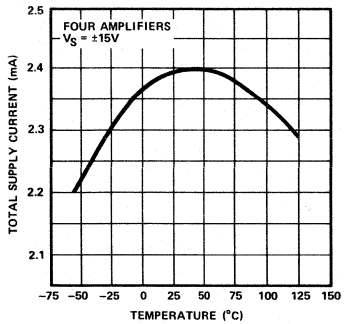


TYPICAL PERFORMANCE CHARACTERISTICS

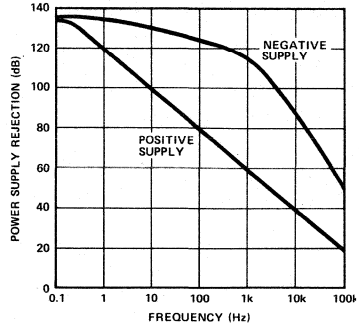
TOTAL SUPPLY CURRENT vs SUPPLY VOLTAGE



TOTAL SUPPLY CURRENT vs TEMPERATURE

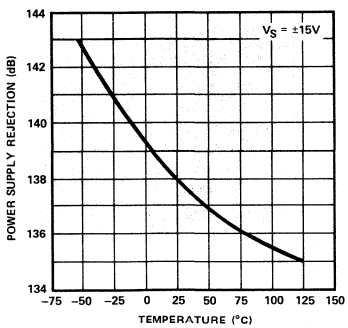


POWER SUPPLY REJECTION vs FREQUENCY

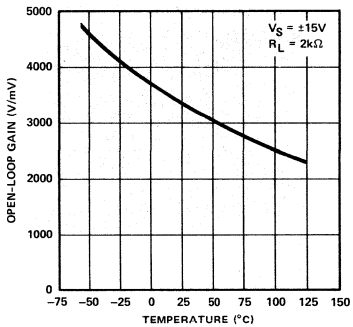


2

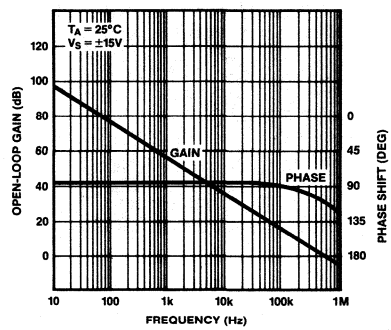
POWER SUPPLY REJECTION vs TEMPERATURE



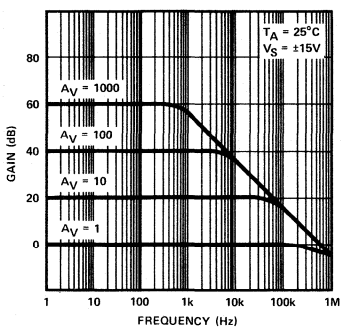
OPEN-LOOP GAIN vs TEMPERATURE



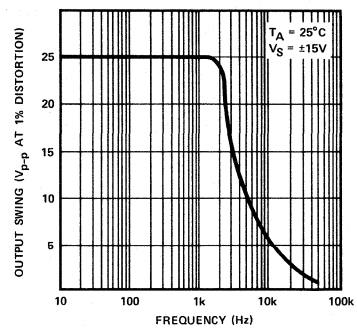
OPEN-LOOP GAIN AND PHASE SHIFT vs FREQUENCY



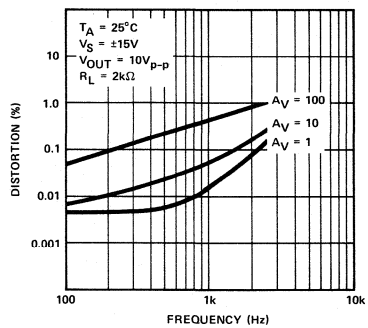
CLOSED-LOOP GAIN vs FREQUENCY



MAXIMUM OUTPUT SWING vs FREQUENCY

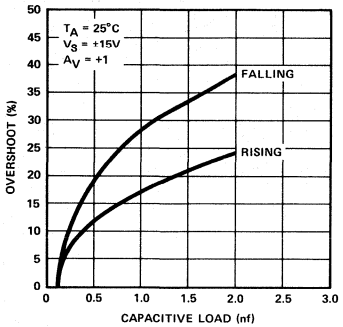


TOTAL HARMONIC DISTORTION vs FREQUENCY

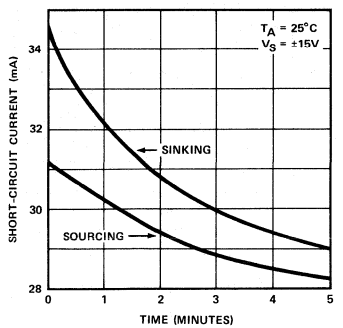


TYPICAL PERFORMANCE CHARACTERISTICS

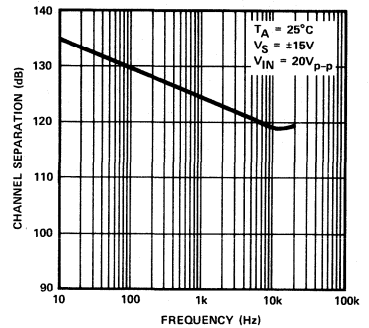
OVERSHOOT vs CAPACITIVE LOAD



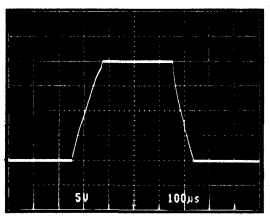
SHORT-CIRCUIT CURRENT vs TIME



CHANNEL SEPARATION vs FREQUENCY

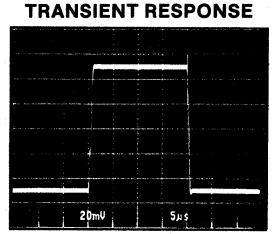


LARGE-SIGNAL TRANSIENT RESPONSE



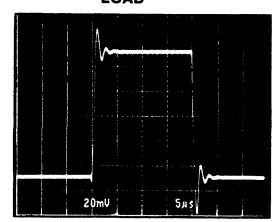
T_A = 25°C
V_S = ±15V
A_V = +1

SMALL-SIGNAL TRANSIENT RESPONSE



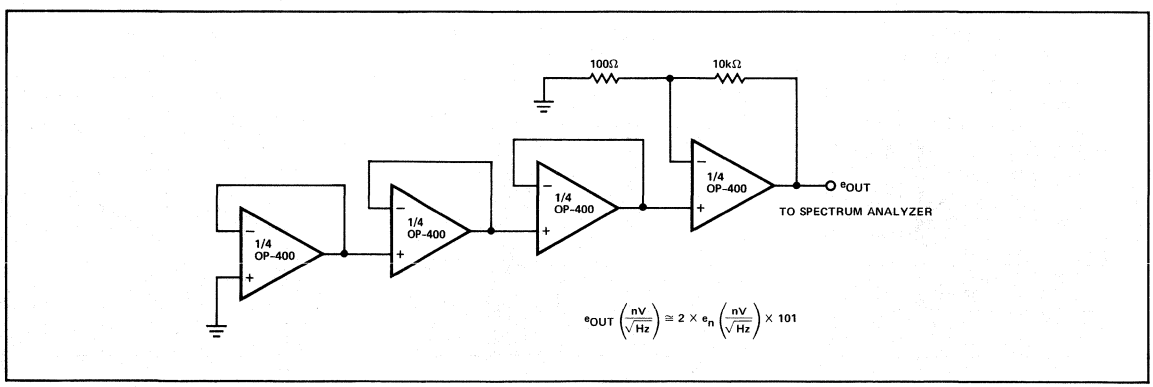
T_A = 25°C
V_S = ±15V
A_V = +1

SMALL-SIGNAL TRANSIENT RESPONSE C_{LOAD} = 1nF

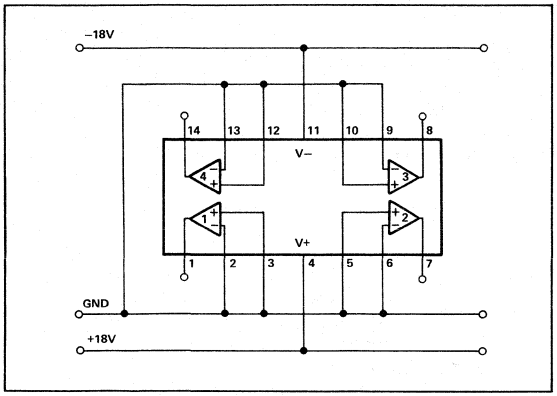


T_A = 25°C
V_S = ±15V
A_V = +1

NOISE TEST SCHEMATIC



BURN-IN CIRCUIT



APPLICATIONS INFORMATION

The OP-400 is inherently stable at all gains and is capable of driving large capacitive loads without oscillating. Nonetheless, good supply decoupling is highly recommended. Proper supply decoupling reduces problems caused by supply line noise and improves the capacitive load driving capability of the OP-400.

Total supply current can be reduced by connecting the inputs of an unused amplifier to V–. This turns the amplifier off, lowering the total supply current.

APPLICATIONS

DUAL LOW-POWER INSTRUMENTATION AMPLIFIER

A dual instrumentation amplifier that consumes less than 33mW of power per channel is shown in Figure 1. The linearity of the instrumentation amplifier exceeds 16 bits in gains of 5 to 200 and is better than 14 bits in gains from 200 to 1000. CMRR is above 115dB (Gain = 1000). Offset voltage drift is typically 0.4μV/°C over the military temperature range which is comparable to the best monolithic instrumentation amplifiers. The bandwidth of the low-power instrumentation amplifier is a function of gain and is shown below:

GAIN	BANDWIDTH
5	150kHz
10	67kHz
100	7.5kHz
1000	500Hz

The output signal is specified with respect to the reference input, which is normally connected to analog ground. The reference input can be used to offset the output from −10V to +10V if required.

FIGURE 1: Dual Low-Power Instrumentation Amplifier

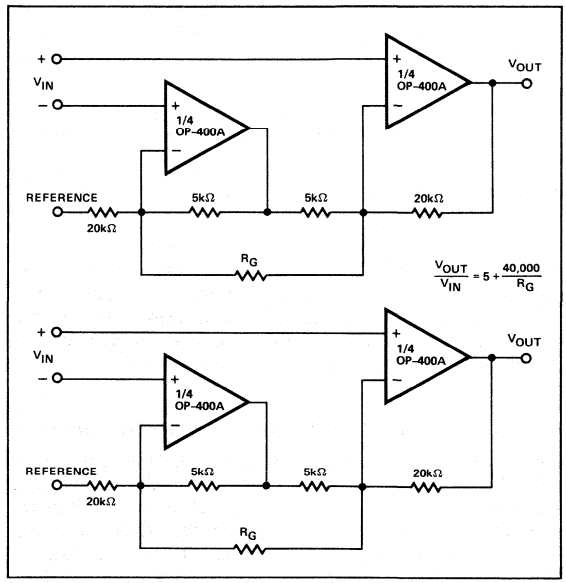
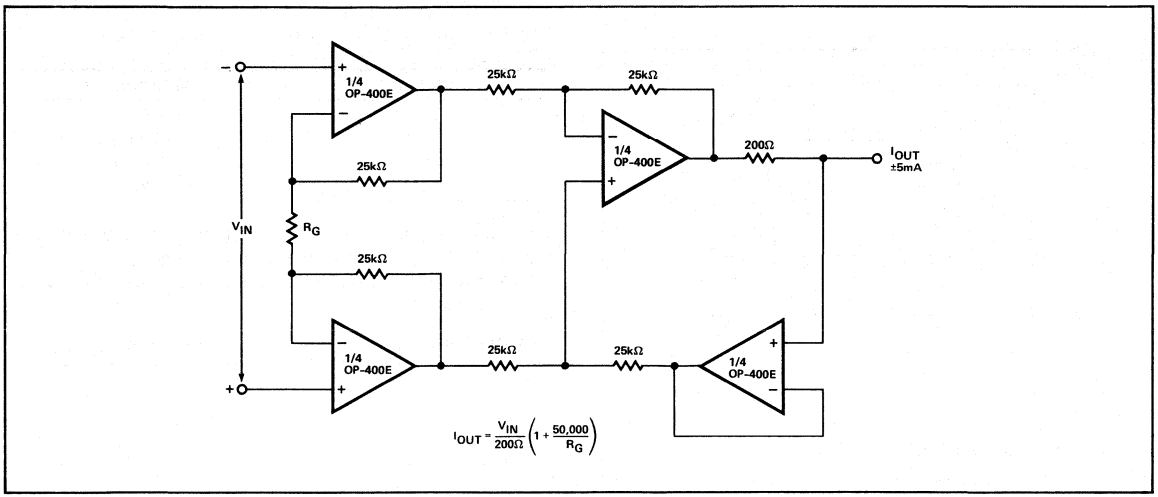


FIGURE 2: Bipolar Current Transmitter



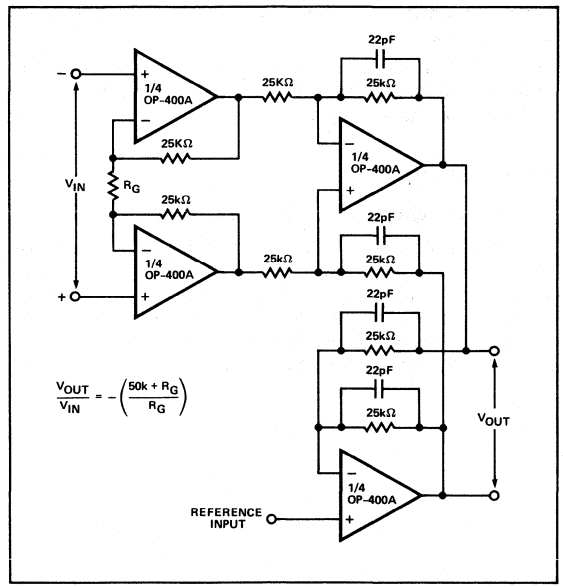
BIPOLAR CURRENT TRANSMITTER

In the circuit of Figure 2, which is an extension of the standard three op-amp instrumentation amplifier, the output current is proportional to the differential input voltage. Maximum output current is ±5mA with voltage compliance equal to ±10V when using ±15V supplies. Output impedance of the current transmitter exceeds 3MΩ and linearity is better than 16 bits with gain set for a full scale input of ±100μV.

DIFFERENTIAL OUTPUT INSTRUMENTATION AMPLIFIER

The output voltage swing of a single-ended instrumentation amplifier is limited by the supplies, normally at ±15V, to a maximum of $24V_{p-p}$. The differential output instrumentation amplifier of Figure 3 can provide an output voltage swing of $48V_{p-p}$ when operated with ±15V supplies. The extended output swing is due to the opposite polarity of the outputs. Both outputs will swing $24V_{p-p}$ but with opposite polarity, for a total output voltage swing of $48V_{p-p}$. The reference input can be used to set a common-mode output voltage over the range ±10V. PSRR of the amplifier is less than 1μV/V with CMRR (Gain = 1000) better than 115dB. Offset voltage drift is typically 0.4μV/°C over the military temperature range.

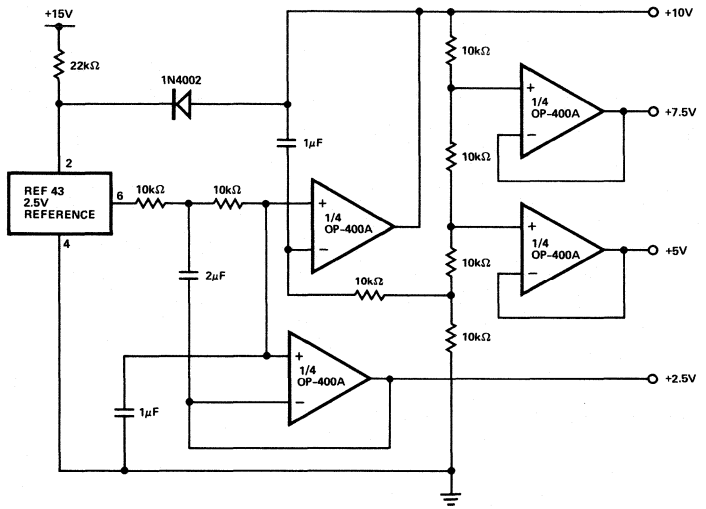
FIGURE 3: Differential Output Instrumentation Amplifier



MULTIPLE OUTPUT TRACKING VOLTAGE REFERENCE

Figure 4 shows a circuit that provides outputs of 10V, 7.5V, 5V, and 2.5V for use as a system voltage reference. Maximum output current from each reference is 5mA with load regulation under 25μV/mA. Line regulation is better than 15μV/V and output voltage drift is under 20μV/°C. Output voltage noise from 0.1Hz to 10Hz is typically 75μV_{p-p} from the 10V output and proportionately less from the 7.5V, 5V, and 2.5V outputs.

FIGURE 4: Multiple-Output Tracking Voltage Reference



ANALOG DEVICES

Quad Micropower Operational Amplifier

OP-420

FEATURES

- **Low Supply Current** ..... **200μA Max @ V_S = +5V**
- **Single-Supply Operation** ..... **+5V to +30V**
- **Dual-Supply Operation** ..... **±2.5V to ±15V**
- **Low Input Offset Voltage** ..... **500μV Typ**
- **Low Input Offset Voltage Drift** ..... **5μV/°C Typ**
- **High Common-Mode Input Range** ... **V− to (V+ − 1.5V)**
- **High CMRR** ..... **100dB Typ**
- **High Open-Loop Gain** ..... **1100V/mV Typ**
- **LM 148 Pinout**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (mV)	PACKAGE CERDIP 14-PIN	PACKAGE LCC 20-CONTACT	PACKAGE PLASTIC	OPERATING TEMPERATURE RANGE
2.5	OP420BY	–	–	MIL
2.5	OP420FY	–	–	IND
4.0	OP420CY	OP420CRC/883	–	MIL
4.0	OP420GY	–	OP420GP	XIND
4.0	–	–	OP420GS	XIND
6.0	OP420HY	–	OP420HP	XIND
6.0	–	–	OP420HS	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

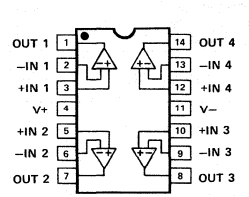
† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

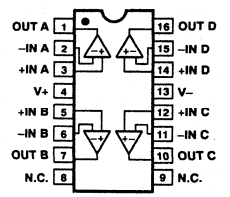
The OP-420 quad micropower operational amplifier is a single-chip quad patterned after the OP-20 precision micropower single operational amplifier. A Darlington PNP input stage allows the input common-mode voltage to include V−. The wide input range combined with low power-supply drain (~40μA/section at 5V), provides a unique solution for designs requiring high functional density and portable operation. Applications include two-wire transmitters for process control loops, battery-operated remote-line filters, signal preconditioning amplifiers, and a variety of multiple-gain block arrays.

For micropower applications requiring offset nulling, see the OP-20, OP-21 and OP-22 data sheets.

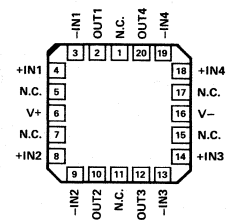
PIN CONNECTIONS



14-PIN HERMETIC DIP
(Y-Suffix)
14-PIN EPOXY DIP
(P-Suffix)

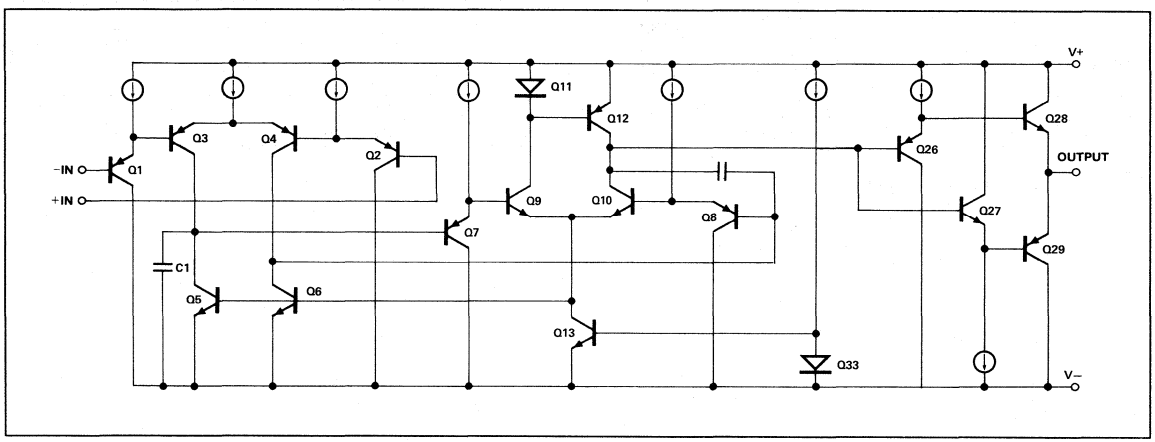


16-PIN SOL
(S-Suffix)



OP-420CRC/883
20-LEAD LCC
(RC-Suffix)

SIMPLIFIED SCHEMATIC (1/4 Shown)



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Differential Input Voltage ..... ±30V
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous
(One Amplifier Only)
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Operating Temperature Range
OP-420BY, OP-420CY, OP-420CRC ..... –55°C to +125°C
OP-420FY ..... –25°C to +85°C
OP-420G, OP-420H ..... –40°C to +85°C
Junction Temperature(T_J) ..... –65°C to +150°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
14-Pin Hermetic DIP (Y)	99	12	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

			OP-420B OP-420F			OP-420C OP-420G			OP-420H			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	0.5	2.5	—	1	4	—	2	6	mV
Input Offset Current (Note 1)	I_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	0.5	1.5	—	0.8	2.5	—	1.2	6	nA
Input Bias Current (Note 1)	I_B	$V_S = \pm 2.5V$ to $\pm 15V$	—	9	20	—	12	30	—	18	40	nA
Input Noise Voltage Density	e_n	$f_O = 10Hz$ $f_O = 100Hz$	—	50	—	—	50	—	—	50	—	$nV/\sqrt{Hz}$
Input Noise Current Density	i_n	$f_O = 10Hz$ $f_O = 100Hz$	—	0.12	—	—	0.12	—	—	0.12	—	$pA/\sqrt{Hz}$
Input Voltage Range	IVR	V+ = +5V, V– = 0V $V_S = \pm 15V$	0/3.5 –15/13.5	— —	— —	0/3.5 –15/13.5	— —	— —	0/3.5 –15/13.5	— —	— —	V
Common-Mode Rejection Ratio	CMRR	V+ = +5V, V– = 0V $0V \le V_{CM} \le 3.5V$ $V_S = \pm 15V$ $-15V \le V_{CM} \le 13.5V$	83 83	100 100	— —	80 80	96 96	— —	76 76	90 90	— —	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$; & V– = 0V, V+ = 5V to 30V	—	10	30	—	20	50	—	30	80	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L = 25k\Omega$, $V_O = \pm 10V$	600	1100	—	400	900	—	200	800	—	V/mV
Slew Rate	SR		—	0.05	—	—	0.05	—	—	0.05	—	V/μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1.0$ $R_L = 10k\Omega$	—	150	—	—	150	—	—	150	—	kHz
Output Voltage Swing	V_O	V+ = 5V, V– = 0V, $R_L = 10k\Omega$ $V_S = \pm 15V$, $R_L = 25k\Omega$	0.7/4.1 ±14.0	— —	— —	0.8/4.0 ±14.0	— —	— —	0.9/3.8 ±13.8	— —	— —	V
Supply Current (Four Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load $V_S = \pm 15V$, No Load	— —	140 330	200 360	— —	170 360	300 460	— —	200 390	400 600	μA

NOTE:
1. I_B and I_{OS} are measured at $V_{CM} = 0$.

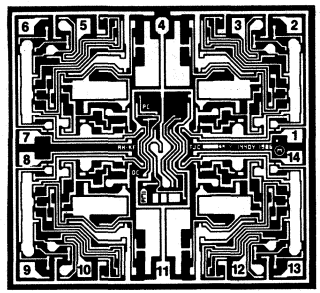
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le +125°C$ for OP-420B and OP-420C, $-25°C \le T_A \le +85°C$ for OP-420F, $-40°C \le T_A \le +85°C$ for OP-420G and OP-420H, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-420B OP-420F MIN	OP-420B OP-420F TYP	OP-420B OP-420F MAX	OP-420C OP-420G MIN	OP-420C OP-420G TYP	OP-420C OP-420G MAX	OP-420H MIN	OP-420H TYP	OP-420H MAX	UNITS
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	Unnulled	—	5	10	—	8	15	—	15	25	µV/°C
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	—	3.5	—	—	5.5	—	—	7.5	mV
Input Offset Current (Note 2)	I_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	—	3	—	—	4	—	—	8	nA
Input Bias Current (Note 2)	I_B	$V_S = \pm 2.5V$ to $\pm 15V$	—	—	30	—	—	40	—	—	60	nA
Input Voltage Range	IVR	V+ = +5V, V− = 0V $V_S = \pm 15V$	0/3.2 −15/13.2	— —	— —	0/3.2 −15/13.2	— —	— —	0/3.2 −15/13.2	— —	— —	V
Common-Mode Rejection Ratio	CMRR	V+ = +5V, V− = 0V, $0V \le V_{CM} \le 3.2V$ $V_S = \pm 15V$, $-15V \le V_{CM} \le 13.2V$	76 76	96 96	— —	73 73	92 92	— —	73 73	86 86	— —	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ and V− = 0V, V+ = 5V to 30V	—	15	50	—	25	80	—	40	100	µV/V
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 50k\Omega$, $V_O = \pm 10V$	300	800	—	200	650	—	100	400	—	V/mV
Output Voltage Swing	V_O	V+ = 5V, V− = 0V, $R_L = 20k\Omega$ $V_S = \pm 15V$, $R_L = 50k\Omega$	0.9/3.9 ±13.8	— —	— —	1.0/3.8 ±13.8	— —	— —	1.1/3.6 ±13.6	— —	— —	V
Supply Current (Four Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load $V_S = \pm 15V$, No Load	— —	170 390	300 500	— —	210 420	400 640	— —	250 500	600 800	µA

NOTES:
1. Sample tested.
2. I_B and I_{OS} are measured at $V_{CM} = 0$.

OP-420

DICE CHARACTERISTICS



DIE SIZE 0.093 × 0.087 inch, 8091 sq. mils
(2.36 × 2.21 mm, 5.22 sq. mm)

1. **OUTPUT 1**
2. **INVERTING INPUT 1**
3. **NONINVERTING INPUT 1**
4. **V+**
5. **NONINVERTING INPUT 2**
6. **INVERTING INPUT 2**
7. **OUTPUT 2**
8. **OUTPUT 3**
9. **INVERTING INPUT 3**
10. **NONINVERTING INPUT 3**
11. **V−**
12. **NONINVERTING INPUT 4**
13. **INVERTING INPUT 4**
14. **OUTPUT 4**

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

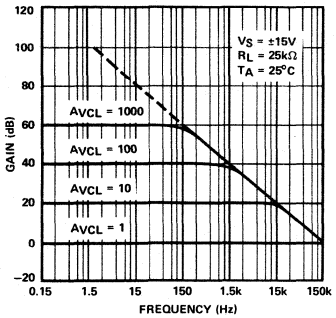
PARAMETER	SYMBOL	CONDITIONS	OP-420N LIMIT	OP-420G LIMIT	OP-420GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	2.5	4	6	mV MAX
Input Offset Current	I_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$, (Note 1)	1.5	2.5	6	nA MAX
Input Bias Current	I_B	$V_S = \pm 2.5V$ to $\pm 15V$, (Note 1)	20	30	40	nA MAX
Input Voltage Range	IVR		−15/13.5	−15/13.5	−15/13.5	V MIN
Common-Mode Rejection Ratio	CMRR	V+ = +5V, V− = 0V $0V \le V_{CM} \le 3.5V$ $V_S = \pm 15V$, $-15V \le V_{CM} \le 13.5V$	83 83	80 80	76 76	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ V− = 0V, V+ = +5V to +30V	30	50	80	μV/V MAX
Large-Signal Voltage Gain	A_{VO}	$R_L = 25k\Omega$, $V_O = \pm 10V$	600	400	200	V/mV MIN
Output Voltage Swing	V_O	V+ = +5V, V− = 0V $R_L = 10k\Omega$ $V_S = \pm 15V$ $R_L = 25k\Omega$	0.7/4.1 ±14.0	0.8/4.0 ±14.0	0.9/3.8 ±13.8	VMAX V MIN
Supply Current	I_{SY}	No Load, (Four Amplifiers)	360	460	600	μA MAX

NOTES:
1. I_B and I_{OS} are measured at $V_{CM} = 0$.

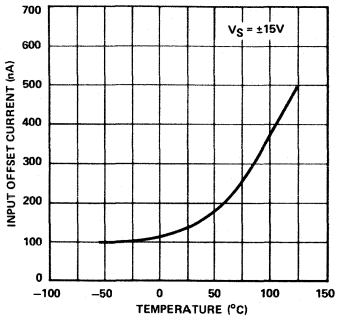
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

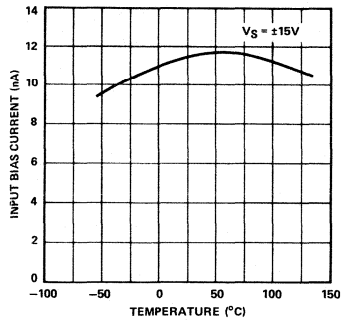
CLOSED-LOOP GAIN vs FREQUENCY



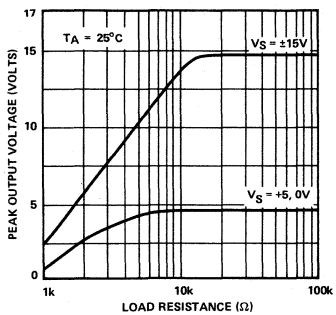
INPUT OFFSET CURRENT vs TEMPERATURE



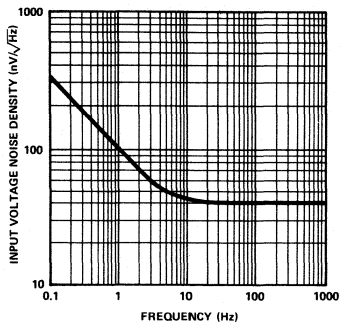
INPUT BIAS CURRENT vs TEMPERATURE



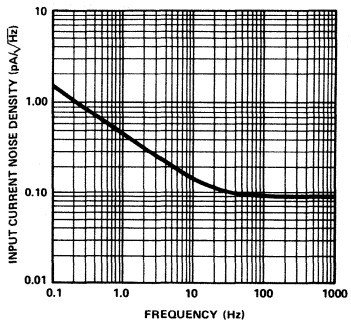
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



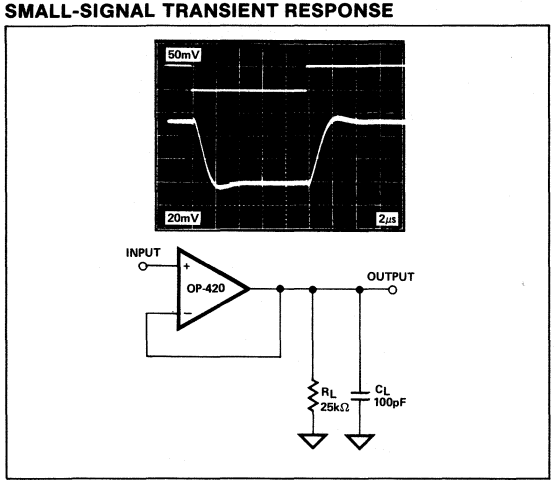
INPUT VOLTAGE NOISE DENSITY (e_n) vs FREQUENCY



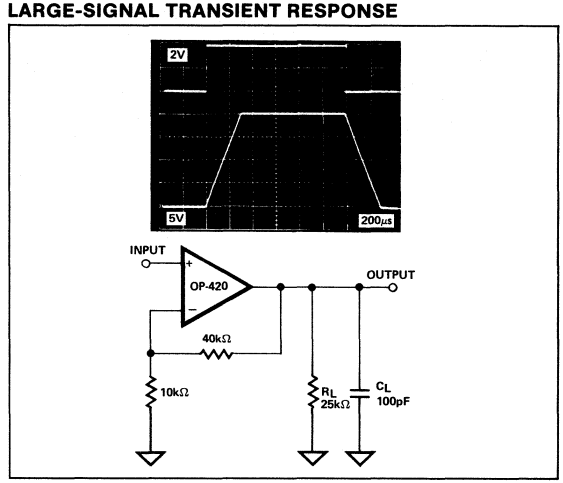
INPUT CURRENT NOISE DENSITY (i_n) vs FREQUENCY



SMALL-SIGNAL TRANSIENT RESPONSE



LARGE-SIGNAL TRANSIENT RESPONSE



Quad Low-Power Operational Amplifier, Single or Dual Supply

OP-421

FEATURES

- **Low Supply Current** ..... **1mA Max**
- **Slew Rate** ..... **0.25V/μs Min**
- **Single Supply Operation** ..... **+5V to +30V**
- **Low Input Offset Voltage** ..... **500μV Typ**
- **Low Input Offset Voltage Drift** ..... **10μV/°C Max**
- **High Common-Mode Input Range** ... **V− to V+ (−1.5V)**
- **High CMRR** ..... **100dB Typ**
- **High Open-Loop Gain** ..... **400V/mV Typ**
- **Single-Chip Monolithic Construction**
- **Pin Compatible With LM124, LM324, LM148, and OP-11**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (mV)	PACKAGE CERDIP 14-PIN	PLASTIC	SO	OPERATING TEMPERATURE RANGE
2.5	OP421BY*	–	–	MIL
2.5	OP421FY	–	–	IND
4.0	OP421CY*	–	–	MIL
4.0	OP421GY	OP421GP	OP421GS	XIND
6.0	OP421HY	OP421HP	OP421HS	XIND

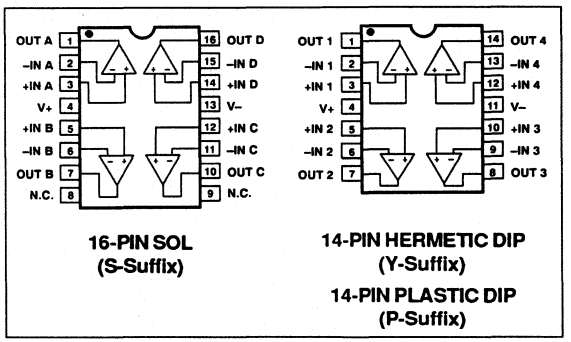
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

The OP-421 quad low-power operational amplifier is a single-chip quad patterned after the OP-21 single operational amplifier. The PNP input stage allows the input common-mode voltage to include V−. Featuring a low power-supply current (150μA/section typical at 5V), the OP-421 offers a unique solution for designs requiring a combination of high function density, wide bandwidth, and low-power operation. Applications for the OP-421 include low-power active filters, battery-operated remote line filters, and signal preconditioning amplifiers. In addition, the ever-present problem of crossover distortion in low-power devices is eliminated by a unique double-buffered output section.

PIN CONNECTIONS

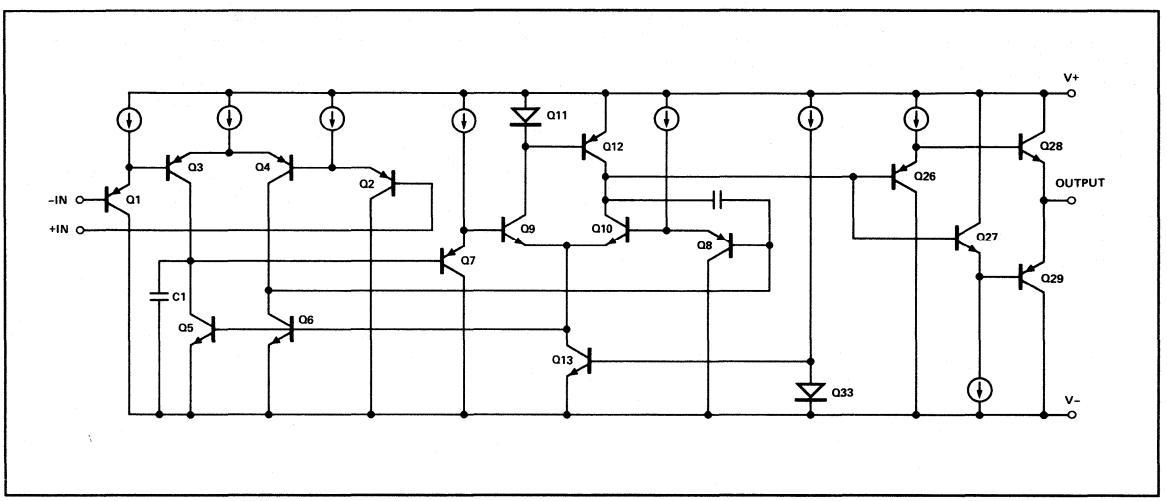


16-PIN SOL (S-Suffix)

14-PIN HERMETIC DIP (Y-Suffix)

14-PIN PLASTIC DIP (P-Suffix)

SIMPLIFIED SCHEMATIC (1/4 Shown)



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Differential Input Voltage ..... ±30V
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous
(One Amplifier Only)
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Operating Temperature Range
OP-421BY, OP-421CY ..... –55°C to +125°C
OP-421FY ..... –25°C to +85°C
OP-421G, OP421H ..... –40°C to +85°C

Junction Temperature (T_j) ..... –65°C to +150°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
14-Pin Hermetic DIP (Y)	99	12	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

			OP-421B OP-421F			OP-421C OP-421G			OP-421H			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	0.5	2.5	—	1	4	—	2	6	mV
Input Offset Current	I_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	0.6	5.0	—	2.0	10	—	5.0	20	nA
Input Bias Current	I_B	$V_S = \pm 2.5V$ to $\pm 15V$	—	20	50	—	50	80	—	100	150	nA
Input Noise Voltage Density	e_n	$f_O = 10Hz$ (Note 1)	—	20	40	—	20	40	—	20	40	$nV/\sqrt{Hz}$
		$f_O = 100Hz$ (Note 1)	—	15	30	—	15	30	—	15	30	
Input Noise Current Density	i_n	$f_O = 10Hz$ (Note 1)	—	0.3	0.6	—	0.3	0.6	—	0.3	0.6	$pA/\sqrt{Hz}$
		$f_O = 100Hz$ (Note 1)	—	0.2	0.4	—	0.2	0.4	—	0.2	0.4	
Input Voltage Range	IVR	V+ = +5V, V– = 0V	0/3.5	—	—	0/3.5	—	—	0/3.5	—	—	V
		$V_S = \pm 15V$	–15/13.5	—	—	–15/13.5	—	—	–15/13.5	—	—	
Common-Mode Rejection Ratio	CMRR	V+ = +5V, V– = 0V, $0V \le V_{CM} \le +3.5V$	83	100	—	80	96	—	76	90	—	dB
		$V_S = \pm 15V$, $-15V \le V_{CM} \le +13.5V$	83	100	—	80	96	—	76	90	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$; & V– = 0V, V+ = 5V to 30V	—	10	30	—	20	50	—	30	80	μV/V
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$, $R_L = 10k\Omega$	200	400	—	100	200	—	100	200	—	V/mV
Output Voltage Swing	V_O	V+ = 5V, V– = 0V, $R_L = 5k\Omega$	0.7/4.0	—	—	0.8/3.9	—	—	0.9/3.8	—	—	V
		$V_S = \pm 15V$, $R_L = 10k\Omega$	±14	—	—	±13.9	—	—	±13.8	—	—	
Closed-Loop Bandwidth (Note 2)	BW	$A_{VCL} = +1.0$, $R_L = 10k\Omega$	1.0	1.9	—	1.0	1.9	—	1.0	1.9	—	MHz
Supply Current (Four Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load	—	0.6	1.0	—	0.7	1.5	—	0.9	2.0	mA
		$V_S = \pm 15V$, No Load	—	1.2	1.8	—	1.4	2.3	—	1.8	3.0	
Slew Rate	SR	(Note 1)	0.25	0.5	—	0.25	0.5	—	0.25	0.5	—	V/μs
Channel Separation	CS	(Note 1)	100	120	—	100	120	—	100	120	—	dB

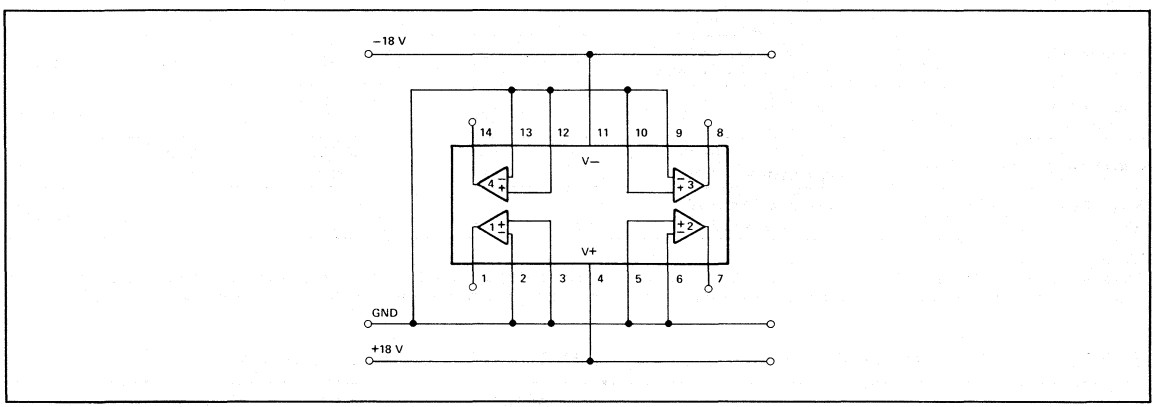
NOTES:
1. Sample tested.
2. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$ for OP-421B and OP-421C, $-25°C \le T_A \le +85°C$ for OP-421F, and $-40°C \le T_A \le +85°C$ for OP-421G and OP-421H, unless otherwise noted.

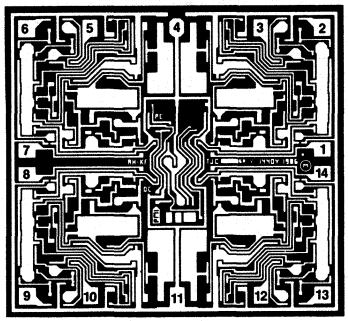
			OP-421B OP-421F			OP-421C OP-421G			OP-421H			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}		—	5	10	—	8	15	—	10	15	µV/°C
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	1	3.5	—	1.8	5.5	—	3	7.5	mV
Input Offset Current	I_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	1.6	8	—	3.0	15	—	6.0	30	nA
Input Bias Current	I_B	$V_S = \pm 2.5V$ to $\pm 15V$	—	25	70	—	60	125	—	140	230	nA
Input Voltage Range	IVR	V+ = +5V, V− = 0V $V_S = \pm 15V$	0/3.2 −15/13.2	—	—	0/3.2 −15/13.2	—	—	0/3.2 −15/13.2	—	—	V
Common-Mode Rejection Ratio	CMRR	V+ = +5V, V− = 0V, $0V \le V_{CM} \le +3.2V$ $V_S = \pm 15V$, $-15V \le V_{CM} \le +13.2V$	78 78	96 96	—	74 74	94 94	—	73 73	86 86	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$; & V− = 0V, V+ = 5V to 30V	— —	15 15	50 50	— —	25 25	80 80	— —	40 40	100 100	µV/V
Large-Signal Voltage Gain	A_{VO}	$V_O = 10V$ $R_L = 20k\Omega$	100	200	—	50	100	—	50	100	—	V/mV
Output Voltage Swing	V_O	V+ = 5V, V− = 0V $R_L = 10k\Omega$ $V_S = \pm 15V$, $R_L = 20k\Omega$	0.8/3.9 ±13.8	—	—	0.9/3.8 ±13.7	—	—	1.0/3.7 ±13.7	—	—	V
Supply Current (Four Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load $V_S = \pm 15V$, No Load	— 0.68	1.2 2.0	1.5 2.5	— 0.68	1.5 2.5	2.0 3.2	— 0.68	2.0 3.2	3.0 4.0	mA

NOTE:
1. Sample tested.

BURN-IN CIRCUIT



DICE CHARACTERISTICS



DIE SIZE 0.093 × 0.087 inch, 8091 sq. mils
(2.36 × 2.21 mm, 5.22 sq. mm)

1. OUTPUT 1
2. INVERTING INPUT 1
3. NONINVERTING INPUT 1
4. V+
5. NONINVERTING INPUT 2
6. INVERTING INPUT 2
7. OUTPUT 2
8. OUTPUT 3
9. INVERTING INPUT 3
10. NONINVERTING INPUT 3
11. V−
12. NONINVERTING INPUT 4
13. INVERTING INPUT 4
14. OUTPUT 4

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-421N LIMIT	OP-421G LIMIT	OP-421GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	2.5	4	6	mV MAX
Input Offset Current	I_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	5	10	20	nA MAX
Input Bias Current	I_B	$V_S = \pm 2.5V$ to $\pm 15V$	50	80	150	nA MAX
Input Voltage Range	IVR		−15/13.5	−15/13.5	−15/13.5	V MIN
Common-Mode Rejection Ratio	CMRR	V+ = +5V, V− = 0V $0V \le V_{CM} \le +3.5V$ $V_S = \pm 15V$, $-15V \le V_{CM} \le +13.5V$	83	80	76	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$; and V− = 0V, V+ = +5V to 30V	30	50	80	μV/V MAX
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 20k\Omega$	200	200	100	V/mV MIN
Output Voltage Swing	V_O	V+ = +5V, V− = 0V, $R_L = 5k\Omega$ $V_S = \pm 15V$, $R_L = 10k\Omega$	0.7/4.0 ±14	0.8/3.9 ±13.9	0.9/3.8 ±13.8	V MIN
Supply Current (Four Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load $V_S = \pm 15V$, No Load	1.0 1.8	1.5 2.3	2.0 3.0	mA MAX

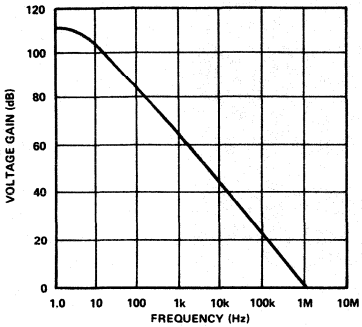
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$, unless otherwise noted.

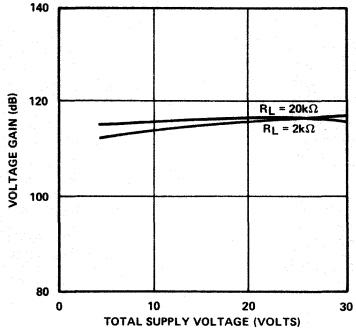
PARAMETER	SYMBOL	CONDITIONS	OP-421N TYPICAL	OP-421G TYPICAL	OP-421GR TYPICAL	UNITS
Input Noise Voltage Density	e_n	$f_O = 10Hz$ $f_O = 100Hz$	20 15	20 15	20 15	$nV/\sqrt{Hz}$
Closed-Loop Bandwidth	BW	$A_{VCL} = +1.0$ $R_L = 10k\Omega$	1.9	1.9	1.9	MHz
Slew Rate	SR		0.5	0.5	0.5	V/μs
Channel Separation	CS		120	120	120	dB

TYPICAL PERFORMANCE CHARACTERISTICS

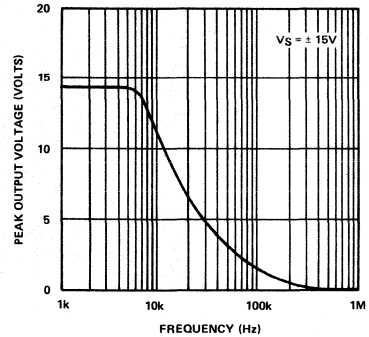
OPEN-LOOP FREQUENCY RESPONSE



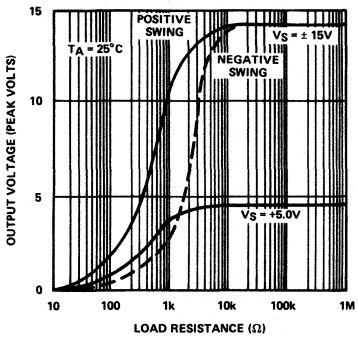
OPEN-LOOP GAIN vs POWER SUPPLY VOLTAGE



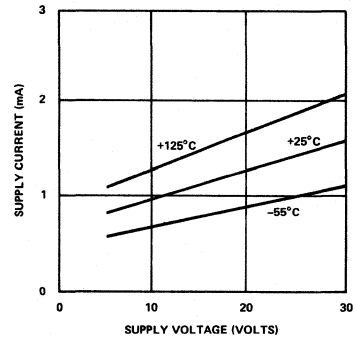
OUTPUT SWING vs FREQUENCY



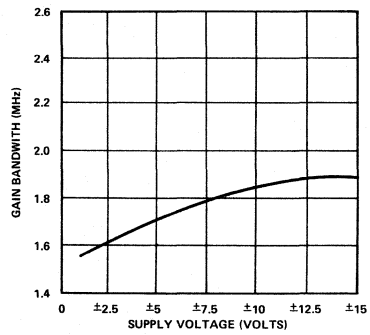
OUTPUT SWING vs OUTPUT LOAD



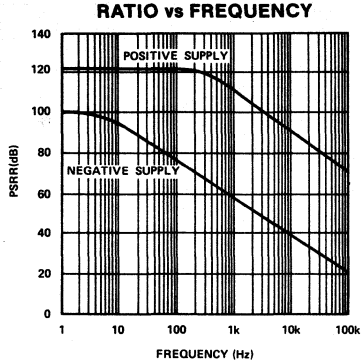
SUPPLY CURRENT vs SUPPLY VOLTAGE



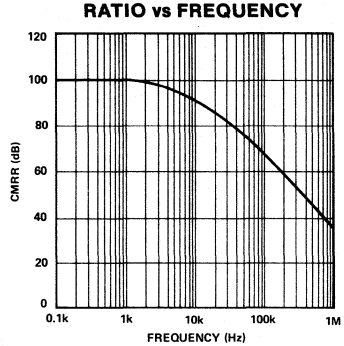
GAIN BANDWIDTH vs SUPPLY VOLTAGE



POWER SUPPLY REJECTION RATIO vs FREQUENCY

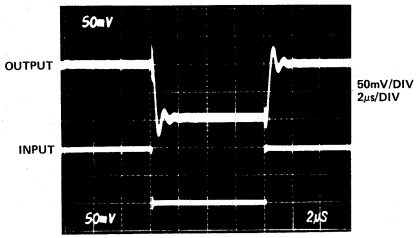


COMMON-MODE REJECTION RATIO vs FREQUENCY



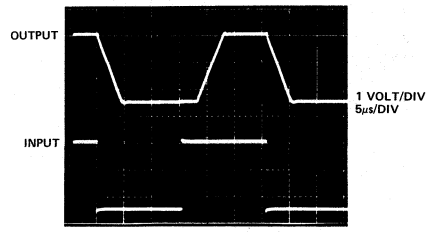
TYPICAL PERFORMANCE CHARACTERISTICS

VOLTAGE FOLLOWER SMALL-SIGNAL RESPONSE



V_S = 0V, +15V
R_L = 10kΩ
T_A = 25°C
C_L = 50pf

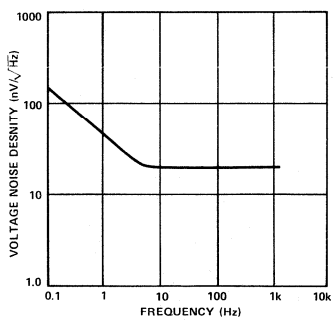
VOLTAGE FOLLOWER LARGE-SIGNAL RESPONSE



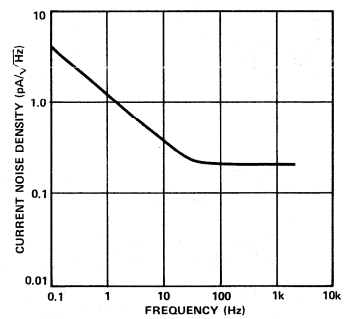
V_S = 0V, +15V
R_L = 10kΩ
T_A = 25°C
C_L = 50pf

NOISE CHARACTERISTICS

INPUT NOISE VOLTAGE DENSITY vs FREQUENCY



INPUT NOISE CURRENT DENSITY vs FREQUENCY



ANALOG DEVICES

Quad Precision, High Speed Operational Amplifier

OP-467

FEATURES
- High Slew Rate – 170 V/μs
- Wide Bandwidth – 30 MHz
- Fast Settling Time – <170 ns to 0.01%
- Low Offset Voltage – 200 μV
- Unity-Gain Stable
- Low Voltage Operation ±5 V to ±15 V
- Low Supply Current – <8 mA
- Drives Capacitive Loads

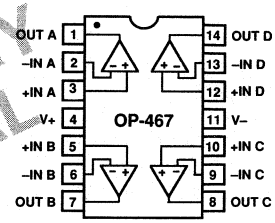
APPLICATIONS
- High Speed Image Display Drivers
- Active Filters
- Fast Amplifiers
- Integrators
- Photo Diode Preamps

PRELIMINARY TECHNICAL DATA

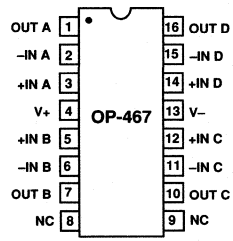
PIN CONNECTIONS

14-Lead Ceramic DIP (Y Suffix)

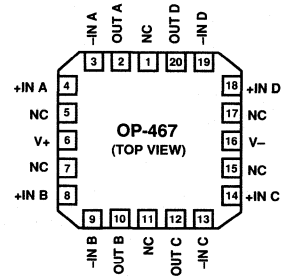
14-Lead Epoxy DIP (P Suffix)



16-Lead SOL (S Suffix)



20-Position Chip Carrier (RC Suffix)



GENERAL DESCRIPTION

The OP-467 is a quad, high speed, precision operational amplifier. It offers the performance of a high speed op amp combined with the advantages of a precision operational amplifier all in a single package. OP-467 is an ideal choice for applications where, traditionally, more than one op amp was used to achieve high performance.

OP-467 internal compensation ensures stable unity-gain operation and can drive large capacitive loads without oscillations. With a gain bandwidth product of 30 MHz driving a 30 pF load, output slew rate in excess of 170 V/μs and settling time to 0.01% in less than 170 ns, provides excellent dynamic accuracy in high speed data-acquisition systems. The channel-to-channel separation is typically 60 dB at 10 MHz.

The dc performance of OP-467 includes less than 1 mV of offset, voltage noise density below 6 nV/$\sqrt{\text{Hz}}$ and total supply current under 8 mA. Common-mode rejection and power supply rejection ratios are typically 80 dB. PSRR is maintained to better than 40 dB with input frequencies as high as 1 MHz. The low offset and drift plus high speed and low noise, make the OP-467 usable in applications such as high speed detectors and instrumentation.

The OP-467 is specified for operation from ±5 V to ±15 V over the extended industrial temperature range (−40°C to +85°C) and is available in plastic and ceramic DIP, plus SOL and LCC surface mount packages.

Contact your local sales office for MIL-STD-883 data sheet and availability.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

OP-467—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			0.2	1	mV
		$-40°C \le T_A \le +85°C$				mV
Input Bias Current	I_B	V_{CM} = 0 V		100		nA
		V_{CM} = 0 V				nA
Input Offset Current	I_{OS}	V_{CM} = 0 V				nA
		V_{CM} = 0 V				nA
Common-Mode Rejection	CMR	V_{CM} = ±11 V, $-40°C \le T_A \le +85°C$	76	80		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ	83	80		dB
		R_L = 2 kΩ, $-40°C \le T_A \le +85°C$				dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			3.5		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$					pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 2 kΩ	−13.0	±13.5	13	V
Open-Loop Output Impedance	Z_{OUT}	f = 1 MHz				Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±18 V	76			
		$-40°C \le T_A \le +85°C$		100		dB
Supply Current	I_{SY}	V_O = 0 V, $-40°C \le T_A \le +85°C$		8		mA
Supply Voltage Range	V_S		±4.5		±18	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ	150	170		V/µs
Full-Power Bandwidth	BW_p	1% Distortion		2.7		MHz
Settling Time	t_s	To 0.01%		170		ns
Gain Bandwidth Product	GBP			25		MHz
Phase Margin	θo			45		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p–p	0.1 Hz to 10 Hz				µV p–p
Voltage Noise Density	e_n	f = 1 kHz		6		nV/$\sqrt{Hz}$
Current Noise Density	i_n					pA/$\sqrt{Hz}$

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ELECTRICAL CHARACTERISTICS (@ V_S = ±5 V, T_A = +25°C unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			1		mV
		$-40°C \le T_A \le +85°C$				mV
Input Bias Current	I_B	V_{CM} = 0 V		100		nA
		V_{CM} = 0 V				nA
Input Offset Current	I_{OS}	V_{CM} = 0 V				nA
		V_{CM} = 0 V				nA
Common-Mode Rejection	CMR	V_{CM} = ±2.5 V, $-40°C \le T_A \le +85°C$		80		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ		80		dB
		R_L = 2 kΩ, $-40°C \le T_A \le +85°C$				dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$					μV/°C
Bias Current Drift	$\Delta I_B/\Delta T$					pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 2 kΩ		±3.5		V
Open-Loop Output Impedance	Z_{OUT}	f = 1 MHz				Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to 5.5 V				
		$-40°C \le T_A \le +85°C$		100		dB
Supply Current	I_{SY}	V_O = 0 V, $-40°C \le T_A \le +85°C$		8		mA
Supply Voltage Range	V_S		±4.5		±18	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		170		V/μs
Full-Power Bandwidth	BW_p	1% Distortion		2.5		MHz
Settling Time	t_s	To 0.01%		200		ns
Gain Bandwidth Product	GBP			25		MHz
Phase Margin	θo			45		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p–p	0.1 Hz to 10 Hz				μV p–p
Voltage Noise Density	e_n	f = 1 kHz		6		nV/$\sqrt{Hz}$
Current Noise Density	i_n					pA/$\sqrt{Hz}$

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

2

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

WAFER TEST LIMITS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise specified.)

Parameter	Symbol	Conditions	Limit	Units
Offset Voltage	V_{OS}		±250	μV typ
Input Bias Current	I_B	V_{CM} = 0 V	60	nA typ
Input Offset Current	I_{OS}	V_{CM} = 0 V	10	nA typ
Input Voltage Range[1]				V min/max
Common-Mode Rejection	CMRR	V_{CM} = ±13 V	90	dB typ
Power Supply Rejection Ratio	PSRR	V = ±4.5 V to ±18 V	100	dB typ
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ	20	V/mV typ
Output Voltage Range	V_O	R_L = 2 kΩ	±13	V typ
Supply Current	I_{SY}	V_O = 0 V, R_L = ∞	8	mA typ

NOTES
Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.
[1]Guaranteed by CMR test.

PRELIMINARY TECHNICAL DATA

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Input Voltage[2] . . . . . ±18 V
Differential Input Voltage[2] . . . . . 36 V
Output Short-Circuit Duration . . . . . Limited
Storage Temperature Range
  Y, RC Package . . . . . −65°C to +175°C
  P, S Package . . . . . −65°C to +150°C
Operating Temperature Range
  OP-467A . . . . . −55°C to +125°C
  OP-467G . . . . . −40°C to +85°C
Junction Temperature Range
  Y, RC Package . . . . . −65°C to +125°C
  P, S Package . . . . . −65°C to +125°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C

Package Type	θ_{JA}[3]	θ_{JC}	Units
14-Pin Cerdip (Y)	94	10	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
16-Pin SOL (S)	88	23	°C/W
20-Contact LCC (RC)	78	33	°C/W

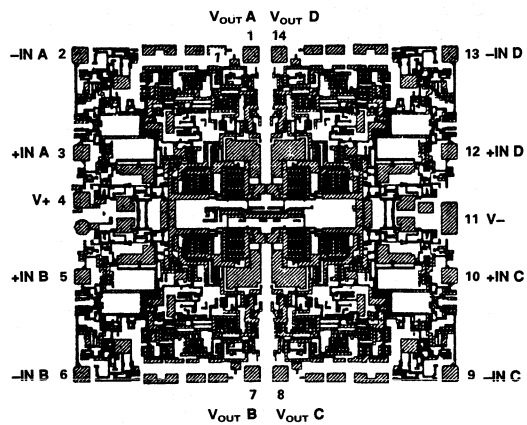
NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.
[3]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered in circuit board for SOIC package.

ORDERING GUIDE

Model	Temperature Range	Package Option*
OP467AY/883	−55°C to +125°C	14-Pin Cerdip
OP467ARC/883	−55°C to +125°C	20-Contact LCC
OP467GP	−40°C to +85°C	14-Pin Plastic DIP
OP467GS	−40°C to +85°C	16-Pin SOL
OP467GBC	+25°C	DICE

*For outline information see Package Information section.

DICE CHARACTERISTICS



OP-467 Die Size 0.111 X 0.100 inch, 11,100 sq. mils

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ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, T_A = +25°C unless otherwise specified.)

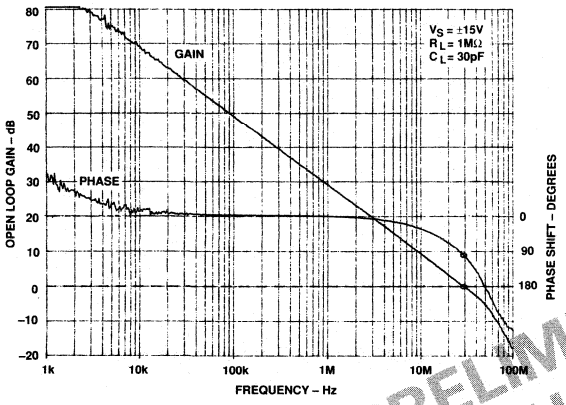


Figure 1. Open-Loop Gain, Phase vs. Frequency

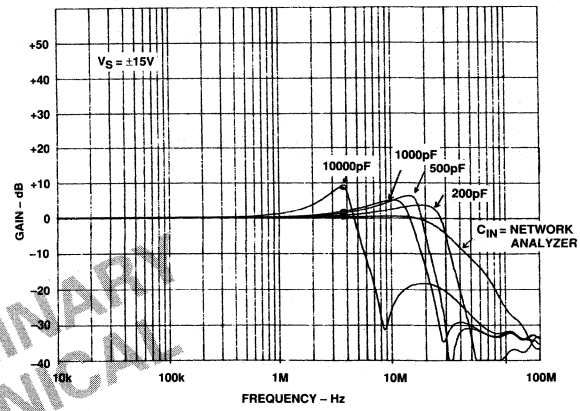


Figure 2. Noninverting Gain vs. Capacitive Loads

PRELIMINARY TECHNICAL DATA

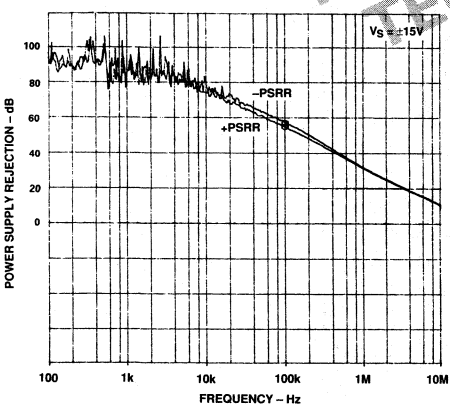


Figure 3. Power Supply Rejection vs. Frequency

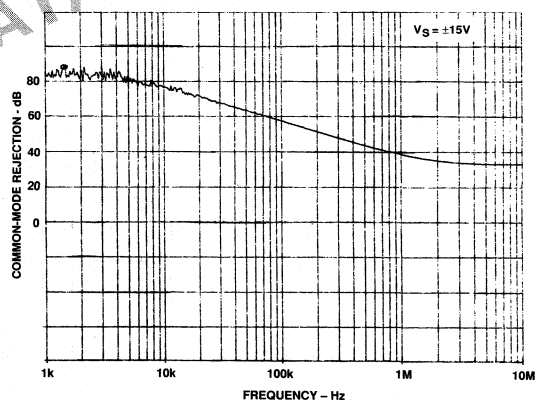


Figure 4. Common-Mode Rejection vs. Frequency

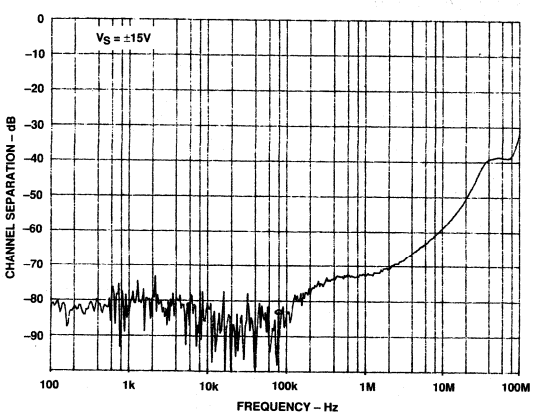


Figure 5. Channel Separation vs. Frequency

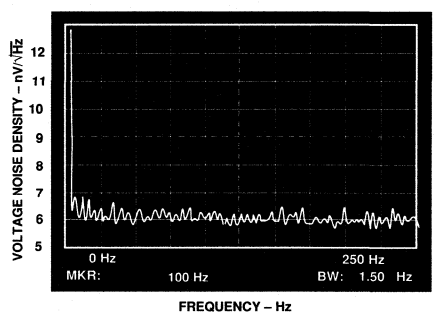


Figure 6. Voltage Noise Density vs. Frequency

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, T_A = +25°C unless otherwise specified.)

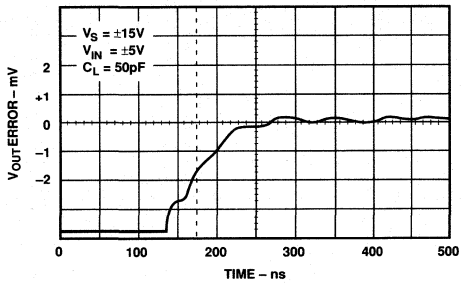


Figure 7. Settling Time, Negative Edge

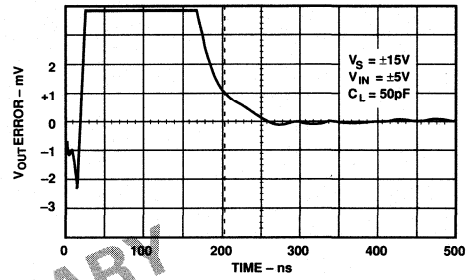


Figure 8. Settling Time, Positive Edge

PRELIMINARY TECHNICAL DATA

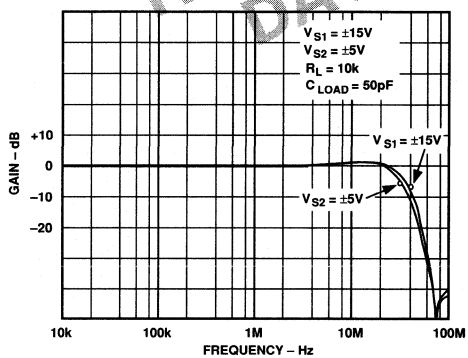


Figure 9. Noninverting Gain vs. Supply Voltage

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ANALOG DEVICES

Very Low-Noise Quad Operational Amplifier

OP-470

FEATURES

- **Very Low Noise** ..... 5nV/$\sqrt{Hz}$ @ 1kHz Max
- **Excellent Input Offset Voltage** ..... 0.4mV Max
- **Low Offset Voltage Drift** ..... 2μV/°C Max
- **Very High Gain** ..... 1000V/mV Min
- **Outstanding CMR** ..... 110dB Min
- **Slew Rate** ..... 2V/μs Typ
- **Gain-Bandwidth Product** ..... 6MHz Typ
- **Industry Standard Quad Pinouts**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (μV)	PACKAGE			OPERATING TEMPERATURE RANGE
	CERDIP 14-PIN	PLASTIC	LCC*	
400	–	–	OP470ARC/883	MIL
400	OP470AY*	–	OP470ATC/883	MIL
400	OP470EY	–	–	IND
800	OP470FY	–	–	IND
1000	–	OP470GP	–	XIND
1000	–	OP470GS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

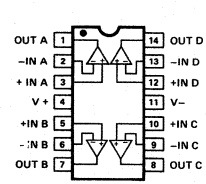
†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

The OP-470 is a high-performance monolithic quad operational amplifier with exceptionally low voltage noise, 5nV/$\sqrt{Hz}$ at 1kHz Max, offering comparable performance to PMI's industry standard OP-27.

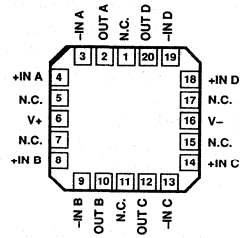
The OP-470 features an input offset voltage below 0.4mV, excellent for a quad op amp, and an offset drift under 2μV/°C, guaranteed over the full military temperature range. Open-loop gain of the OP-470 is over 1,000,000 into a 10kΩ load insuring excellent gain accuracy and linearity, even in high-gain applications. Input bias current is under 25nA which reduces errors due to signal source resistance. The OP-470's CMR of over 110dB and PSRR of less than 1.8μV/V significantly reduce errors due to ground noise and power supply fluctuations. Power consumption of the quad OP-470 is half that of four OP-27s, a significant advantage for power con-

PIN CONNECTIONS

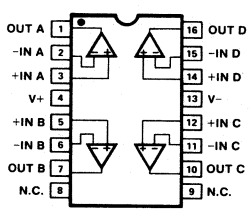


14-PIN HERMETIC DIP (Y-Suffix)

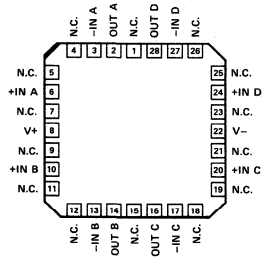
14-PIN PLASTIC MINI-DIP (P-Suffix)



20-LEAD LCC (RC-Suffix)

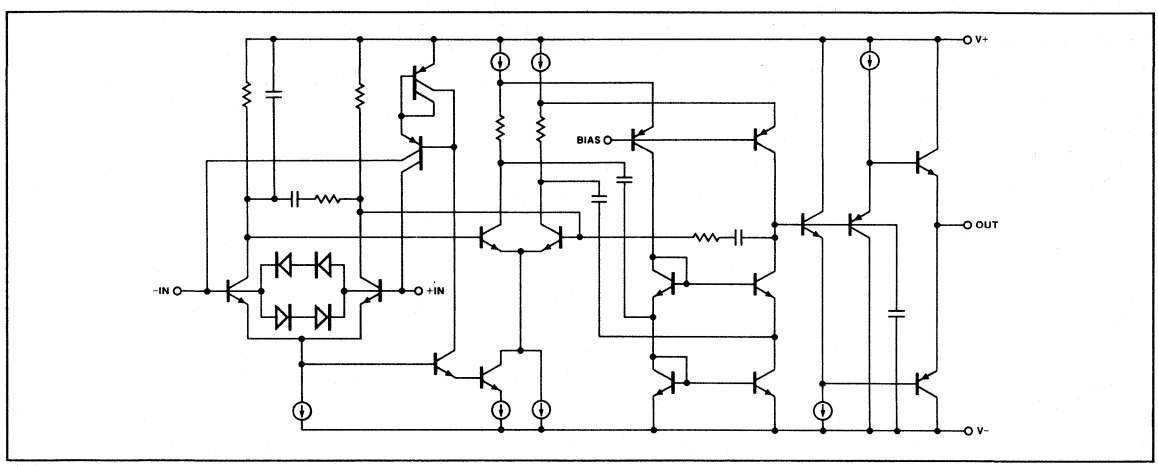


16-PIN SOL (S-Suffix)



28-LEAD LCC (TC-Suffix)

SIMPLIFIED SCHEMATIC



scious applications. The OP-470 is unity-gain stable with a gain-bandwidth product of 6MHz and a slew rate of 2V/μs.

The OP-470 offers excellent amplifier matching which is important for applications such as multiple gain blocks, low-noise instrumentation amplifiers, quad buffers, and low-noise active filters.

The OP-470 conforms to the industry standard 14-pin DIP pinout. It is pin compatible with the OP-11, LM148/149, HA4741, HA5104, and RM4156 quad op amps and can be used to upgrade systems using these devices.

For higher speed applications the OP-471, with a slew rate of 8V/μs, is recommended.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Differential Input Voltage (Note 2) ..... ±1.0V
Differential Input Current (Note 2) ..... ±25mA
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous
Storage Temperature Range
P, TC, Y-Package ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature (T_J) ..... –65°C to +150°C
Operating Temperature Range
OP-470A ..... –55°C to +125°C
OP-470E, OP-470F ..... –25°C to +85°C
OP-470G ..... –40°C to +85°C

PACKAGE TYPE	Θ_{JA} (Note 3)	Θ_{JC}	UNITS
14-Pin Hermetic DIP (Y)	94	10	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
20-Contact LCC (RC)	78	30	°C/W
28-Contact LCC (TC)	70	28	°C/W
16-Pin SOL (S)	88	23	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. The OP-470's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise performance. If differential voltage exceeds ±1.0V, the input current should be limited to ±25mA.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO and PLCC packages.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted.

			OP-470A/E			OP-470F			OP-470G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.1	0.4	—	0.2	0.8	—	0.4	1.0	mV
Input Offset Current	I_{OS}	V_{CM} = 0V	—	3	10	—	6	20	—	12	30	nA
Input Bias Current	I_B	V_{CM} = 0V	—	6	25	—	15	50	—	25	60	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 1)	—	80	200	—	80	200	—	80	200	nV_{p-p}
Input Noise Voltage Density	e_n	f_O = 10Hz	—	3.8	6.5	—	3.8	6.5	—	3.8	6.5	$nV/\sqrt{Hz}$
		f_O = 100Hz	—	3.3	5.5	—	3.3	5.5	—	3.3	5.5	
		f_O = 1kHz (Note 2)	—	3.2	5.0	—	3.2	5.0	—	3.2	5.0	
Input Noise Current Density	i_n	f_O = 10Hz	—	1.7	—	—	1.7	—	—	1.7	—	$pA/\sqrt{Hz}$
		f_O = 100Hz	—	0.7	—	—	0.7	—	—	0.7	—	
		f_O = 1kHz	—	0.4	—	—	0.4	—	—	0.4	—	
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V										
		R_L = 10kΩ	1000	2300	—	800	1700	—	800	1700	—	V/mV
		R_L = 2kΩ	500	1200	—	400	900	—	400	900	—	
Input Voltage Range	IVR	(Note 3)	±11	±12	—	±11	±12	—	±11	±12	—	V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	—	±12	±13	—	±12	±13	—	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	110	125	—	100	120	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	—	0.56	1.8	—	1.0	5.6	—	1.0	5.6	μV/V
Slew Rate	SR		1.4	2	—	1.4	2	—	1.4	2	—	V/μs

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-470A/E MIN	OP-470A/E TYP	OP-470A/E MAX	OP-470F MIN	OP-470F TYP	OP-470F MAX	OP-470G MIN	OP-470G TYP	OP-470G MAX	UNITS
Supply Current (All Amplifiers)	I_{SY}	No Load	—	9	11	—	9	11	—	9	11	mA
Gain Bandwidth Product	GBW	$A_V = +10$	—	6	—	—	6	—	—	6	—	MHz
Channel Separation	CS	$V_O = 20V_{p-p}$ $f_O = 10Hz$ (Note 1)	125	155	—	125	155	—	125	155	—	dB
Input Capacitance	C_{IN}		—	2	—	—	2	—	—	2	—	pF
Input Resistance Differential-Mode	R_{IN}		—	0.4	—	—	0.4	—	—	0.4	—	MΩ
Input Resistance Common-Mode	R_{INCM}		—	11	—	—	11	—	—	11	—	GΩ
Settling Time	t_s	$A_V = +1$ to 0.1% to 0.01%	— —	5.5 6.0	— —	— —	5.5 6.0	— —	— —	5.5 6.0	— —	μs

NOTES:
1. Guaranteed but not 100% tested.
2. Sample tested.
3. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq 125°C$ for OP-470A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-470A MIN	OP-470A TYP	OP-470A MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.14	0.6	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.4	2	μV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	5	20	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	15	50	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	750 400	1600 800	— —	V/mV
Input Voltage Range	IVR	(Note 1)	±11	±12	—	V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	1.0	5.6	μV/V
Supply Current (All Amplifiers)	I_{SY}	No Load	—	9.2	11	mA

NOTE:
1. Guaranteed by CMR test.

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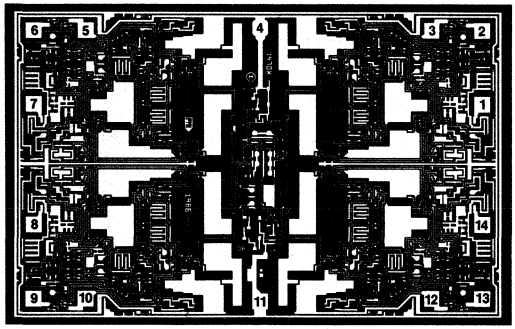
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-25°C \le T_A \le +85°C$ for OP-470E/F, $-40°C \le T_A \le +85°C$ for OP-470G, unless otherwise noted.

			OP-470E			OP-470F			OP-470G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}		—	0.12	0.5	—	0.24	1.0	—	0.5	1.5	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.4	2	—	0.6	4	—	2	—	µV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	4	20	—	7	40	—	20	50	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	11	50	—	20	70	—	40	75	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	 800 400	 1800 900	 — —	 600 300	 1400 700	 — —	 600 300	 1500 800	 — —	V/mV
Input Voltage Range	IVR	(Note 1)	±11	±12	—	±11	±12	—	±11	±12	—	V
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12	±13	—	±12	±13	—	±12	±13	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	100	120	—	90	115	—	90	110	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	0.7	5.6	—	1.8	10	—	1.8	10	µV/V
Supply Current (All Amplifiers)	I_{SY}	No Load	—	9.2	11	—	9.2	11	—	9.3	11	mA

NOTE:
1. Guaranteed by CMR test.

DICE CHARACTERISTICS



DIE SIZE 0.163 × 0.106 inch, 17,278 sq. mils
(4.14 × 2.69 mm, 11.14 sq. mm)

1. OUT A
2. −IN A
3. +IN A
4. V+
5. +IN B
6. −IN B
7. OUT B
8. OUT C
9. −IN C
10. +IN C
11. V−
12. +IN D
13. −IN D
14. OUT D

2

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-470GBC LIMIT	UNITS
Input Offset Voltage	V_{OS}		0.8	mV MAX
Input Offset Current	I_{OS}	$V_{CM} = 0V$	20	nA MAX
Input Bias Current	I_B	$V_{CM} = 0V$	50	nA MAX
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	 800 400	 V/mV MIN
Input Voltage Range	IVR	(Note 1)	±11	V MIN
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	V MIN
Common Mode Rejection	CMR	$V_{CM} = \pm 11V$	100	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	5.6	μV/V MAX
Slew Rate	SR		1.4	V/μs MIN
Supply Current (All Amplifiers)	I_{SY}	No Load	11	mA MAX

NOTE:
1. Guaranteed by CMR test.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

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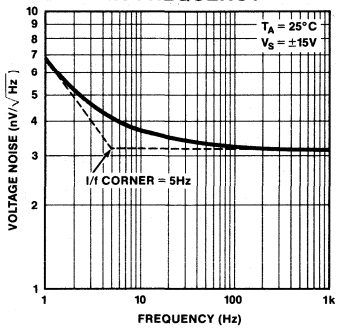
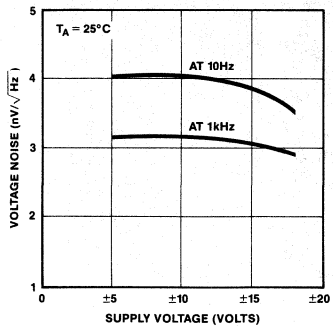
TYPICAL PERFORMANCE CHARACTERISTICS

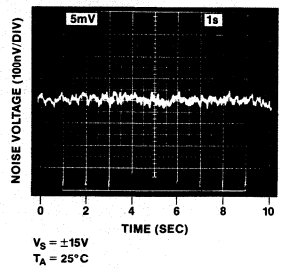
VOLTAGE NOISE DENSITY vs FREQUENCY



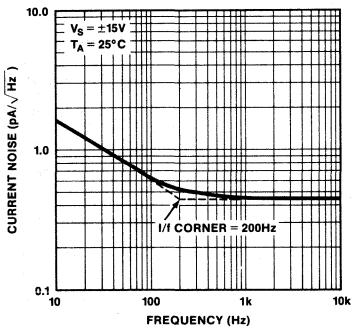
VOLTAGE NOISE DENSITY vs SUPPLY VOLTAGE



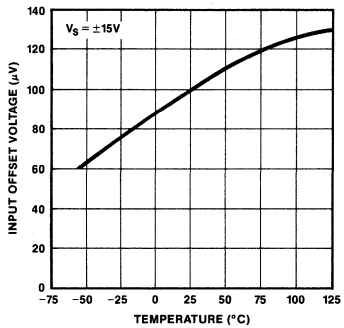
0.1Hz TO 10Hz NOISE



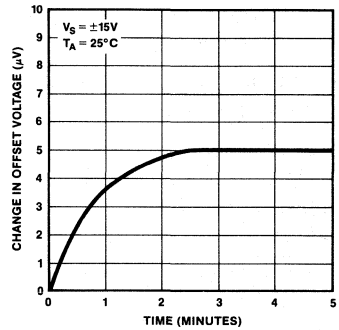
CURRENT NOISE DENSITY vs FREQUENCY



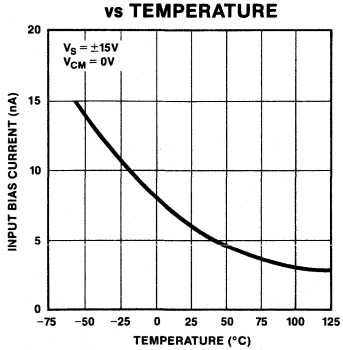
INPUT OFFSET VOLTAGE vs TEMPERATURE



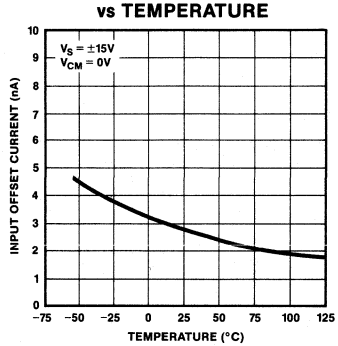
WARM-UP OFFSET VOLTAGE DRIFT



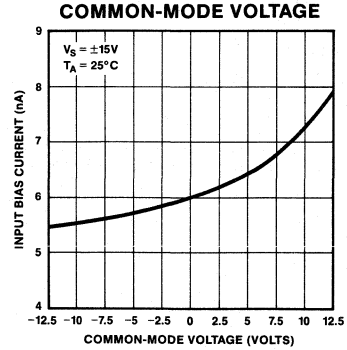
INPUT BIAS CURRENT vs TEMPERATURE



INPUT OFFSET CURRENT vs TEMPERATURE

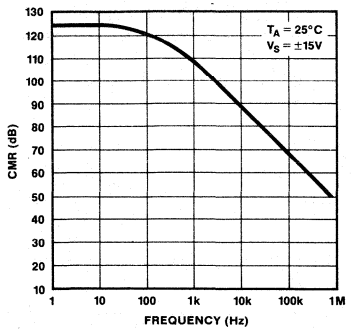


INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

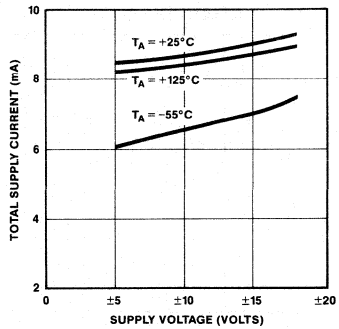


TYPICAL PERFORMANCE CHARACTERISTICS

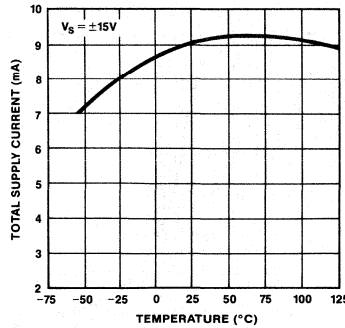
CMR vs FREQUENCY



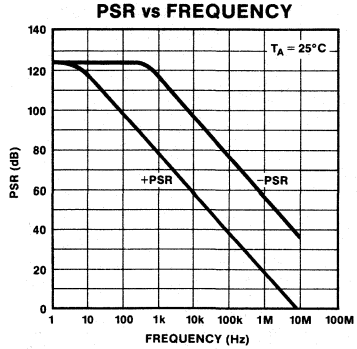
TOTAL SUPPLY CURRENT vs SUPPLY VOLTAGE



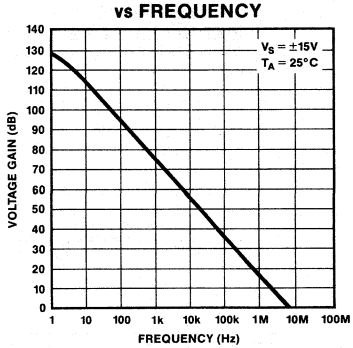
TOTAL SUPPLY CURRENT vs TEMPERATURE



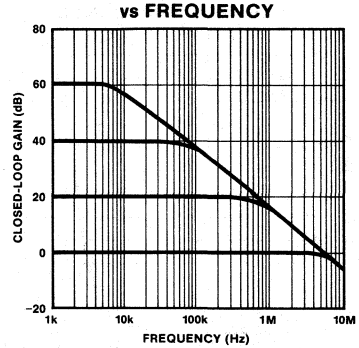
PSR vs FREQUENCY



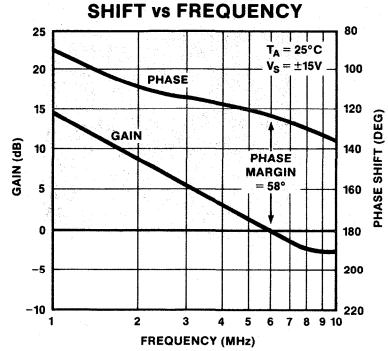
OPEN-LOOP GAIN vs FREQUENCY



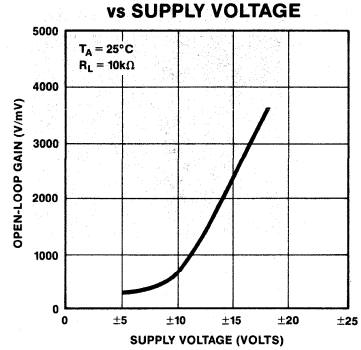
CLOSED-LOOP GAIN vs FREQUENCY



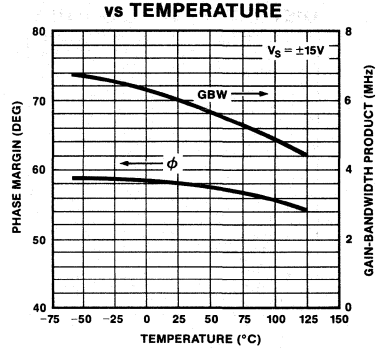
OPEN-LOOP GAIN, PHASE SHIFT vs FREQUENCY



OPEN-LOOP GAIN vs SUPPLY VOLTAGE



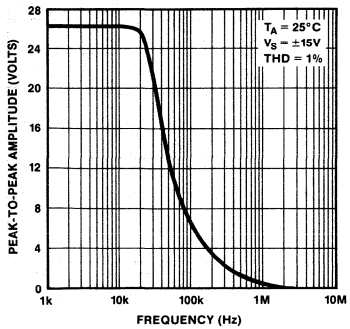
GAIN-BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE



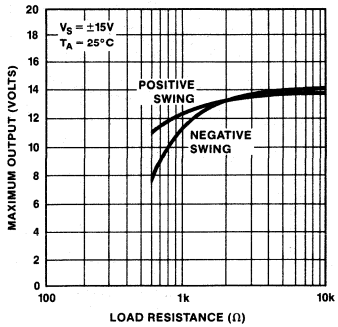
OP-470

TYPICAL PERFORMANCE CHARACTERISTICS

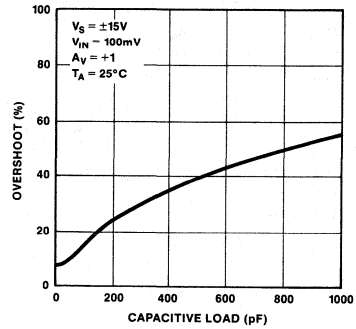
MAXIMUM OUTPUT SWING vs FREQUENCY



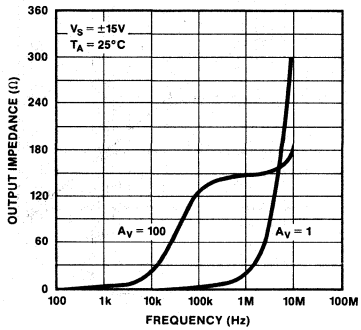
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



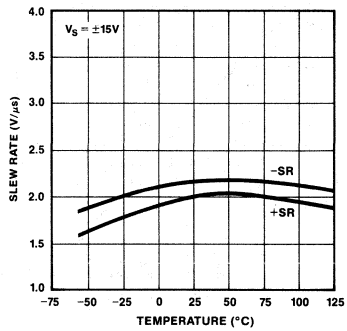
SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD



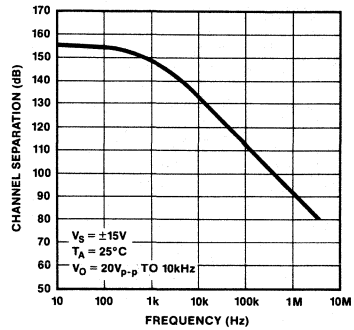
OUTPUT IMPEDANCE vs FREQUENCY



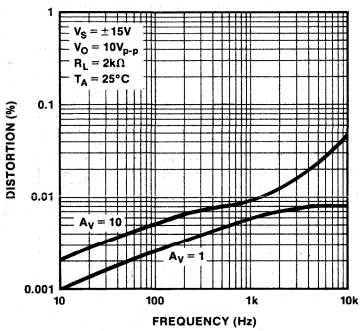
SLEW RATE vs TEMPERATURE



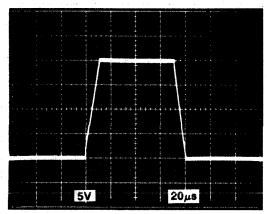
CHANNEL SEPARATION vs FREQUENCY



TOTAL HARMONIC DISTORTION vs FREQUENCY

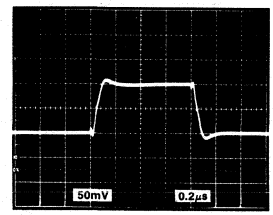


LARGE-SIGNAL TRANSIENT RESPONSE



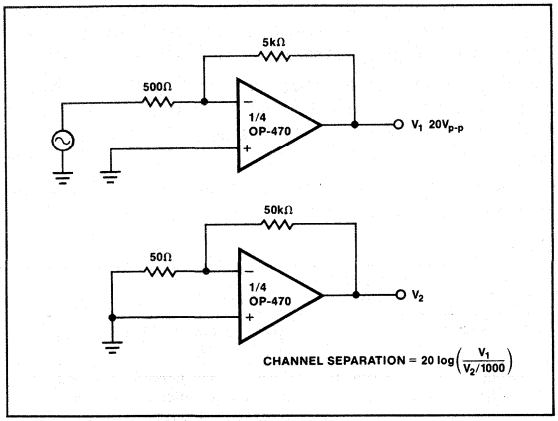
T_A = 25°C
V_S = ±15V
A_V = +1

SMALL-SIGNAL TRANSIENT RESPONSE

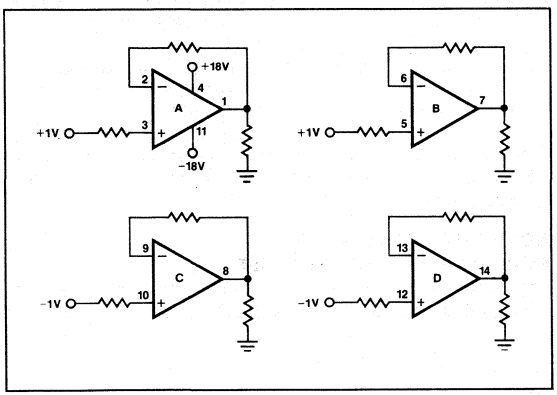


T_A = 25°C
V_S = ±15V
A_V = +1

CHANNEL SEPARATION TEST CIRCUIT



BURN-IN CIRCUIT



APPLICATIONS INFORMATION

VOLTAGE AND CURRENT NOISE

The OP-470 is a very low-noise quad op amp, exhibiting a typical voltage noise of only 3.2nV/$\sqrt{Hz}$ @ 1kHz. The exceptionally low noise characteristics of the OP-470 is in part achieved by operating the input transistors at high collector currents since the voltage noise is inversely proportional to the square root of the collector current. Current noise, however, is directly proportional to the square root of the collector current. As a result, the outstanding voltage noise performance of the OP-470 is gained at the expense of current noise performance, which is typical for low noise amplifiers.

To obtain the best noise performance in a circuit it is vital to understand the relationship between voltage noise (e_n), current noise (i_n), and resistor noise (e_t).

TOTAL NOISE AND SOURCE RESISTANCE

The total noise of an op amp can be calulated by:

$$E_n = \sqrt{(e_n)^2 + (i_n R_S)^2 + (e_t)^2}$$

where:

E_n = total input referred noise

e_n = op amp voltage noise

i_n = op amp current noise

e_t = source resistance thermal noise

R_S = source resistance

The total noise is referred to the input and at the output would be amplified by the circuit gain.

Figure 1 shows the relationship between total noise at 1kHz and source resistance. For $R_S < 1k\Omega$ the total noise is dominated by the voltage noise of the OP-470. As R_S rises above

FIGURE 1: Total Noise vs Source Resistance (Including Resistor Noise) at 1kHz

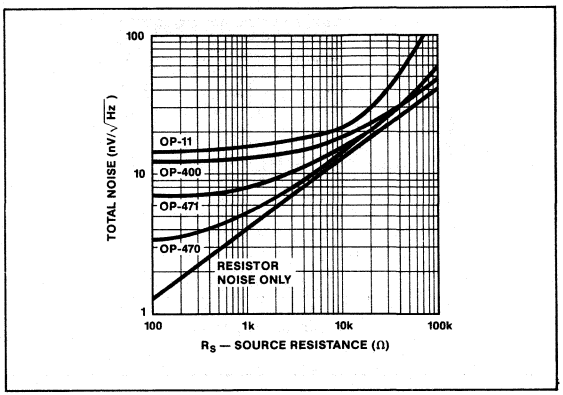
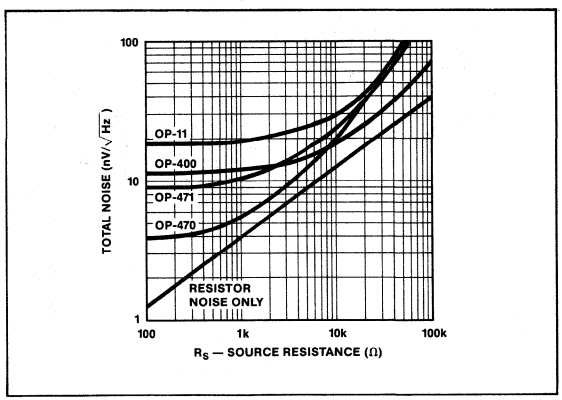


FIGURE 2: Total Noise vs Source Resistance (Including Resistor Noise) at 10Hz



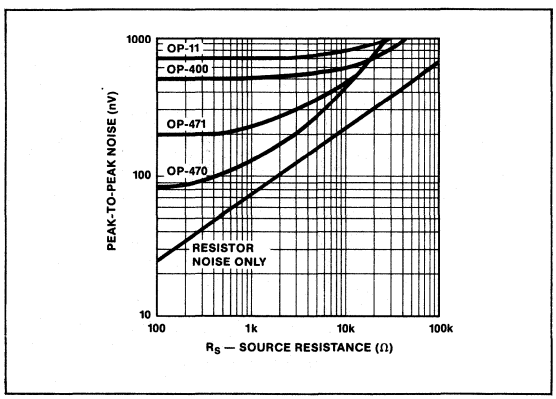
1kΩ, total noise increases and is dominated by resistor noise rather than by voltage or current noise of the OP-470. When R_S exceeds 20kΩ, current noise of the OP-470 becomes the major contributor to total noise.

Figure 2 also shows the relationship between total noise and source resistance, but at 10Hz. Total noise increases more quickly than shown in Figure 1 because current noise is inversely proportional to the square root of frequency. In Figure 2, current noise of the OP-470 dominates the total noise when $R_S > 5k\Omega$.

From Figures 1 and 2 it can be seen that to reduce total noise, source resistance must be kept to a minimum. In applications with a high source resistance, the OP-400, with lower current noise than the OP-470, will provide lower total noise.

Figure 3 shows peak-to-peak noise versus source resistance over the 0.1Hz to 10Hz range. Once again, at low values of R_S, the voltage noise of the OP-470 is the major contributor to peak-to-peak noise with current noise the major contributor as R_S increases. The crossover point between the OP-470 and the OP-400 for peak-to-peak noise is at $R_S = 17k\Omega$.

FIGURE 3: Peak-To-Peak Noise (0.1Hz To 10Hz) vs Source Resistance (Includes Resistor Noise)



The OP-471 is a higher speed version of the OP-470, with a slew rate of 8V/μs. Noise of the OP-471 is only slightly higher than the OP-470. Like the OP-470, the OP-471 is unity-gain stable.

For reference, typical source resistances of some signal sources are listed in Table I.

TABLE I

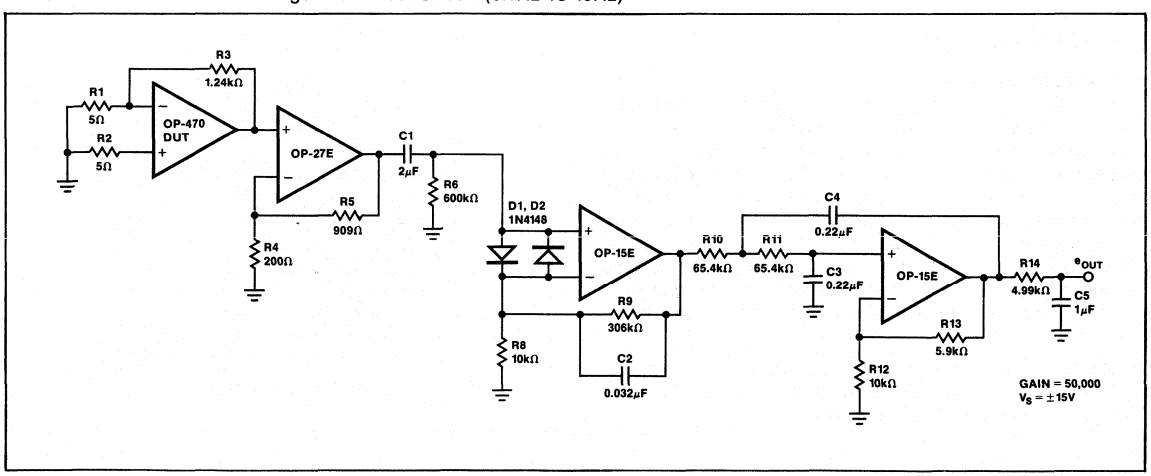
DEVICE	SOURCE IMPEDANCE	COMMENTS
Strain gauge	<500Ω	Typically used in low-frequency applications.
Magnetic tapehead	<1500Ω	Low I_B very important to reduce self-magnetization problems when direct coupling is used. OP-470 I_B can be neglected.
Magnetic phonograph cartridges	<1500Ω	Similar need for low I_B in direct coupled applications. OP-470 will not introduce any self-magnetization problem.
Linear variable differential transformer	<1500Ω	Used in rugged servo-feedback applications. Bandwidth of interest is 400Hz to 5kHz.

For further information regarding noise calculations, see "Minimization of Noise in Op-Amp Applications," Application Note AN-15.

NOISE MEASUREMENTS — PEAK-TO-PEAK VOLTAGE NOISE

The circuit of Figure 4 is a test setup for measuring peak-to-peak voltage noise. To measure the 200nV peak-to-peak

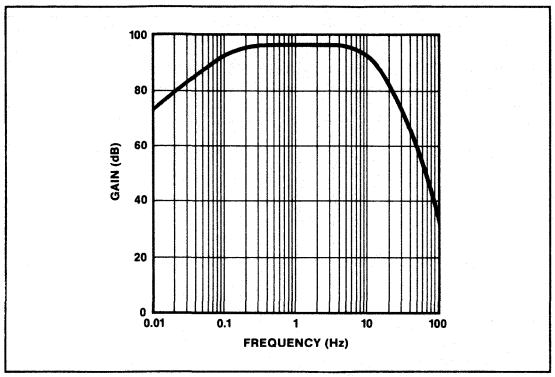
FIGURE 4: Peak-To-Peak Voltage Noise Test Circuit (0.1Hz To 10Hz)



noise specification of the OP-470 in the 0.1Hz to 10Hz range, the following precautions must be observed:

1. The device has to be warmed-up for at least five minutes. As shown in the warm-up drift curve, the offset voltage typically changes 5μV due to increasing chip temperature after power-up. In the 10-second measurement interval, these temperature-induced effects can exceed tens-of-nanovolts.
2. For similar reasons, the device has to be well-shielded from air currents. Shielding also minimizes thermocouple effects.
3. Sudden motion in the vicinity of the device can also "feed-through" to increase the observed noise.
4. The test time to measure 0.1Hz-to-10Hz noise should not exceed 10 seconds. As shown in the noise-tester frequency-response curve of Figure 5, the 0.1Hz corner is defined by only one pole. The test time of 10 seconds acts as an additional pole to eliminate noise contribution from the frequency band below 0.1Hz.
5. A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage-density measurement will correlate well with a 0.1Hz-to-10Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the 1/f corner frequency.
6. Power should be supplied to the test circuit by well bypassed low-noise supplies, e.g. batteries. These will minimize output noise introduced via the amplifier supply pins.

FIGURE 5: 0.1Hz To 10Hz Peak-To-Peak Voltage Noise Test Circuit Frequency Response



NOISE MEASUREMENT — NOISE VOLTAGE DENSITY

The circuit of Figure 6 shows a quick and reliable method of measuring the noise voltage density of quad op amps. Each individual amplifier is series-connected and is in unity-gain, save the final amplifier which is in a noninverting gain of 101. Since the ac noise voltages of each amplifier are uncorrelated, they add in rms fashion to yield:

$$e_{OUT} = 101\left(\sqrt{e_{nA}^2 + e_{nB}^2 + e_{nC}^2 + e_{nD}^2}\right)$$

The OP-470 is a monolithic device with four identical amplifiers. The noise voltage density of each individual amplifier will match, giving:

$$e_{OUT} = 101\left(\sqrt{4e_n^2}\right) = 101\ (2e_n)$$

FIGURE 6: Noise Voltage Density Test Circuit

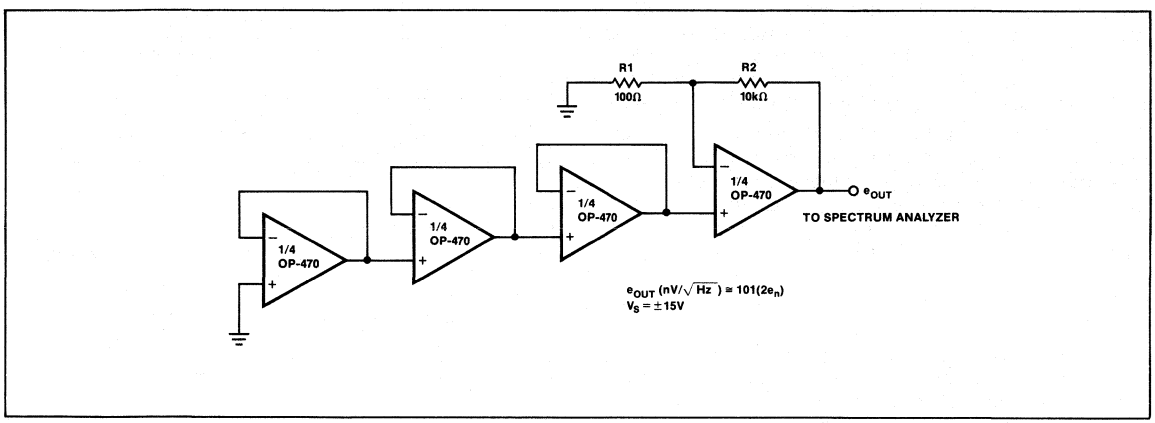
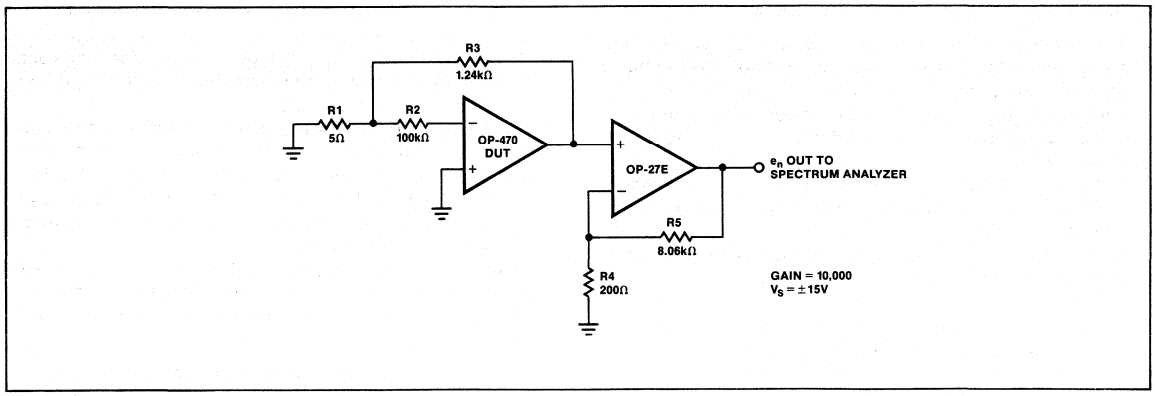


FIGURE 7: Current Noise Density Test Circuit



NOISE MEASUREMENT — CURRENT NOISE DENSITY

The test circuit shown in Figure 7 can be used to measure current noise density. The formula relating the voltage output to current noise density is:

$$i_n = \frac{\sqrt{\left(\frac{e_{nOUT}}{G}\right)^2 - \left(40nV/\sqrt{Hz}\right)^2}}{R_S}$$

where:

G = gain of 10000
R_S = 100kΩ source resistance

CAPACITIVE LOAD DRIVING AND POWER SUPPLY CONSIDERATIONS

The OP-470 is unity-gain stable and is capable of driving large capacitive loads without oscillating. Nonetheless, good supply bypassing is highly recommended. Proper supply bypassing reduces problems caused by supply line noise and improves the capacitive load driving capability of the OP-470.

In the standard feedback amplifier, the op amp's output resistance combines with the load capacitance to form a low-pass filter that adds phase shift in the feedback network and reduces stability. A simple circuit to eliminate this effect is shown in Figure 8. The added components, C1 and R3, decouple the amplifier from the load capacitance and provide additional stability. The values of C1 and R3 shown in Figure 8 are for a load capacitance of up to 1000pF when used with the OP-470.

In applications where the OP-470's inverting or noninverting inputs are driven by a low source impedance (under 100Ω) or connected to ground, if V+ is applied before V−, or when V− is disconnected, excessive parasitic currents will flow. Most

FIGURE 8: Driving Large Capacitive Loads

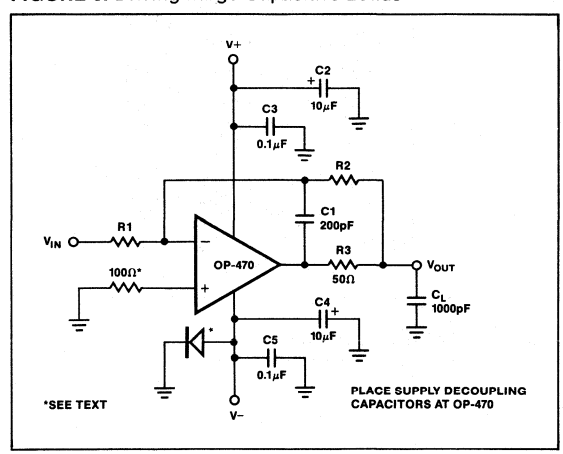
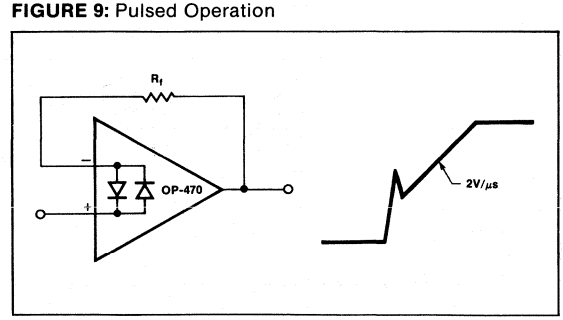


FIGURE 9: Pulsed Operation



applications use dual tracking supplies and with the device supply pins properly bypassed, power-up will not present a problem. A source resistance of at least 100Ω in series with all inputs (Figure 8) will limit the parasitic currents to a safe level if V− is disconnected. It should be noted that any source resistance, even 100Ω, adds noise to the circuit. Where noise is required to be kept at a minimum, a germanium or Schottky diode can be used to clamp the V− pin and eliminate the parasitic current flow instead of using series limiting resistors. For most applications, only one diode clamp is required per board or system.

UNITY-GAIN BUFFER APPLICATIONS

When $R_f \leq 100\Omega$ and the input is driven with a fast, large-signal pulse (>1V), the output waveform will look as shown in Figure 9.

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input, and a current, limited only by the output short-circuit protection, will be drawn by the signal generator. With $R_f \geq 500\Omega$, the output is capable of handling the current requirements ($I_L \leq 20mA$ at 10V); the amplifier will stay in its active mode and a smooth transition will occur.

When $R_f > 3k\Omega$, a pole created by R_f and the amplifier's input capacitance (2pF) creates additional phase shift and reduces phase margin. A small capacitor (20 to 50pF) in parallel with R_f helps eliminate this problem.

APPLICATIONS

LOW NOISE AMPLIFIER

A simple method of reducing amplifier noise by paralleling amplifiers is shown in Figure 10. Amplifier noise, depicted in Figure 11, is around $2nV/\sqrt{Hz}$ @ 1kHz (R.T.I.). Gain for each paralleled amplifier and the entire circuit is 1000. The 200Ω resistors limit circulating currents and provide an effective output resistance of 50Ω. The amplifier is stable with a 10nF capacitive load and can supply up to 30mA of output drive.

DIGITAL PANNING CONTROL

Figure 12 uses a DAC-8408, a quad 8-bit DAC, to pan a signal between two channels. The complementary DAC current outputs of two of the DAC-8408's four DACs drive current-to-voltage converters built from a single quad OP-470. The amplifiers have complementary outputs with the amplitudes dependent upon the digital code applied to the DAC. Figure 13 shows the complementary outputs for a 1kHz input signal and digital ramp applied to the DAC data inputs. Distortion of the digital panning control is less than 0.01%.

Gain error due to the mismatching between the internal DAC ladder resistors and the current-to-voltage feedback resistors is eliminated by using feedback resistors internal to the DAC. Of the four DACs available in the DAC-8408, only two, DACs A and C, actually pass a signal. DACs B and D are used to provide the additional feedback resistors needed in the circuit. If the $V_{REF}B$ and $V_{REF}D$ inputs remain unconnected the currrent-to-voltage converters using $R_{FB}B$ and $R_{FB}D$ are unaffected by digital data reaching DACs B and D.

FIGURE 10: Low Noise Amplifier

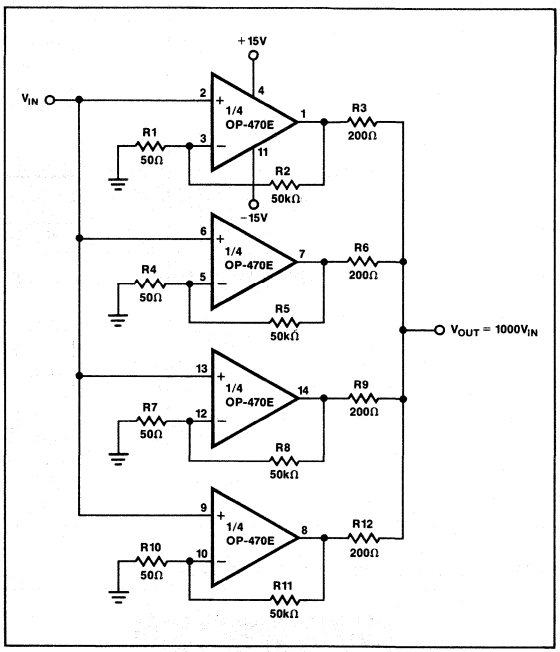


FIGURE 11: Noise Density of Low Noise Amplifier, G = 1000

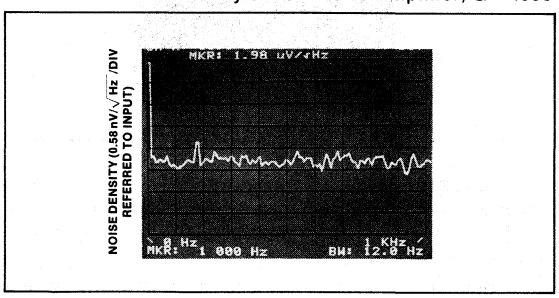


FIGURE 12: Digital Panning Control Circuit

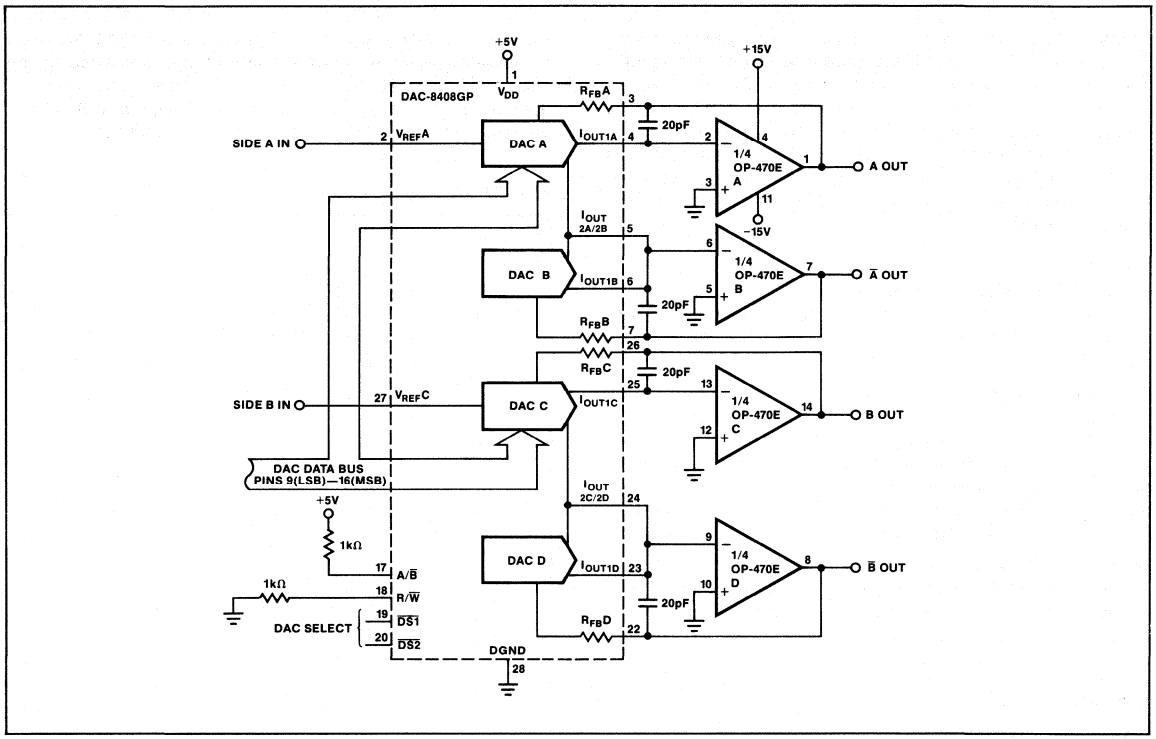


FIGURE 13: Digital Panning Control Output

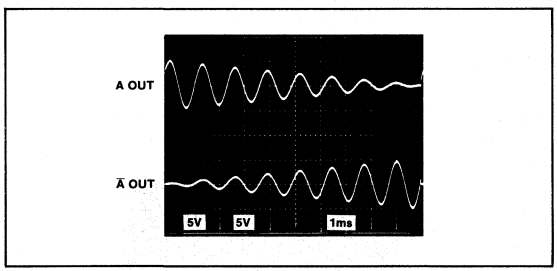
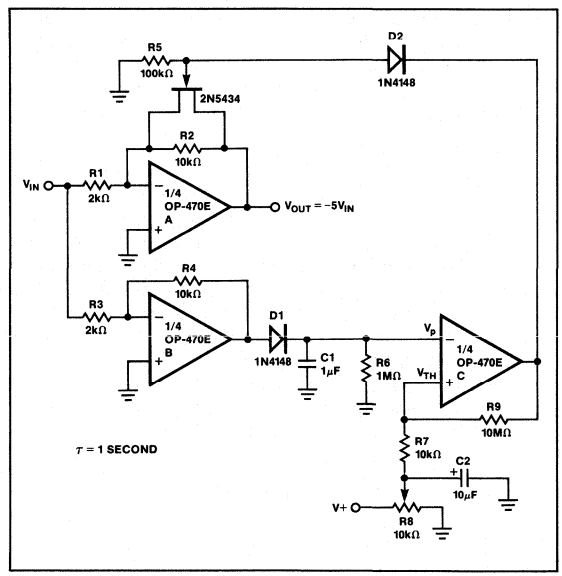


FIGURE 14: Squelch Amplifier



SQUELCH AMPLIFIER

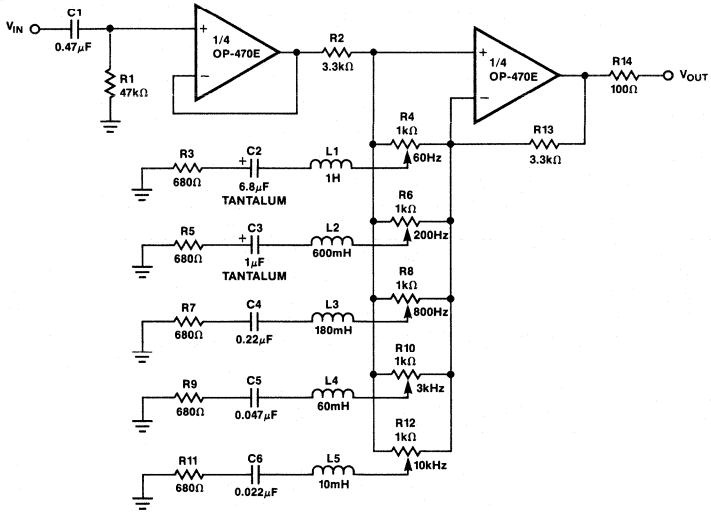
The circuit of Figure 14 is a simple squelch amplifier that uses a FET switch to cut off the output when the input signal falls below a preset limit.

The input signal is sampled by a peak detector with a time constant set by C1 and R6. When the output of the peak detector, V_p, falls below the threshold voltage, V_{TH}, set by R8, the comparator formed by op amp C switches from V– to V+. This drives the gate of the N-channel FET high, turning it ON, reducing the gain of the inverting amplifier formed by op amp A to zero.

FIVE-BAND LOW NOISE STEREO GRAPHIC EQUALIZER

The graphic equalizer circuit shown in Figure 15 provides 15dB of boost or cut over a 5-band range. Signal-to-noise ratio over a 20kHz bandwidth is better than 100dB referred to a 3V rms input. Larger inductors can be replaced by active inductors but this reduces the signal-to-noise ratio.

FIGURE 15: 5-Band Low Noise Graphic Equalizer



ANALOG DEVICES

High Speed, Low Noise Quad Operational Amplifier

OP-471

FEATURES

- **Excellent Speed** ..... **8V/μs Typ**
- **Low Noise** ..... **11nV/√Hz @ 1kHz Max**
- **Unity-Gain Stable**
- **High Gain-Bandwidth** ..... **6.5MHz Typ**
- **Low Input Offset Voltage** ..... **0.8mV Max**
- **Low Offset Voltage Drift** ..... **4μV/°C Max**
- **High Gain** ..... **500V/mV Min**
- **Outstanding CMR** ..... **105 dB Min**
- **Industry Standard Quad Pinouts**
- **Avaliable in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (μV)	PACKAGE			OPERATING TEMPERATURE RANGE
	CERDIP	PLASTIC	LCC*	
800	OP471AY*	–	OP471ATC/883	MIL
800	–	–	OP471ARC/883	MIL
800	OP471EY	–	–	IND
1500	OP471FY	–	–	IND
1800	–	OP471GP	–	XIND
1800	–	OP471GS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

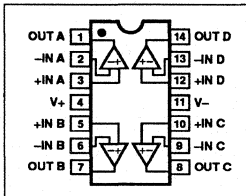
†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

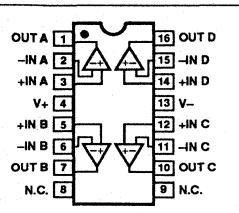
The OP-471 is a monolithic quad op amp featuring low noise, 11nV/√Hz Max @ 1kHz, excellent speed, 8V/μs typical, a gain-bandwidth of 6.5MHz, and unity-gain stability.

The OP-471 has an input offset voltage under 0.8mV and an input offset voltage drift below 4μV/°C, guaranteed over the full military temperature range. Open loop gain of the OP-471 is over 500,000 into a 10kΩ load insuring outstanding gain accuracy and linearity. The input bias current is under 25nA

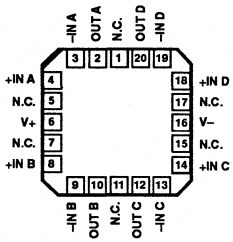
PIN CONNECTIONS



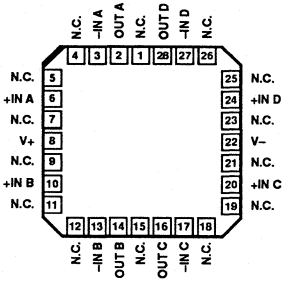
14-PIN HERMETIC DIP (Y-Suffix)
14-PIN PLASTIC DIP (P-Suffix)



16-PIN SOL (S-Suffix)

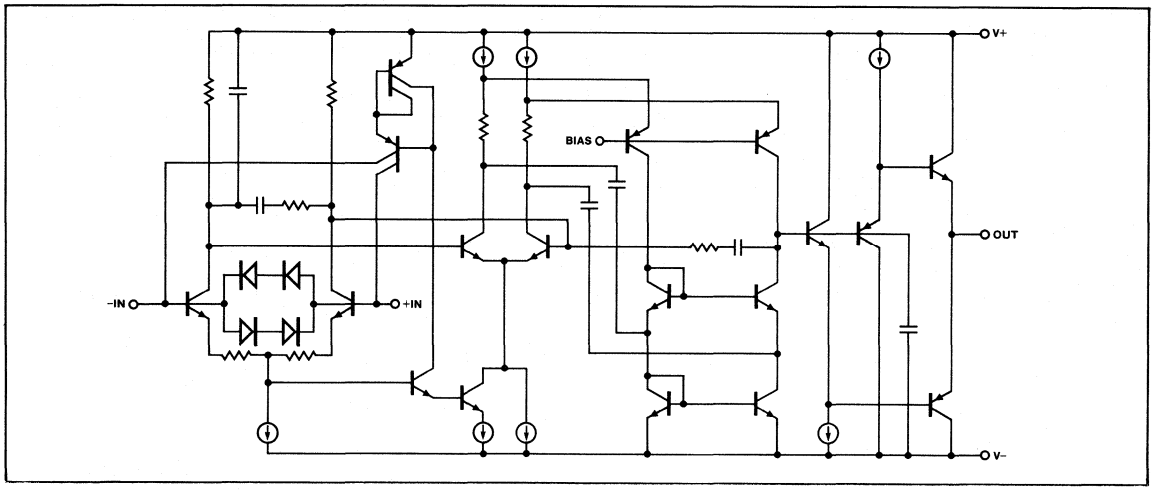


20-LEAD LCC (RC-Suffix)



28-LEAD LCC (TC-Suffix)

SIMPLIFIED SCHEMATIC (One of four amplifiers is shown.)



limiting errors due to signal source resistance. The OP-471's CMR of over 105dB and PSRR of under 5.6μV/V significantly reduce errors caused by ground noise and power supply fluctuations.

The OP-471 offers excellent amplifier matching which is important for applications such as multiple gain blocks, low-noise instrumentation amplifiers, quad buffers and low-noise active filters.

The OP-471 conforms to the industry standard 14-pin DIP pinout. It is pin compatible with the OP-11, LM148/149, HA4741, RM4156, MC33074, TL084 and TL074 quad op amps and can be used to upgrade systems using these devices.

For applications requiring even lower voltage noise the OP-470, with a voltage density of $5nV/\sqrt{Hz}$ Max @ 1kHz, is recommended.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Differential Input Voltage (Note 3) ..... ±1.0V
Differential Input Current (Note 3) ..... ±25mW
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous
Storage Temperature Range
P, RC, TC, Y-Package ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature (T_J) ..... –65°C to +150°C
Operating Temperature Range
OP-471A ..... –55°C to +125°C
OP-471E, OP-471F ..... –25°C to +85°C
OP-471G ..... –40°C to +85°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
14-Pin Hermetic DIP (Y)	94	10	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
20-Contact LCC (RC)	78	30	°C/W
28-Contact LCC (TC)	70	28	°C/W
16-Pin SOL (S)	88	23	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.
3. The OP-471's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise performance. If differential voltage exceeds ±1.0V, the input current should be limited to ±25mA.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $T_A = 25°C$, unless otherwise noted.

			OP-471A/E			OP-471F			OP-471G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.25	0.8	—	0.5	1.5	—	1.0	1.8	mV
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	4	10	—	7	20	—	12	30	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	7	25	—	15	50	—	25	60	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 1)	—	250	500	—	250	500	—	250	500	nV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$	—	9	16	—	9	16	—	9	16	$nV/\sqrt{Hz}$
		$f_O = 100Hz$	—	7	12	—	7	12	—	7	12	
		$f_O = 1kHz$ (Note 2)	—	6.5	11	—	6.5	11	—	6.5	11	
Input Noise Current Density	i_n	$f_O = 10Hz$	—	1.7	—	—	1.7	—	—	1.7	—	$pA/\sqrt{Hz}$
		$f_O = 100Hz$	—	0.7	—	—	0.7	—	—	0.7	—	
		$f_O = 1kHz$	—	0.4	—	—	0.4	—	—	0.4	—	
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm10V$										V/mV
		$R_L = 10k\Omega$	500	700	—	300	500	—	300	500	—	
		$R_L = 2k\Omega$	350	550	—	175	275	—	175	275	—	
Input Voltage Range	IVR	(Note 3)	±11	±12	—	±11	±12	—	±11	±12	—	V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	—	±12	±13	—	±12	±13	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm11V$	105	120	—	95	115	—	95	115	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm4.5V$ to ±18V	—	1	5.6	—	5.6	17.8	—	5.6	17.8	μV/V
Slew Rate	SR		6.5	8	—	6.5	8	—	6.5	8	—	V/μs

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-471A/E MIN	OP-471A/E TYP	OP-471A/E MAX	OP-471F MIN	OP-471F TYP	OP-471F MAX	OP-471G MIN	OP-471G TYP	OP-471G MAX	UNITS
Supply Current (All Amplifiers)	I_{SY}	No Load	—	9.2	11	—	9.2	11	—	9.2	11	mA
Gain-Bandwidth Product	GBW	$A_V = +10$	—	6.5	—	—	6.5	—	—	6.5	—	MHz
Channel Separation	CS	$V_O = 20V_{p-p}$ $f_O = 10Hz$ (Note 1)	125	150	—	125	150	—	125	150	—	dB
Input Capacitance	C_{IN}		—	2.6	—	—	2.6	—	—	2.6	—	pF
Input Resistance Differential-Mode	R_{IN}		—	1.1	—	—	1.1	—	—	1.1	—	MΩ
Input Resistance Common-Mode	R_{INCM}		—	11	—	—	11	—	—	11	—	GΩ
Settling Time	t_s	$A_V = +1$ to 0.1% to 0.01%	— —	4.5 7.5	— —	— —	4.5 7.5	— —	— —	4.5 7.5	— —	μs

NOTES:
1. Guaranteed but not 100% tested.
2. Sample tested.
3. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq 125°C$ for OP-471A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-471A MIN	OP-471A TYP	OP-471A MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.4	1.2	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	1	4	μV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	6	20	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	16	50	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	 375 250	 500 350	 — —	V/mV
Input Voltage Range	IVR	(Note 1)	±11	±12	—	V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	100	115	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	5.6	10	μV/V
Supply Current (All Amplifiers)	I_{SY}	No Load	—	9.3	11	mA

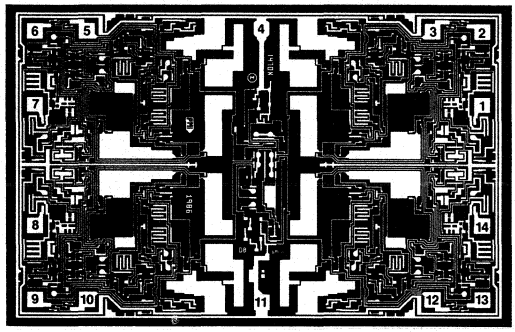
NOTE:
1. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-25°C \leq T_A \leq +85°C$ for OP-471E/F, $-40°C \leq T_A \leq +85°C$ for OP-471G, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-471E MIN	OP-471E TYP	OP-471E MAX	OP-471F MIN	OP-471F TYP	OP-471F MAX	OP-471G MIN	OP-471G TYP	OP-471G MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.3	1.1	—	0.6	2.0	—	1.2	2.5	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	1	4	—	2	7	—	4	—	µV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	5	20	—	8	40	—	20	50	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	13	50	—	25	70	—	40	75	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$										
		$R_L = 10k\Omega$	375	600	—	200	400	—	200	400	—	V/mV
		$R_L = 2k\Omega$	250	400	—	125	200	—	125	200	—	
Input Voltage Range	IVR	(Note 1)	±11	±12	—	±11	±12	—	±11	±12	—	V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	—	±12	±13	—	±12	±13	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	100	115	—	90	110	—	90	110	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	3.2	10	—	18	31.6	—	18	31.6	µV/V
Supply Current (All Amplifiers)	I_{SY}	No Load	—	9.3	11	—	9.3	11	—	9.3	11	mA

NOTE:
1. Guaranteed by CMR test.

DICE CHARACTERISTICS



DIE SIZE 0.163 × 0.106 inch, 17,278 sq. mils
(4.14 × 2.69 mm, 11.14 sq. mm)

1. OUT A
2. −IN A
3. +IN A
4. V+
5. +IN B
6. −IN B
7. OUT B
8. OUT C
9. −IN C
10. +IN C
11. V−
12. +IN D
13. −IN D
14. OUT D

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

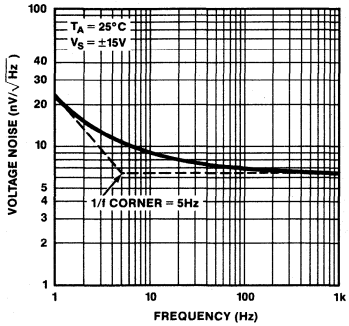
PARAMETER	SYMBOL	CONDITIONS	OP-471GBC LIMIT	UNITS
Input Offset Voltage	V_{OS}		1.5	mV MAX
Input Offset Current	I_{OS}	$V_{CM} = 0V$	20	nA MAX
Input Bias Current	I_B	$V_{CM} = 0V$	50	nA MAX
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	 300 175	V/mV MIN
Input Voltage Range	IVR	Note 1	±11	V MIN
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	95	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	17.8	μV/V MAX
Slew Rate	SR		6.5	V/μs MIN
Supply Current (All Amplifiers)	I_{SY}	No Load	11	mA MAX

NOTES:
1. Guaranteed by CMR test.

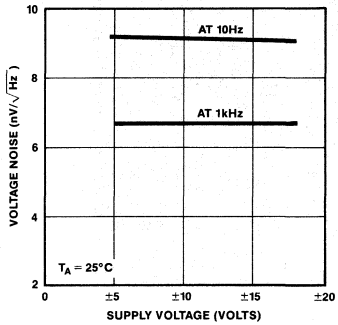
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

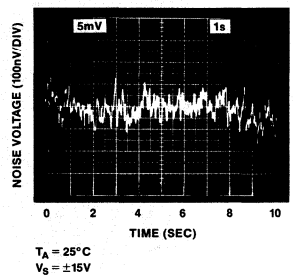
VOLTAGE NOISE DENSITY vs FREQUENCY



VOLTAGE NOISE DENSITY vs SUPPLY VOLTAGE

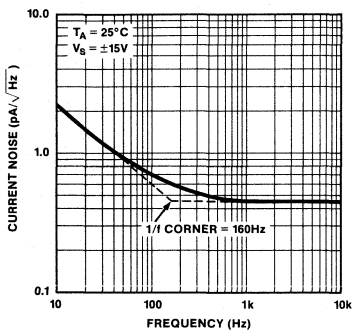


0.1Hz TO 10Hz NOISE

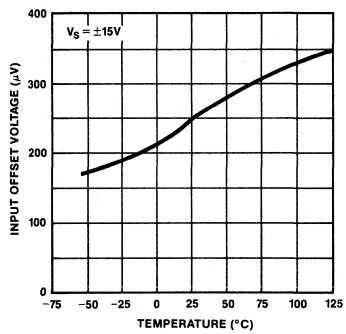


T_A = 25°C
V_S = ±15V

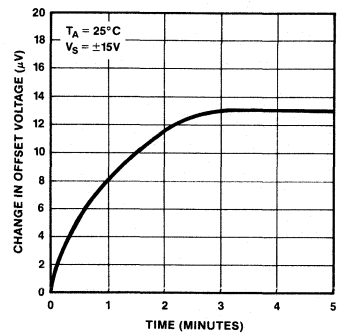
CURRENT NOISE DENSITY vs FREQUENCY



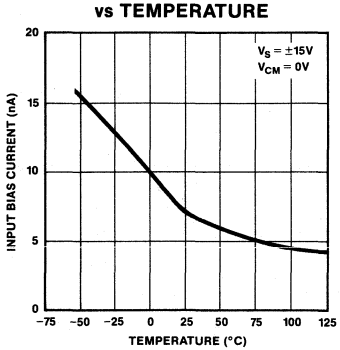
INPUT OFFSET VOLTAGE vs TEMPERATURE



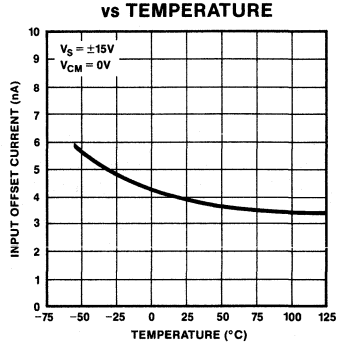
WARM-UP OFFSET VOLTAGE DRIFT



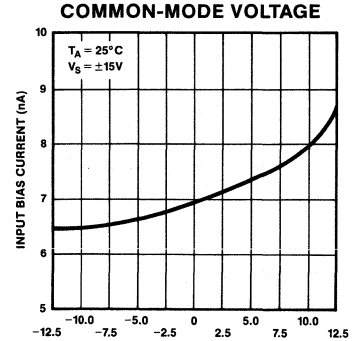
INPUT BIAS CURRENT vs TEMPERATURE



INPUT OFFSET CURRENT vs TEMPERATURE

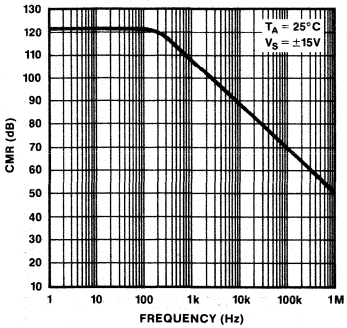


INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

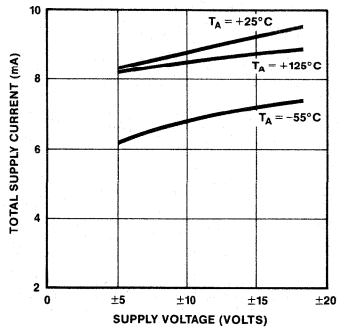


TYPICAL PERFORMANCE CHARACTERISTICS

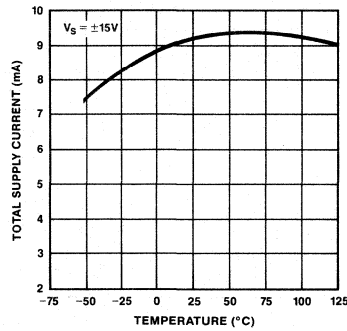
CMR vs FREQUENCY



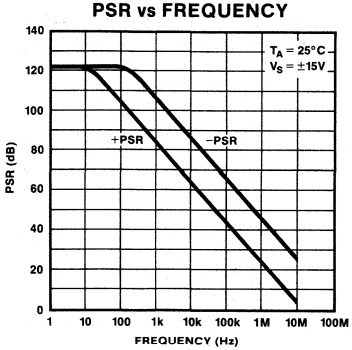
TOTAL SUPPLY CURRENT vs SUPPLY VOLTAGE



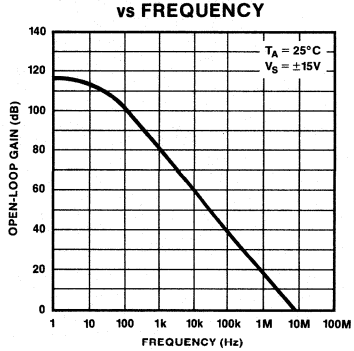
TOTAL SUPPLY CURRENT vs TEMPERATURE



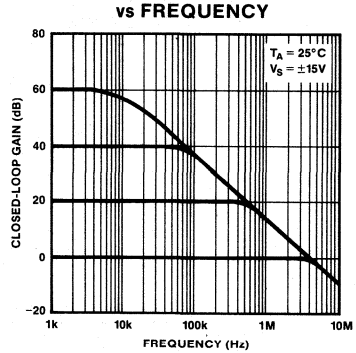
PSR vs FREQUENCY



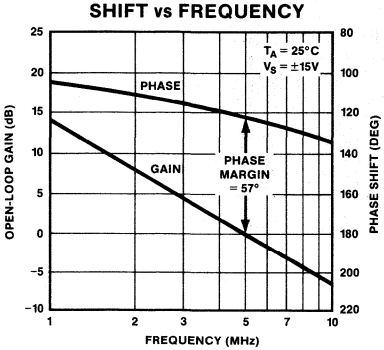
OPEN-LOOP GAIN vs FREQUENCY



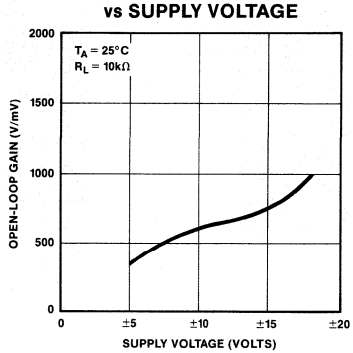
CLOSED-LOOP GAIN vs FREQUENCY



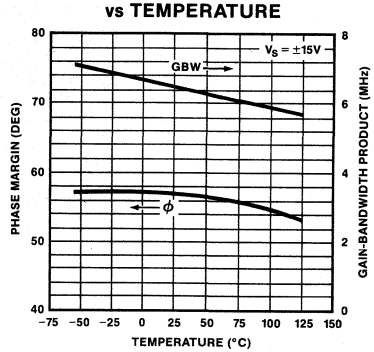
OPEN-LOOP GAIN, PHASE SHIFT vs FREQUENCY



OPEN-LOOP GAIN vs SUPPLY VOLTAGE

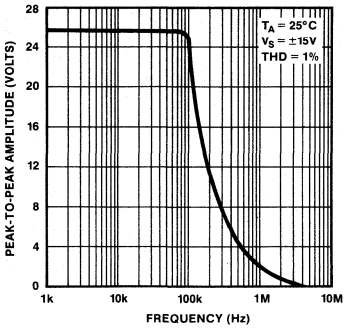


GAIN-BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE

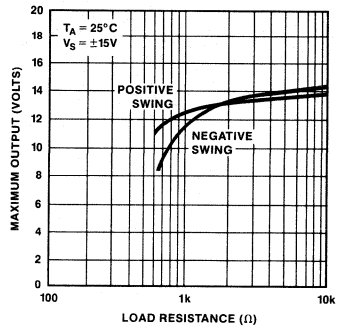


TYPICAL PERFORMANCE CHARACTERISTICS

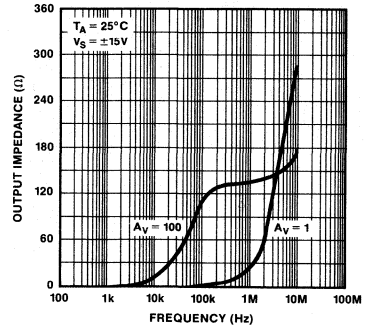
MAXIMUM OUTPUT SWING vs FREQUENCY



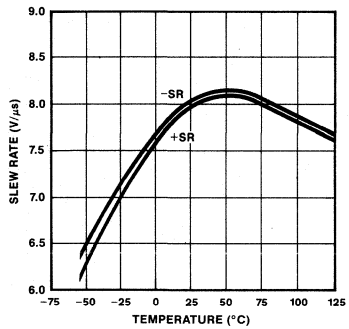
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



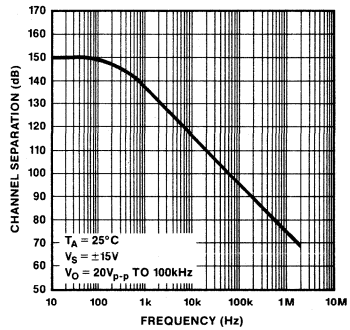
CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



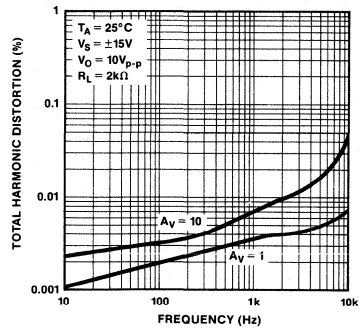
SLEW RATE vs TEMPERATURE



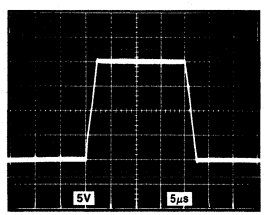
CHANNEL SEPARATION vs FREQUENCY



TOTAL HARMONIC DISTORTION vs FREQUENCY

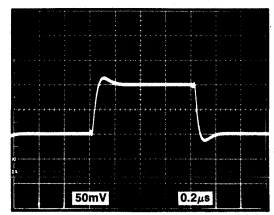


LARGE-SIGNAL TRANSIENT RESPONSE



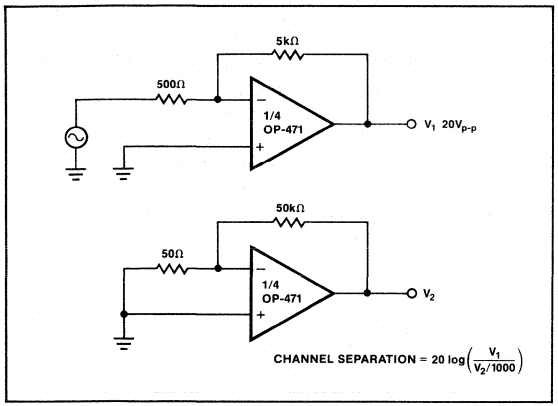
T_A = 25°C
V_S = ±15V
A_V = +1

SMALL-SIGNAL TRANSIENT RESPONSE

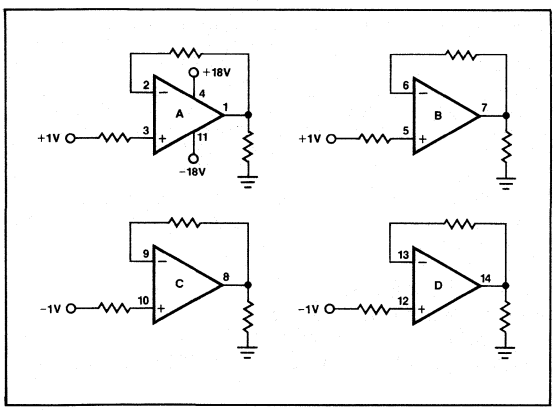


T_A = 25°C
V_S = ±15V
A_V = +1

CHANNEL SEPARATION TEST CIRCUIT



BURN-IN CIRCUIT



APPLICATIONS INFORMATION

VOLTAGE AND CURRENT NOISE

The OP-471 is a very low-noise quad op amp, exhibiting a typical voltage noise of only 6.5nV/$\sqrt{Hz}$ @ 1kHz. The low noise characteristic of the OP-471 is in part achieved by operating the input transistors at high collector currents since the voltage noise is inversely proportional to the square root of the collector current. Current noise, however, is directly proportional to the square root of the collector current. As a result, the outstanding voltage noise performance of the OP-471 is gained at the expense of current noise performance which is typical for low noise amplifiers.

To obtain the best noise performance in a circuit it is vital to understand the relationship between voltage noise (e_n), current noise (i_n), and resistor noise (e_t).

TOTAL NOISE AND SOURCE RESISTANCE

The total noise of an op amp can be calulated by:

$$E_n = \sqrt{(e_n)^2 + (i_n R_S)^2 + (e_t)^2}$$

where:

E_n = total input referred noise

e_n = op amp voltage noise

i_n = op amp current noise

e_t = source resistance thermal noise

R_S = source resistance

The total noise is referred to the input and at the output would be amplified by the circuit gain.

Figure 1 shows the relationship between total noise at 1kHz and source resistance. For $R_S < 1k\Omega$ the total noise is domi-

FIGURE 1: Total Noise vs Source Resistance (Including Resistor Noise) at 1kHz

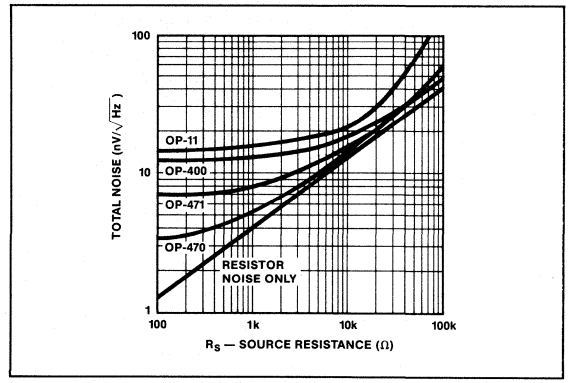
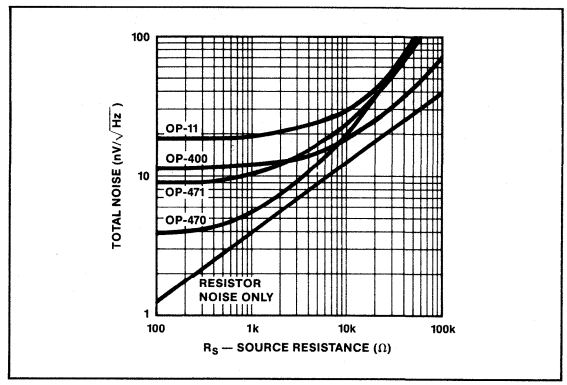


FIGURE 2: Total Noise vs Source Resistance (Including Resistor Noise) at 10Hz



nated by the voltage noise of the OP-471. As R_S rises above 1kΩ, total noise increases and is dominated by resistor noise rather than by voltage or current noise of the OP-471. When R_S exceeds 20kΩ, current noise of the OP-471 becomes the major contributor to total noise.

Figure 2 also shows the relationship between total noise and source resistance, but at 10Hz. Total noise increases more quickly than shown in Figure 1 because current noise is inversely proportional to the square root of frequency. In Figure 2, current noise of the OP-471 dominates the total noise when $R_S > 5k\Omega$.

From Figures 1 and 2 it can be seen that to reduce total noise, source resistance must be kept to a minimum. In applications with a high source resistance, the OP-400, with lower current noise than the OP-471, will provide lower total noise.

Figure 3 shows peak-to-peak noise versus source resistance over the 0.1Hz to 10Hz range. Once again, at low values of R_S, the voltage noise of the OP-471 is the major contributor to peak-to-peak noise. Current noise becomes the major contributor as R_S increases. The crossover point between the OP-471 and the OP-400 for peak-to-peak noise is at $R_S = 17k\Omega$.

The OP-470 is a lower noise version of the OP-471, with a typical noise voltage density of $3.2nV/\sqrt{Hz}$ @ 1kHz. The OP-470 offers lower offset voltage and higher gain than the OP-471, but is a slower speed device, with a slew rate of 2V/μs compared to a slew rate of 8V/μs for the OP-471.

For reference, typical source resistances of some signal sources are listed in Table I.

FIGURE 3: Peak-To-Peak Noise (0.1Hz To 10Hz) vs Source Resistance (Includes Resistor Noise)

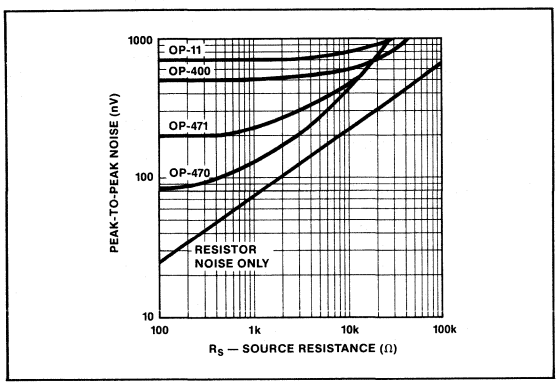


TABLE I

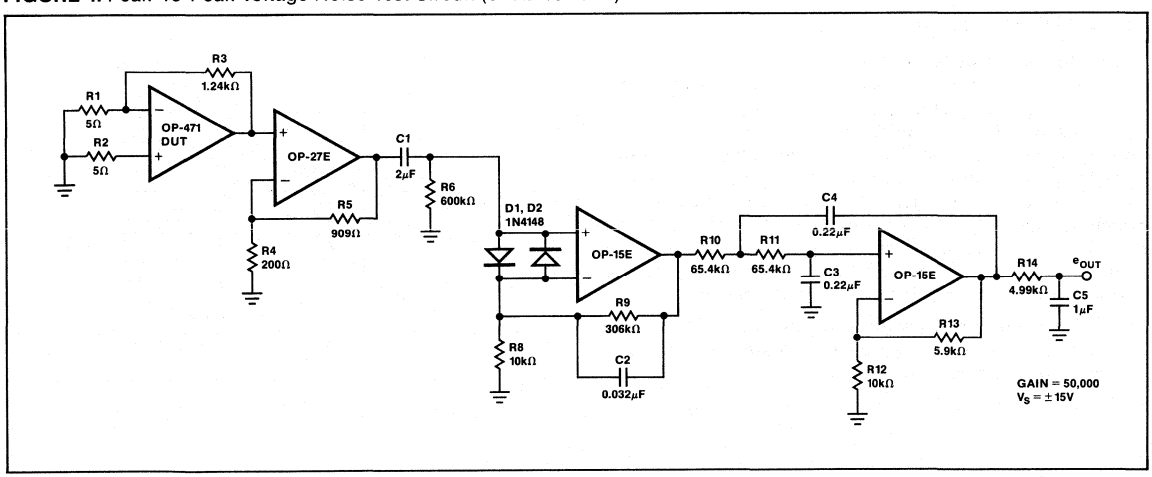
DEVICE	SOURCE IMPEDANCE	COMMENTS
Strain gauge	<500Ω	Typically used in low-frequency applications.
Magnetic tapehead	<1500Ω	Low I_B very important to reduce self-magnetization problems when direct coupling is used. OP-471 I_B can be neglected.
Magnetic phonograph cartridges	<1500Ω	Similar need for low I_B in direct coupled applications. OP-471 will not introduce any self-magnetization problem.
Linear variable differential transformer	<1500Ω	Used in rugged servo-feedback applications. Bandwidth of interest is 400Hz to 5kHz.

For further information regarding noise calculations, see "Minimization of Noise in Op-Amp Applications", Application Note AN-15.

NOISE MEASUREMENTS — PEAK-TO-PEAK VOLTAGE NOISE

The circuit of Figure 4 is a test setup for measuring peak-to-peak voltage noise. To measure the 500nV peak-to-peak

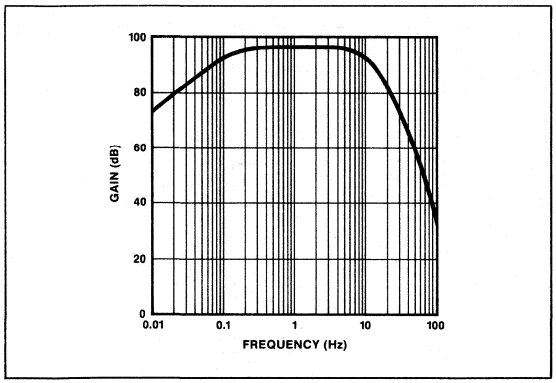
FIGURE 4: Peak-To-Peak Voltage Noise Test Circuit (0.1Hz To 10Hz)



noise specification of the OP-471 in the 0.1Hz to 10Hz range, the following precautions must be observed:

1. The device has to be warmed-up for at least five minutes. As shown in the warm-up drift curve, the offset voltage typically changes 13μV due to increasing chip temperature after power-up. In the 10-second measurement interval, these temperature-induced effects can exceed tens-of-nanovolts.
2. For similar reasons, the device has to be well-shielded from air currents. Shielding also minimizes thermocouple effects.
3. Sudden motion in the vicinity of the device can also "feed-through" to increase the observed noise.
4. The test time to measure 0.1Hz-to-10Hz noise should not exceed 10 seconds. As shown in the noise-tester frequency-response curve of Figure 5, the 0.1Hz corner is defined by only one pole. The test time of 10 seconds acts as an additional pole to eliminate noise contribution from the frequency band below 0.1Hz.
5. A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage-density measurement will correlate well with a 0.1Hz-to-10Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the 1/f corner frequency.
6. Power should be supplied to the test circuit by well bypassed low-noise supplies, e.g. batteries. These will minimize output noise introduced through the amplifier supply pins.

FIGURE 5: 0.1Hz To 10Hz Peak-To-Peak Voltage Noise Test Circuit Frequency Response



NOISE MEASUREMENT — NOISE VOLTAGE DENSITY

The circuit of Figure 6 shows a quick and reliable method of measuring the noise voltage density of quad op amps. Each individual amplifier is series-connected and is in unity-gain, save the final amplifier which is in a noninverting gain of 101. Since the ac noise voltages of each amplifier are uncorrelated, they add in rms fashion to yield:

$$e_{OUT} = 101\ (\sqrt{e_{nA}^2 + e_{nB}^2 + e_{nC}^2 + e_{nD}^2})$$

The OP-471 is a monolithic device with four identical amplifiers. The noise voltage density of each individual amplifier will match, giving:

$$e_{OUT} = 101\ (\sqrt{4e_n^2}) = 101\ (2e_n)$$

FIGURE 6: Noise Voltage Density Test Circuit

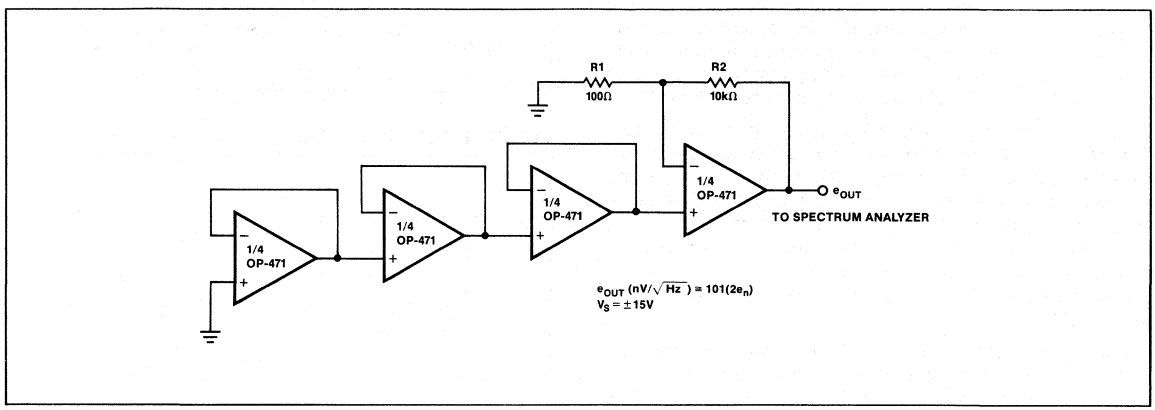
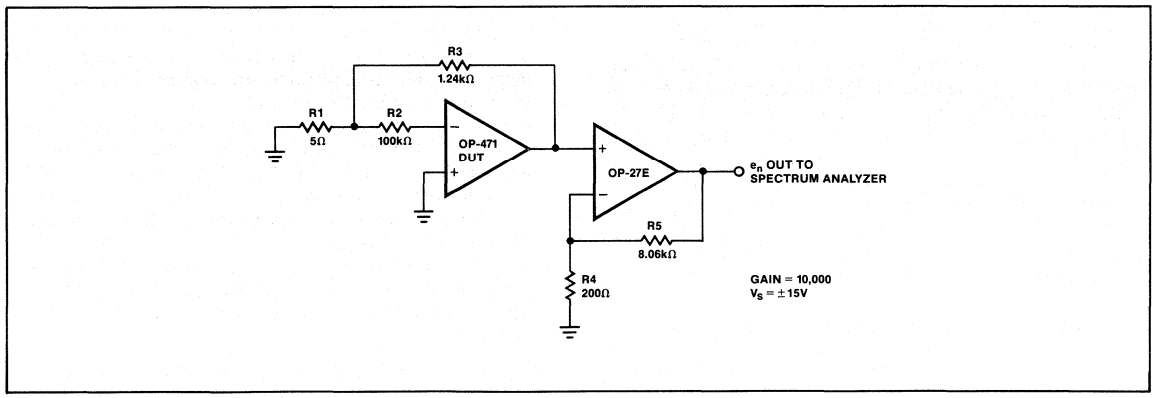


FIGURE 7: Current Noise Density Test Circuit



NOISE MEASUREMENT — CURRENT NOISE DENSITY

The test circuit shown in Figure 7 can be used to measure current noise density. The formula relating the voltage output to current noise density is:

$$i_n = \frac{\sqrt{\left(\frac{e_{nOUT}}{G}\right)^2 - \left(40nV/\sqrt{Hz}\right)^2}}{R_S}$$

where:

G = gain of 10000
R_S = 100kΩ source resistance

CAPACITIVE LOAD DRIVING AND POWER SUPPLY CONSIDERATIONS

The OP-471 is unity-gain stable and is capable of driving large capacitive loads without oscillating. Nonetheless, good supply bypassing is highly recommended. Proper supply bypassing reduces problems caused by supply line noise and improves the capacitive load driving capability of the OP-471.

In the standard feedback amplifier, the op amp's output resistance combines with the load capacitance to form a low-pass filter that adds phase shift in the feedback network and reduces stability. A simple circuit to eliminate this effect is shown in Figure 8. The added components, C1 and R3, decouple the amplifier from the load capacitance and provide additional stability. The values of C1 and R3 shown in Figure 8 are for load capacitances of up to 1000pF when used with the OP-471.

In applications where the OP-471's inverting or noninverting inputs are driven by a low source impedance (under 100Ω) or connected to ground, if V+ is applied before V–, or when V– is disconnected, excessive parasitic currents will flow. Most

FIGURE 8: Driving Large Capacitive Loads

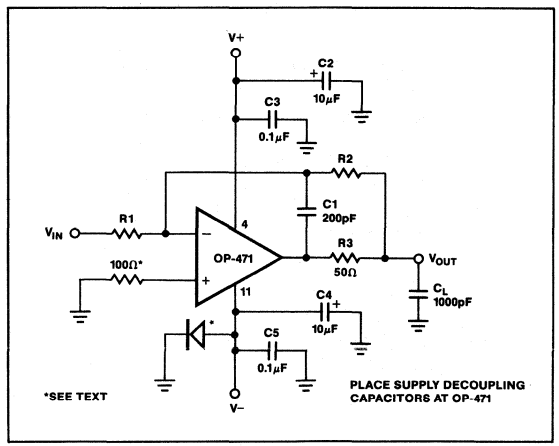
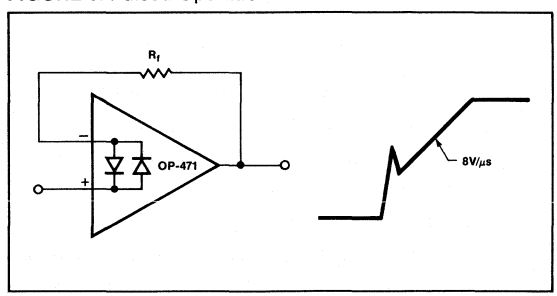


FIGURE 9: Pulsed Operation



applications use dual tracking supplies and with the device supply pins properly bypassed, power-up will not present a problem. A source resistance of at least 100Ω in series with all inputs (Figure 8) will limit the parasitic currents to a safe level if V– is disconnected. It should be noted that any source resistance, even 100Ω, adds noise to the circuit. Where noise is required to be kept at a minimum, a germanium or Schottky diode can be used to clamp the V– pin and eliminate the parasitic current flow instead of using series limiting resistors. For most applications, only one diode clamp is required per board or system.

UNITY-GAIN BUFFER APPLICATIONS

When $R_f \leq 100\Omega$ and the input is driven with a fast, large-signal pulse (>1V), the output waveform will look as shown in Figure 9.

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input, and a current, limited only by the output short-circuit protection, will be drawn by the signal generator. With $R_f \geq 500\Omega$, the output is capable of handling the current requirements ($I_L \leq 20mA$ at 10V); the amplifier will stay in its active mode and a smooth transition will occur.

When $R_f > 3k\Omega$, a pole created by R_f and the amplifier's input capacitance (2.6pF) creates additional phase shift and reduces phase margin. A small capacitor (20 to 50pF) in parallel with R_f helps eliminate this problem.

APPLICATIONS

LOW NOISE AMPLIFIER

A simple method of reducing amplifier noise by paralleling amplifiers is shown in Figure 10. Amplifier noise, depicted in Figure 11, is around $5nV/\sqrt{Hz}$ @ 1kHz (R.T.I.). Gain for each paralleled amplifier and the entire circuit is 100. The 200Ω resistors limit circulating currents and provide an effective output resistance of 50Ω. The amplifier is stable with a 10nF capacitive load and can supply up to 30mA of output drive.

HIGH-SPEED DIFFERENTIAL LINE DRIVER

The circuit of Figure 12 is a unique line driver widely used in professional audio applications. With ±18V supplies the line driver can deliver a differential signal of $30V_{p-p}$ into a 1.5kΩ load. The output of the differential line driver looks exactly like a transformer. Either output can be shorted to ground without changing the circuit gain of 5, so the amplifier can easily be set for inverting, noninverting, or differential operation. The line driver can drive unbalanced loads, like a true transformer.

HIGH OUTPUT AMPLIFIER

The amplifier shown in Figure 13 is capable of driving $20V_{p-p}$ into a floating 400Ω load. Design of the amplifier is based on a bridge configuration. A1 amplifies the input signal and drives the load with the help of A2. Amplifier A3 is a unity-gain inverter which drives the load with help from A4. Gain of the high output amplifier with the component values shown is 10, but can easily be changed by varying R1 or R2.

FIGURE 10: Low Noise Amplifier

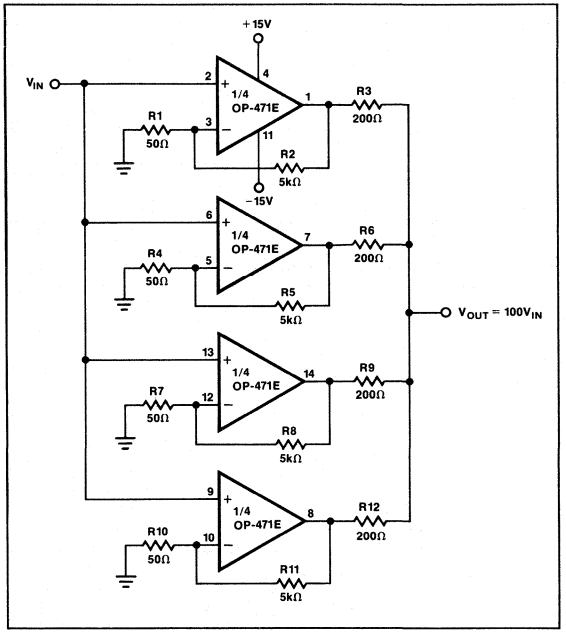


FIGURE 11: Noise Density of Low Noise Amplifier, G = 100

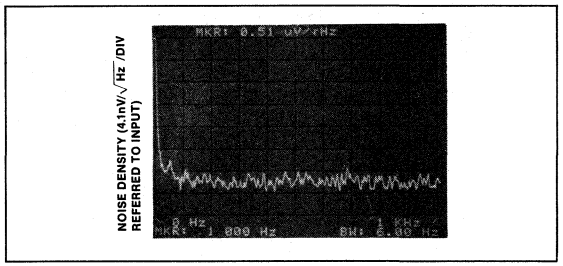


FIGURE 12: High-Speed Differential Line Driver

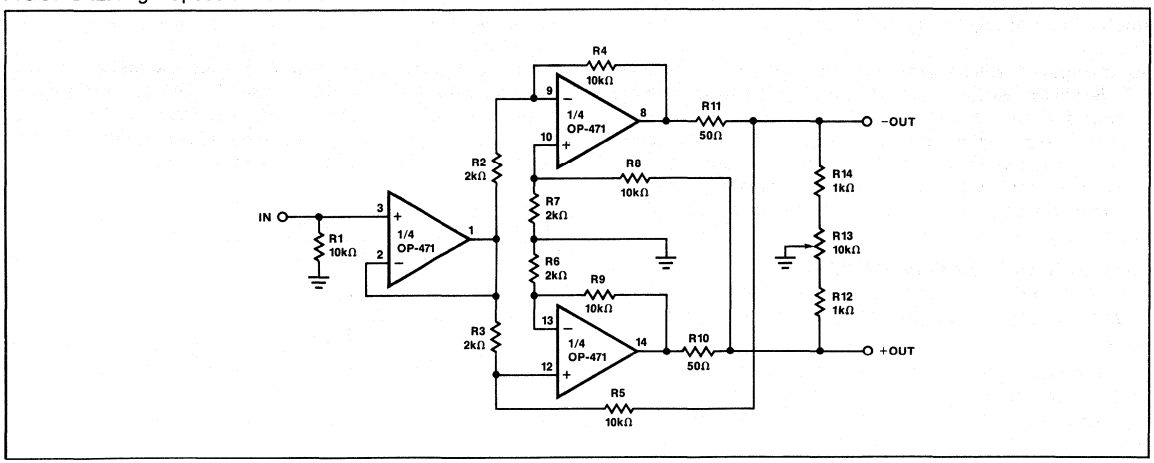
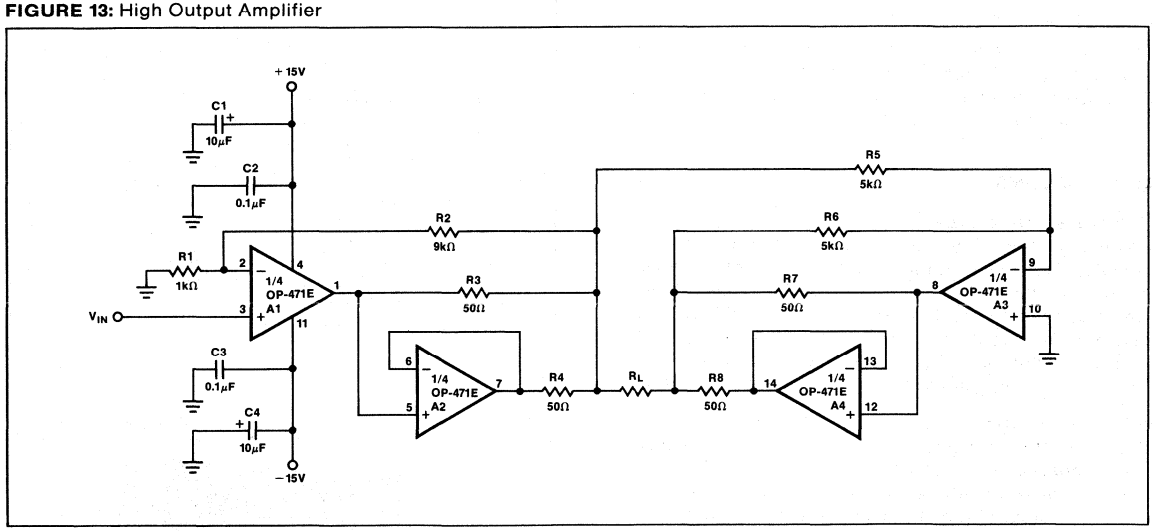


FIGURE 13: High Output Amplifier



QUAD PROGRAMMABLE GAIN AMPLIFIER

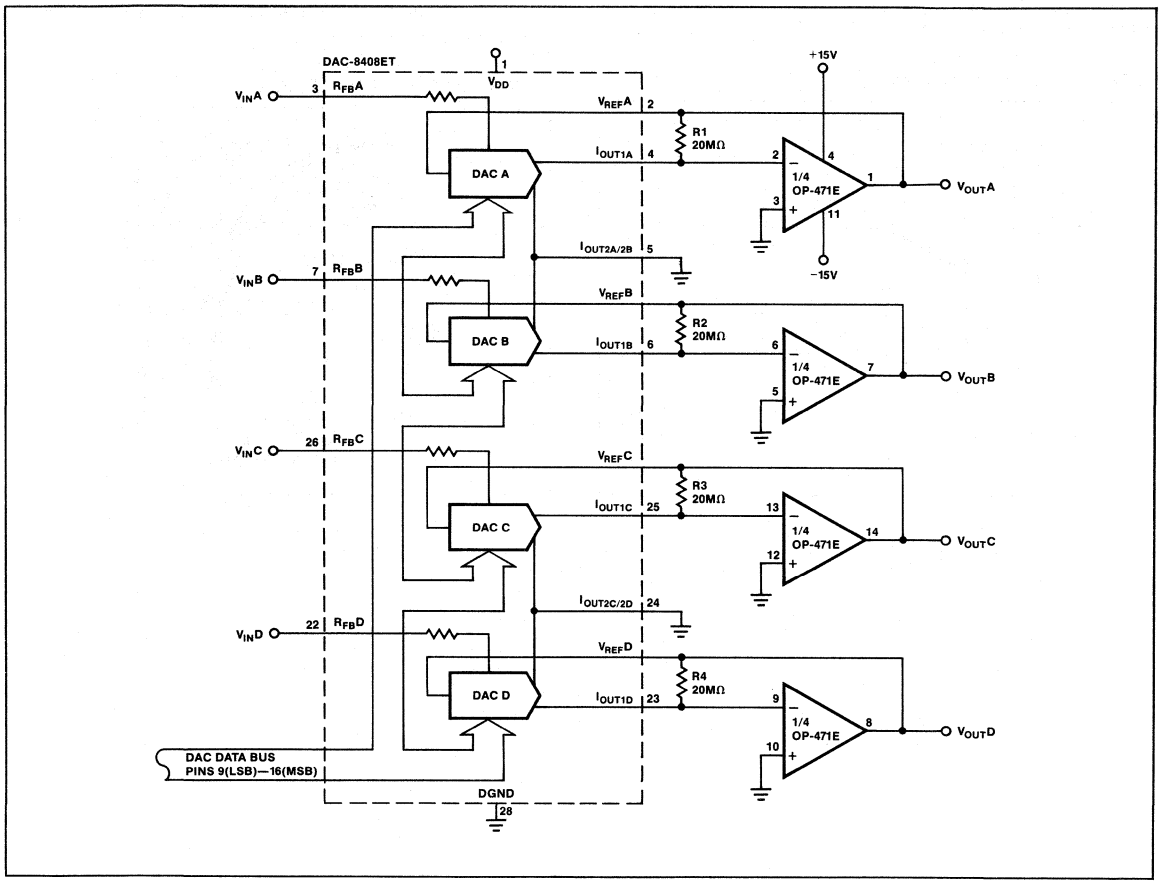
The combination of the quad OP-471 and the DAC-8408, a quad 8-bit CMOS DAC, creates a space-saving quad programmable gain amplifier. The digital code present at the DAC, which is easily set by a microprocessor, determines the ratio between the fixed DAC feedback resistor and the impedance the DAC ladder presents to the op amp feedback loop. Gain of each amplifier is:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{256}{n},$$

where n equals the decimal equivalent of the 8-bit digital code present at the DAC. If the digital code present at the DAC consists of all zeros, the feedback loop will be open causing the op amp output to saturate. The 20MΩ resistors placed in parallel with the DAC feedback loop eliminates this problem with a very small reduction in gain accuracy.

2

FIGURE 14: Quad Programmable Gain Amplifier



LOW PHASE ERROR AMPLIFIER

The simple amplifier depicted in Figure 15 utilizes monolithic matched operational amplifiers and a few resistors to substantially reduce phase error compared to conventional amplifier designs. At a given gain, the frequency range for a specified phase accuracy is over a decade greater than for a standard single op amp amplifier.

The low phase error amplifier performs second-order frequency compensation through the response of op amp A2 in the feedback loop of A1. Both op amps must be extremely well matched in frequency response. At low frequencies, the A1 feedback loop forces $V_2/(K1 + 1) = V_{IN}$. The A2 feedback loop forces $V_O/(K1 + 1) = V_2/(K1 + 1)$ yielding an overall transfer function of $V_O/V_{IN} = K1 + 1$. The DC gain is determined by the resistor divider at the output, V_O, and is not directly affected by the resistor divider around A2. Note, that like a conventional single op amp amplifier, the DC gain is set by resistor ratios only. Minimum gain for the low phase error amplifier is 10.

Figure 16 compares the phase error performance of the low phase error amplifier with a conventional single op amp amplifier and a cascaded two-stage amplifier. The low phase error amplifier shows a much lower phase error, particularly for frequencies where $\omega/\beta\omega_T < 0.1$. For example, phase error of −0.1° occurs at $0.002\ \omega/\beta\omega_T$ for the single op amp amplifier, but at $0.11\ \omega/\beta\omega_T$ for the low phase error amplifier.

For more detailed information on the low phase error amplifier, see Application Note AN-107.

FIGURE 15: Low Phase Error Amplifier

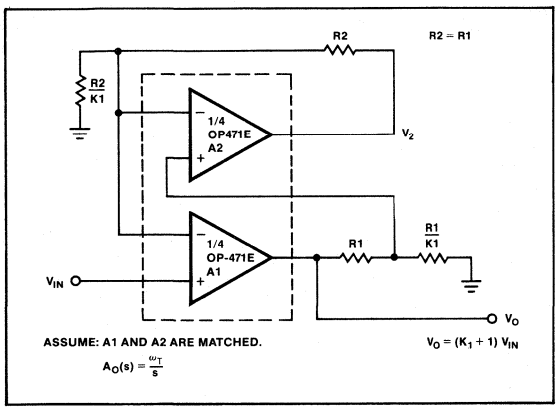
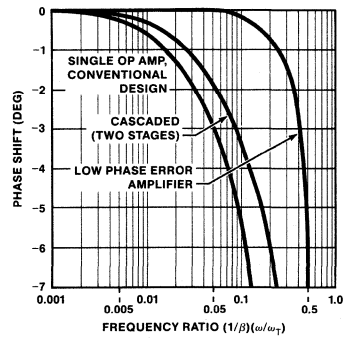


FIGURE 16: Phase Error Comparison



Low-Voltage Micropower Quad Operational Amplifier

OP-490

FEATURES

- **Single/Dual Supply Operation ..... +1.6V to +36V**
  ..... ±0.8V to ±18V
- **True Single-Supply Operation; Input and Output Voltage Ranges Include Ground**
- **Low Supply Current ..... 80μA Max**
- **High Output Drive ..... 5mA Min**
- **Low Offset Voltage ..... 0.5mA Max**
- **High Open-Loop Gain ..... 700V/mV Min**
- **Outstanding PSRR ..... 5.6μV/V Min**
- **Industry Standard Quad Pinouts**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (mV)	PACKAGE			OPERATING TEMPERATURE RANGE
	CERDIP 14-PIN	PLASTIC	LCC 28-CONTACT	
0.5	OP490AY*	–	OP490ATC/883	MIL
0.5	OP490EY	–	–	IND
0.75	OP490FY	–	–	IND
1.0	–	OP490GP	–	XIND
1.0	–	OP490GS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

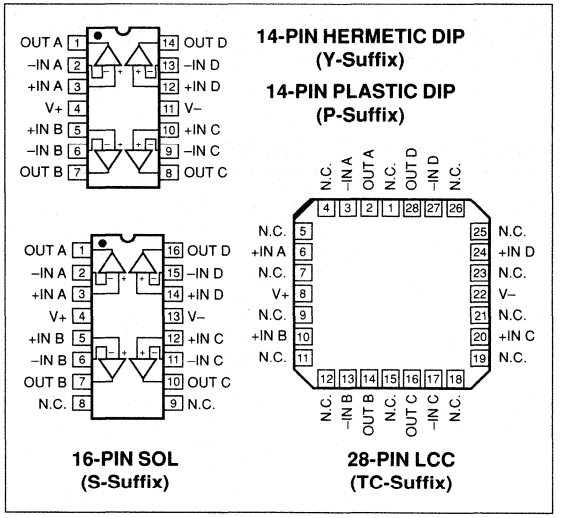
†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

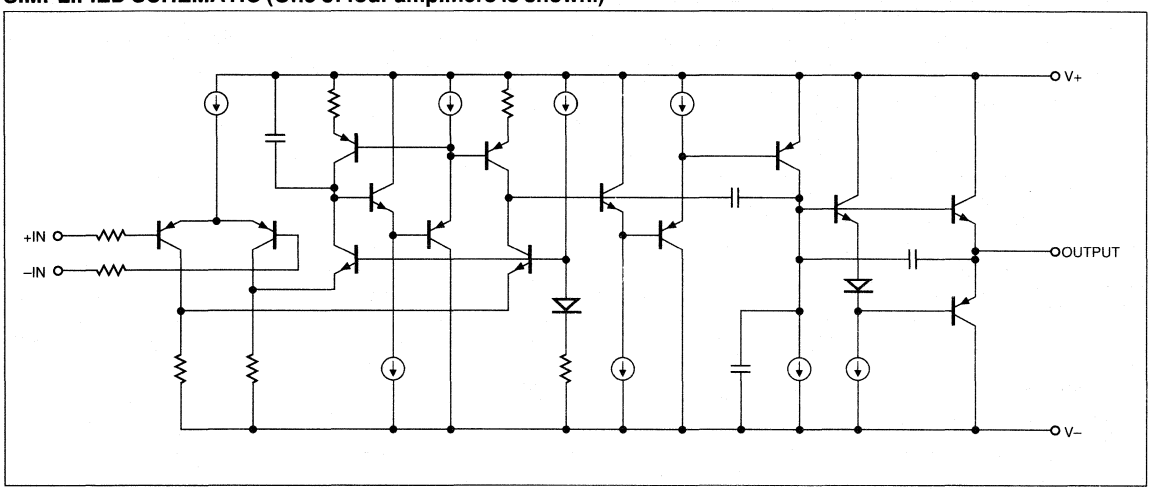
The OP-490 is a high-performance micropower quad op amp that operates from a single supply of +1.6V to +36V or from dual supplies of ±0.8V to ±18V. Input voltage range includes the negative rail allowing the OP-490 to accommodate input signals down to ground in single-supply operation. The OP-490's output swing also includes ground when operating from a single supply, enabling "zero-in, zero-out" operation.

Continued

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC (One of four amplifiers is shown.)



The quad OP-490 draws less than 20μA of quiescent supply current per amplifier, but each amplifier is able to deliver over 5mA of output current to a load. Input offset voltage is under 0.5mV with offset drift below 5μV/°C over the military temperature range. Gain exceeds 700,000 and CMR is better than 100dB. A PSRR of under 5.6μV/V minimizes offset voltage changes experienced in battery powered systems.

The quad OP-490 combines high performance with the space and cost savings of quad amplifiers. The minimal voltage and current requirements of the OP-490 makes it ideal for battery and solar powered applications, such as portable instruments and remote sensors.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage ..... ±18V
Differential Input Voltage ..... [(V–) – 20V] to [(V+) + 20V]
Common-Mode Input Voltage ..... [(V–) – 20V] to [(V+) + 20V]
Output Short-Circuit Duration ..... Continuous
Storage Temperature Range
TC, Y, P Package ..... –65°C to +150°C
Operating Temperature Range
OP-490A ..... –55°C to +125°C
OP-490E, OP-490F ..... –25°C to +85°C
OP-490G ..... –40°C to +85°C
Junction Temperature (T_j) ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
14-Pin Hermetic DIP (Y)	99	12	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
28-Contact LCC (TC)	78	30	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.
2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm1.5V$ to $\pm15V$, $T_A = +25°C$, unless otherwise noted.

			OP-490A/E			OP-490F			OP-490G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.2	0.5	—	0.4	0.75	—	0.6	1.0	mV
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	0.4	3	—	0.4	5	—	0.4	5	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	4.2	15	—	4.2	20	—	4.2	25	nA
Large Signal Voltage Gain	A_{VO}	$V_S = \pm15V$, $V_O = \pm10V$										
		$R_L = 100k\Omega$	700	1200	—	500	1000	—	400	800	—	V/mV
		$R_L = 10k\Omega$	350	600	—	250	500	—	200	400	—	
		$R_L = 2k\Omega$	125	250	—	100	200	—	100	200	—	
		V+ = 5V, V– = 0V, $1V < V_O < 4V$										
		$R_L = 100k\Omega$	200	400	—	125	300	—	100	250	—	
		$R_L = 10k\Omega$	100	180	—	75	140	—	70	140	—	
Input Voltage Range	IVR	V+ = 5V, V– = 0V	0/4	—	—	0/4	—	—	0/4	—	—	V
		$V_S = \pm15V$ (Note 1)	−15/13.5	—	—	−15/13.5	—	—	−15/13.5	—	—	
Output Voltage Swing	V_O	$V_S = \pm15V$										
		$R_L = 10k\Omega$	±13.5	±14.2	—	±13.5	±14.2	—	±13.5	±14.2	—	V
		$R_L = 2k\Omega$	±10.5	±11.5	—	±10.5	±11.5	—	±10.5	±11.5	—	
	V_{OH}	V+ = 5V, V– = 0V										
		$R_L = 2k\Omega$	4.0	4.2	—	4.0	4.2	—	4.0	4.2	—	V
	V_{OL}	V+ = 5V, V– = 0V										
		$R_L = 10k\Omega$	—	100	500	—	100	500	—	100	500	μV
Common Mode Rejection	CMR	V+ = 5V, V– = 0V, $0V < V_{CM} < 4V$	90	110	—	80	100	—	80	100	—	dB
		$V_S = \pm15V$, $-15V < V_{CM} < 13.5V$	100	130	—	90	120	—	90	120	—	
Power Supply Rejection Ratio	PSRR		—	1.0	5.6	—	3.2	10	—	3.2	10	μV/V
Slew Rate	SR	$V_S = \pm15V$	5	12	—	5	12	—	5	12	—	V/ms
Supply Current (All Amplifiers)	I_{SY}	$V_S = \pm1.5V$ No Load	—	40	60	—	40	60	—	40	60	μA
		$V_S = \pm15V$ No Load	—	60	80	—	60	80	—	60	80	
Capacitive Load Stability		$A_V = +1$	—	650	—	—	650	—	—	650	—	pF
Input Noise Voltage	e_{np-p}	$f_O = 0.1Hz$ to 10Hz, $V_S = \pm15V$	—	3	—	—	3	—	—	3	—	μV_{p-p}

ELECTRICAL CHARACTERISTICS at $V_S = \pm1.5V$ to $\pm15V$, $T_A = +25°C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-490A/E MIN	OP-490A/E TYP	OP-490A/E MAX	OP-490F MIN	OP-490F TYP	OP-490F MAX	OP-490G MIN	OP-490G TYP	OP-490G MAX	UNITS
Input Resistance Differential Mode	R_{IN}	$V_S = \pm15V$	—	30	—	—	30	—	—	30	—	MΩ
Input Resistance Common Mode	R_{INCM}	$V_S = \pm15V$	—	20	—	—	20	—	—	20	—	GΩ
Gain Bandwidth Product	GBWP	$A_V = +1$	—	20	—	—	20	—	—	20	—	kHz
Channel Separation	CS	$f_O = 10Hz$ $V_O = 20V_{p-p}$ $V_S = \pm15V$ (Note 2)	120	150	—	120	150	—	120	150	—	dB

NOTES:
1. Guaranteed by CMR test.
2. Guaranteed but not 100% tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm1.5V$ to $\pm15V$, $-55°C \le T_A \le 125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-490A MIN	OP-490A TYP	OP-490A MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.4	1.0	mV
Average Input Offset Voltage Drift	TCV_{OS}	$V_S = \pm15V$	—	2	5	μV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	1.5	5	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	4.4	20	nA
Large Signal Voltage Gain	A_{VO}	$V_S = \pm15V$, $V_O = \pm10V$				V/mV
		$R_L = 100k\Omega$	225	400	—	
		$R_L = 10k\Omega$	125	240	—	
		$R_L = 2k\Omega$	50	110	—	
		V+ = 5V, V− = 0V, $1V < V_O < 4V$				
		$R_L = 100k\Omega$	100	200	—	
		$R_L = 10k\Omega$	50	110	—	
Input Voltage Range	IVR	V+ = 5V, V− = 0V	0/3.5	—	—	V
		$V_S = \pm15V$ (Note 1)	−15/13.5	—	—	
Output Voltage Swing	V_O	$V_S = \pm15V$				V
		$R_L = 10k\Omega$	±13	±13.7	—	
		$R_L = 2k\Omega$	±10	±11	—	
	V_{OH}	V+ = 5V, V− = 0V				V
		$R_L = 2k\Omega$	3.9	4.1	—	
	V_{OL}	V+ = 5V, V− = 0V				μV
		$R_L = 10k\Omega$	—	100	500	
Common Mode Rejection	CMR	V+ = 5V, V− = 0V, $0V < V_{CM} < 3.5V$	85	105	—	dB
		$V_S = \pm15V$, $-15V < V_{CM} < 13.5V$	95	115	—	
Power Supply Rejection Ratio	PSRR		—	3.2	10	μV/V
Supply Current (All Amplifiers)	I_{SY}	$V_S = \pm1.5V$ No Load	—	70	100	μA
		$V_S = \pm15V$	—	90	120	

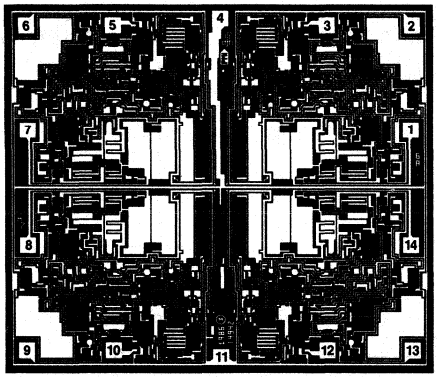
NOTE:
1. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5V$ to $\pm 15V$, $-25°C \le T_A \le +85°C$ for OP-490E/F, $-40°C \le T_A \le +85°C$ for OP490G, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-490E MIN	OP-490E TYP	OP-490E MAX	OP-490F MIN	OP-490F TYP	OP-490F MAX	OP-490G MIN	OP-490G TYP	OP-490G MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.32	0.8	—	0.6	1.35	—	0.8	1.5	mV
Average Input Offset Voltage Drift	TCV_{OS}	$V_S = \pm 15V$	—	2	5	—	4	—	—	4	—	µV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	0.8	3	—	1.0	5	—	1.3	7	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	4.4	15	—	4.4	20	—	4.4	25	nA
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_O = \pm 10V$										V/mV
		$R_L = 100k\Omega$	500	800	—	350	700	—	300	600	—	
		$R_L = 10k\Omega$	250	400	—	175	350	—	150	250	—	
		$R_L = 2k\Omega$	100	200	—	75	150	—	75	125	—	
		V+ = 5V, V− = 0V, $1V < V_O < 4V$										
		$R_L = 100k\Omega$	150	280	—	100	220	—	80	160	—	
		$R_L = 10k\Omega$	75	140	—	50	110	—	40	90	—	
Input Voltage Range	IVR	V+ = 5V, V− = 0V	0/3.5	—	—	0/3.5	—	—	0/3.5	—	—	V
		$V_S = \pm 15V$ (Note 1)	−15/13.5	—	—	−15/13.5	—	—	−15/13.5	—	—	
Output Voltage Swing	V_O	$V_S = \pm 15V$										V
		$R_L = 10k\Omega$	±13	±14	—	±13	±14	—	±13	±14	—	
		$R_L = 2k\Omega$	±10	±11	—	±10	±11	—	±10	±11	—	
	V_{OH}	V+ = 5V, V− = 0V										V
		$R_L = 2k\Omega$	3.9	4.1	—	3.9	4.1	—	3.9	4.1	—	
	V_{OL}	V+ = 5V, V− = 0V										µV
		$R_L = 10k\Omega$	—	100	500	—	100	500	—	100	500	
Common Mode Rejection	CMR	V+ = 5V, V− = 0V, $0V < V_{CM} < 3.5V$	90	110	—	80	100	—	80	100	—	dB
		$V_S = \pm 15V$, $-15V < V_{CM} < 13.5V$	100	120	—	90	110	—	90	110	—	
Power Supply Rejection Ratio	PSRR		—	1.0	5.6	—	3.2	10	—	5.6	17.8	µV/V
Supply Current (All Amplifiers)	I_{SY}	$V_S = \pm 1.5V$ No Load	—	65	100	—	65	100	—	60	100	µA
		$V_S = \pm 15V$ No Load	—	80	120	—	80	120	—	75	120	

NOTE:
1. Guaranteed by CMR test.

DICE CHARACTERISTICS



DIE SIZE 0.139 × 0.121 inch, 16,819 sq. mils
(3.53 × 3.07 mm, 10.84 sq. mm)

1. OUT A
2. −IN A
3. +IN A
4. V+
5. +IN B
6. −IN B
7. OUT B
8. OUT C
9. −IN C
10. +IN C
11. V−
12. +IN D
13. −IN D
14. OUT D

2

WAFER TEST LIMITS at $V_S = \pm 1.5V$ to $\pm 15V$, $T_A = 25°C$, unless otherwise noted.

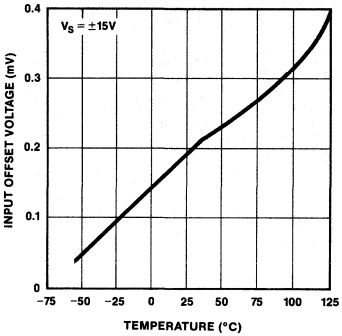
PARAMETER	SYMBOL	CONDITIONS	OP-490GBC LIMIT	UNITS
Input Offset Voltage	V_{OS}		0.75	mV MAX
Input Offset Current	I_{OS}	$V_{CM} = 0V$	5	nA MAX
Input Bias Current	I_B	$V_{CM} = 0V$	20	nA MAX
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_O = \pm 10V$ $R_L = 100k\Omega$ $R_L = 10k\Omega$	 500 250	V/mV MIN
		V+ = 5V, V− = 0V, $1V < V_O < 4V$, $R_L = 100k\Omega$	125	V/mV MIN
Input Voltage Range	IVR	V+ = 5V, V− = 0V $V_S = \pm 15V$ (Note 1)	0/4 −15/13.5	V MIN
Output Voltage Swing	V_O	$V_S = \pm 15V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	 ±13.5 ±10.5	V MIN
	V_{OH}	V+ = 5V, V− = 0V $R_L = 2k\Omega$	 4.0	V MIN
	V_{OL}	V+ = 5V, V− = 0V $R_L = 10k\Omega$	 500	μV MAX
Common Mode Rejection	CMR	V+ = 5V, V− = 0V, $0V < V_{CM} < 4V$ $V_S = \pm 15V$, $-15V < V_{CM} < 13.5V$	80 90	dB MIN
Power Supply Rejection Ratio	PSRR		10	μV/V MAX
Supply Current (All Amplifiers)	I_{SY}	$V_S = \pm 15V$, No Load	80	μA MAX

NOTES:
1. Guaranteed by CMR test.

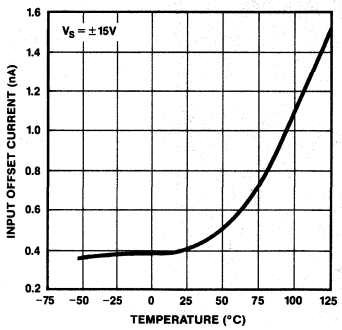
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

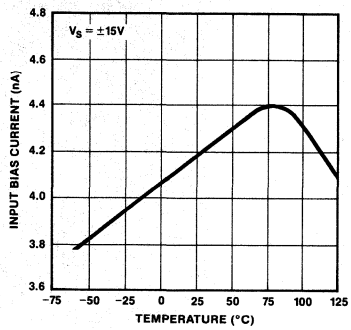
INPUT OFFSET VOLTAGE vs TEMPERATURE



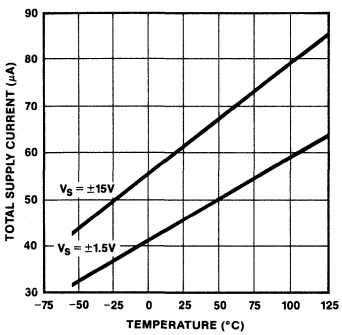
INPUT OFFSET CURRENT vs TEMPERATURE



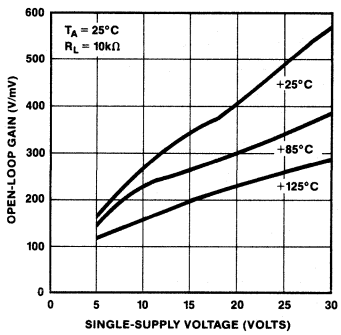
INPUT BIAS CURRENT vs TEMPERATURE



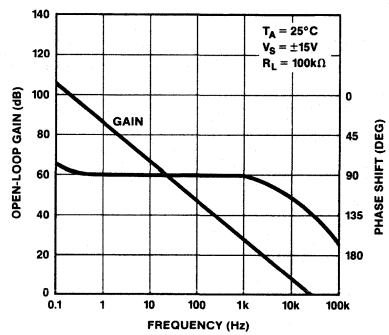
TOTAL SUPPLY CURRENT vs TEMPERATURE



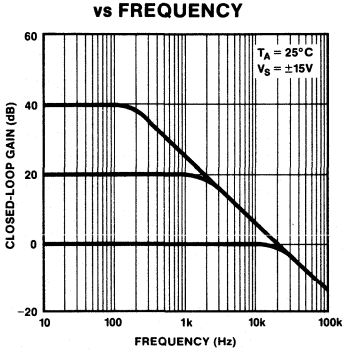
OPEN-LOOP GAIN vs SINGLE-SUPPLY VOLTAGE



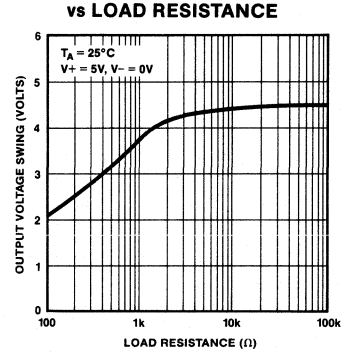
OPEN-LOOP GAIN AND PHASE SHIFT vs FREQUENCY



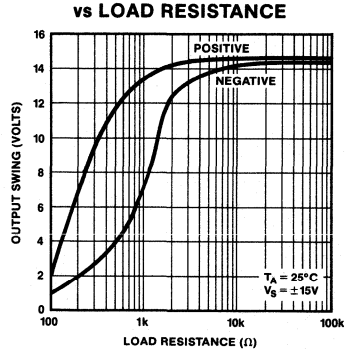
CLOSED-LOOP GAIN vs FREQUENCY



OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

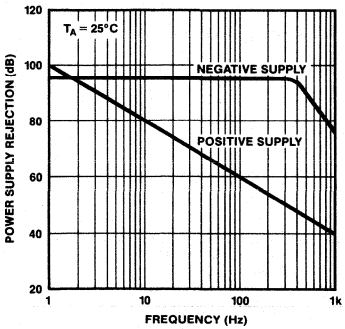


OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

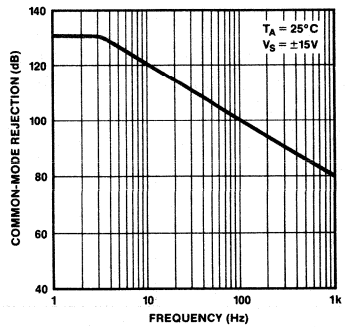


TYPICAL PERFORMANCE CHARACTERISTICS

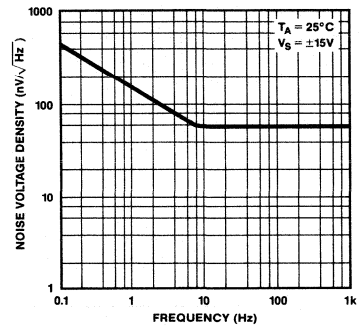
POWER SUPPLY REJECTION vs FREQUENCY



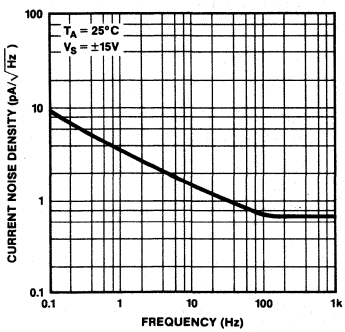
COMMON-MODE REJECTION vs FREQUENCY



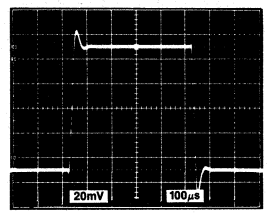
NOISE VOLTAGE DENSITY vs FREQUENCY



CURRENT NOISE DENSITY vs FREQUENCY

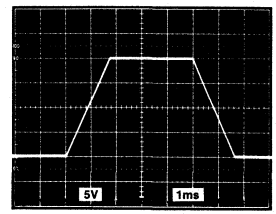


SMALL-SIGNAL TRANSIENT RESPONSE



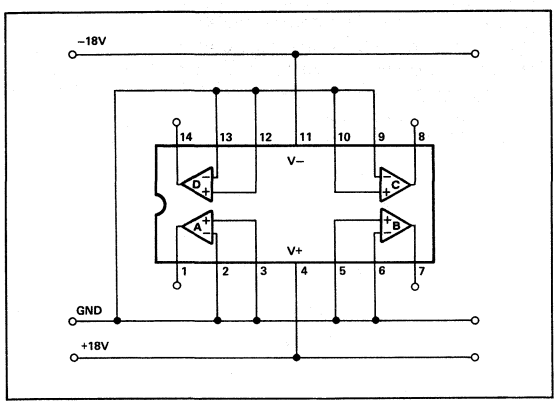
T_A = 25°C
V_S = ±15V
A_V = +1
R_L = 10kΩ
C_L = 500pF

LARGE-SIGNAL TRANSIENT RESPONSE

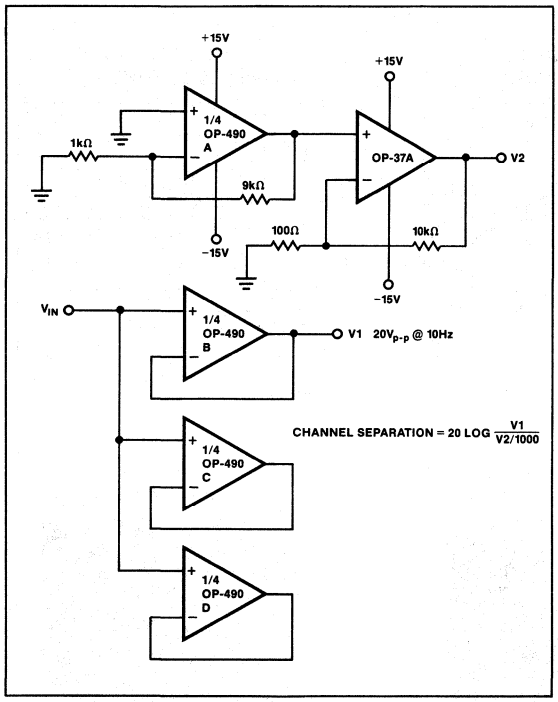


T_A = 25°C
V_S = ±15V
A_V = +1
R_L = 10kΩ
C_L = 500pF

BURN-IN CIRCUIT



CHANNEL SEPARATION TEST CIRCUIT



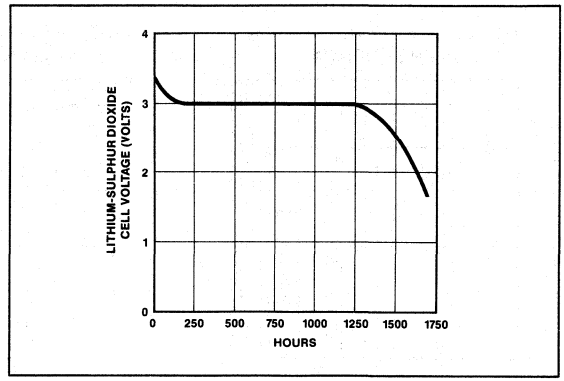
APPLICATIONS INFORMATION

BATTERY-POWERED APPLICATIONS

The OP-490 can be operated on a minimum supply voltage of +1.6V, or with dual supplies ±0.8V, and draws only 60μA of supply current. In many battery-powered circuits, the OP-490 can be continuously operated for hundreds of hours before requiring battery replacement, reducing equipment downtime and operating cost.

High-performance portable equipment and instruments frequently use lithium cells because of their long shelf-life, light weight, and high energy density relative to older primary cells. Most lithium cells have a nominal output voltage of 3V and are noted for a flat discharge characteristic. The low supply voltage requirement of the OP-490, combined with the flat discharge characteristic of the lithium cell, indicates that the OP-490 can be operated over the entire useful life of the cell. Figure 1 shows the typical discharge characteristic of a 1Ah lithium cell powering an OP-490 with each amplifier, in turn, driving full output swing into a 100kΩ load.

FIGURE 1: Lithium-Sulphur Dioxide Cell Discharge Characteristic With OP-490 and 100kΩ Loads



SINGLE-SUPPLY OUTPUT VOLTAGE RANGE

In single-supply operation the OP-490's input and output ranges include ground. This allows true "zero-in, zero-out" operation. The output stage provides an active pull-down to around 0.8V above ground. Below this level, a load resistance of up to 1MΩ to ground is required to pull the output down to zero.

In the region from ground to 0.8V the OP-490 has voltage gain equal to the data sheet specification. Output current source capability is maintained over the entire voltage range including ground.

INPUT VOLTAGE PROTECTION

The OP-490 uses a PNP input stage with protection resistors in series with the inverting and noninverting inputs. The high breakdown of the PNP transistors coupled with the protection resistors provides a large amount of input protection, allowing the inputs to be taken 20V beyond either supply without damaging the amplifier.

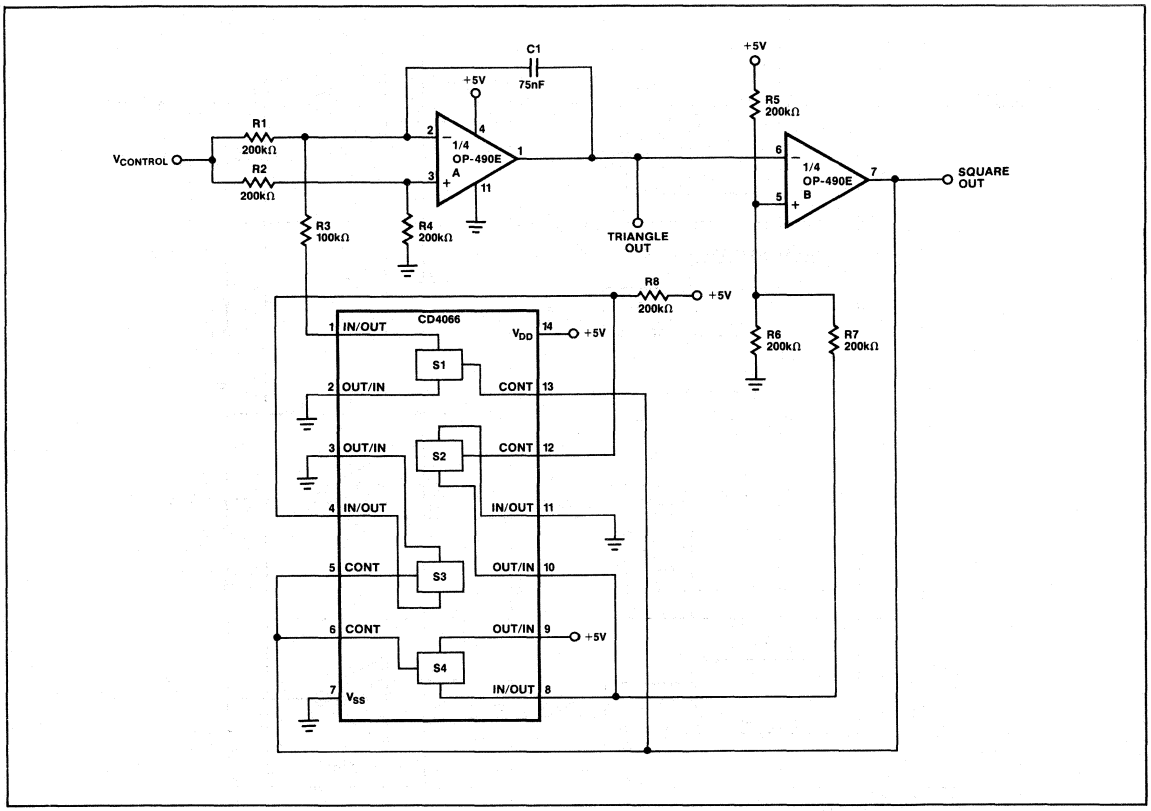
MICROPOWER VOLTAGE-CONTROLLED OSCILLATOR

An OP-490 in combination with an inexpensive quad CMOS switch comprise the precision VCO of Figure 2. This circuit provides triangle and square wave outputs and draws only 75μA from a single 5V supply. A acts as an integrator; S1 switches the charging current symmetrically to yield positive and negative ramps. The integrator is bounded by B which acts as a Schmitt trigger with a precise hysteresis of 1.67 volts, set by resistors R5, R6, and R7, and associated CMOS switches. The resulting output of A is a triangle wave with upper and lower levels of 3.33 and 1.67 volts. The output of B is a square wave with almost rail-to-rail swing. With the components shown, frequency of operation is given by the equation:

$$f_{OUT} = V_{CONTROL}\ (\text{Volts}) \times 10\text{Hz/V}$$

but this is easily changed by varying C1. The circuit operates well up to a few hundred hertz.

FIGURE 2: Micropower Voltage Controlled Oscillator



MICROPOWER SINGLE-SUPPLY QUAD VOLTAGE-OUTPUT 8-BIT DAC

The circuit of Figure 3 uses the DAC-8408 CMOS quad 8-bit DAC, and the OP-490 to form a single-supply quad voltage-output DAC with a supply drain of only 140μA. The DAC-8408 is used in the voltage switching mode and each DAC has an output resistance (≈10kΩ) independent of the digital input code. The output amplifiers act as buffers to avoid loading the DACs. The 100kΩ resistors insure that the OP-490 outputs will swing below 0.8V when required.

FIGURE 3: Micropower Single-Supply Quad Voltage-Output 8-Bit DAC

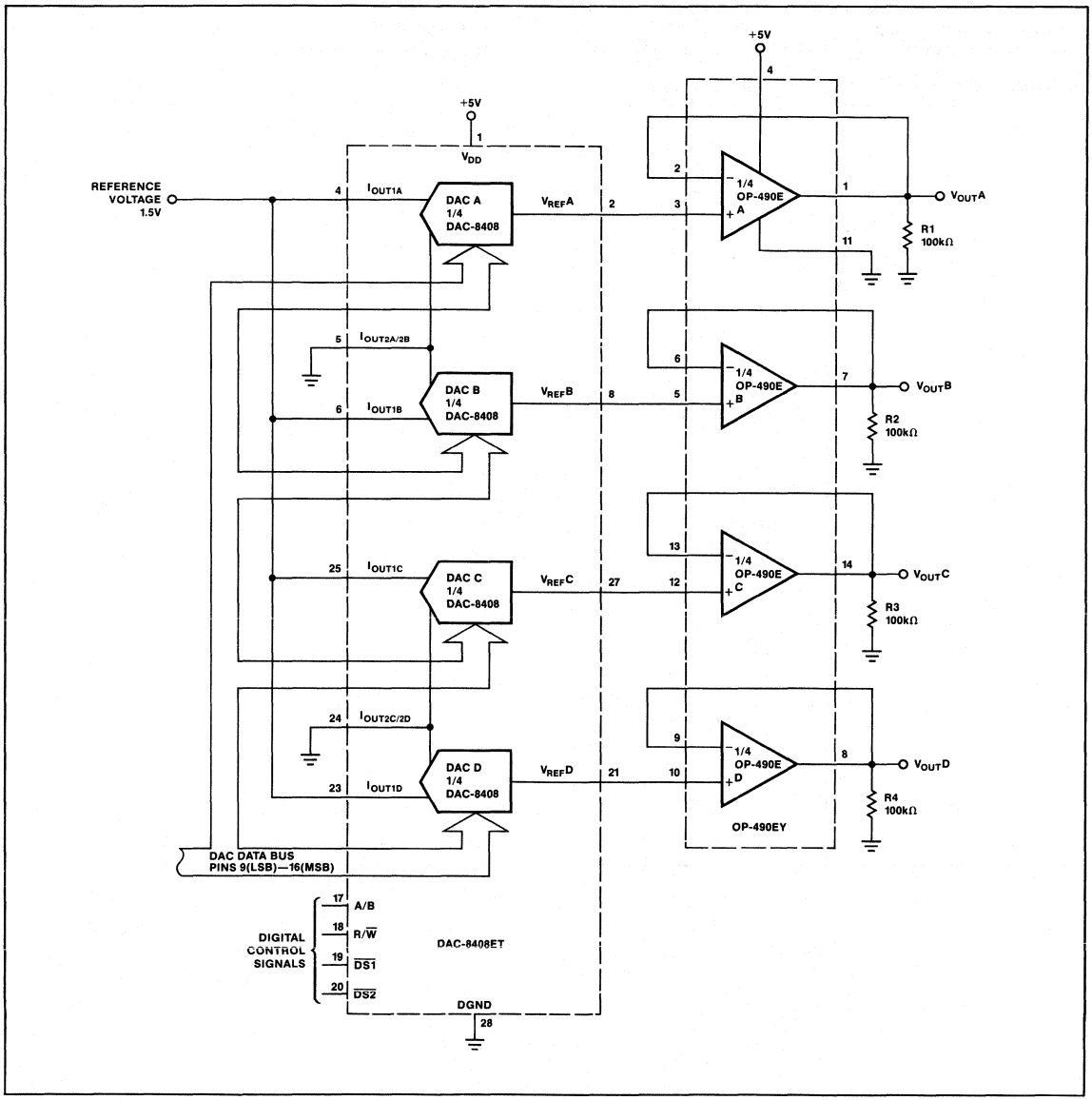
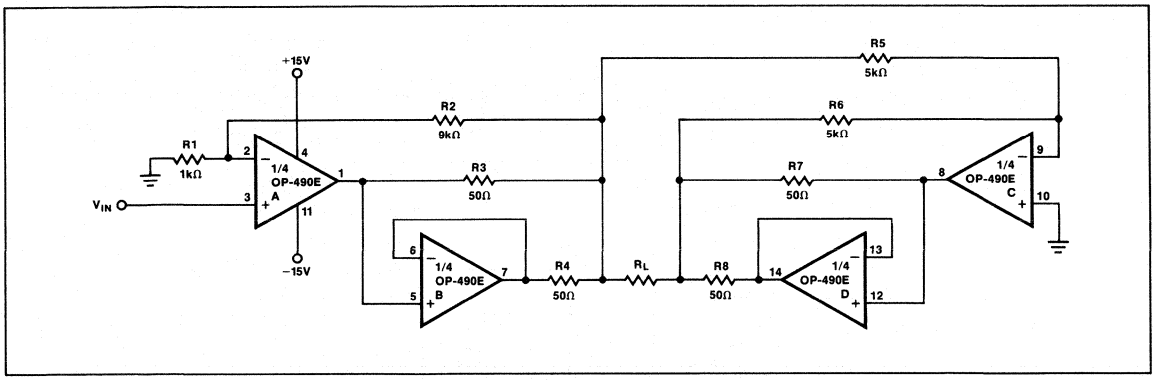


FIGURE 4: High Output Amplifier



HIGH OUTPUT AMPLIFIER

The amplifier shown in Figure 4 is capable of driving $25V_{p-p}$ into a 1kΩ load. Design of the amplifier is based on a bridge configuration. A amplifies the input signal and drives the load with the help of B. Amplifier C is a unity-gain inverter which drives the load with help from D. Gain of the high output amplifier with the component values shown is 10, but can easily be changed by varying R1 or R2.

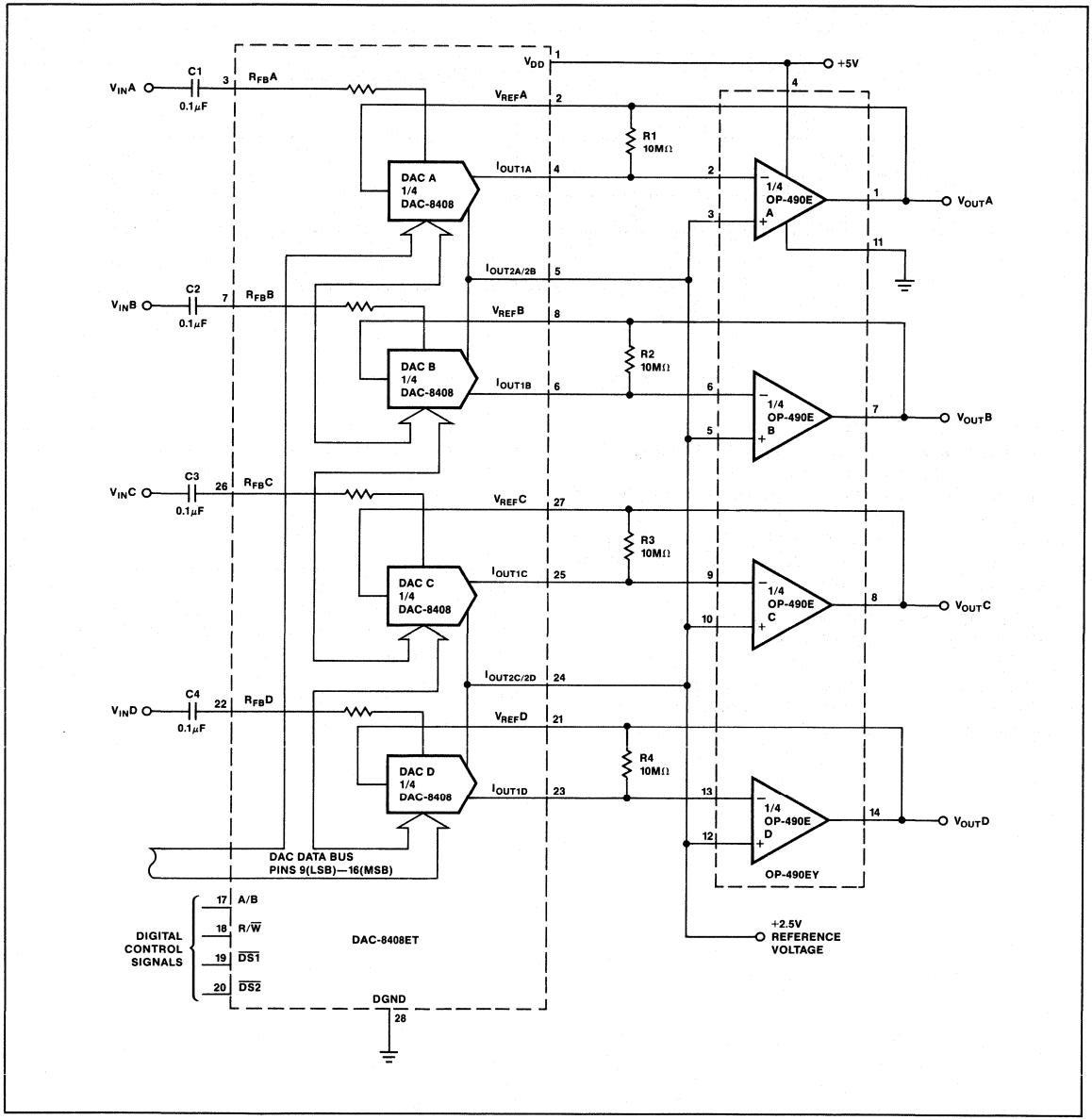
SINGLE-SUPPLY MICROPOWER QUAD PROGRAMMABLE GAIN AMPLIFIER

The combination of the quad OP-490 and the DAC-8408 quad 8-bit CMOS DAC, creates a quad programmable gain amplifier with a quiescent supply drain of only 140μA. The digital code present at the DAC, which is easily set by a microprocessor, determines the ratio between the fixed DAC feedback resistor and the resistance the DAC ladder presents to the op amp feedback loop. Gain of each amplifier is:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{256}{n},$$

where n equals the decimal equivalent of the 8-bit digital code present at the DAC. If the digital code present at the DAC consists of all zeros, the feedback loop will be open causing the op amp output to saturate. The 10MΩ resistors placed in parallel with the DAC feedback loop eliminates this problem with a very small reduction in gain accuracy. The 2.5V reference biases the amplifiers to the center of the linear region providing maximum output swing.

FIGURE 5: Single-Supply Micropower Quad Programmable-Gain Amplifier



Precision Picoampere Input Current Quad Operational Amplifier

OP-497

FEATURES

Low Offset Voltage: 50 μV max
Low Offset Voltage Drift: 0.5 μV/°C max
Very Low Bias Current
+25°C: 100 pA max
−55°C to +125°C: 450 pA max
Very High Open-Loop Gain: 2000 V/mV min
Low Supply Current (per Amplifier): 625 μA max
Operates from ±2 V to ±20 V Supplies
High Common-Mode Rejection: 120 dB min

APPLICATIONS

Strain Gage and Bridge Amplifiers
High Stability Thermocouple Amplifiers
Instrumentation Amplifiers
Photo-Current Monitors
High-Gain Linearity Amplifiers
Long-Term Integrators/Filters
Sample-and-Hold Amplifiers
Peak Detectors
Logarithmic Amplifiers
Battery-Powered Systems

GENERAL DESCRIPTION

The OP-497 is a quad op amp with precision performance in the space saving, industry standard 16-pin SOIC package. Its combination of exceptional precision with low power and extremely low input bias current makes the quad OP-497 useful in a wide variety of applications.

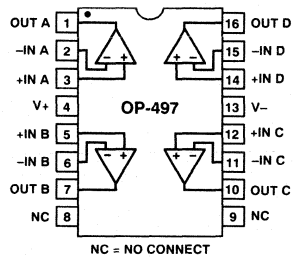
Precision performance of the OP-497 includes very low offset, under 50 μV, and low drift, below 0.5 μV/°C. Open-loop gain exceeds 2000 V/mV insuring high linearity in every application. Errors due to common-mode signals are eliminated by the OP-497's common-mode rejection of over 120 dB. The OP-497's power supply rejection of over 120 dB minimizes offset voltage changes experienced in battery powered systems. Supply current of the OP-497 is under 625 μA per amplifier, and it can operate with supply voltages as low as ±2 V.

The OP-497 utilizes a superbeta input stage with bias current cancellation to maintain picoamp bias currents at all temperatures. This is in contrast to FET input op amps whose bias currents start in the picoamp range at 25°C, but double for every 10°C rise in temperature, to reach the nanoamp range above 85°C. Input bias current of the OP-497 is under 100 pA at 25°C and is under 450 pA over the military temperature range.

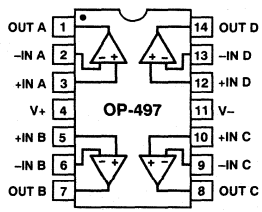
Combining precision, low power and low bias current, the OP-497 is ideal for a number of applications including instrumentation amplifiers, log amplifiers, photo-diode preamplifiers and long term integrators. For a single device see the OP-97, for a dual see the OP-297.

PIN CONNECTIONS

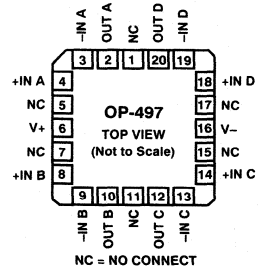
16-Lead Wide Body SOIC
(S Suffix)

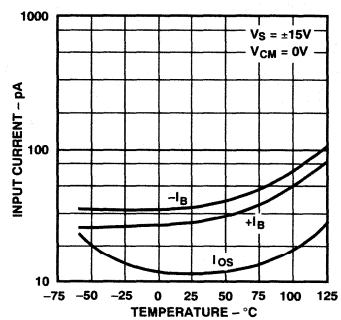


14-Lead Plastic Dip
(P Suffix)
14-Lead Ceramic Dip
(Y Suffix)



20-Position Chip Carrier
(RC Suffix)





Input Bias, Offset Current vs. Temperature

OP-497—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Condition	A Min	A Typ	A Max	B/F Min	B/F Typ	B/F Max	C/G Min	C/G Typ	C/G Max	Units
INPUT CHARACTERISTICS												
Offset Voltage	V_{OS}			20	50		40	75		80	150	µV
		−40°C ≤ T_A ≤ +85°C					70	150		120	250	
		−55°C ≤ T_A ≤ +125°C		40	100		80	150		140	300	
Average Input Offset Voltage Drift	TCV_{OS}	T_{min}–T_{max}		0.2	0.5		0.4	1.0		0.6	1.5	µV/°C
Long Term Input Offset Voltage Stability				0.1			0.1			0.1		µV/Mo
Input Bias Current	I_B	V_{CM} = 0 V		30	100		40	150		60	200	pA
		−40°C ≤ T_A ≤ +85°C					60	200		80	300	
		−55°C ≤ T_A ≤ +125°C		80	450		110	600		130	600	
Average Input Bias Current Drift	TC_{IB}	−40°C ≤ T_A ≤ +85°C					0.3			0.3		
		−55°C ≤ T_A ≤ +125°C		0.5			0.7			0.7		pA/°C
Input Offset Current	I_{OS}	V_{CM} = 0 V		15	100		30	150		50	200	pA
		−40°C ≤ T_A ≤ +85°C					50	200		80	300	
		−55°C ≤ T_A ≤ +125°C		35	400		60	600		90	600	
Average Input Offset Current Drift	T_CI_{OS}			0.2			0.3			0.4		pA/°C
Input Voltage Range[1]	IVR		±13	±14		±13	±14		±13	±14		V
		T_{min}–T_{max}	±13	±13.5		±13	±13.5		±13	±13.5		
Common-Mode Rejection	CMR	V_{CM} = ±13 V	120	140		114	135		114	135		dB
		T_{min}–T_{max}	114	130		108	120		108	120		
Large Signal Voltage Gain	A_{VO}	V_O = ±10 V R_L = 2 kΩ	2000	6000		1500	4000		1200	4000		V/mV
		−40°C ≤ T_A ≤ +85°C	1200	4000		800	2000		800	2000		
		−55°C ≤ T_A ≤ +125°C				1000	3000		800	3000		
Input Resistance Differential Mode	R_{IN}			30			30			30		MΩ
Input Resistance Common Mode	R_{INCM}			500			500			500		GΩ
Input Capacitance	C_{IN}			3			3			3		pF
OUTPUT CHARACTERISTICS												
Output Voltage Swing	V_O	R_L = 2 kΩ	±13	±13.7		±13	±13.7		±13	±13.7		V
		R_L = 10 kΩ	±13	±14		±13	±14		±13	±14		
		T_{min}–T_{max}, R_L = 10 kΩ	±13	±13.5		±13	±13.5		±13	±13.5		
Short Circuit	I_{SC}			±25			±25			±25		mA
POWER SUPPLY												
Power Supply Rejection Ratio	PSRR	V_S = ±2 V to ±20 V	120	140		114	135		114	135		dB
		V_S = ±2.5 V to ±20 V										
		T_{min}–T_{max}	114	130		108	120		108	120		
Supply Current (per Amplifier)	I_{SY}	No Load		525	625		525	625		525	625	µA
		T_{min}–T_{max}		580	750		580	750		580	750	
Supply Voltage Range	V_S	Operating Range	±2		±20	±2		±20	±2		±20	V
		T_{min}–T_{max}	±2.5		±20	±2.5		±20	±2.5		±20	
DYNAMIC PERFORMANCE												
Slew Rate	SR		0.05	0.15		0.05	0.15		0.05	0.15		V/µs
Gain Bandwidth Product	GBW			500			500			500		kHz
Channel Separation	CS	V_O = 20 V p–p fo = 10 Hz		150			150			150		dB
NOISE PERFORMANCE												
Voltage Noise	e_n p–p	0.1 Hz to 10 Hz		0.3			0.3			0.3		µV p–p
Voltage Noise Density	e_n = 10 Hz			17			17			17		nV/√Hz
	e_n = 1 kHz			15			15			15		nV/√Hz
Current Noise Density	i_n = 10 Hz			20			20			20		fA/√Hz

NOTE
[1]Guaranteed by CMR Test.
Specifications subject to change without notice.

WAFER TEST LIMITS (@ V_S = ±15 V, T_A = +25°C, unless otherwise noted)

Parameter	Symbol	Condition	OP-497 GBC Limit	Units
Input Offset Voltage	V_{OS}		150	μV max
Input Offset Current	I_{OS}	V_{CM} = 0 V	150	pA max
Input Bias Current	I_B	V_{CM} = 0 V	150	pA max
Input Voltage Range[1]	IVR		±13	V min
Large Signal Voltage Gain	A_{VO}	V_O = ±10 V, $R_L \leq 10$ kΩ	1500	V/mV min
Common-Mode Rejection	CMR	V_{CM} = ±13 V	114	dB min
Power Supply Rejection	PSR	V_S = ±2 V to ±20 V	114	dB min
Output Voltage Swing	V_O	$R_L \leq 10$ kΩ	±13	V min
		$R_L \leq 2$ kΩ	±13	V min
Supply Current per Amplifier	I_{SY}	No Load	625	μA max

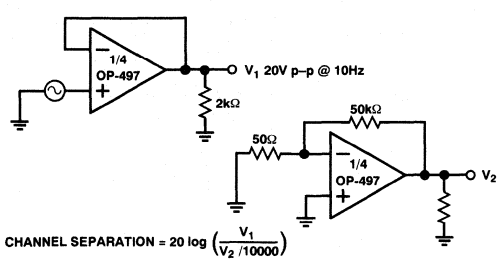
NOTE
[1]Guaranteed by CMR test. Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±20 V
Input Voltage[2] . . . . . ±20 V
Differential Input Voltage[2] . . . . . 40 V
Output Short-Circuit Duration . . . . . Indefinite
Storage Temperature Range
Y, RC Package . . . . . −65°C to +175°C
P, S Package . . . . . −65°C to +150°C
Operating Temperature Range
OP-497A, B, C (Y) . . . . . −55°C to +125°C
OP-497F, G (Y) . . . . . −40°C to +85°C
OP-497F, G (P, S) . . . . . −40°C to +85°C
Junction Temperature
Y, RC Package . . . . . −65°C to +175°C
P, S Package . . . . . −65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C

Package Type	θ_{JA}	θ_{JA}	Units
14-Pin Cerdip (Y)	94	10	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
20-Contact LCC (RC)	78	33	°C/W
16-Pin SOIC (S)	92	23	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±20 V, the absolute maximum input voltage is equal to the supply voltage.
[3]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered to printed circuit board for SOIC package.



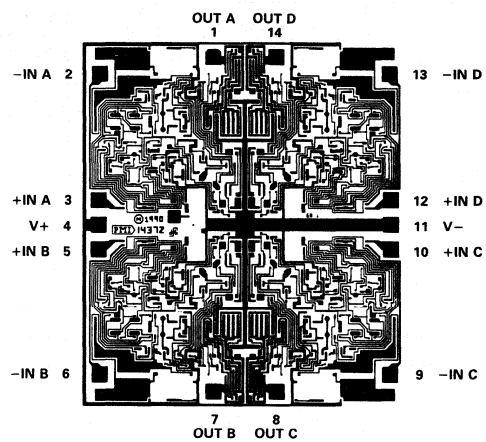
Channel Separation Test Circuit

ORDERING GUIDE

Model	Temperature Range	Package Option*
OP497AY	−55°C to +125°C	14-Pin Cerdip
OP497BY	−55°C to +125°C	14-Pin Cerdip
OP497CY	−55°C to +125°C	14-Pin Cerdip
OP497BRC/883	−55°C to +125°C	20-Contact LCC
OP497FY	−40°C to +85°C	14-Pin Cerdip
OP497FP	−40°C to +85°C	14-Pin Plastic DIP
OP497FS	−40°C to +85°C	16-Pin SOIC
OP497GY	−40°C to +85°C	14-Pin Cerdip
OP497GP	−40°C to +85°C	14-Pin Plastic DIP
OP497GS	−40°C to +85°C	16-Pin SOIC

*For outline information see Package Information section.

DICE CHARACTERISTICS



Die Size 0.112 × 0.129 inch, 14,448 sq. mils

OP-497—Typical Characteristics (@ +25°C, V_S = ±15 V, unless otherwise noted)

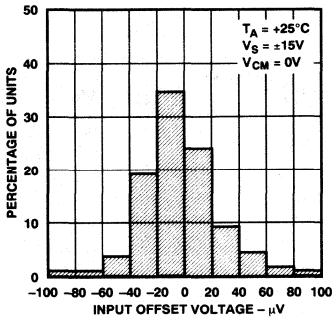


Figure 1. Typical Distribution of Input Offset Voltage

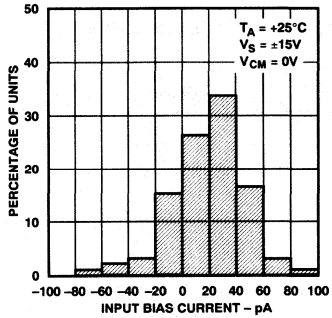


Figure 2. Typical Distribution of Input Bias Current

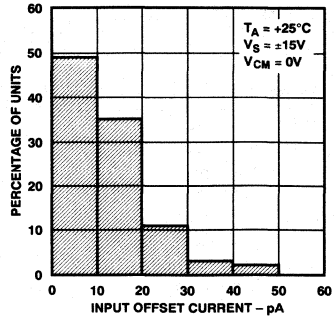


Figure 3. Typical Distribution of Input Offset Current

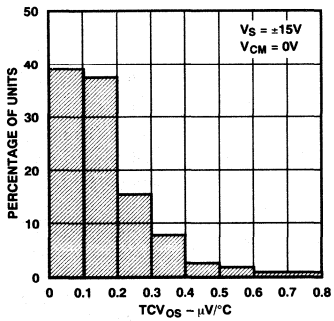


Figure 4. Typical Distribution of TCV_{OS}

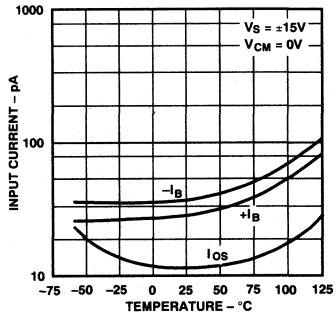


Figure 5. Input Bias, Offset Current vs. Temperature

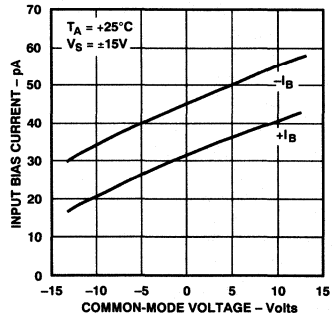


Figure 6. Input Bias Current vs. Common-Mode Voltage

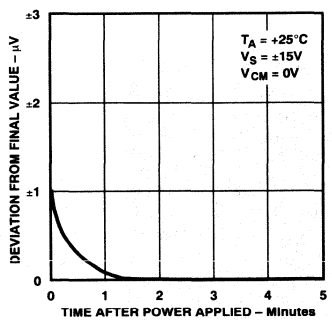


Figure 7. Input Offset Voltage Warm-Up Drift

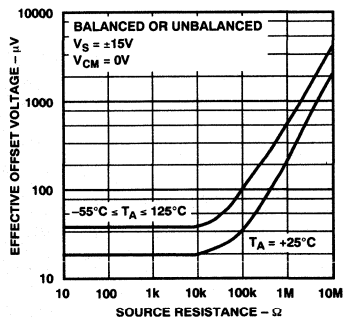


Figure 8. Effective Offset Voltage vs. Source Resistance

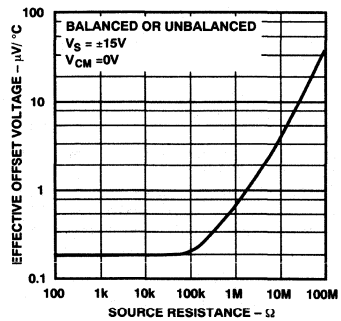


Figure 9. Effective TCV_{OS} vs. Source Resistance

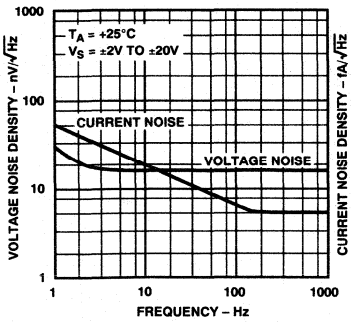


Figure 10. Voltage Noise Density vs. Frequency

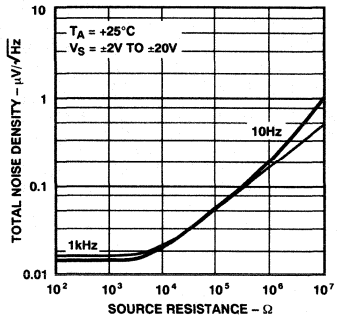


Figure 11. Total Noise Density vs. Source Resistance

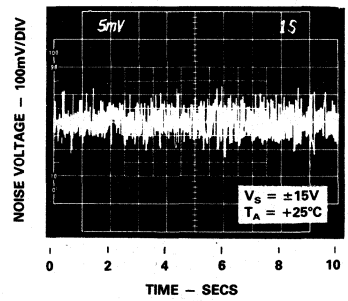


Figure 12. 0.1 Hz to 10 Hz Noise Voltage

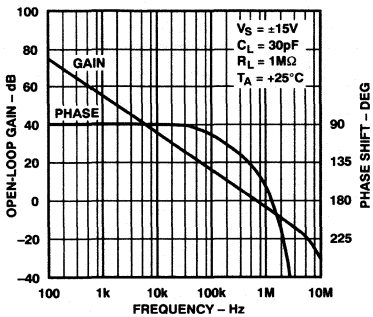


Figure 13. Open-Loop Gain, Phase vs. Frequency

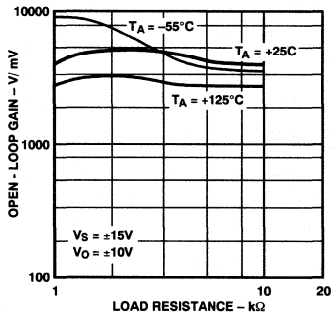


Figure 14. Open-Loop Gain vs. Load Resistance

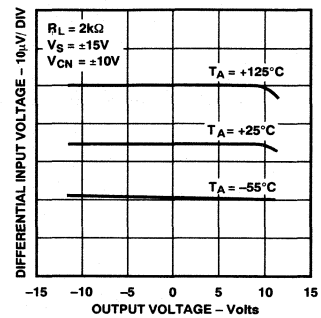


Figure 15. Open-Loop Gain Linearity

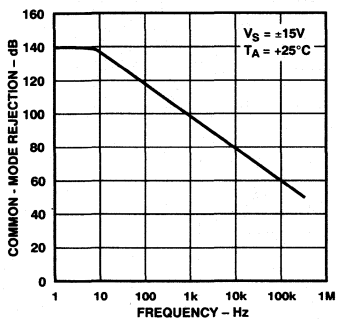


Figure 16. Common-Mode Rejection vs. Frequency

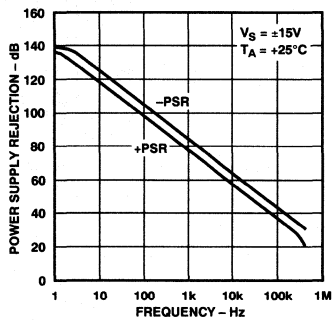


Figure 17. Power Supply Rejection vs. Frequency

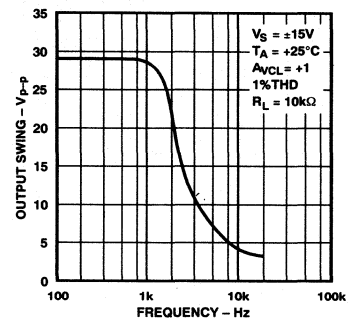


Figure 18. Maximum Output Swing vs. Frequency

OP-497—Typical Characteristics (@ +25°C, V_S = ±15 V, unless otherwise noted)

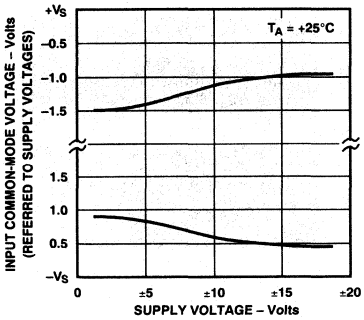


Figure 19. Input Common-Mode Voltage Range vs. Supply Voltage

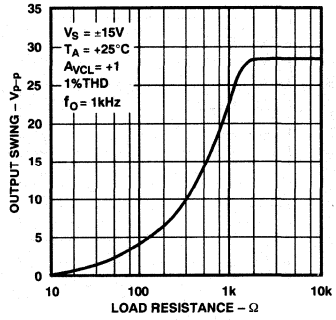


Figure 20. Maximum Output Swing vs. Load Resistance

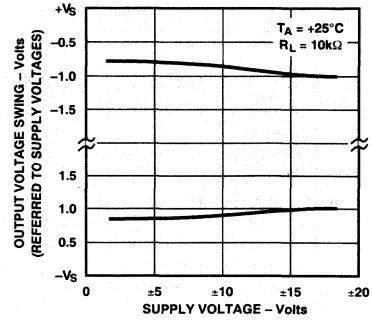


Figure 21. Output Voltage Swing vs. Supply Voltage

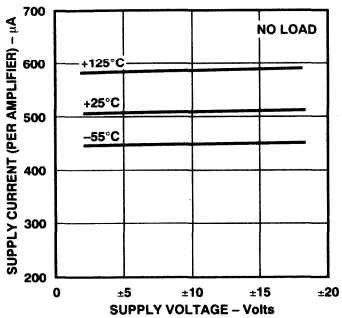


Figure 22. Supply Current (per Amplifier) vs. Supply Voltage

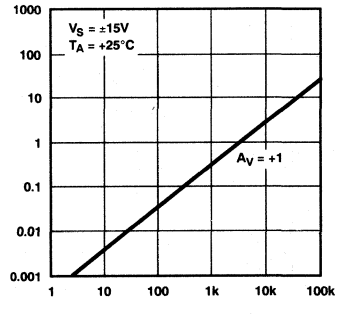


Figure 23. Closed-Loop Output Impedance vs. Frequency

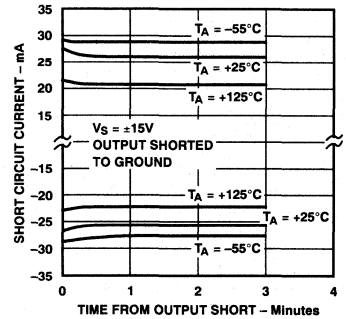


Figure 24. Short-Circuit Current vs. Time Temperature

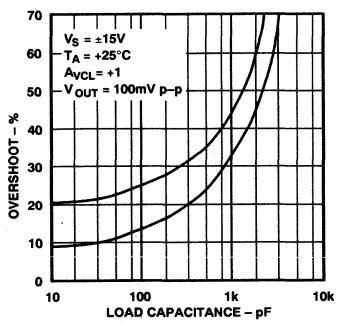


Figure 25. Small-Signal Overshoot vs. Capacitance Load

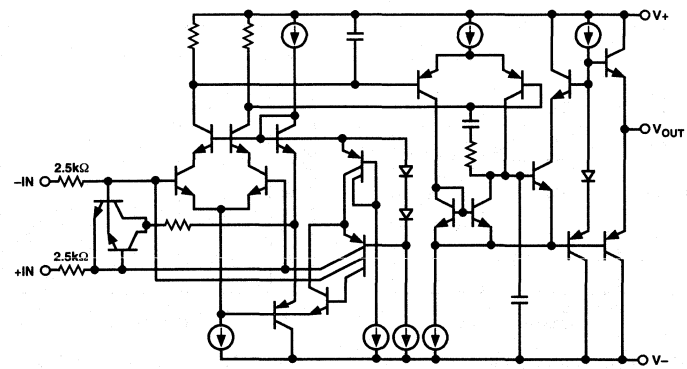


Figure 26. Simplified Schematic Showing One Amplifier

APPLICATIONS INFORMATION

Extremely low bias current over the full military temperature range makes the OP-497 attractive for use in sample-and-hold amplifiers, peak detectors, and log amplifiers that must operate over a wide temperature range. Balancing input resistances is not necessary with the OP-497. Offset voltage and TCV_{OS} are degraded only minimally by high source resistance, even when unbalanced.

The input pins of the OP-497 are protected against large differential voltage by back-to-back diodes and current-limiting resistors. Common-mode voltages at the inputs are not restricted, and may vary over the full range of the supply voltages used.

The OP-497 requires very little operating headroom about the supply rails, and is specified for operation with supplies as low as ±2 V. Typically, the common-mode range extends to within one volt of either rail. The output typically swings to within one volt of the rails when using a 10 kΩ load.

AC PERFORMANCE

The OP-497's ac characteristics are highly stable over its full operating temperature range. Unity-gain small-signal response is shown in Figure 27. Extremely tolerant of capacitive loading on the output, the OP-497 displays excellent response even with 1000 pF loads (Figure 28).

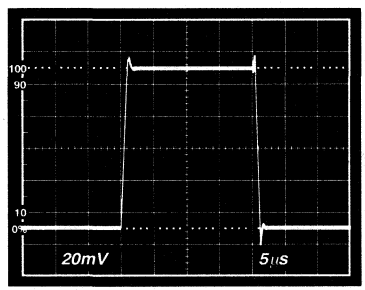


Figure 27. Small Signal Transient Response (C_{LOAD} = 100 pF, A_{VCL} = +1)

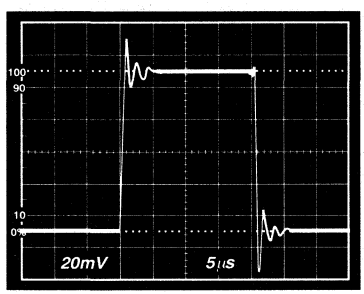


Figure 28. Small Signal Transient Response (C_{LOAD} = 1000 pF, A_{VCL} = +1)

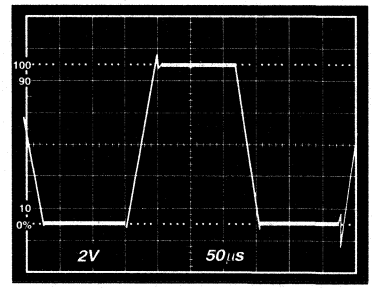


Figure 29. Large Signal Transient Response (A_{VCL} = +1)

GUARDING AND SHIELDING

To maintain the extremely high input impedances of the OP-497, care must be taken in circuit board layout and manufacturing. Board surfaces must be kept scrupulously clean and free of moisture. Conformal coating is recommended to provide a humidity barrier. Even a clean PC board can have 100 pA of leakage currents between adjacent traces, so guard rings should be used around the inputs. Guard traces are operated at a voltage close to that on the inputs, as shown in Figure 30, so that leakage currents become minimal. In noninverting applications, the guard ring should be connected to the common-mode voltage at the inverting input. In inverting applications, both inputs remain at ground, so the guard trace should be grounded. Guard traces should be on both sides of the circuit board.

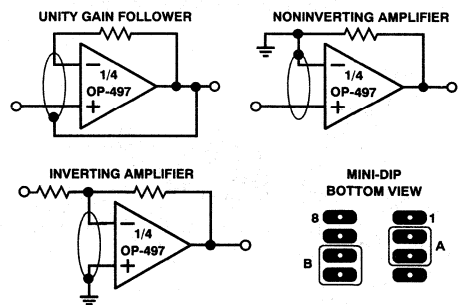


Figure 30. Guard Ring Layout and Connections

OPEN-LOOP GAIN LINEARITY

The OP-497 has both an extremely high gain of 2000 V/mv minimum and constant gain linearity. This enhances the precision of the OP-497 and provides for very high accuracy in high closed-loop gain applications. Figure 31 illustrates the typical open-loop gain linearity of the OP-497 over the military temperature range.

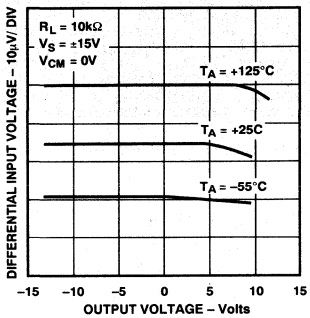


Figure 31. Open-Loop Linearity of the OP-497

APPLICATIONS

Precision Absolute Value Amplifier

The circuit of Figure 32 is a precision absolute value amplifier with an input impedance of 30 MΩ. The high gain and low TCV_{OS} of the OP-497 insure accurate operation with microvolt input signals. In this circuit, the input always appears as a common-mode signal to the op amps. The CMR of the OP-497 exceeds 120 dB, yielding an error of less than 2 ppm.

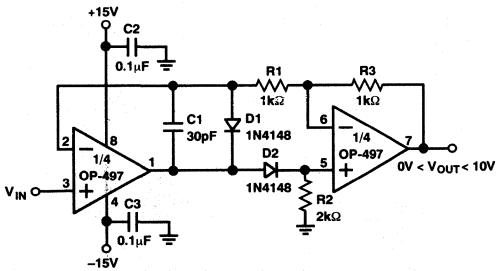


Figure 32. Precision Absolute Value Amplifier

PRECISION CURRENT PUMP

Maximum output current of the precision current pump shown in Figure 33 is ±10 mA. Voltage compliance is ±10 V with ±15 V supplies. Output impedance of the current transmitter exceeds 3 MΩ with linearity better than 16 bits.

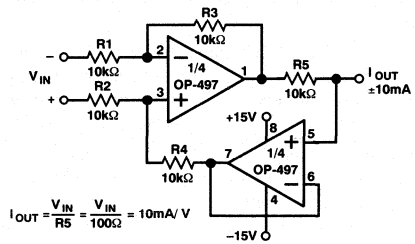


Figure 33. Precision Current Pump

PRECISION POSITIVE PEAK DETECTOR

In Figure 34, the C_H must be of polystyrene, Teflon*, or polyethylene to minimize dielectric absorption and leakage. The droop rate is determined by the size of C_H and the bias current of the OP-497.

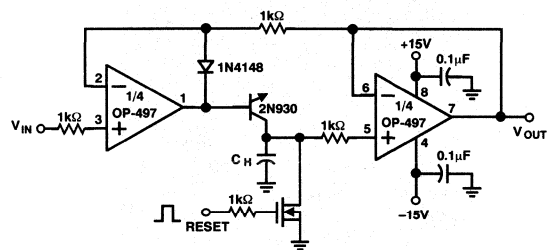


Figure 34. Precision Positive Peak Detector

SIMPLE BRIDGE CONDITIONING AMPLIFIER

Figure 35 shows a simple bridge conditioning amplifier using the OP-497. The transfer function is:

$$V_{OUT} = V_{REF}\left(\frac{\Delta R}{R + \Delta R}\right)\frac{R_F}{R}$$

The REF-43 provides an accurate and stable reference voltage for the bridge. To maintain the highest circuit accuracy, R_F should be 0.1% or better with a low temperature coefficient.

*Teflon is a registered trademark of the Dupont Company.

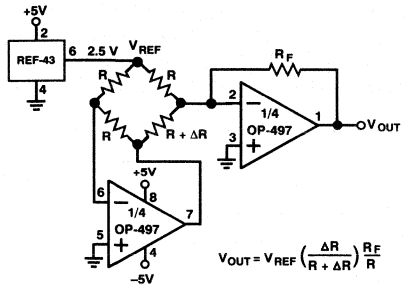


Figure 35. A Simple Bridge Conditioning Amplifier Using the OP-497

NONLINEAR CIRCUITS

Due to its low input bias currents, the OP-497 is an ideal log amplifier in nonlinear circuits such as the square and square-root circuits shown in Figures 36 and 37. Using the squaring circuit of Figure 36 as an example, the analysis begins by writing a voltage loop equation across transistors Q_1, Q_2, Q_3 and Q_4.

$$V_{T1}\, In\left(\frac{I_{IN}}{I_{S1}}\right) + V_{T2}\, In\left(\frac{I_{IN}}{I_{S2}}\right) = V_{T3}\, In\left(\frac{I_O}{I_{S3}}\right) + V_{T4}\, In\left(\frac{I_{REF}}{I_{S4}}\right)$$

All the transistors of the MAT-04 are precisely matched and at the same temperature, so the I_S and V_T terms cancel, giving:

$$2\, In\, I_{IN} = In\, I_O + In\, I_{REF} = In\,(I_O \times I_{REF})$$

Exponentiating both sides of the equation leads to:

$$I_O = \frac{(I_{IN})^2}{I_{REF}}$$

Op amp A_2 forms a current-to-voltage converter which gives $V_{OUT} = R2 \times I_O$. Substituting $(V_{IN}/R1)$ for I_{IN} and the above equation for I_O yields:

$$V_{OUT} = \left(\frac{R2}{I_{REF}}\right)\left(\frac{V_{IN}}{R1}\right)^2$$

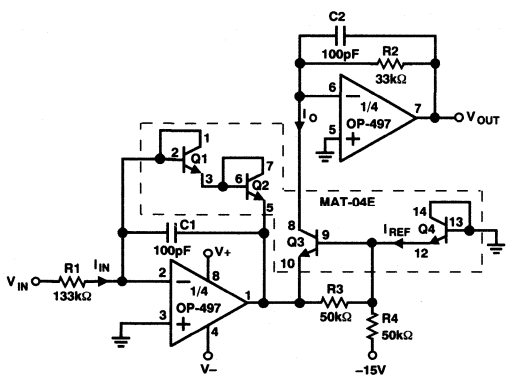


Figure 36. Squaring Amplifier

A similar analysis made for the square-root circuit of Figure 37 leads to its transfer function:

$$V_{OUT} = R2\sqrt{\frac{(V_{IN})\,(I_{REF})}{R1}}$$

In these circuits, I_{REF} is a function of the negative power supply. To maintain accuracy, the negative supply should be well regulated. For applications where very high accuracy is required, a voltage reference may be used to set I_{REF}. An important consideration for the squaring circuit is that a sufficiently large input voltage can force the output beyond the operating range of the output op amp. Resistor R4 can be changed to scale I_{REF}, or R1 and R2 can be varied to keep the output voltage within the usable range.

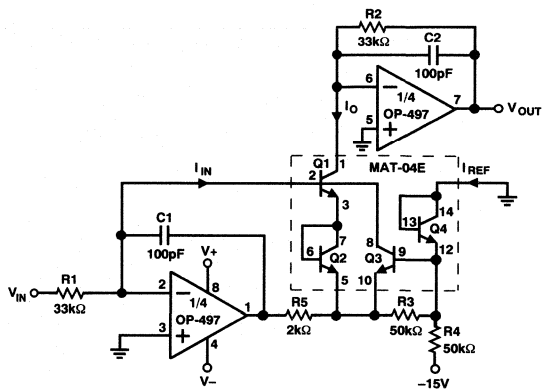


Figure 37. Square Root Amplifier

Unadjusted accuracy of the square-root circuit is better than 0.1% over an input voltage range of 100 mV to 10 V. For a similar input voltage range, the accuracy of the squaring circuit is better than 0.5%.

OP-497 SPICE MACRO-MODEL

Figure 38 and Table I show the node and net list for a SPICE macro-model of the OP-497. The model is a simplified version of the actual device and simulates important dc parameters such as V_{OS}, I_{OS}, I_B, A_{VO}, CMR, V_O and I_{SY}. AC parameters such as slew rate, gain and phase response and CMR change with frequency are also simulated by the model.

The model uses typical parameters for the OP-497. The poles and zeros in the model were determined from the actual open and closed-loop gain and phase response of the OP-497. In this way, the model presents an accurate ac representation of the actual device. The model assumes an ambient temperature of 25°C.

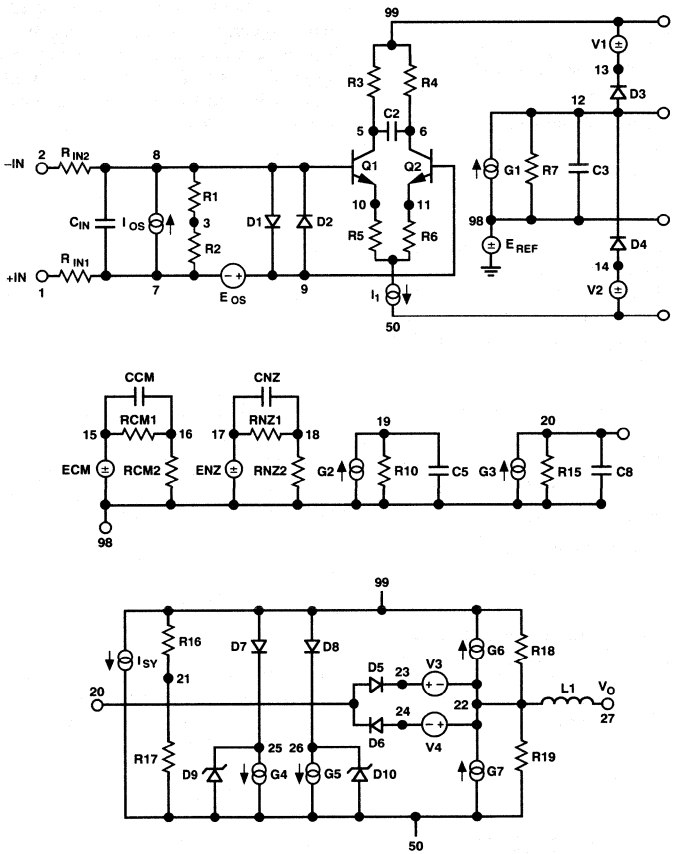


Figure 38. OP-497 Macro-Model

Table I. OP-497 SPICE Net-List

```
*NODE ASSIGNMENTS
*                          NONINVERTING INPUT
*                             INVERTING INPUT
*                                POSITIVE SUPPLY
*                                     NEGATIVE SUPPLY
*                                          OUTPUT
*
*
*SUBCKT OP-497          1   2   99   50   27
*
*INPUT STAGE & POLE AT 6 MHz
*
RIN1     1    7    2500
RIN2     2    8    2500
R1       8    3    6.782E8
R2       7    3    6.782E8
R3       5    99   542.57
R4       6    99   542.57
CIN      7    8    3E-12
C2       5    6    24.445E-12
I1       4    50   0.1E-3
IOS      7    8    15E-12
EOS      9    7    POLY(1)        16    21    40E-6    1
Q1       5    8    10        QX
Q2       6    9    11        QX
R5       10   4    25.374
R6       11   4    25.374
D1       8    9    DX
D2       9    8    DX
*
EREF     98   0    21        0     1
*
*GAIN STAGE & DOMINANT POLE AT 0.11 Hz
*
R7       12   98   2.1703E9
C3       12   98   666.67E-12
G1       98   12   5         6     1.8431E-3
V1       99   13   1.275
V2       14   50   1.275
D3       12   13   DX
D4       14   12   DX
*
*COMMON-MODE GAIN NETWORK WITH ZERO AT 50 Hz
*
RCM1     15   16   1E6
CCM      15   16   3.183E-9
RCM2     16   98   1
ECM      15   98   3         21    177.83E-3
*
*NEGATIVE ZERO AT 1.8 MHz
*
E1       17   98   12        21    1E6
R8       17   18   1E6
C4       17   18   -88.419E-15
R9       18   98   1
*
*POLE AT 6 MHz
*
G2       98   19   18        21    1E-6
R10      19   98   1E6
C5       19   98   26.526E-15
*
*POLE AT 1.8 MHz
*
G3       98   20   19        21    1E-6
R15      20   98   1E6
C8       20   98   88.419E-15
*
*OUTPUT STAGE
*
R16      99   21   160k
R17      21   50   160k
ISY      99   50   331E-6
V3       23   22   1.9
D5       20   23   DX
V4       22   24   1.9
D6       24   20   DX
D7       99   25   DX
G4       25   50   20        22    5E-3
D9       50   25   DY
D8       99   26   DX
G5       26   50   22        20    5E-3
D10      50   26   DY
G6       22   99   99        20    5E-3
R18      99   22   200
G7       50   22   20        50    5E-3
R19      22   50   200
L1       22   27   0.1E-6
*
*MODELS USED
*
.MODEL QX NPN (BF = 1.25E6)
.MODEL DX D (IS = 1E-15)
.MODEL DY D (IS = 1E-15 BV = 50)
.ENDS OP-497
```

ANALOG DEVICES

Low-Input-Current Operational Amplifiers

PM-108/PM-208/PM-308

FEATURES

- **Low Offset Current** ..... **200pA Max**
- **Low Bias Current** ..... **2nA Max**
- **Low Power Consumption** ..... **18mW Max @ ±15V**
- **Wide Supply Range** ..... **±3V to ±20V**
- **High Power-Supply Rejection Ratio** ..... **96dB Min**
- **Low Offset Voltage Drift** ..... **5μV/°C Max**
- **High Common-Mode Input Range** ..... **±13.5V Min**
- **High Common-Mode Rejection Ratio** ..... **96dB Min**
- **MIL-STD-883 Processing Models Available**
- **Silicon-Nitride Passivation**

GENERAL DESCRIPTION

The PM-108A series of precision operational amplifiers feature very low input offset and bias currents. Although directly interchangeable with industry-standard types, Precision Monolithics' advanced processing provides the PM-108A series with a significant improvement in input noise voltage. Low supply current drain over a wide power-supply range makes the PM-108A attractive in battery operated and other low-power applications. The low bias current provides excellent performance with piezoelectric and capacitive transducers and in such high-impedance circuits as long-period intergrators and sample-and-holds. For improved performance see OP-08, OP-12, OP-20, OP-21, OP-22, and PM-1008.

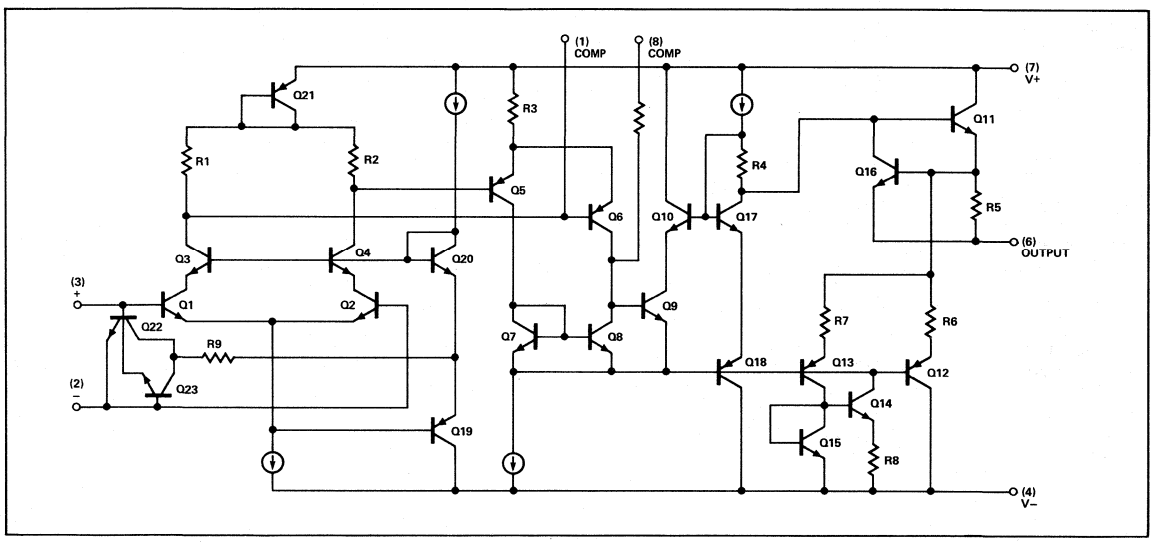
ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (mV)	PACKAGE				OPERATING TEMPERATURE RANGE
	TO-99	CERDIP 8-PIN	LCC 20-CONTACT	PLASTIC 8-PIN	
0.5	PM108AJ/883	PM108AZ*	PM108ARC/883	—	MIL
0.5	PM308AJ	—	—	PM308AP	COM
2.0	PM108J/883	PM108Z*	—	—	MIL
2.0	PM208J	PM208Z	—	—	IND
7.5	—	PM308Z	—	—	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 3)

Supply Voltage
- PM-108A, PM-108, PM-208, PM-108ARC ..... ±20V
- PM-308A, PM-308 ..... ±18V

Differential Input Current (Note 2) ..... ±10mA
Input Voltage (Note 3) ..... ±15V
Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range
- PM-108A, PM-108, PM-108ARC ..... −55°C to +125°C
- PM-208 ..... −25°C to +85°C
- PM-308A, PM-308 ..... 0°C to +70°C

Storage Temperature Range
- (Q-, J-, Z- or ARC-Package) ..... −65°C to +150°C
- (P-Package) ..... −65°C to +125°C

Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC (RC)	98	38	°C/W

NOTES:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages.
2. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, if a differential input voltage in excess of 1V is applied between the inputs, excessive current will flow, unless some limiting resistance is provided.
3. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS at $\pm5V \le V_S \le \pm20V$ and $T_A = 25°C$, unless otherwise noted.

			PM-108A			PM-108 PM-208			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.3	0.5	—	0.7	2.0	mV
Input Offset Current	I_{OS}		—	0.05	0.2	—	0.05	0.2	nA
Input Bias Current	I_B		—	0.8	2.0	—	0.8	2.0	nA
Input Resistance	R_{IN}	(Note 1)	30	70	—	30	70	—	MΩ
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm15V$, $V_{OUT} = \pm10V$, $R_L \ge 10k\Omega$	80	300	—	50	300	—	V/mV
Supply Current	I_{SY}	$I_{OUT} = 0$, $V_{OUT} = 0$, Each Amplifier	—	0.3	0.6	—	0.3	0.6	mA

ELECTRICAL CHARACTERISTICS at $\pm5V \le V_S \le \pm20V$, $-55°C \le T_A \le +125°C$ for PM-108A, PM-108, $-25°C \le T_A \le +85°C$ for PM-208, unless otherwise noted.

			PM-108A			PM-108 PM-208			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.4	1.0	—	1.0	3.0	mV
Average Input Offset Voltage Drift	TCV_{OS}	(Note 2)	—	1	5	—	3	15	µV/°C
Input Offset Current	I_{OS}		—	0.1	0.4	—	0.1	0.4	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	0.5	2.5	—	0.5	2.5	pA/°C
Input Bias Current	I_B		—	1	3	—	1	3	nA
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm15V$, $V_{OUT} = \pm10V$, $R_L \ge 10k\Omega$	40	200	—	25	200	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm15V$, $R_L = 10k\Omega$	±13	±14	—	±13	±14	—	V
Input Voltage Range	IVR	$V_S = \pm15V$	±13.5	—	—	±13.5	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_S = \pm15V$, $V_{CM} = \pm13.5V$	96	110	—	85	100	—	dB
Power-Supply Rejection Ratio	PSRR	$V_S = \pm5V$ to $\pm20V$	—	3	15	—	15	100	µV/V
Supply Current	I_{SY}	$V_{OUT} = 0$, T_A = MAX, Each Amplifier	—	0.15	0.4	—	0.15	0.4	mA

NOTES:
1. Guaranteed by input bias current.
2. Sample tested.

ELECTRICAL CHARACTERISTICS at $\pm 5V \le V_S \le \pm 15V$ and $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-308A MIN	PM-308A TYP	PM-308A MAX	PM-308 MIN	PM-308 TYP	PM-308 MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.3	0.5	—	2.0	7.5	mV
Input Offset Current	I_{OS}		—	0.2	1.0	—	0.2	1.0	nA
Input Bias Current	I_B		—	1.5	7.0	—	1.5	7.0	nA
Input Resistance	R_{IN}	(Note 1)	10	40	—	10	40	—	MΩ
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \ge 10k\Omega$	80	300	—	25	300	—	V/mV
Supply Current	I_{SY}	$I_{OUT} = 0$, $V_{OUT} = 0$, Each Amplifier	—	0.3	0.8	—	0.3	0.8	mA

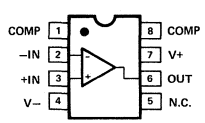
2

ELECTRICAL CHARACTERISTICS at $\pm 5V \le V_S \le \pm 15V$ and $0°C \le T_A \le +70°C$, unless otherwise noted.

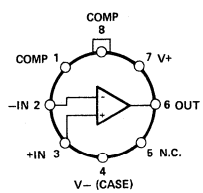
PARAMETER	SYMBOL	CONDITIONS	PM-308A MIN	PM-308A TYP	PM-308A MAX	PM-308 MIN	PM-308 TYP	PM-308 MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.4	0.73	—	3.0	10.0	mV
Average Input Offset Voltage Drift	TCV_{OS}	(Note 1)	—	1	5	—	6	30	μV/°C
Input Offset Current	I_{OS}		—	0.3	1.5	—	0.3	1.5	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 1)	—	2	10	—	2	10	pA/°C
Input Bias Current	I_B		—	2	10	—	2	10	nA
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \ge 10k\Omega$	60	200	—	15	100	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm 15V$, $R_L = 10k\Omega$	±13	±14	—	±13	±14	—	V
Input Voltage Range	IVR	$V_S = \pm 15V$	±14	—	—	±13	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$	96	110	—	80	100	—	dB
Power-Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	—	3	15	—	15	100	μV/V
Supply Current	I_{SY}	$V_{OUT} = 0$, T_A = MAX, Each Amplifier	—	0.23	—	—	0.23	—	mA

NOTE:
1. Guaranteed by input bias current.

PIN CONNECTIONS

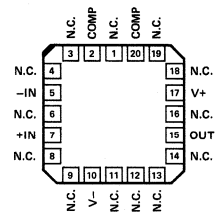


EPOXY MINI-DIP
(P-Suffix)
AND
8-PIN HERMETIC DIP
(Z-Suffix)



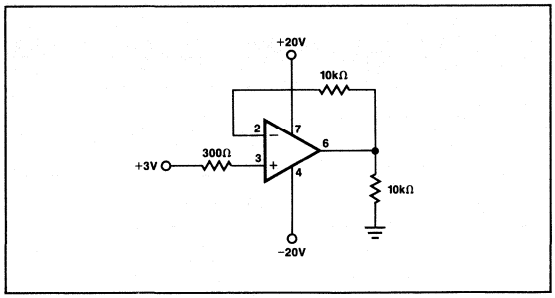
TO-99
(J-Suffix)

PM-108ARC/883



LCC PACKAGE
(RC-Suffix)

BURN-IN CIRCUIT

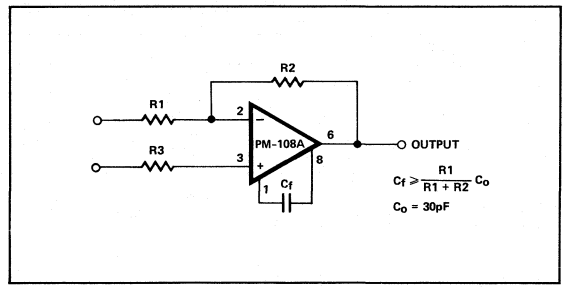


APPLICATIONS INFORMATION

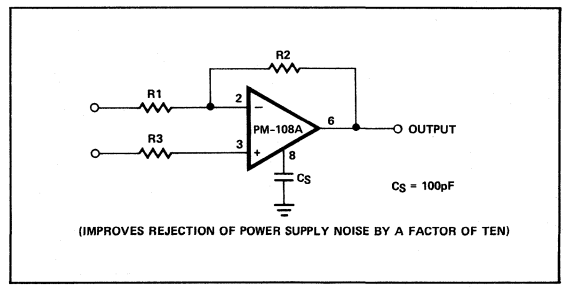
The PM-108A series has very low input offset and bias currents; the user is cautioned that printed circuit board leakages can produce significant errors, especially at high board temperatures. Careful attention to board layout and cleaning procedure is required to achieve the PM-108A's rated performance. It is suggested that board leakage be minimized by encircling the input pins with a guard ring maintained at a potential close to that of the inputs. The guard ring should be driven by a low impedance source such as an amplifier's output or ground.

COMPENSATION CIRCUITS

STANDARD



ALTERNATE



ANALOG DEVICES

Monolithic JFET-Input Operational Amplifiers

PM-155A/PM-156A/PM-157A

FEATURES

All Devices

- Low Input Bias and Offset Currents
- Low Input Offset Voltage 1.0mV
- Low Input Offset Voltage Drift ..... 3.0μV/°C
- Low Input Noise Current ..... 0.01pA/√Hz
- High Common-Mode Rejection Ratio 100dB

PM-155 (Only) ..... **LF155 Replacement**

- Low Supply Current 2mA

PM-156 (Only) ..... **LF156 Replacement**

- High Slew Rate 12V/μsec
- Fast Settling to ±0.01% 4.0μsec

PM-157 (Only) ..... **LF157 Replacement**

- Wide-Bandwidth Decompensated (A_{VCL} = 5 Min)...20MHz
- High Slew Rate 45V/μsec
- Fast Settling to ±0.01% 4.0μsec

GENERAL DESCRIPTION

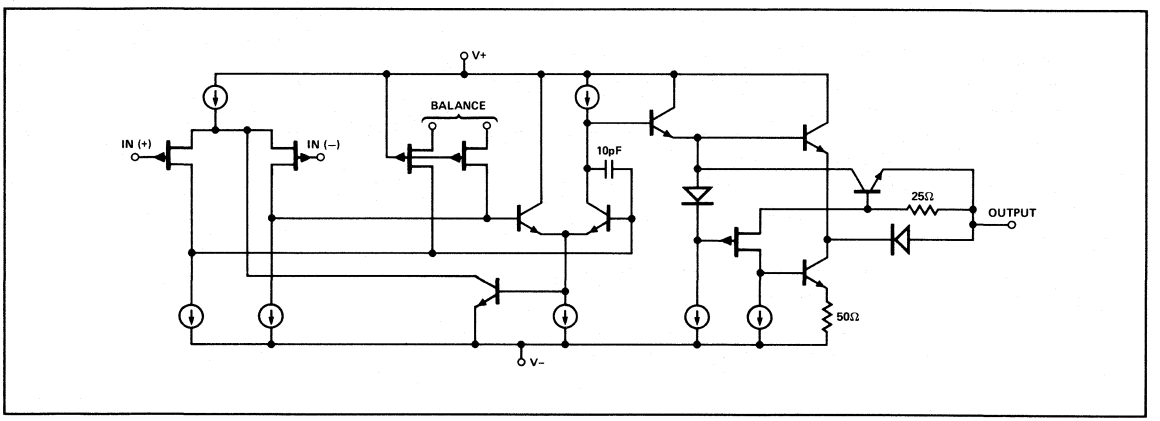
The PM JFET-input series provides low input current, high slew rate, and direct interchangeability with LF155, 156, and 157 types. These operational amplifiers use a new process which allows fabrication of matched JFET transistors and standard bipolar transistors on the same chip. High accuracy and low cost make the PM JFET-input series useful in new designs and as replacements for modular and hybrid types. Unlike many designs, nulling the input offset voltage does not degrade common-mode rejection ratio or input offset voltage drift. Low input voltage noise and current noise plus a low 1/f noise corner frequency allow these amplifiers to be used in a variety of low noise, wide-bandwidth applications.

Dynamic specifications for the PM-155 include a slew rate of 5V/μs, a 2.5MHz gain bandwidth product, and settling time to within ±0.01% of final value in 5.0μs. The PM-156 has a slew rate of 12V/μs and a settling time of 4.0μs to ±0.01% of final value.

The PM-157 is a very fast decompensated device. This results in a 45V/μs slew rate, a 20MHz gain bandwidth product, and a settling time of 4.0μs. Decompensation requires a minimum closed-loop gain of five because of stability considerations.

For improved performance, see the OP-15/OP-16/OP-17 data sheet. For duals, see the OP-215 data sheet.

SIMPLIFIED SCHEMATIC



PM-155A/PM-156A/PM-157A

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
PM-155A, PM-156A, PM-157A, PM-155, PM-156, PM-157, PM-355A, PM-356A, PM-357A ..... ±22V
Operating Temperature Range
PM-155A, PM-156A, PM-157A, PM-155, PM-156, PM-157 ..... −55°C to +125°C
PM-355A, PM-356A, PM-357A ..... 0°C to +70°C
Maximum Junction Temperature (T_j)
PM-155A, PM-156A, PM-157A, PM-155, PM-156, PM-157 ..... +150°C
PM-355A, PM-356A, PM-357A ..... +100°C
Differential Input Voltage
PM-155A, PM-156A, PM-157A, PM-155, PM-156, PM-157, PM-355A, PM-356A, PM-357A ..... ±40V
Input Voltage
PM-155A, PM-156A, PM-157A, PM-155, PM-156, PM-157, PM-355A, PM-356A, PM-357A ..... ±20V

Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) .... +300°C

PACKAGE TYPE	Θ_{JA} (NOTE 2)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
20-Contact LCC (RC)	98	38	°C/W

NOTES:
1. The absolute maximum negative input voltage is equal to the negative power supply voltage.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP, and LCC packages.

ELECTRICAL CHARACTERISTICS

at ±15V ≤ V_S ≤ ±20V, −55°C ≤ T_A ≤ +125°C and T_{HIGH} = +125°C for PM-155A, PM-156A and PM-157A, 0°C ≤ T_A ≤ +70°C and T_{HIGH} = +70°C for PM-355A, PM-356A and PM-357A, unless otherwise noted.

			PM-155A/ PM-156A/ PM-157A			PM-355A/ PM-356A/ PM-357A			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	R_S = 50Ω	—	1.4	2.5	—	1.2	2.3	mV
Input Offset Voltage Drift	TCV_{OS}	R_S = 50Ω	—	3	5	—	3	5	µV/°C
Change in Input Offset Drift with V_{OS} Adjust	$\left(\frac{\Delta TCV_{OS}}{\Delta V_{OS}}\right)$	R_S = 50Ω	—	0.5	—	—	0.5	—	µV/°C per mV
Input Offset Current	I_{OS}	$T_j \leq T_{HIGH}$ (Note 1)	—	4.0	10	—	0.4	1.0	nA
Input Bias Current	I_B	$T_j \leq T_{HIGH}$ (Note 1)	—	±10	±25	—	±2	±5	nA
Large-Signal Voltage Gain	A_{VO}	V_S = ±15V, V_O = ±10V, R_L = 2kΩ	25	75	—	25	75	—	V/mV
Output Voltage Swing	V_O	V_S = ±15V, R_L = 10kΩ V_S = ±15V, R_L = 2kΩ	±12 ±10	±13 ±12	— —	±12 ±10	±13 ±12	— —	V
Input Voltage Range	IVR	V_S = ±15V	±10.4	+15.1 −12.0	—	±10.4	+15.1 −12.0	—	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±IVR	85	100	—	85	100	—	dB
Power Supply Rejection Ratio	PSRR	(Note 2)	—	10	57	—	10	57	µV/V

NOTES:
1. PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at V_{CM} = 0.
2. Power supply rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

ELECTRICAL CHARACTERISTICS at $\pm 15V \leq V_S \leq \pm 20V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		PM-155A/ PM-156A/ PM-157A MIN	TYP	MAX	PM-355A/ PM-356A/ PM-357A MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$		—	1	2	—	1	2	mV
Input Offset Current	I_{OS}	$T_j = 25°C$ (Note 1)		—	3	10	—	3	10	pA
Input Bias Current	I_B	$T_j = 25°C$ (Note 1)		—	±30	±50	—	±30	±50	pA
Input Resistance	R_{IN}			—	10^{12}	—	—	10^{12}	—	Ω
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 2k\Omega$		50	200	—	50	200	—	V/mV
Supply Current	I_{SY}	$V_S = \pm 15V$	PM-155	—	2	4	—	2	4	mA
			PM-156/PM-157	—	5	7	—	5	7	
Slew Rate	SR	$A_{VCL} = +1$, $V_S = \pm 15V$	PM-155	3	5	—	3	5	—	V/μs
			PM-156	10	12	—	10	12	—	
		$A_{VCL} = +5$, $V_S = \pm 15V$	PM-157	40	45	—	40	45	—	
Gain Bandwidth Product	GBW	$A_{VCL} = +1$, $V_S = \pm 15V$	PM-155	—	2.5	—	—	2.5	—	MHz
			PM-156	4.0	4.5	—	4.0	4.5	—	
		$A_{VCL} = +5$, $V_S = \pm 15V$	PM-157	15	20	—	15	20	—	
Settling Time (to ±0.01%)	t_S	$V_S = \pm 15V$ (Note 2)	PM-155	—	5.0	—	—	4.0	—	μs
			PM-156	—	4.0	—	—	1.5	—	
		$V_S = \pm 15V$ (Note 3)	PM-157	—	4.0	—	—	1.5	—	
Input Noise Voltage	e_n	$R_S = 100\Omega$, f = 100Hz	PM-155	—	25	—	—	25	—	$nV/\sqrt{Hz}$
		$R_S = 100\Omega$, f = 1000Hz		—	20	—	—	20	—	
		$R_S = 100\Omega$, f = 100Hz	PM-156/PM-157	—	15	—	—	15	—	
		$R_S = 100\Omega$, f = 1000Hz		—	12	—	—	12	—	
Input Noise Current	i_n	f = 100Hz, $V_S = \pm 15V$		—	0.01	—	—	0.01	—	$pA/\sqrt{Hz}$
		f = 1000Hz, $V_S = \pm 15V$		—	0.01	—	—	0.01	—	
Input Capacitance	C_{IN}			—	3	—	—	3	—	pF

NOTES:

1. PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
2. Settling time is defined here for a unity gain inverter connection using 2kΩ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. See settling time test circuit.
3. Settling time is defined here for a $A_V = -5$ connection with $R_F = 2k\Omega$. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 2V step input is applied to the inverter. See settling time test circuit.

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $\pm 15V \leq V_S \leq \pm 20V$ for PM-155, PM-156 and PM-157, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		PM-155 PM-156 PM-157 MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$		—	3	5	mV
Input Offset Current	I_{OS}	$T_j = 25°C$ (Note 1)		—	3	20	pA
Input Bias Current	I_B	$T_j = 25°C$ (Note 1)		—	±30	±100	pA
Input Resistance	R_{IN}			—	10^{12}	—	Ω
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 2k\Omega$		50	200	—	V/mV
Supply Current	I_{SY}	$V_S = \pm 15V$	PM-155	—	2	4	mA
			PM-156/PM-157	—	5	7	
Slew Rate	SR	$A_{VCL} = +1$, $V_S = \pm 15V$	PM-155	—	5	—	V/μs
			PM-156	7.5	12	—	
		$A_{VCL} = +5$, $V_S = \pm 15V$	PM-157	30	40	—	
Gain Bandwidth Product	GBW	$A_{VCL} = +1$, $V_S = \pm 15V$	PM-155	—	2.5	—	MHz
			PM-156	—	5	—	
		$A_{VCL} = +5$, $V_S = \pm 15V$	PM-157	—	20	—	
Settling Time (to ±0.01%)	t_S	$V_S = \pm 15V$ (Note 2)	PM-155	—	5	—	μs
			PM-156	—	4	—	
		$V_S = \pm 15V$ (Note 3)	PM-157	—	4	—	
Input Noise Voltage	e_n	$R_S = 100\Omega$, f = 100Hz	PM-155	—	25	—	$nV/\sqrt{Hz}$
		$R_S = 100\Omega$, f = 1000Hz		—	20	—	
		$R_S = 100\Omega$, f = 100Hz	PM-156/PM-157	—	15	—	
		$R_S = 100\Omega$, f = 1000Hz		—	12	—	
Input Noise Current	i_n	f = 100Hz, $V_S = \pm 15V$		—	0.01	—	$pA/\sqrt{Hz}$
		f = 1000Hz, $V_S = \pm 15V$					
Input Capacitance	C_{IN}			—	3	—	pF

NOTES:

1. PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
2. Settling time is defined here for a unity gain inverter connection using 2kΩ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. See settling time test circuit.
3. Settling time is defined here for a $A_V = -5$ connection with $R_F = 2k\Omega$. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 2V step input is applied to the inverter. See settling time test circuit.

ELECTRICAL CHARACTERISTICS at $\pm 15V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq +125°C$ and $T_{HIGH} = +125°C$ for PM-155, PM-156 and PM-157, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-155 PM-156 PM-157 MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	4	7	mV
Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	—	5	—	µV/°C
Change In Input Offset Drift With V_{OS} Adjust.	$\left(\frac{\Delta TCV_{OS}}{\Delta V_{OS}}\right)$	$R_S = 50\Omega$	—	0.5	—	µV/°C per mV
Input Offset Current	I_{OS}	$T_j \leq T_{HIGH}$ (Note 1)	—	8	20	nA
Input Bias Current	I_B	$T_j \leq T_{HIGH}$ (Note 1)	—	±2	±50	nA
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_O = \pm 10V$ $R_L = 2k\Omega$	25	75	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm 15V$, $R_L = 10k\Omega$ $V_S = \pm 15V$, $R_L = 2k\Omega$	±12 ±10	±13 ±12	— —	V
Input Voltage Range	IVR	$V_S = \pm 15V$	±10.4	+15.1 −12.0	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm IVR$	85	100	—	dB
Power Supply Rejection Ratio	PSRR	(Note 2)	—	10	57	µV/V

NOTES:

1. PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$, $T_j = +125°C$.
2. Power supply rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

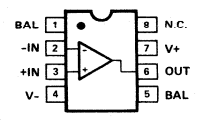
ORDERING INFORMATION†

$T_A = 25°C$ V_{OS} MAX (mV)	PACKAGE TO-99 8-PIN	8-PIN HERMETIC DIP	LCC	OPERATING TEMPERATURE RANGE
2.0	PM155AJ*	PM155AZ/883	PM155ARC/883	MIL
	PM156AJ*	PM156AZ*	PM156ARC/883	
	PM157AJ/883	PM157AZ*	—	
2.0	PM355AJ	PM355AZ	—	COM
	PM356AJ	PM356AZ	—	
	PM357AJ	PM357AZ	—	
5.0	PM155J*	PM155Z*	—	MIL
	PM156J*	PM156Z*	—	
	PM157J*	PM157Z*	—	

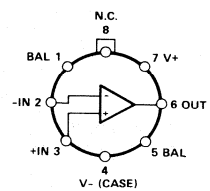
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

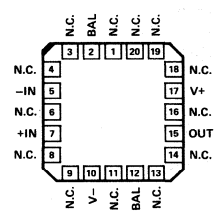
PIN CONNECTIONS



8-PIN HERMETIC DIP (Z-Suffix)



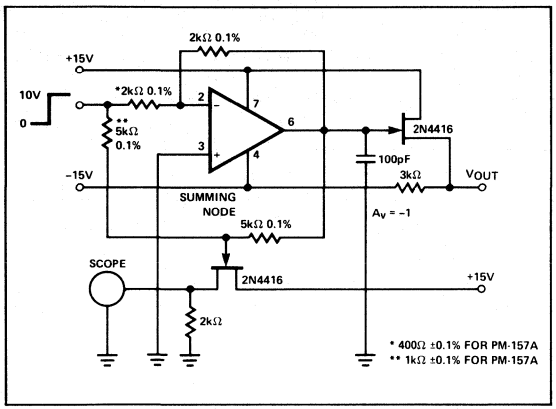
TO-99 (J-Suffix)



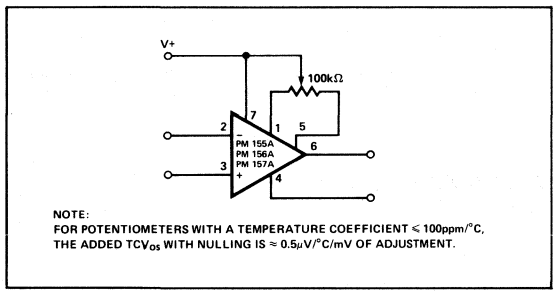
PM-155ARC/883, PM-156ARC/883 20-LEAD LCC (RC-Suffix)

BASIC CONNECTIONS

SETTLING-TIME TEST CIRCUIT

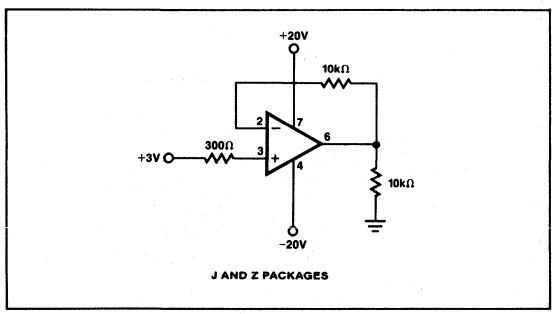


INPUT OFFSET VOLTAGE NULLING



NOTE:
FOR POTENTIOMETERS WITH A TEMPERATURE COEFFICIENT ≤ 100ppm/°C, THE ADDED TCV_{OS} WITH NULLING IS ≈ 0.5μV/°C/mV OF ADJUSTMENT.

BURN-IN CIRCUIT



J AND Z PACKAGES

APPLICATIONS INFORMATION

INPUT VOLTAGE CONSIDERATIONS

The PM series JFET input stages can accommodate large input differential voltages without external clamping as long as neither input exceeds the negative power supply. An input voltage which is more negative than V− can result in a destroyed unit.

If both inputs exceed the negative common-mode voltage limit, the amplifier will be forced to a high positive output. If only one input exceeds the negative common-mode voltage limit, a phase reversal takes place forcing the output to the corresponding high or low state. In either of the above conditions, normal operation will return when both inputs are returned to within the specified common-mode voltage range.

Exceeding the positive common-mode limit on a single input will not change the phase of the output. However, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

POWER SUPPLY CONSIDERATIONS

Power supply polarity reversal can result in a destroyed unit.

DYNAMIC OPERATING CONSIDERATIONS

As with most amplifiers, care should be taken with lead dress, component placement, and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input. This minimizes "pick-up" and increases the frequency of the feedback pole by minimizing the capacitance from input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device to AC ground sets the frequency of the pole. In many instances, the frequency of this pole is much greater than the expected 3dB frequency of the closed-loop gain. Consequently, the pole has negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3dB frequency, a lead capacitor should be placed from the output to the inverting input of the op amp. The capacitor value should be such that the RC time constant of the capacitor and feedback resistor is greater than, or equal to, the original feedback-pole time constant.

ANALOG DEVICES

Low-Power Precision Operational Amplifier

PM-1012

FEATURES

- **Low Supply Current** ..... **600μA Max**
- **Very Low Offset** ..... **35μV Max**
- **Low Drift** ..... **1.5μV/°C Max**
- **Very Low Bias Current**
  - **25°C** ..... **100pA Max**
  - **−55°C to +125°C** ..... **250pA Max**
- **Low Noise** ..... **0.5μV_{p-p} Typ**
- **High Common-Mode Rejection** ..... **114dB Min**
- **Available in Die Form**

ORDERING INFORMATION †

V_{OS} (μV)	PACKAGE TO-99	PACKAGE CERDIP 8-PIN	PACKAGE PLASTIC 8-PIN	OPERATING TEMPERATURE RANGE
35	PM1012AJ*	PM1012AZ*	–	MIL
50	PM1012GJ	PM1012GZ	–	COM
50	–	–	PM1012GP	XIND
50	–	–	PM1012GS	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

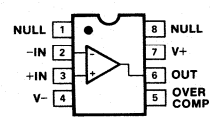
† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

The PM-1012 is a general-purpose, precision operational amplifier. Offering several performance enhancements over industry-standard precision op amps such as the OP-07, the PM-1012 requires less than 1/6 the supply current. These enhancements include exceptionally low bias currents of only ±80pA, typical, over the full military temperature range and 132dB of common-mode rejection and power-supply rejection. The PM-1012's low offset voltage of 35μV maximum frees the user from external nulling in most circuits.

An open-loop gain of two million into a 10kΩ load ensures that excellent linearity is maintained even in high-gain configurations, and 5mA of output current allows 2kΩ loads to be driven

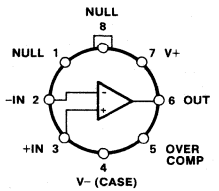
PIN CONNECTIONS



EPOXY MINI-DIP
(P-Suffix)

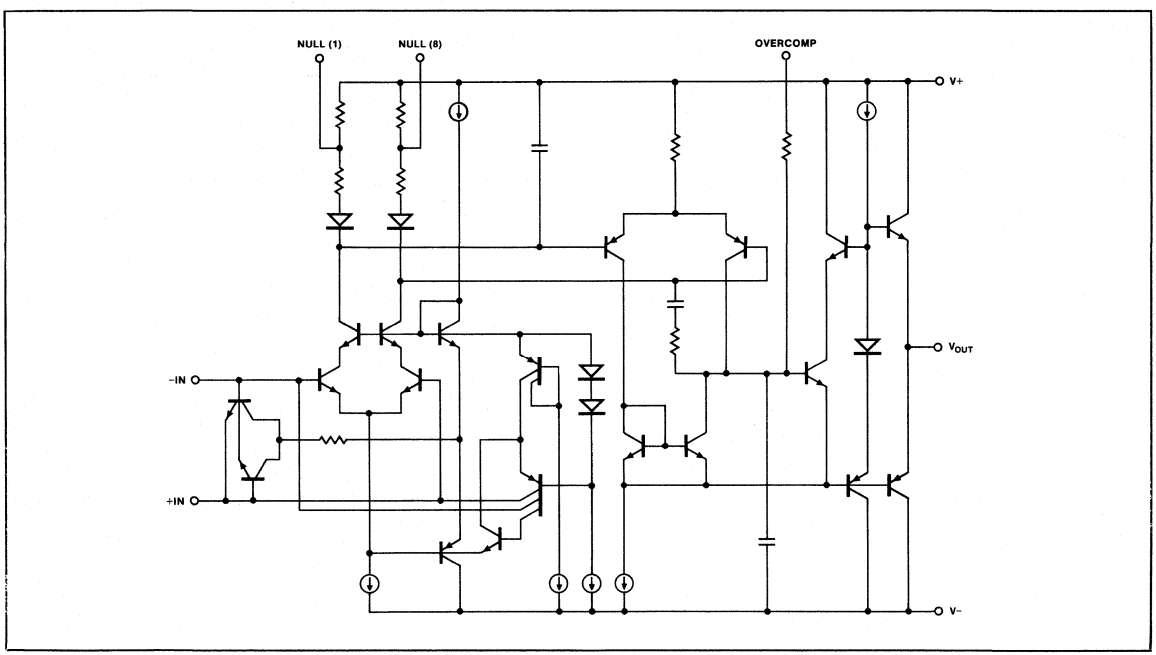
8-PIN HERMETIC DIP
(Z-Suffix)

EPOXY SO
(S-Suffix)



TO-99
(J-Suffix)

SIMPLIFIED SCHEMATIC



with an open-loop gain of one million. The PM-1012 offers low noise, especially for a low-power amplifier — only 17nV/$\sqrt{Hz}$ at 10Hz. Exceptionally low current-noise minimizes noise contributions when high source impedances are used. The PM-1012 may be overcompensated using pin 5 to limit the amplifier's bandwidth, further reducing system noise and increasing stability with large capacitive loads.

The PM-1012 conforms to the OP-07 pinout with nulling through pins 1 and 8 to the positive supply. It offers an upgrade to the OP-07 in sockets where reduced power dissipation or low bias currents are attractive. It may also be used as an upgrade from the OP-12, OP-05 and 725 type op amps. The PM-1012 may replace 741 type op amps by removing the nulling potentiometer, if used. For an externally compensated amplifier sharing many of the PM-1012's precision specifications, see the PM-1008 data sheet.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±20V
Input Voltage (Note 3) ..... ±20V
Differential Input Voltage (Note 4) ..... ±1V
Differential Input Current (Note 4) ..... ±10mA
Output Short-Circuit Duration ..... Indefinite

Operating Temperature Range
PM-1012A (J,Z) ..... −55°C to +125°C
PM-1012G (J,Z) ..... 0°C to +70°C
PM-1012G (P,S) ..... −40°C to +85°C
Storage Temperature Range ..... −65° to +150°C
Junction Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

PACKAGE TYPE	Θ_{jA} (Note 2)	Θ_{jC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket for TO, CerDIP and P-DIP packages; Θ_{jA} is specified for device soldered to printed circuit board for SO package.
3. For supply voltages less than ±20V, the absolute maximum input voltage is equal to the supply voltage.
4. The PM-1012's inputs are protected by back-to-back diodes. Current- limiting resistors are not used in order to achieve low noise. Differential input voltages greater than 1V will cause excessive current to flow through the input protection diodes unless limiting resistance is used.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25°C$ unless otherwise noted.

			PM-1012A			PM-1012G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	8	35	—	10	50	µV
		(Note 1)	—	20	90	—	25	120	
Long-Term V_{OS} Stability	ΔV_{OS}/Time		—	0.3	—	—	0.3	—	µV/month
Input Offset Current	I_{OS}		—	15	100	—	20	150	pA
		(Note 1)	—	25	150	—	30	200	
Input Bias Current	I_B		—	±25	±100	—	±30	±150	pA
		(Note 1)	—	±35	±150	—	±40	±200	
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.5	—	—	0.5	—	μV_{p-p}
Input Noise Voltage Density	e_n	f_O = 10Hz (Note 3)	—	17	30	—	17	30	nV/$\sqrt{Hz}$
		f_O = 1000Hz (Note 4)	—	14	22	—	14	22	
Input Noise Current Density	i_N	f_O = 10Hz	—	20	—	—	20	—	fA/$\sqrt{Hz}$
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 12V$; $R_L = 10k\Omega$	300	2000	—	200	2000	—	V/mV
		$V_O = \pm 10V$; $R_L = 2k\Omega$	200	1000	—	120	1000	—	
Common-Mode Rejection	CMR	$V_{CM} = \pm 13.5V$	114	132	—	110	132	—	dB
Power-Supply Rejection	PSR	$V_S = \pm 2V$ to $\pm 20V$	114	132	—	110	132	—	dB
Input Voltage Range	IVR	(Note 2)	±13.5	±14.0	—	±13.5	±14.0	—	V
Output Voltage Swing	V_O	$R_L = 10k\Omega$	±13	±14	—	±13	±14	—	V
Slew Rate	SR		0.1	0.2	—	0.1	0.2	—	V/µs
Full-Power Bandwidth	BW_P		—	3	—	—	3	—	kHz
Gain-Bandwidth Product	GBW	$A_V = 100$	—	0.5	—	—	0.5	—	MHz
Supply Current	I_{SY}	(Note 1)	—	380	600	—	380	600	µA
Supply Voltage	V_S	Operating Range	±2	±15	±20	±2	±15	±20	V

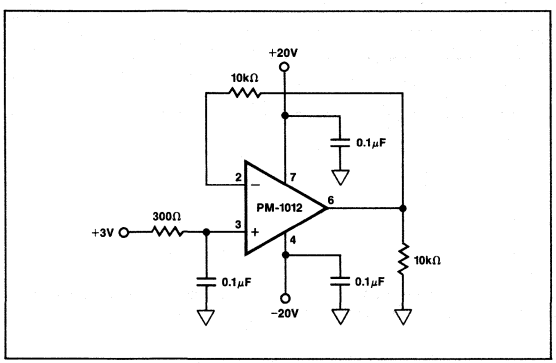
NOTES:
1. These specifications apply for $\pm 2V \le V_S \le \pm 20V$ and $-13.5V \le V_{CM} \le +13.5V$ (for $V_S = \pm 15V$).
2. Guaranteed by CMR test.
3. 10Hz noise voltage density is sample tested. Devices 100% tested for noise are available on request.
4. Sample Tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $V_{CM} = 0V$, $0°C \leq T_A \leq +70°C$ for PM-1012 GJ and GZ, $-40°C \leq T_A \leq +85°C$ for PM1012GP, GS and $-55° C \leq T_A \leq +125°C$ for PM-1012A, unless otherwise noted.

			PM-1012A			PM-1012G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}		—	30	180	—	20	120	μV
		(Note 1)	—	40	250	—	30	200	
Average Temperature Coefficient of V_{OS}	TCV_{OS}		—	0.2	1.5	—	0.2	1.5	$\mu V/°C$
Input Offset Current	I_{OS}		—	30	250	—	20	230	pA
		(Note 1)	—	70	350	—	40	300	
Average Temperature Coefficient of I_{OS}	TCI_{OS}		—	0.3	2.5	—	0.3	2.5	pA/°C
Input Bias Current	I_B		—	±50	±250	—	±35	±230	pA
		(Note 1)	—	±80	±350	—	±50	±300	
Average Temperature Coefficient of I_B	TCI_B		—	0.3	2.5	—	0.3	2.5	pA/°C
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 12V$; $R_L = 10k\Omega$	150	1000	—	150	1500	—	V/mV
		$V_O = \pm 10V$; $R_L = 2k\Omega$	100	600	—	100	800	—	
Common-Mode Rejection	CMR	$V_{CM} = \pm 13.5V$	108	128	—	108	130	—	dB
Power-Supply Rejection	PSR	$V_S = \pm 2.5V$ to $\pm 20V$	108	126	—	108	128	—	dB
Input Voltage Range	IVR	(Note 2)	±13.5	±14.0	—	±13.5	±14.0	—	V
Output Voltage Swing	V_O	$R_L = 10k\Omega$	±13	±14	—	±13	±14	—	V
Slew Rate	SR		0.05	0.15	—	0.05	0.15	—	$V/\mu s$
Supply Current	I_{SY}	(Note 1)	—	400	800	—	400	800	μA
Supply Voltage	V_S	Operating Range	±2.5	±15	±20	±2.5	±15	±20	V

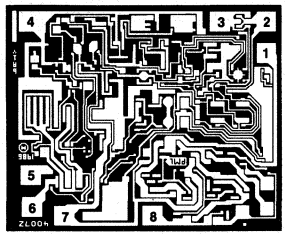
NOTES:
1. These specifications apply for $\pm 2.5V \leq V_S \leq \pm 20V$ and $-13.5V \leq V_{CM} \leq +13.5V$ (for $V_S = \pm 15V$).
2. Guaranteed by CMR test.

BURN-IN CIRCUIT



PM-1012

DICE CHARACTERISTICS



DIE SIZE 0.063 × 0.074 inch, 4662 sq. mils
(1.60 × 1.88 mm, 3.01 sq. mm)

1. NULL
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V–
5. OVERCOMPENSATION
6. OUTPUT
7. V+
8. NULL

WAFER TEST LIMITS at $V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25°C$, unless otherwise noted.

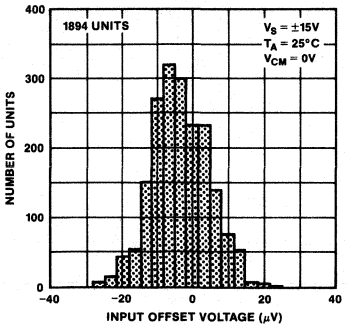
PARAMETER	SYMBOL	CONDITIONS	PM-1012N LIMIT	UNITS
Input Offset Voltage	V_{OS}	(Note 1) (Note 2)	250 300	μV MAX
Input Offset Current	I_{OS}	(Note 2)	150 200	pA MAX
Input Bias Current	I_B	(Note 2)	±150 ±200	pA MAX
Large-Signal Voltage Gain	A_{VO}	$V_{OUT} = \pm 12V$, $R_L = 10k\Omega$ $V_{OUT} = \pm 10V$, $R_L = 2k\Omega$	200 120	V/mV MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 13.5V$	110	dB MIN
Power-Supply Rejection	PSR	$V_S = \pm 2V$ to $\pm 20V$	110	dB MIN
Input Voltage Range	IVR	(Note 3)	±13.5	V MIN
Output Voltage Swing	V_O	$R_L = 10k\Omega$	±13	V MIN
Slew Rate	SR		0.1	V/μs MIN
Supply Current	I_{SY}	No Load	600	μA MAX

NOTES:
1. Final offset trims are not performed on dice. These trims are typically performed after packaging. Precision Monolithics Inc. assumes no responsibility for improper trimming by the customer. Contact factory for trim methods.
2. These specifications apply for $\pm 2V \leq V_S \leq \pm 20V$ and $-13.5V \leq V_{CM} \leq +13.5V$ (for $V_S = \pm 15V$).
3. Guaranteed by CMR test.

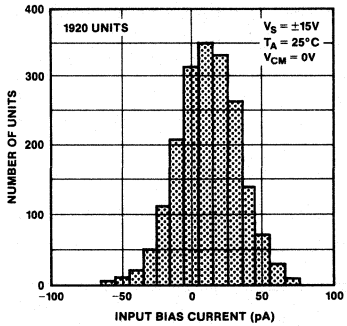
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

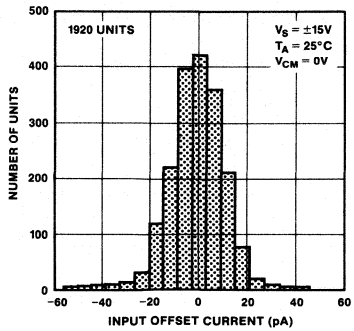
TYPICAL DISTRIBUTION OF INPUT OFFSET VOLTAGE



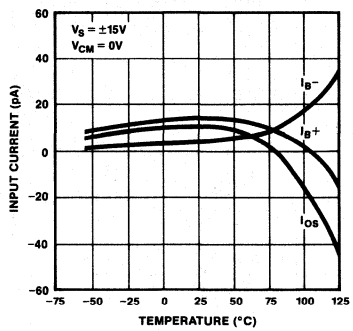
TYPICAL DISTRIBUTION OF INPUT BIAS CURRENT



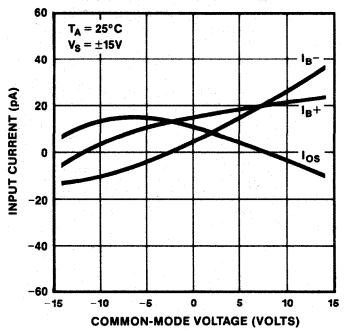
TYPICAL DISTRIBUTION OF INPUT OFFSET CURRENT



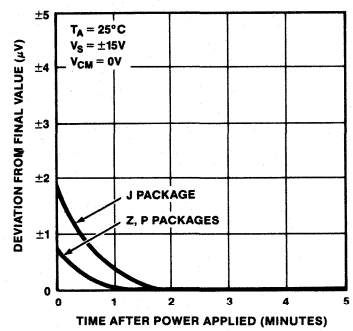
INPUT BIAS, OFFSET CURRENT vs TEMPERATURE



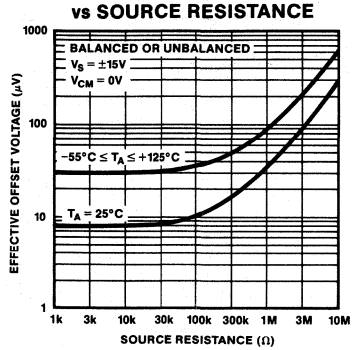
INPUT BIAS, OFFSET CURRENT vs COMMON-MODE VOLTAGE



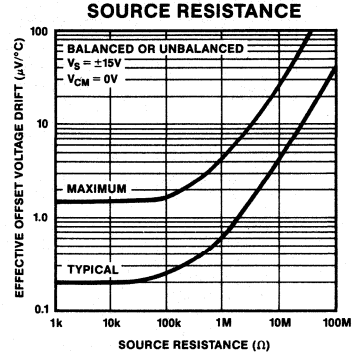
INPUT OFFSET VOLTAGE WARM-UP DRIFT



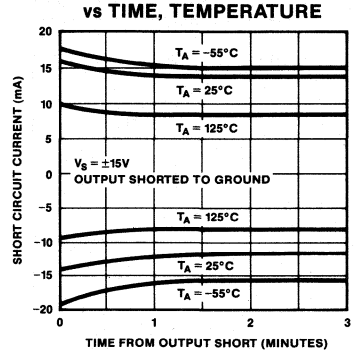
EFFECTIVE OFFSET VOLTAGE vs SOURCE RESISTANCE



EFFECTIVE TCV_{OS} vs SOURCE RESISTANCE



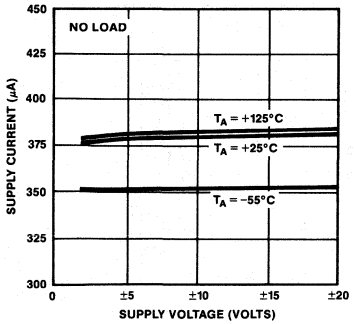
SHORT CIRCUIT CURRENT vs TIME, TEMPERATURE



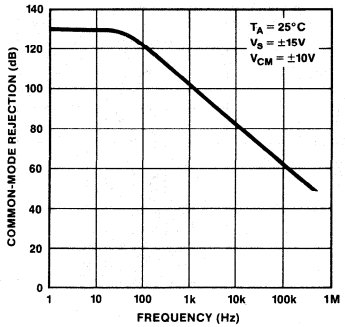
PM-1012

TYPICAL PERFORMANCE CHARACTERISTICS

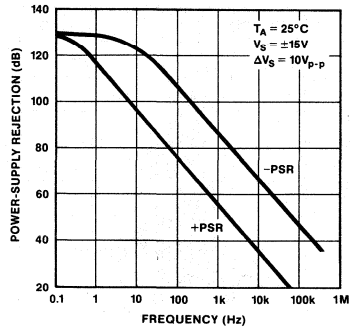
SUPPLY CURRENT vs SUPPLY VOLTAGE



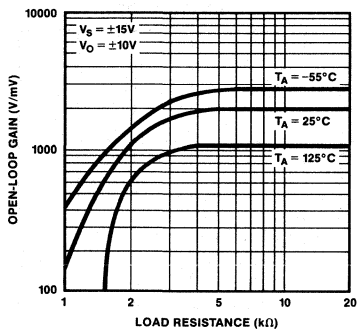
COMMON-MODE REJECTION vs FREQUENCY



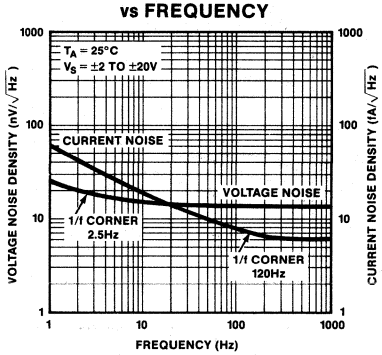
POWER-SUPPLY REJECTION vs FREQUENCY



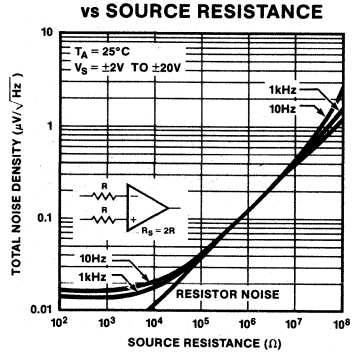
OPEN-LOOP GAIN vs LOAD RESISTANCE



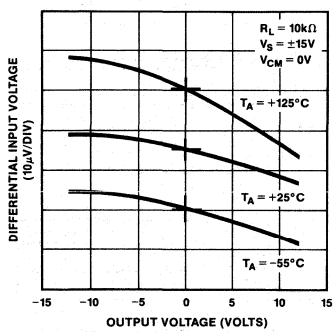
NOISE DENSITY vs FREQUENCY



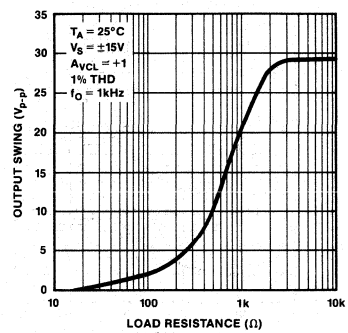
TOTAL NOISE DENSITY vs SOURCE RESISTANCE



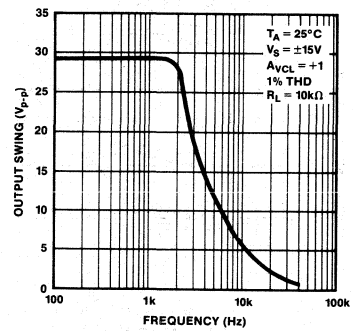
OPEN-LOOP GAIN LINEARITY



MAXIMUM OUTPUT SWING vs LOAD RESISTANCE

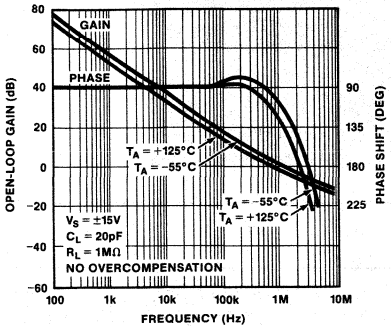


MAXIMUM OUTPUT SWING vs FREQUENCY

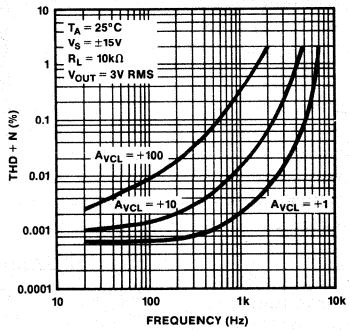


TYPICAL PERFORMANCE CHARACTERISTICS

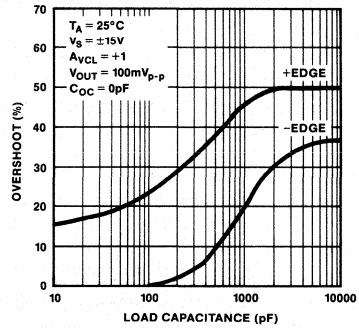
OPEN-LOOP GAIN, PHASE vs FREQUENCY (C_{OC} = 0pF)



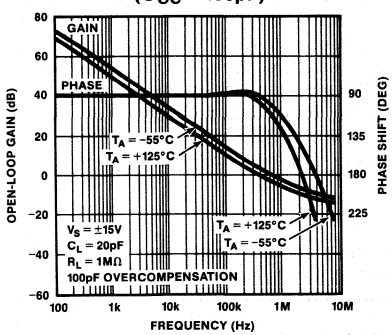
TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY



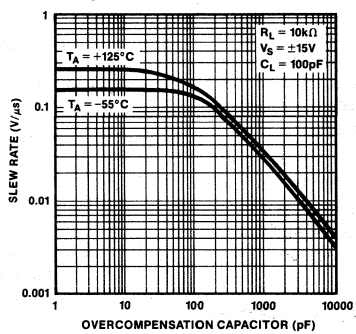
SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD



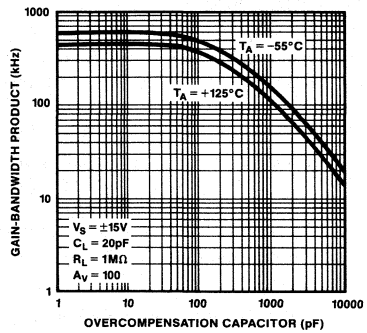
OPEN-LOOP GAIN, PHASE vs FREQUENCY (C_{OC} = 100pF)



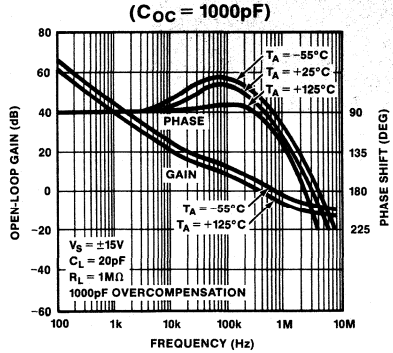
SLEW RATE vs OVERCOMPENSATION



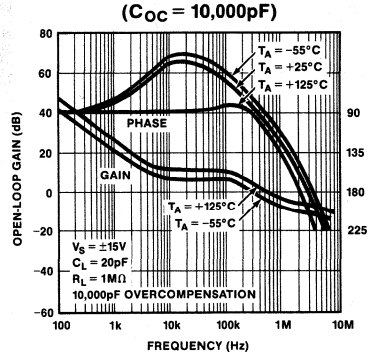
GAIN-BANDWIDTH PRODUCT vs OVERCOMPENSATION



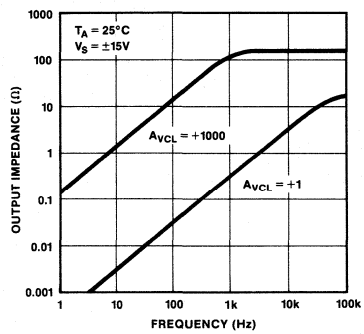
OPEN-LOOP GAIN, PHASE vs FREQUENCY (C_{OC} = 1000pF)



OPEN-LOOP GAIN, PHASE vs FREQUENCY (C_{OC} = 10,000pF)



CLOSED-LOOP OUTPUT RESISTANCE vs FREQUENCY



APPLICATIONS INFORMATION

The PM-1012 is an ideal amplifier for general-purpose applications where precision is critical and power dissipation must be minimized. Excellent input specifications and a wide supply-voltage range allows the PM-1012 to be stocked as a standard amplifier for a wide variety of circuits. Overall performance of the PM-1012 is similar to, and in many respects better than traditional amplifiers such as the OP-07, and the PM-1012 will directly upgrade these sockets.

Extremely low bias current over the full military temperature range makes the PM-1012 attractive for use in sample-and-hold amplifiers, peak detectors, and log amplifiers that must operate over a wide temperature range. Balancing input resistances is not necessary with the PM-1012. Offset voltage and TCV_{OS} are degraded only minimally by high source resistance, even when unbalanced.

The input pins of the PM-1012 are protected against large differential voltages by back-to-back diodes. Current-limiting resistors are not used so that low-noise performance is maintained. If differential voltages above ±1V are expected at the inputs, series resistors must be used to limit the current flow to a maximum of 10mA. Common-mode voltages at the inputs are not restricted, and may vary over the full range of the supply voltages used.

The PM-1012 requires very little operating headroom about the supply rails, and is specified for operation with supplies as low as ±2V. Typically, the common-mode range extends to within one volt of either rail. The output typically swings to within one volt of the rails when using a 10kΩ load.

Offset nulling is achieved utilizing the same circuitry as an OP-07. A potentiometer between 5kΩ and 100kΩ is connected between pins 1 and 8 with the wiper connected to the positive supply. The trim range is between 300μV and 850μV, depending upon the internal trimming of the device.

FIGURE 1: Optional Input Offset Voltage Nulling and Overcompensation Circuits

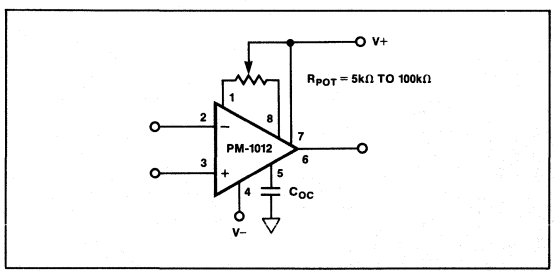
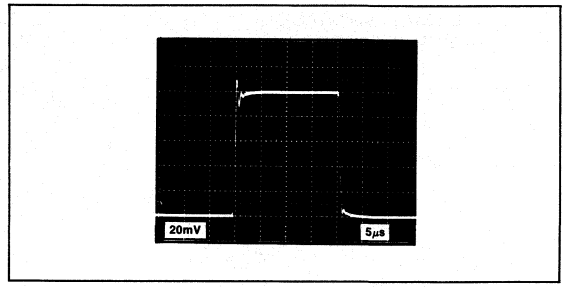


FIGURE 2: Small Signal Transient Response (C_{LOAD} = 100pF, A_{VCL} = +1)



AC PERFORMANCE

The PM-1012's AC characteristics are highly stable over its full operating temperature range. Unity-gain small signal response is shown in Figure 2. Extremely tolerant of capacitive loading on the output, the PM-1012 displays excellent response even with 1000pF loads (Figure 3). In large-signal applications, the input protection diodes effectively short the input to the output during the transients if the amplifier is connected in the usual unity-gain configuration. The output enters short-circuit current limit, with the flow going through the protection diodes. Improved large-signal transient response is obtained by using a feedback resistor between the output and the inverting input. Figure 4 shows the large-signal response of the PM-1012 in unity-gain with a 10kΩ feedback resistor. The unity-gain follower circuit is shown in Figure 5.

FIGURE 3: Small-Signal Transient Response (C_{LOAD} = 1000pF, A_{VCL} = +1)

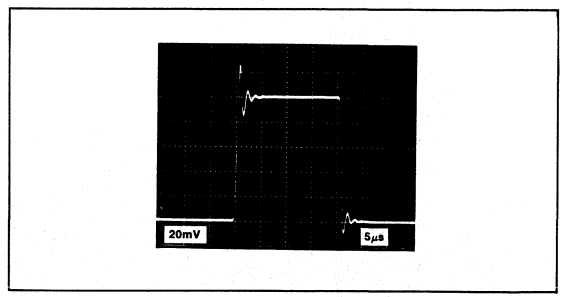


FIGURE 4: Large Signal Transient Response ($A_{VCL} = +1$)

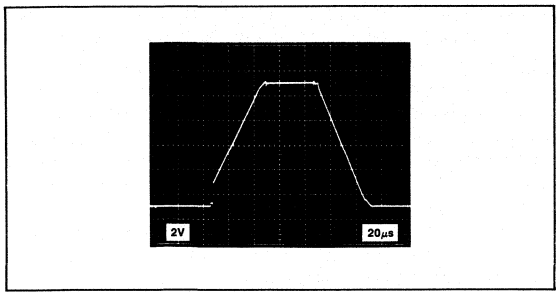
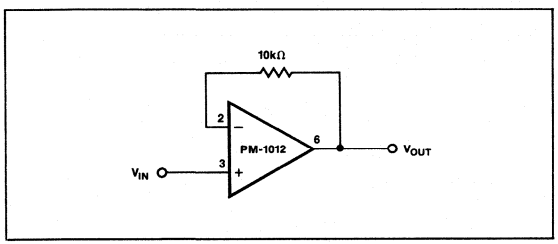


FIGURE 5: Unity-Gain Follower



USING OVERCOMPENSATION

The overcompensation pin provides flexibility for shaping AC response to an application's requirements. This pin may be used to increase the stability of circuits with large capacitive loads or gain in the feedback loop, or for feedforward compensation to improve slew rate.

Figure 6 shows feedforward compensation for a unity-gain follower. Slew rate is increased to close to 10V/µs in this circuit. Load driving ability is adversely affected by this compensation, and gain errors are incurred even with 10kΩ loads. Feedforward compensation should be used with care to ensure that significant errors are not introduced.

Capacitive load driving ability is improved by using overcompensation in the circuit of Figure 1. The signal response in Figure 8 was made under the same conditions as Figure 3, except for the addition of a 220pF capacitor placed between pin 5 and ground. Overcompensation in this manner increases phase margin and decreases the gain-bandwidth product of the amplifier.

FIGURE 6: Follower Feedforward Compensation

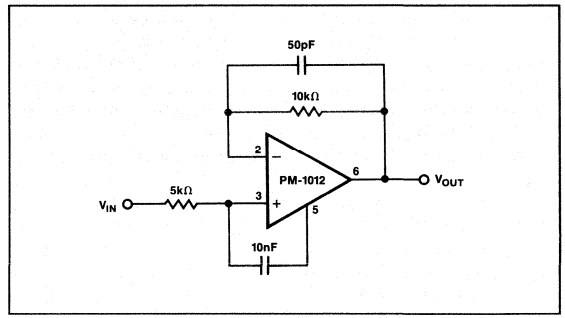


FIGURE 7: Feedforward Compensation Transient Response

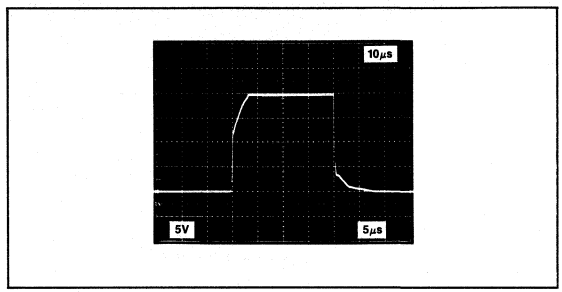
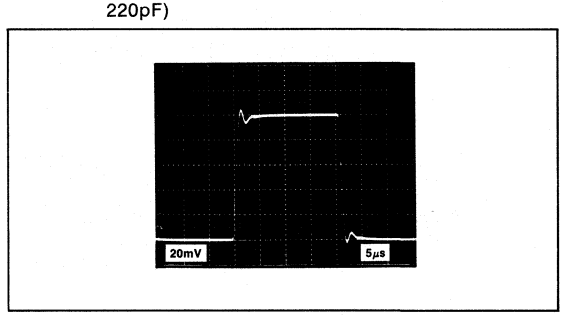


FIGURE 8: Small Signal Transient Response with Overcompensation (C_{LOAD} = 1000pF, $A_{VCL} = +1$, C_{OC} = 220pF)



GUARDING AND SHIELDING

To maintain the extremely high input impedances of the PM-1012, care must be taken in circuit board layout and manufacturing. Board surfaces must be kept scrupulously clean and free of moisture. Conformal coating is recommended to provide a humidity barrier. Even a clean PC board can have 100pA of leakage currents between adjacent traces, so that guard rings should be used around the inputs. Guard traces are operated at a voltage close to that on the inputs, so that leakage currents become minimal. In noninverting applications, the guard ring should be connected to the common-mode voltage at the inverting input (pin 2). In inverting applications, both inputs remain at ground, so that the guard trace should be grounded. Guard traces should be made on both sides of the circuit board.

High impedance circuitry is extremely susceptible to RF pickup, line-frequency hum, and radiated noise from switching power-supplies. Enclosing sensitive analog sections within grounded shields is generally necessary to prevent excessive noise pickup. Twisted-pair cable will aid in rejection of line-frequency hum.

A precision absolute-value current-to-voltage converter that operates over a wide temperature range is shown in Figure 10. The PM-1012's low bias current over its full common-mode and temperature ranges ensures a high degree of linearity in this circuit. The PM-1012 acts as an inverting or noninverting current-to-voltage converter, depending upon the polarity of the input. While the input is sinking current, the voltage is developed across the resistor at the noninverting input, hence sources must have reasonable compliance. While the input is sourcing current, it remains at one diode drop below ground; compliance of a current sink at the input is less critical. If 1MΩ resistors are used, the circuit will output 1V/μA of input current.

FIGURE 9: Guard Ring Layout and Connections

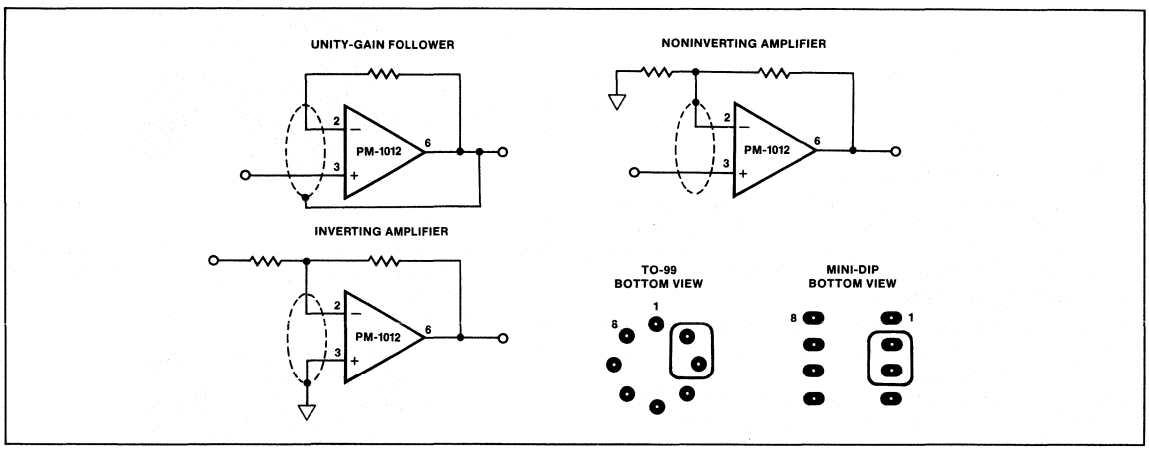


FIGURE 10: Precision Absolute-Value Current-to-Voltage Converter

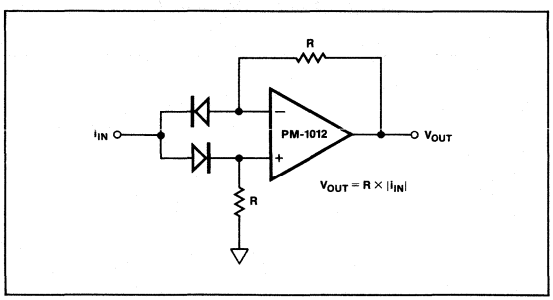
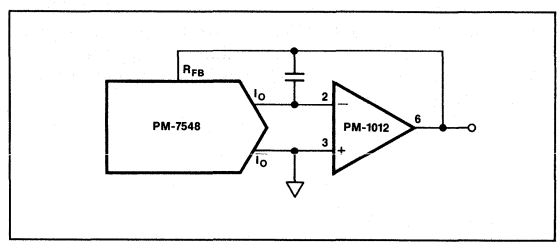


FIGURE 11: DAC Output Amplifier



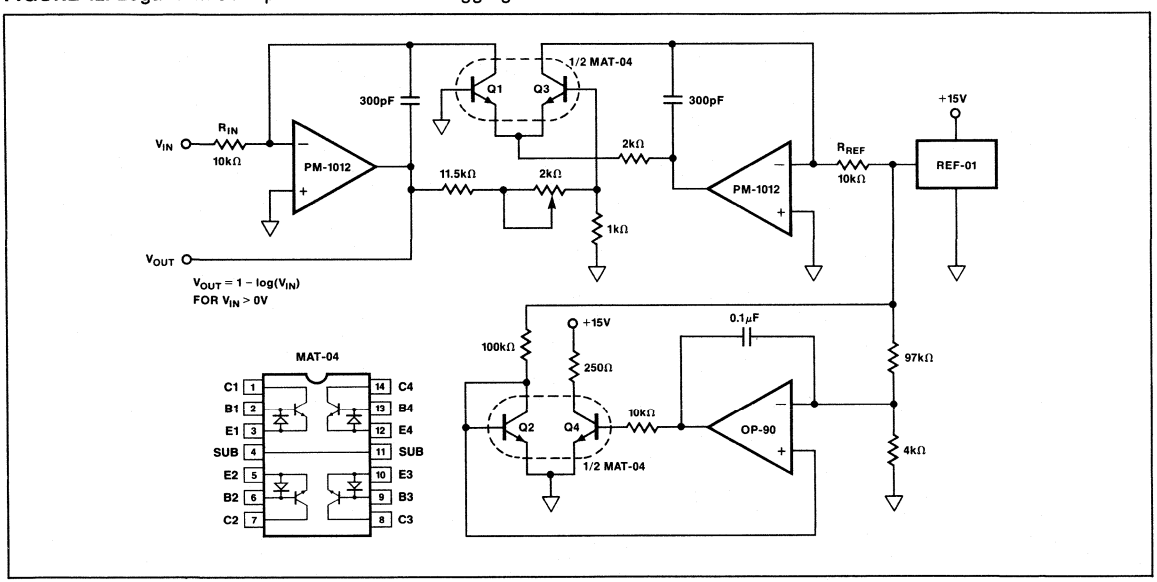
The PM-1012 is an excellent amplifier for CMOS and bipolar DACs where high linearity is critical. Its low bias current and offset voltage ensures that linearity errors are negligible, even when operating with high resolution DACs and low reference voltages. A capacitor should be placed in the feedback loop of the amplifier to cancel the pole formed by the additional input capacitance from the DAC. Twenty to forty picofarads is usually adequate for compensation with CMOS or bipolar DACs.

The logarithmic amplifier in Figure 12 eliminates thermal drift caused by temperature dependencies of the logging transistors by maintaining a monolithic quad matched transistor at a predetermined temperature. The MAT-04 has four transistors laid-out at the corners of a square die. Two transistors across a diagonal are used for logging elements. One of the remaining transistors is used as a heater to maintain a constant chip temperature, and the remaining transistor, diagonally opposite to the heater, is used as a temperature sensor.

The OP-90 servo amplifier uses thermal feedback to set the temperature of the die. The base-to-emitter voltage of Q2 is maintained at the level set by the resistive divider from the REF-01, by controlling the current flowing through Q4. Although Q4 may operate at higher than the MAT-04's rated levels, this does not degrade operation since the characteristics of the heater transistor are non-critical. For best thermal regulation, the MAT-04 package should be encased in insulation. Urethane foam used for housing insulation is excellent for this purpose.

Gain is trimmed using the 2kΩ potentiometer. The zero-crossing point is adjusted by changing the value of R_{REF}. Input scaling may be changed by varying resistor R_{IN}.

FIGURE 12: Logarithmic Amplifier with Heated Logging Transistors



Comparators
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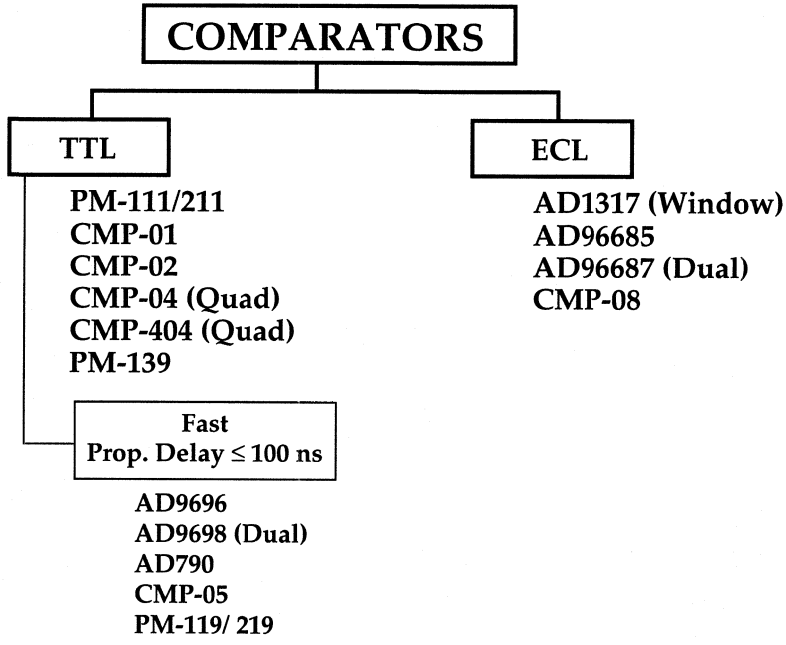
Selection Tree
Comparators



Selection Guide
Comparators

Model	Prop Delay ns max	Dispersion ps	Logic	V_{OS} mV max	Package Options[1]	Temp Range[2]	Page[3]	Comments
AD1317	2.5	250	ECL	10	12	C	SL 6-15	Dedicated Window Comparator with Wide CM Range
AD96685	**3.5**	**50**	**ECL**	**2**	**3, 4, 5, 6, 7**	**I, M**	**3-21**	**Ultrafast**
AD96687	**3.5**	**50**	**ECL**	**2**	**3, 4, 5, 6**	**I, M**	**3-21**	**Dual AD96685**
AD9696	**7.0**	**100**	**TTL**	**2**	**2, 3, 6, 7, 12**	**C, M**	**3-13**	**Single Comparator**
AD9698	**7.0**	**100**	**TTL**	**2**	**3, 6, 7, 12**	**C, M**	**3-13**	**Dual Comparator**
AD790	**45**	**–**	**TTL**	**0.25–1**	**2, 3, 6**	**C, I, M**	**3-5**	**Fast, Precise Single or Dual Supply**
CMP-05	55	–	TTL	0.6	2, 3, 6, 7	I, M	3-51	High Speed Precision Comparator
PM-111/211	180	–	TTL	3.0	1, 2, 4, 6, 7	I, M	3-59	Fast, Wide Input Range, General Purpose
CMP-01	180	–	TTL	0.8	2, 3, 7	C, M	3-27	Fast Precision Comparator
CMP-02	**270**	**–**	**TTL**	**0.8**	**2, 3, 7**	**C, M**	**3-35**	**Low Input Current Precision Comparator**
CMP-04	300 typ	–	TTL	1.0	2, 3, 6	I, M	3-43	Quad Low Power Precision Comparator
PM-139/239	1300	–	TTL	2	1, 2, 4	I, M	3-65	Low Power, Single or Dual Supply

[1]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack, 11 = Single-in-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92; 17 = Plastic Pin Grid Array.
[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.
[3]SL = *Special Linear Reference Manual.*
Boldface Type: Product recommended for new design.
*New product.

Orientation
Comparators

A comparator is a special category of op amp specifically designed to compare the voltages between its two inputs. The comparator operates in the open-loop condition, providing either a positive or a negative output voltage. These two states represent the sign of the net difference between the two inputs. Therefore, the comparator's output will be a logic "1" if the voltage at its +input is greater than that at its −input and a logic "0" for the opposite case.

A comparator is normally used in applications where some varying level is compared to a fixed level (usually a voltage reference). Since it is, in effect, a 1-bit A/D converter, the comparator is a basic element in all A/D converters. A comparator may be used for time measurement if one of its inputs is driven by a ramp. The steadily increasing (or decreasing) ramp is applied to the comparator; its output will change state when its reference level is crossed. The comparator is also an important element of pulse-width modulators, peak detectors, delay generators, and switch drivers.

A comparator is essentially a fast, high-gain amplifier whose output is always at an upper or lower limit, except when switching. The simplest comparator would be an open-loop-connected, uncompensated, high-gain, high-slew-rate op amp with excellent offset & drift characteristics, fast recovery from overdrive and an overdrive-protected input.

In addition, practical comparators have a small amount of hysteresis (internal or external) to help keep noise from causing the output to bounce around, and most have a *latch*, which makes it possible to freeze the output at the state it has at a given instant of time, in response to a logic signal. Since the comparator is producing a digital decision, its outputs are generally compatible with either TTL or ECL.

Aside from its op amp related specifications, such as bias current, offset & drift and the various logic-related timing and interface specs, the key comparator spec is *propagation delay*: the time required for the output to reach the 50% point of a transition, after the net input has crossed the offset voltage—when driven by a square wave to a prescribed value of input overdrive, usually 5 mV or 10 mV. Dispersion is the typical uncertainty (or "jitter") in the propagation delay.

The Selection Guide classifies Analog Devices comparators by propagation delay, presence or absence of a latch and interface logic compatibility. It also indicates the presence of *dual* comparators, each comprising two independent comparators on a single monolithic chip. Pairs of comparators may be used for *window* measurements, as well as for simple two-in-one space-saving.

ANALOG DEVICES

Fast, Precision Comparator

AD790

FEATURES

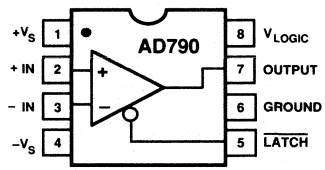
- 45 ns max Propagation Delay
- Single +5 V or Dual ±15 V Supply Operation
- CMOS or TTL Compatible Output
- 250 μV max Input Offset Voltage
- 500 μV max Input Hysteresis Voltage
- 15 V max Differential Input Voltage
- On-Board Latch
- 60 mW Power Dissipation
- Available in 8-Pin Plastic and Hermetic Cerdip Packages
- MIL-STD-883B Processing Available
- Available in Tape and Reel in Accordance with EIA-481A Standard

APPLICATIONS

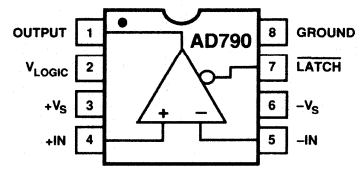
- Zero-Crossing Detectors
- Overvoltage Detectors
- Pulse-Width Modulators
- Precision Rectifiers
- Discrete A/D Converters
- Delta-Sigma Modulator A/Ds

CONNECTION DIAGRAMS

8-Pin Plastic Mini-DIP (N) and Cerdip (Q) Packages



8-Pin SOIC (R) Package



PRODUCT DESCRIPTION

The AD790 is a fast (45 ns), precise voltage comparator, with a number of features that make it exceptionally versatile and easy to use. The AD790 may operate from either a single +5 V supply or a dual ±15 V supply. In the single-supply mode, the AD790's inputs may be referred to ground, a feature not found in other comparators. In the dual-supply mode it has the unique ability of handling a maximum differential voltage of 15 V across its input terminals, easing their interfacing to large amplitude and dynamic signals.

This device is fabricated using Analog Devices' Complementary Bipolar (CB) process – which gives the AD790's combination of fast response time and outstanding input voltage resolution (1 mV max). To preserve its speed and accuracy, the AD790 incorporates a "low glitch" output stage that does not exhibit the large current spikes normally found in TTL or CMOS output stages. Its controlled switching reduces power supply disturbances that can feed back to the input and cause undesired oscillations. The AD790 also has a latching function which makes it suitable for applications requiring synchronous operation.

The AD790 is available in five performance grades. The AD790J and the AD790K are rated over the commercial temperature range of 0 to +70°C. The AD790A and AD790B are rated over the industrial temperature range of −40°C to +85°C. The AD790S is rated over the military temperature range of −55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

PRODUCT HIGHLIGHTS

1. The AD790's combination of speed, precision, versatility and low cost makes it suitable as a general purpose comparator in analog signal processing and data acquisition systems.
2. Built-in hysteresis and a low-glitch output stage minimize the chance of unwanted oscillations, making the AD790 easier to use than standard open-loop comparators.
3. The hysteresis combined with a wide input voltage range enables the AD790 to respond to both slow, low level (e.g., 10 mV) signals and fast, large amplitude (e.g., 10 V) signals.
4. A wide variety of supply voltages are acceptable for operation of the AD790, ranging from single +5 V to dual +5 V/ −12 V, ±5 V, or +5 V/±15 V supplies.
5. The AD790's power dissipation is the lowest of any comparator in its speed range.
6. The AD790's output swing is symmetric between V_{LOGIC} and ground, thus providing a predictable output under a wide range of input and output conditions.

AD790—SPECIFICATIONS

DUAL SUPPLY (Operation @ +25°C and $+V_S$ = +15 V, $-V_S$ = −15 V, V_{LOGIC} = +5 V unless otherwise noted)

Parameter	Conditions	AD790J/A Min	AD790J/A Typ	AD790J/A Max	AD790K/B Min	AD790K/B Typ	AD790K/B Max	AD790S Min	AD790S Typ	AD790S Max	Units
RESPONSE CHARACTERISTIC	100 mV Step										
Propagation Delay, t_{PD}	5 mV Overdrive		40	45		40	45		40	45	ns
	T_{min} to T_{max}			45/50			45/50			60	ns
OUTPUT CHARACTERISTICS											
Output HIGH Voltage, V_{OH}	1.6 mA Source		4.65			4.65			4.65		
	6.4 mA Source	**4.3**	4.45		**4.3**	4.45		**4.3**	4.45		V
	T_{min} to T_{max}	**4.3/4.3**			**4.3**			**4.3**			V
Output LOW Voltage, V_{OL}	1.6 mA Sink		0.35			0.35			0.35		V
	6.4 mA Sink		0.44	**0.5**		0.44	**0.5**		0.44	**0.5**	V
	T_{min} to T_{max}			**0.5/0.5**			**0.5**			**0.5**	V
INPUT CHARACTERISTICS											
Offset Voltage[1]			0.2	**1.0**		0.05	**0.25**		0.2	**1.0**	mV
	T_{min} to T_{max}			1.5			**0.5**			**1.5**	mV
Hysteresis[2]	T_{min} to T_{max}	0.3	0.4	0.6	**0.3**	0.4	**0.5**	**0.3**	0.4	**0.65**	mV
Bias Current	Either Input		2.5	5		1.8	**3.5**		2.5	**5**	μA
	T_{min} to T_{max}			6.5			**4.5**			**7**	μA
Offset Current			0.04	**0.25**		0.02	**0.15**		0.04	**0.25**	μA
	T_{min} to T_{max}			0.3			**0.2**			**0.4**	μA
Power Supply Rejection Ratio dc	V_S ±20%	**80**	90		**88**	100		**80**	90		dB
	T_{min} to T_{max}	76	88		**85**	93		**76**	85		dB
Input Voltage Range											
Differential Voltage	$V_S \leq \pm 15$ V			$\pm V_S$			$\pm V_S$			$\pm V_S$	V
Common Mode		$-V_S$		$+V_S-2$ V	$-V_S$		$+V_S-2$ V	$-V_S$		$+V_S-2$ V	V
Common Mode Rejection Ratio	$-10\text{ V} < V_{CM} < +10\text{ V}$	**80**	95		**88**	105		**80**	95		dB
	T_{min} to T_{max}	76	90		**85**	100		**76**	88		dB
Input Impedance			20‖2			20‖2			20‖2		MΩ‖pF
LATCH CHARACTERISTICS											
Latch Hold Time, t_H			25	35		25	35		25	35	ns
Latch Setup Time, t_S			5	10		5	10		5	10	ns
LOW Input Level, V_{IL}	T_{min} to T_{max}			0.8			**0.8**			**0.8**	V
HIGH Input Level, V_{IH}	T_{min} to T_{max}	1.6			**1.6**			**1.6**			V
Latch Input Current			2.3	**5**		2.3	**3.5**		2.3	**5**	μA
	T_{min} to T_{max}			7			5			**8**	μA
SUPPLY CHARACTERISTICS											
Diff Supply Voltage[3]	V_{LOGIC} = 5 V										
	T_{min} to T_{max}	4.5		33	**4.5**		**33**	**4.7**		**33**	V
Logic Supply	T_{min} to T_{max}	4.0		7	**4.0**		**7**	**4.2**		**7**	V
Quiescent Current											
$+V_S$	$+V_S$ = 15 V		8	**10**		8	**10**		8	**10**	mA
$-V_S$	$-V_S$ = −15 V		4	5		4	5		4	5	mA
V_{LOGIC}	V_{LOGIC} = 5 V		2	**3.3**		2	**3.3**		2	**3.3**	mA
Power Dissipation				**242**			**242**			**242**	mW
TEMPERATURE RANGE											
Rated Performance	T_{min} to T_{max}	0 to +70/−40 to +85			0 to +70/−40 to +85			−55 to +125			°C

NOTES

[1]Defined as the average of the input voltages at the low to high and high to low transition points. Refer to Figure 14.

[2]Defined as half the magnitude between the input voltages at the low to high and high to low transition points. Refer to Figure 14.

[3]$+V_S$ must be no lower than (V_{LOGIC} −0.5 V) in any supply operating conditions, except during power up.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final test.

Specifications subject to change without notice.

SINGLE SUPPLY (Operation @ +25°C and $+V_S = V_{LOGIC} = +5$ V, $-V_S = 0$ unless otherwise noted)[1]

Parameter	Conditions	AD790J/A Min	AD790J/A Typ	AD790J/A Max	AD790K/B Min	AD790K/B Typ	AD790K/B Max	AD790S Min	AD790S Typ	AD790S Max	Units
RESPONSE CHARACTERISTIC	100 mV Step										
Propagation Delay, t_{PD}	5 mV Overdrive		45	50		45	50		45	50	ns
	T_{min} to T_{max}			50/60			50/60			65	ns
OUTPUT CHARACTERISTICS											
Output HIGH Voltage, V_{OH}	1.6 mA Source		4.65			4.65			4.65		
	6.4 mA Source	**4.3**	4.45		**4.3**	4.45		**4.3**	4.45		V
	T_{min} to T_{max}	4.3			**4.3**			**4.3**			V
Output LOW Voltage, V_{OL}	1.6 mA Sink		0.35			0.35			0.35		V
	6.4 mA Sink		0.44	**0.5**		0.44	**0.5**		0.44	**0.5**	V
	T_{min} to T_{max}			0.5			**0.5**			**0.5**	V
INPUT CHARACTERISTICS											
Offset Voltage[2]			0.45	**1.5**		0.35	**0.6**		0.45	**1.5**	mV
	T_{min} to T_{max}			2.0			**0.85**			**2.0**	mV
Hysteresis[3]	T_{min} to T_{max}	0.3	0.5	0.75	**0.3**	0.5	**0.65**	**0.3**	0.7	**1.0**	mV
Bias Current	Either Input		2.7	5		2.0	**3.5**		2.7	**5**	μA
	T_{min} to T_{max}			7			**5**			**8**	μA
Offset Current			0.04	**0.25**		0.02	**0.15**		0.04	**0.25**	μA
	T_{min} to T_{max}			0.3			**0.2**			**0.4**	μA
Power Supply											
Rejection Ratio dc	4.5 V≤V_S≤5.5 V	**80**	90		**86**	100		**80**	90		dB
	T_{min} to T_{max}	**76/76**	88		**82**	93		**76**	85		dB
Input Voltage Range											
Differential Voltage				**±V_S**			**±V_S**			**±V_S**	V
Common Mode		0		**+V_S−2 V**	0		**+V_S−2 V**	0		**+V_S−2 V**	V
Input Impedance			20‖2			20‖2			20‖2		MΩ‖pF
LATCH CHARACTERISTICS											
Latch Hold Time, t_H			25	35		25	35		25	35	ns
Latch Setup Time, t_S			5	10		5	10		5	10	ns
LOW Input Level, V_{IL}	T_{min} to T_{max}			0.8			**0.8**			**0.8**	V
HIGH Input Level, V_{IH}	T_{min} to T_{max}	1.6			**1.6**			**1.6**			V
Latch Input Current			2.3	5		2.3	3.5		2.3	5	μA
	T_{min} to T_{max}			7			5			**8**	μA
SUPPLY CHARACTERISTICS											
Supply Voltage[4]	T_{min} to T_{max}	4.5		7	**4.5**		**7**	**4.7**		**7**	V
Quiescent Current			10	**12**		10	**12**		10	**12**	mA
Power Dissipation				**60**			**60**			**60**	mW
TEMPERATURE RANGE											
Rated Performance	T_{min} to T_{max}	0 to +70/−40 to +85			0 to +70/−40 to +85			−55 to +125			°C

NOTES
[1]Pin 1 tied to Pin 8, and Pin 4 tied to Pin 6.
[2]Defined as the average of the input voltages at the low to high and high to low transition points. Refer to Figure 14.
[3]Defined as half the magnitude between the input voltages at the low to high and high to low transition points. Refer to Figure 14.
[4]$-V_S$ must not be connected above ground.

Specifications subject to change without notice.

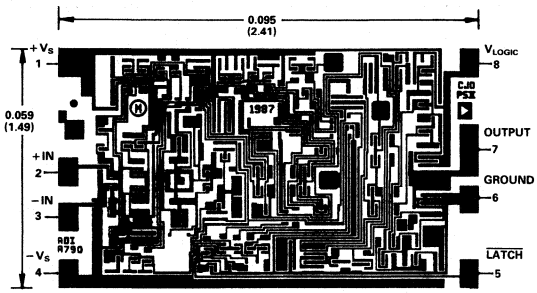
All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final test.

ABSOLUTE MAXIMUM RATINGS[1, 2]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2] . . . . . 500 mW
Differential Input Voltage . . . . . ±16.5 V
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range
(N, R) . . . . . −65°C to +125°C
(Q) . . . . . −65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C
Logic Supply Voltage . . . . . 7 V

METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).
Call factory for chip specifications.



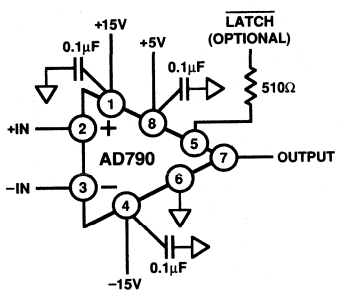


Figure 1. Basic Dual Supply Configuration (N, Q Package Pinout)

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functionalop-eration of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Thermal characteristics: plastic N-8 package: θ_{JA} = 90°C/watt; ceramic Q-8 package: θ_{JA} = 110°C/watt, θ_{JC} = 30°C/watt.
SOIC (R-8) package: θ_{JA} = 160°C/watt; θ_{JC} = 42°C/watt.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD790JN	0°C to +70°C	Plastic DIP	N-8
AD790JR	0°C to +70°C	SOIC	R-8
AD790JR-REEL	0°C to +70°C	Reel	
AD790KN	0°C to +70°C	Plastic DIP	N-8
AD790AQ	−40°C to +85°C	Cerdip	Q-8
AD790BQ	−40°C to +85°C	Cerdip	Q-8
AD790SQ	−55°C to +125°C	Cerdip	Q-8
AD790SQ/883B	−55°C to +125°C	Cerdip	Q-8
AD790S Chips	−55°C to +125°C	Die	

*For outline information see Package Information section.

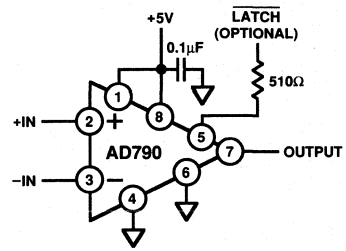


Figure 2. Basic Single Supply Configuration (N, Q Package Pinout)

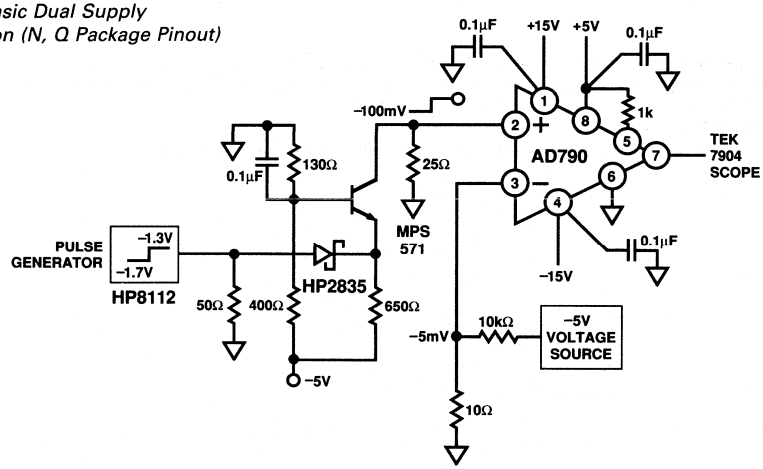


Figure 3. Response Time Test Circuit (N, Q Package Pinout)

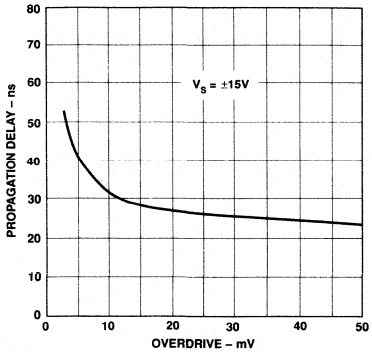


Figure 4. Propagation Delay vs. Overdrive

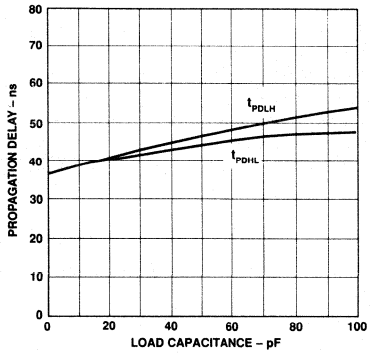


Figure 5. Propagation Delay vs. Load Capacitance

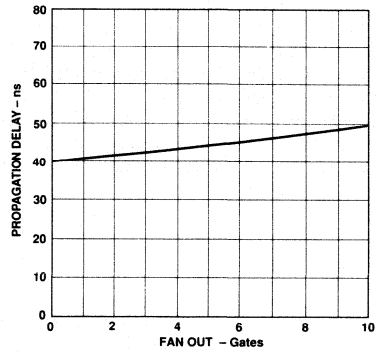


Figure 6. Propagation Delay vs. Fanout (LSTTL and CMOS)

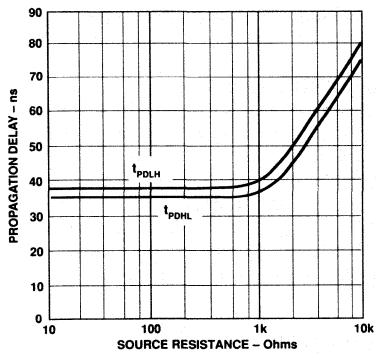


Figure 7. Propagation Delay vs. Source Resistance

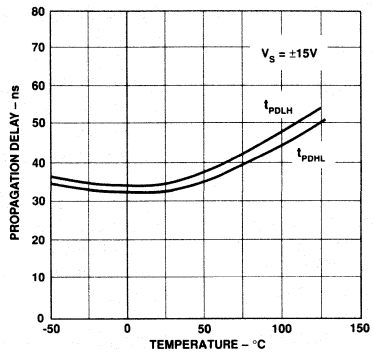


Figure 8. Propagation Delay vs. Temperature

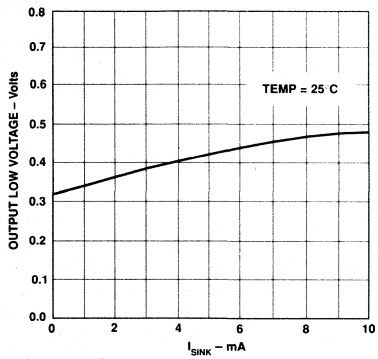


Figure 9. Output Low Voltage vs. Sink Current

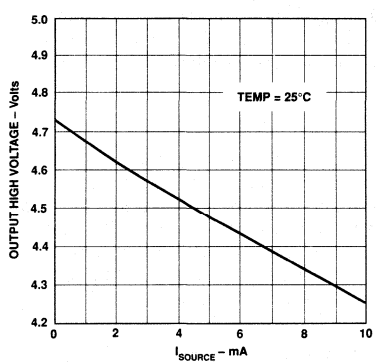


Figure 10. Output High Voltage vs. Source Current

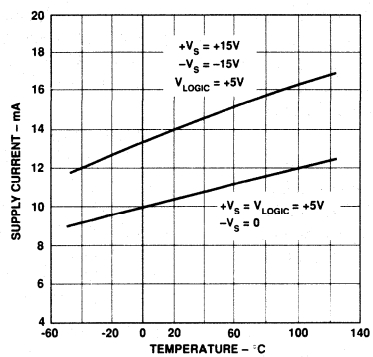


Figure 11. Total Supply Current vs. Temperature

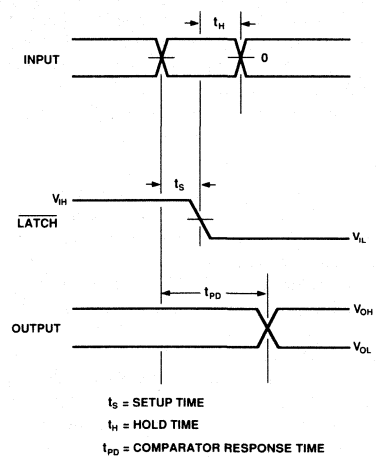


Figure 12. Latch Timing

CIRCUIT DESCRIPTION

The AD790 possesses the overall characteristics of a standard monolithic comparator: differential inputs, high gain and a logic output. However, its function is implemented with an architecture which offers several advantages over previous comparator designs. Specifically, the output stage alleviates some of the limitations of classic "TTL" comparators and provides a symmetric output. A simplified representation of the AD790 circuitry is shown in Figure 13.

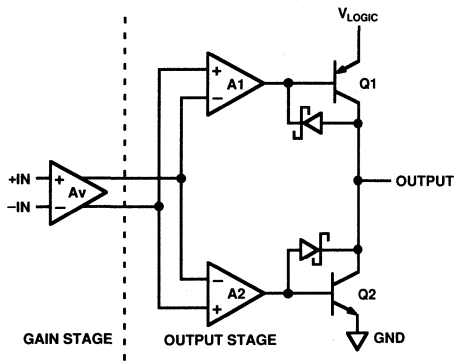


Figure 13. AD790 Block Diagram

The output stage takes the amplified differential input signal and converts it to a single-ended logic output. The output swing is defined by the pull-up PNP and the pull-down NPN. These produce inherent rail-to-rail output levels, compatible with CMOS logic, as well as TTL, without the need for clamping to internal bias levels. Furthermore, the pull-up and pull-down levels are symmetric about the center of the supply range and are referenced off the V_{LOGIC} supply and ground. The output stage has nearly symmetric dynamic drive capability, yielding equal rise and fall times into subsequent logic gates.

Unlike classic TTL or CMOS output stages, the AD790 circuit does not exhibit large current spikes due to unwanted current flow between the output transistors. The AD790 output stage has a controlled switching scheme in which amplifiers A1 and A2 drive the output transistors in a manner designed to reduce the current flow between Q1 and Q2. This also helps minimize the disturbances feeding back to the input which can cause troublesome oscillations.

The output high and low levels are well controlled values defined by V_{LOGIC} (+5 V), ground and the transistor equivalent "Schottky" clamps and are compatible with TTL and CMOS logic requirements. The fanout of the output stage is shown in Figure 6 for standard LSTTL or HCMOS gates. Output drive behavior vs. capacitive load is shown in Figure 5.

HYSTERESIS

The AD790 uses internal feedback to develop hysteresis about the input reference voltage. Figure 14 shows how the input offset voltage and hysteresis terms are defined. Input offset voltage (V_{OS}) is the difference between the center of the hysteresis range and the ground level. This can be either positive or negative. The hysteresis voltage (V_H) is one-half the width of the

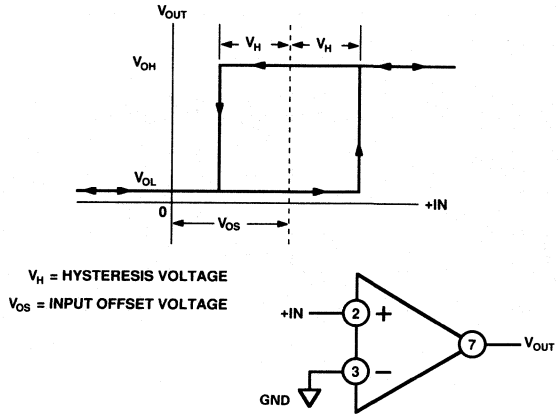


Figure 14. Hysteresis Definitions (N, Q Package Pinout)

hysteresis range. This built-in hysteresis allows the AD790 to avoid oscillation when an input signal slowly crosses the ground level.

SUPPLY VOLTAGE CONNECTIONS

The AD790 may be operated from either single or dual supply voltages. Internally, the V_{LOGIC} circuitry and the analog front-end of the AD790 are connected to separate supply pins. If dual supplies are used, any combination of voltages in which $+V_S \geq V_{LOGIC} - 0.5$ V and $-V_S \leq 0$ may be chosen. For single supply operation (i.e. $+V_S = V_{LOGIC}$), the supply voltage can be operated between 4.5 V and 7 V. Figure 15 shows some other examples of typical supply connections possible with the AD790.

BYPASSING AND GROUNDING

Although the AD790 is designed to be stable and free from oscillations, it is important to properly bypass and ground the power supplies. Ceramic 0.1 μF capacitors are recommended and should be connected directly at the AD790's supply pins. These capacitors provide transient currents to the device during comparator switching. The AD790 has three supply voltage pins, $+V_S$, $-V_S$ and V_{LOGIC}. It is important to have a common ground lead on the board for the supply grounds and the GND pin of the AD790 to provide the proper return path for the supply current.

LATCH OPERATION

The AD790 has a latch function for retaining input information at the output. The comparator decision is "latched" and the output state is held when Pin 5 is brought low. As long as Pin 5 is kept low, the output remains in the high or low state , and does not respond to changing inputs. Proper capture of the input signal requires that the timing relationships shown in Figure 12 are followed. Pin 5 should be driven with CMOS or TTL logic levels.

The output of the AD790 will respond to the input when Pin 5 is at a high logic level. When not in use, Pin 5 should be connected to the positive logic supply. When using dual supplies, it is recommended that a 510 Ω resistor be placed in series with Pin 5 and the driving logic gate to limit input currents during power up.

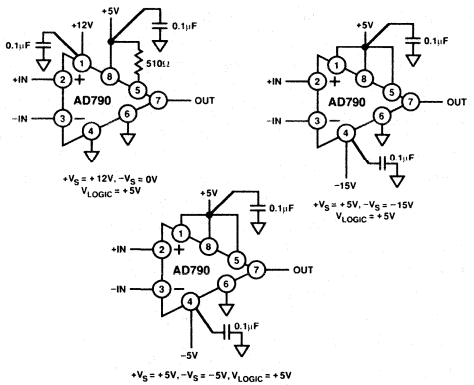


Figure 15. Typical Power Supply Connections (N, Q Package Pinout)

Window Comparator for Over-Voltage Detection

The wide differential input range of the AD790 makes it suitable for monitoring large amplitude signals. The simple overvoltage detection circuit shown in Figure 16 illustrates direct connection of the input signal to the high impedance inputs of the comparator without the need for special clamp diodes to limit the differential input voltage across the inputs.

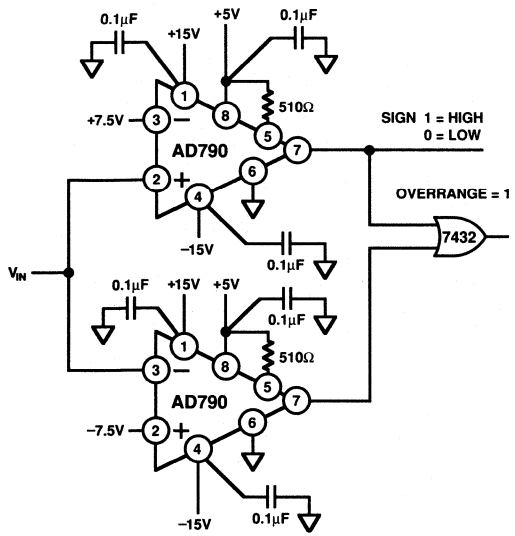


Figure 16. Overvoltage Detector (N, Q Package Pinout)

Single Supply Ground Referred Overload Detector

The AD790 is useful as an overload detector for sensitive loads that must be powered from a single supply. A simple ground referenced overload detector is shown in Figure 16. The comparator senses a voltage across a PC board trace and compares that to a reference (trip) voltage established by the comparator's minus supply current through a 2.7 Ω resistor. This sets up a 10 mV reference level that is compared to the sense voltage. The minus supply current is proportional to absolute temperature and compensates for the change in the sense resistance with temperature. The width and length of the PC board trace determine the resistance of the trace and consequently the trip current level.

$I_{LIMIT} = 10\ mV/R_{SENSE}$

R_{SENSE} = rho (trace length/trace width)

rho = resistance of a unit square of trace

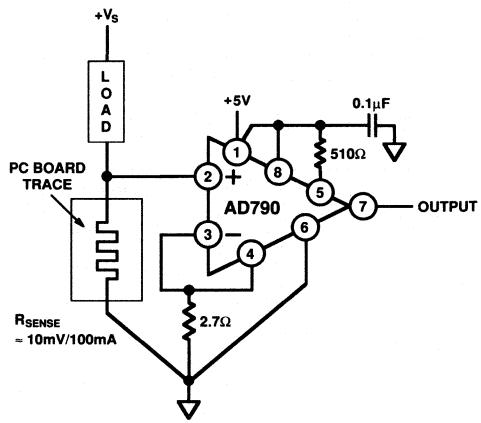


Figure 17. Ground Referred Overload Detector Circuit (N, Q Package Pinout)

Precision Full-Wave Rectifier

The high speed and precision of the AD790 make it suitable for use in the wide dynamic range full-wave rectifier shown in Figure 18. This circuit is capable of rectifying low level signals as small as a few mV or as high as 10 V. Input resolution, propagation delay and op amp settling will ultimately limit the maximum input frequency for a given accuracy level. Total comparator plus switch delay is approximately 100 ns, which limits the maximum input frequency to 1 MHz for clean rectification.

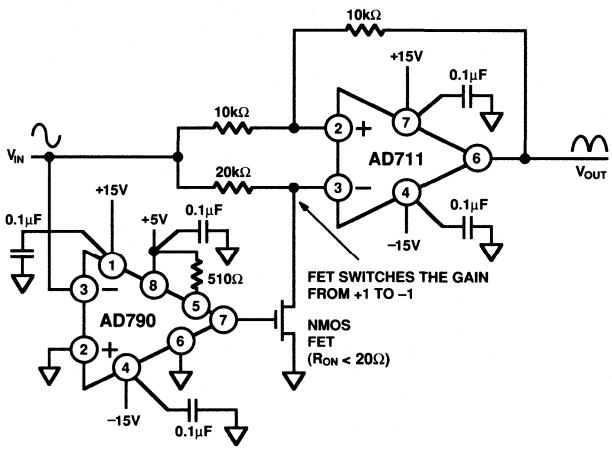
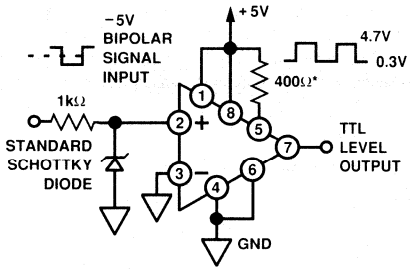


Figure 18. Precision Full-Wave Rectifier (N, Q Package Pinout)



*A RESISTOR UP TO 10kΩ MAYBE USED TO REDUCE THE SOURCE AND SINK CURRENT OF THE DRIVER. HOWEVER, THIS WILL SLIGHTLY LOWER THE MAXIMUM USABLE CLOCK RATE.

Figure 19. A Bipolar to CMOS TTL Line Receiver (N, Q Package Pinout)

Bipolar to CMOS/TTL

It is sometimes desirable to translate a bipolar signal (e.g., ±5 V) coming from a communications cable or another section of the system to CMOS/TTL logic levels; such an application is referred to as a line receiver. Previously, the interface to the bipolar signal required either a dual (±) power supply or a reference voltage level about which the line receiver would switch. The AD790 may be used in a simple circuit to provide a unique capability: the ability to receive a bipolar signal while powered from a single +5 V supply. Other comparators cannot perform this task. Figure 19 shows a 1 kΩ resistor in series with the input signal which is then clamped by a Schottky diode, holding the input of the comparator at 0.4 V below ground. Although the comparator is specified for a common mode range down to $-V_S$, (in this case ground)it is permissible to bring one of the inputs a few hundred mV below ground. The comparator switches around this level and produces a CMOS/TTL compatible swing. The circuit will operate to switching frequencies of 20 MHz.

ANALOG DEVICES

Ultrafast TTL Comparators

AD9696/AD9698

FEATURES
4.5 ns Propagation Delay
200 ps Maximum Propagation Delay Dispersion
Single +5 V or ±5 V Supply Operation
Complementary Matched TTL Outputs

APPLICATIONS
High Speed Line Receivers
Peak Detectors
Window Comparators
High Speed Triggers
Ultrafast Pulse Width Discriminators

GENERAL DESCRIPTION

The AD9696 and AD9698 are ultrafast TTL-compatible voltage comparators able to achieve propagation delays previously possible only in high performance ECL devices. The AD9696 is a single comparator providing 4.5 ns propagation delay, 200 ps maximum delay dispersion and 1.7 ns setup time. The AD9698 is a dual comparator with equally high performance; both devices are ideal for critical timing circuits in such applications as ATE, communications receivers and test instruments.

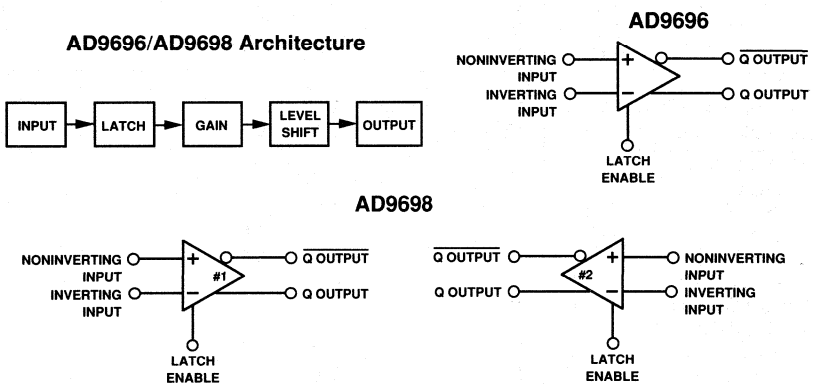
Both devices allow the use of either a single +5 V supply or ±5 V supplies. The choice of supplies determines the common mode input voltage range available: −2.2 V to +3.7 V for ±5 V operation, +1.4 V to +3.7 V for single +5 V supply operation.

The differential input stage features high precision, with offset voltages which are less than 2 mV and offset currents less than 1 μA. A latch enable input is provided to allow operation in either sample-and-hold or track-and-hold applications.

The AD9696 and AD9698 are both available as commercial temperature range devices operating from ambient temperatures of 0°C to +70°C, and as extended temperature range devices for ambient temperatures from −55°C to +125°C. Both versions are available qualified to MIL-STD-883 class B.

Package options for the AD9696 include a 10-pin TO-100 metal can, an 8-pin ceramic DIP, an 8-pin plastic DIP, and an 8-lead small outline plastic package. The AD9698 is available in a 16-pin ceramic DIP, a 16-lead ceramic gullwing, a 16-pin plastic DIP, and a 16-lead small outline plastic package. Military qualified versions of the AD9696 come in the TO-100 can and ceramic DIP; the dual AD9698 comes in ceramic DIP.

FUNCTIONAL BLOCK DIAGRAM



AD9696/AD9698—SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ($+V_S/-V_S$) . . . . . +7 V/−7 V
Input Voltage Range . . . . . ±5 V
Differential Input Voltage . . . . . 5.4 V
Latch Enable Voltage . . . . . −0.5 V to $+V_S$
Output Current (Continuous) . . . . . 20 mA
Power Dissipation . . . . . 600 mW

Operating Temperature Range[2]
AD9696/AD9698KH/KN/KQ/KR[3] . . . . . 0°C to +70°C
AD9696/AD9698TH/TQ[3] . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature
KH/KQ/TH/TQ Suffixes . . . . . +175°C
KN/KR Suffixes . . . . . +150°C
Lead Soldering Temperature (10 sec) . . . . . +300°C

ELECTRICAL CHARACTERISTICS (Supply Voltages = −5.2 V and +5.0 V; load as specified in Note 4, unless otherwise indicated)

Parameter	Temp	Test Level	0°C to +70°C AD9696/AD9698 KH/KN/KQ/KR[3] Min	Typ	Max	−55°C to +125°C AD9696/AD9698 TH/TQ[3] Min	Typ	Max	Units
INPUT CHARACTERISTICS									
Input Offset Voltage[5]	+25°C	I		1.0	2.0		1.0	2.0	mV
	Full	VI			3.0			3.0	mV
Input Offset Voltage Drift	Full	V		10			10		µV/°C
Input Bias Current	+25°C	I		16	55		16	55	µA
	Full	VI			110			110	µA
Input Offset Current	+25°C	I		0.4	1.0		0.4	1.0	µA
	Full	VI			1.3			1.3	µA
Input Capacitance	+25°C	V		3			3		pF
Input Voltage Range									
±5.0 V	Full	VI	−2.2		+3.7	−2.2		+3.7	V
+5.0 V	Full	VI	+1.4		+3.7	+1.4		+3.7	V
Common Mode Rejection Ratio									
±5.0 V	Full	VI	80	85		80	85		dB
+5.0 V	Full	VI	57	63		57	63		dB
LATCH ENABLE INPUT									
Logic "1" Voltage Threshold	Full	VI	2.0			2.0			V
Logic "0" Voltage Threshold	Full	VI			0.8			0.8	V
Logic "1" Current	Full	VI			10			10	µA
Logic "0" Current	Full	VI			1			1	µA
DIGITAL OUTPUTS									
Logic "1" Voltage (Source 4 mA)	Full	VI	2.7	3.5		2.7	3.5		V
Logic "0" Voltage (Sink 10 mA)	Full	VI		0.4	0.5		0.4	0.5	V
SWITCHING PERFORMANCE									
Propagation Delay (t_{PD})[6]									
Input to Output HIGH	Full	IV		4.5	7.0		4.5	7.0	ns
Input to Output LOW	Full	IV		4.5	7.0		4.5	7.0	ns
Latch Enable to Output HIGH	+25°C	IV		6.5	8.5		6.5	8.5	ns
Latch Enable to Output LOW	+25°C	IV		6.5	8.5		6.5	8.5	ns
Delta Delay Between Outputs	+25°C	IV		0.5	1.5		0.5	1.5	ns
Propagation Delay Dispersion									
20 mV to 100 mV Overdrive	+25°C	V		100			100		ps
100 mV to 1.0 V Overdrive	+25°C	IV		100	200		100	200	ps
Rise Time[11]	+25°C	V		1.85			1.85		ns
Fall Time[11]	+25°C	V		1.35			1.35		ns
Latch Enable									
Pulse Width [$t_{PW(E)}$]	+25°C	IV	3.5	2.5		3.5	2.5		ns
Setup Time (t_S)	+25°C	IV	3	1.7		3	1.7		ns
Hold Time (t_H)	+25°C	IV	3	1.9		3	1.9		ns

Parameter	Temp	Test Level	0°C to +70°C AD9696/AD9698 KH/KN/KQ/KR[3] Min	Typ	Max	−55°C to +125°C AD9696/AD9698 TH/TQ[3] Min	Typ	Max	Units
POWER SUPPLY[7]									
Positive Supply Current[8]									(+5.0 V)
AD9696	Full	VI		26	32		26	32	mA
AD9698	Full	VI		52	64		52	64	mA
Negative Supply Current[9]									(−5.2 V)
AD9696	Full	VI		2.5	4.0		2.5	4.0	mA
AD9698	Full	VI		5.0	8.0		5.0	8.0	mA
Power Dissipation									
AD9696 +5.0 V	Full	V		130			130		mW
AD9696 ±5.0 V	Full	V		146			146		mW
AD9698 +5.0 V	Full	V		260			260		mW
AD9698 ±5.0 V	Full	V		292			292		mW
Power Supply Rejection Ratio[10]	+25°C	VI	70			70			dB
	Full	VI	65			65			dB

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Typical thermal impedances:

AD9696 Metal Can	θ_{JA} = 170°C/W	θ_{JC} = 50°C/W
AD9696 Ceramic DIP	θ_{JA} = 110°C/W	θ_{JC} = 20°C/W
AD9696 Plastic DIP	θ_{JA} = 160°C/W	θ_{JC} = 30°C/W
AD9696 Plastic SOIC	θ_{JA} = 180°C/W	θ_{JC} = 30°C/W
AD9698 Ceramic DIP	θ_{JA} = 90°C/W	θ_{JC} = 25°C/W
AD9698 Plastic DIP	θ_{JA} = 100°C/W	θ_{JC} = 20°C/W
AD9698 Plastic SOIC	θ_{JA} = 120°C/W	θ_{JC} = 20°C/W

[3]Suffixes KH and TH apply only to model AD9696; AD9698 not available in metal can.

[4]Load circuit has 420 Ω from $+V_S$ to output; 460 Ω from output to ground.

[5]$R_S \leq 100$ Ω.

[6]Propagation delays measured with 100 mV pulse; 10 mV overdrive.

[7]Supply voltages should remain stable within ±5% for normal operation.

[8]Specification applies to both +5 V and ±5 V supply operation.

[9]Specification applies to only ±5 V supply operation.

[10]Measured with nominal values ±5% of $+V_S$ and $-V_S$.

[11]Although fall time is faster than rise time, the complementary outputs cross at midpoint of logic swing because of delay on start of falling edge.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

II – 100% production tested at +25°C, and sample tested at specified temperatures.

III – Sample tested only.

IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

ORDERING GUIDE

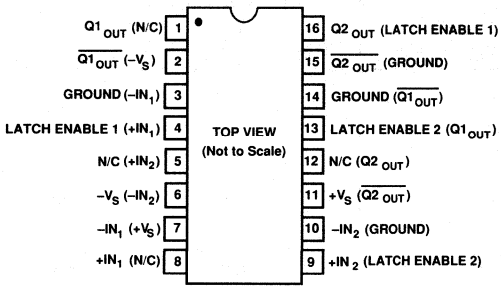
Model	Package	Temperature	Package Option[1]
AD9696KH	TO-100 Can	0°C to +70°C	H-10
AD9696KN	Plastic DIP	0°C to +70°C	N-8
AD9696KR	SOIC	0°C to +70°C	R-8
AD9696KQ	Cerdip	0°C to +70°C	Q-8
AD9696TH	TO-100 Can	−55°C to +125°C	H-10
AD9696TQ	Cerdip	−55°C to +125°C	Q-8
AD9696TZ/883B[2]	Gullwing	−55°C to +125°C	Z-8
AD9698KN	Plastic DIP	0°C to +70°C	N-16
AD9698KR	SOIC	0°C to +70°C	R-16A
AD9698KQ	Cerdip	0°C to +70°C	Q-16
AD9698TQ	Cerdip	−55°C to +125°C	Q-16
AD9698TZ/883B[3]	Gullwing	−55°C to +125°C	Z-16

[1]H = Hermetic Metal Can, N = Plastic DIP, Q = Cerdip, R = Small Outline (SOIC), Z = Ceramic Leaded Chip Carrier. For outline information see Package Information section.

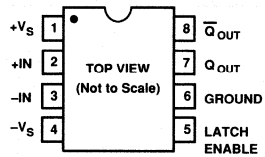
[2]Refer to AD9696TZ/883B military data sheet.

[3]Refer to AD9698TZ/883B military data sheet.

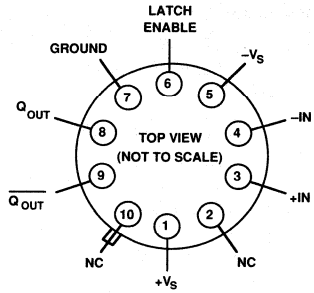
PIN CONFIGURATIONS



AD9698KN/KQ/TQ
[AD9698KR PINOUTS SHOWN IN ( )]



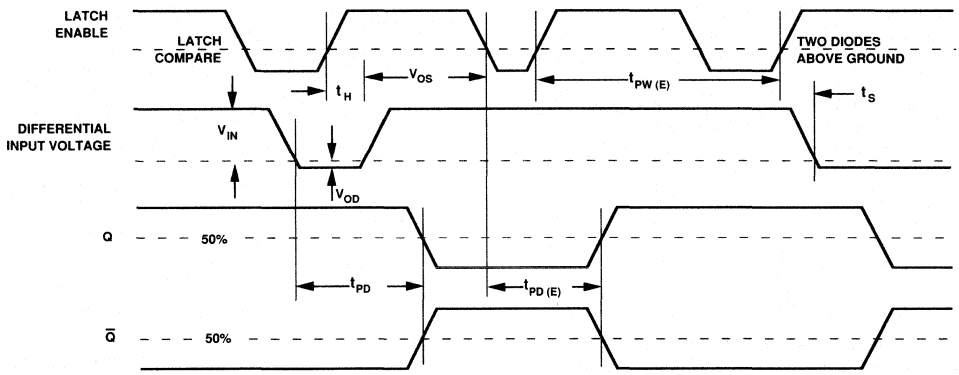
AD9696KN/KR/KQ/TQ



AD9696KH/TH

PIN DESCRIPTIONS

Name	Function
$Q1_{OUT}$	One of two complementary outputs. $Q1_{OUT}$ will be at logic HIGH if voltage at $+IN_1$ is greater than voltage at $-IN_1$ and LATCH ENABLE 1 is at logic LOW.
$\overline{Q1_{OUT}}$	One of two complementary outputs. $\overline{Q1_{OUT}}$ will be at logic HIGH if voltage at $-IN_1$ is greater than voltage at $+IN_1$ and LATCH ENABLE 1 is at logic LOW.
GROUND	Analog and digital ground return. All GROUND pins should be connected together and to a low impedance ground plane near the comparator.
LATCH ENABLE 1	Output at $Q1_{OUT}$ will track differential changes at the inputs when LATCH ENABLE 1 is at logic LOW. When LATCH ENABLE 1 is at logic HIGH, the output at $Q1_{OUT}$ will reflect the input state at the application of the latch command, delayed by the Latch Enable Setup Time (t_S). Since the architecture of the input stage (see block diagram) is faster than the logic of the latch stage, data will typically be latched if applied to the comparator(s) within 1.7 ns after the latch. This is the Setup Time (t_S); for guaranteed performance, t_S must be 3 ns.
N/C	No internal connection to comparator.
$-V_S$	Negative power supply connection; nominally −5.2 V.
$-IN_1$	Inverting input of differential input stage for Comparator #1.
$+IN_1$	Noninverting input of differential input stage for Comparator #1.
$+IN_2$	Noninverting input of differential input stage for Comparator #2.
$-IN_2$	Inverting input of differential input stage for Comparator #2.
$+V_S$	Positive power supply connection; nominally +5 V.
LATCH ENABLE 2	Output at $Q2_{OUT}$ will track differential changes at the inputs when LATCH ENABLE 2 is at logic LOW. When LATCH ENABLE 2 is at logic HIGH, the output at $Q2_{OUT}$ will reflect the input state at the application of the latch command, delayed by the Latch Enable Setup Time (t_S). Since the architecture of the input stage (see block diagram) is faster than the logic of the latch stage, data will typically be latched if applied to the comparator(s) within 1.7 ns after the latch. This is the Setup Time (t_S); for guaranteed performance, t_S must be 3 ns.
$\overline{Q2_{OUT}}$	One of two complementary outputs. $\overline{Q2_{OUT}}$ will be at logic HIGH if voltage at $-IN_2$ is greater than voltage at $+IN_2$ and LATCH ENABLE 2 is at logic LOW.
$Q2_{OUT}$	One of two complementary outputs. $Q2_{OUT}$ will be at logic HIGH if voltage at $+IN_2$ is greater than voltage at $-IN_2$ and LATCH ENABLE 2 is at logic LOW.

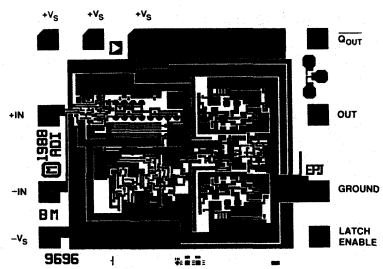


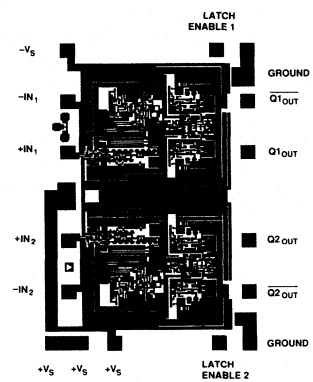
t_S – MINIMUM SETUP TIME (Typically 1.7ns)
t_H – MINIMUM HOLD TIME (Typically 1.9ns)
t_{PD} – INPUT TO OUTPUT DELAY
$t_{PD(E)}$ – LATCH ENABLE TO OUTPUT DELAY
$t_{PW(E)}$ – MINIMUM LATCH ENABLE PULSE WIDTH (Typically 2.5ns)
V_{OS} – INPUT OFFSET VOLTAGE
V_{OD} – OVERDRIVE VOLTAGE

AD9696/AD9698 Timing Diagram

DIE LAYOUT AND MECHANICAL INFORMATION

Die Dimensions AD9696	59×71×15 (±2) mils
AD9698	79×109×15 (±2) mils
Pad Dimensions	4×4 mils
Metalization	Aluminum
Backing	None
Substrate Potential	$-V_S$
Passivation	Nitride





THEORY OF OPERATION

Refer to the block diagram of the AD9696/AD9698 comparators. The AD9696 and AD9698 TTL voltage comparator architecture consists of five basic stages: input, latch, gain, level shift and output. Each stage is designed to provide optimal performance and make it easy to use the comparators.

The input stage operates with either a single +5-volt supply, or with a +5-volt supply and a −5.2-volt supply. For optimum power efficiency, the remaining stages operate with only a single +5-volt supply. The input stage is an input differential pair without the customary emitter follower buffers. This configuration increases input bias currents but maximizes the input voltage range.

A latch stage allows the most recent output state to be retained as long as the latch input is held high. In this way, the input to the comparator can be changed without any change in the output state. As soon as the latch enable input is switched to LOW, the output changes to the new value dictated by the signal applied to the input stage.

The gain stage assures that even with small values of input voltage, there will be sufficient levels applied to the following stages to cause the output to switch TTL states as required. A level shift stage between the gain stage and the TTL output stage guarantees that appropriate voltage levels are applied from the gain stage to the TTL output stage.

Only the output stage uses TTL logic levels; this minimum use of TTL circuits maximizes speed and minimizes power consumption. The outputs are clamped with Schottky diodes to assure that the rising and falling edges of the output signal are closely matched.

The AD9696 and AD9698 represent the state of the art in high speed TTL voltage comparators. Great care has been taken to optimize the propagation delay dispersion performance. This assures that the output delays will remain constant despite varying levels of input overdrive. This characteristic, along with closely matched rising and falling outputs, provides extremely consistent results at previously unattainable speeds.

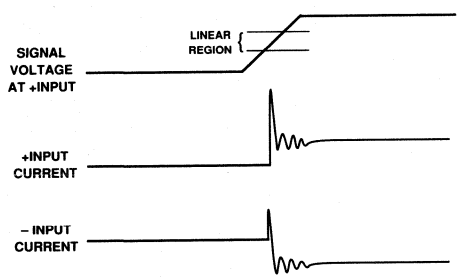
APPLICATIONS

General

Two characteristics of the AD9696 and AD9698 should be considered for any application. First is the fact that all TTL comparators are prone to oscillate if the inputs are close to equal for any appreciable period of time. One instance of this happening would be slow changes in the unknown signal; the probability of oscillation is reduced when the unknown signal passes through the threshold at a high slew rate. Another instance is if the unknown signal does not overdrive the comparator logic. Unless they are overdriven, TTL comparators have undershoot when switching logic states. The smaller the overdrive, the greater the undershoot; when small enough, the comparator will oscillate, not being able to determine a valid logic state. For the AD9696 and AD9698, 20 mV is the smallest overdrive which will assure crisp switching of logic states without significant undershoot.

The second characteristic to keep in mind when designing threshold circuits for these comparators is twofold: (1) bias currents change when the threshold is exceeded; and (2) ac input impedance decreases when the comparator is in its linear region.

During the time both transistors in the differential pair are conducting, the ac input impedance drops by orders of magnitude. Additionally, the input bias current switches from one input to the other, depending upon whether or not the threshold is exceeded. As a result, the input currents follow approximately the characteristic curves shown below.



Threshold Input Currents

This characteristic will not cause problems unless a high impedance threshold circuit or drive circuit is employed. A circuit similar to that shown in the window comparator application can eliminate this possible problem.

Window Comparator

Many applications require determining when a signal's voltage falls within, above, or below a particular voltage range. A simple tracking window comparator can provide this data. Figure 1 shows such a window comparator featuring high speed, TTL compatibility, and ease of implementation.

Two comparators are required to establish a "window" with upper and lower threshold voltages. The circuit shown uses the AD9698 dual ultrafast TTL comparator. In addition to the cost and space savings over a design using two single comparators, the dual comparator on a single die produces better matching of both dc and dynamic characteristics.

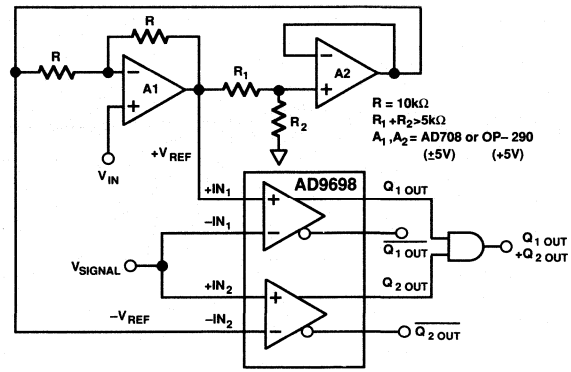


Figure 1. AD9698 Used as Window Detector

When configured as shown, the op amps generate reference levels for the comparators that are equally spaced above and below the applied V_{IN}. The width of the window is established by the ratio of R1 and R2. For a given ratio of R1 and R2, $+V_{REF}$ and $-V_{REF}$ will be fixed percentages above and below V_{IN}. As an example, using 2.2 kΩ for R1 and 10 kΩ for R2 creates a ±10% window. When V_{IN} equals +3 V, $+V_{REF}$ will be +3.3 V and $-V_{REF}$ will be +2.7 V. Likewise, for a −2 V input, the thresholds will be −1.8 V and −2.2 V. Windows of differing percentage width can be calculated with the equation:

$$(1-X)/2X = R2/R1$$

where:

X = % window

Additionally, the low impedance of the op amp outputs assures that the threshold voltages will remain constant when the input currents change as the signal passes through the threshold voltage levels.

The output of the AND gate will be high while the signal is inside the window. $\overline{Q1_{OUT}}$ will be high when the signal is above $+V_{REF}$, and $\overline{Q2_{OUT}}$ will be high when the signal is below $-V_{REF}$.

Crystal Oscillator

Oscillators are used in a wide variety of applications from audio circuits to waveform generators, from ATE triggers and telecommunications transceivers to radar. Figure 2 shows a versatile and inexpensive oscillator. The circuit uses the AD9696, in a positive feedback mode, and is capable of generating accurate and stable oscillations with frequencies ranging from 1 MHz to more than 40 MHz.

To generate oscillations from 1 to 25 MHz, a fundamental mode crystal is used without the dc blocking capacitor and choke. The parallel capacitor on the inverting input is selected for stability (0.1 μF for 1–10 MHz; 220 pF for frequencies above 10 MHz).

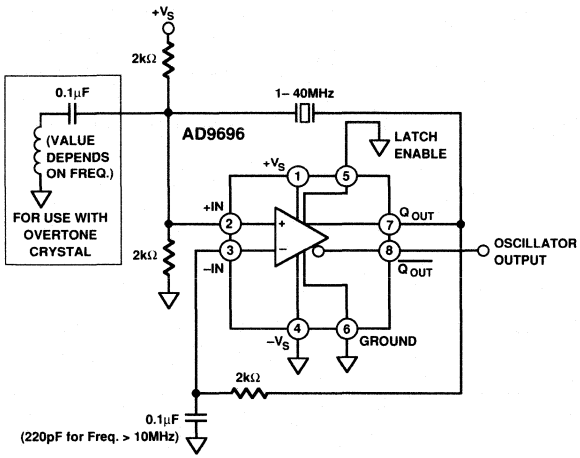


Figure 2. AD9696 Oscillator Circuit (Based on DIP Pinouts)

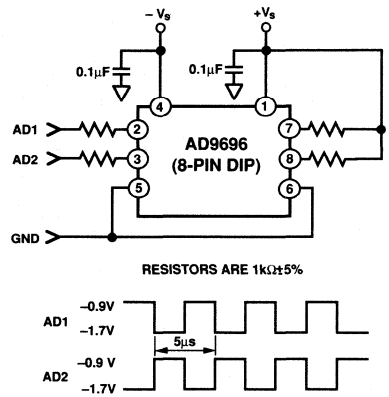
When generating frequencies using a nonfundamental mode crystal, a choke and dc blocking capacitor are added. As an example, a 36 MHz oscillator can be achieved by using a 12 MHz crystal operating on its third overtone. To suppress oscillation at the 12 MHz fundamental, the value of the choke is chosen to provide a low reactive impedance at the fundamental frequency while maintaining a high reactive impedance at the desired output frequency (for 36 MHz operation, L = 1.8 μH). The shunt capacitor at the inverting input has a value of 220 pF for a stable 36 MHz frequency.

LAYOUT CONSIDERATIONS

When working with high speed circuits, proper layout is critical. Analog signal paths should be kept as short as possible and be properly terminated to avoid reflections. In addition, digital signal paths should be kept short, and run lengths should be matched to avoid propagation delay mismatch. All analog signals should be kept as far away from digital signal paths as possible; this reduces the amount of digital switching noise that might be capacitively coupled into the analog section of the circuit.

In high speed circuits, layout of the ground circuit is the most important factor. A single, low impedance ground plane, on the component side of the board, will reduce noise in the circuit ground. It is especially important to maintain continuity of the ground plane under and around the AD9696 or AD9698.

Sockets limit the dynamic performance of the device and should be used only for prototypes or evaluation.



Burn-In Circuit

ANALOG DEVICES

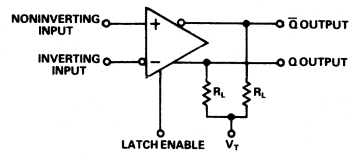
Ultrafast Comparators

AD96685/AD96687

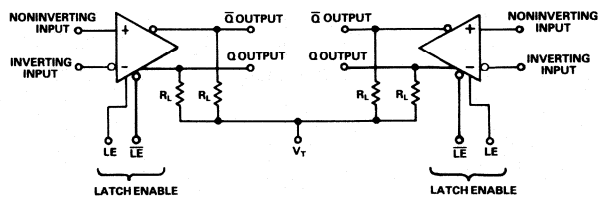
FEATURES
Fast: 2.5ns Propagation Delay
Low Power: 118mW per Comparator
Packages: DIP, TO-100, SOIC, PLCC
Power Supplies: +5V, −5.2V
Logic Compatibility: ECL
MIL-STD-883 Versions Available
50ps Delay Dispersion

APPLICATIONS
High Speed Triggers
High Speed Line Receivers
Threshold Detectors
Window Comparators
Peak Detectors

AD96685 FUNCTIONAL BLOCK DIAGRAM



AD96687 FUNCTIONAL BLOCK DIAGRAM



THE OUTPUTS ARE OPEN EMITTERS, REQUIRING EXTERNAL PULL-DOWN RESISTORS. THESE RESISTORS MAY BE IN THE RANGE OF 50Ω – 200Ω CONNECTED TO −2.0V, OR 200Ω – 2000Ω

GENERAL DESCRIPTION

The AD96685 and AD96687 are ultrafast voltage comparators. The AD96685 is a single comparator with 2.5ns propagation delay; the AD96687 is an equally fast dual comparator. Both devices feature 50ps propagation delay dispersion which is a particularly important characteristic of high speed comparators. It is a measure of the difference in propagation delay under differing overdrive conditions.

A fast, high precision differential input stage permits consistent propagation delay with a wide variety of signals in the common-mode range from −2.5V to +5V. Outputs are complementary digital signals fully compatible with ECL 10K and 10KH logic families. The outputs provide sufficient drive current to directly drive transmission lines terminated in 50Ω to −2V. A level-sensitive latch input is included which permits tracking, track-hold, or sample-hold modes of operation.

The AD96685 and AD96687 are available in both industrial, −25°C to +85°C, and military temperature ranges. Industrial range devices are available in 16-pin DIP, SOIC, and 20-lead PLCC; additionally, the AD96685 is available in a 10-pin, TO-100 metal can. Both devices are available qualified to MIL-STD-883, Class B in 16-pin ceramic DIP and 20-lead ceramic LCC; the TO-100 version of the AD96685 is also mil-qualified.

AD96685/AD96687—SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_S$) . . . . . +6.5V
Negative Supply Voltage ($-V_S$) . . . . . −6.5V
Input Voltage Range[2] . . . . . ±5V
Differential Input Voltage 5.5V
Latch Enable Voltage . . . . . $-V_S$ to 0V
Output Current 30mA

Operating Temperature Range[3]
AD96685/87/BH/BQ/BP/BR . . . . . −25°C to +85°C
AD96685/87/TE/TH/TQ . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −55°C to +150°C
Junction Temperature . . . . . +175°C
Lead Soldering Temperature (10sec) . . . . . +300°C

ELECTRICAL CHARACTERISTICS (Positive Supply Voltage = +5.0V; Negative Supply Voltage = −5.2V, unless otherwise stated)

			Industrial Temp. Range −25°C to +85°C						Extended Temp. Range −55°C to +125°C						
		Test	AD96685BH/BQ/BP/BR			AD96687BQ/BP/BR			AD96685TE/TH/TQ			AD96687TE/TQ			
Parameter	Temp	Level	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
INPUT CHARACTERISTICS															
Input Offset Voltage[4]	+25°C	I		1	2		1	2		1	2		1	2	mV
	Full	VI			3			3			3			3	mV
Input Offset Drift	Full	V		20			20			20			20		µV/°C
Input Bias Current	+25°C	I		7	10		7	10		7	10		7	10	µA
	Full	VI			13			13			16			16	µA
Input Offset Current	+25°C	I		0.1	1.0		0.1	1.0		0.1	1.0		0.1	1.0	µA
	Full	VI			1.2			1.2			1.2			1.2	µA
Input Resistance	+25°C	V		200			200			200			200		kΩ
Input Capacitance	+25°C	V		2			2			2			2		pF
Input Voltage Range[5]	Full	VI	−2.5		+5.0	−2.5		+5.0	−2.5		+5.0	−2.5		+5.0	V
Common-Mode Rejection Ratio	Full	VI	80	90		80	90		80	90		80	90		dB
ENABLE INPUT															
Logic "1" Voltage	Full	VI	−1.1			−1.1			−1.1			−1.1			V
Logic "0" Voltage	Full	VI			−1.5			−1.5			−1.5			−1.5	V
Logic "1" Current	Full	VI			40			40			40			40	µA
Logic "0" Current	Full	VI			5			5			5			5	µA
DIGITAL OUTPUTS[6]															
Logic "1" Voltage	Full	VI	−1.1			−1.1			−1.1			−1.1			V
Logic "0" Voltage	Full	VI			−1.5			−1.5			−1.5			−1.5	V
SWITCHING PERFORMANCE[6]															
Propagation Delays[7]															
Input to Output HIGH	+25°C	IV		2.5	3.5		2.5	3.5		2.5	3.5		2.5	3.5	ns
Input to Output LOW	+25°C	IV		2.5	3.5		2.5	3.5		2.5	3.5		2.5	3.5	ns
Latch Enable to Output HIGH	+25°C	IV		2.5	3.5		2.5	3.5		2.5	3.5		2.5	3.5	ns
Latch Enable to Output LOW	+25°C	IV		2.5	3.5		2.5	3.5		2.5	3.5		2.5	3.5	ns
Dispersion[8]	+25°C	V		50			50			50			50		ps
Latch Enable															
Minimum Pulse Width	+25°C	IV		2.0	3.0		2.0	3.0		2.0	3.0		2.0	3.0	ns
Minimum Setup Time	+25°C	IV		0.5	1.0		0.5	1.0		0.5	1.0		0.5	1.0	ns
Minimum Hold Time	+25°C	IV		0.5	1.0		0.5	1.0		0.5	1.0		0.5	1.0	ns
POWER SUPPLY[9]															
Positive Supply Current (+5.0V)	Full	VI		8	9		15	18		8	9		15	18	mA
Negative Supply Current (−5.2V)	Full	VI		15	18		31	36		15	18		31	36	mA
Power Supply Rejection Ratio[10]	Full	VI	60	70		60	70		60	70		60	70		dB

NOTES
[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Under no circumstances should the input voltages exceed the supply voltages.
[3]Typical thermal impedances . . .

AD96685 Metal Can	$\theta_{JA} = 172°C/W; \theta_{JC} = 52°C/W$
AD96685 Ceramic	$\theta_{JA} = 115°C/W; \theta_{JC} = 57°C/W$
AD96685 LCC	$\theta_{JA} = 172°C/W; \theta_{JC} = 65°C/W$
AD96685 SOIC	$\theta_{JA} = 170°C/W; \theta_{JC} = 60°C/W$
AD96685 PLCC	$\theta_{JA} = 88°C/W; \theta_{JC} = 45°C/W$
AD96687 Ceramic	$\theta_{JA} = 115°C/W; \theta_{JC} = 57°C/W$
AD96687 LCC	$\theta_{JA} = 82°C/W; \theta_{JC} = 31°C/W$
AD96687 SOIC	$\theta_{JA} = 92°C/W; \theta_{JC} = 47°C/W$
AD96687 PLCC	$\theta_{JA} = 81°C/W; \theta_{JC} = 45°C/W$

[4]$R_S = 100\Omega$.
[5]Input Voltage Range can be extended to $-3.3V$ if $-V_S = -6.0V$.
[6]Outputs terminated through 50Ω to −2.0V.
[7]Propagation delays measured with 100mV pulse (10mV overdrive), to 50% transition point of the output.
[8]Change in propagation Delay from 100mV to 1V input overdrive.
[9]Supply voltages should remain stable within ±5% for normal operation.
[10]Measured at ±5% of $+V_S$ and $-V_S$.
Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

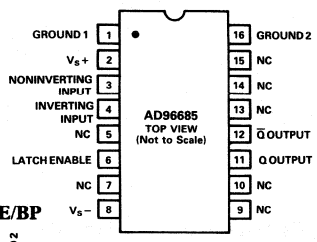
Test Level
I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures.
III – Sample tested only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% production tested at +25°C; 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

FUNCTIONAL DESCRIPTION

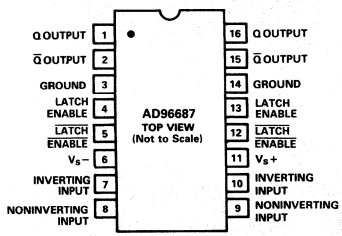
Pin Name	Description
$+V_S$	– Positive supply terminal, nominally +5.0V.
NONINVERTING INPUT	– Noninverting analog input of the differential input stage. The NONINVERTING INPUT must be driven in conjunction with the INVERTING INPUT.
INVERTING INPUT	– Inverting analog input of the differential input stage. The INVERTING INPUT must be driven in conjunction with the NONINVERTING INPUT.
LATCH ENABLE	– In the "compare" mode (logic HIGH), the output will track changes at the input of the comparator. In the "latch" mode (logic LOW), the output will reflect the input state just prior to the comparator being placed in the "latch" mode. $\overline{\text{LATCH ENABLE}}$ must be driven in conjunction with LATCH ENABLE for the AD96687.
$\overline{\text{LATCH ENABLE}}$	– In the "compare" mode (logic LOW), the output will track changes at the input of the comparator. In the "latch" mode (logic HIGH), the output will reflect the input state just prior to the comparator being placed in the "latch" mode. LATCH ENABLE must be driven in conjunction with $\overline{\text{LATCH ENABLE}}$ for the AD96687.
$-V_S$	– Negative supply terminal, nominally −5.2V.
Q	– One of two complementary outputs. Q will be at logic HIGH if the analog voltage at the NONINVERTING INPUT is greater than the analog voltage at the INVERTING INPUT (provided the comparator is in the "compare" mode). See LATCH ENABLE and $\overline{\text{LATCH ENABLE}}$ (AD96687 only) for additional information.
$\overline{Q}$	– One of two complementary outputs. $\overline{Q}$ will be at logic LOW if the analog voltage at the NONINVERTING INPUT is greater than the analog voltage at the INVERTING INPUT (provided the comparator is in the "compare" mode). See LATCH ENABLE and $\overline{\text{LATCH ENABLE}}$ (AD96687 only) for additional information.
GROUND 1	– One of two grounds, but primarily associated with the digital ground. Both grounds should be connected together near the comparator.
GROUND 2	– One of two grounds, but primarily associated with the analog ground. Both grounds should be connected together near the comparator.

PIN DESIGNATIONS

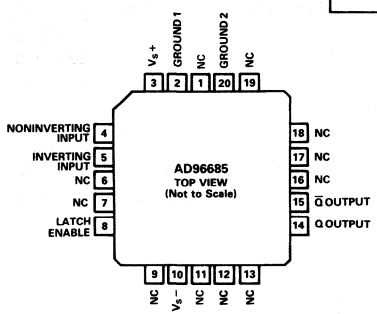
AD96685BQ/TQ/BR



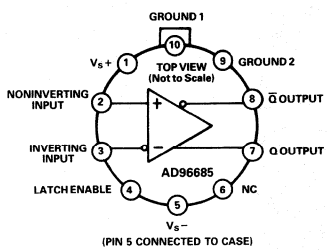
AD96687BQ/TQ/BR



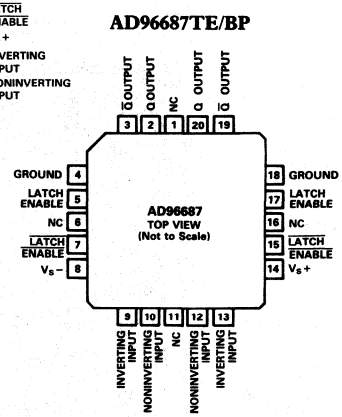
AD96685TE/BP



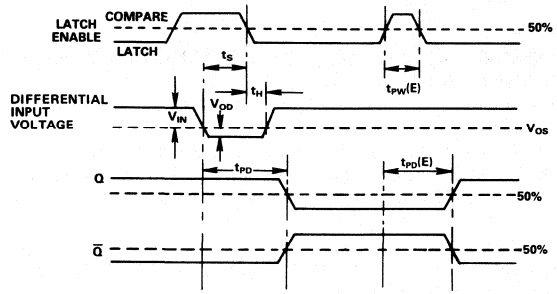
AD96685BH/TH



AD96687TE/BP

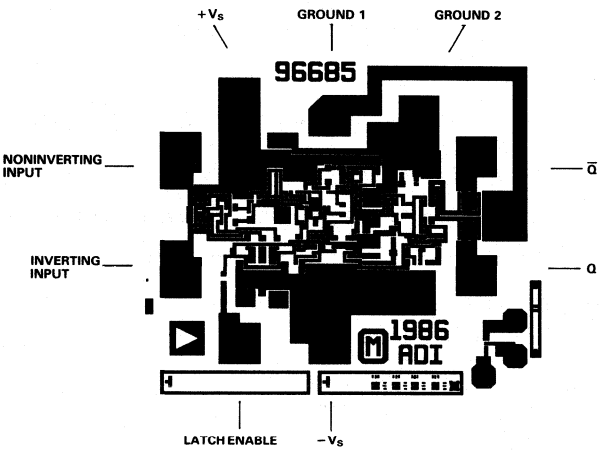


SYSTEM TIMING DIAGRAM

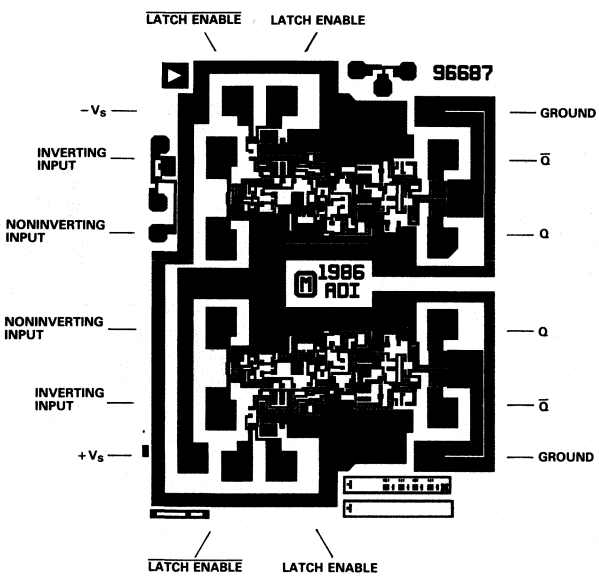


t_S	–	Minimum Setup Time
t_H	–	Minimum Hold Time
t_{PD}	–	Input to Output Delay
$t_{PD}(E)$	–	LATCH ENABLE to Output Delay
$t_{PW}(E)$	–	Minimum LATCH ENABLE Pulse Width
V_{OS}	–	Input Offset Voltage
V_{OD}	–	Overdrive Voltage

DIE LAYOUT AND MECHANICAL INFORMATION



Die Dimensions	AD96685	44 × 50 × 15 (± 2) mils
Pad Dimensions		4 × 4 mils
Metalization		Aluminum
Backing		None
Substrate Potential		–Vs
Passivation		Oxynitride
Die Attach		Gold Eutectic
Bond Wire		1.25 mil, Aluminum; Ultrasonic Bonding or 1mil, Gold, Gold Ball Bonding



Die Dimensions	AD96687	77 × 60 × 15 (± 2) mils
Pad Dimensions		4 × 4 mils
Metalization		Aluminum
Backing		None
Substrate Potential		–Vs
Passivation		Oxynitride
Die Attach		Gold Eutectic
Bond Wire		1.25 mil, Aluminum; Ultrasonic Bonding or 1mil, Gold, Gold Ball Bonding

ORDERING GUIDE

Device	Type	Temperature Range	Description	Package Options*
AD96685BH	Single	−25°C to +85°C	10-Pin Can, Industrial	H-10A
AD96685BP	Single	−25°C to +85°C	20-Pin PLCC, Industrial	P-20A
AD96685BQ	Single	−25°C to +85°C	16-Pin DIP, Industrial	Q-16
AD96685BR	Single	−25°C to +85°C	16-Pin SOIC, Industrial	R-16
AD96685TE	Single	−55°C to +125°C	20-Pin LCC, Extended Temperature	E-20A
AD96685TH	Single	−55°C to +125°C	10-Pin Can, Extended Temperature	H-10A
AD96685TQ	Single	−55°C to +125°C	16-Pin DIP, Extended Temperature	Q-16
AD96687BP	Dual	−25°C to +85°C	20-Pin PLCC, Industrial	P-20A
AD96687BQ	Dual	−25°C to +85°C	16-Pin DIP, Industrial	Q-16
AD96687BR	Dual	−25°C to +85°C	16-Pin SOIC, Industrial	R-16
AD96687TE	Dual	−55°C to +125°C	20-Pin LCC, Extended Temperature	E-20A
AD96687TQ	Dual	−55°C to +125°C	16-Pin DIP, Extended Temperature	Q-16

*For outline information see Package Information section.

APPLICATIONS INFORMATION

The AD96685/87 comparators are very high speed devices. Consequently, high speed design techniques must be employed to achieve the best performance. The most critical aspect of any AD96685/87 design is the use of a low impedance ground plane.

Another area of particular importance is power supply decoupling. Normally, both power supply connections should be separately decoupled to ground through 0.1μF ceramic and 0.001μF mica capacitors. The basic design of comparator circuits makes the negative supply somewhat more sensitive to variations. As a result more attention should be placed on insuring a "clean" negative supply.

The LATCH ENABLE input is active LOW (latched). If the latching function is not used, the LATCH ENABLE input should be grounded (ground is an ECL logic HIGH). The LATCH ENABLE input of the AD96687 should be tied to −2.0V or left "floating," to disable the latching function. An alternate use of the LATCH ENABLE input is as a hysteresis control input. By varying the voltage at the LATCH ENABLE input for the AD96685 and the differential voltage between both latch inputs for the AD96687, small variations in the hysteresis can be achieved.

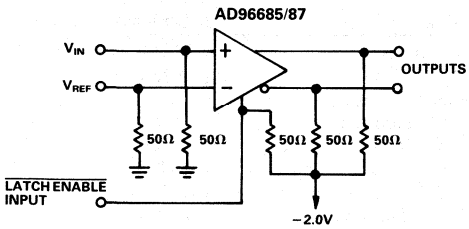
Occasionally, one of the two comparator stages within the AD96687 will not be used. The inputs of the unused comparator should not be allowed to "float." The high internal gain may cause the output to oscillate (possibly affecting the other comparator which is being used) unless the output is forced into a fixed state. This is easily accomplished by insuring that the two inputs are at least one diode drop apart, while also grounding the LATCH ENABLE input.

The best performance will be achieved with the use of proper ECL terminations. The open-emitter outputs of the AD96685/87 are designed to be terminated through 50Ω resistors to −2.0V, or any other equivalent ECL termination. If high speed ECL signals must be routed more than a few centimeters, MicroStrip or StripLine techniques may be required to insure proper transition times and prevent output ringing.

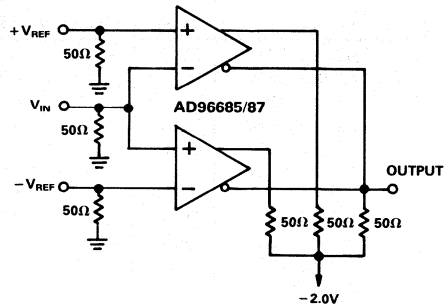
The AD96685/87 have been specifically designed to reduce propagation delay dispersion over an input overdrive range of 100mV to 1V. Propagation delay dispersion is the change in propagation delay which results from a change in the degree of overdrive (how far the switching point is exceeded by the input). The overall result is a higher degree of timing accuracy since the AD96685/87 is far less sensitive to input variations than most comparator designs.

AD96685/AD96687—Typical Applications

HIGH SPEED SAMPLING CIRCUIT



HIGH SPEED WINDOW COMPARATOR



ANALOG DEVICES

Fast Precision Comparator

CMP-01

FEATURES

- Fast Response Time ..... 180ns Max
- High Input Slew Rate 92V/μs
- Low Offset Voltage ..... 0.3mV Typical, 0.8mV Max
- Low Offset Current ..... 4nA Typical, 25nA Max
- Low Offset Drift ..... 1μV/°C, 30pA/°C
- Standard Power Supplies ..... +5V or ±5V to ±18V
- Guaranteed Operation from Single +5V Supply
- No Pull-Up Resistor Required for TTL Drive
- Wired OR Capability
- Fits 111, 106, 710 Sockets
- Easy Offset Nulling ..... Single 2kΩ Potentiometer
- Easy to Use ..... Free from Oscillations
- Available in Die Form

GENERAL DESCRIPTION

The CMP-01 is a monolithic fast precision voltage comparator using an advanced NPN-Schottky Barrier Diode process. It features fast response time to both large and small input signals, while maintaining excellent input characteristics. The CMP-01 is capable of operating over a wide range of supply voltages including single ended 5 volt supply. The large output current sinking and high output voltage capability assure good application flexibility, while the combination of fast response, high accuracy, and freedom from oscillation assure performance in precision level detectors and 12 and 13-bit A/D converters. The CMP-01 is pin-compatible to earlier 111, 106, and 710 types. For applications requiring lower input offset and bias currents, refer to the CMP-02 data sheet.

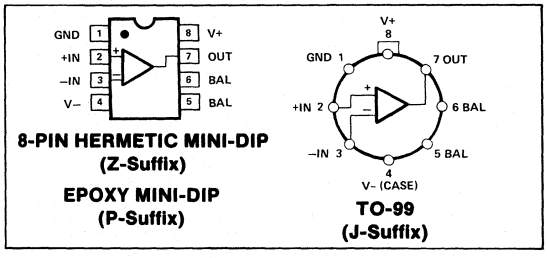
ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (mV)	PACKAGE TO-99	PACKAGE CERDIP 8-PIN	PACKAGE PLASTIC 8-PIN	OPERATING TEMPERATURE RANGE
0.8	CMP01J*	CMP01Z/883	–	MIL
0.8	CMP01EJ	CMP01EZ	CMP01EP	COM
2.8	CMP01CJ	CMP01CZ	CMP01CP	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

PIN CONNECTIONS

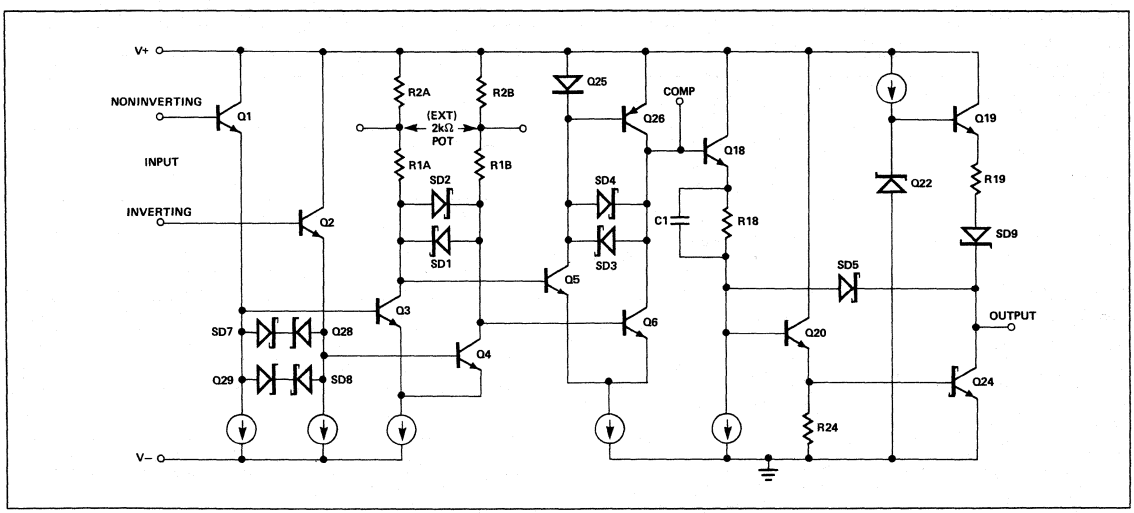


8-PIN HERMETIC MINI-DIP (Z-Suffix)

EPOXY MINI-DIP (P-Suffix)

TO-99 (J-Suffix)

SIMPLIFIED SCHEMATIC



CMP-01

ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage, V+ to V– 36V
Output to Ground ..... –5V to +32V
Output to Negative Supply Voltage 50V
Ground to Negative Supply Voltage 30V
Positive Supply Voltage to Ground ..... +30V
Positive Supply Voltage to Offset Null ..... 0 to 2V
Differential Input Voltage ..... ±11V
Input Voltage (V_S = ±15V) ..... ±15V
Output Sink Current (Continuous Operation) 75mA
Operating Temperature Range
CMP-01 ..... –55°C to +125°C
CMP-01E, CMP-01C ..... 0°C to +70°C
Junction Temperature (T_j) ..... –65°C to +150°C
Storage Temperature Range ..... –65°C to +150°C
P-Suffix ..... –65°C to +125°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
Output Short-Circuit Duration
To Ground ..... Indefinite
To V+ ..... 1 Minute

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Plastic DIP (P)	148	16	°C/W
8-Pin SO (S)	103	43	°C/W

NOTES:
1. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO and P-DIP packages.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted.

			CMP-01 CMP-01E			CMP-01C			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \le 5k\Omega$, (Note 1)	—	0.3	0.8	—	0.4	2.8	mV
Input Offset Current	I_{OS}	(Note 1)	—	4	25	—	5	80	nA
Input Bias Current	I_B		—	350	600	—	400	900	nA
Differential Input Resistance	R_{IN}	(Note 2)	150	300	—	100	200	—	kΩ
Voltage Gain	A_V	V_O = 0.4V to 2.4V, (Notes 1, 2)	200	500	—	100	500	—	V/mV
Response Time (Note 3)	t_r	100mV step, 5mV Overdrive							ns
		No Load (No Pull-Up)	—	110	180	—	110	180	
		5kΩ to 5v (Pull-Up)	—	110	—	—	110	—	
		TTL Fan-Out = 4, No Pull-Up	—	110	—	—	110	—	
		5V Step 5mV Overdrive							
		No Load (No Pull-Up)	—	160	—	—	160	—	
		5kΩ to 5v (Pull-Up)	—	160	—	—	160	—	
		TTL Fan-Out = 4, No Pull-Up	—	160	—	—	160	—	
Input Slew Rate			—	92	—	—	92	—	V/μs
Input Voltage Range	CMVR		±12.5	±13	—	±12.5	±13	—	V
Common-Mode Rejection Ratio	CMRR		94	110	—	90	110	—	dB
Power Supply Rejection Ratio	PSRR	$5V \le V_{S+} \le 18V$, $-18V \le V_{S-} \le 0V$	80	100	—	74	98	—	dB
Positive Output Voltage	V_{OH}	$V_{IN} \ge 3mV$, I_O = 320μA	2.4	3.2	—	—	—	—	V
		$V_{IN} \ge 3mV$, I_O = 240μA	—	—	—	2.4	3.4	—	
		$V_{IN} \ge 3mV$, I_O = 0mA	2.4	4.8	—	2.4	4.8	—	
Saturation Voltage	V_{OL}	$V_{IN} \le -10mV$, I_{sink} = 0mA	—	0.16	0.4	—	0.16	0.4	V
		$V_{IN} \le -10mV$, $I_{sink} \le 6.4mA$	—	0.3	0.45	—	0.31	0.45	
		$V_{IN} \le -10mV$, $I_{sink} \le 12mA$ (CMP-01 only)	—	0.36	0.5	—	—	—	
Output Leakage Current	I_{LEAK}	$V_{IN} \ge 10mV$, V_O = +30V	—	0.03	2	—	0.05	8	μA
Positive Supply Current	I+	$V_{IN} \le -10mV$	—	5.6	8	—	5.6	8.5	mA
Negative Supply Current	I–	$V_{IN} \le -10mV$	—	1.3	2.2	—	1.3	2.2	mA
Power Dissipation	P_d	$V_{IN} \le -10mV$	—	103	153	—	103	161	mW
Offset Voltage Adjustment Range		Nulling Pot ≥ 2kΩ	—	±5	—	—	±5	—	mV

NOTES:
1. These parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1kΩ load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.
2. Guaranteed by design.
3. Sample tested.

ELECTRICAL CHARACTERISTICS at $V_{S+} = 5V$, $V_{S-} = 0V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-01 / CMP-01E MIN	CMP-01 / CMP-01E TYP	CMP-01 / CMP-01E MAX	CMP-01C MIN	CMP-01C TYP	CMP-01C MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$, (Note 1)	—	0.4	1.5	—	0.5	3.5	mV
Input Offset Current	I_{OS}	(Note 1)	—	3	21	—	4	65	nA
Input Bias Current	I_B		—	250	500	—	300	720	nA
Voltage Gain	A_V	$V_O = 0.4V$ to 2.4V, (Notes 1, 2)	—	50	—	—	50	—	V/mV
Response Time	t_r	100mV Step, 5mV Overdrive 5kΩ to 5V (Pull-Up) TTL Fan-Out = 4, 5kΩ to 5V (Pull-Up)	— —	150 150	— —	— —	150 150	— —	ns
Input Voltage Range	CMVR		1.8	1.7-3.8	3.5	1.8	1.7-3.8	3.5	V
Saturation Voltage	V_{OL}	$V_{IN} \leq -10mV$, $I_{sink} \leq 6.4mA$	—	0.3	0.45	—	0.3	0.45	V
Positive Supply Current	I+	$V_{IN} \leq -10mV$	—	2.3	3.2	—	2.4	3.8	mA
Power Dissipation	P_d	$V_{IN} \leq -10mV$	—	11.5	16	—	12	19	mW

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq 125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-01 MIN	CMP-01 TYP	CMP-01 MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$, (Note 1) $V_{S+} = 5V$, $V_{S-} = 0V$, (Note 1)	— —	0.5 0.6	1.6 2.8	mV
Average Input Offset Voltage Drift Without External Trim With External Trim	 TCV_{OS} TCV_{OSn}	 $R_S = 50\Omega$	 — —	 1.5 1	 — —	 µV/°C
Input Offset Current	I_{OS}	$T_A = +125°C$, (Note 1) $T_A = -55°C$, (Note 1)	— —	4 5	25 45	nA
Average Input Offset Current Drift	TCI_{OS}	$+25°C \leq T_A \leq +125°C$ $-55°C \leq T_A \leq +25°C$	— —	12 35	— —	pA/°C
Input Bias Current	I_B	$T_A = +125°C$ $T_A = -55°C$	— —	330 550	600 1400	nA
Voltage Gain	A_V	$V_O = 0.4V$ to 2.4V, (Notes 1, 2)	100	500	—	V/mV
Response Time	t_r	100mV Step, 5mV Overdrive, (Note 2) $T_A = +125°C$, No Load $T_A = -55°C$, No Load	 —	220 100	— —	ns
Input Voltage Range	CMVR		±12	±13	—	V
Common-Mode Rejection Ratio	CMRR		88	106	—	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{S+} \leq 15V$, $-15V \leq V_{S-} \leq 0V$	75	96	—	dB
Positive Output Voltage	V_{OH}	$V_{IN} \geq 4mV$, $I_O = 200\mu A$	2.4	3	—	V
Saturation Voltage	V_{OL}	$V_{IN} \leq -10mV$, $I_{sink} = 0mA$ $V_{IN} \leq -10mV$, $I_{sink} = 6.4mA$	— —	0.20 0.32	0.4 0.5	V

NOTES:
1. These parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1kΩ load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.
2. Guaranteed by design.

CMP-01

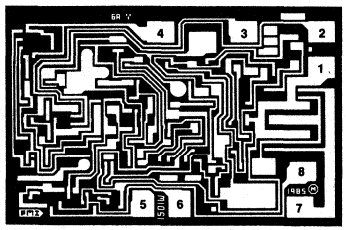
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0°C \leq T_A \leq 70°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-01E MIN	CMP-01E TYP	CMP-01E MAX	CMP-01C MIN	CMP-01C TYP	CMP-01C MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$, (Note 1)	—	0.4	1.4	—	0.5	3.5	mV
		$V_{S+} = 5V$, $V_{S-} = 0V$, (Note 1)	—	0.5	2.4	—	0.6	4.3	
Average Input Offset Voltage Drift									
Without External Trim	TCV_{OS}	$R_S = 50\Omega$	—	1.5	—	—	1.8	—	$\mu V/°C$
With External Trim	TCV_{OSn}		—	1.0	—	—	1.2	—	
Input Offset Current	I_{OS}	$T_A = +70°C$, (Note 1)	—	4	25	—	5	80	nA
		$T_A = 0°C$, (Note 1)	—	5	45	—	6	120	
Average Input Offset Current Drift	TCI_{OS}	$+25°C \leq T_A \leq +70°C$	—	12	—	—	12	—	pA/°C
		$0°C \leq T_A \leq +25°C$	—	35	—	—	40	—	
Input Bias Current	I_B	$T_A = +70°C$	—	330	600	—	340	900	nA
		$T_A = 0°C$	—	400	950	—	450	1200	
Voltage Gain	A_V	$V_O = 0.4V$ to $2.4V$, (Notes 1, 2)	100	500	—	70	500	—	V/mV
Response Time	t_r	100mV Step, 5mV Overdrive							
		$T_A = +70°C$, No Load	—	150	—	—	150	—	ns
		$T_A = 0°C$, No Load	—	100	—	—	100	—	
Input Voltage Range	CMVR		±12.0	±13.3	—	±12.0	±13.3	—	V
Common-Mode Rejection Ratio	CMRR		90	108	—	86	108	—	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{S+} \leq 15V$, $-15V \leq V_{S-} \leq 0V$	77	98	—	70	88	—	dB
Positive Output Voltage	V_{OH}	$V_{IN} \geq 4mV$, $I_O = 200\mu A$	2.4	3.2	—	2.4	3.2	—	V
Saturation Voltage	V_{OL}	$V_{IN} \leq -10mV$, $I_{sink} = 0$	—	0.17	0.4	—	0.17	0.4	V
		$V_{IN} \leq -10mV$, $I_{sink} = 6.4mA$	—	0.3	0.5	—	0.31	0.5	

NOTES:

1. These parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1kΩ load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.
2. Guaranteed by design.

DICE CHARACTERISTICS



DIE SIZE 0.065 × 0.043 inch, 2730 sq. mils
(1.651 × 1.092 mm, 1.803 sq. mm)

1. GROUND
2. NONINVERTING INPUT
3. INVERTING INPUT
4. NEGATIVE SUPPLY (SUBSTRATE)
5. BALANCE
6. BALANCE
7. OUTPUT
8. POSITIVE SUPPLY

3

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$.

PARAMETER	SYMBOL	CONDITIONS	CMP-01N LIMIT	CMP-01GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$, (Note 1)	0.8	2.8	mV MAX
Input Offset Current	I_{OS}	(Note 1)	25	80	nA MAX
Input Bias Current	I_B		600	900	nA MAX
Differential Input Resistance	R_{IN}	(Note 2)	150	100	kΩ MIN
Input Voltage Range	CMVR		±12.5	±12.5	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm$CMVR	94	90	dB MIN
Power Supply Rejection Ratio	PSRR	$5V \leq V_S+ \leq 18V$ $-18V \leq V_S- \leq 0V$	80	74	dB MIN
Positive Output Voltage	V_{OH}	$V_{IN} \geq 3mV$, $I_O = 320\mu A$ $V_{IN} \geq 3mV$, $I_O = 240\mu A$	2.4 —	— 2.4	V MIN
Saturation Voltage	V_{OL}	$I_{sink} = 6.4mA$	0.45	0.45	V MAX
Output Leakage Current	I_{LEAK}	$V_{IN} \geq 10mV$, $V_O = 30V$	2	8	μA MAX
Positive Supply Current	I+	$V_{IN} \leq -10mV$	8.0	8.5	mA MAX
Negative Supply Current	I−	$V_{IN} \leq -10mV$	2.2	2.2	mA MAX
Power Consumption	P_d	$V_{IN} \leq -10mV$	153	161	mW MAX

NOTES:
1. These parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1kΩ load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.
2. Guaranteed by design.

WAFER TEST LIMITS at $V_S+ = 5V$ and $V_S- = 0V$, $T_A = 25°C$.

PARAMETER	SYMBOL	CONDITIONS	CMP-01N LIMIT	CMP-01GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$, (Note 1)	1.5	3.5	mV MAX
Input Offset Current	I_{OS}		21	65	nA MAX

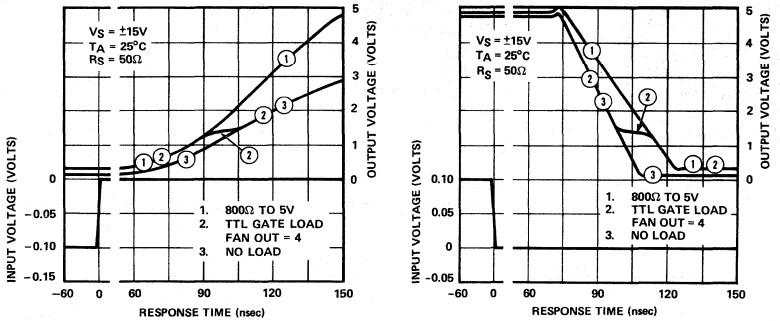
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, and 25°C.

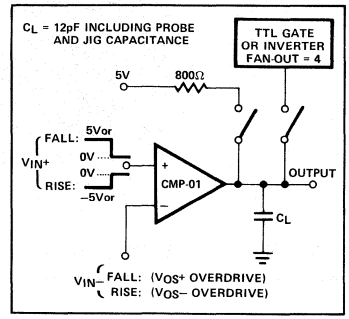
PARAMETER	SYMBOL	CONDITIONS	CMP-01N TYPICAL	CMP-01GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	1.5	1.8	μV/°C
Average Input Offset Current Drift	TCI_{OS}		35	40	pA/°C
Response Time	t_r	100mV Step, 5mV Overdrive No Load (No Pull-Up), $T_A = 25°C$	110	110	ns

TYPICAL PERFORMANCE CHARACTERISTICS

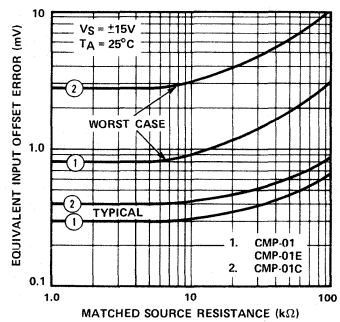
RESPONSE TIME, 100mV STEP, 5mV OVERDRIVE, VARIOUS LOADS



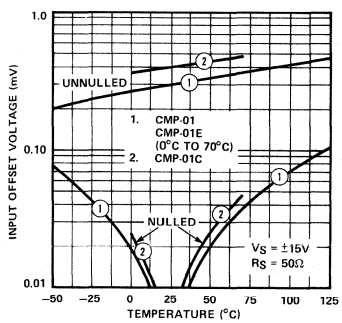
RESPONSE TIME TEST CIRCUIT



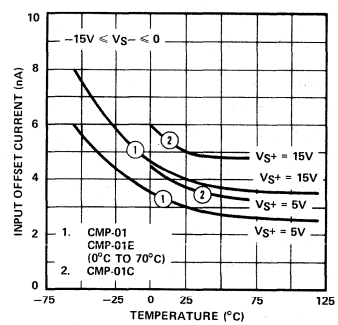
INPUT OFFSET ERROR vs SOURCE RESISTANCE



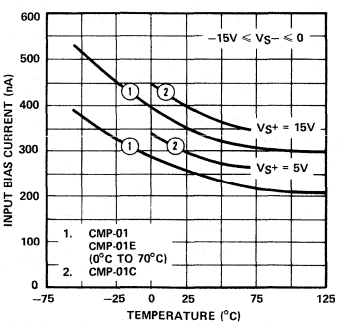
OFFSET VOLTAGE vs TEMPERATURE



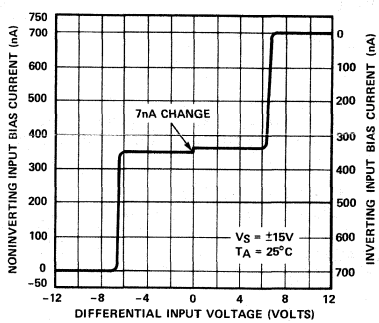
INPUT OFFSET CURRENT vs TEMPERATURE



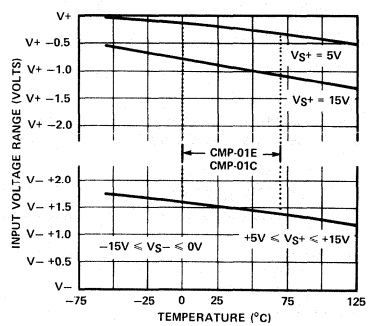
INPUT BIAS CURRENT vs TEMPERATURE



INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE

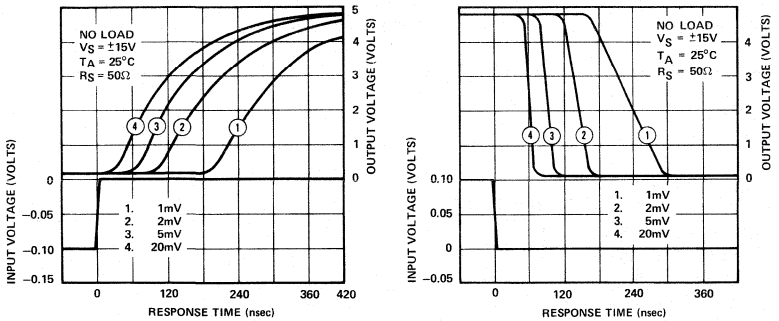


INPUT VOLTAGE RANGE vs TEMPERATURE

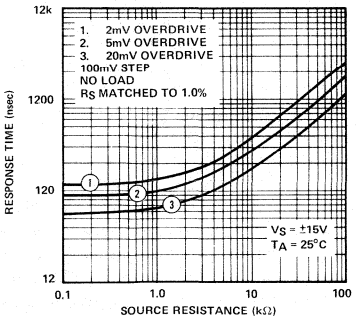


TYPICAL PERFORMANCE CHARACTERISTICS

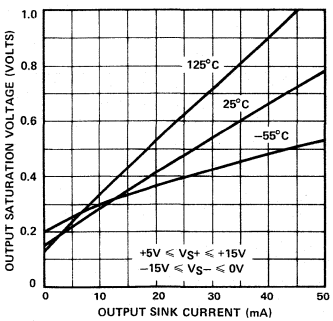
RESPONSE TIME FOR 100mV STEP AND VARIOUS INPUT OVERDRIVES



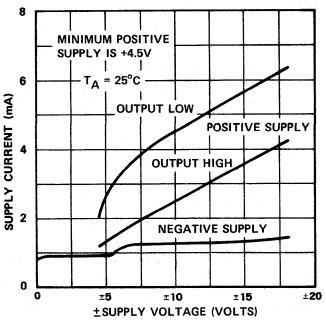
RESPONSE TIME vs SOURCE RESISTANCE



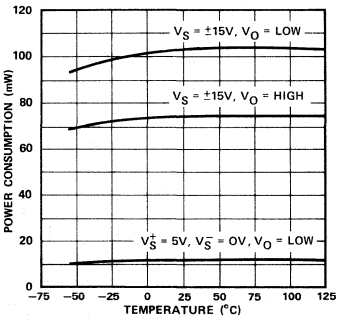
SATURATION VOLTAGE vs SINK CURRENT



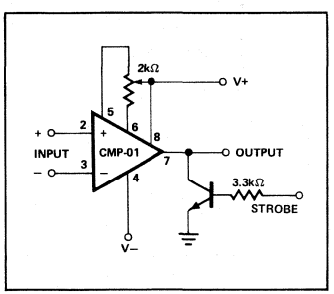
SUPPLY CURRENT vs SUPPLY VOLTAGE



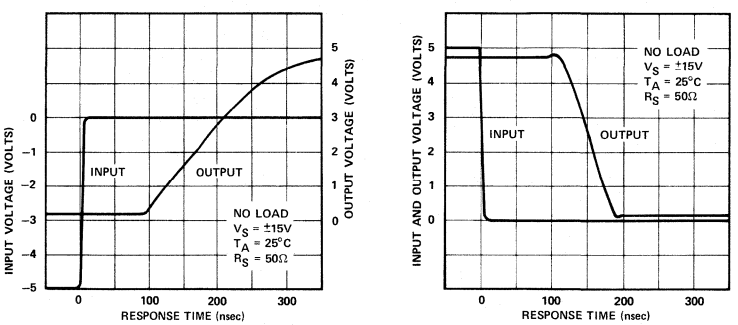
POWER CONSUMPTION vs TEMPERATURE



OFFSET TRIMMING AND STROBE CIRCUIT



RESPONSE TIME FOR 5V STEP AND 5mV OVERDRIVE



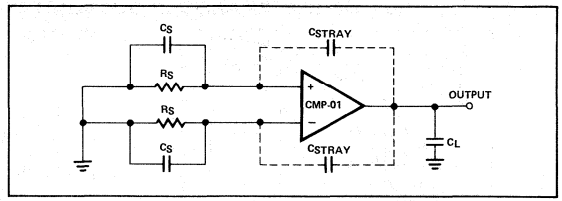
APPLICATIONS INFORMATION

The CMP-01 provides fast response times even with small overdrives; to achieve this performance requires very high gain at high frequencies. The CMP-01 is completely free of oscillations; however, small values of stray capacitance from output to input when combined with high-source resistances can cause an unstable condition. DC characteristics are not affected, but when the input is within a few microvolts of the transition level, certain conditions can create an oscillation region. The width of this oscillatory region and the size of source resistance where oscillations begin is a strong function of the stray coupling present. The following suggestions are offered as a guide towards minimizing the conditions for oscillation: matched source resistors, minimized stray capacitances (e.g., a ground plane between output and input), or capacitive output loading (C_L). The capacitive loading techniques will eliminate the oscillations, but result in slower response time. Matched bypass capacitors across the input resistors also can eliminate the instability,

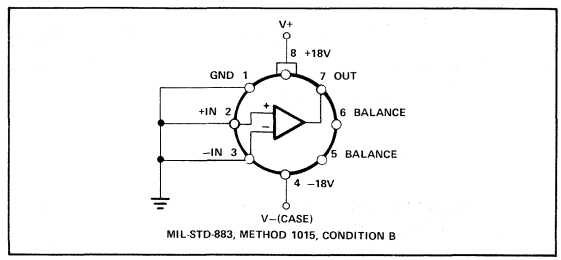
$$\text{and if } C_S \geq 20\text{pF}\left(\frac{\text{maximum step size}}{\text{minimum overdrive}}\right)$$

the response time will approximate the response time for low values of R_S. It should be noted that the offset nulling terminals do not require bypassing for stability. As with all wideband circuits, it is recommended that the supplies be bypassed near the socket of the device.

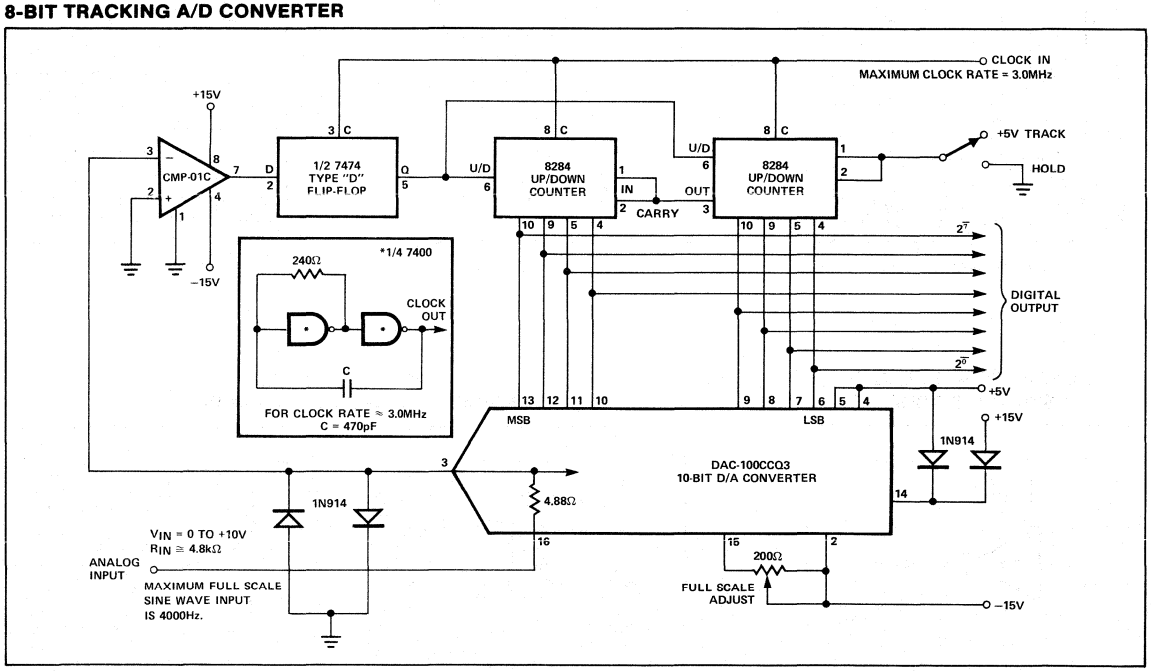
MINIMIZING OSCILLATION



BURN-IN CIRCUIT



8-BIT TRACKING A/D CONVERTER



ANALOG DEVICES

Low Input Current Precision Comparator

CMP-02

FEATURES

- **Low Offset Voltage** ..... **0.3mV Typ, 0.8mV Max**
- **Low Offset Current** ..... **0.3nA Typ, 3nA Max**
- **Low Bias Current** ..... **28nA Typ, 50nA Max**
- **Low Offset Drift** ..... **1μV/°C, 4pA/°C**
- **High Gain** ..... **200,000 Min**
- **High CMRR** ..... **110dB Typ, 94dB Min**
- **High Input Impedance** **16MΩ**
- **Fast Response Time** ..... **190ns Typ, 270ns Max**
- **Standard Power Supplies** ..... **+5V or ±5V to ±18V**
- **Guaranteed Operation from Single +5V**
- **No Pull-Up Resistor Required for TTL Drive**
- **Wired OR Capability**
- **Fits 111, 106, 710 Sockets**
- **Easy Offset Nulling** ..... **Single 2kΩ Potentiometer**
- **Easy to Use** ..... **Free from Oscillations**
- **Available in Die Form**

ORDERING INFORMATION †

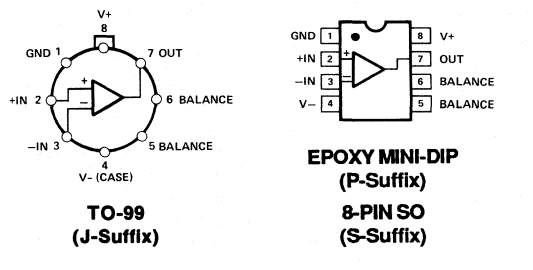
T_A = +25°C V_{OS} MAX (mV)	PACKAGE TO-99	PLASTIC 8-PIN	SO 8-PIN	OPERATING TEMPERATURE RANGE
0.8	–	CMP02EP	–	COM
2.8	CMP02CJ	CMP02CP	CMP02CS	XIND

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

The CMP-02 is a monolithic low input current comparator using an advanced NPN-Schottky Barrier Diode process. It features superior input characteristics with extremely low offset voltage, offset current, bias current and temperature drift. High common-mode and power supply rejection plus good response time contribute to excellent performance in the most demanding applications. The balanced offset nulling, large output drive, and wired-OR capability combined with internal pull-up maximize application convenience. The CMP-02 is capable of operating over a wide range of supply voltages, including single plus 5 volt supply operation, and is pin-compatible to earlier 111, 106, and 710 types. For applications requiring faster response time, please refer to the CMP-01 fast precision comparator data sheet.

PIN CONNECTIONS

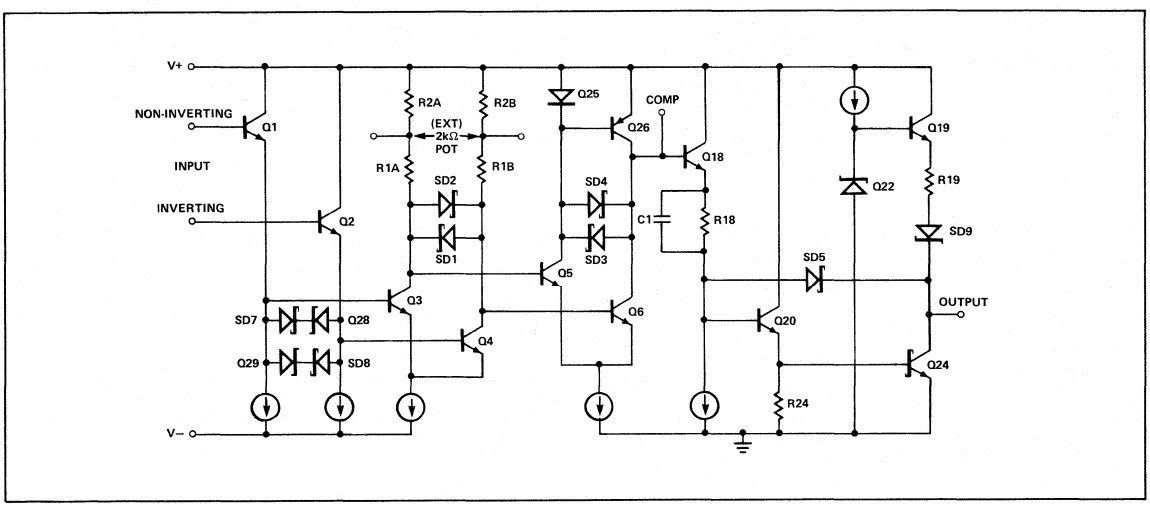


TO-99 (J-Suffix)

EPOXY MINI-DIP (P-Suffix)

8-PIN SO (S-Suffix)

SIMPLIFIED SCHEMATIC



CMP-02

ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage, V+ to V– 36V
Output to Ground ..... –5V to +32V
Output to Negative Supply Voltage 50V
Ground to Negative Supply Voltage 30V
Positive Supply Voltage to Ground 30V
Positive Supply Voltage to Offset Null ..... 0 to 2V
Differential Input Voltage ..... ±11V
Input Voltage (V_S = ±15V) ..... ±15V
Output Sink Current (Continuous Operation) 75mA
Operating Temperature Range
  CMP-02E ..... 0°C to +70°C
  CMP-02C ..... –40°C to +85°C
Junction Temperature (T_J) ..... –65°C to +150°C
Storage Temperature Range ..... –65°C to +150°C
  P-Suffix ..... –65°C to +125°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
Output Short-Circuit Duration
  To Ground ..... Indefinite
  To V+ ..... 1 Minute

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted.

			CMP-02E			CMP-02C			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \le 5k\Omega$, (Note 1)	—	0.3	0.8	—	0.4	2.8	mV
Input Offset Voltage	V_{OS}	$R_S \le 50k\Omega$, (Note 1)	—	0.3	0.9	—	0.4	3	mV
Input Offset Current	I_{OS}	(Note 1)	—	0.3	3.0	—	0.4	15	nA
Input Bias Current	I_B		—	28	50	—	35	100	nA
Differential Input Resistance	R_{IN}	(Note 2)	1.7	3	—	0.9	2	—	MΩ
Voltage Gain	A_V	V_O = 1 to 3V, (Note 2)	200	500	—	100	500	—	V/mV
Response Time (Note 3)	t_r	100mV step, 5mV Overdrive							
		No Load (No Pull-Up)	—	190	270	—	190	270	ns
		5kΩ to 5V (Pull-Up)	—	190	—	—	190	—	ns
		TTL Fan-Out = 4, No Pull-Up	—	190	—	—	190	—	ns
Input Slew Rate			—	15	—	—	15	—	V/μs
Input Voltage Range	CMVR		±12.5	±13.0	—	±12.5	±13.0	—	V
Common-Mode Rejection Ratio	CMRR		94	110	—	90	110	—	dB
Power Supply Rejection Ratio	PSRR	$5V \le V_{S+} \le 18V$, $-18V \le V_{S-} \le 0V$	80	100	—	74	98	—	dB
Positive Output Voltage	V_{OH}	$V_{IN} \ge 3mV$, $I_O = 320\mu A$	2.4	3.2	—	—	—	—	V
		$V_{IN} \ge 3mV$, $I_O = 240\mu A$	—	—	—	2.4	3.4	—	V
		$V_{IN} \ge 3mV$, $I_O = 0mA$	2.4	4.8	—	2.4	4.8	—	V
Saturation Voltage	V_{OL}	$V_{IN} \le -10mV$, $I_{sink} = 0mA$	—	0.16	0.40	—	0.16	0.40	V
		$V_{IN} \le -10mV$, $I_{sink} \le 6.4mA$	—	0.3	0.45	—	0.31	0.45	V
		$V_{IN} \le -10mV$, $I_{sink} \le 12mA$ (CMP-02 only)	—	0.36	0.5	—	—	—	V
Output Leakage Current	I_{LEAK}	$V_{IN} \ge 10mV$, V_O = +30V	—	0.03	2.0	—	0.05	8.0	μA
Positive Supply Current	I+	$V_{IN} \le -10mV$	—	5.5	8.0	—	5.6	8.5	mA
Negative Supply Current	I–	$V_{IN} \le -10mV$	—	1.1	2.2	—	1.2	2.2	mA
Power Dissipation	P_d	$V_{IN} \le -10mV$	—	99	153	—	102	161	mW
Offset Voltage Adjustment Range		Nulling Pot ≥ 2kΩ	—	±5	—	—	±5	—	mV

NOTES:
1. These Parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1kΩ load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.
2. Guaranteed by design.
3. Sample tested.

ELECTRICAL CHARACTERISTICS at $V_S = 5V$, $V_{S-} = 0V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-02E MIN	CMP-02E TYP	CMP-02E MAX	CMP-02C MIN	CMP-02C TYP	CMP-02C MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$, (Note 1)	—	0.4	1.5	—	0.5	3.5	mV
Input Offset Current	I_{OS}	(Note 1)	—	0.25	3	—	0.35	14	nA
Input Bias Current	I_B		—	24	45	—	30	90	nA
Voltage Gain	A_V	$V_O = 1$ to 3V	—	50	—	—	50	—	V/mV
Response Time	t_r	100mV Step, 5mV Overdrive							ns
		$5k\Omega$ to 5V (Pull-Up)	—	250	—	—	250	—	
		TTL Fan-Out = 4, $5k\Omega$ to 5V	—	250	—	—	250	—	
Input Voltage Range	CMVR		1.8-3.5	1.7-3.8	—	1.8-3.5	1.7-3.8	—	V
Saturation Voltage	V_{OL}	$V_{IN} \leq -3.5mV$, $I_{sink} \leq 6.4mA$	—	0.3	0.45	—	0.3	0.45	V
Positive Supply Current	I+	$V_{IN} \leq -10mV$	—	2.2	3	—	2.3	3.6	mA
Power Dissipation	P_d	$V_{IN} \leq -10mV$	—	11	15	—	11.5	18	mW

NOTE:
1. These Parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a $1k\Omega$ load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.

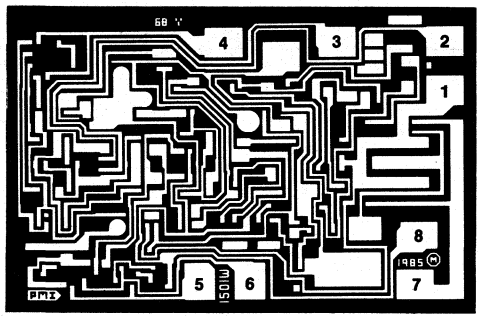
ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $0°C \leq T_A \leq +70°C$ for E Grade, $-40°C \leq T_A \leq +85°C$ for C Grade, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-02E MIN	CMP-02E TYP	CMP-02E MAX	CMP-02C MIN	CMP-02C TYP	CMP-02C MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$, (Note 1)	—	0.4	1.4	—	0.5	3.5	mV
		$V_{S+} = 5V$, $V_{S-} = 0V$, (Note 1)	—	0.5	2.4	—	0.6	4.3	
Average Input Offset Voltage Drift									
Without External Trim	TCV_{OS}	$R_S = 50\Omega$	—	1.5	—	—	1.8	—	µV/°C
With External Trim	TCV_{OSn}	$R_S = 50\Omega$	—	1	—	—	1.2	—	
Input Offset Current	I_{OS}	$T_A = +70°C$, (Note 1)	—	0.3	3	—	0.4	15	nA
		$T_A = 0°C$, (Note 1)	—	0.4	6	—	0.5	25	
Average Input Offset Current Drift	TCI_{OS}	$+25°C \leq T_A \leq +70°C$	—	2	—	—	3	—	pA/°C
		$0°C \leq T_A \leq +25°C$	—	4	—	—	5	—	
Input Bias Current	I_B	$T_A = +70°C$	—	26	50	—	33	100	nA
		$T_A = 0°C$	—	34	80	—	42	160	
Voltage Gain	A_V	$V_O = 1$ to 3V, (Note 2)	100	500	—	70	500	—	V/mV
Response Time	t_r	100mV Step, 5mV Overdrive							ns
		$T_A = +70°C$, No Load	—	225	—	—	225	—	
		$T_A = 0°C$, No Load	—	180	—	—	180	—	
Input Voltage Range	CMVR		±12.0	±13	—	±12	±13	—	V
Common-Mode Rejection Ratio	CMRR		90	108	—	86	108	—	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{S+} \leq 15V$, $-15V \leq V_{S-} \leq 0V$	77	98	—	70	88	—	dB
Positive Output Voltage	V_{OH}	$V_{IN} \geq 4mV$, $I_O = 200\mu A$	2.4	3.2	—	2.4	3.2	—	V
Saturation Voltage	V_{OL}	$V_{IN} \leq -10mV$, $I_{sink} = 0$	—	0.17	0.4	—	0.17	0.4	V
		$V_{IN} \leq -10mV$, $I_{sink} = 6.4mA$	—	0.30	0.5	—	0.31	0.5	

NOTES:
1. These Parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a $1k\Omega$ load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.
2. Guaranteed by design.

CMP-02

DICE CHARACTERISTICS



1. GROUND
2. NONINVERTING INPUT
3. INVERTING INPUT
4. NEGATIVE SUPPLY (SUBSTRATE)
5. BALANCE
6. BALANCE
7. OUTPUT
8. POSITIVE SUPPLY

DIE SIZE 0.065 × 0.043 inch, 2730 sq. mils
(1.651 × 1.094 mm, 1.806 sq. mm)

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$.

PARAMETER	SYMBOL	CONDITIONS	CMP-02N LIMIT	CMP-02GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$ $R_S \leq 50k\Omega$	0.8 0.9	2.8 3	mV MAX
Input Offset Current	I_{OS}		3	15	nA MAX
Input Bias Current	I_B		50	100	nA MAX
Differential Input Resistance	R_{IN}		1.7	0.9	MΩ MIN
Input Voltage Range	CMVR		±12.5	±12.5	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm$CMVR	94	90	dB MIN
Power Supply Rejection Ratio	PSRR	$5V \leq V_S+ \leq 18V$ $-18V \leq V_S- \leq 0V$	80	74	dB MIN
Positive Output Voltage	V_{OH}	$V_{IN} \geq 3mV$, $I_O = 320\mu A$ $V_{IN} \geq 3mV$, $I_O = 240\mu A$	2.4 —	— 2.4	V MIN
Saturation Voltage	V_{OL}	$I_{sink} = 6.4mA$	0.45	0.45	V MAX
Output Leakage Current	I_{LEAK}	$V_{IN} \geq 10mV$, $V_O = 30V$	2	8	μA MAX
Positive Supply Current	I+	$V_{IN} \leq -10mV$	8	8.5	mA MAX
Negative Supply Current	I−	$V_{IN} \leq -10mV$	2.2	2.2	mA MAX
Power Consumption	P_d	$V_{IN} \leq -10mV$	153	161	mW MAX

WAFER TEST LIMITS at $V_S+ = 5V$ and $V_S- = 0V$, $T_A = 25°C$.

PARAMETER	SYMBOL	CONDITIONS	CMP-02N LIMIT	CMP-02GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$	1.5	3.5	mV MAX
Input Offset Current	I_{OS}		3	14	nA MAX

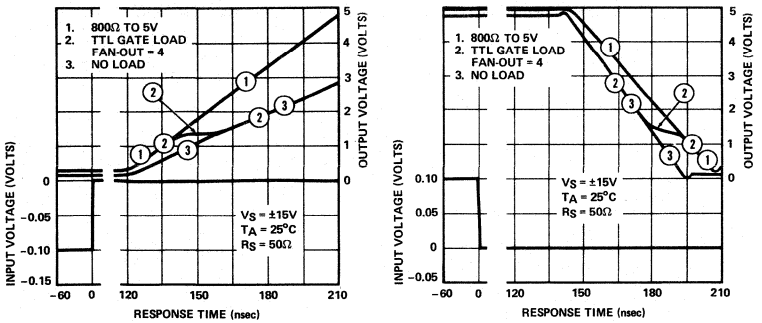
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$.

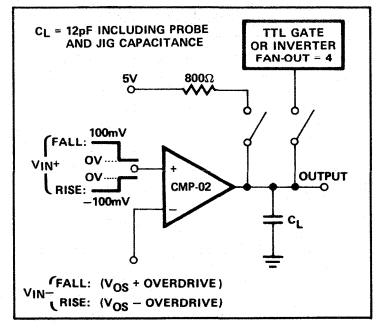
PARAMETER	SYMBOL	CONDITIONS	CMP-02N TYPICAL	CMP-02GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	1.5	1.8	μV/°C
Average Input Offset Current Drift	TCI_{OS}		4	5	pA/°C
Response Time	t_r	100mV Step, 5mV Overdrive No Load (No Pull-Up), $T_A = 25°C$	190	190	ns

TYPICAL PERFORMANCE CHARACTERISTICS

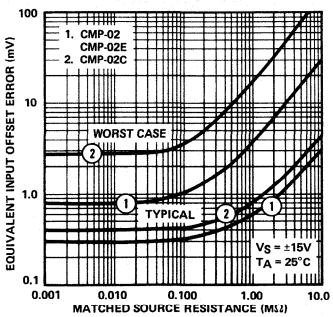
RESPONSE TIME, 100mV STEP, 5mV OVERDRIVE, VARIOUS LOADS



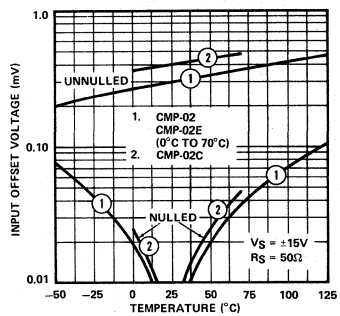
RESPONSE TIME TEST CIRCUIT



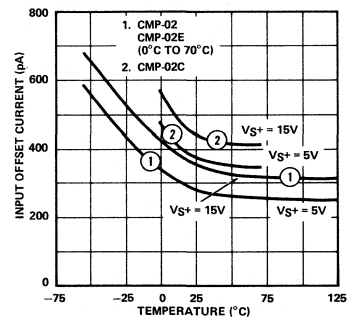
INPUT OFFSET ERROR vs SOURCE RESISTANCE



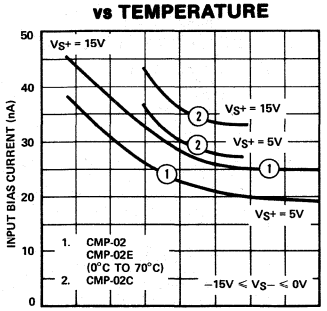
OFFSET VOLTAGE vs TEMPERATURE



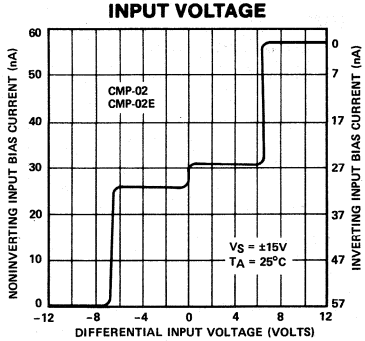
INPUT OFFSET CURRENT vs TEMPERATURE



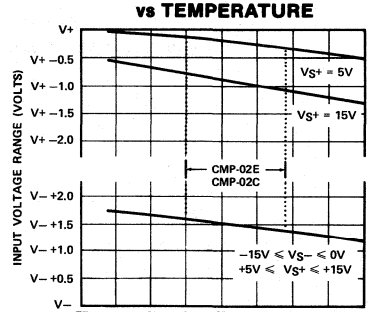
INPUT BIAS CURRENT vs TEMPERATURE



INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE

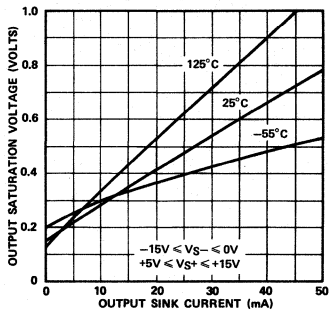


INPUT VOLTAGE RANGE vs TEMPERATURE

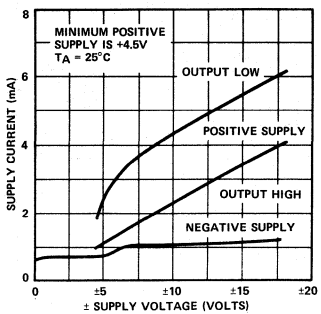


TYPICAL PERFORMANCE CHARACTERISTICS

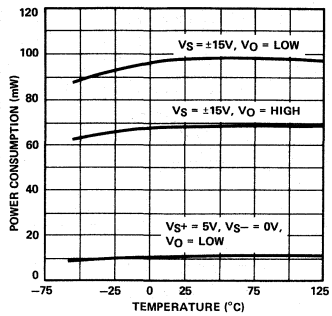
SATURATION VOLTAGE vs SINK CURRENT



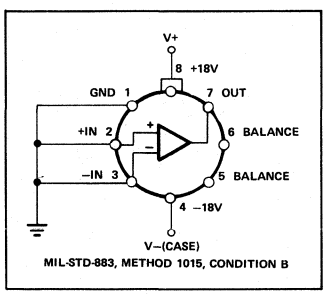
SUPPLY CURRENT vs SUPPLY VOLTAGE



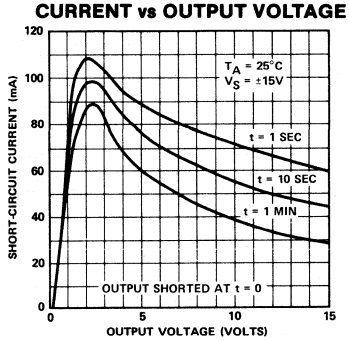
POWER CONSUMPTION vs TEMPERATURE



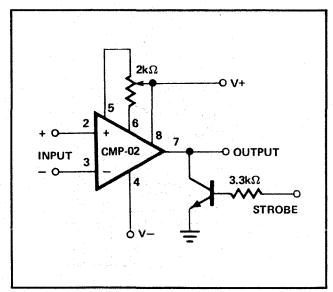
STANDARD BURN-IN CIRCUIT



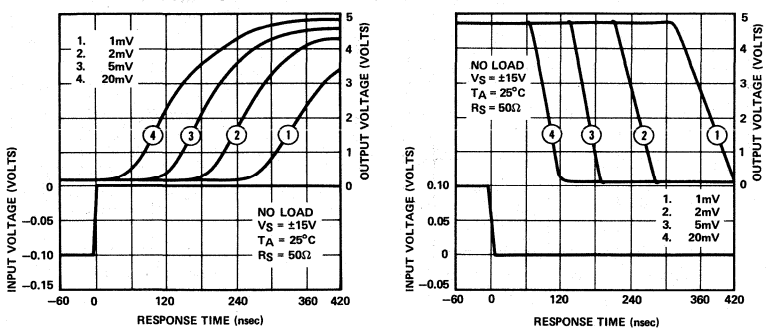
OUTPUT SHORT-CIRCUIT CURRENT vs OUTPUT VOLTAGE



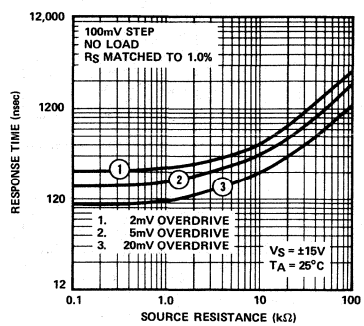
OFFSET TRIMMING AND STROBE CIRCUITS



RESPONSE TIME, 100mV STEP AND VARIOUS INPUT OVERDRIVES



RESPONSE TIME vs SOURCE RESISTANCE



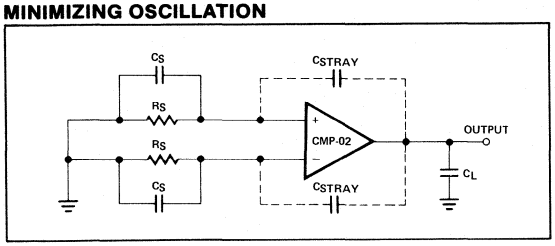
APPLICATIONS INFORMATION

The CMP-02 provides fast response times even with small overdrives; to achieve this performance requires very high gain at high frequencies. The CMP-02 is completely free of oscillations; however, small values of stray capacitance from output to input when combined with high-source resistances can cause an unstable condition. DC characteristics are not affected, but when the input is within a few microvolts of the transition level, certain conditions can create an oscillation region. The width of this oscillatory region and the size of source resistance where oscillations begin is a strong function of the stray coupling present. The following suggestions are offered as a guide towards minimizing the conditions for oscillation: matched source resistors, minimized stray capacitances (e.g., a ground plane between output and input), or capacitive output loading (C_L). The capacitive loading techniques will eliminate the oscillations, but result in slower response time. Matched bypass capacitors across the input resistors also can eliminate the instability,

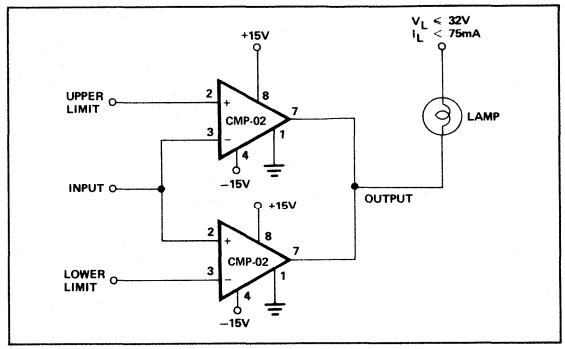
$$\text{and if } C_S \geq 20\text{pF}\left(\frac{\text{maximum step size}}{\text{minimum overdrive}}\right)$$

the response time will approximate the response time for low values of R_S. It should be noted that the offset nulling terminals do not require bypassing for stability. As with all wideband circuits, it is recommended that the supplies be bypassed near the socket of the device.

MINIMIZING OSCILLATION



PRECISION, DUAL LIMIT, GO/NO GO TESTER



3

ANALOG DEVICES

Quad Low-Power Precision Comparator

CMP-04

FEATURES

- **High Gain ..... 200V/mV Typ**
- **Single or Dual Supply Operation**
- **Input Voltage Range Includes Ground**
- **Low Power Consumption (1.5mW/Comparator)**
- **Low Input Bias Current ..... 100nA Max**
- **Low Input Offset Current ..... 10nA Max**
- **Low Offset Voltage ..... 1mV Max**
- **Low Output Saturation Voltage ..... 250mV @ 4mA**
- **Logic Output Compatible with TTL, DTL, ECL, MOS and CMOS**
- **Directly Replaces LM139/239/339 Comparators**
- **Available in Die Form**

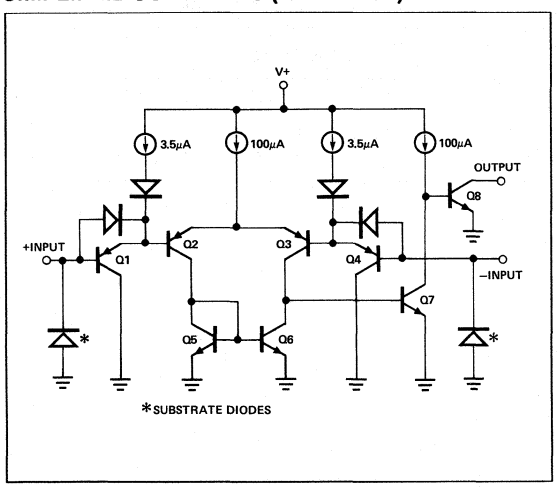
ORDERING INFORMATION †

T_A = +25°C V_{OS} (mV)	PACKAGE CERDIP 14-PIN	PACKAGE PLASTIC 14-PIN	PACKAGE SO 14-PIN	OPERATING TEMPERATURE RANGE
1	CMP04BY*	–	–	MIL
1	CMP04FY	CMP04FP	CMP04FS	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

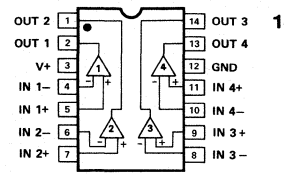
SIMPLIFIED SCHEMATIC (1/4 CMP-04)



GENERAL DESCRIPTION

Four precision independent comparators comprise the CMP-04. Performance highlights include a very low offset voltage, low output saturation voltage and high gain in a single supply design. The input voltage range includes ground for single supply operation and V– for split supplies. A low power supply current of 2mA, which is independent of supply voltage, makes this the preferred comparator for precision applications requiring minimal power consumption. Maximum logic interface flexibility is offered by the open-collector TTL output.

PIN CONNECTIONS

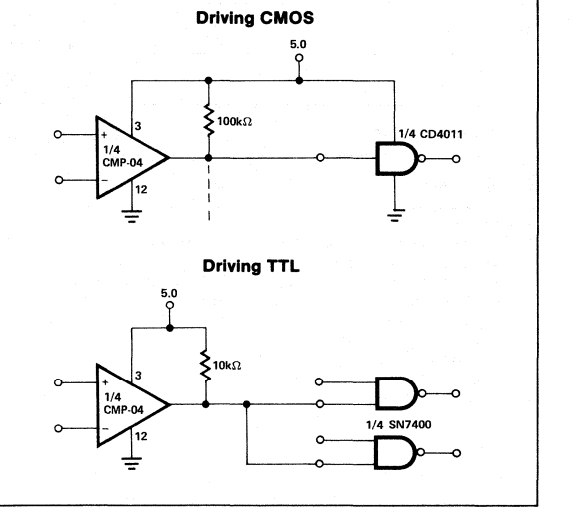


14-PIN HERMETIC DIP (Y-Suffix)

14-PIN EPOXY DIP (P-Suffix)

14-PIN SO (S-Suffix)

TYPICAL INTERFACE



CMP-04

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... 36V or ±18V
Differential Input Voltage ..... $36V_{DC}$
Input Voltage ..... –0.3V to +36V
Operating Temperature Range
CMP-04FY ..... –40°C to +85°C
CMP-04BY ..... –55°C to +125°C
CMP-04FP, FS ..... –40°C to +85°C
Junction Temperature (T_J) ..... –65°C to +150°C
Storage Temperature Range ..... –65°C to +150°C
P-Suffix) ..... –65°C to +125°C
Input Current (V_{IN} < –3.0V) 50mA
Output Short-Circuit to GND ..... Continuous
Lead Temperature (Soldering, 60 sec) ..... 300°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
14-Pin Hermetic DIP (Z)	110	26	°C/W
14-Pin Plastic DIP (P)	83	39	°C/W
14-Pin SO (S)	120	36	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V+ = +5V, T_A = 25°C, unless otherwise noted.

			CMP-04B/F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	R_S = 0Ω, R_L = 5.1kΩ V_O = 1.4V, (Note 1)	—	0.4	1	mV
Input Offset Current	I_{OS}	$I_{IN}(+) - I_{IN}(-)$ R_L = 5.1kΩ V_O = 1.4V	—	2	10	nA
Input Bias Current	I_B	$I_{IN}(+)$ or $I_{IN}(-)$	—	25	100	nA
Voltage Gain	A_V	$R_L \geq$ 15kΩ, V+ = 15V, (Note 5)	80	200	—	V/mV
Large-Signal Response Time	t_r	V_{IN} = TTL Logic Swing V_{REF} = 1.4V, (Note 4) V_{RL} = 5V, R_L = 5.1kΩ	—	300	—	ns
Small-Signal Response Time	t_r	V_{IN} = 100mV Step, (Note 4) 5mV Overdrive V_{RL} = 5V, R_L = 5.1kΩ	—	1.3	—	μs
Input Voltage Range	CMVR	(Note 2)	0	—	V+ –1.5	V
Common-Mode Rejection Ratio	CMRR	(Notes 3, 5)	80	100	—	dB
Power Supply Rejection Ratio	PSRR	V+ = +5V to 18V, (Note 5)	80	100	—	dB
Saturation Voltage	V_{OL}	$V_{IN}(-) \geq$ 1V, $V_{IN}(+)$ = 0, $I_{SINK} \leq$ 4mA	—	250	400	mV
Output Sink Current	I_{SINK}	$V_{IN}(-) \geq$ 1V, $V_{IN}(+)$ = 0, $V_O \leq$ 1.5V	6	16	—	mA
Output Leakage Current	I_{LEAK}	$V_{IN}(+) \geq$ 1V, $V_{IN}(-)$ = 0, V_O = 30V	—	0.1	100	nA
Supply Current	I+	R_L = ∞, All Comps V+ = 30V	—	0.8	2.0	mA

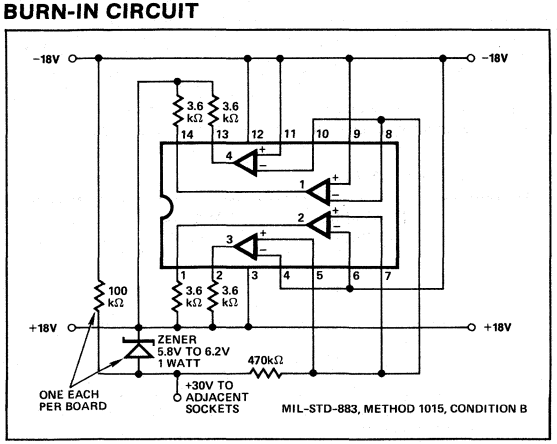
NOTES:
1. At output switch point, V_O = 1.4V, R_S = 0Ω with V+ from 5V; and over the full input common-mode range (0V to V+ – 1.5V).
2. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ – 1.5V, but either or both inputs can go to +30V without damage.
3. $R_L \geq$ 15kΩ, V+ = 15V, V_{CM} = 1.5V to 13.5V.
4. Sample tested.
5. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at V+ = +5V, −55°C ≤ T_A ≤ +125°C for CMP-04BY, −40°C ≤ T_A ≤ +85°C for CMP-04FY/FP/FS, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-04B/F (Note 3) MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 0\Omega$, $R_L = 5.1k\Omega$ $V_O = 1.4V$, (Note 1)	—	1	2	mV
Input Offset Current	I_{OS}	$I_{IN}(+) - I_{IN}(-)$ $R_L = 5.1k\Omega$ $V_O = 1.4V$	—	4	20	nA
Input Bias Current	I_B	$I_{IN}(+)$ or $I_{IN}(-)$	—	40	200	nA
Voltage Gain	A_V	$R_L \geq 15k\Omega$, V+ = 15V, (Note 5)	70	125	—	V/mV
Large-Signal Response Time	t_r	V_{IN} = TTL Logic Swing $V_{REF} = 1.4V$, (Note 4) $V_{RL} = 5V$, $R_L = 5.1k\Omega$	—	300	—	ns
Small-Signal Response Time	t_r	V_{IN} = 100mV Step, (Note 4) 5mV Overdrive $V_{RL} = 5V$, $R_L = 5.1k\Omega$	—	1.3	—	μs
Input Voltage Range	CMVR	(Note 2)	0	—	V+ −1.5	V
Common-Mode Rejection Ratio	CMRR	(Notes 3, 5)	60	100	—	dB
Power Supply Rejection Ratio	PSRR	V+ = +5V to 18V	80	100	—	dB
Saturation Voltage	V_{OL}	$V_{IN}(-) \geq 1V$, $V_{IN}(+) = 0$, $I_{SINK} \leq 4mA$	—	250	700	mV
Output Sink Current	I_{SINK}	$V_{IN}(-) \geq 1V$, $V_{IN}(+) = 0$, $V_O \leq 1.5V$	5	16	—	mA
Output Leakage Current	I_{LEAK}	$V_{IN}(+) \geq 1V$, $V_{IN}(-) = 0$, $V_O = 30V$	—	0.1	200	nA
Supply Current	I+	$R_L = \infty$, All Comps V+ = 30V	—	1.2	3.0	mA

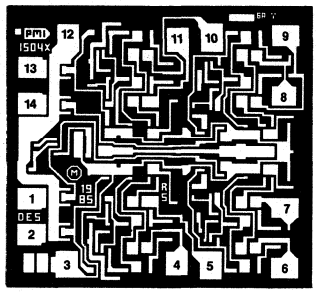
NOTES:
1. At output switch point, $V_O = 1.4V$, $R_S = 0\Omega$ with V+ from 5V; and over the full input common-mode range (0V to V+ − 1.5V).
2. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ − 1.5V, but either or both inputs can go to +30V without damage.
3. $R_L \geq 15k\Omega$, V+ = 15V, V_{CM} = 1.5V to 13.5V.
4. Sample tested.
5. Guaranteed by design.

BURN-IN CIRCUIT



CMP-04

DICE CHARACTERISTICS



DIE SIZE 0.058 × 0.055 inch, 3190 sq. mils
(1.47 × 1.40 mm, 2.058 sq. mm)

1. OUTPUT (2)
2. OUTPUT (1)
3. POSITIVE SUPPLY
4. INVERTING INPUT (1)
5. NONINVERTING INPUT (1)
6. INVERTING INPUT (2)
7. NONINVERTING INPUT (2)
8. INVERTING INPUT (3)
9. NONINVERTING INPUT (3)
10. INVERTING INPUT (4)
11. NONINVERTING INPUT (4)
12. GROUND (SUBSTRATE)
13. OUTPUT (4)
14. OUTPUT (3)

WAFER TEST LIMITS at V+ = +5V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-04N LIMIT	CMP-04G LIMIT	UNITS
Input Offset Voltage	V_{OS}	R_S = 0Ω, R_L = 5.1kΩ V_O = 1.4V, (Note 1)	1	2	mV MAX
Input Offset Current	I_{OS}	$I_{IN}(+) - I_{IN}(-)$ R_L = 5.1kΩ V_O = 1.4V	10	25	nA MAX
Input Bias Current	I_B	$I_{IN}(+)$ or $I_{IN}(-)$, (Note 1)	100	100	nA MAX
Voltage Gain	A_V	$R_L \geq$ 15kΩ, V+ = 15V, (Note 3)	80	50	V/mV MIN
Input Voltage Range	CMVR	(Notes 2, 3)	V+ − 1.5	V+ − 1.5	V MAX
Common-Mode Rejection Ratio	CMRR	(Note 4)	80	80	dB MIN
Power Supply Rejection Ratio	PSRR	V+ = 5V to +18V	80	80	dB MIN
Saturation Voltage	V_{OL}	$V_{IN}(-) \geq$ 1V, $V_{IN}(+)$ = 0, $I_{SINK} \leq$ 4mA	400	400	mV MAX
Output Sink Current	I_{SINK}	$V_{IN}(-) \geq$ 1V, $V_{IN}(+)$ = 0, $V_O \leq$ 1.5V	6	6	mA MIN
Output Leakage Current	I_{LEAK}	$V_{IN}(+) \geq$ 1V, $V_{IN}(-)$ = 0, V_O = 30V	100	100	nA MAX
Supply Current	I+	R_L = ∞, All Comps V+ = 30V	2	2	mA MAX

NOTES:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

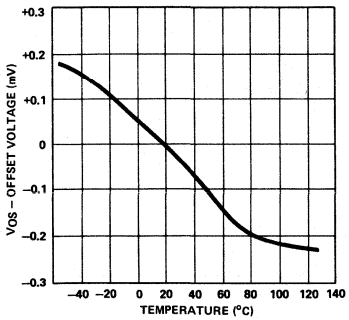
TYPICAL ELECTRICAL CHARACTERISTICS at V+ = +5V, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-04N TYPICAL	CMP-04G TYPICAL	UNITS
Large-Signal Response Time	t_r	V_{IN} = TTL Logic Swing V_{REF} = 1.4V, (Note 5) V_{RL} = 5V, R_L = 5.1kΩ	600	600	ns
Small-Signal Response Time	t_r	V_{IN} = 100mV Step, (Note 5) 5mV Overdrive V_{RL} = 5V, R_L = 5.1kΩ	1.3	1.3	µs

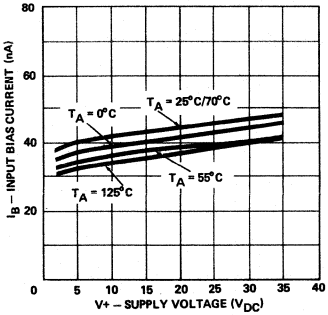
NOTES:
1. At output switch point, V_O = 1.4V, R_S = 0Ω with V+ from 5V; and over the full input common-mode range (0V to V+ − 1.5V).
2. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ − 1.5V, but either or both inputs can go to +30V without damage.
3. Guaranteed by design.
4. $R_L \geq$ 15kΩ. V_{CM} = 1.5V to 13.5V.
5. Sample tested.

TYPICAL PERFORMANCE CHARACTERISTICS

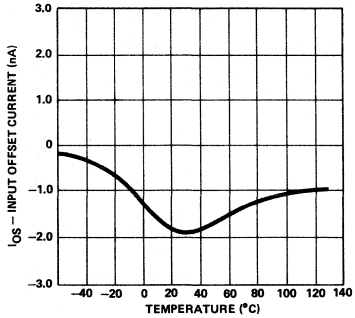
OFFSET VOLTAGE vs TEMPERATURE



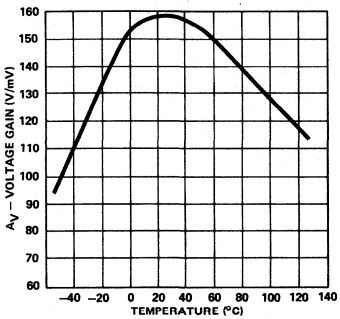
INPUT BIAS CURRENT vs V+ AND TEMPERATURE



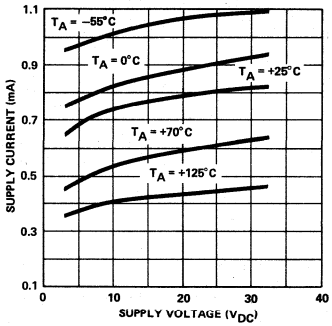
INPUT OFFSET CURRENT vs TEMPERATURE



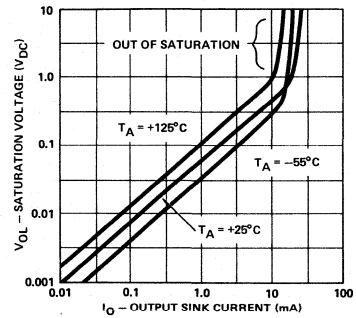
VOLTAGE GAIN vs TEMPERATURE



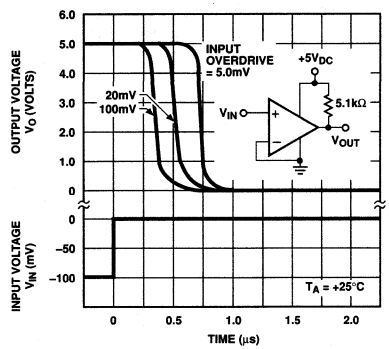
SUPPLY CURRENT vs SUPPLY VOLTAGE



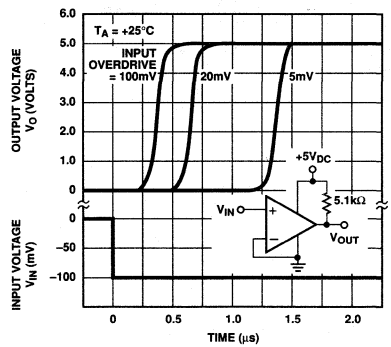
OUTPUT VOLTAGE vs OUTPUT CURRENT AND TEMPERATURE



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES — NEGATIVE TRANSITION



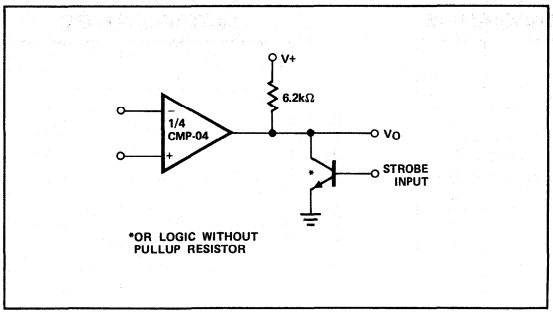
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES — POSITIVE TRANSITION



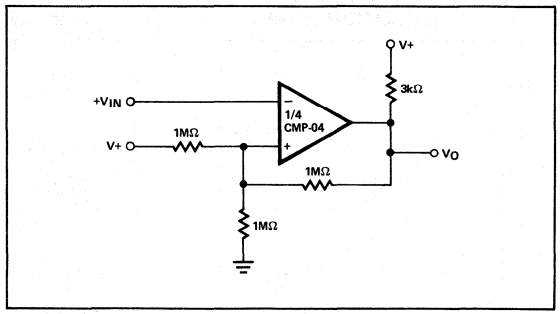
CMP-04

TYPICAL APPLICATIONS

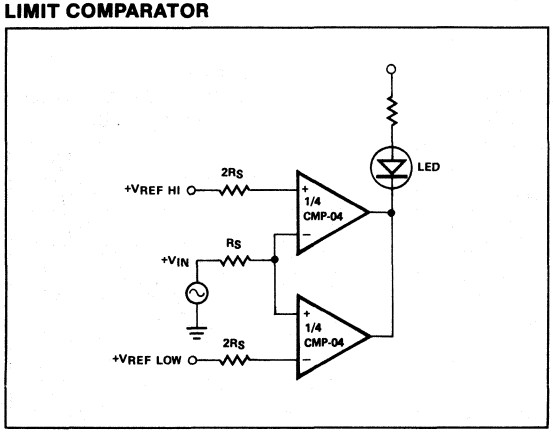
OUTPUT STROBING



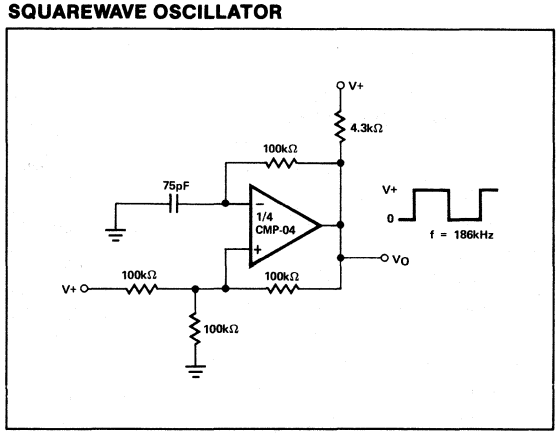
INVERTING COMPARATOR WITH HYSTERESIS



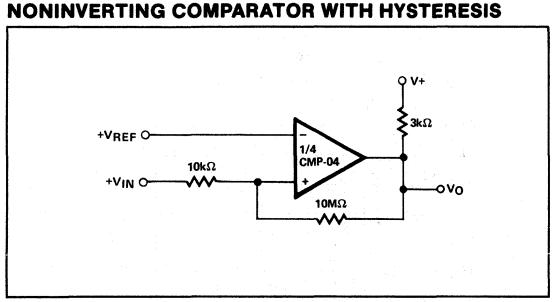
LIMIT COMPARATOR



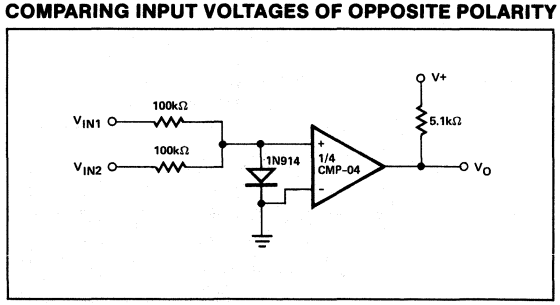
SQUAREWAVE OSCILLATOR



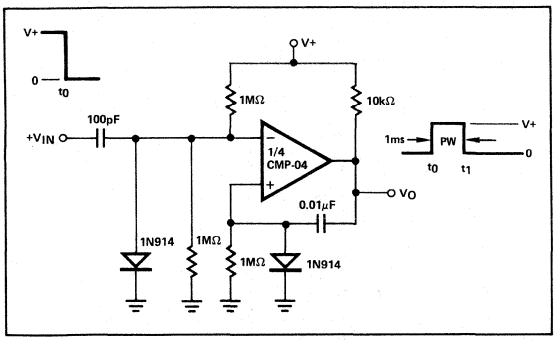
NONINVERTING COMPARATOR WITH HYSTERESIS



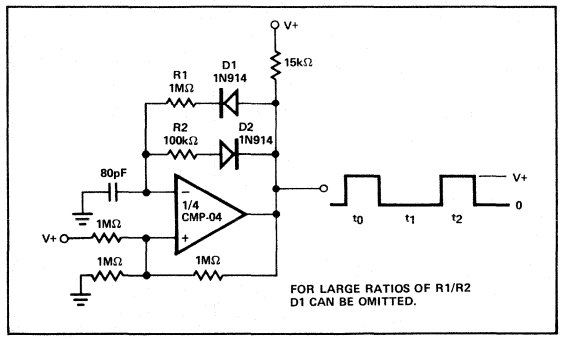
COMPARING INPUT VOLTAGES OF OPOSITE POLARITY



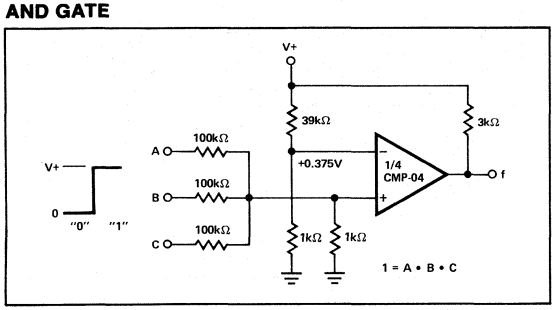
ONE-SHOT MULTIVIBRATOR



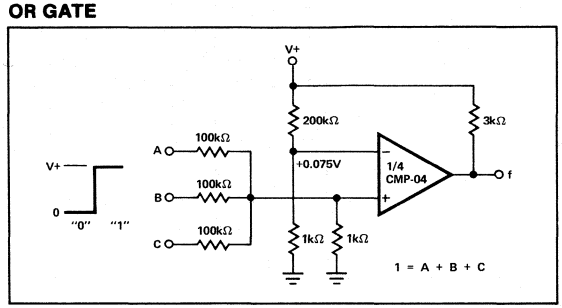
PULSE GENERATOR



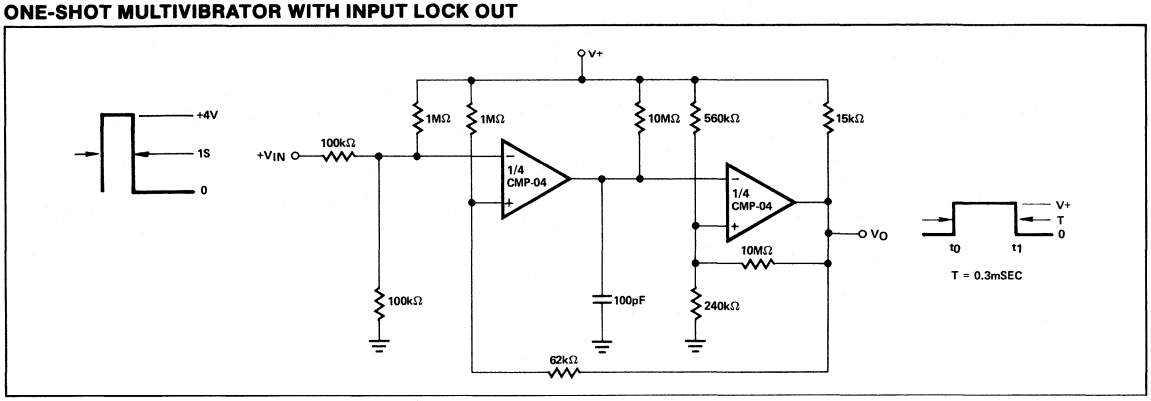
AND GATE



OR GATE

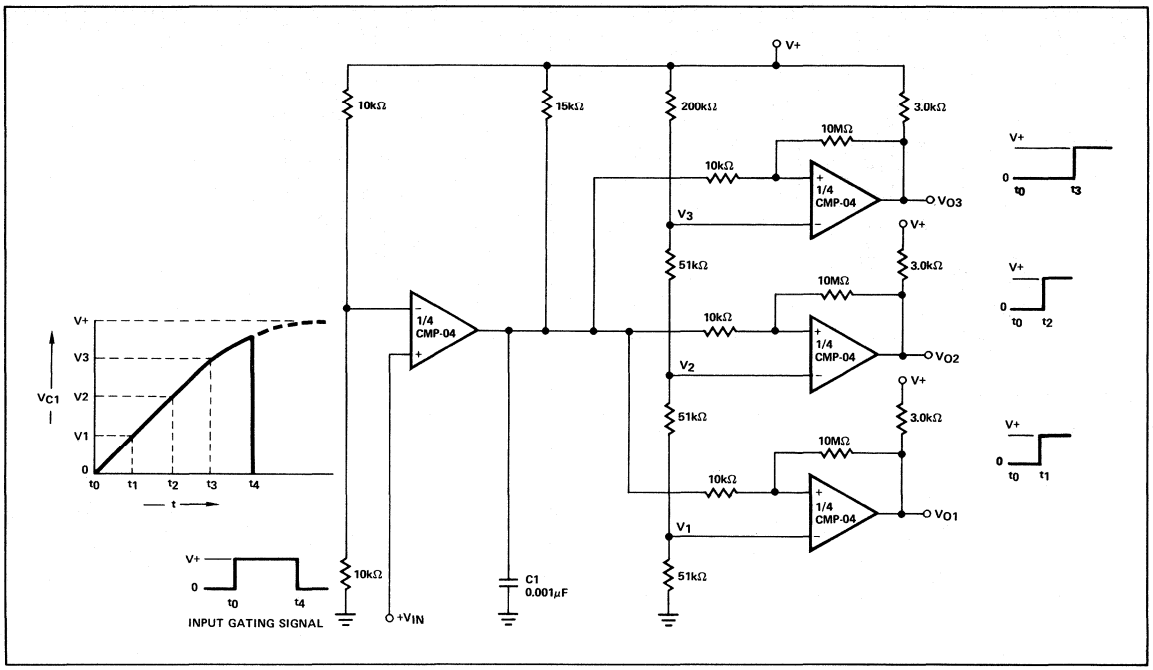


ONE-SHOT MULTIVIBRATOR WITH INPUT LOCK OUT



TYPICAL APPLICATIONS

TIME DELAY GENERATOR



ANALOG DEVICES

High Speed Precision Comparator

CMP-05

FEATURES

- **Precision Input Stage**
  - **Input Offset Voltage 150μV**
  - **Input Offset Current 15nA**
- **Fast Response Time (5mV Overdrive) 38ns**
- **High Voltage Gain 16,000V/V**
- **Latch Function with TTL Compatible Input**
- **TTL Compatible Output**
- **Available in Hermetic Mini-DIP Package**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} (μV)	PACKAGE TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	SO 8-PIN	OPERATING TEMPERATURE RANGE
600	CMP05BJ/883	CMP05BZ/883	–	–	MIL
600	CMP05FJ	CMP05FZ	–	–	IND
1000	CMP05CJ/883	CMP05CZ*	–	–	MIL
1000	–	CMP05GZ	CMP05GP	CMP05GS	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

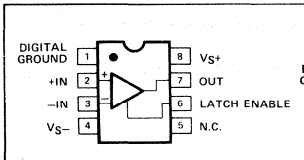
GENERAL DESCRIPTION

The CMP-05's very high speed and precision input specifications make it the ideal comparator in systems needing 12-bit accuracy along with high speed. An exceptionally fast response time of 60nsec is possible with only 1/2 LSB overdrive (12-bit, 10-volt system).

The CMP-05 design makes it the ideal component in systems requiring high speed with excellent low-level analog signal resolution. High-speed 12-bit successive approximation A/D converters, zero crossing detectors and logic threshold detectors are typical system applications.

3

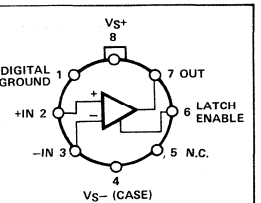
PIN CONNECTIONS



8-PIN HERMETIC MINI-DIP (Z-Suffix)

EPOXY MINI-DIP (P-Suffix)

8-PIN SO (S-Suffix)

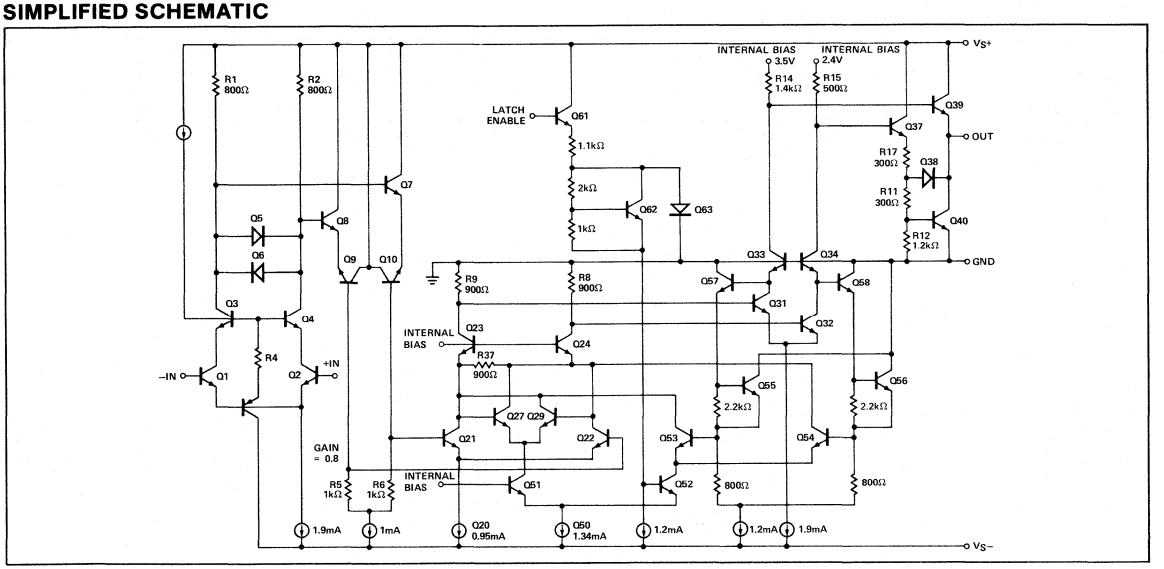


TO-99 (J-Suffix)

LOGIC TABLE

LATCH ENABLE	OUT
0 or NC	Comparing
1	Latched

SIMPLIFIED SCHEMATIC



CMP-05

ABSOLUTE MAXIMUM RATINGS (Note 1)

Positive Supply Voltage ..... +6V
Negative Supply Voltage ..... −18V
Differential Input Voltage ..... ±5V
Latch Enable Input Voltage ..... −0.5V to V+ Supply
Operating Temperature Range
CMP-05B/C (J, Z) (Note 2) ..... −55°C to +125°C
CMP-05F/G (J, P, S, Z) ..... −40°C to +85°C
Junction Temperature (T_j) ..... −65°C to +150°C
Storage Temperature Range ..... −65°C to +150°V
P-Suffix ..... −65°C to +125°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
Output Short-Circuit Duration
To Ground ..... Indefinite
To V+ = 5.0V ..... 1 Minute

PACKAGE TYPE	Θ_{JA} (Note 3)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Latch is functional for $-55°C \le T_A \le +85°C$.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO, CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at $V_S+ = 5.0V$, $V_S- = -5.0V$, $T_A = 25°C$ and Latch Enable grounded, unless otherwise noted.

			CMP-05B/F			CMP-05C/G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	150	600	—	400	1000	µV
Input Offset Current	I_{OS}		—	15	80	—	30	150	nA
Input Bias Current	I_B		—	0.6	1.2	—	0.8	1.8	µA
Voltage Gain	A_{VO}	(Note 1)	8	16	—	7	14	—	V/mV
Input Voltage Range	CMVR	(Note 1)	±3.0	±3.3	—	±3.0	±3.3	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 3.0V$, (Note 1)	86	91	—	84	89	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.75V$ to $V_S = \pm 5.25V$	—	51	126	—	64	126	µV/V
		P Package	—	—	—	—	120	360	
		$V_S+ = 5V$, $V_S- = -5V$ to $-15V$	—	15	51	—	18	63	
		P Package	—	—	—	—	36	180	
Output High Voltage	V_{OH}	$V_{IN} \ge 10mV$, $I_O = 0\mu A$	2.4	2.9	—	2.4	2.9	—	V
		$V_{IN} \ge 10mV$, $I_O = 320\mu A$	2.4	2.9	—	—	—	—	
		$V_{IN} \ge 10mV$, $I_O = 200\mu A$	—	—	—	2.4	2.9	—	
Saturation Voltage	V_{SAT}	$V_{IN} \le -10mV$, $I_{SINK} = 0mA$	—	0.13	0.40	—	0.13	0.40	V
		$V_{IN} \le -10mV$, $I_{SINK} = 8mA$	—	—	—	—	0.28	0.40	
		$V_{IN} \le -10mV$, $I_{SINK} = 12.8mA$	—	0.32	0.40	—	—	—	
Positive Supply Current	I_S+	$V_O \le 2.4V$, (Note 1)	—	7.5	11	—	8.0	12	mA
		$V_O \le 0.4V$	—	10	15	—	11	16	
Negative Supply Current	I_S-	$V_O \le 0.4V$	—	11	16	—	12	18	mA
Power Dissipation	P_d	$V_O \le 0.4V$	—	105	155	—	115	170	mW
Latch Input Voltage									
Logic 1	V_{LH}	Over Operating Temp. Range, Latch Enabled, (Note 1)	2.0	—	—	2.0	—	—	V
Logic 0	V_{LL}	Over Operating Temp. Range, Latch Disabled, (Note 1)	—	—	0.8	—	—	0.8	
Latch Input Current									
Logic 1	I_{LH}	$V_{LH} = 3.0V$, (Note 1)	—	10	45	—	10	45	µA
Logic 0	I_{LL}	$V_{LL} = 0.8V$, (Note 1)	—	6	25	—	6	25	
Input to Output High Response Time	t_{pd+}	$V_{OD} = 1.2mV$, (Note 2)	—	60	—	—	60	—	ns
		$V_{OD} = 5.0mV$, (Note 2)	—	41	55	—	41	55	
Input to Output Low Response Time	t_{pd-}	$V_{OD} = 1.2mV$, (Note 2)	—	60	—	—	60	—	ns
		$V_{OD} = 5.0mV$, (Note 2)	—	37	55	—	37	55	
Latch Disable Time	t_{LPD}	(Note 3)	—	50	65	—	50	65	ns

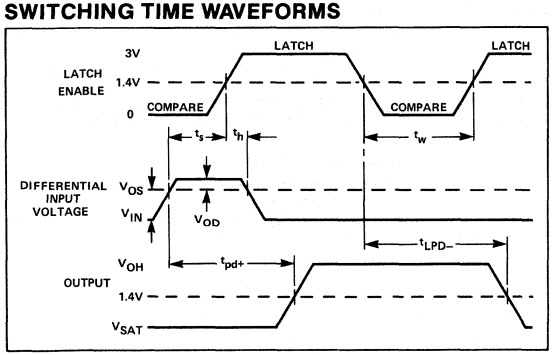
NOTES:
1. Guaranteed by design.
2. Times are for 100mV step inputs. See switching time waveforms.
3. See switching time waveforms.

ELECTRICAL CHARACTERISTICS at $V_S+ = 5.0V$, $V_S- = -5.0V$, and Latch Enable grounded, $-55°C \le T_A \le +125°C$ for CMP-05B/C, $-25°C \le T_A \le +85°C$ for CMP-05F, $-40°C \le T_A \le +85°C$ for CMP-05G, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-05B/F MIN	CMP-05B/F TYP	CMP-05B/F MAX	CMP-05C/G MIN	CMP-05C/G TYP	CMP-05C/G MAX	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	0.3	1.5	—	0.55	2.0	mV
Input Offset Voltage Drift	TCV_{OS}		—	1.5	7.5	—	2.5	15	µV/°C
Input Offset Current	I_{OS}		—	40	250	—	70	400	nA
Input Bias Current	I_B		—	1.1	2.5	—	1.5	3.8	µA
Voltage Gain	A_{VO}	(Note 1)	6	11	—	5	10	—	V/mV
Input Voltage Range	CMVR	(Note 1)	±2.9	±3.2	—	±2.9	±3.2	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 2.9V$, (Note 1)	83	90	—	80	88	—	dB
Power Supply Rejection Ratio	PSRR	$\pm 4.75V \le V_S \le \pm 5.25V$ P Package	— —	63 —	178 —	— —	80 150	252 400	µV/V
Output High Voltage	V_{OH}	$V_{IN} \ge 10mV$, $I_O = 0\mu A$ $V_{IN} \ge 10mV$, $I_O = 240\mu A$ $V_{IN} \ge 10mV$, $I_O = 160\mu A$	2.4 2.4 —	— — —	— — —	2.4 — 2.4	— — —	— — —	V
Saturation Voltage	V_{SAT}	$V_{IN} \le -10mV$, $I_{SINK} = 0mA$ $V_{IN} \le -10mV$, $I_{SINK} = 9.6mA$ $V_{IN} \le -10mV$, $I_{SINK} = 6.4mA$	— — —	0.18 0.2 —	0.40 0.40 —	— — —	0.20 — 0.30	0.40 — 0.40	V
Positive Supply Current	I_S+	$V_O \le 0.4V$	—	11	16	—	12	17	mA
Negative Supply Current	I_S-	$V_O \le 0.4V$	—	12	17	—	13	19	mA
Power Dissipation	P_d	$V_O \le 0.4V$	—	115	165	—	125	180	mW
Latch Input Current Logic 1 Logic 0	 I_{LH} I_{LL}	 $V_{LH} = 3V$, (Notes 1, 4) $V_{LL} = 0.8V$, (Notes 1, 4)	 — —	 18 10	 90 50	 — —	 18 10	 90 50	µA
Input to Output High Response Time	t_{pd+}	$V_{OD} = 1.2mV$, (Note 2) $V_{OD} = 5.0mV$, (Note 2)	— —	125 92	— —	— —	125 92	— —	ns
Input to Output Low Response Time	t_{pd-}	$V_{OD} = 1.2mV$, (Note 2) $V_{OD} = 5.0mV$, (Note 2)	— —	115 88	— —	— —	115 88	— —	ns
Latch Disable Time	t_{LPD+} t_{LPD-}	(Notes 2, 4)	— —	56 30	— —	— —	56 30	— —	ns

NOTES:
1. Guaranteed by design.
2. Times are for 100mV step inputs. See switching time waveforms.
3. A high on the latch enable input will cause the latch to assume the state of the comparator and not follow subsequent inputs.
4. Latch is functional for $-55°C \le T_A \le +85°C$.

SWITCHING TIME WAVEFORMS



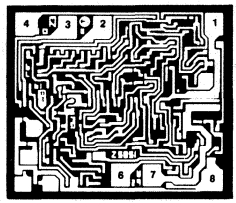
Minimum Input Timing Requirements*

Parameter		Minimum Limit	Units
t_S	Setup Time	35	ns
t_h	Hold Time	10	
t_w	Latch Pulse Width	25	

*t_S, t_h, t_w are tested with $V_{IN} = 100mV$ and $V_{OD} = 5mV$.

CMP-05

DICE CHARACTERISTICS



1. DIGITAL GROUND
2. NONINVERTING INPUT
3. INVERTING INPUT
4. NEGATIVE SUPPLY (SUBSTRATE)
6. LATCH ENABLE
7. OUTPUT
8. POSITIVE SUPPLY

DIE SIZE 0.052 × 0.046 inch, 2392 sq. mils
(1.321 × 1.168mm, 1.543 sq. mm)

WAFER TEST LIMITS at $V_S = \pm 5V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-05G LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	1000	μV MAX
Input Offset Current	I_{OS}		150	nA MAX
Input Bias Current	I_B		1.8	μA MAX
Voltage Gain	A_{VO}	(Note 1)	7	V/mV MIN
Input Voltage Range	CMVR	(Note 1)	±3.0	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 2.9V$ (Note 1)	80	dB MIN
Power Supply Rejection Ratio	PSRR	$\pm 4.75 \le V_S \le \pm 5.25$ $V_S+ = 5V$, $V_S- = -5V$ to $-15V$	178 63	μV/V MAX
Positive Output Voltage	V_{OH}	$V_{IN} \ge 10mV$, $I_O = 0\mu A$	2.4	V MIN
Saturation Voltage	V_{SAT}	$V_{IN} \le 10mV$, $I_O = 0\mu A$	0.4	V MAX
Positive Supply Current	I+	$V_O \le 0.4V$	16	mA MAX
Negative Supply Current	I−	$V_O \le 0.4V$	18	mA MAX
Negative Supply Current	I−	$V- = -15V$, $V_O \le 0.4V$	20	mA MAX
Latch Input Voltage Logic 1 Logic 0	 V_{LH} V_{LL}	 Latch Enabled Latch Disabled	 2.0 0.8	 V MIN V MAX
Latch Input Current Logic 1 Logic 0	 I_{LH} I_{LL}	 $V_{LH} = 3.0V$, (Notes 1, 4) $V_{LL} = 0.8V$, (Notes 1, 4)	 45 25	 μA MAX
Input to Output High Response Time	t_{pd+}	$V_{OD} = 5.0mV$, (Notes 1, 2)	60	ns MAX
Input to Output Low Response Time	t_{pd-}	$V_{OD} = 5.0mV$, (Notes 1, 2)	60	ns MAX

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

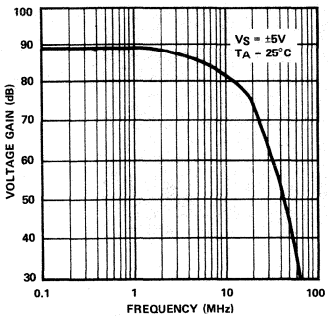
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 5V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-05G TYPICAL	UNITS
Input to Output High Response Time	t_{pd+}	$V_{OD} = 1.2mV$, (Note 2)	41	ns
Input to Output Low Response Time	t_{pd-}	$V_{OD} = 1.2mV$, (Note 2)	37	ns
Latch Disable Time	t_{LPD}	(Notes 3, 4)	50	ns

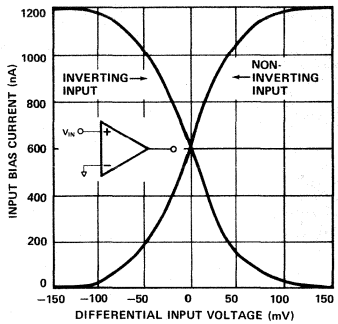
NOTES:
1. Guaranteed by design.
2. Times are for 100mV step inputs.
3. See switching time waveforms.
4. Latch is functional for $-55°C \le T_A \le 85°C$.

TYPICAL PERFORMANCE CHARACTERISTICS

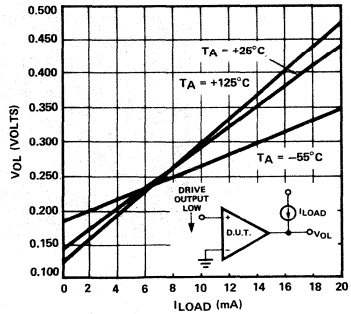
VOLTAGE GAIN vs FREQUENCY



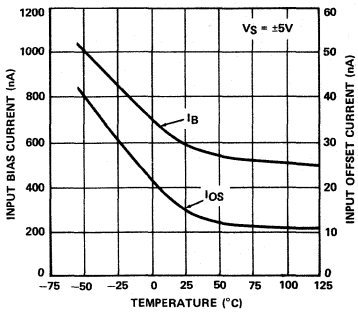
INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



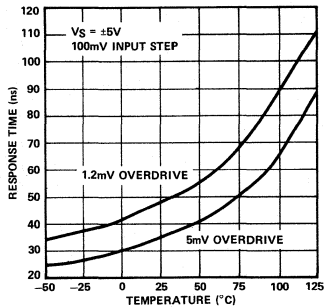
V_{SAT} vs LOAD CURRENT



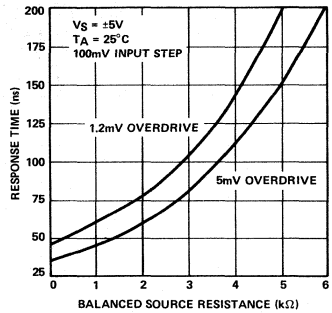
INPUT CURRENTS vs TEMPERATURE



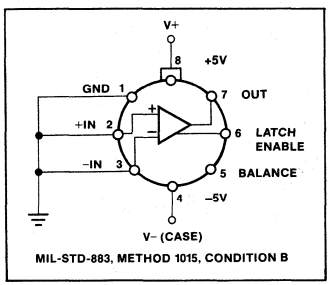
RESPONSE TIME vs TEMPERATURE



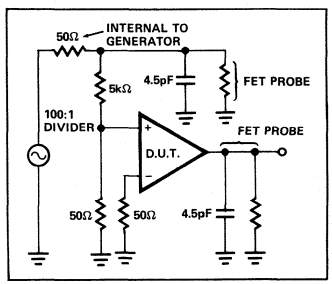
RESPONSE TIME vs BALANCED SOURCE RESISTANCE



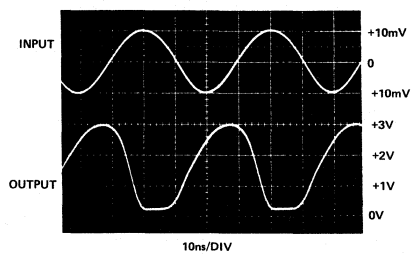
STANDARD BURN-IN CIRCUIT



RESPONSE PHOTOGRAPH TEST SET-UP



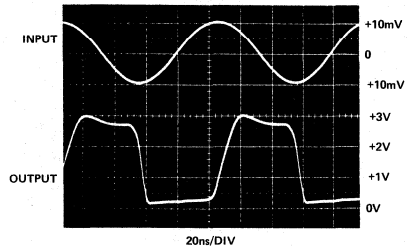
RESPONSE TO 25MHz SINE WAVE



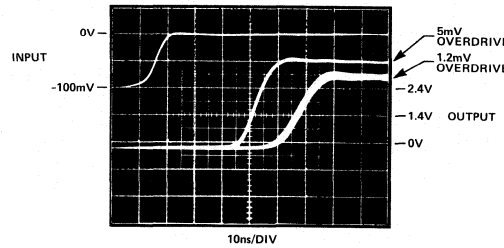
3

TYPICAL PERFORMANCE CHARACTERISTICS

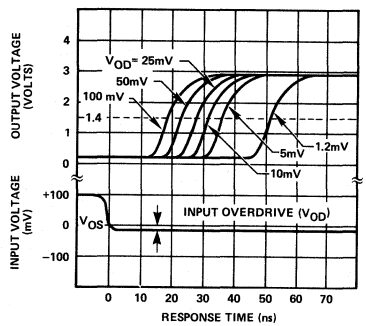
RESPONSE TO 10MHz SINE WAVE



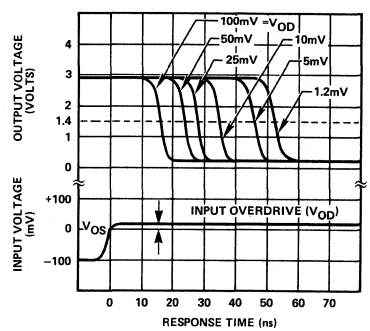
RESPONSE TIME TO 5mV AND 1.2mV (= 1/2 LSB) OVERDRIVES



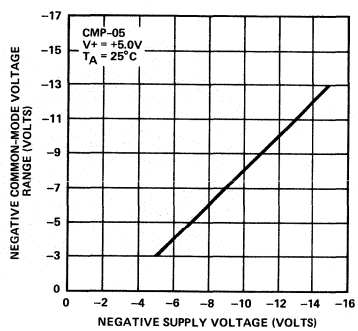
t_{pd+} RESPONSE TIME



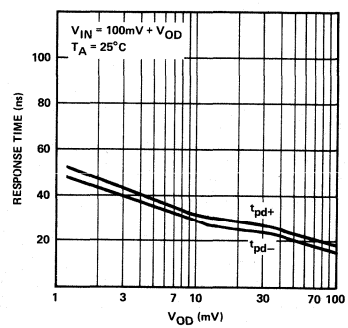
t_{pd-} RESPONSE TIME



CMP-05 NEGATIVE COMMON-MODE INPUT RANGE vs NEGATIVE SUPPLY



RESPONSE TIME vs OVERDRIVE VOLTAGE



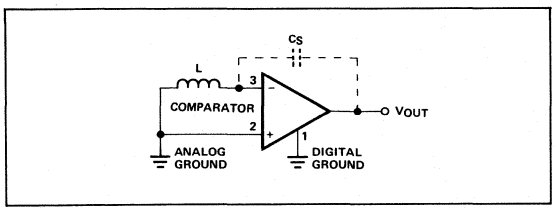
APPLICATION INFORMATION

The CMP-05 is a very accurate device providing fast response time even with small—Microvolt level—overdrives. To achieve this performance requires high gain at high frequencies. As shown in the voltage gain versus frequency curve, the gain—bandwidth product of the CMP-05 is 1.5×10^{11} Hz. It maintains its full gain to approximately 8MHz and rolls off at a very fast rate beyond that frequency due to the fact that five poles occur in the 30 to 60MHz range. At 30MHz the gain of the comparator is still 2000. Therefore, in the transition region small values of source lead inductance and stray feedback capacitance can cause an oscillatory condition.

For example (in the figure below) with $L = 0.1\mu H$, $C_S = 0.15pF$, the closed-loop gain of the circuit at 30MHz is:

$$A_V = \frac{1}{LC_S\omega^2} = \frac{1}{10^{-7} \times 0.15 \times 10^{-12} \times (2\pi \times 30 \times 10^6)^2} = 1880$$

POTENTIAL FEEDBACK SOURCES



With the open-loop gain at 2000 oscillation will occur since the phase shift exceeds 180° C. To minimize these problems power supplies should be decoupled, lead lengths should be kept as short as possible, and a ground plane should be used to reduce the stray feedback capacitance. In addition, a ground plane substantially diminishes the possibility of the output current spike coupling back to the inputs through the ground lead. Keeping a separate digital ground (pin 1) and analog ground (to which the inputs are referenced) also reduces the magnitude of the problem.

Fortunately, in high-speed circuitry the comparator inputs will be driven at a fast rate, in which case no transition region oscillations will occur. As the minimum slew rate versus source resistance curve indicates, if the input is driven at a rate exceeding 6mV/μsec, no oscillations will occur with source resistors of less than 1kΩ. Examples of "clean" transitions can be observed in the photographs of the response time with 5mV and 1.2mV overdrives, and the response to the 10 and 25MHz input signals.

In order to not degrade its speed the CMP-05's inputs are not internally clamped. If large differential voltages are present it is recommended that the inputs be clamped with high speed, low capacitance diodes such as the H.P. 5082-2835, which is a Schottky Diode.

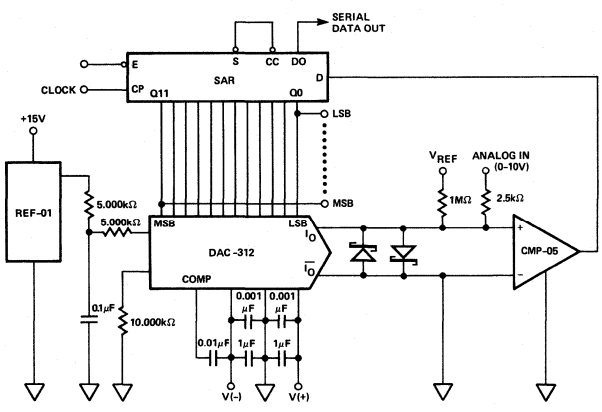
As in all high-speed devices, it is to the user's advantage to keep the source impedances low and matched.

LATCH

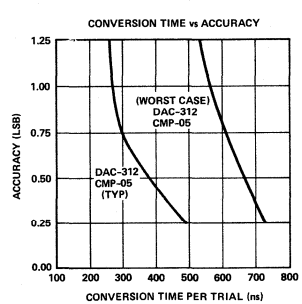
The CMP-05 has a latch feature which functions over −55° C to +85° C. When the latch is enabled, the output stays in its existing logic state regardless of the input signal. The input timing requirements of the latch are presented in the Switching Time Waveforms. The latch opens up a broader applications area at no sacrifice in total system speed. Effectively, the latch allows high speed sampling of comparison decisions. This is important in automatic test equipment limit comparators, in measuring pods used in logic analyzers and other similar synchronous measurement circuitry needing fast clocking frequencies. The latch pulse width t_w allows sampling of input signals to take place in 25nsec.

The latch prevents self oscillation (due to positive feedback) from taking place when slowly-moving high-source-impedance signals pass thru the linear amplification region of the comparator. This is successfully accomplished by rapidly strobing the comparator near its minimum t_w time which prevents self oscillation from making a complete cycle since t_w is shorter than the total response time t_{pd} through the comparator.

12-BIT FAST A/D CONVERTER



NOTE:
DEVICE(S) CONNECTED TO ANALOG INPUT MUST BE CAPABLE OF SOURCING 4.0mA. A BUFFER (eg. BUF-03) MAY BE REQUIRED.



CONVERSION TIME (ns)	TYP	WORST CASE
SAR	33	55
CMP-05	92	125
TOTAL	375ns	680ns
× 13	4.9μs	8.8μs

ANALOG DEVICES

Precision Voltage Comparators

PM-111/PM-211

FEATURES

- High Output Drive 50mA
- Low Input Bias Current ..... 50nA Max
- Low Offset Voltage ..... 3mV Max
- Differential Input Voltage Range ..... ±30V
- Logic Outputs Compatible with Bipolar and CMOS
- Fully-Specified at All Temperatures
- Available In Die Form

ORDERING INFORMATION †

V_{OS} MAX (mV)	PACKAGE TO-99	CERDIP	PLASTIC 8-PIN	SO 8-PIN	LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
3.0	PM111J*	PM111Y*	–	–	PM111RC/883	MIL
3.0	–	PM111Z*	–	–	–	MIL
3.0	PM211J	PM211Y	–	–	–	IND
3.0	–	PM211Z	–	–	–	IND
3.0	–	–	PM211P	PM211S	–	XIND

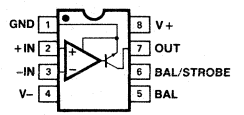
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

The PM-111/PM-211 are voltage comparators featuring low input bias and offset currents, high-differential voltage ranges, and wide-supply voltage ranges. The inputs and outputs can be isolated from system ground, and the output can drive loads referred to ground or either supply voltage. Strobing and offset balancing are available and the outputs can be wire OR'ed.

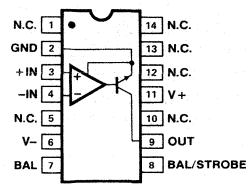
PIN CONNECTIONS



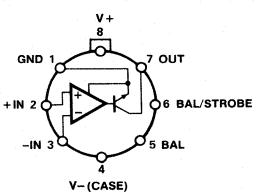
HERMETIC MINI-DIP
(Z-Suffix)

8-PIN PLASTIC
(P-Suffix)

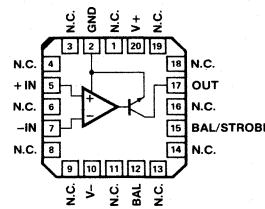
8-PIN SO
(S-Suffix)



14-PIN HERMETIC DIP
(Y-Suffix)

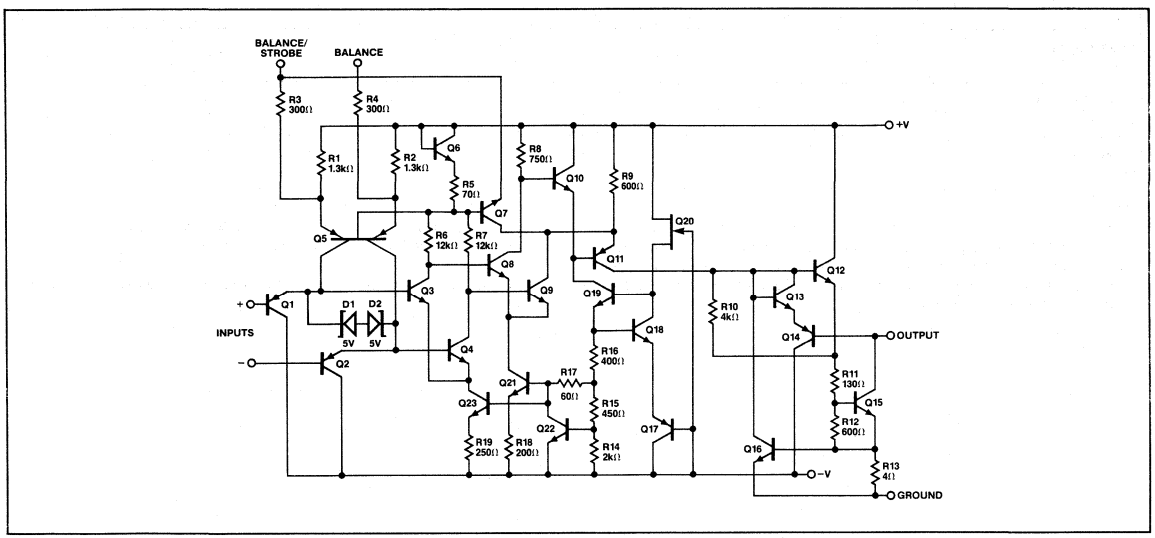


TO-99
(J-Suffix)



PM-111RC/883
LCC
(RC-Suffix)

SIMPLIFIED SCHEMATIC



PM-111/PM-211

ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage, V+ to V– 36V
Output to Negative Supply Voltage 50V
Ground to Negative Supply Voltage 30V
Strobe Pin Voltage ..... V^+–5V
Differential Input Voltage ..... ±30V
Input Voltage (Note 2) ..... ±15V
Output Short-Circuit Duration 10s
Operating Temperature Range
PM-111 ..... –55°C to +125°C
PM-211 (J, Y, Z) ..... –25°C to +85°C
PM-211S/PM-211P ..... –40°C to +85°C
Junction Temperature (T_J) ..... –65°C to +150°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE TYPE	Θ_{JA} (Note 3)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
14-Pin Hermetic DIP (Y)	108	16	°C/W
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC (RC)	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Rating applies to V_S = ±15V. The positive input-voltage limit is 30V above the negative supply. The negative input-voltage limit is equal to the negative supply or 30V below the positive supply, whichever is less.
3. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{jA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, ground pin at ground and T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-111/PM-211 MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	0.75	3.0	mV
Input Offset Current	I_{OS}	(Note 1)	—	0.3	5.0	nA
Input Bias Current	I_B	(Note 1)	—	25	50	nA
Voltage Gain (Emitter)	A_{VE}	(Note 2)	—	75	—	V/mV
Voltage Gain (Collector)	A_{VC}		—	200	—	V/mV
Response Time	t_r	R_L = 500Ω (tied to V+) V_{OD} = 5mV (Note 3)	—	180	—	ns
Saturation Voltage	V_{OL}	$V_{IN} \leq -5mV$ I_{OUT} = 50mA	—	0.68	1.0	V
Output Leakage Current	I_{CEX}	$V_{IN} \geq +5mV$ V_{OUT} = 50V	—	5	15	nA
Positive Supply Current	I_{SY^+}		—	3.3	5	mA
Negative Supply Current	I_{SY^-}		—	2.4	4	mA
Input Voltage Range	IVR		−14.5 +13	−14.8 +14	—	V

NOTES:
1. The offset voltage, offset current, and bias current given are the maximum values required to drive the collector output to within 1V of the supplies with a 7.5kΩ load. These parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
2. Average of A_{V^+} and A_{V^-} over a ±10V output range measured at the emitter.
3. The response time specified is for a 100mV input step with a 5mV overdrive and is the time required for the slowest edge. The slowest response occurs at the highest temperature of operation.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, ground pin at ground and $-25°C \le T_A \le +85°C$ for PM-211J, Z and Y, $-40°C \le T_A \le +85°C$ for PM-211P and S, unless otherwise noted.

			PM-211			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	(Note 1)	—	0.8	3.0	mV
Input Offset Current	I_{OS}	(Note 1)	—	0.3	7	nA
Input Bias Current	I_B	(Note 1)	—	25	100	nA
Voltage Gain (Emitter)	A_{VE}	(Note 2)	—	35	—	V/mV
Response Time	t_r	$R_L = 500\Omega$ (tied to V+) $V_{OD} = 5mV$ (Note 3)	—	240	—	ns
Saturation Voltage	V_{OL}	$V_{IN} \le -5mV$ $I_{OUT} = 50mA$	—	0.8	1.5	V
Output Leakage Current	I_{CEX}	$V_{IN} \ge +5mV$ $V_{OUT} = 50V$	—	10	100	nA
Positive Supply Current	I_{SY^+}		—	4	6	mA
Negative Supply Current	I_{SY^-}		—	2.8	5	mA
Input Voltage Range	IVR		−14.5 13	−14.8 14	—	V

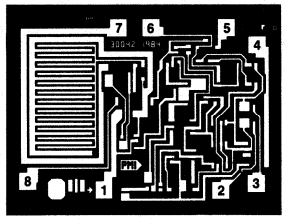
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, ground pin at ground and $-55°C \le T_A \le +125°C$, unless otherwise noted.

			PM-111			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}	(Note 1)	—	0.8	3.0	mV
Input Offset Current	I_{OS}	(Note 1)	—	0.3	10	nA
Input Bias Current	I_B	(Note 1)	—	25	100	nA
Voltage Gain (Emitter)	A_{VE}	(Note 2)	—	20	—	V/mV
Response Time	t_r	$R_L = 500\Omega$ (tied to V+) $V_{OD} = 5mV$ (Note 3)	—	420	—	ns
Saturation Voltage	V_{OL}	$V_{IN} \le -5mV$ $I_{OUT} = 50mA$	—	0.62	1.5	V
Output Leakage Current	I_{CEX}	$V_{IN} \ge +5mV$ $V_{OUT} = 50V$	—	145	500	nA
Positive Supply Current	I_{SY^+}		—	4.2	6	mA
Negative Supply Current	I_{SY^-}		—	3	5	mA
Input Voltage Range	IVR		−14.5 +13	−14.8 +14	—	V

NOTES:
1. The offset voltage, offset current, and bias current given are the maximum values required to drive the collector output to within 1V of the supplies with a 7.5kΩ load. These parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
2. Average of A_{V^+} and A_{V^-} over a ±10V output range measured at the emitter.
3. The response time specified is for a 100mV input step with a 5mV overdrive and is the time required for the slowest edge. The slowest response occurs at the highest temperature of operation.

PM-111/PM-211

DICE CHARACTERISTICS



DIE SIZE 0.066 × 0.050 inch, 3300 sq. mils
(1.68 × 1.27mm, 2.13 sq. mm)

1. **GROUND**
2. **+IN**
3. **−IN**
4. **V−**
5. **BALANCE**
6. **BALANCE/STROBE**
7. **OUTPUT**
8. **V+**

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$ and ground pin at ground for PM-111GBC, $T_A = 125°C$ for PM-111GTBC, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-111GTBC LIMIT	PM-111GBC LIMIT	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	3	3	mV MAX
Input Offset Current	I_{OS}	(Note 1)	10	5	nA MAX
Input Bias Current	I_B	(Note 1)	100	50	nA MAX
Saturation Voltage	V_{OL}		1.5	1.0	V MAX
Output Leakage Current	I_{CEX}	$V_{IN} \geq +5mV$ $V_{OUT} = 50V$	500	15	nA MAX
Input Voltage Range	IVR		±13	—	V MIN
Positive Supply Current	$I_{SY}+$		6	5	mA MAX
Negative Supply Current	$I_{SY}-$		5	4	mA MAX

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

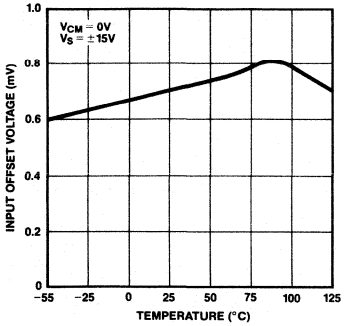
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$ and ground pin at ground for PM-111GBC, $T_A = 125°C$ for PM-111GTBC, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-111GTBC TYPICAL	PM-111GBC TYPICAL	UNITS
Voltage Gain (Emitter)	A_{VE}	(Note 2)	20	75	V/mV
Response Time	t_r	(Note 3)	420	180	ns

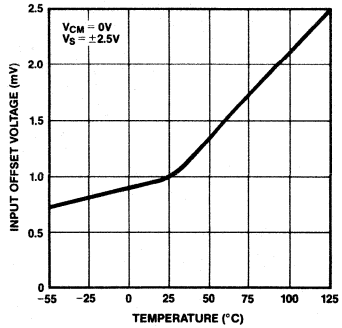
NOTES:
1. The offset voltage, offset current, and bias current given are the maximum values required to drive the collector output to within 1V of the supplies with a 7.5kΩ load. These parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
2. Average of A_V+ and A_V- over a ±10V output range measured at the emitter.
3. The response time specified is for a 100mV input step with a 5mV overdrive and is the time required for the slowest edge. The slowest response occurs at the highest temperature of operation.

TYPICAL PERFORMANCE CHARACTERISTICS

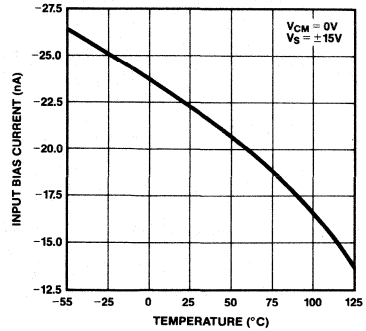
INPUT OFFSET VOLTAGE vs TEMPERATURE



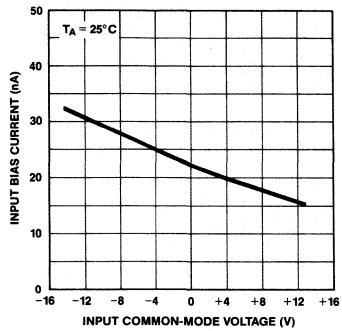
INPUT OFFSET VOLTAGE vs TEMPERATURE



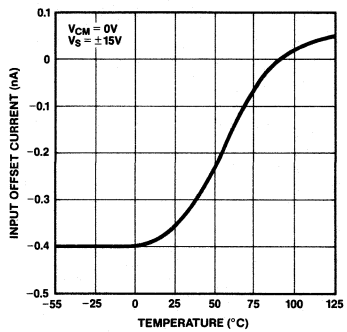
INPUT BIAS CURRENT vs TEMPERATURE



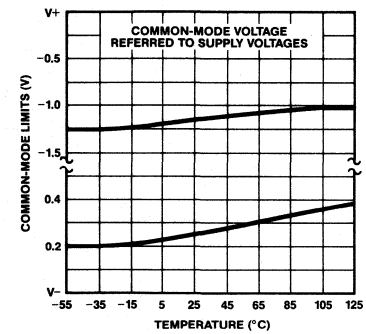
INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE



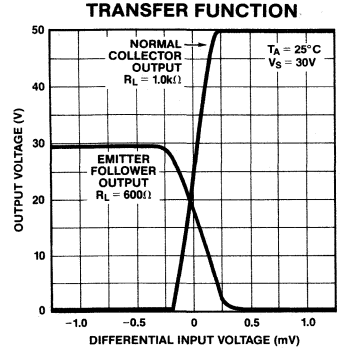
INPUT OFFSET CURRENT vs TEMPERATURE



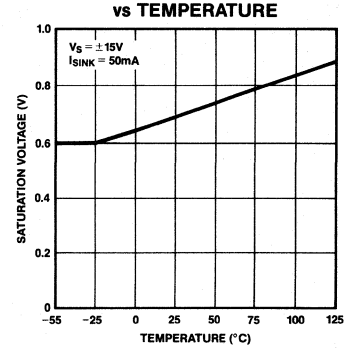
COMMON-MODE LIMITS vs TEMPERATURE



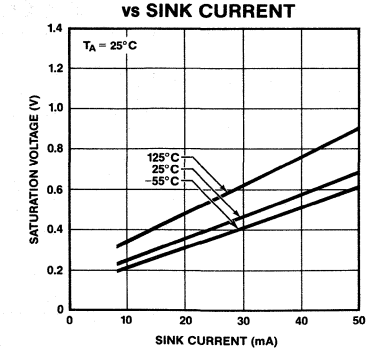
TRANSFER FUNCTION



SATURATION VOLTAGE vs TEMPERATURE

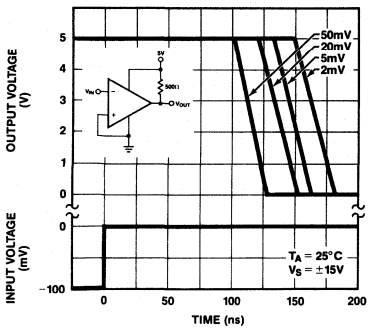


SATURATION VOLTAGE vs SINK CURRENT

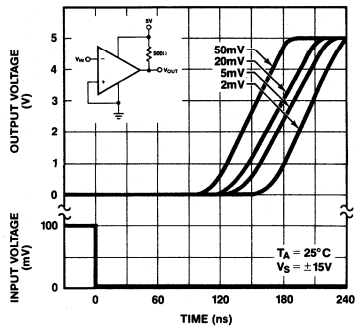


TYPICAL PERFORMANCE CHARACTERISTICS

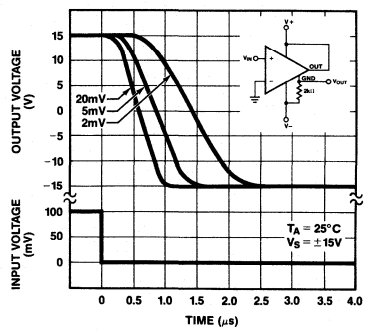
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



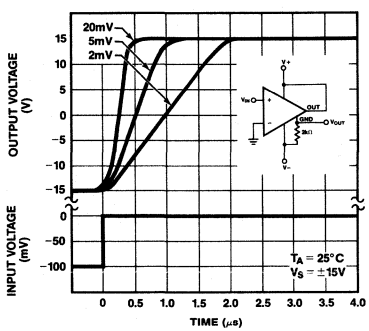
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



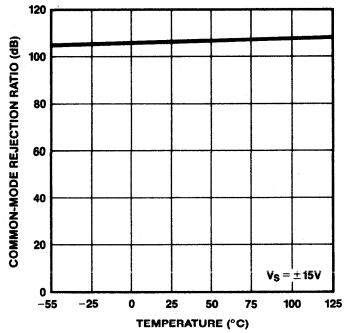
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



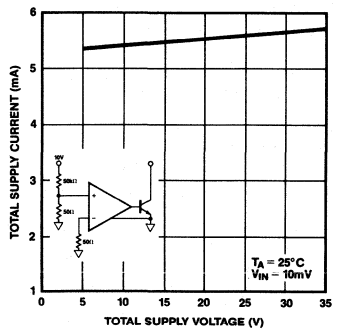
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



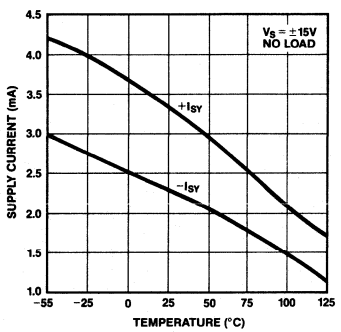
COMMON-MODE REJECTION RATIO vs TEMPERATURE



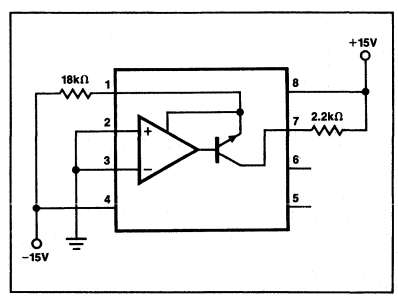
TOTAL SUPPLY CURRENT vs TOTAL SUPPLY VOLTAGE



SUPPLY CURRENT vs TEMPERATURE



BURN-IN CIRCUIT



ANALOG DEVICES

Quad Low-Power Voltage Comparators

PM-139/PM-139A/PM-239

FEATURES

- **Single or Dual Supply Operation**
- **Input Voltage Range Includes Ground**
- **Low Power Consumption (2mW/Comparator)**
- **Low Input Bias Current 25nA**
- **Low Input Offset Current ..... ±5nA**
- **Low Offset Voltage ..... ±2mV**
- **Low Output Saturation Voltage (250mV @ 4mA)**
- **Logic Outputs Compatible with TTL, DTL, ECL, MOS, and CMOS**
- **Directly Replaces LM139 and LM139A Comparators**
- **Available in Die Form**

ORDERING INFORMATION †

+25°C V_{OS} (mV)	PACKAGE DIP 14-PIN	PACKAGE LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
±2*	PM139AY*	PM139ARC/883	MIL
±5*	PM139Y*	–	MIL
±5	PM239P	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

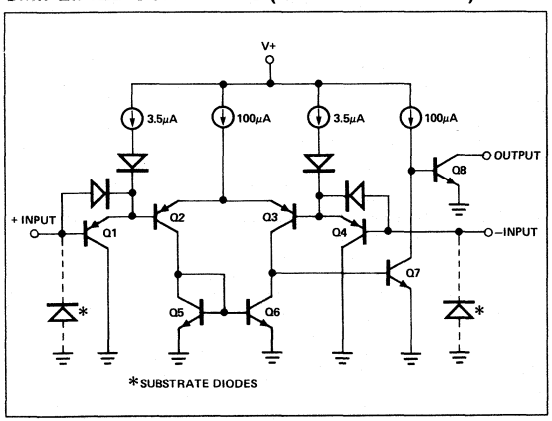
JAN ORDERING INFORMATION

JAN PART NUMBER	DESCRIPTION
JM38510/11201BCA	PM139Y5/38510 LEVEL B
JM38510/11201BCB	PM139Y2/38510 LEVEL B
JM38510/11201SCA*	PM139Y5/38510 LEVEL S

Table above is for MIL-M-38510 processing. Refer to 11201 slash sheet for electrical processing parameters.

* Undergoing Part I qualification. Consult ADI for availability.

SIMPLIFIED SCHEMATIC (ONE COMPARATOR)

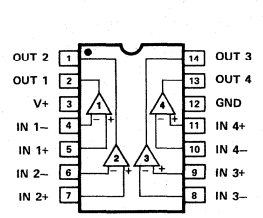


GENERAL DESCRIPTION

The PM-139 has four independent voltage comparators, each with precision DC specifications. Low offset voltage, bias current, power consumption and output saturation voltage are offered in a design that features single power supply operation. The input voltage range includes ground for convenient single supply operation. The 2mA power supply current, independent of supply voltage – coupled with the single supply operation, makes this comparator ideal for low power applications. Open collector outputs allow maximum applications flexibility.

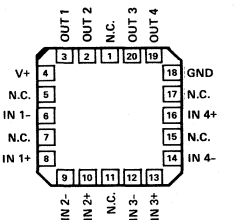
3

PIN CONNECTIONS



14-PIN HERMETIC DIP (Y-Suffix)

14-PIN PLASTIC DIP (P-Suffix)



PM-139ARC/883 LCC PACKAGE (RC-Suffix)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V+ ..... 36V or ±18V
Differential Input Voltage 36V
Input Voltage ..... –0.3V to +36V
Derate Above 100°C ..... 10mW/°C
Output Short-Circuit to Ground ..... Continuous
Input Current (V_{IN} < –0.3V) 50mA
Operating Temperature Range
PM-139A/139/139ARC ..... –55°C to +125°C
PM-239P ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
Junction Temperature ..... +150°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
14-Pin Hermetic DIP (Y)	110	26	°C/W
14-Pin Plastic DIP (P)	90	47	°C/W

NOTE:

1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages.

ELECTRICAL CHARACTERISTICS at V+ = +5V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-139A MIN	PM-139A TYP	PM-139A MAX	PM-139/239 MIN	PM-139/239 TYP	PM-139/239 MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	1	2	—	2	5	mV
Input Bias Current	I_B	$I_{IN}(+)$ or $I_{IN}(-)$ with Output in Linear Range	—	25	100	—	25	100	nA
Input Offset Current	I_{OS}	$I_{IN}(+)$ or $I_{IN}(-)$	—	3	25	—	3	25	nA
Input Common-Mode Voltage Range	CMVR	(Notes 2, 5, 6)	0	—	3.5	0	—	3.5	V
Supply Current	I_S	$R_L = \infty$ on all Comparators V+ = 30V	—	0.8	2	—	0.8	2	mA
Voltage Gain	A_{VO}	$R_L \geq 15k\Omega$, V+ = 15V (To support large V_O swing) (Note 5)	50	200	—	50	200	—	V/mV
Large-Signal Response Time	t_r	V_{IN} = TTL Logic Swing, V_{REF} = 1.4V, V_{RL} = 5V, R_L = 5.1kΩ, (Note 4)	—	300	—	—	300	—	ns
Response Time	t_r	V_{RL} = 5V, R_L = 5.1kΩ (Notes 3, 4)	—	1.3	—	—	1.3	—	μs
Output Sink Current	I_{SINK}	$V_{IN}(-) \geq 1V$, $V_{IN}(+) = 0$, $V_O \leq 1.5V$	6	16	—	6	16	—	mA
Saturation Voltage	V_{OL}	$V_{IN}(-) \geq 1V$, $V_{IN}(+) = 0$, $I_{SINK} \leq 4mA$	—	250	400	—	250	400	mV
Output Leakage Current	I_{LEAK}	$V_{IN}(+) \geq 1V$, $V_{IN}(-) = 0$, V_O = 30V	—	0.1	—	—	0.1	—	nA

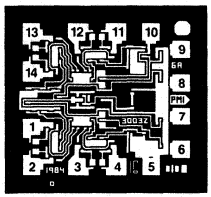
ELECTRICAL CHARACTERISTICS at V+ = +5V, −55°C ≤ T_A ≤ +125°C for PM-139A and PM-139, −40°C ≤ T_A ≤ +85°C for PM-239, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-139A MIN	PM-139A TYP	PM-139A MAX	PM-139/239 MIN	PM-139/239 TYP	PM-139/239 MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	—	—	4	—	—	9	mV
Input Offset Current	I_{OS}	$I_{IN}(+)$ or $I_{IN}(-)$	—	—	100	—	—	100	nA
Input Bias Current	I_B	$I_{IN}(+)$ OR $I_{IN}(-)$ with Output in Linear Range	—	—	300	—	—	300	nA
Input Common-Mode Voltage Range	CMVR	(Notes 3, 5)	0	—	V+ −2	0	—	V+ −2	V
Saturation Voltage	V_{OL}	$V_{IN}(-) \geq 1V$, $V_{IN}(+) = 0$, $I_{SINK} \leq 4mA$	—	—	700	—	—	700	mV
Output Leakage Current	I_{LEAK}	$V_{IN}(+) \geq 1V$, $V_{IN}(-) = 0$, V_O = 30V	—	—	1	—	—	1	μA
Differential Input Voltage		Keep All $V_{IN's} \geq 0V$	—	—	36	—	—	36	V

NOTES:

1. At output switch point, V_O = 1.4V, R_S = 0Ω with V+ from 5V, and over the full input common-mode range (0V to V+ −1.5V).
2. The input common-mode voltage or either input voltage signal should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ −1.5V, but either or both inputs can go to +30V without damage.
3. The response time specified is for a 100mV input step with 5mV overdrive. For larger overdrive signals 300ns can be obtained. See characteristics section.
4. Sample tested.
5. Guaranteed by design.
6. Positive CMVR limit equals V+ −1.5V for supply voltages other than 5V.

DICE CHARACTERISTICS



DIE SIZE 0.051 × 0.048 inch, 2448 sq. mils (1.295 × 1.220 mm, 1.58 sq. mm)

1. OUTPUT (2)
2. OUTPUT (1)
3. POSITIVE SUPPLY
4. INVERTING INPUT (1)
5. NONINVERTING INPUT (1)
6. INVERTING INPUT (2)
7. NONINVERTING INPUT (2)
8. INVERTING INPUT (3)
9. NONINVERTING INPUT (3)
10. INVERTING INPUT (4)
11. NONINVERTING INPUT (4)
12. GROUND (SUBSTRATE)
13. OUTPUT (4)
14. OUTPUT (3)

3

WAFER TEST LIMITS at V+ = +5V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-139N LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S = 0\Omega$, $R_L = 5.1k\Omega$ $V_O = 1.4V$, (Note 1)	2	mV MAX
Input Offset Current	I_{OS}	$I_{IN}(+) - I_{IN}(-)$ $R_L = 5.1k\Omega$ $V_O = 1.4V$	25	nA MAX
Input Bias Current	I_B	$I_{IN}(+)$ or $I_{IN}(-)$, (Note 1)	100	nA MAX
Voltage Gain	A_V	$R_L \geq 15k\Omega$, V+ = 15V, (Note 3)	50	V/mV MIN
Input Voltage Range	CMVR	(Notes 2, 3)	V+ − 1.5	V MAX
Common-Mode Rejection Ratio	CMRR	(Note 4)	60.5	dB MIN
Power Supply Rejection Ratio	PSRR	V+ = 5V to +18V	60.5	dB MIN
Saturation Voltage	V_{OL}	$V_{IN}(-) \geq 1V$, $V_{IN}(+) = 0$, $I_{SINK} \leq 4mA$	400	mV MAX
Output Sink Current	I_{SINK}	$V_{IN}(-) \geq 1V$, $V_{IN}(+) = 0$, $V_O \leq 1.5V$	6	mA MIN
Output Leakage Current	I_{LEAK}	$V_{IN}(+) \geq 1V$, $V_{IN}(-) = 0$, $V_O = 30V$	500	nA MAX
Supply Current	I+	$R_L = \infty$, All Comps V+ = 30V	2	mA MAX

NOTES:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

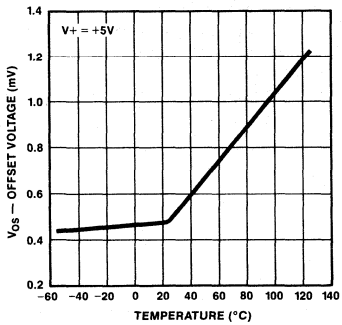
TYPICAL ELECTRICAL CHARACTERISTICS at V+ = +5V, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-139N TYPICAL	UNITS
Large-Signal Response Time	t_r	V_{IN} = TTL Logic Swing $V_{REF} = 1.4V$, (Note 5) $V_{RL} = 5V$, $R_L = 5.1k\Omega$	600	ns
Small-Signal Response Time	t_r	V_{IN} = 100mV Step, (Note 5) 5mV Overdrive $V_{RL} = 5V$, $R_L = 5.1k\Omega$	1.3	μs

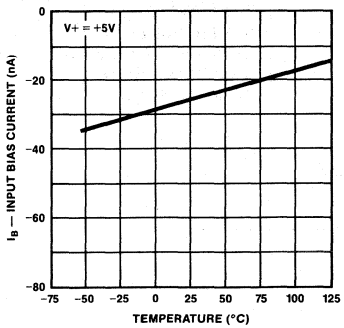
NOTES:
1. At output switch point, $V_O = 1.4V$, $R_S = 0\Omega$ with V+ from 5V; and over the full input common-mode range (0V to V+ − 1.5V).
2. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ − 1.5V, but either or both inputs can go to +30V without damage.
3. Guaranteed by design.
4. $R_L \geq 15k\Omega$. V_{CM} = 1.5V to 13.5V, V+ = 15V.
5. Sample tested.

TYPICAL PERFORMANCE CHARACTERISTICS

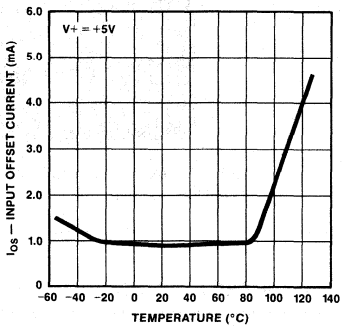
OFFSET VOLTAGE vs TEMPERATURE



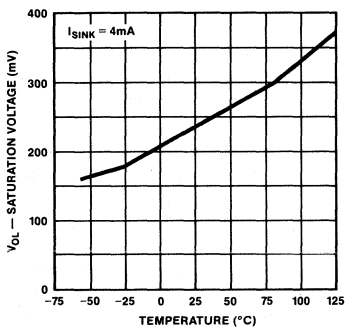
INPUT BIAS CURRENT vs TEMPERATURE



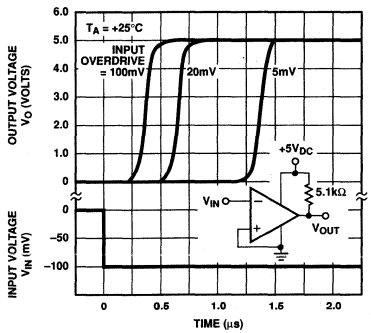
INPUT OFFSET CURRENT vs TEMPERATURE



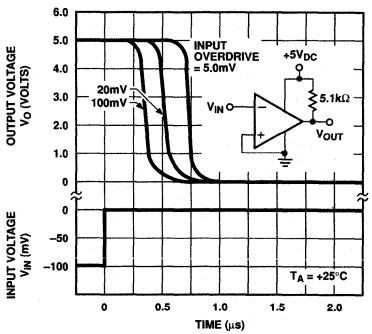
SATURATION VOLTAGE vs TEMPERATURE



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES — POSITIVE TRANSITION

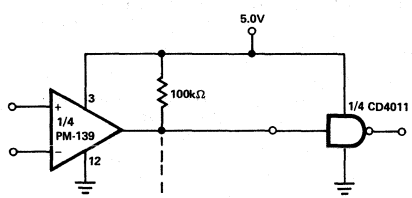


RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES — NEGATIVE TRANSITION

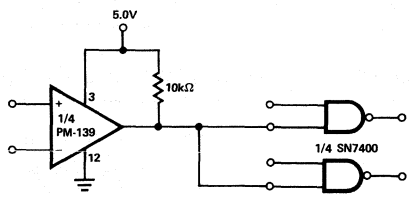


TYPICAL INTERFACE

DRIVING CMOS

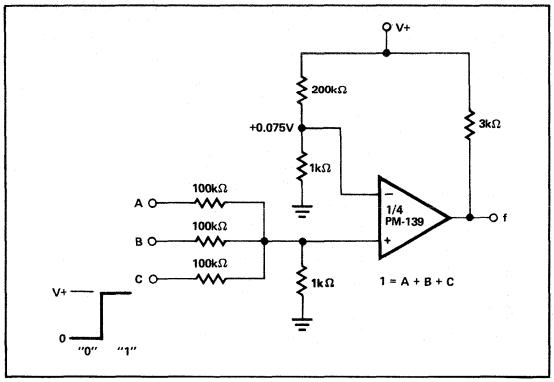


DRIVING TTL

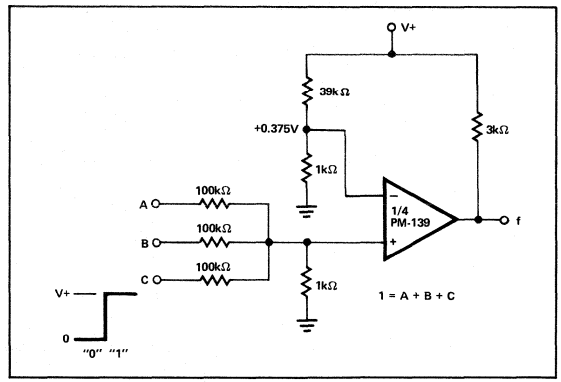


TYPICAL APPLICATIONS

OR GATE

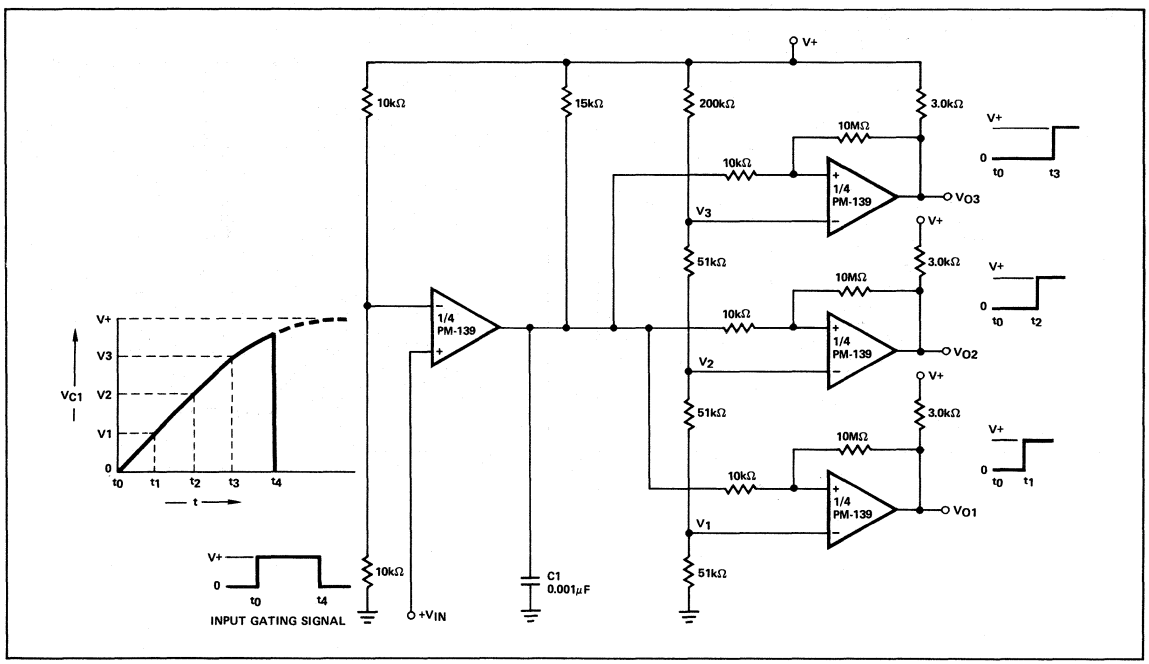


AND GATE



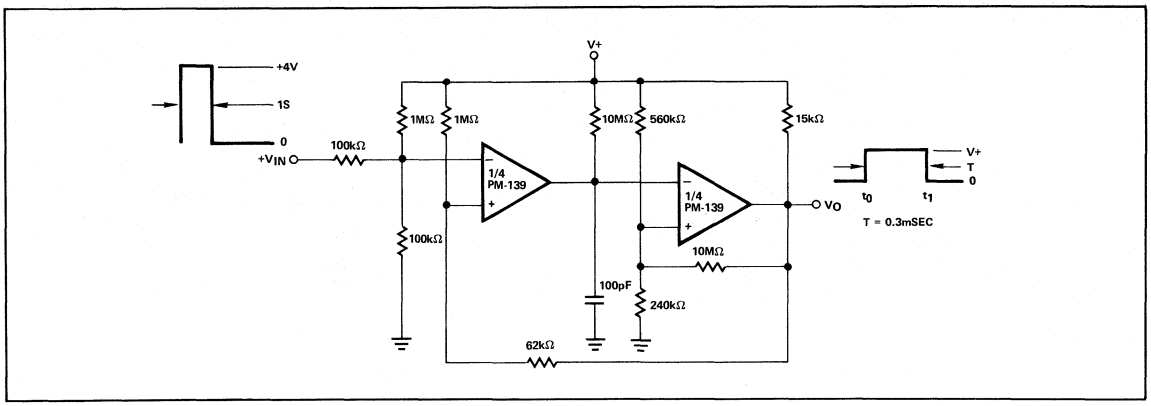
3

TIME DELAY GENERATOR

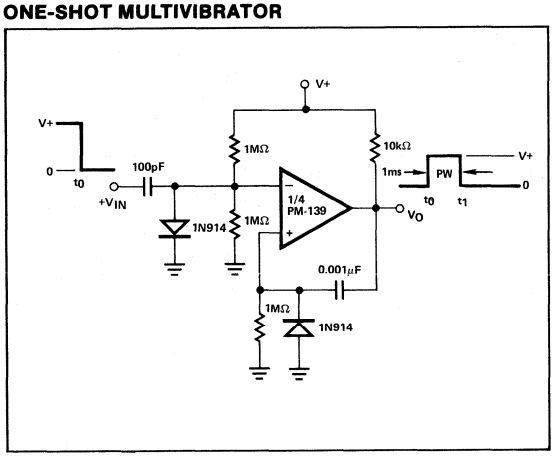


TYPICAL APPLICATIONS

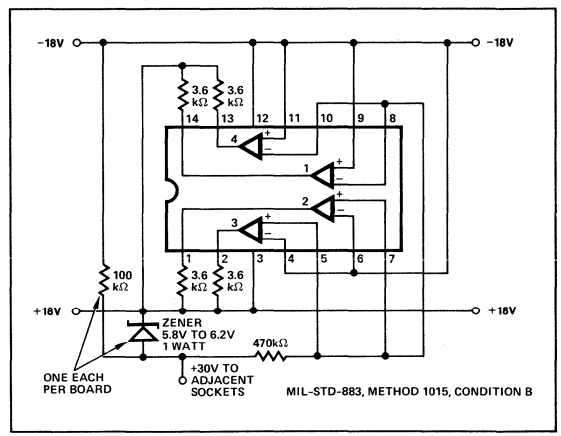
ONE-SHOT MULTIVIBRATOR WITH INPUT LOCK-OUT



ONE-SHOT MULTIVIBRATOR



BURN-IN CIRCUIT



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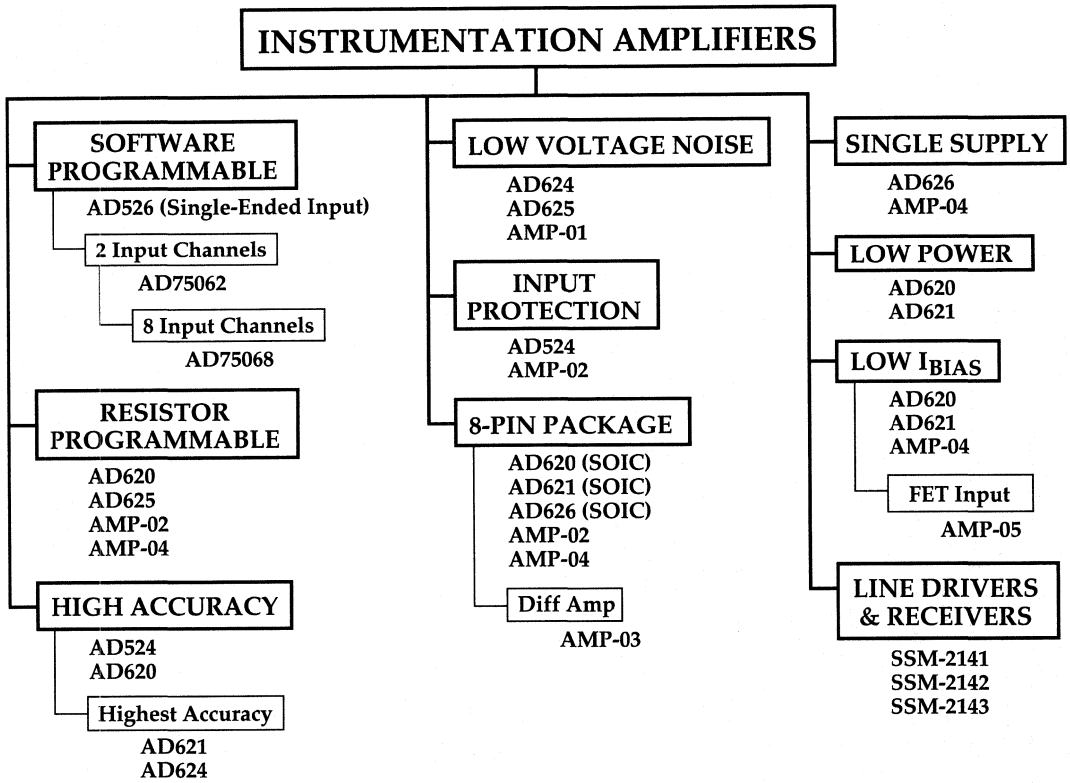
Selection Tree
Instrumentation Amplifiers



Selection Guide
Instrumentation Amplifiers

Model	Gain Ranges	Gain Error % max	Gain TC ppm/°C max	BW MHz typ[1]	Package Options[2]	Temp Range[3]	Page[4]	Comments
AD526	**1, 2, 4, 8, 16**	**0.01–0.15**	**2–5**	**4.0**	**1, 2**	**C, I, M**	**4-39**	**Software Programmable, µP Interface**
AD624	**1, 100, 200, 500, 1000**	**0.02–1.0**	**5–25**	**1.0**	**1**	**I, M**	**4-71**	**Pin Programmable**
AD524	**1, 10, 100, 1000**	**0.02–2.0**	**5–100**	**1.0**	**1, 4**	**I, M**	**4-27**	**Pin Programmable, Input Protection**
AD625	**1–10,000**	**0.02–0.05**	**5**	**0.65**	**1, 2**	**C, I, M**	**4-83**	**Resistor Programmable, Low Cost**
AMP-02	**1–10,000**	**0.02**	**50**	**1.20**	**2, 3, 6**	**I, M**	**4-137**	**High Accuracy, 8-Pin Package Single Resistor Gain Set**
***AD620**	**1–1,000**	**0.02–0.10**	**50**	**1.0**	**2, 3, 6**	**I, M**	**4-51**	**Low Cost in an 8-Pin SOIC**
AD365	1, 10, 100, 500	0.05–0.1	5–10	0.8	8	I	4-9	Digitally Programmable with T/H
***AD621**	**10, 100**	**0.05–0.1**	**5–10**	**0.8**	**2, 3, 6**	**I, M**	**4-67**	**Low Cost, Precision, 8-Pin SOIC**
AD522	1–10,000	0.05–1.0	2–50	0.3	1	I, M	4-23	Resistor Programmable
AMP-01	**0.1–1000**	**0.6**	**10**	**0.57**	**3, 4, 6**	**C, I, M**	**4-115**	**Low Noise, Precision**
AMP-05	0.1–2000	0.5	20	3.0	3	I, M	4-165	JFET Input, Fast Settling
***AD626**	**10, 100**	**0.2**	**150**	**0.1**	**2, 3, 6**	**I, M**	**4-95**	**Single Supply, High CMV**
AD521	0.1–1000	0.25–3.0	3–50	2	1	C, M	4-17	Resistor Programmable
AMP-03	**1**	**0.008**	**—**	**3.0**	**1.7**	**I, M**	**4-149**	**Precision Unity-Gain Differential Amplifier**
***AMP-04**	**1–1,000**	**0.5%**	**—**	**0.3**	**2, 6**	**I, M**	**4-159**	**Precision, Single Supply**
SSM-2016	1–1,000	0.3 (dB)	—	1	2	C	4-185	Ultralow Noise Differential Amplifier
SSM-2017	1–1,000	0.1 (dB)	—	4	2, 3, 6	I	4-193	Self-Contained Audio Preamplifier
SSM-2141	1	0.01	—	3	2, 6	I	4-201, AV	High Common-Mode Rejection Differential Line Receiver
SSM-2142	2	2	—	—	2, 6	I	4-207, AV	Balanced Line Driver
***SSM-2143**	**1/2, 2**	**0.1**	**–**	**7.0**	**2, 6**	**I**	**4-213, AV**	**Gain of 0.5 for Unity Gain System When Used with SSM-2142**

[1]Unity gain small signal bandwidth.
[2]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack, 11 = Single-in-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92; 17 = Plastic Pin Grid Array.
[3]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.
[4]AV = *Audio/Video Reference Manual*.
Boldface Type: Product recommended for new design.
*New product.

Orientation
Instrumentation Amplifiers

What Is an Instrumentation Amplifier?
An instrumentation amplifier is a closed-loop gain block which has a differential input and an output which is singled-ended with respect to a reference terminal. Most commonly, the impedances of the two input terminals are balanced and have high values, typically 10^9 Ω or greater. As with op amps, output impedance is very low, nominally only a few milliohms. Unlike an op amp, which has its closed-loop gain determined by external resistors connected between its inverting input and its output, an in amp employs an internal feedback resistor network which is isolated from its signal input terminals. With the input signal applied across the two differential inputs, gain is either preset internally or is user-set by an internal (via pins) or external gain resistor, which is also isolated from the signal inputs. Figure 1 contrasts the differences between op-amp and in-amp input characteristics.

Common-mode rejection, the property of cancelling out any signals which are common (the same potential on both inputs) while amplifying any signals which are differential (a potential difference between the inputs), is the most important function an instrumentation amplifier provides. Common-mode gain (A_{CM}) is the ratio of change in output voltage to a change in common-mode input voltage. This is the net gain (or attenuation) from input to output for voltages common to both inputs. For example, an in amp with a common-mode gain of 1/1,000 and a 10 volt common-mode voltage at its inputs will exhibit a 10 mV output change. The differential or "normal mode" gain (A_D) is the gain between input and output for voltages applied differentially (or across) the two inputs. The common-mode rejection ratio (CMRR) is simply the ratio of the differential gain (A_D) to the common-mode gain (A_{CM}).

Common-mode rejection is usually specified for a full-range common-mode voltage (CMV) change at a given frequency, and a specified imbalance of source impedance (e.g., 1 kΩ source unbalance, at 60 Hz). The term CMR is a logarithmic expression of the common-mode rejection ratio (CMRR).

That is: $CMR = 20\ Log_{10}\ CMRR$.

In order to be effective, an in amp needs to be able to amplify microvolt-level signals while simultaneously rejecting volts of common-mode at its inputs.

This requires that instrumentation amplifiers have very high common-mode rejection—typical values of CMR are 70 dB to over 100 dB, with CMR usually improving at higher gains. While it is true that operational amplifiers, connected as subtractors, also provide common-mode rejection, the user must provide closely matched external resistors. On the other hand, monolithic in amps with their pretrimmed resistor networks, are far easier to apply.

For a comprehensive discussion of in amp theory and applications, refer to the *Instrumentation Amplifier Application Guide*, available FREE from Analog Devices.

INSTRUMENTATION AMPLIFIER SPECIFICATIONS
To successfully apply any electronic component, a full understanding of its specifications is required. That is to say, the numbers contained in a spec sheet are of little value if the user doesn't have a clear picture of what each spec means. A typical monolithic instrumentation amplifier specification sheet will be reviewed along with some of its more important specifications. These will be discussed in terms of how they are measured and what errors they might contribute to the overall performance of the circuit.

The following table shows a portion of the specification sheet for the Analog Devices AD620 instrumentation amplifier.

A → AD620—SPECIFICATIONS (typical @ +25°C, V_S = ±15 V, and R_L = 2 kΩ unless otherwise specified)

	Model	Conditions	AD620A Min	AD620A Typ	AD620A Max	AD620B Min	AD620B Typ	AD620B Max	AD620S Min	AD620S Typ	AD620S Max	Units
B →	GAIN	G = 1 + (49.4 k/R_G)										
C →	Gain Range		1		10,000	1		10,000	1		10,000	
D →	Gain Error[1]	V_{OUT} = ±10 V										
	G = 1			0.03	0.10		0.01	0.02		0.03	0.10	%
	G = 10			0.15	0.30		0.10	0.15		0.15	0.30	%
	G = 100			0.15	0.30		0.10	0.15		0.15	0.30	%
	G = 1000			0.40	0.70		0.35	0.50		0.40	0.70	%
E →	Nonlinearity,	V_{OUT} = −10 V to +10 V,										
	G = 1–1000	R_L = 10 kΩ		10	40		10	40		10	40	ppm
	G = 1–100	R_L = 2 kΩ		10	95		10	95		10	95	ppm
F →	Gain vs. Temperature	Gain <1000			−50			−50			−50	ppm/°C
G →	VOLTAGE OFFSET	(Total RTI Error = V_{OSI} + V_{OSO}/G)										
	Input Offset, V_{OSI}	V_S = ±5 V to ±15 V		30	125		15	50		30	125	µV
	over Temperature	V_S = ±5 V to ±15 V			185			85			225	µV
	Average TC	V_S = ±5 V to ±15 V		0.3	1.0		0.1	0.6		0.3	1.0	µV/°C
	Output Offset, V_{OSO}	V_S = ±15 V		400	1000		200	500		400	1000	µV
		V_S = +5 V			1500			750			1500	µV
	over Temperature	V_S = ±5 V to ±15 V			2000			1000			2000	µV
	Average TC	V_S = ±5 V to ±15 V		5.0	15		2.5	7.0		5.0	15	µV/°C
	Offset Referred to the Input vs. Supply (PSR)	V_S = ±2 V to ±18 V										
	G = 1		80	100		80	100		80	100		dB
	G = 10		95	120		100	120		95	120		dB
	G = 100		110	140		120	140		110	140		dB
	G = 1000		110	140		120	140		110	140		dB
H →	INPUT CURRENT											
	Input Bias Current			0.5	2.0		0.5	1.0		0.5	2	nA
	over Temperature				2.5			1.5			4	nA
	Average TC			3.0			3.0			8.0		pA/°C
	Input Offset Current			0.3	1.0		0.3	0.5		0.3	1.0	nA
	over Temperature				1.5			0.75			2.0	nA
	Average TC			1.5			1.5			8.0		pA/°C
	INPUT											
	Input Impedance											
	Differential			10‖2			10‖2			10‖2		GΩ‖pF
	Common-Mode			10‖2			10‖2			10‖2		GΩ‖pF
	Input Voltage Range	V_S = ±2.3 V to ±5 V	$-V_S$ + 1.9		$+V_S$ − 1.2	$-V_S$ + 1.9		$+V_S$ − 1.2	$-V_S$ + 1.9		$+V_S$ − 1.2	V
	over Temperature		$-V_S$ + 2.1		$+V_S$ − 1.3	$-V_S$ + 2.1		$+V_S$ − 1.3	$-V_S$ + 2.1		$+V_S$ − 1.3	V
		V_S = ±5 V to ±18 V	$-V_S$ + 1.9		$+V_S$ − 1.4	$-V_S$ + 1.9		$+V_S$ − 1.4	$-V_S$ + 1.9		$+V_S$ − 1.4	V
	over Temperature		$-V_S$ + 2.1		$+V_S$ − 1.4	$-V_S$ + 2.1		$+V_S$ − 1.4	$-V_S$ + 2.3		$+V_S$ − 1.4	V
I →	Common-Mode Rejection Ratio DC to 60 Hz with 1 kΩ Source Imbalance	V_{CM} = 0 V to ±10 V										
	G = 1		73	90		80	90		73	90		dB
	G = 10		93	110		100	110		93	110		dB
	G = 100		110	130		120	130		110	130		dB
	G = 1000		110	130		120	130		110	130		dB
	OUTPUT											
	Output Swing	R_L = 10 kΩ,										
		V_S = ±2.3 V to ±5 V	$-V_S$ + 1.1		$+V_S$ − 1.2	$-V_S$ + 1.1		$+V_S$ − 1.2	$-V_S$ + 1.1		$+V_S$ − 1.2	V
	over Temperature		$-V_S$ + 1.4		$+V_S$ − 1.3	$-V_S$ + 1.4		$+V_S$ − 1.3	$-V_S$ + 1.6		$+V_S$ − 1.3	V
		V_S = ±5 V to ±18 V	$-V_S$ + 1.2		$+V_S$ − 1.4	$-V_S$ + 1.2		$+V_S$ − 1.4	$-V_S$ + 1.2		$+V_S$ − 1.4	V
	over Temperature		$-V_S$ + 1.6		$+V_S$ − 1.5	$-V_S$ + 1.6		$+V_S$ − 1.5	$-V_S$ + 2.3		$+V_S$ − 1.5	V
	Short Current Circuit			±18			±18			±18		mA
	DYNAMIC RESPONSE											
	Small Signal −3 dB Bandwidth											
	G = 1			1000			1000			1000		kHz
	G = 10			800			800			800		kHz
	G = 100			120			120			120		kHz
	G = 1000			12			12			12		kHz
	Slew Rate		0.75	1.2		0.75	1.2		0.75	1.2		V/µs
J →	Settling Time to 0.01%	10 V Step										
	G = 1–100			15			15			15		µs
	G = 1000			150			150			150		µs

(A) Conditions

At the top of the spec sheet is the statement that the listed specs are typical @ $V_S = \pm 15$ V, $R_L = 2$ kΩ and $T_A = +25°C$ unless otherwise specified. This tells the user that these are the normal operating conditions under which the device is tested. Deviations from these conditions might degrade (or improve) performance. When deviations from the "normal" conditions are likely (such as a change in temperature) the significant effects are usually indicated within the specs. This statement also tells us that all numbers are typical unless noted; "typical" means that the manufacturers characterization process has shown this number to be average, but individual devices may vary.

Specifications not discussed in detail are self-explanatory and require only a basic knowledge of electronic measurements. Those specs do not apply uniquely to instrumentation amplifiers.

(B) Gain

These specifications relate to the transfer function of the device. The gain equation of the AD620 is:

$$Gain = 1 + \frac{49.4\ k\Omega}{R_G}$$

To select an R_G for a given gain, solve the equation for R_G:

$$R_G = \frac{49{,}400\ \Omega}{GAIN - 1}$$

For example, the calculated resistance and the closest standard value for some common gains:

$G = 1$: $R_G = \infty$ (*Open Circuit*)
$G = 10$: $R_G = 5.49\ k\Omega$
$G = 100$: $R_G = 499\ \Omega$
$G = 1000$: $R_G = 49.5$ (*cal*) *or* $49.9\ \Omega$

Note that there will be a gain error if the standard resistance values are different from those calculated. In addition, the tolerance of the resistors used (normally 1% metal film) will also affect accuracy. Of course the user must provide a very clean (low leakage) circuit board to realize an accurate gain of 1, since even a 200 MΩ leakage resistance will cause a gain error of 0.1%!

Note that resistor tolerance must be taken into consideration. Normal metal film resistors are within 1% of their stated value which means that any two resistors could be as much as 2% different in value from one another. Thin-film resistors in monolithic integrated circuits have an absolute tolerance of only ±20%, however the matching between resistors on the same chip can be excellent: typically better than 0.1%.

(C) Gain Range

Often specified as having a gain range of 1 to 1000, or 1 to 10,000, many instrumentation amplifiers may (and in fact will) work at higher gains, but the manufacturer will not promise a specific level of performance. In practice, as the gain resistor becomes increasingly smaller, any errors due to the resistance of the metal runs and bond wires become significant. These errors, along with an increase in noise and drift, may make higher gains impractical.

(D) Gain Error

The number given by this specification describes maximum deviation from the gain equation. Monolithic in-amps such as the AD620 have very low factory trimmed gain errors with its maximum error of ±0.02% at unity gain and ±0.50% at a gain of 1000 being typical for a high quality in-amp. Although externally connected gain networks allow the user to set the gain exactly, the temperature coefficients of the external resistors and the temperature differences between individual resistors within the network, all contribute to the overall gain error.

If the data is eventually digitized and fed to an "intelligent system" (such as a microprocessor), it may be possible to correct for gain errors by measuring a known reference voltage and then multiplying by a constant.

(E) Nonlinearity

Nonlinearity is defined as the deviation from a straight line on the plot of output versus input. Figure 1 shows the transfer function of a device with exaggerated nonlinearity. The magnitude of this error can be calculated by:

$$Nonlinearity = \frac{Actual\ Output - Calculated\ Output}{Rated\ Full\text{-}Scale\ Output\ Range}$$

To confuse matters, this deviation can be specified relative to any straight line or to a specific straight line. There are two commonly used methods of specifying this ideal straight line relative to the performance of a precision measurement device.

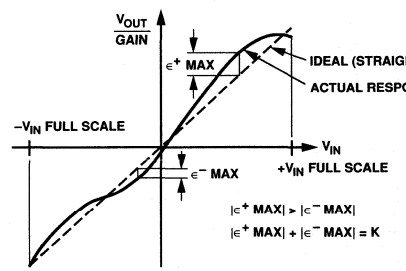


Figure 1. Transfer Function Illustrating Exaggerated Nonlinearity

The "Best Straight Line" method of nonlinearity specification consists of measuring the peak positive and peak negative deviations and then adjusting the slope of the device transfer function (by adjusting the gain and offset) so that these maximum positive and negative errors are equal. This method yields the best specifications but is difficult to implement because it requires that the user examine the entire output signal range to determine these maximum positive and negative deviations. The results of a best-straight-line calibration is shown by the transfer function of Figure 2.

The "End-Point" method of specifying nonlinearity requires that the user perform his offset and/or gain calibrations at the extremes of the output range. This is much easier to implement but may result in nonlinearity errors of up to twice those attained with best-straight-line techniques. This worst case error will occur when the transfer function is "bowed" in one direction only. Figure 3 shows the results of end-point calibration.

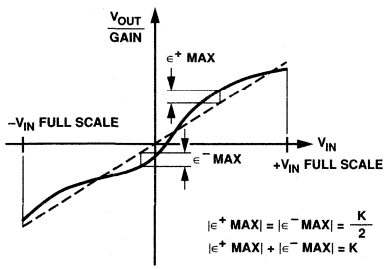


Figure 2. The Transfer Function of Figure 1 After Calibration by Best-Straight-Line Method

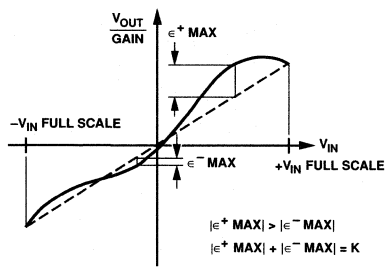


Figure 3. The Transfer Function of Figure 1 After Calibration by End-Point Method

Most linear devices, such as instrumentation amplifiers, are specified for best-straight-line linearity. This needs to be considered when evaluating the error budget for a particular application.

Regardless of the method used to specify nonlinearity, the errors thus created are irreducible. That is to say: these are neither fixed errors nor are they proportional to input or output voltage and, therefore, **cannot** be reduced by adjustment.

(F) Gain vs. Temperature
These numbers give both maximum and typical deviations from the gain equation as a function of temperature. An intelligent system can correct for this with an "auto-gain" cycle (measure a reference and renormalize).

(G) Voltage Offset
Voltage offset specifications are often considered a figure of merit for instrumentation amplifiers. While initial offset may be adjusted to zero, shifts in offset voltage due to temperature variations will cause errors. Intelligent systems can often correct for this factor with an auto-zero cycle, but there are many small-signal high-gain applications that don't have this capability.

Voltage offset and drift comprise two components each; input and output offset and offset drift referred to both input and output. Input offset is that component of offset that is directly proportional to gain, i.e., input offset as measured at the output at G = 100 is 100 times greater that at G = 1. Output offset is independent of gain. At low gains, output offset drift is dominant, while at high gains input offset drift dominates. Therefore, the output offset voltage drift is normally specified as drift at G = 1 (where input effects are insignificant), while input offset voltage drift is given by drift specification at a high gain (where output offset effects are negligible). All input-related numbers are referred to the input (RTI) which is to say that the effect on the output is "G" times larger. Voltage offset vs. power supply is also specified at one or more gain settings and is also RTI.

(H) Input Current
Input bias currents are those currents necessary to bias the input transistors of a dc amplifier. FET input devices have lower bias currents, but those currents increase dramatically with temperature, doubling approximately every 11°C. Since bias currents can be considered as a source of voltage offset (when multiplied by source resistance), the change in bias currents is of more concern than the magnitude of the bias currents. Input offset current is the difference between the two input bias currents.

Although instrumentation amplifiers have differential inputs, there must be a return path for the bias currents. If this is not provided, those currents will charge stray capacitances, which will cause the output to drift uncontrollably or to saturate. Therefore, when amplifying "floating" input sources such as transformers and thermocouples, as well as ac-coupled sources, there must still be a dc path from each input to ground.

(I) Common-Mode Rejection
Common-mode rejection is a measure of the change in output voltage when both inputs are changed equal amounts. These specifications are usually given for both a full-range input voltage change and for a specified source imbalance. Common-mode rejection ratio (CMRR) is a ratio expression while common-mode rejection (CMR) is the logarithm of that ratio. For example, a CMRR of 10,000 corresponds to a CMR of 80 dB.

In most IAs, the CMRR increases with gain. This is because most designs have a front-end configuration that does not amplify common-mode signals. Since the standard for CMRR specifications is referred to the output (RTO), a gain for differential signals in the total absence of gain for common-mode input signals will yield a 1-to-1 improvement of CMRR with gain. For example, if an instrumentation amplifier provides a CMR of 60 dB at unity gain, then increasing the amplifier's gain to 10 will increase the differential gain 10 times. But, (ideally) the common-mode gain will remain at unity. Therefore, the CMR is now 80 dB—a direct improvement with gain.

This means that the common-mode output error signal will not increase with gain, it does not mean that it decreases with gain! At higher gains, however, amplifier bandwidth does decrease. Since differences in phase shift through the differential input stage will show up as a common-mode error, CMRR becomes more frequency dependent at high gains.

(J) Settling Time
Settling time is defined as that length of time required for the output voltage to approach and remain within a certain tolerance of its final value. It is usually specified for a fast full-scale input step and includes output slewing time. Since several factors contribute to the overall setting time, fast settling to 0.1% doesn't necessarily mean proportionally fast settling to 0.01%. In addition, settling time is not necessarily a function of gain. Some of the contributing factors include slew rate limiting, underdamping (ringing) and thermal gradients (long tails).

Programmable Gain & T/H DAS Amplifier

AD365

FEATURES

Software Programmable Gain (1, 10, 100, 500)
Low Input Noise (0.2μV p-p)
Low Gain Error (0.05% max)
Low Nonlinearity (0.005% max)
Low Gain Drift (10ppm/°C max)
Low Offset Drift (2μV/°C RTI max)
Fast Settling (15μs @ Gain 100)
Small 16-Pin Metal DIP

APPLICATIONS

Digitally Controlled Gain Amplifier
Auto-Gain Ranging Amplifier
Wide Dynamic Range Measurement System
Gain Selection/Channel Amplifier
Transducer/Bridge Amplifier
Test Equipment

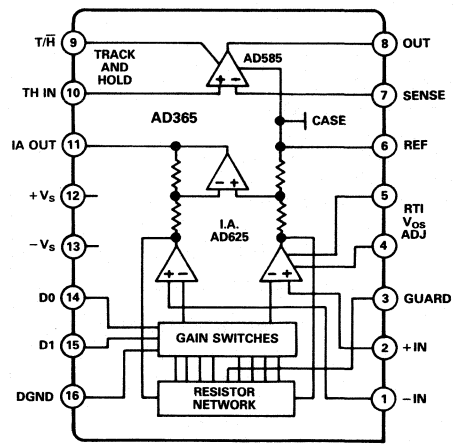
HIGHLIGHTS

The AD365 is a two stage data acquisition system (DAS) front end consisting of a digitally selectable gain amplifier followed by an independent track/hold amplifier. The programmable gain amplifier features differential inputs for excellent common-mode rejection, high open loop gain for superior linearity, and fast settling for use in multiplexed high speed systems. The track/hold amplifier features high open loop gain for 12-bit compatible linearity, internal hold capacitor for high reliability, and fast acquisition time for use with multichannel systems. Both amplifiers are capable of being used separately and are specified as independent function blocks.

GENERAL DESCRIPTION

The AD365 is comprised of the AD625 monolithic precision instrumentation amplifier to provide a precision differential input, the AD7502 monolithic CMOS multiplexer to handle gain switching, a precision thin-film resistor network, and the AD585 monolithic track and hold amplifier with internal hold capacitor.

FUNCTIONAL BLOCK DIAGRAM



The input stage provides high common-mode rejection, low noise, fast settling at all gains, and low drift over temperature. The gains of 1, 10, 100, and 500 are digitally selected with the two gain control lines which are 5V CMOS compatible.

The track and hold amplifier section is ideally suited for high speed 12-bit applications where fast settling, low noise, and low sample-to-hold offset are critical. The T/H mode is controlled with a single input line which can be tied to the status output line of the accompanying A/D converter.

AD365—SPECIFICATIONS (typical @ V_S = ±15V, R_L = 2kΩ and T_A = +25°C unless otherwise specified).

AD365AM	Min	Typ	Max	Units
PGA GAIN				
Inaccuracy[1]				
@ G = 1, 10, 100		0.02	0.05	%
@ G = 500		0.04	0.1	%
Nonlinearity				
@ G = 1, 10, 100			0.005	%
@ G = 500			0.01	%
Drift				
@ G = 1		1	5	ppm/°C
@ G = 10, 100, 500		3	10	ppm/°C
PGA OFFSET (May be Nulled at Input and Output)				
Input Offset Voltage (RTI)		25	200	μV
vs. Temperature		0.1	2	μV/°C
vs. Common-Mode Voltage		0.5	3.2	μV/V
vs. Supply Voltage		1	10	μV/V
Output Offset Voltage (RTO)		1	5	mV
vs. Temperature		30	150	μV/°C
vs. Common-Mode Voltage		60	316	μV/V
vs. Supply Voltage		60	316	μV/V
PGA INPUT				
Common- Mode and Differential Impedance		$10^9 \| 5$		Ω|pF
Differential Input Voltage, Linear	10	12		V
Common-Mode Voltage, Linear		$12 - V_{DIFF} \times G/2$		V
Input Stage Noise 0.1 to 10Hz		0.2		μV p-p
Input Stage Noise Density @ 1kHz		4		$nV/\sqrt{Hz}$
Bias Current		5	50	nA
vs. Temperature		50		pA/°C
Offset Current		2	20	nA
vs. Temperature		20		pA/°C
Noise Current (0.1 to 10Hz)		60		pA p-p
PGA OUTPUT				
Voltage 2kΩLoad	10	12		V
Output Impedance		0.2		Ω
Short Circuit Current		25		mA
Capacitive Load		500		pF
Output Stage Noise 0.1 to 10Hz		10		μV p-p
Output Stage Noise Density @ 1kHz		75		$nV/\sqrt{Hz}$
Guard Voltage		$(V_{+IN} + V_{-IN})/2$		V
Guard Offset		−550		mV
PGA DYNAMIC RESPONSE				
Small Signal − 3dB				
G = 1		800		kHz
G = 10		400		kHz
G = 100		150		kHz
G = 500		40		kHz
Full Power Bandwidth G = 1 @ V_O = 20V p-p		60		kHz
Slew Rate		4		V/μs
Settling Time to 0.01% @ V_O = 20V p-p				
G = 1, 10		8	10	μs
G = 100		12	15	μs
G = 500		40	50	μs
Gain Switching Time		1.5		μs
Overdrive Recovery Time V_{IN} = 15V @ G = 1		7		μs
PGA DIGITAL INPUTS				
Logic Low	0		0.8	V
Logic High	3.0		$+V_S$	V
Current, I_{INH} or I_{INL}		0.01	1	μA

AD365AM	Min	Typ	Max	Units
TRACK AND HOLD AMPLIFIER SECTION				
TRANSFER CHARACTERISTICS				
Open Loop Gain V_O = 10V, R_L = 2k	100k	200k		V/V
Nonlinearity @ G = +1			0.005	% FSR
Output Voltage R_L = 2kΩ	10	12		V
Capacitive Load		100		pF
Short Circuit Current		25		mA
TRACK MODE DYNAMICS				
Acquisition Time to 0.01% 10V Step		2	3	μs
20V Step		4	5	μs
Small Signal Bandwidth −3dB		2		MHz
Full Power Bandwidth (20V p-p)		120		kHz
Slew Rate		10		V/μs
TRACK/HOLD SWITCHING				
Aperture Time		35		ns
Aperture Uncertainty		0.5		ns
Switching Transient		40		mV
Settling Time to 2mV		0.5		μs
HOLD MODE				
Droop Rate @ +25°C		0.3	1	V/sec
from $T_{AMBIENT}$ to T_{MAX}		Doubles/10°C		V/sec
Feedthrough		25		μV/V
Pedestal, Offset @ +25°C		2	3	mV
Over Temperature		3		mV
T/H ANALOG INPUT				
Bias Current		0.1	2	nA
Over Temperature		0.2	5	nA
Offset Voltage			2	mV
Over Temperature			3	mV
vs. Common Mode		25	100	μV/V
vs. Supplies		100	316	μV/V
Input Impedance		10^{12}‖10		Ω‖pF
Noise Density @ 1kHz		50		nV/√Hz
Noise 0.1Hz to 10Hz		10		μV p-p
T/H DIGITAL INPUT CHARACTERISTICS				
Logic Low (Hold Mode)	0		0.8	V
Logic High (Track Mode)	2.0		$+V_S$	V
Input Current		10	50	μA
AD365 POWER REQUIREMENTS				
Positive Supply Range	+11		+17	V
Negative Supply Range	−11		−17	V
Quiescent Current		12	16	mA
Power Dissipation		360	550	mW
Warm-Up Time to Specification		5		Minutes
Ambient Operating Temperature	−25		+85	°C
Package Thermal Resistance (θ_{ja})		60		°C/W
AD365 ABSOLUTE MAXIMUM RATINGS				
Positive Supply $+V_S$	−0.3		+17	V dc
Negative Supply $-V_S$	+0.3		−17	V dc
Analog Input Voltage	$-V_S$		$+V_S$	V
Analog Input Current	−10		+10	mA
Digital Input Voltage	−0.3		$+V_S$	V
T/H Differential V_{IN}			±30	V
Storage Temperature	−65		+150	°C
Lead Soldering, 10 Sec			300	°C
Short Circuit Duration		Indefinite		
PACKAGE OPTION[2]				
DH-16B				

NOTES
[1]Gain = 10, 100 and 500 are trimmed and tested ratiometric to G = 1.
[2]For outline information see Package Information section.
Specifications subject to change without notice.

4

AD365—Typical Characteristics (@ +25°C unless otherwise noted)

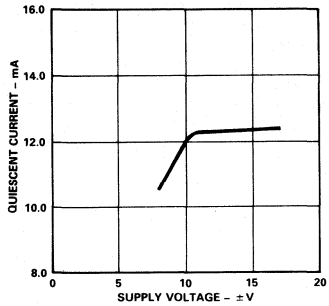


Figure 1. AD365 Quiescent Current vs. Supply Voltage

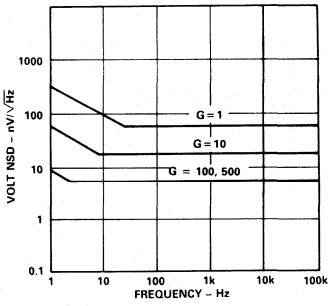


Figure 2. PGA RTI Noise Spectral Density vs. Gain

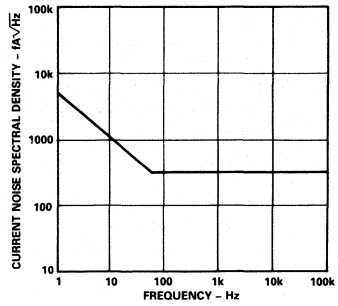


Figure 3. PGA Input Current Noise

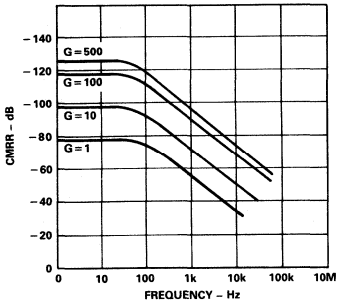


Figure 4. PGA CMRR vs. Frequency RTI, Zero to 1kΩ Source Imbalance

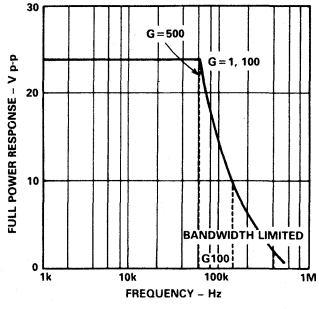


Figure 5. PGA Large Signal Frequency Response

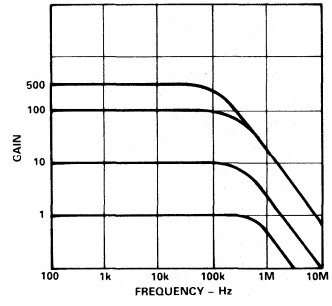


Figure 6. PGA Gain vs. Frequency

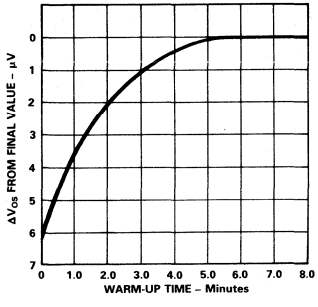


Figure 7. PGA Offset Voltage, RTI, Turn On Drift

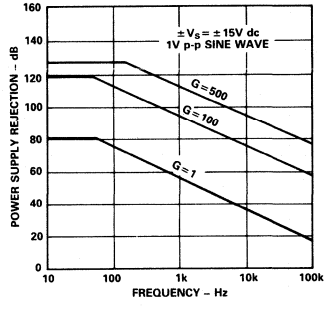


Figure 8. PGA PSRR vs. Frequency

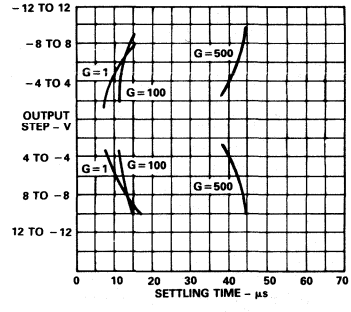


Figure 9. PGA Settling Time to 0.01%

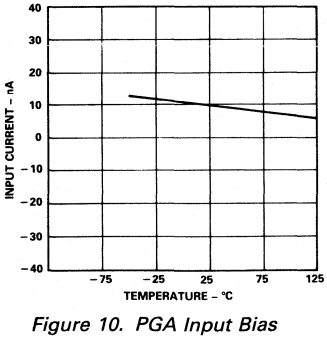


Figure 10. PGA Input Bias Current vs. Temperature

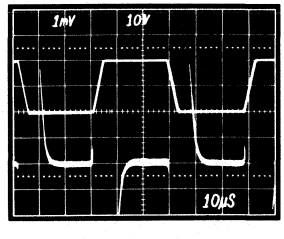


Figure 11. PGA Large Signal Pulse Response and Settling Time, G = 100

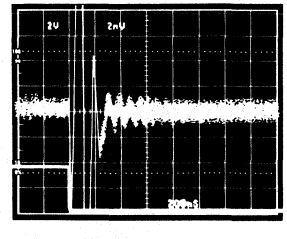


Figure 12. Sample-to-Hold Settling Time

The AD365 PGA section uses the AD625 monolithic instrumentation amplifier based on a modification of the classic three-op-amp approach. Monolithic construction and laser-wafer-trimming allow the tight matching and tracking of circuit components. This insures the high level of performance inherent in this circuit architecture.

A preamp stage (Q1-Q4) provides additional gain to A1 and A2. Feedback from the outputs of A1 and A2 forces the collector currents of Q1-Q4 to be constant, thereby, impressing the input voltage across R_G. This creates a differential voltage at the outputs of A1 and A2 which is given by the gain ($2R_F/R_G$ + 1) times the differential portion of the input voltage. The unity gain subtractor, A3, removes any common-mode signal from the output voltage yielding a single ended output, V_{OUT}, referred to the potential at the reference pin.

Digital gain control is provided using the D0 and D1 inputs (pins 14 and 15) which are decoded internally in the gain switching AD7502 as shown in Figure 15 below. The switch selects the resistance R_G from the laser trimmed resistor network according to the following gain select table.

D1	D0	PGA GAIN
0	0	1
0	1	10
1	0	100
1	1	500

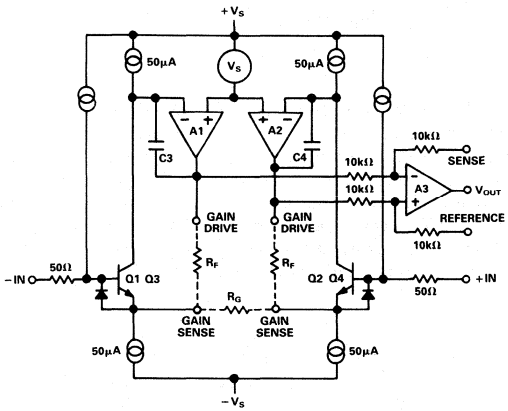


Figure 13. Simplified Circuit of the PGA

INPUT PROTECTION

Differential input amplifiers frequently encounter input voltages outside of their linear range of operation. There are two considerations when applying input protection for the PGA; 1) that continuous input current must be limited to less than 10mA and 2) that input voltages must not exceed either supply by more than one diode drop (approximately 0.6V @ 25°C).

Under differential overload conditions there is (R_G + 300)Ω in series with two diode drops (approximately 1.2V) between the plus and minus inputs, in either direction. With no external protection and R_G very small (i.e., 80Ω @ G = 500), the maximum overload voltage the PGA can withstand, continuously, is approximately ±5V. Figure 14 shows the external components

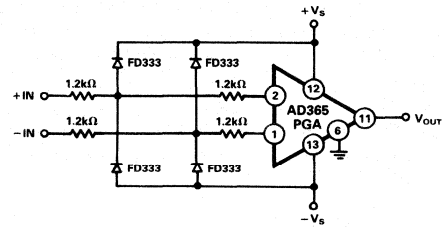


Figure 14. Input Protection Circuit for PGA

necessary to protect the PGA under all overload conditions at any gain. The diodes to the supplies are only necessary if input voltages outside of the range of the supplies are encountered.

REFERENCE TERMINAL

The reference terminal may be used to offset the output by up to ±2V. This is useful when the load is "floating" or does not share a ground with the rest of the system. It also provides a direct means of injecting a precise offset. It must be remembered, however, that the total output swing, to be shared between signal and reference offset, should be ± 10 volts (from ground).

The PGA section reference terminal must be presented with nearly zero impedance. Any significant resistance, including those caused by PC layouts or other connection techniques, will increase the gain of the noninverting signal path, thereby, upsetting the common-mode rejection of the In-Amp. Inadvertent thermocouple connections created in the sense and reference lines should also be avoided as they will directly affect the output offset voltage and output offset voltage drift.

In the AD625, a reference source resistance will unbalance the CMR trim by the ratio of 10kΩ/R_{REF}. For example, if the reference source impedance is 1Ω, CMR will be reduced to 80dB (10kΩ/1Ω = 80dB). An operational amplifier may be used to provide the low impedance reference point as shown in Figure 15. The input offset voltage characteristics of that amplifier will add directly to the output offset voltage performance of the instrumentation amplifier.

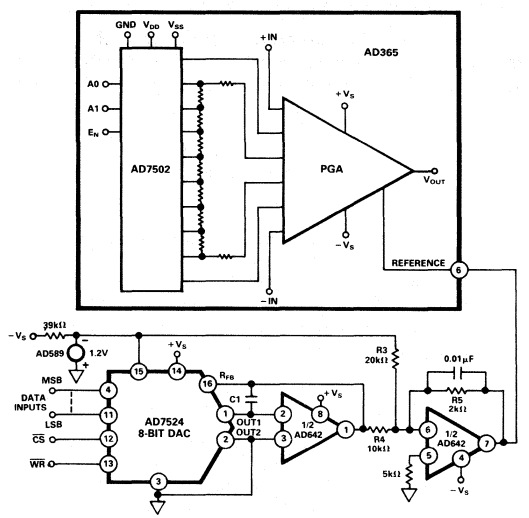


Figure 15. Software Controllable Offset

The circuit of Figure 15 also shows a CMOS DAC operating in the bipolar mode and connnected to the reference terminal to provide software controllable offset adjustments. The total offset range is equal to $\pm(V_{REF}/2 \times R_5/R_4)$. To be symmetrical about 0V, R_3 must be equal to $2 \times R_4$.

The offset per bit is equal to the total offset range divided by 2^N, where N = number of bits of the DAC. The range of offset for Figure 15 is ±120mV, and the offset is incremented in steps of 0.9375mV/LSB.

INPUT AND OUTPUT OFFSET VOLTAGE

Offset voltage specifications are often considered a figure of merit for instrumentation amplifiers. While initial offset may be adjusted to zero, shifts in offset voltage due to temperature variations will cause errors. Intelligent systems can often correct for this factor with an auto-zero cycle, but this requires extra circuitry.

Offset voltage and offset voltage drift each have two components: input and output. Input offset is that component of offset that is generated at the input stage. Measured at the output it is directly proportional to gain, i.e., input offset as measured at the output at G = 100 is 100 times greater than that measured at G = 1. Output offset is generated at the output and is constant for all gains. Input errors dominate at high gains and output errors dominate at low gains.

By separating these errors, one can evaluate the total error independent of the gain. For a given gain, both errors can be combined to give a total error referred to the input (RTI) or output (RTO) by the following formula:

Total Error RTI = input error + (output error/gain)

Total Error RTO = (Gain × input error) + output error

The AD365 provides for input offset voltage adjustment (see Figure 16). This simplifies nulling in very high precision applications and minimizes offset voltage effects in switched gain applications. In such applications the input offset is adjusted first at the highest programmed gain, then the output offset is adjusted at G = 1. If only a single null is desired, the input offset null should be used. The most additional drift when using only the input offset null is 0.9μV/°C, RTO.

Output offset adjustment is normally provided by the A/D converter offset adjustment which will compensate for the output offset of the PGA, offset of the T/H amplifier, and offset of the A/D.

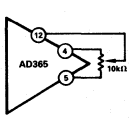


Figure 16. Input Voltage Offset Adjustment

COMMON-MODE REJECTION

In an instrumentation amplifier, degradation of common-mode rejection is caused by a differential phase shift due to differences in distributed stray capacitances. In many applications shielded cables are used to minimize noise. This technique can create common-mode rejection errors unless the shield is properly driven. Figure 17 shows active data guards which are configured to improve ac common-mode rejection by "bootstrapping" the capacitances of the input cabling, thus minimizing differential phase shift.

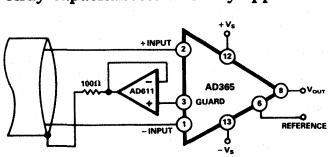


Figure 17. Common-Mode Shield Driver

GROUNDING

In order to isolate low level analog signals from a noisy digital environment, many data-acquisition components have two or more ground pins. These grounds must eventually be tied together at one point. It would be convenient to use a single ground line, however, current through ground wires and pc runs of the circuit card can cause hundreds of millivolts of error. Therefore, separate ground returns should be provided to minimize the current flow from the sensitive points to the system ground (see Figure 18). Since the AD365 output voltage is developed with respect to the potential on the reference terminal, it can solve many grounding problems.

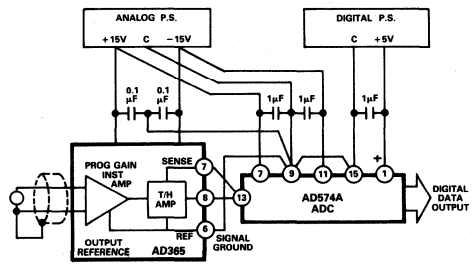


Figure 18. Basic Grounding Practice

GROUND RETURNS FOR BIAS CURRENTS

Input bias currents are those currents necessary to bias the input transistors of a dc amplifier. There must be a direct return path for these currents, otherwise they will charge external capacitances, causing the output to drift uncontrollably or saturate. Therefore, when amplifying "floating" input sources such as transformers, or ac-coupled sources, there must be a dc path from each input to ground as shown in Figure 19.

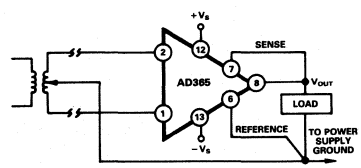


Figure 19a. Ground Returns for Bias Currents with Transformer Coupled Inputs

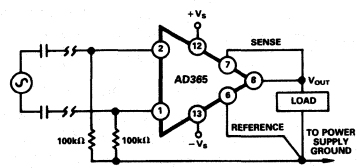


Figure 19b. Ground Returns for Bias Currents with ac Coupled Inputs

AUTO-ZERO CIRCUITS

In many applications it is necessary to maintain high accuracy. At room temperature, offset effects can be nulled by the use of offset trimpots. Over the operating temperature range, however, offset nulling becomes a problem. For these applications the auto-zero circuit of Figure 20 provides a hardware solution.

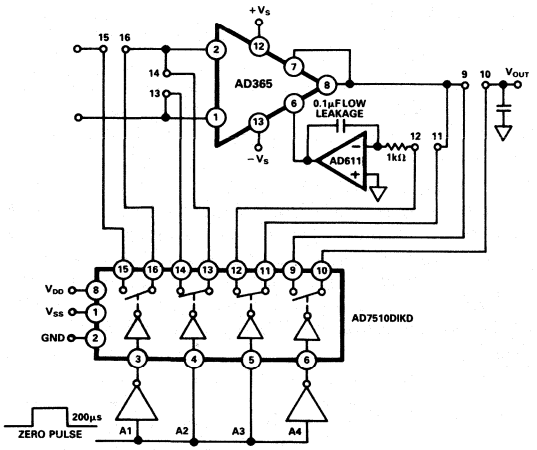


Figure 20. Auto-Zero Circuit

OTHER CONSIDERATIONS

One of the more overlooked problems in designing ultra-low-drift dc amplifiers is thermocouple induced offset. In a circuit comprised of two dissimilar conductors (i.e., copper, kovar), a current flows when the two junctions are at different temperatures. When this circuit is broken, a voltage known as the "Seebeck" or thermocouple emf can be measured. Standard IC lead material (kovar) and copper form a thermocouple with a high thermoelectric potential (about 35μV°C). This means that care must be taken to insure that all connections (especially those in the input circuit of the AD365) remain isothermal. This includes the input leads (1, 2). In addition, the user should also avoid air currents over the circuitry since slowly fluctuating thermocouple voltages will appear as "flicker" noise.

The base emitter junction of an input transistor can rectify out-of-band signals (i.e., RF interference). When amplifying small signals, these rectified voltages act as small dc offset errors. In the case of a resistive transducer, a capacitor across the input working against the internal resistance of the transducer may suffice to provide an RC filter. These capacitances may also be incorporated as part of the external input protection circuit (see section on input protection). As a general practice every effort should be made to match the extraneous capacitance at pins 1 and 2, to preserve high ac CMR.

THEORY OF OPERATION – T/H SECTION

In sampled data systems there are a number of limiting factors in digitizing high frequency signals accurately. Figure 21 shows pictorially the track-and-hold errors that are the limiting factors. In the following discussions of error sources the errors will be divided into the following groups: 1. Track-to-Hold Transition, 2. Hold Mode and 3. Hold-to-Track Transition.

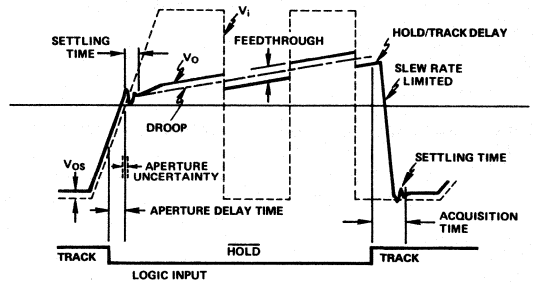


Figure 21. Pictorial Showing Various T/H Characteristics

TRACK-TO-HOLD TRANSITION

The aperture delay time is the time required for the track-and-hold amplifier to switch from track to hold. Since this is effectively a constant, it may be tuned out. If however, the aperture delay time is not accounted for then errors of the magnitude as shown in Figure 22 will result.

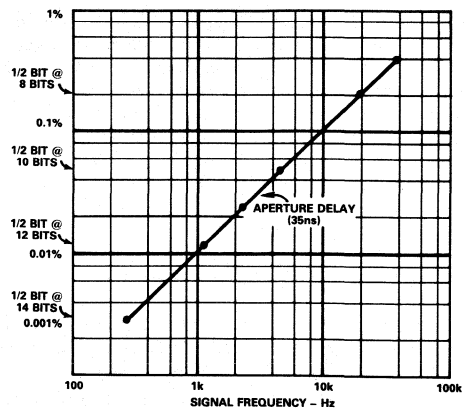


Figure 22. Aperture Delay Error vs. Frequency

To eliminate the aperture delay as an error source the track-to-hold command may be advanced with respect to the input signal.

Once the aperture delay time has been eliminated as an error source then T/H trigger uncertainty/jitter and internal aperture jitter which are the variations in aperture delay time from sample-to-sample remain. The aperture jitter is a true error source and must be considered. The aperture jitter is a result of noise within the switching network which modulates the phase of the hold command and is manifested in the variations in the value of the analog input that has been held. The aperture error which results from this jitter is directly related to the dV/dt of the analog input.

The error due to aperture jitter is easily calculated as shown below. The error calculation takes into account the desired accuracy corresponding to the resolution of the N-bit A/D converter.

$$F_{max} = \frac{2^{-(N+1)}}{\pi \text{ (Aperture Jitter)}}$$

For an application with a 12-bit A/D converter with a 10V full scale to a 1/2LSB error maximum:

$$F_{max} = \frac{2^{-(12+1)}}{\pi\,(0.5 \times 10^{-9})} = 77.7\text{kHz}$$

Track-to-hold offset is caused by the transfer of charge to the holding capacitor via the gate capacitance of the switch when switching into hold. Since the gate capacitance couples the switch-control voltage applied to the gate on to the hold capacitor, the resulting track-to-hold offset is a function of the logic level applied to the gate and the change in the gate capacitance over temperature.

HOLD MODE

In the hold mode there are two important specifications that must be considered; feedthrough and the droop rate. Feedthrough errors appear as an attenuated version of the input at the output while in the hold mode. Hold-Mode feedthrough varies with frequency, increasing at higher frequencies. Feedthrough is an important specification when a track and hold follows an analog multiplexer that switches among many different channels.

Hold-mode droop rate is the change in output voltage per unit of time while in the hold mode. Hold mode droop originates as leakage from the hold capacitor, of which the major leakage current contributors are switch leakage current and bias current. The rate of voltage change on the capacitor dV/dt is the ratio of the total leakage current I_L to the hold capacitance C_H.

$$\text{Droop Rate} = \frac{dV_{OUT}}{dt}\,(\text{Volts/Sec}) = \frac{I_L(\text{pA})}{C_H(\text{pF})}$$

For the AD365 in particular;

$$\text{Droop Rate} = \frac{100\text{pA}}{100\text{pF}} = 1\text{V/sec maximum}$$

Additionally the leakage current doubles for every 10°C increase in temperature above 25°C; therefore, the hold-mode droop rate characteristic will also double in the same fashion.

Since a track and hold is used typically in combination with an A/D converter, then the total droop in the output voltage has to be less than 1/2LSB during the period of a conversion. The maximum allowable signal change on the input of an A/D converter is:

$$\Delta V \text{ max} = \frac{\text{Full Scale Voltage}}{2^{(N+1)}}$$

Once the maximum ΔV is determined then the conversion time of the A/D converter (t_{CONV}) is required to calculate the maximum allowable dV/dt.

$$\frac{dV \text{ max}}{dt} = \frac{\Delta V \text{ max}}{t_{CONV}}$$

The maximum $\frac{dV \text{ max}}{dt}$ as shown by the previous equation is the limit not only at 25°C but at the maximum expected operating temperature range. Therefore, over the operating temperature range the following criteria must be met ($T_{OPERATION} - 25°C$) = ΔT.

$$\frac{dV\ 25°C}{dt} \times 2^{\frac{(\Delta T°C)}{10°C}} \leq \frac{dV \text{ max}}{dt}$$

HOLD-TO-TRACK TRANSITION

The Nyquist theorem states that a band-limited signal which is sampled at a rate at least twice the maximum signal frequency can be reconstructed without loss of information. This means that a sampled data system must sample, convert and acquire the next point at a rate at least twice the signal frequency. Thus the maximum input frequency is equal to

$$f_{MAX} = \frac{1}{2(T_{ACQ} + T_{CONV} + T_{AP})}$$

Where T_{ACQ} is the acquisition time of the sample-to-hold amplifier, T_{AP} is the maximum aperture time (small enough to be ignored) and T_{CONV} is the conversion time of the A/D converter.

DATA ACQUISITION SYSTEMS

The fast acquisition time of the AD365 when used with a high speed A/D converter allows accurate digitization of high frequency signals and high throughput rates in multichannel data acquisition systems. The AD365 can be used with a number of different A/D converters to achieve high throughput rates. Figures 23 and 24 show the use of an AD365 with the AD578 and AD574A.

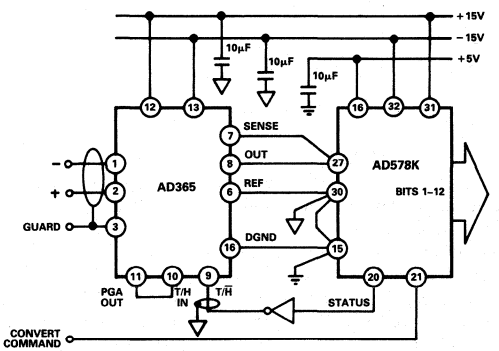


Figure 23. A/D Conversion System, 117.6kHz Throughput 58.8kHz Max Signal Input

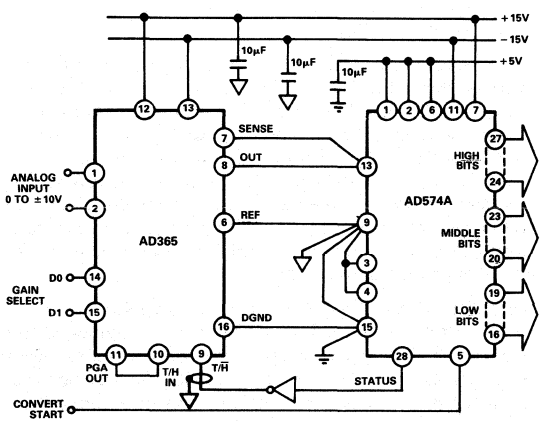


Figure 24. 12-Bit A/D Conversion System, 26.3kHz Throughput Rate, 13.1kHz Max Signal Input

ANALOG DEVICES

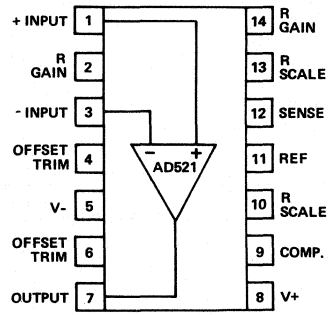
Integrated Circuit Precision Instrumentation Amplifier

AD521

FEATURES

Programmable Gains from 0.1 to 1000
Differential Inputs
High CMRR: 110dB min
Low Drift: 2μV/°C max (L)
Complete Input Protection, Power ON and Power OFF
Functionally Complete with the Addition of Two Resistors
Internally Compensated
Gain Bandwidth Product: 40MHz
Output Current Limited: 25mA
Very Low Noise: 0.5μV p-p, 0.1Hz to 10Hz, RTI @ G = 1000
Chips are Available

PIN CONFIGURATION



4

PRODUCT DESCRIPTION

The AD521 is a second generation, low cost, monolithic IC instrumentation amplifier developed by Analog Devices. As a true instrumentation amplifier, the AD521 is a gain block with differential inputs and an accurately programmable input/output gain relationship.

The AD521 IC instrumentation amplifier should not be confused with an operational amplifier, although several manufacturers (including Analog Devices) offer op amps which can be used as building blocks in variable gain instrumentation amplifier circuits. Op amps are general-purpose components which, when used with precision-matched external resistors, can perform the instrumentation amplifier function.

An instrumentation amplifier is a precision differential voltage gain device optimized for operation in a real world environment, and is intended to be used wherever acquisition of a useful signal is difficult. It is characterized by high input impedance, balanced differential inputs, low bias currents and high CMR.

As a complete instrumentation amplifier, the AD521 requires only two resistors to set its gain to any value between 0.1 and 1000. The ratio matching of these resistors does not affect the high CMRR (up to 120dB) or the high input impedance ($3 \times 10^9 \Omega$) of the AD521. Furthermore, unlike most operational amplifier-based instrumentation amplifiers, the inputs are protected against overvoltages up to ±15 volts beyond the supplies.

The AD521 IC instrumentation amplifier is available in four different versions of accuracy and operating temperature range. The economical "J" grade, the low drift "K" grade, and the lower drift, higher linearity "L" grade are specified from 0 to +70°C. The "S" grade guarantees performance to specification over the extended temperature range: -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD521 is a true instrumentation amplifier in integrated circuit form, offering the user performance comparable to many modular instrumentation amplifiers at a fraction of the cost.
2. The AD521 has low guaranteed input offset voltage drift (2μV/°C for L grade) and low noise for precision, high gain applications.
3. The AD521 is functionally complete with the addition of two resistors. Gain can be preset from 0.1 to more than 1000.
4. The AD521 is fully protected for input levels up to 15V beyond the supply voltages and 30V differential at the inputs.
5. Internally compensated for all gains, the AD521 also offers the user the provision for limiting bandwidth.
6. Offset nulling can be achieved with an optional trim pot.
7. The AD521 offers superior dynamic performance with a gain-bandwidth product of 40MHz, full peak response of 100kHz (independent of gain) and a settling time of 5μs to 0.1% of a 10V step.

AD521—SPECIFICATIONS (typical @ V_S = ±15V, R_L = 2kΩ and T_A = +25°C unless otherwise specified)

MODEL	AD521JD	AD521KD	AD521LD	AD521SD (AD521SD/883B)
GAIN				
Range (For Specified Operation, Note 1)	1 to 1000	•	•	•
Equation	$G = R_S/R_G V/V$	•	•	•
Error from Equation	(±0.25–0.004G)%	•	•	•
Nonlinearity (Note 2)				
$1 \leq G \leq 1000$	0.2% max	•	0.1% max	•
Gain Temperature Coefficient	±(3 ±0.05G)ppm/°C	•	•	±(15 ±0.4G)ppm/°C
OUTPUT CHARACTERISTICS				
Rated Output	±10V, ±10mA min	•	•	•
Output at Maximum Operating Temperature	±10V @ 5mA min	•	•	•
Impedance	0.1Ω	•	•	•
DYNAMIC RESPONSE				
Small Signal Bandwidth (±3dB)				
G = 1	>2MHz	•	•	•
G = 10	300kHz	•	•	•
G = 100	200kHz	•	•	•
G = 1000	40kHz	•	•	•
Small Signal, ±1.0% Flatness				
G = 1	75kHz	•	•	•
G = 10	26kHz	•	•	•
G = 100	24kHz	•	•	•
G = 1000	6kHz	•	•	•
Full Peak Response (Note 3)	100kHz	•	•	•
Slew Rate, $1 \leq G \leq 1000$	10V/μs	•	•	•
Settling Time (any 10V step to within 10mV of Final Value)				
G = 1	7μs	•	•	•
G = 10	5μs	•	•	•
G = 100	10μs	•	•	•
G = 1000	35μs	•	•	•
Differential Overload Recovery (±30V Input to within 10mV of Final Value) (Note 4)				
G = 1000	50μs	•	•	•
Common Mode Step Recovery (30V Input to within 10mV of Final Value) (Note 5)				
G = 1000	10μs	•	•	•
VOLTAGE OFFSET (may be nulled)				
Input Offset Voltage (V_{OS_I})	3mV max (2mV typ)	1.5mV max (0.5mV typ)	1.0mV max (0.5mV typ)	••
vs. Temperature	15μV/°C max (7μV/°C typ)	5μV/°C max (1.5μV/°C typ)	2μV/°C max	••
vs. Supply	3μV/%	•	•	•
Output Offset Voltage (V_{OS_O})	400mV max (200mV typ)	200mV max (30mV typ)	100mV max	••
vs. Temperature	400μV/°C max (150μV/°C typ)	150μV/°C max (50μV/°C typ)	75μV/°C max	••
vs. Supply (Note 6)	$0.005V_{OS_O}$/%	•	•	•
INPUT CURRENTS				
Input Bias Current (either input)	80nA max	40nA max	••	••
vs. Temperature	1nA/°C max	500pA/°C max	••	••
vs. Supply	2%/V	•	•	•
Input Offset Current	20nA max	10nA max	••	••
vs. Temperature	250pA/°C max	125pA/°C max	••	••
INPUT				
Differential Input Impedance (Note 7)	$3 \times 10^9 \Omega \| 1.8pF$	•	•	•
Common Mode Input Impedance (Note 8)	$6 \times 10^{10} \Omega \| 3.0pF$	•	•	•
Input Voltage Range for Specified Performance (with respect to ground)	±10V	•	•	•
Maximum Voltage without Damage to Unit, Power ON or OFF Differential Mode (Note 9)	30V	•	•	•
Voltage at either input (Note 9)	V_S ±15V	•	•	•
Common Mode Rejection Ratio, DC to 60Hz with 1kΩ source unbalance				
G = 1	70dB min (74dB typ)	74dB min (80dB typ)	••	••
G = 10	90dB min (94dB typ)	94dB min (100dB typ)	••	••
G = 100	100dB min (104dB typ)	104dB min (114dB typ)	••	••
G = 1000	100dB min (110dB typ)	110dB min (120dB typ)	••	••
NOISE				
Voltage RTO (p-p) @ 0.1Hz to 10Hz (Note 10)	$\sqrt{(0.5G)^2 + (225)^2}\ \mu V$	•	•	•
RMS RTO, 10Hz to 10kHz	$\sqrt{(1.2G)^2 + (50)^2}\ \mu V$	•	•	•
Input Current, rms, 10Hz to 10kHz	15pA (rms)	•	•	•
REFERENCE TERMINAL				
Bias Current	3μA	•	•	•
Input Resistance	10MΩ	•	•	•
Voltage Range	±10V	•	•	•
Gain to Output	1	•	•	•
POWER SUPPLY				
Operating Voltage Range	±5V to ±18V	•	•	•
Quiescent Supply Current	5mA max	•	•	•
TEMPERATURE RANGE				
Specified Performance	0 to +70°C	•	•	−55°C to +125°C
Operating	−25°C to +85°C	•	•	−55°C to +125°C
Storage	−65°C to +150°C	•	•	•

*Specifications same as AD521JD.
**Specifications same as AD521KD.
Specifications subject to change without notice.

NOTES:

1. Gains below 1 and above 1000 are obtained by simply adjusting the gain setting resistors. (Input voltage should be restricted to ±10V for gains equal to or less than 1.)

2. Nonlinearity is defined as the ratio of the deviation from the "best straight line" through a full scale output range of ±9 volts. With a combination of high gain and ±10 volt output swing, distortion may increase to as much as 0.3%.

3. Full Peak Response is the frequency below which a typical amplifier will produce full output swing.

4. Differential Overload Recovery is the time it takes the amplifier to recover from a pulsed 30V differential input with 15V of common mode voltage, to within 10mV of final value. The test input is a 30V, 10μs pulse at a 1kHz rate. (When a differential signal of greater than 11V is applied between the inputs, transistor clamps are activated which drop the excess input voltage across internal input resistors. If a continuous overload is maintained, power dissipated in these resistors causes temperature gradients and a corresponding change in offset voltage, as well as added thermal time constant, but will not damage the device.)

5. Common Mode Step Recovery is the time it takes the amplifier to recover from a 30V common mode input with zero volts of differential signal to within 10mV of final value. The test input is 30V, 10μs pulse at a 1kHz rate. (When a common mode signal greater than V_S −0.5V is applied to the inputs, transistor clamps are activated which drop the excessive input voltage across internal input resistors. Power dissipated in these resistors causes temperature gradients and a corresponding change in offset voltage, as well as an added thermal time constant, but will not damage the device.)

6. Output Offset Voltage versus Power Supply includes a constant 0.005 times the unnulled output offset per percent change in either power supply. If the output offset is nulled, the output offset change versus supply change is substantially reduced.

7. Differential Input Impedance is the impedance between the two inputs.

8. Common Mode Input Impedance is the impedance from *either* input to the power supplies.

9. Maximum Input Voltage (differential or at either input) is 30V when using ±15V supplies. A more general specification is that neither input may exceed either supply (even when $V_S = 0$) by more than 15V and that the difference between the two inputs must not exceed 30V. (See also Notes 4 and 5.)

10. 0.1Hz to 10Hz Peak-to-Peak Voltage Noise is defined as the maximum peak-to-peak voltage noise ovserved during 2 of 3 separate 10 second periods with the test circuit of Figure 8.

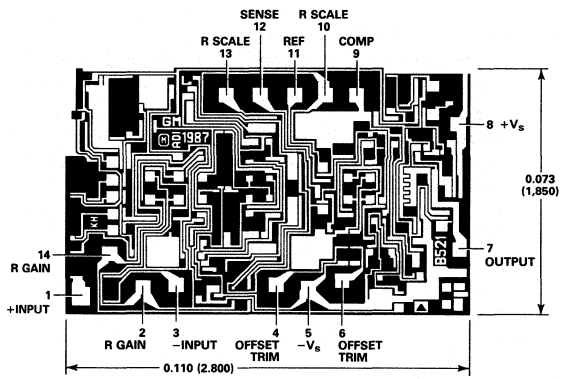
ORDERING GUIDE

Model	Temperature Range	Description	Package Option[1]
AD521JD	0°C to +70°C	14-Pin Ceramic DIP	D-14
AD521KD	0°C to +70°C	14-Pin Ceramic DIP	D-14
AD521LD	0°C to +70°C	14-Pin Ceramic DIP	D-14
AD521SD	−55°C to +125°C	14-Pin Ceramic DIP	D-14
AD521SD/883B[2]	−55°C to +125°C	14-Pin Ceramic DIP	D-14
AD521J Chips	0°C to +70°C	Die	
AD521K Chips	0°C to +70°C	Die	
AD521S Chips	−55°C to +125°C	Die	

NOTES
[1]For outline information see Package Information section.
[2]Standard military drawing available.

METALIZATION PHOTOGRAPHY

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



DESIGN PRINCIPLE

Figure 1 is a simplified schematic of the AD521. A differential input voltage, V_{IN}, appears across R_G causing an imbalance in the currents through Q_1 and Q_2, $\Delta I = V_{IN}/R_G$. That imbalance is forced to flow in R_S because the collector currents of Q_3 and Q_4 are constrained to be equal by their biasing (current mirror). These conditions can only be satisfied if the differential voltage across R_S (and hence the output voltage of the AD521) is equal to $\Delta I \times R_S$. The feedback amplifier, A_{FB} performs that function. Therefore, $V_{OUT} = \frac{V_{IN}}{R_G} \times R_S$ or $\frac{V_{OUT}}{V_{IN}} = \frac{R_S}{R_G}$

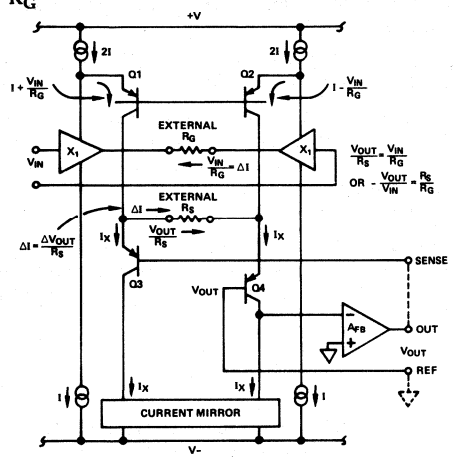


Figure 1. Simplified AD521 Schematic

APPLICATION NOTES FOR THE AD521

These notes ensure the AD521 will achieve the high level of performance necessary for many diversified IA applications.

1. Gains below 1 are realized by adjusting the gain setting resistors as shown in Figure 2 (the resistor, R_S between pins 10 and 13 should remain 100kΩ ±15%, see application note 3). For best results, the input voltage should be restricted to ±10V even though the gain may be less than 1. See Figure 6 for gains above 1000.

2. Provide a return path to ground for input bias currents. The AD521 is an instrumentation amplifier, not an isolation amplifier. When using a thermocouple or other "floating" source, this return path may be provided directly to ground or indirectly through a resistor to ground from pins 1 and/or 3, as shown in Figure 3. If the return path is not provided, bias currents will cause the output to saturate. The value of the resistor may be determined by dividing the maximum allowable common mode voltage for the application by the bias current of the instrumentation amplifier.

3. The resistors between pins 10 and 13, (R_{SCALE}) must equal 100kΩ ±15% (Figure 2). If R_{SCALE} is too low (below 85kΩ) the output swing of the AD521 is reduced. At values below 80kΩ and above 120kΩ the stability of the AD521 may be impaired.

4. Do not exceed the allowable input signal range. The linearity of the AD521 decreases if the inputs are driven within 5 volts of the supply rails, particularly when the device is used at a gain less than 1. To avoid this possibility, attenuate the input signal through a resistive divider network and use the AD521 as a buffer, as shown in Figure 4. The resistor R/2 matches the impedance seen by both AD521 inputs so that the voltage offset caused by bias currents will be minimized.

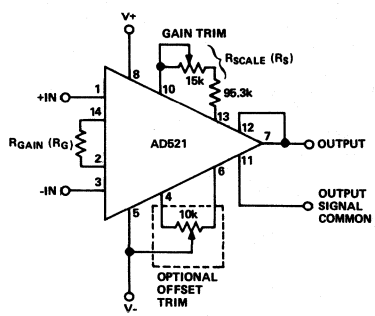
5. Use the compensation pin (pin 9) and the applicable compensation circuit when the amplifier is required to drive a capacitive load. It is worth mentioning that coaxial cables can "invisibly" provide such capacitance since many popular coaxial cables display capacitance in the vicinity of 30pF per foot.

This compensation (bandwidth control) feature permits the user to fit the response of the AD521 to the particular application as illustrated by Figure 5. In cases of extremely high load capacitance the compensation circuit may be changed as follows:

1. Reduce 680Ω to 24Ω
2. Reduce 330Ω to 7.5Ω
3. Increase 1000pF to 0.1μF
4. Set C_X to 1000pF if no compensation was originally used. Otherwise, do not alter the original value.

This allows stable operation for load capacitances up to 3000pF, but limits the slew rate to approximately 0.16V/μs.

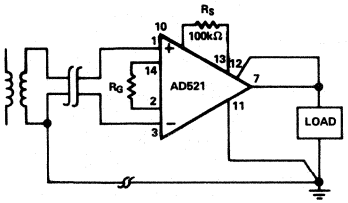
6. Signals having frequency components above the Instrumentation Amplifier's output amplifier closed-loop bandwidth will be transmitted from V– to the output with little or no attenuation. Therefore, it is advisable to decouple the V– supply line to the output common or to pin 11.[1]



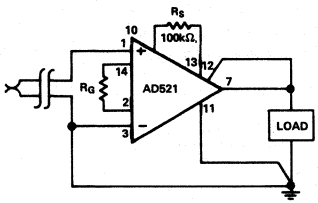
GAIN	VALUE OF RG
0.1	1MΩ
1	100kΩ
10	10kΩ
100	1kΩ
1000	100Ω

Figure 2. Operating Connections for AD521

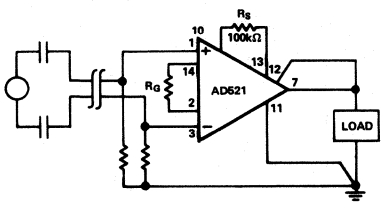
[1] For further details, refer to "An I.C. User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change," by A. Paul Brokaw. This application note is available from Analog Devices without charge upon request.



a). Transformer Coupled, Direct Return

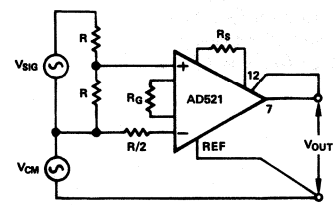


b). Thermocouple, Direct Return



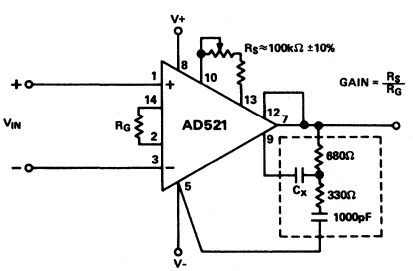
c). AC Coupled, Indirect Return

Figure 3. Ground Returns for "Floating" Transducers



1. INCREASE R_G TO PICK UP GAIN LOST BY R DIVIDER NETWORK
2. INPUT SIGNAL MUST BE REDUCED IN PROPORTION TO POWER SUPPLY VOLTAGE LEVEL

Figure 4. Operating Conditions for $V_{IN} \approx V_S = 10V$



$C_X = \frac{1}{100\pi f_t}$ *when f_t is the desired bandwidth.*

(f_t in kHz, C_X in μF)

Figure 5. Optional Compensation Circuit

INPUT OFFSET AND OUTPUT OFFSET

When specifying offsets and other errors in an operational amplifier, it is often convenient to refer these errors to the inputs. This enables the user to calculate the maximum error he would see at the output with any gain or circuit configuration. An op amp with 1mV of input offset voltage, for example, would produce 1V of offset at the output in a gain of 1000 configuration.

In the case of an instrumentation amplifier, where the gain is controlled in the amplifier, it is more convenient to separate errors into two categories. Those errors which simply add to the output signal and are unaffected by the gain can be classified as output errors. Those which act as if they are associated with the input signal, such that their effect at the output is proportional to the gain, can be classified as input errors.

As an illustration, a typical AD521 might have a +30mV output offset and a -0.7mV input offset. In a unity gain configuration, the *total* output offset would be +29.3mV or the sum of the two. At a gain of 100, the output offset would be -40mV or: 30mV + 100(-0.7mV) = -40mV.

By separating these errors, one can evaluate the total error independent of the gain settings used, similar to the situation with the input offset specifications on an op amp. In a given gain configuration, both errors can be combined to give a total error *referred to the input* (R.T.I.) or *output* (R.T.O.) by the following formula:

Total Error R.T.I. = input error + (output error/gain)

Total Error R.T.O. = (Gain x input error) + output error

The offset trim adjustment (pins 4 and 6, Figure 2) is associated primarily with the output offset. At any gain it can be used to introduce an output offset equal and opposite to the input offset voltage multiplied by the gain. As a result, the total output offset can be reduced to zero.

As shown in Figure 6, the gain range on the AD521 can be extended considerably by adding an attenuator in the sense terminal feedback path (as well as adjusting the ratio, R_S/R_G). Since the sense terminal is the inverting input to the output amplifier, the additional gain to the output is controlled by R_1 and R_2. This gain factor is $1 + R_2/R_1$.

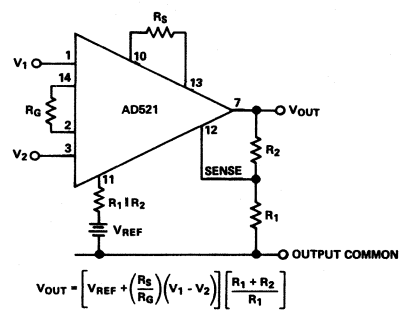


Figure 6. Circuit for utilizing some of the unique features of the AD521. Note that gain changes introduced by changing R1 and R2 will have a minimum effect on output offset if the offset is carefully nulled at the highest gain setting.

4

Where offset errors are critical, a resistor equal to the parallel combination of R_1 and R_2 should be placed between pin 11 and V_{REF}. This minimizes the offset errors resulting from the input current flowing in R_1 and R_2 at the sense terminal. Note that gain changes introduced by changing the R_1/R_2 attenuator will have a minimum effect on output offset if the offset is carefully nulled at the highest gain setting.

When a predetermined output offset is desired, V_{REF} can be placed in series with pin 11. This offset is then multiplied by the gain factor $1 + R_2/R_1$ as shown in the equation of Figure 6.

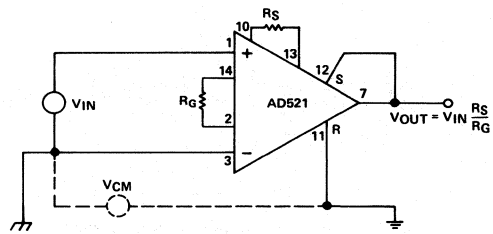


Figure 7. Ground loop elimination. The reference input, Pin 11, allows remote referencing of ground potential. Differences in ground potentials are attenuated by the high CMRR of the AD521.

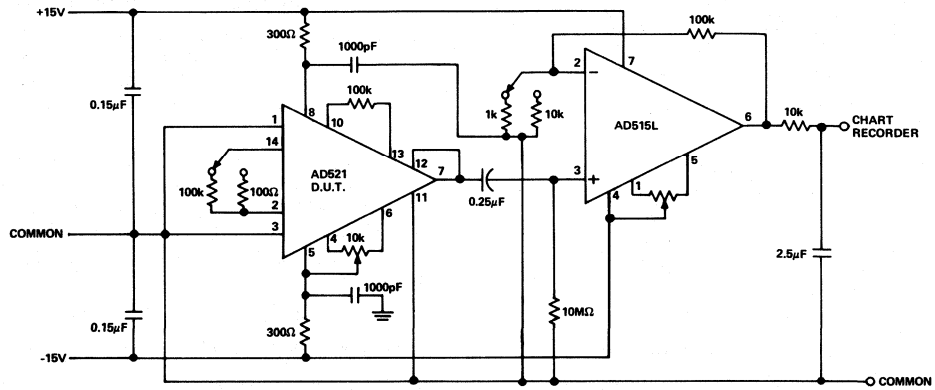


Figure 8. Test circuit for measuring peak to peak noise in the bandwidth 0.1Hz to 10Hz. Typical measurements are found by reading the maximum peak to peak voltage noise of the device under test (D.U.T.) for 3 observation periods of 10 seconds each.

High Accuracy Data Acquisition Instrumentation Amplifier

AD522

FEATURES

Performance

- Low Drift: 2.0μV/°C (AD522B)
- Low Nonlinearity: 0.005% (G = 100)
- High CMRR: >110dB (G = 1000)
- Low Noise: 1.5μV p-p (0.1 to 100Hz)
- Low Initial V_{OS}: 100μV (AD522B)

Versatility

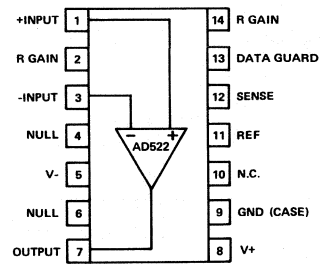
- Single-Resistor Gain Programmable: $1 \leqslant G \leqslant 1000$
- Output Reference and Sense Terminals
- Data Guard for Improving ac CMR

Value

- Internally Compensated
- No External Components except Gain Resistor
- Active Trimmed Offset, Gain, and CMR

FUNCTIONAL BLOCK DIAGRAM

14-Pin DIP



4

PRODUCT DESCRIPTION

The AD522 is a precision IC instrumentation amplifier designed for data acquisition applications requiring high accuracy under worst-case operating conditions. An outstanding combination of high linearity, high common mode rejection, low voltage drift, and low noise makes the AD522 suitable for use in many 12-bit data acquisition systems.

An instrumentation amplifier is usually employed as a bridge amplifier for resistance transducers (thermistors, strain gages, etc.) found in process control, instrumentation, data processing, and medical testing. The operating environment is frequently characterized by low signal-to-noise levels, fluctuating temperatures, unbalanced input impedances, and remote location which hinders recalibration.

The AD522 was designed to provide highly accurate signal conditioning under these severe conditions. It provides output offset voltage drift of less than 10μV/°C, input offset voltage drift of less than 2.0μV/°C, CMR above 80dB at unity gain (110dB at G = 1000), maximum gain nonlinearity of 0.001% at G = 1, and typical input impedance of $10^9\,\Omega$.

This excellent performance is achieved by combining a proven circuit configuration with state-of-the-art manufacturing technology which utilizes active laser trimming of tight-tolerance thin-film resistors to achieve low cost, small size and high reliability. This combination of high value with no-compromise performance gives the AD522 the best features of both monolithic and modular instrumentation amplifiers, thus providing extremely cost-effective precision low-level amplification.

The AD522 is available in three versions with differing accuracies and operating temperature ranges; the "A", and "B" are specified from -25°C to +85°C, and the "S" is guaranteed over the extended aerospace temperature range of -55°C to +125°C. All versions are packaged in a 14-pin DIP and are supplied in a pin configuration similar to that of the popular AD521 instrumentation amplifier.

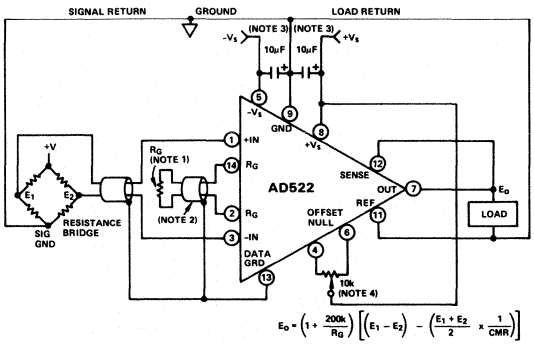
AD522—SPECIFICATIONS (typical @ V_S = ±15V, R_L = 2kΩ & T_A = +25°C unless otherwise specified)

MODEL	AD522AD	AD522BD	AD522SD
GAIN			
Gain Equation	$1 + \frac{2\ (10^5)}{R_g}$	•	•
Gain Range	1 to 1000	•	•
Equation Error			
G = 1	0.2% max	0.05% max	••
G = 1000	1.0% max	0.2% max	••
Nonlinearity, max (see Fig. 4)			
G = 1	0.005%	0.001%	••
G = 1000	0.01%	0.005%	••
vs. Temp, max			
G = 1	2ppm/°C (1ppm/°C typ)	•	•
G = 1000	50ppm/°C (25ppm/°C typ)	•	•
OUTPUT CHARACTERISTICS			
Output Rating	±10V @ 5mA	•	•
DYNAMIC RESPONSE (see Fig. 6)			
Small Signal (–3dB)			
G = 1	300kHz	•	•
G = 100	3kHz	•	•
Full Power GBW	1.5kHz	•	•
Slew Rate	0.1V/μs	•	•
Settling Time to 0.1%, G = 100	0.5ms	•	•
to 0.01%, G = 100	5ms	•	•
to 0.01%, G = 10	2ms	•	•
to 0.01%, G = 1	0.5ms	•	•
VOLTAGE OFFSET			
Offsets Referred to Input			
Initial Offset Voltage (adjustable to zero)			
G = 1	±400μV max (±200μV typ)	±200μV max (±100μV typ)	±200μV max (±100μV typ)
vs. Temperature, max (see Fig. 3)			
G = 1	±50μV/°C (±10μV/°C typ)	±25μV/°C (±5μV/°C typ)	±100μV/°C (±10μV/°C typ)
G = 1000	±6μV/°C	±2μV/°C	±6μV/°C
1 < G < 1000	$\pm(\frac{50}{G} + 6)\mu V/°C$	$\pm(\frac{25}{G} + 2)\mu V/°C$	$\pm(\frac{100}{G} + 6)\mu V/°C$
vs. Supply, max			
G = 1	±20μV/%	•	•
G = 1000	1.0μV/°C	0.5μV/°C	••
INPUT CURRENTS			
Input Bias Current			
Initial max, +25°C	±25nA	•	•
vs. Temperature	±100pA/°C	•	•
Input Offset Current			
Initial max, +25°C	±20nA	•	•
vs. Temperature	±100pA/°C	•	•
INPUT			
Input Impedance			
Differential	$10^9\Omega$	•	•
Common Mode	$10^9\Omega$	•	•
Input Voltage Range			
Maximum Differential Input, Linear	±10V	•	•
Maximum Differential Input, Safe	±20V	•	•
Maximum Common Mode, Linear	±10V	•	•
Maximum Common Mode Input, Safe	±15V	•	•
Common Mode Rejection Ratio, Min @ ±10V, 1kΩ Source Imbalance (see Fig. 5)			
G = 1 (dc to 30Hz)	75dB (90dB typ)	80dB (100dB typ)	75dB (90dB typ)
G = 10 (dc to 10Hz)	90dB (100dB typ)	95dB (110dB typ)	90dB (110dB typ)
G = 100 (dc to 3Hz)	100dB (110dB typ)	100dB (120dB typ)	100dB (120dB typ)
G = 1000 (dc to 1Hz)	100dB (120dB typ)	110dB (>120dB typ)	100dB (>120dB typ)
G = 1 to 1000 (dc to 60Hz)	75dB (88dB typ)	80dB (88dB typ)	•
NOISE			
Voltage Noise, RTI (see Fig. 4)			
0.1Hz to 100Hz (p-p)			
G = 1	15μV	•	•
G = 1000	1.5μV	•	•
10Hz to 10kHz (rms)			
G = 1	15μV	•	•
TEMPERATURE RANGE			
Specified Performance	-25°C to +85°C	•	-55°C to +125°C
Operating	-55°C to +125°C	•	•
Storage	-65°C to +150°C	•	•
POWER SUPPLY			
Power Supply Range	±(5 to 18)V	•	•
Quiescent Current, max @ ±15V	±10mA	±8mA	••
PACKAGE OPTIONS[2]			
Ceramic (DH-14B)	AD522AD	AD522BD	AD522SD

NOTES
[1]Specifications guaranteed after 10 minute warm-up.
[2]For output information see Package Information section.
*Specifications same as AD522A.
**Specifications same as AD522B.
Specifications subject to change without notice.

GENERAL APPLICATION CONSIDERATIONS

Figure 1 illustrates the AD522 wiring configuration when used in a typical bridge amplifier application. In any low-level, high impedance, noise-dominated environment, proper shielding and grounding are requisite for optimum performance; a recommended technique is shown.



NOTES:
1. GAIN RESISTOR R_G SHOULD BE <5ppm/°C (VISHAY TYPE RECOMMENDED).
2. SHIELDED CONNECTIONS TO R_G RECOMMENDED WHEN MAXIMUM SYSTEM BANDWIDTH AND AC CMR IS REQUIRED, AND WHEN R_G IS LOCATED MORE THAN SIX INCHES FROM AD522. NO INSTABILITIES ARE CAUSED BY REMOTE R_G LOCATIONS. WHEN NOT USED, THE DATA GUARD PIN CAN BE LEFT UNCONNECTED.
3. POWER SUPPLY FILTERS ARE RECOMMENDED FOR MINIMUM NOISE IN NOISY ENVIRONMENTS.
4. NO TRIM REQUIRED FOR MOST APPLICATIONS. IF REQUIRED, A 10kΩ, 25ppm/°C, 25 TURN TRIM POT (SUCH AS VISHAY 1202-Y-10k) IS RECOMMENDED.

Figure 1. Typical Bridge Application

Direct coupling of the AD522 inputs makes it necessary to provide a signal ground return for input amplifier bias currents. This can be achieved by direct connection as shown, or through an indirect path of less than 1MΩ resistance such as other system interconnections.

To minimize noise, shielding should be provided for the input leads and gain resistor connections. A passive data guard is provided to improve ac common mode rejection by "bootstrapping" the capacitance of the input cabling, thus minimizing differential phase shift. This will also reduce degradation of system bandwidth.

Balanced design eliminates the need for external bypass capacitors for most applications. If, however, the power supplies are remotely located (farther than 10 feet or so) or if they are likely to carry more than a few millivolts of noise, local filtering will enable the user to retain optimal performance.

Reference and sense pins are provided to permit remote load sensing. These points can also be used to trim the device CMR, add an output booster, or to offset the output to a reference level. These applications are illustrated in following sections.

It is good practice to place R_G within several inches of the AD522. Longer leads will increase stray capacitance and cause phase shifts that will degrade CMR at higher frequencies. For frequencies below 10Hz, a remote R_G is generally acceptable; no stability problems are caused. Bear in mind that a leakage impedance of 200MΩ between R_G pins will cause an 0.1% gain error at G = 1. Unity gain is not trimmable.

TYPICAL APPLICATION AND ERROR BUDGET ANALYSIS (See Figure 1 and Table I)

A floating transducer with a 0 to 1 volt output has a 1kΩ source imbalance. A noisy environment induces a one volt 0 to 60Hz common mode signal in the ground return. This signal must be amplified to interface with a data acquisition system calibrated for a 0 to 10 volt signal range. The operating temperature range is 0 to +50°C and an AD522B is to be used. Table I lists error sources and their effect on system accuracy.

The total effect on absolute accuracy is less than ±0.2%, allowing adjustment-free 8-bit operation. In computer or microprocessor controlled data-acquisition systems, automatic recalibration can nullify gain and offset drifts leaving noise, distortion and CMR as the only error sources. In this case, full 12-bit operation is achieved.

Gain Errors: Absolute gain errors can be nulled by trimming R_G. Gain drift is a linear effect, not detrimental to resolution and is caused by the change in value of internal resistors over the operating temperature range. An "intelligent" system can correct for these errors with an automatic calibration cycle. Gain nonlinearity never exceeds 0.002% at G = 10.

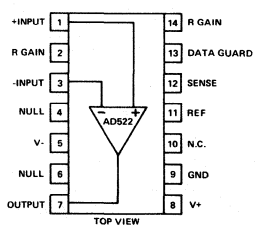
Offset Drift & Pins Current Errors: Special care has been taken in the design of the AD522 input stage to minimize offset drift. Unless transducer impedances are unbalanced by more than 2kΩ, errors caused by offset current drift are negligible compared to offset voltage drift. Although initial offset voltages are laser-nulled for most applications, provisions have been made to allow further adjustment to correct for initial system offset. In this example, all offset drifts amount to ±0.014% and do not effect resolution (can be corrected with an automatic calibration cycle).

CMR and Noise Errors: Common mode rejection and noise performance of instrumentation amplifiers are critical because

Error Source	Specification	Effect on Absolute Accuracy, % of F.S.	Effect on Resolution % of F.S.
Gain Nonlinearity	±0.002% max, G = 10 (from Spec. Sheet and Fig. 4)	±0.002	±0.002
Voltage Drift	$\frac{25\mu V/°C}{\text{Gain}}$ + 2.0µV/°C = 4.5µV/°C R.T.I. = 0.00055%/°C (from Spec. Sheet)	±0.011	---
CMR	86dB (from Spec. Sheet, CMR vs. F vs. G, typical curve)	±0.005	±0.005
Noise, R.T.O. (0.1 to 100Hz)	15µV (p-p) R.T.O. (from Spec. Sheet, Noise vs. G typical curve)	±0.0015	±0.0015
Offset Current Drift	±50pA/°C x 1k source imbalance (Spec. Sheet) = ±50µV/°C = ±1.25µV R.T.I.	±0.000125	---
Gain Drift (add 10ppm/°C for external R_G)	60ppm/°C (Spec. Sheet)	±0.15	---

Table I. Error Sources

PIN CONFIGURATION



these errors can not be corrected by calibration. Common mode rejection of the AD522 is active laser-trimmed to the limits of thin-film resistor stability. Further trimming could improve CMR on a short term basis, but regular readjustment would be necessary to maintain this improvement (see Figure 2). In this example, untrimmed CMR and noise cause a total error of ±0.0065% of full scale and are the major contributors to resolution error.

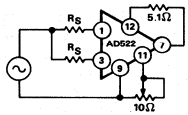


Figure 2. Optional CMR Trim

PERFORMANCE CHARACTERISTICS

Offset Voltage and Current Drift: The AD522 is available in three drift selections. Figure 3 is a graph of maximum RTO offset voltage drift vs. gain for all versions. Errors caused by offset voltage drift can thus be determined for any gain. Offset current drift will cause a voltage error equal to the product of the offset current drift and the source impedance unbalance.

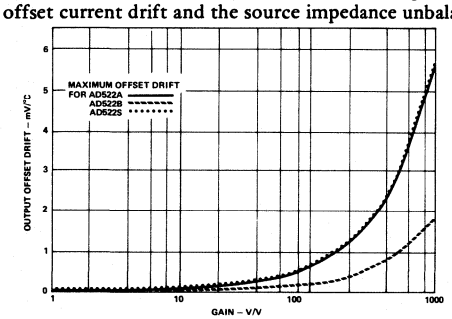


Figure 3. Output Offset Drift (RTO) vs. Gain

Gain Nonlinearity and Noise: Gain nonlinearity increases with gain as the device loop-gain decreases. Figure 4 is a plot of typical nonlinearity vs. gain. The shape of the curve can be safely used to predict worst-case nonlinearity at gains below 100. Noise vs. gain is shown on the same graph.

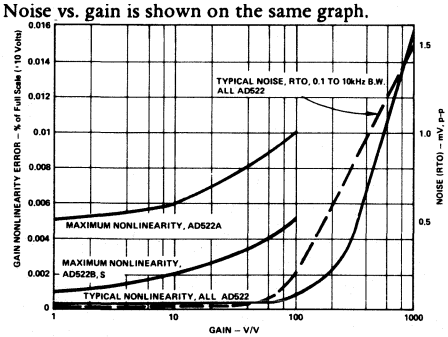


Figure 4. Gain Nonlinearity and Noise (RTO) vs. Gain

Common Mode Rejection: CMR is rated at ±10V and 1kΩ source imbalance. At lower gains, CMR depends mainly on thin-film resistor stability but due to gain-bandwidth considerations, is relatively constant with frequency to beyond 60Hz. The dc CMR improves with increasing gain and is increasingly subject to phase shifts in limited bandwidth high-gain amplifiers. Figure 5 illustrates CMR vs. Gain and Frequency.

Dynamic Performance: Settling time and unity gain bandwidth are directly proportional to gain. As a result, dynamic performance can be predicted from the well-behaved curves of Figure 6.

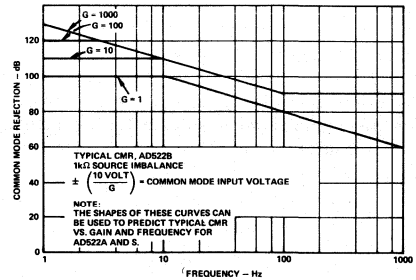


Figure 5. Common Mode Rejection vs. Frequency and Gain

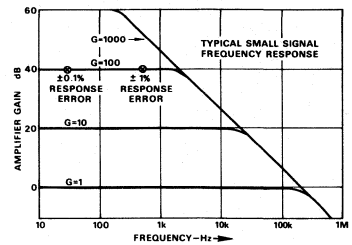


Figure 6. Small Signal Frequency Response (-3dB)

SPECIAL APPLICATIONS

Offset and Gain Trim: Gain accuracy depends largely on the quality of R_G. A precision resistor with a 10ppm/°C temperature coefficient is advised. Offset, like gain, is laser-trimmed to a level suitable for most applications. If further adjustment is required, the circuit shown in Figure 1 is recommended. Note that good quality (25ppm) pots are necessary to maintain voltage drift specifications.

CMR Trim: A short-term CMR improvement of up to 10dB at low gains can be realized with the circuit of Figure 2. Apply a low-frequency 20/G volt peak-to-peak input signal to *both* inputs through their equivalent source resistances and trim the pot for an ac output null .

Sense Output: A sense output is provided to enable remote load sensing or use of an output current booster. Figure 7 illustrates these applications. Being "inside the loop", booster drift errors are minimized. When not used, the sense output should be tied to the output.

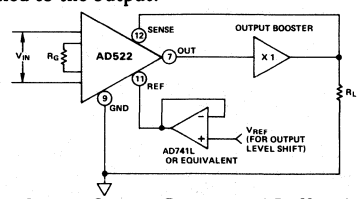


Figure 7. Output Current Booster and Buffered Output Level Shifter

Reference Output: The reference terminal is provided to permit the user to offset or "level shift" the output level to a datum compatible with his load. It must be remembered that the total output swing is ±10 volts to be shared between signal and reference offset. Furthermore, any reference source resistance will unbalance the CMR trim by the ratio $10k/R_{ref}$. For example, if the reference source impedance is 1Ω, CMR will be reduced to 80dB (10kΩ/1Ω = 10,000 = 80dB). A buffer amplifier can be used to eliminate this error, as shown in Figure 7, but the drift of the buffer will add to output offset drift. When not used, the reference terminal should be grounded.

ANALOG DEVICES

Precision Instrumentation Amplifier

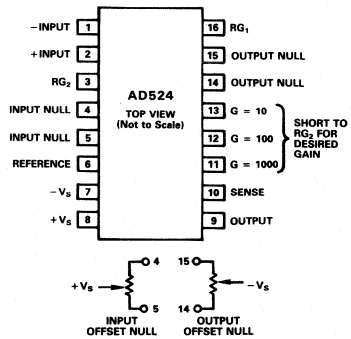
AD524

FEATURES

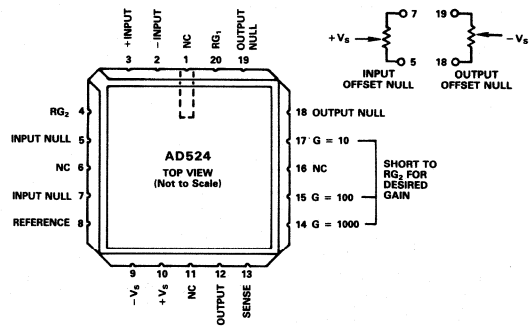
Low Noise: 0.3μV p-p 0.1Hz to 10Hz
Low Nonlinearity: 0.003% (G = 1)
High CMRR: 120dB (G = 1000)
Low Offset Voltage: 50μV
Low Offset Voltage Drift: 0.5μV/°C
Gain Bandwidth Product: 25MHz
Pin Programmable Gains of 1, 10, 100, 1000
Input Protection, Power On – Power Off
No External Components Required
Internally Compensated
MIL-STD-883B, Chips, and Plus Parts Available
16-Pin Ceramic DIP and SOIC Packages and 20-Terminal Leadless Chip Carriers Available
Available in Tape and Reel in Accordance with EIA-481A Standard
Standard Military Drawing Also Available

CONNECTION DIAGRAMS

Ceramic (D) and SOIC (R) Packages



Leadless Chip Carrier (E) Package



PRODUCT DESCRIPTION

The AD524 is a precision monolithic instrumentation amplifier designed for data acquisition applications requiring high accuracy under worst-case operating conditions. An outstanding combination of high linearity, high common mode rejection, low offset voltage drift, and low noise makes the AD524 suitable for use in many data acquisition systems.

The AD524 has an output offset voltage drift of less than 25μV/°C, input offset voltage drift of less than 0.5μV/°C, CMR above 90dB at unity gain (120dB at G = 1000) and maximum nonlinearity of 0.003% at G = 1. In addition to the outstanding dc specifications the AD524 also has a 25MHz gain bandwidth product (G = 100). To make it suitable for high speed data acquisition systems the AD524 has an output slew rate of 5V/μs and settles in 15μs to 0.01% for gains of 1 to 100.

As a complete amplifier the AD524 does not require any external components for fixed gains of 1, 10, 100 and 1,000. For other gain settings between 1 and 1000 only a single resistor is required. The AD524 input is fully protected for both power on and power off fault conditions.

The AD524 IC instrumentation amplifier is available in four different versions of accuracy and operating temperature range. The economical "A" grade, the low drift "B" grade and lower drift, higher linearity "C" grade are specified from −25°C to +85°C. The "S" grade guarantees performance to specification over the extended temperature range −55°C to +125°C. Devices are available in 16-pin ceramic DIP and SOIC packages and a 20-terminal leadless chip carrier.

PRODUCT HIGHLIGHTS

1. The AD524 has guaranteed low offset voltage, offset voltage drift and low noise for precision high gain applications.
2. The AD524 is functionally complete with pin programmable gains of 1, 10, 100 and 1000, and single resistor programmable for any gain.
3. Input and output offset nulling terminals are provided for very high precision applications and to minimize offset voltage changes in gain ranging applications.
4. The AD524 is input protected for both power on and power off fault conditions.
5. The AD524 offers superior dynamic performance with a gain bandwidth product of 25MHz, full power response of 75kHz and a settling time of 15μs to 0.01% of a 20V step (G = 100).

AD524—SPECIFICATIONS (@ V_S = ±15V, R_L = 2kΩ and T_A = +25°C unless otherwise noted)

Model	AD524A Min	AD524A Typ	AD524A Max	AD524B Min	AD524B Typ	AD524B Max	AD524C Min	AD524C Typ	AD524C Max	AD524S Min	AD524S Typ	AD524S Max	Units
GAIN													
Gain Equation (External Resistor Gain Programming)		$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$		
Gain Range (Pin Programmable)		1 to 1000			1 to 1000			1 to 1000			1 to 1000		
Gain Error													
G = 1			±0.05			±0.03			±0.02			±0.05	%
G = 10			±0.25			±0.15			±0.1%			±0.25	%
G = 100			±0.5			±0.35			±0.25			±0.5	%
G = 1000			±2.0			±1.0			±0.5			±2.0	%
Nonlinearity													
G = 1			±0.01			±0.005			±0.003			±0.01	%
G = 10, 100			±0.01			±0.005			±0.003			±0.01	%
G = 1000			±0.01			±0.01			±0.01			±0.01	%
Gain vs. Temperature													
G = 1			5			5			5			5	ppm/°C
G = 10			15			10			10			10	ppm/°C
G = 100			35			25			25			25	ppm/°C
G = 1000			100			50			50			50	ppm/°C
VOLTAGE OFFSET (May be Nulled)													
Input Offset Voltage			250			100			50			100	µV
vs. Temperature			2			0.75			0.5			2.0	µV/°C
Output Offset Voltage			5			3			2.0			3.0	mV
vs. Temperature			100			50			25			50	µV/°C
Offset Referred to the Input vs. Supply													
G = 1	70			75			80			75			dB
G = 10	85			95			100			95			dB
G = 100	95			105			110			105			dB
G = 1000	100			110			115			110			dB
INPUT CURRENT													
Input Bias Current			±50			±25			±15			±50	nA
vs. Temperature		±100			±100			±100			±100		pA/°C
Input Offset Current			±35			±15			±10			±35	nA
vs. Temperature		±100			±100			±100			±100		pA/°C
INPUT													
Input Impedance													
Differential Resistance		10^9			10^9			10^9			10^9		Ω
Differential Capacitance		10			10			10			10		pF
Common Mode Resistance		10^9			10^9			10^9			10^9		Ω
Common Mode Capacitance		10			10			10			10		pF
Input Voltage Range													
Max Differ. Input Linear (V_{DIL})[1]	±10			±10			±10			±10			V
Max Common Mode Linear (V_{CM})		$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$		V
Common Mode Rejection dc to 60Hz with 1kΩ Source Imbalance													
G = 1	70			75			80			70			dB
G = 10	90			95			100			90			dB
G = 100	100			105			110			100			dB
G = 1000	110			115			120			110			dB
OUTPUT RATING													
V_{OUT}, R_L = 2kΩ		±10			±10			±10			±10		V
DYNAMIC RESPONSE													
Small Signal -3dB													
G = 1		1			1			1			1		MHz
G = 10		400			400			400			400		kHz
G = 100		150			150			150			150		kHz
G = 1000		25			25			25			25		kHz
Slew Rate		5.0			5.0			5.0			5.0		V/µs
Settling Time to 0.01%, 20V Step													
G = 1 to 100		15			15			15			15		µs
G = 1000		75			75			75			75		µs
NOISE													
Voltage Noise, 1kHz													
R.T.I.		7			7			7			7		$nV/\sqrt{Hz}$
R.T.O.		90			90			90			90		$nV/\sqrt{Hz}$
R.T.I., 0.1 to 10Hz													
G = 1		15			15			15			15		µV p-p
G = 10		2			2			2			2		µV p-p
G = 100, 1000		0.3			0.3			0.3			0.3		µV p-p
Current Noise													
0.1Hz to 10Hz		60			60			60			60		pA p-p

Model	AD524A Min	AD524A Typ	AD524A Max	AD524B Min	AD524B Typ	AD524B Max	AD524C Min	AD524C Typ	AD524C Max	AD524S Min	AD524S Typ	AD524S Max	Units
SENSE INPUT													
R_{IN}		20			20			20			20		kΩ ±20%
I_{IN}		15			15			15			15		μA
Voltage Range	±10			±10			±10			±10			V
Gain to Output		1			1			1			1		%
REFERENCE INPUT													
R_{IN}		40			40			40			40		kΩ ±20%
I_{IN}		15			15			15			15		μA
Voltage Range	±10			±10			10			10			V
Gain to Output		1			1			1			1		%
TEMPERATURE RANGE													
Specified Performance	−25		+85	−25		+85	−25		+85	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
POWER SUPPLY													
Power Supply Range	**±6**	±15	**±18**	**±6**	±15	**±18**	**±6**	±15	**±18**	**±6**	±15	**±18**	V
Quiescent Current		3.5	**5.0**		3.5	**5.0**		3.5	**5.0**		3.5	**5.0**	mA

NOTES
[1]V_{OL} is the maximum differential input voltage at G = 1 for specified nonlinearity.
V_{DL} at other gains = 10V/G.
V_D = Actual differential input voltage.
Example: G = 10, V_D = 0.50
V_{CM} = 12V − (10/2 × 0.50V) = 9.5V
Specifications subject to change without notice.
All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

4

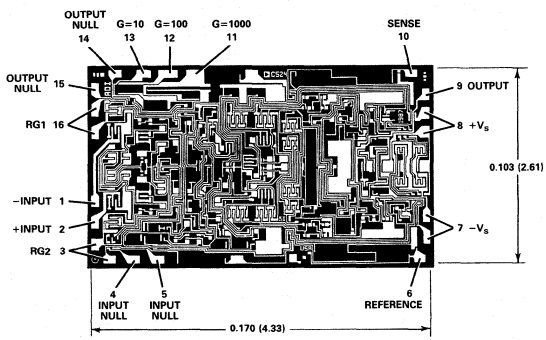
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18V
Internal Power Dissipation 450mW
Input Voltage,[2]
(Either Input Simultaneously) $|V_{IN}| + |V_S|$ . . . . . <36V
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range
(R) . . . . . −65°C to +125°C
(D, E) . . . . . −65°C to +150°C
Operating Temperature Range
AD524A/B/C . . . . . −25°C to +85°C
AD524S . . . . . −55°C to +125°C
Lead Temperature Range (Soldering 60 seconds) . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Max input voltage specification refers to maximum voltage to which either input terminal may be raised with or without device power applied. For example, with ±18 volt supplies max V_{IN} is ±18 volts, with zero supply voltage max V_{IN} is ±36 volts.

METALIZATION PHOTOGRAPHY

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



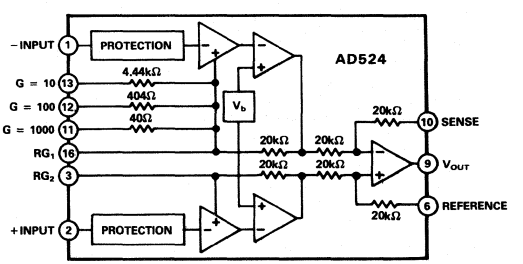
PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE D-16 AND R-16 16-PIN CERAMIC PACKAGES.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD524AD	−40°C to +85°C	16-Pin Ceramic DIP	D-16
AD524AE	−40°C to +85°C	20-Pin Leadless Chip Carrier	E-20A
AD524AR	−40°C to +85°C	16-Pin Gull-Wing SOIC	R-16
AD524AR-REEL	−40°C to +85°C	Tape & Reel Packaging	
AD524BD	−40°C to +85°C	16-Pin Ceramic DIP	D-16
AD524BE	−40°C to +85°C	20-Pin Leadless Chip Carrier	E-20A
AD524CD	−40°C to +85°C	16-Pin Ceramic DIP	D-16
AD524CE	−40°C to +85°C	20-Pin Leadless Chip Carrier	E-20A
AD524SD	−55°C to +125°C	16-Pin Ceramic DIP	D-16
AD524SE	−55°C to +125°C	20-Pin Leadless Chip Carrier	E-20A
AD524SD/883B	−55°C to +125°C	16-Pin Ceramic DIP	D-16
AD524SE/883B	−55°C to +125°C	20-Pin Leadless Chip Carrier	E-20A
AD524AChips	−40°C to +85°C	Die	
AD524CChips	−40°C to +85°C	Die	
AD524SChips	−55°C to +125°C	Die	

*For outline information see Package Information section.

FUNCTIONAL BLOCK DIAGRAM



AD524—Typical Characteristics

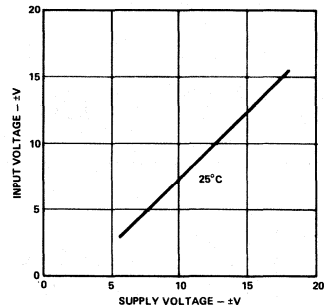


Figure 1. Input Voltage Range vs. Supply Voltage, G = 1

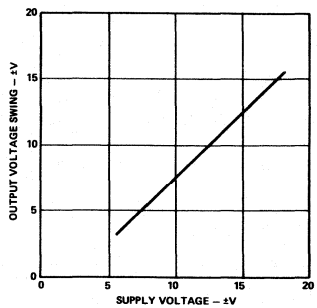


Figure 2. Output Voltage Swing vs. Supply Voltage

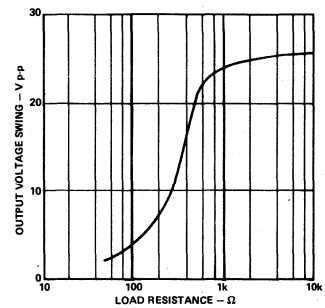


Figure 3. Output Voltage Swing vs. Load Resistance

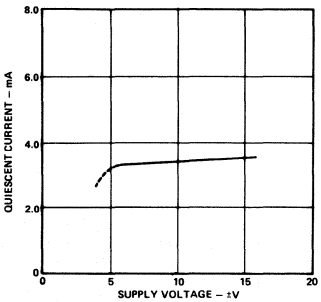


Figure 4. Quiescent Current vs. Supply Voltage

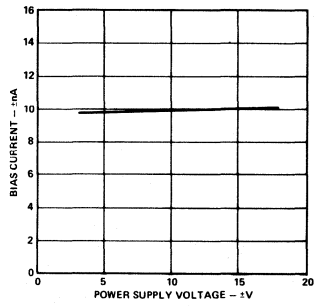


Figure 5. Input Bias Current vs. Supply Voltage

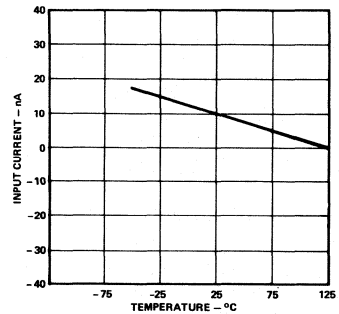


Figure 6. Input Bias Current vs. Temperature

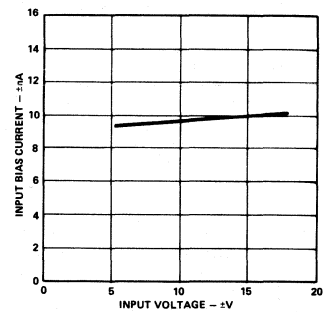


Figure 7. Input Bias Current vs. CMV

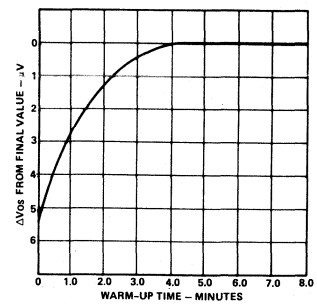


Figure 8. Offset Voltage, RTI, Turn On Drift

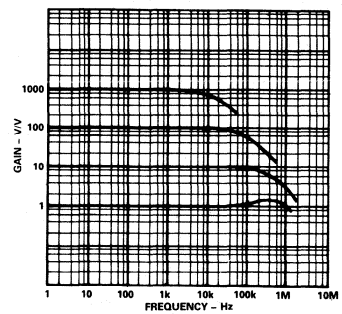


Figure 9. Gain vs. Frequency

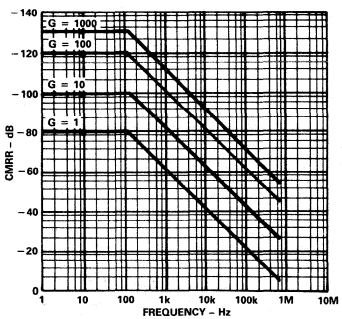


Figure 10. CMRR vs. Frequency RTI, Zero to 1k Source Imbalance

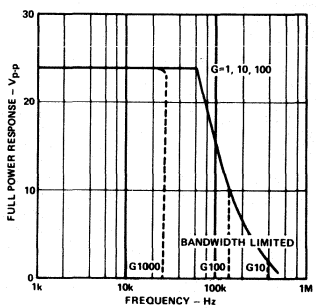


Figure 11. Large Signal Frequency Response

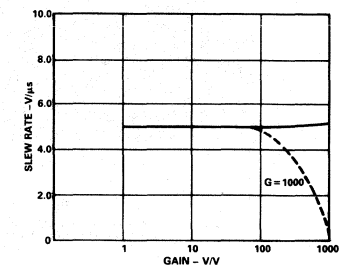


Figure 12. Slew Rate vs. Gain

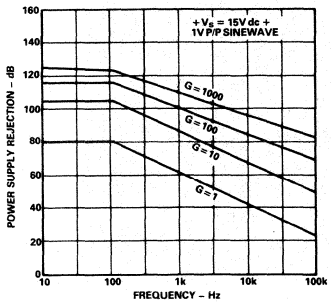


Figure 13. Positive PSRR vs. Frequency

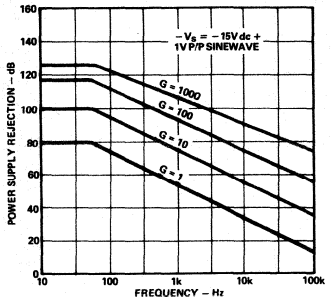


Figure 14. Negative PSRR vs. Frequency

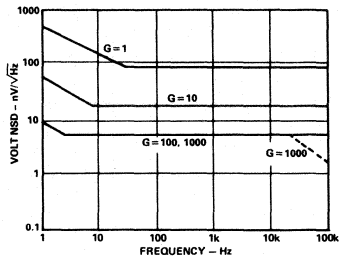


Figure 15. RTI Noise Spectral Density vs. Gain

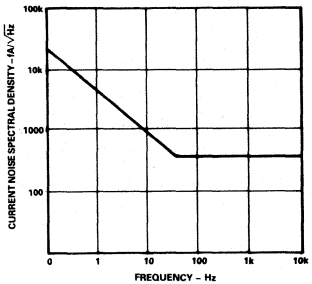


Figure 16. Input Current

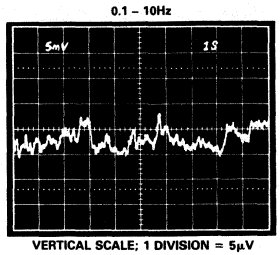


Figure 17. Low Frequency Noise – G = 1 (System Gain = 1000)

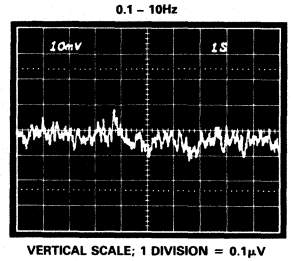


Figure 18. Low Frequency Noise – G = 1000 (System Gain = 100,000)

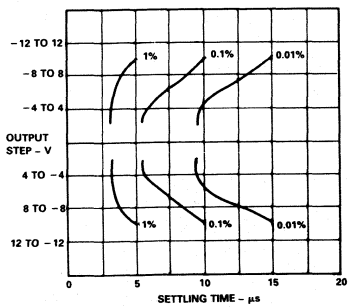


Figure 19. Settling Time Gain = 1

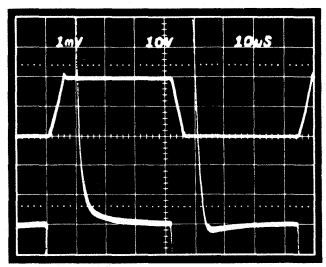


Figure 20. Large Signal Pulse Response and Settling Time – G = 1

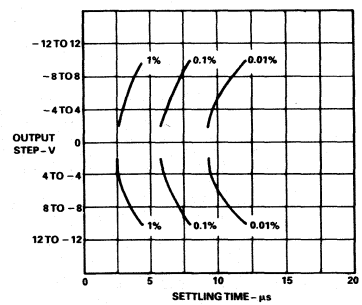


Figure 21. Settling Time Gain = 10

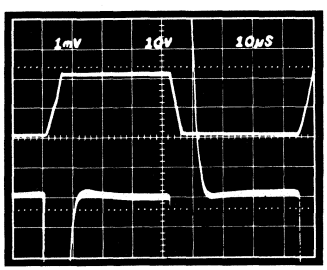


Figure 22. Large Signal Pulse Response and Settling Time G = 10

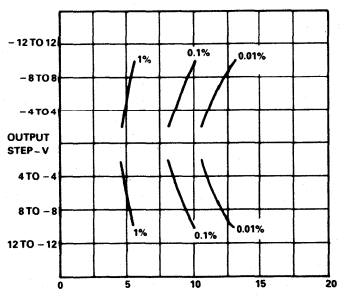


Figure 23. Settling Time Gain = 100

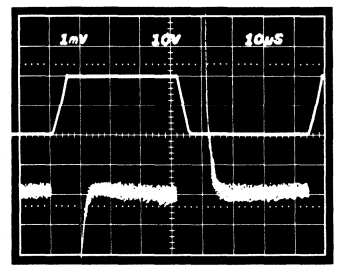


Figure 24. Large Signal Pulse Response and Settling Time G = 100

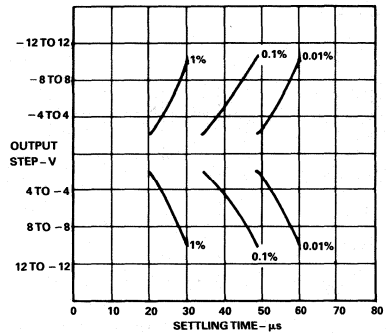


Figure 25. Settling Time Gain = 1000

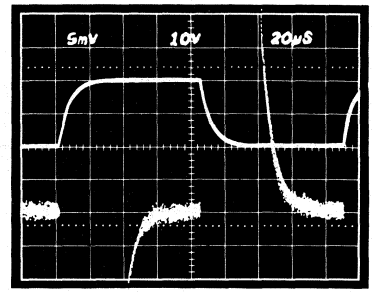


Figure 26. Large Signal Pulse Response and Settling Time G = 1000

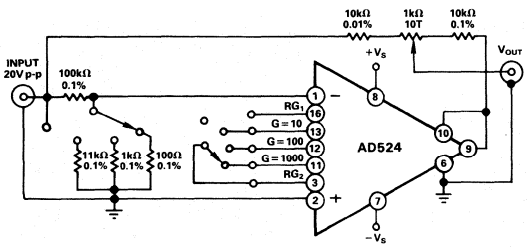


Figure 27. Settling Time Test Circuit

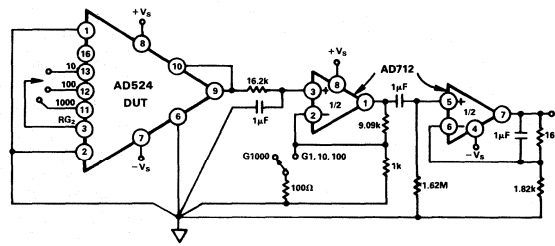


Figure 28. Noise Test Circuit

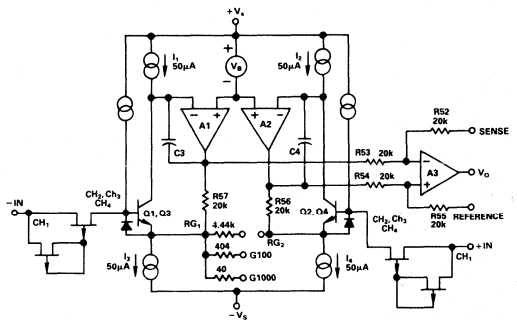


Figure 29. Simplified Circuit of Amplifier; Gain is Defined as ((R56 + R57)/(R_G) + 1. For a Gain of 1, R_G is an Open Circuit

Theory of Operation

The AD524 is a monolithic instrumentation amplifier based on the classic 3 op amp circuit. The advantage of monolithic construction is the closely matched components that enhance the performance of the input preamp. The preamp section develops the programmed gain by the use of feedback concepts. The programmed gain is developed by varying the value of R_G (smaller values increase the gain) while the feedback forces the collector currents Q1, Q2, Q3 and Q4 to be constant which impresses the input voltage across R_G.

As R_G is reduced to increase the programmed gain, the transconductance of the input preamp increases to the transconductance of the input transistors. This has three important advantages. First, this approach allows the circuit to achieve a very high open loop gain of 3×10^8 at a programmed gain of 1000 thus reducing gain related errors to a negligible 30ppm. Second, the gain bandwith product which is determined by C3 or C4 and the input transconductance, reaches 25MHz. Third, the input voltage noise reduces to a value determined by the collector current of the input transistors for an RTI noise of $7nV/\sqrt{Hz}$ at G = 1000.

INPUT PROTECTION

As interface amplifiers for data acquisition systems, instrumentation amplifiers are often subjected to input overloads, i.e., voltage levels in excess of the full scale for the selected gain range. At low gains, 10 or less, the gain resistor acts as a current limiting element in series with the inputs. At high gains the lower value of R_G will not adequately protect the inputs from excessive currents. Standard practice would be to place series limiting resistors in each input, but to limit input current to below 5mA with a full differential overload (36V) would require over 7k of resistance which would add $10nV\sqrt{Hz}$ of noise. To provide both input protection and low noise a special series protect FET was used.

A unique FET design was used to provide a bidirectional current limit, thereby, protecting against both positive and negative overloads. Under nonoverload conditions, three channels CH_2, CH_3, CH_4, act as a resistance ($\approx$1kΩ) in series with the input as before. During an overload in the positive direction, a fourth channel, CH_1, acts as a small resistance ($\approx$3kΩ) in series with the gate, which draws only the leakage current, and the FET limits I_{DSS}. When the FET enhances under a negative overload, the gate current must go through the small FET formed by CH_1 and when this FET goes into saturation, the gate current is limited and the main FET will go into controlled enhancement. The bidirectional limiting holds the maximum input current to 3mA over the 36V range.

INPUT OFFSET AND OUTPUT OFFSET

Voltage offset specifications are often considered a figure of merit for instrumentation amplifiers. While initial offset may be adjusted to zero, shifts in offset voltage due to temperature variations will cause errors. Intelligent systems can often correct for this factor with an auto-zero cycle, but there are many small-signal high-gain applications that don't have this capability.

Voltage offset and drift comprise two components each; input and output offset and offset drift. Input offset is that component of offset that is directly proportional to gain i.e., input offset as measured at the output at G = 100 is 100 times greater than at G = 1. Output offset is independent of gain. At low gains, output offset drift is dominant, while at high gains input offset drift dominates. Therefore, the output offset voltage drift is normally specified as drift at G = 1 (where input effects are insignificant), while input offset voltage drift is given by drift specification at a high gain (where output offset effects are negligible). All input-related numbers are referred to the input (RTI) which is to say that the effect on the output is "G" times larger. Voltage offset vs. power supply is also specified at one or more gain settings and is also RTI.

By separating these errors, one can evaluate the total error independent of the gain setting used. In a given gain configuration both errors can be combined to give a total error referred to the input (R.T.I.) or output (R.T.O.) by the following formula:

Total Error R.T.I. = input error + (output error/gain)

Total Error R.T.O. = (Gain × input error) + output error

As an illustration, a typical AD524 might have a +250μV output offset and a −50μV input offset. In a unity gain configuration, the *total* output offset would be 200μV or the sum of the two. At a gain of 100, the output offset would be −4.75mV or: +250μV + 100(−50μV) = −4.75mV.

The AD524 provides for both input and output offset adjustment. This simplifies very high precision applications and minimize offset voltage changes in switched gain applications. In such applications the input offset is adjusted first at the highest programmed gain, then the output offset is adjusted at G = 1.

GAIN

The AD524 has internal high accuracy pretrimmed resistors for pin programmable gain of 1, 10, 100 and 1000. One of the preset gains can be selected by pin strapping the appropriate gain terminal and RG_2 together (for G = 1 RG_2 is not connected).

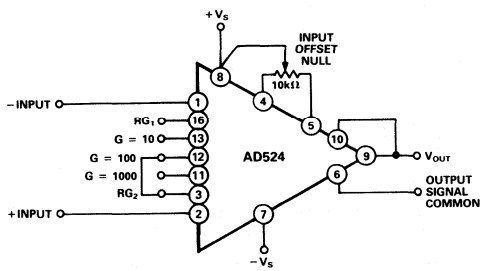


Figure 30. Operating Connections for G = 100

The AD524 can be configured for gains other than those that are internally preset; there are two methods to do this. The first method uses just an external resistor connected between pins 3 and 16 which programs the gain according to the formula $R_G = \frac{40k}{G-1}$ (see Figure 31). For best results R_G should be a precision resistor with a low temperature coefficient. An external R_G affects both gain accuracy and gain drift due to the mismatch between it and the internal thin-film resistors. Gain accuracy is determined by the tolerance of the external R_G and the absolute accuracy of the internal resistors (±20%). Gain drift is determined by the mismatch of the temperature coefficient of R_G and the temperature coefficient of the internal resistors (−50ppm/°C typ).

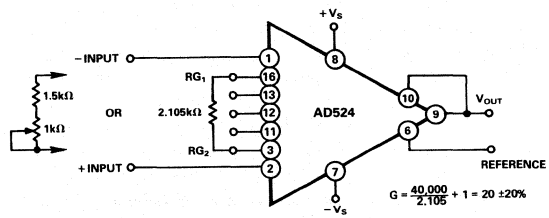


Figure 31. Operating Connections for G = 20

The second technique uses the internal resistors in parallel with an external resistor (Figure 32). This technique minimizes the gain adjustment range and reduces the effects of temperature coefficient sensitivity.

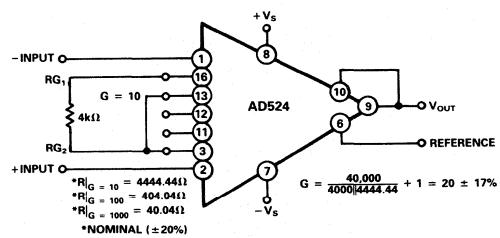


Figure 32. Operating Connections for G = 20, Low Gain T.C. Technique

The AD524 may also be configured to provide gain in the output stage. Figure 33 shows an H pad attenuator connected to the reference and sense lines of the AD524. R1, R2 and R3 should be made as low as possible to minimize the gain variation and reduction of CMRR. Varying R2 will precisely set the gain without affecting CMRR. CMRR is determined by the match of R1 and R3.

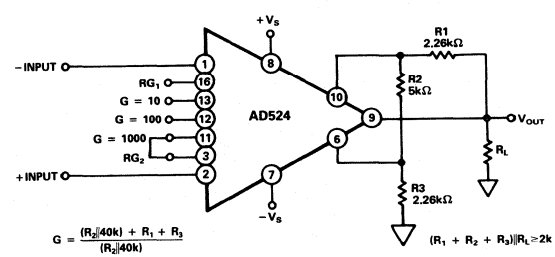


Figure 33. Gain of 2000

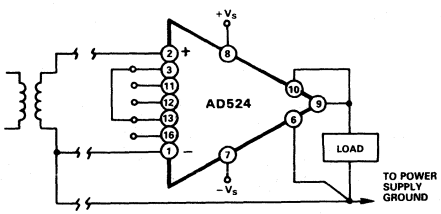
Output Gain	R2	R1,R3	Nominal Gain
2	5kΩ	2.26kΩ	2.02
5	1.05kΩ	2.05kΩ	5.01
10	1kΩ	4.42kΩ	10.1

Table I. Output Gain Resistor Values

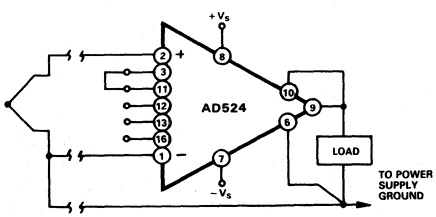
INPUT BIAS CURRENTS

Input bias currents are those currents necessary to bias the input transistors of a dc amplifier. Bias currents are an additional source of input error and must be considered in an total error budget. The bias currents when multiplied by the source resistance appear as an offset voltage. What is of concern in calculating bias current errors is the change in bias current with respect to signal voltage and temperature. Input offset current is the difference between the two input bias currents. The effect of offset current is an input offset voltage whose magnitude is the offset current times the source impedance imbalance.

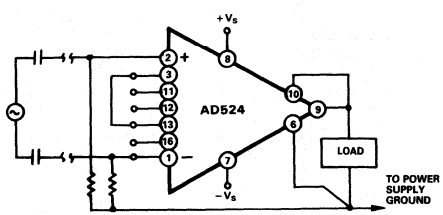
Although instrumentation amplifiers have differential inputs, there must be a return path for the bias currents. If this is not provided, those currents will charge stray capacitances, causing the output to drift uncontrollably or to saturate. Therefore, when amplifying "floating" input sources such as transformers and thermocouples, as well as ac-coupled sources, there must still be a dc path from each input to ground.



a. Transformer Coupled



b. Thermocouple



c. AC Coupled

Figure 34. Indirect Ground Returns for Bias Currents

COMMON-MODE REJECTION

Common-mode rejection is a measure of the change in output voltage when both inputs are changed equal amounts. These specifications are usually given for a full-range input voltage change and a specified source imbalance. "Common-Mode Rejection Ratio" (CMRR) is a ratio expression while "Common-Mode Rejection" (CMR) is the logarithm of that ratio. For example, a CMRR of 10,000 corresponds to a CMR of 80dB.

In an instrumentation amplifier, ac common-mode rejection is only as good as the differential phase shift. Degradation of ac common-mode rejection is caused by unequal drops across differing track resistances and a differential phase shift due to varied stray capacitances or cable capacitances. In many applications shielded cables are used to minimize noise. This technique can create common mode rejection errors unless the shield is properly driven. Figures 35 and 36 shows active data guards which are configured to improve ac common mode rejection by "bootstrapping" the capacitances of the input cabling, thus minimizing differential phase shift.

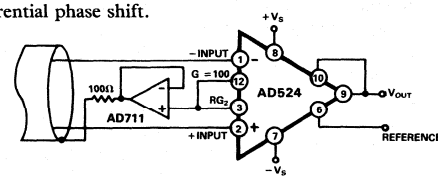


Figure 35. Shield Driver, G ≥ 100

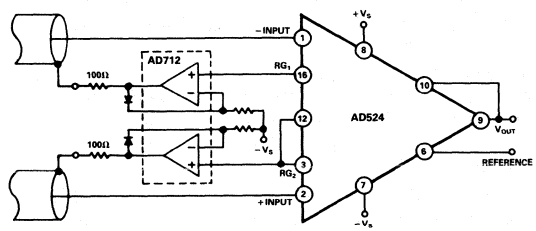


Figure 36. Differential Shield Driver

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths

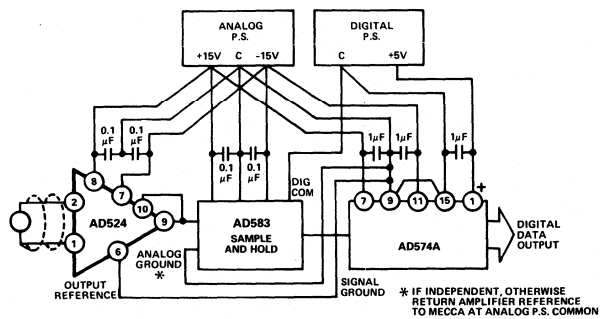


Figure 37. Basic Grounding Practice

have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the data acquisition components. Separate ground returns should be provided to minimize the current flow in the path from the sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Since the output voltage is developed with respect to the potential on the reference terminal an instrumentation amplifier can solve many grounding problems.

SENSE TERMINAL

The sense terminal is the feedback point for the instrument amplifier's output amplifier. Normally it is connected to the instrument amplifier output. If heavy load currents are to be drawn through long leads, voltage drops due to current flowing through lead resistance can cause errors. The sense terminal can be wired to the instrument amplifier at the load thus putting the IxR drops "inside the loop" and virtually eliminating this error source.

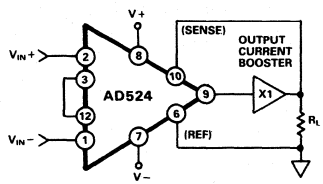


Figure 38. AD524 Instrumentation Amplifier with Output Current Booster

Typically, IC instrumentation amplifiers are rated for a full ±10 volt output swing into 2kΩ. In some applications, however, the need exists to drive more current into heavier loads. Figure 38 shows how a high-current booster may be connected "inside the loop" of an instrumentation amplifier to provide the required current boost without significantly degrading overall performance. Nonlinearities, offset and gain inaccuracies of the buffer are minimized by the loop gain of the IA output amplifier. Offset drift of the buffer is similarly reduced.

REFERENCE TERMINAL

The reference terminal may be used to offset the output by up to ±10V. This is useful when the load is "floating" or does not share a ground with the rest of the system. It also provides a direct means of injecting a precise offset. It must be remembered that the total output swing is ±10 volts to be shared between signal and reference offset.

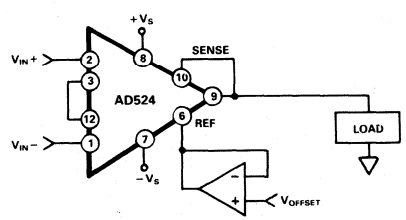


Figure 39. Use of Reference Terminal to Provide Output Offset

When the IA is of the three-amplifier configuration it is necessary that nearly zero impedance be presented to the reference terminal. Any significant resistance from the reference terminal to ground increases the gain of the noninverting signal path thereby upsetting the common-mode rejection of the IA.

In the AD524 a reference source resistance will unbalance the CMR trim by the ratio of $20k\Omega/R_{REF}$. For example, if the reference source impedance is 1Ω, CMR will be reduced to 86dB ($20k\Omega/1\Omega = 86dB$). An operational amplifier may be used to provide that low impedance reference point as shown in Figure 39. The input offset voltage characteristics of that amplifier will add directly to the output offset voltage performance of the instrumentation amplifier.

An instrumentation amplifier can be turned into a voltage-to-current converter by taking advantage of the sense and reference terminals as shown in Figure 40.

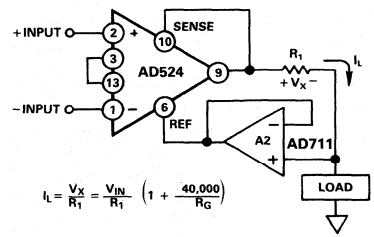


Figure 40. Voltage-to-Current Converter

By establishing a reference at the "low" side of a current setting resistor, an output current may be defined as a function of input voltage, gain and the value of that resistor. Since only a small current is demanded at the input of the buffer amplifier A_2, the forced current I_L will largely flow through the load. Offset and drift specifications of A_2 must be added to the output offset and drift specifications of the IA.

PROGRAMMABLE GAIN

Figure 41 shows the AD524 being used as a software programmable gain amplifier. Gain switching can be accomplished with mechanical switches such as DIP switches or reed relays. It should be noted that the "on" resistance of the switch in series with the internal gain resistor becomes part of the gain equation and will have an effect on gain accuracy.

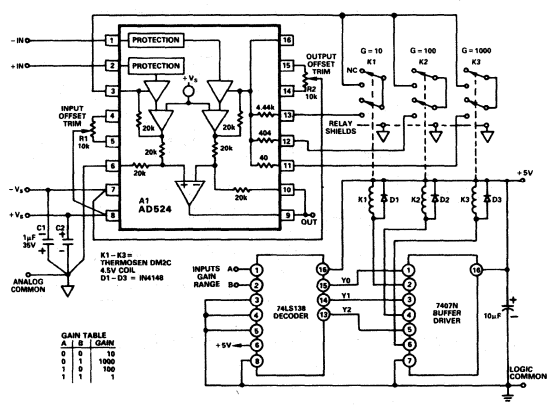


Figure 41. 3 Decade Gain Programmable Amplifier

The AD524 can also be connected for gain in the output stage. Figure 42 shows an AD547 used as an active attenuator in the output amplifier's feedback loop. The active attenuation presents a very low impedance to the feedback resistors therefore minimizing the common rejection ratio degradation.

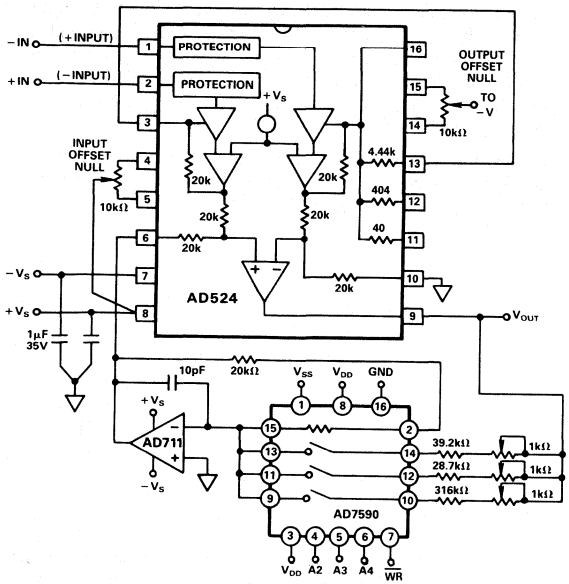


Figure 42. Programmable Output Gain

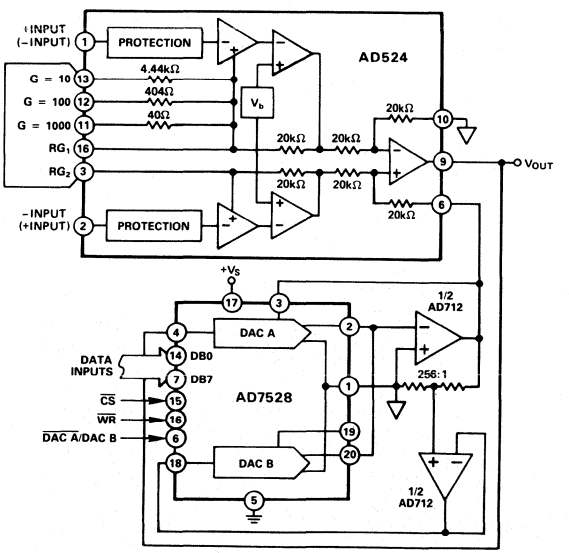


Figure 43. Programmable Output Gain Using a DAC

Another method for developing the switching scheme is to use a DAC. The AD7528 dual DAC which acts essentially as a pair of switched resistive attenuators having high analog linearity and symmetrical bipolar transmission is ideal in this application. The multiplying DAC's advantage is that it can handle inputs of either polarity or zero without affecting the programmed gain. The circuit shown uses an AD7528 to set the gain (DAC A) and to perform a fine adjustment (DAC B).

AUTO-ZERO CIRCUITS

In many applications it is necessary to provide very accurate data in high gain configurations. At room temperature the offset effects can be nulled by the use of offset trimpots. Over the operating temperature range, however, offset nulling becomes a problem. The circuit of Figure 44 show a CMOS DAC operating in the bipolar mode and connected to the reference terminal to provide software controllable offset adjustments.

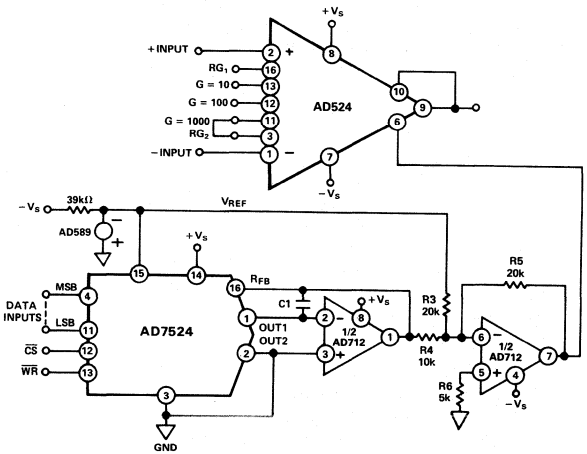


Figure 44. Software Controllable Offset

In many applications complex software algorithms for auto-zero applications are not available. For those applications Figure 45 provides a hardware solution.

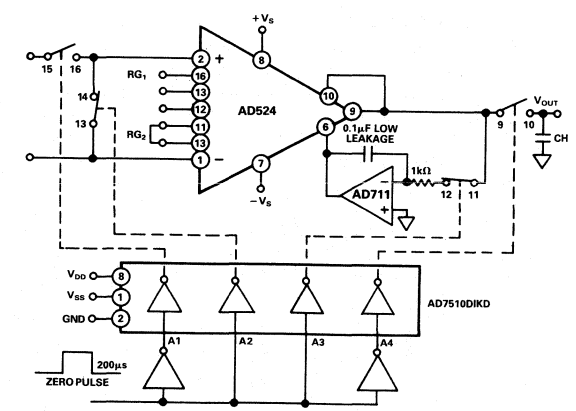


Figure 45. Auto-Zero Circuit

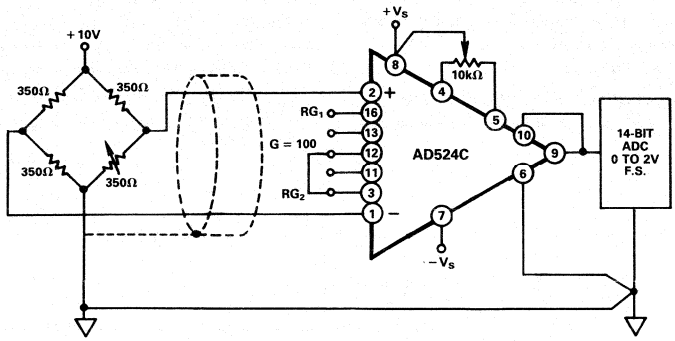


Figure 46. Typical Bridge Application

ERROR BUDGET ANALYSIS

To illustrate how instrumentation amplifier specifications are applied, we will now examine a typical case where an AD524 is required to amplify the output of an unbalanced transducer. Figure 46 shows a differential transducer, unbalanced by 100Ω, supplying a 0 to 20mV signal to an AD524C. The output of the IA feeds a 14-bit A to D converter with a 0 to 2 volt input voltage range. The operating temperature range is −25°C to +85°C. Therefore, the largest change in temperature ΔT within the operating range is from ambient to +85°C (85°C − 25°C = 60°C).

In many applications, differential linearity and resolution are of prime importance. This would be so in cases where the absolute value of a variable is less important than changes in value. In these applications, only the irreducible errors (45ppm = 0.004%) are significant. Furthermore, if a system has an intelligent processor monitoring the A to D output, the addition of a auto-gain/auto-zero cycle will remove all reducible errors and may eliminate the requirement for initial calibration. This will also reduce errors to 0.004%.

Error Source	AD524C Specifications	Calculation	Effect on Absolute Accuracy at T_A = 25°C	Effect on Absolute Accuracy at T_A = 85°C	Effect on Resolution
Gain Error	±0.25%	±0.25% = 2500ppm	2500ppm	2500ppm	–
Gain Instability	25ppm	(25ppm/°C)(60°C) = 1500ppm	–	1500ppm	–
Gain Nonlinearity	±0.003%	±0.003% = 30ppm	–	–	30ppm
Input Offset Voltage	±50μV, RTI	±50μV/20mV = ±2500ppm	2500ppm	2500ppm	–
Input Offset Voltage Drift	±0.5μV/°C	(±0.5μV/°C)(60°C) = 30μV 30μV/20mV = 1500ppm	–	1500ppm	–
Output Offset Voltage[1]	±2.0mV	±2.0mV/20mV = 1000ppm	1000ppm	1000ppm	–
Output Offset Voltage Drift[1]	±25μV/°C	(±25μV/°C)(60°C) = 1500μV 1500μV/20mV = 750ppm	–	750ppm	–
Bias Current – Source Imbalance Error	±15nA	(±15nA)(100Ω) = 1.5μV 1.5μV/20mV = 75ppm	75ppm	75ppm	–
Bias Current – Source Imbalance Drift	±100pA/°C	(±100pA/°C)(100Ω)(60°C) = 0.6μV 0.6μV/20mV = 30ppm	–	30ppm	–
Offset Current – Source Imbalance Error	±10nA	(±10nA)(100Ω) = 1μV 1μV/20mV = 50ppm	50ppm	50ppm	–
Offset Current – Source Imbalance Drift	±100pA/°C	(100pA/°C)(100Ω)(60°C) = 0.6μV 0.6μV/20mV = 30ppm	–	30ppm	–
Offset Current – Source Resistance – Error	±10nA	(10nA)(175Ω) = 3.5μV 3.5μV/20mV = 87.5ppm	87.5ppm	87.5ppm	–
Offset Current – Source Resistance – Drift	±100pA/°C	(100pA/°C)(175Ω)(60°C) = 1μV 1μV/20mV = 50ppm	–	50ppm	–
Common Mode Rejection 5V dc	115dB	115dB = 1.8ppm × 5V = 8.8μV 8.8μV/20mV = 444ppm	444ppm	444ppm	–
Noise, RTI (0.1–10Hz)	0.3μV p-p	0.3μV p-p/20mV = 15ppm	–	–	15ppm
		Total Error	6656.5ppm	10516.5ppm	45ppm

[1]Output offset voltage and output offset voltage drift are given as RTI figures.

Table II. Error Budget Analysis of AD524CD in Bridge Application

Figure 47 shows a simple application, in which the variation of the cold-junction voltage of a Type J thermocouple–iron(+)–constantan– is compensated for by a voltage developed in series by the temperature-sensitive output current of an AD590 semiconductor temperature sensor.

The circuit is calibrated by adjusting R_T for proper output voltage with the measuring junction at a known reference temperature and the circuit near 25°C. If resistors with low tempcos are used, compensation accuracy will be to within ±0.5°C, for temperatures between +15°C and +35°C. Other thermocouple types may be accommodated with the standard resistance values shown in the table. For other ranges of ambient temperature, the equation in the figure may be solved for the optimum values of R_T and R_A.

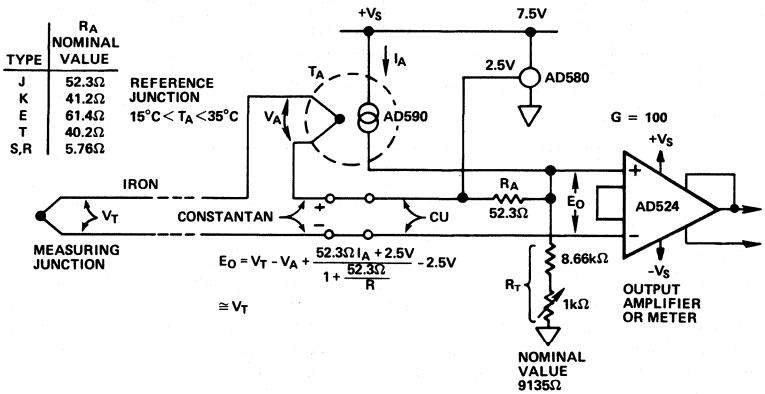


Figure 47. Cold-Junction Compensation

The microprocessor controlled data acquisition system shown in Figure 48 includes both auto-zero and auto-gain capability. By dedicating two of the differential inputs, one to ground and one to the A/D reference, the proper program calibration cycles can eliminate both initial accuracy errors and accuracy errors over temperature. The auto-zero cycle, in this application, converts a number that appears to be ground and then writes that same number (8 bit) to the AD7524 which eliminates the zero error since its output has an inverted scale. The auto-gain cycle converts the A/D reference and compares it with full scale. A multiplicative correction factor is then computed and applied to subsequent readings.

For a comprehensive study of instrumentation amplifier design and applications, refer to the *Instrumentation Amplifier Application Guide*, available free from Analog Devices.

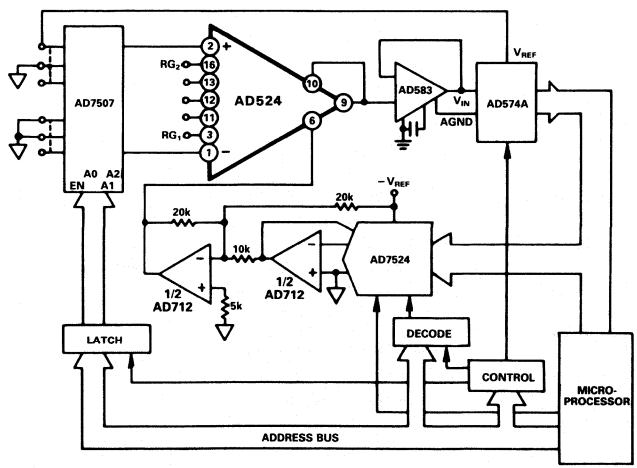


Figure 48. Microprocessor Controlled Data Acquisition System

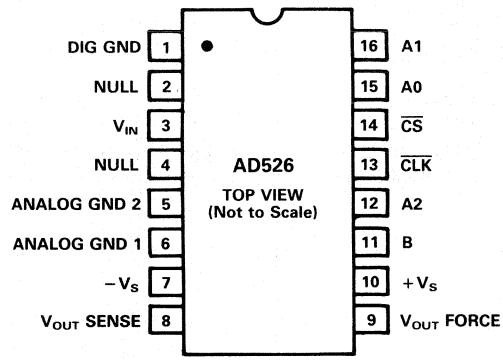
Software Programmable Gain Amplifier

AD526

FEATURES

- **Digitally Programmable Binary Gains from 1 to 16**
- **Two-Chip Cascade Mode Achieves Binary Gain from 1 to 256**
- **Gain Error:**
  - **0.01% max, Gain = 1, 2, 4 (C Grade)**
  - **0.02% max, Gain = 8, 16 (C Grade)**
  - **0.5ppm/°C Drift Over Temperature**
- **Fast Settling Time**
  - **10V Signal Change:**
    - **0.01% in 4.5μs (Gain = 16)**
  - **Gain Change:**
    - **0.01% in 5.6μs (Gain = 16)**
- **Low Nonlinearity: ±0.005% FSR max (J Grade)**
- **Excellent DC Accuracy:**
  - **Offset Voltage: 0.5mV max (C Grade)**
  - **Offset Voltage Drift: 3μV/°C (C Grade)**
- **TTL Compatible Digital Inputs**
- **Standard Military Drawing Available**

PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD526 is a single-ended, monolithic software programmable gain amplifier (SPGA) that provides gains of 1, 2, 4, 8 and 16. It is complete, including amplifier, resistor network and TTL-compatible latched inputs, and requires no external components.

Low gain error and low nonlinearity make the AD526 ideal for precision instrumentation applications requiring programmable gain. The small signal bandwidth is 350kHz at a gain of 16. In addition, the AD526 provides excellent dc precision. The FET-input stage results in a low bias current of 50pA. A guaranteed maximum input offset voltage of 0.5mV max (C grade) and low gain error (0.01%, G=1, 2, 4, C grade) are accomplished using Analog Devices' laser trimming technology.

To provide flexibility to the system designer, the AD526 can be operated in either latched or transparent mode. The force/sense configuration preserves accuracy when the output is connected to remote or low impedance loads.

The AD526 is offered in one commercial (0 to +70°C) grade, J, and three industrial grades, A, B and C, which are specified from −40°C to +85°C. The S grade is specified from −55°C to +125°C. The military version is available processed to MIL-STD 883B, Rev C. The J grade is supplied in a 16-pin plastic DIP, and the other grades are offered in a 16-pin hermetic side-brazed ceramic DIP.

APPLICATION HIGHLIGHTS

1. **Dynamic Range Extension for ADC Systems:** A single AD526 in conjunction with a 12-bit ADC can provide 96dB of dynamic range for ADC systems.
2. **Gain Ranging Pre-Amps:** The AD526 offers complete digital gain control with precise gains in binary steps from 1 to 16. Additional gains of 32, 64, 128 and 256 are possible by cascading two AD526s.

AD526—SPECIFICATIONS (@ V_S = ±15V, R_L = 2kΩ and T_A = +25°C unless otherwise otherwise specified)

Model	AD526J Min	AD526J Typ	AD526J Max	AD526A Min	AD526A Typ	AD526A Max	AD526B/S Min	AD526B/S Typ	AD526B/S Max	AD526C Min	AD526C Typ	AD526C Max	Units
GAIN													
Gain Range													
(Digitally Programmable)		1, 2, 4, 8, 16			1, 2, 4, 8, 16			1, 2, 4, 8, 16			1, 2, 4, 8, 16		
Gain Error													
G = 1			**0.05**			**0.02**			**0.01**			**0.01**	%
G = 2			**0.05**			**0.03**			**0.02**			**0.01**	%
G = 4			**0.10**			**0.03**			**0.02**			**0.01**	%
G = 8			**0.15**			**0.07**			**0.04**			**0.02**	%
G = 16			**0.15**			**0.07**			**0.04**			**0.02**	%
Gain Error Drift													
Over Temperature													
G = 1		0.5	2.0		0.5	2.0		0.5	2.0		0.5	2.0	ppm/°C
G = 2		0.5	2.0		0.5	2.0		0.5	2.0		0.5	2.0	ppm/°C
G = 4		0.5	3.0		0.5	3.0		0.5	3.0		0.5	3.0	ppm/°C
G = 8		0.5	5.0		0.5	5.0		0.5	5.0		0.5	5.0	ppm/°C
G = 16		1.0	5.0		1.0	5.0		1.0	5.0		1.0	5.0	ppm/°C
Gain Error (T_{min} to T_{max})													
G = 1			0.06			**0.03**			**0.02**			**0.015**	%
G = 2			0.06			**0.04**			**0.03**			**0.015**	%
G = 4			0.12			**0.04**			**0.03**			**0.015**	%
G = 8			0.17			**0.08**			**0.05**			**0.03**	%
G = 16			0.17			**0.08**			**0.05**			**0.03**	%
Nonlinearity													
G = 1			**0.005**			**0.005**			**0.005**			**0.0035**	% FSR
G = 2			0.001			0.001			0.001			0.001	% FSR
G = 4			0.001			0.001			0.001			0.001	% FSR
G = 8			0.001			0.001			0.001			0.001	% FSR
G = 16			0.001			0.001			0.001			0.001	% FSR
Nonlinearity (T_{min} to T_{max})													
G = 1			0.01			**0.01**			**0.01**			**0.007**	% FSR
G = 2			0.001			0.001			0.001			0.001	% FSR
G = 4			0.001			0.001			0.001			0.001	% FSR
G = 8			0.001			0.001			0.001			0.001	% FSR
G = 16			0.001			0.001			0.001			0.001	% FSR
VOLTAGE OFFSET, ALL GAINS													
Input Offset Voltage		0.4	**1.5**		0.25	**0.7**		0.25	**0.5**		0.25	**0.5**	mV
Input Offset Voltage Drift Over Temperature		5	20		3	10		3	10		3	10	µV/°C
Input Offset Voltage T_{min} to T_{max}			2.0			**1.0**			**0.8**			**0.8**	mV
Input Offset Voltage vs. Supply (V_S ± 10%)	**80**			**80**			**84**			**90**			dB
INPUT BIAS CURRENT													
Over Input Voltage Range ± 10V		50	**150**		50	**150**		50	**150**		50	**150**	pA
ANALOG INPUT													
CHARACTERISTICS													
Voltage Range													
(Linear Operation)	**±10**	± 12		**±10**	± 12		**±10**	± 12		**±10**	± 12		V
Capacitance		5			5			5			5		pF
RATED OUTPUT													
Voltage	**±10**	± 12		**±10**	± 12		**±10**	± 12		**±10**	± 12		V
Current (V_{OUT} = ± 10V)	**±5**	± 10		**±5**	± 10		**±5**	± 10		**±5**	± 10		mA
Short-Circuit Current	**15**	30		**15**	30		**15**	30		**15**	30		mA
DC Output Resistance		0.002			0.002			0.002			0.002		Ω
Load Capacitance													
(For Stable Operation)		700			700			700			700		pF
NOISE, ALL GAINS													
Voltage Noise, RTI													
0.1Hz to 10Hz		3			3			3			3		µV p-p
Voltage Noise Density, RTI													
f = 10Hz		70			70			70			70		nV/√Hz
f = 100Hz		60			60			60			60		nV/√Hz
f = 1kHz		30			30			30			30		nV/√Hz
f = 10kHz		25			25			25			25		nV/√Hz

Model	AD526J Min	AD526J Typ	AD526J Max	AD526A Min	AD526A Typ	AD526A Max	AD526B/S Min	AD526B/S Typ	AD526B/S Max	AD526C Min	AD526C Typ	AD526C Max	Units
DYNAMIC RESPONSE													
– 3dB Bandwidth (Small Signal)													
G = 1		4.0			4.0			4.0			4.0		MHz
G = 2		2.0			2.0			2.0			2.0		MHz
G = 4		1.5			1.5			1.5			1.5		MHz
G = 8		0.65			0.65			0.65			0.65		MHz
G = 16		0.35			0.35			0.35			0.35		MHz
Signal Settling Time to 0.01% ($\Delta V_{OUT} = \pm 10V$)													
G = 1		2.1	4		2.1	4		2.1	4		2.1	4	µs
G = 2		2.5	5		2.5	5		2.5	5		2.5	5	µs
G = 4		2.7	5		2.7	5		2.7	5		2.7	5	µs
G = 8		3.6	7		3.6	7		3.6	7		3.6	7	µs
G = 16		4.1	7		4.1	7		4.1	7		4.1	7	µs
Full Power Bandwidth													
G = 1, 2, 4		0.10			0.10			0.10			0.10		MHz
G = 8, 16		0.35			0.35			0.35			0.35		MHz
Slew Rate													
G = 1, 2, 4	**4**	6		**4**	6		**4**	6		**4**	6		V/µs
G = 8, 16	**18**	24		**18**	24		**18**	24		**18**	24		V/µs
DIGITAL INPUTS (T_{min} to T_{max})													
Input Current (V_H = 5V)	60	100	140	60	100	140	60	100	140	60	100	140	µA
Logic "1"	2		6	2		6	2		6	2		6	V
Logic "0"	0		0.8	0		0.8	0		0.8	0		0.8	V
TIMING[1] (V_L = 0.2V, V_H = 3.7V)													
A0, A1, A2													
T_C	50			50			50			50			ns
T_S	30			30			30			30			ns
T_H	30			30			30			30			ns
B													
T_C	50			50			50			50			ns
T_S	40			40			40			40			ns
T_H	10			10			10			10			ns
TEMPERATURE RANGE													
Specified Performance	0		+70	–40		+85	–40/–55		+85/+125	–40		+85	°C
Storage	–65		+125	–65		+150	–65		+150	–65		+150	°C
POWER SUPPLY													
Operating Range	**±4.5**		**±16.5**	**±4.5**		**±16.5**	**±4.5**		**±16.5**	**±4.5**		**±16.5**	V
Positive Supply Current		10	**14**		10	**14**		10	**14**		10	**14**	mA
Negative Supply Current		10	**13**		10	**13**		10	**13**		10	**13**	mA
PACKAGE OPTIONS[2]													
Plastic (N-16)	AD526JN												
Ceramic DIP (D-16)				AD526AD			AD526BD AD526SD AD526SD/883B			AD526CD			
Chips	AD526JChips												

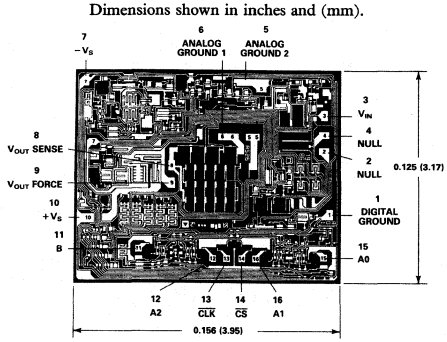
NOTES
[1]Refer to Figure 35 for definitions.
FSR = Full-Scale Range = 20V.
RTI = Referred to Input.
[2]For outline information see Package Information section.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

METALIZATION PHOTOGRAPHY

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



AD526—Typical Characteristics

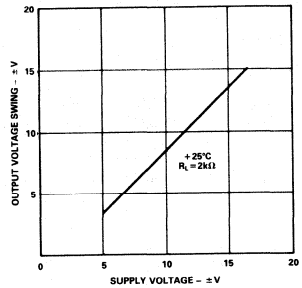


Figure 1. Output Voltage Swing vs. Supply Voltage, G = 16

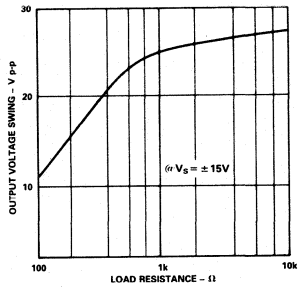


Figure 2. Output Voltage Swing vs. Load Resistance

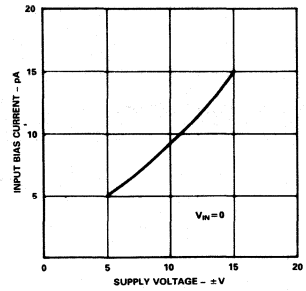


Figure 3. Input Bias Current vs. Supply Voltage

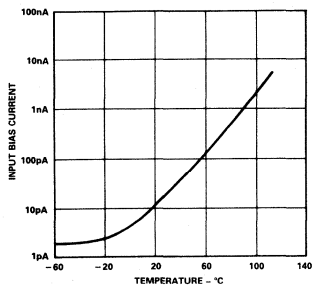


Figure 4. Input Bias Current vs. Temperature

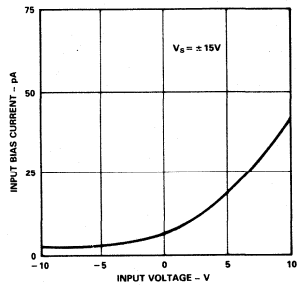


Figure 5. Input Bias Current vs. Input Voltage

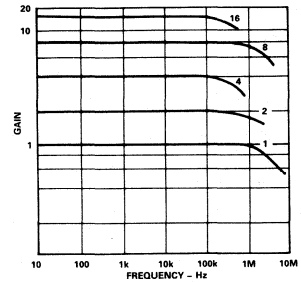


Figure 6. Gain vs. Frequency

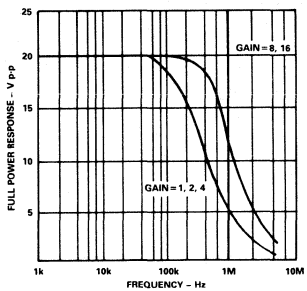


Figure 7. Large Signal Frequency Response

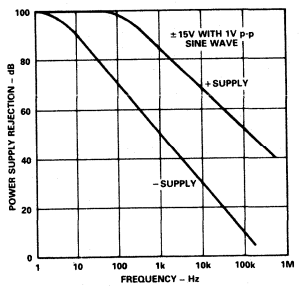


Figure 8. PSRR vs. Frequency

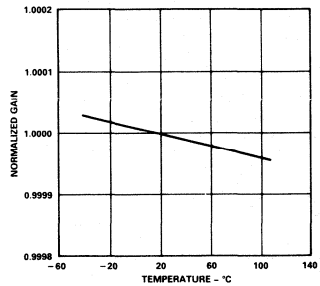


Figure 9. Normalized Gain vs. Temperature, Gain = 1

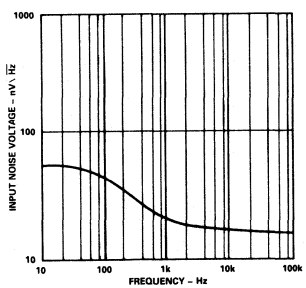


Figure 10. Noise Spectral Density

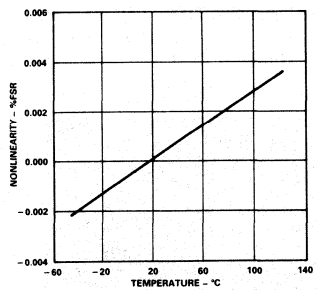


Figure 11. Nonlinearity vs. Temperature, Gain = 1

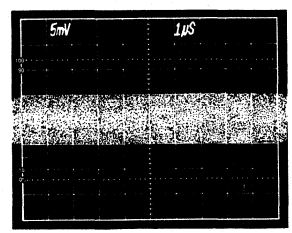


Figure 12. Wideband Output Noise, G = 16 (Amplified by 10)

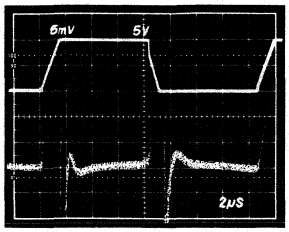


Figure 13. Large Signal Pulse Response and Settling Time*, G = 1

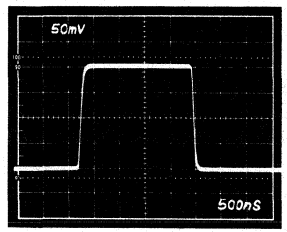


Figure 14. Small Signal Pulse Response, G = 1

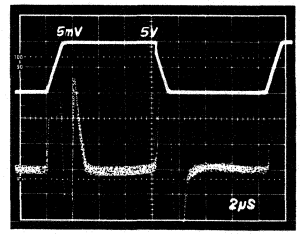


Figure 15. Large Signal Pulse Response and Settling Time*, G = 2

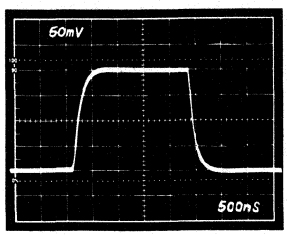


Figure 16. Small Signal Pulse Response, G = 2

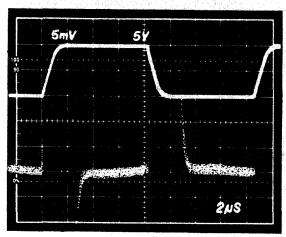


Figure 17. Large Signal Pulse Response and Settling Time*, G = 4

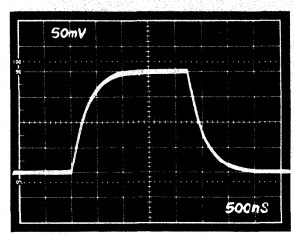


Figure 18. Small Signal Pulse Response, G = 4

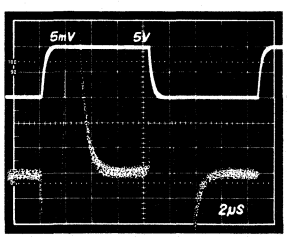


Figure 19. Large Signal Pulse Response and Settling Time*, G = 8

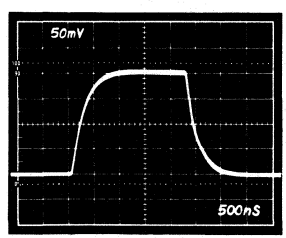


Figure 20. Small Signal Pulse Response, G = 8

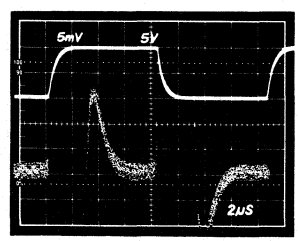


Figure 21. Large Signal Pulse Response and Settling Time*, G = 16

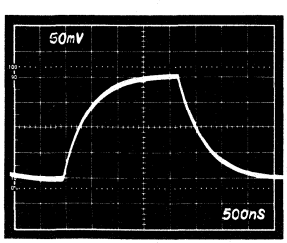


Figure 22. Small Signal Pulse Response, Gain = 16

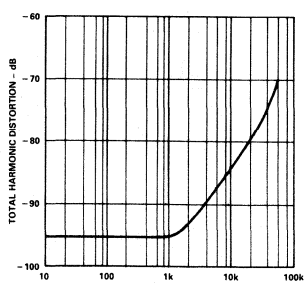


Figure 23. Total Harmonic Distortion vs. Frequency, Gain = 16

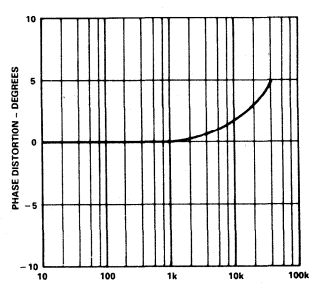


Figure 24. Phase Distortion vs. Frequency, Gain = 16

*For Settling Time Traces, 0.01% = 1/2 Vertical Division

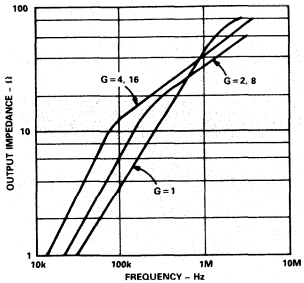


Figure 25. Output Impedance vs. Frequency

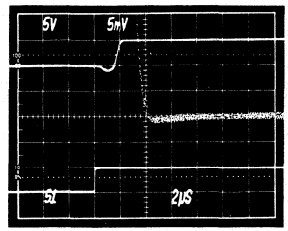


Figure 26. Gain Change Settling Time*, Gain Change: 1 to 2

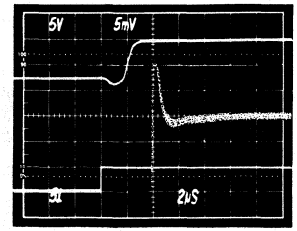


Figure 27. Gain Change Settling Time*, Gain Change 1 to 4

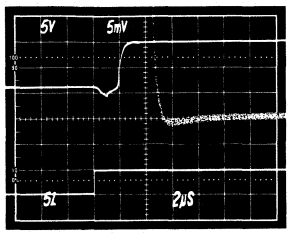


Figure 28. Gain Change Settling Time*, Gain Change 1 to 8

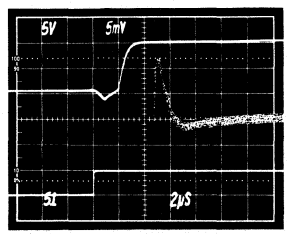


Figure 29. Gain Change Settling Time*, Gain Change 1 to 16

*Scope Traces are:
Top: Output Transition
Middle: Output Settling
Bottom: Digital Input

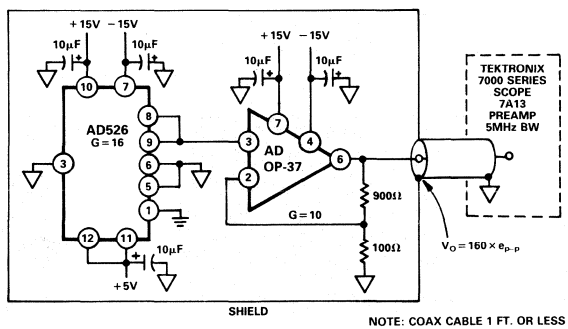


Figure 30. Wideband Noise Test Circuit

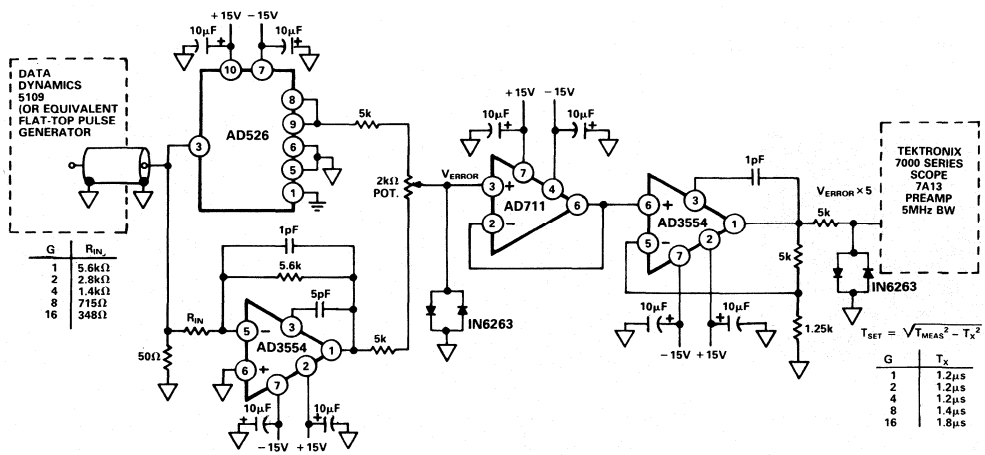


Figure 31. Settling Time Test Circuit

THEORY OF OPERATION

The AD526 is a complete software programmable gain amplifier (SPGA) implemented monolithically with a drift-trimmed BiFET amplifier, a laser wafer trimmed resistor network, JFET analog switches and TTL compatible gain code latches.

A particular gain is selected by applying the appropriate gain code (see Table I) to the control logic. The control logic turns on the JFET switch that connects the correct tap on the gain network to the inverting input of the amplifier; all unselected JFET gain switches are off (open). The "on" resistance of the gain switches causes negligible gain error since only the amplifier's input bias current, which is less than 150pA, actually flows through these switches.

The AD526 is capable of storing the gain code, (latched mode), B, A0, A1, A2, under the direction of control inputs $\overline{CLK}$ and $\overline{CS}$. Alternatively, the AD526 can respond directly to gain code changes if the control inputs are tied low (transparent mode).

For gains of 8 and 16, a fraction of the frequency compensation capacitance (C1 in Figure 32) is automatically switched out of the circuit. This increases the amplifier's bandwidth and improves its signal settling time and slew rate.

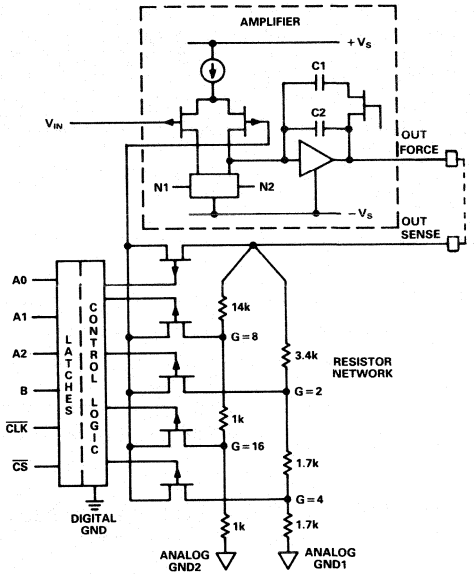


Figure 32. Simplified Schematic of the AD526

4

TRANSPARENT MODE OF OPERATION

In the transparent mode of operation, the AD526 will respond directly to level changes at the gain code inputs (A0, A1, A2) if B is tied high and both $\overline{CS}$ and $\overline{CLK}$ are allowed to float low.

After the gain codes are changed, the AD526's output voltage typically requires 5.5µs to settle to within 0.01% of the final value. Figures 26 to 29 show the performance of the AD526 for positive gain code changes.

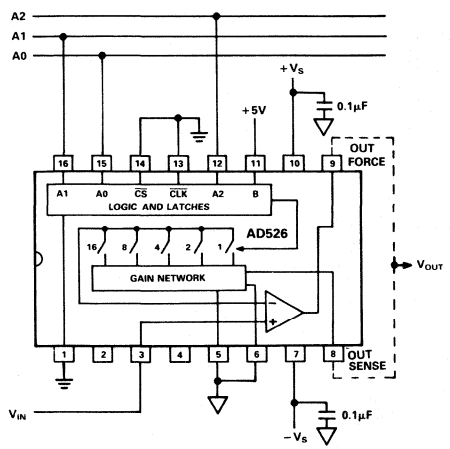


Figure 33. Transparent Mode

LATCHED MODE OF OPERATION

The latched mode of operation is shown in Figure 34. When either $\overline{CS}$ or $\overline{CLK}$ go to a logic "1," the gain code (A0, A1, A2, B) signals are latched into the registers and held until both $\overline{CS}$ and $\overline{CLK}$ return to "0." *Unused $\overline{CS}$ or $\overline{CLK}$ inputs should be tied to ground.* The $\overline{CS}$ and $\overline{CLK}$ inputs are functionally and electrically equivalent.

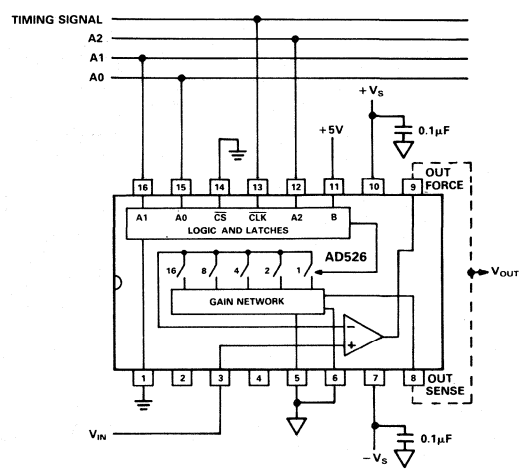


Figure 34. Latched Mode

TIMING AND CONTROL

GAIN CODE				CONTROL	CONDITION	
A2	A1	A0	B	$\overline{CLK}$ ($\overline{CS}$ = 0)	Gain	Condition
X	X	X	X	1	Previous State	Latched
0	0	0	1	0	1	Transparent
0	0	1	1	0	2	Transparent
0	1	0	1	0	4	Transparent
0	1	1	1	0	8	Transparent
1	X	X	1	0	16	Transparent
X	X	X	0	0	1	Transparent
X	X	X	0	1	1	Latched
0	0	0	1	1	1	Latched
0	0	1	1	1	2	Latched
0	1	0	1	1	4	Latched
0	1	1	1	1	8	Latched
1	X	X	1	1	16	Latched

NOTE: X = Don't Care

Table I. AD526 Logic Input Truth Table

The specifications on page 3 in combination with Figure 35 give the timing requirements for loading new gain codes.

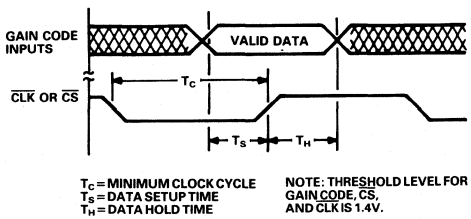


Figure 35. AD526 Timing

DIGITAL FEEDTHROUGH

With either $\overline{CS}$ or $\overline{CLK}$ or both held high, the AD526 gain state will remain constant regardless of the transitions at the A0, A1, A2 or B inputs. However, high-speed logic transitions will unavoidably feed through to the analog circuitry within the AD526 causing spikes to occur at the signal output.

This feedthrough effect can be completely eliminated by operating the AD526 in the transparent mode and latching the gain code in an external bank of latches (Figure 36).

To operate the AD526 using serial inputs, the configuration shown in Figure 36 can be used with the 74LS174 replaced by a serial-in/parallel-out latch, such as the 54LS594.

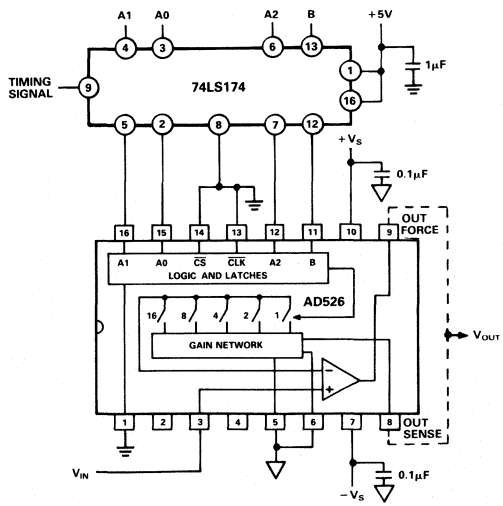


Figure 36. Using an External Latch to Minimize Digital Feedthrough

GROUNDING AND BYPASSING

Proper signal and grounding techniques must be applied in board layout so that specified performance levels of precision data acquisition components, such as the AD526, are not degraded.

As is shown in Figure 37, logic and signal grounds should be separate. By connecting the signal source ground locally to the AD526 analog ground Pins 5 and 6, gain accuracy of the AD526 is maintained. This ground connection should not be corrupted by currents associated with other elements within the system.

Utilizing the force and sense outputs of the AD526, as shown in Figure 38, avoids signal drops along etch runs to low impedance loads.

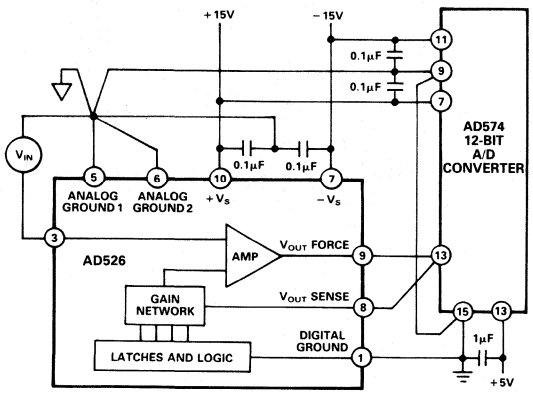


Figure 37. Grounding and Bypassing

CASCADED OPERATION

A cascade of two AD526s can be used to achieve binarily weighted gains from 1 to 256. If gains from 1 to 128 are needed, no additional components are required. This is accomplished by using the B pin as shown in Figure 38. When the B pin is low, the AD526 is held in a unity gain stage independent of the other gain code values.

V_{OUT}/V_{IN}	A2	A1	A0
1	0	0	0
2	0	0	1
4	0	1	0
8	0	1	1
16	1	0	0
32	1	0	1
64	1	1	0
128	1	1	1

Table II. Logic Table for Figure 38

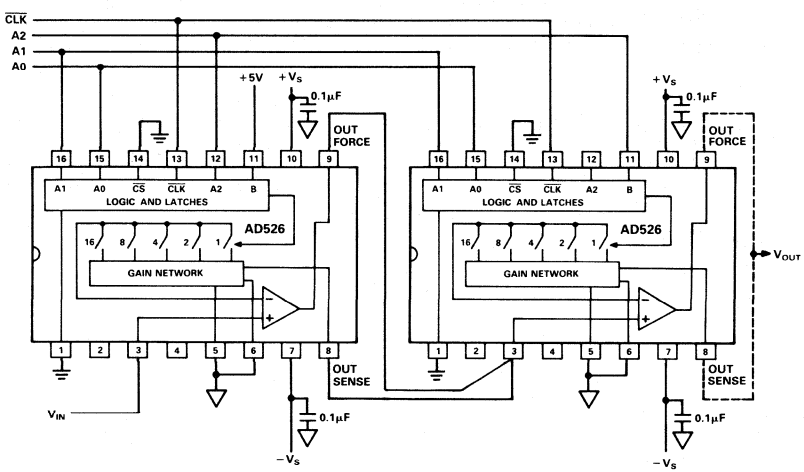


Figure 38. Cascaded Operation

OFFSET NULLING

Input voltage offset nulling of the AD526 is best accomplished at a gain of 16, since the referred-to-input (RTI) offset is amplified the most at this gain and therefore is most easily trimmed. The resulting trimmed value of RTI voltage offset typically varies less than 3μV across all gain ranges.

Note that the low input current of the AD526 minimizes RTI voltage offsets due to source resistance.

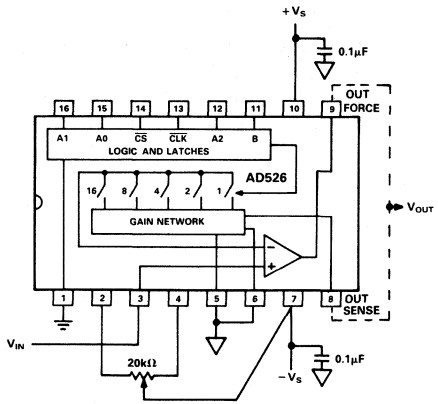


Figure 39. Offset Voltage Null Circuit

OUTPUT CURRENT BOOSTER

The AD526 is rated for a full ±10V output voltage swing into 2kΩ. In some applications, the need exists to drive more current into heavier loads. As shown in Figure 40, a high current booster may be connected "inside the loop" of the SPGA to provide the required current boost without significantly degrading overall performance. Nonlinearities, offset and gain inaccuracies of the buffer are minimized by the loop gain of the AD526 output amplifier.

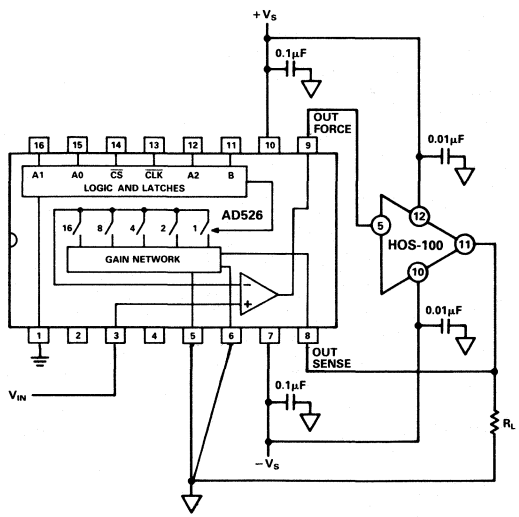


Figure 40. Current Output Boosting

OFFSET NULLING WITH A D/A CONVERTER

Figure 41 shows the AD526 with offset nulling accomplished with an 8-bit D/A converter (AD7524) circuit instead of the potentiometer shown in Figure 39. The calibration procedure is the same as before except that instead of adjusting the potentiometer, the D/A converter corrects for the offset error. This calibration circuit has a number of benefits in addition to eliminating the trimpot. The most significant benefit is that calibration can be under the control of a microprocessor and therefore can be implemented as part of an autocalibration scheme. Secondly, dipswitches or RAM can be used to hold the 8-bit word after its value has been determined. In Figure 42 the offset null sensitivity, at a gain of 16, is 80μV per LSB of adjustment, which guarantees dc accuracy to the 16-bit performance level.

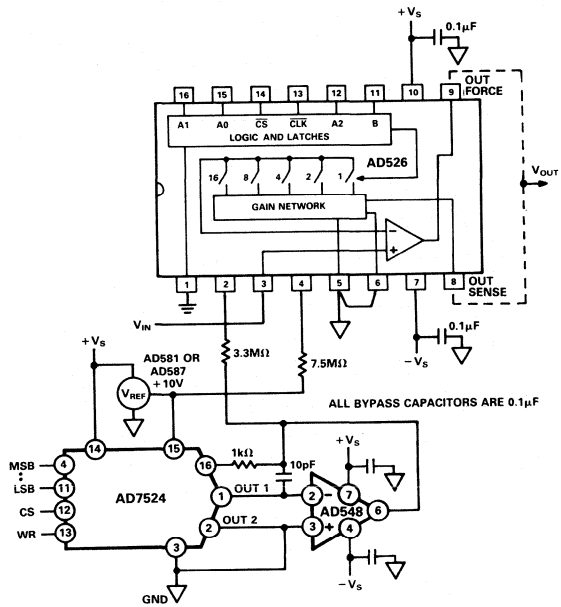


Figure 41. Offset Nulling Using a DAC

FLOATING-POINT CONVERSION

High resolution converters are used in systems to obtain high accuracy, improve system resolution or increase dynamic range. There are a number of high resolution converters available with throughput rates of 66.6kHz that can be purchased as a single component solution; however in order to achieve higher throughput rates, alternative conversion techniques must be employed. A floating point A/D converter can improve both throughput rate and dynamic range of a system.

In a floating point A/D converter (Figure 42), the output data is presented as a 16-bit word, the lower 12 bits from the A/D converter form the mantissa and the upper 4 bits from the digital signal used to set the gain form the exponent. The AD526 programmable gain amplifier in conjunction with the comparator circuit scales the input signal to a range between half scale and full scale for the maximum usable resolution.

The A/D converter diagrammed in Figure 42 consists of a pair of AD585 sample/hold amplifiers, a flash converter, a five-range programmable gain amplifier (the AD526) and a fast 12-bit A/D converter (the AD7572). The floating-point A/D converter achieves its high throughput rate of 125kHz by overlapping the acquisition time of the first sample/hold amplifier and the settling time of the AD526 with the conversion time of the A/D converter. The first sample/hold amplifier holds the signal for the flash autoranger, which determines which binary quantum the input falls within, relative to full scale. Once the AD526 has settled to the appropriate level, then the second sample/hold amplifier can be put into hold which holds the amplified signal while the AD7572 performs its conversion routine. The acquisition time for the AD585 is 3μs, and the conversion time for the AD7572 is 5μs for a total of 8μs, or 125kHz. This performance relies on the fast settling characteristics of the AD526 after the flash autoranging (comparator) circuit quantizes the input signal. A 16-bit register holds the 3-bit output from the flash autoranger and the 12-bit output of the AD7572.

The A/D converter in Figure 42 has a dynamic range of 96dB. The dynamic range of a converter is the ratio of the full-scale input range to the LSB value. With a floating-point A/D converter the smallest value LSB corresponds to the LSB of the monolithic converter divided by the maximum gain of the PGA. The floating point A/D converter has a full-scale range of 5V, a maximum gain of 16V/V from the AD526 and a 12-bit A/D converter; this produces:

LSB = ([FSR/2^N]/Gain) = ([5V/4096]/16) = 76μV. The dynamic range in dBs is based on the log of the ratio of the full-scale input range to the LSB; dynamic range = 20log(5V/76μV) = 96dB.

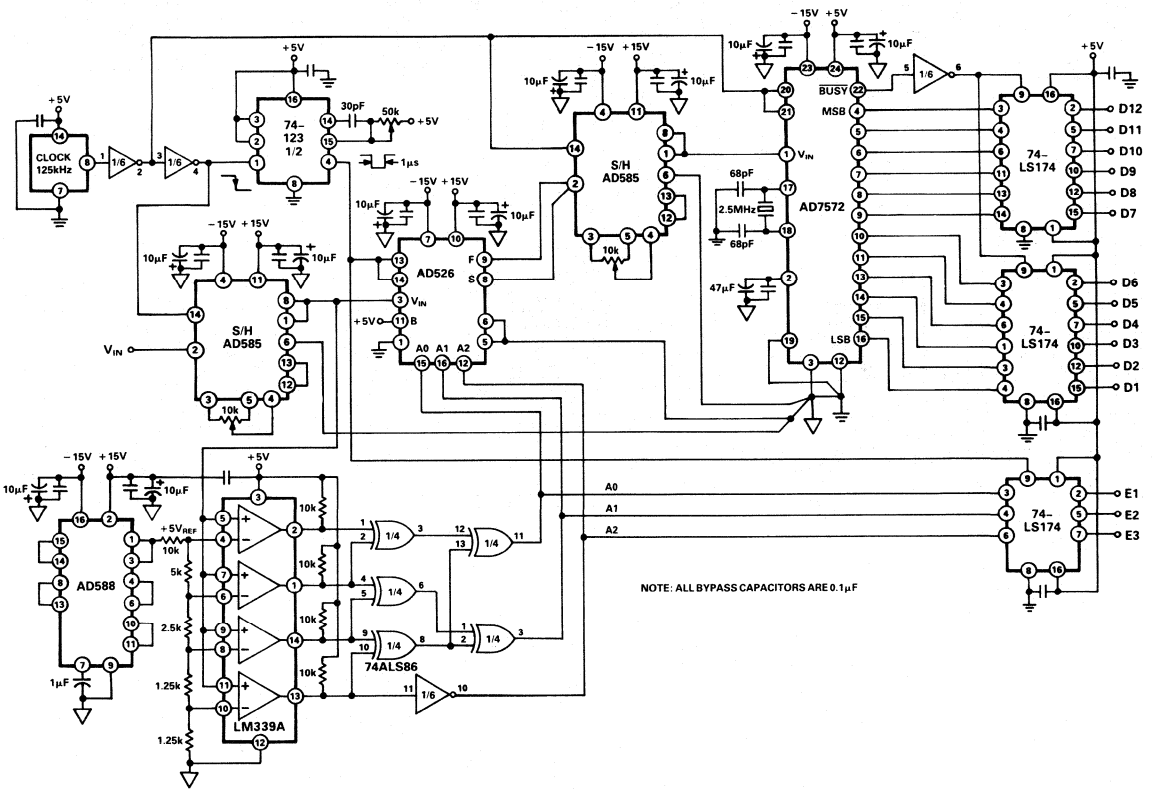


Figure 42. Floating-Point A/D Converter

HIGH ACCURACY A/D CONVERTERS

Very high accuracy and high resolution floating-point A/D converters can be achieved by the incorporation of offset and gain calibration routines. There are two techniques commonly used for calibration, a hardware circuit as shown in Figure 43 and/or a software routine. In this application the microprocessor is functioning as the autoranging circuit, requiring software overhead; therefore, a hardware calibration technique was applied which reduces the software burden. The software is used to set the gain of the AD526. In operation the signal is converted, and if the MSB of the AD574 is not equal to a logical 1, the gain is increased by binary steps, up to the maximum gain. This maximizes the full-scale range of the conversion process and insures a wide dynamic range.

The calibration technique uses two point correction, offset and gain. The hardware is simplified by the use of programmable magnitude comparators, the 74ALS528s, which can be "burned" for a particular code. In order to prevent under or over range hunting during the calibration process, the reference offset and gain codes should be different from the endpoint codes. A calibration cycle consists of selecting whether gain or offset is to be calibrated then selecting the appropriate multiplexer channel to apply the reference voltage to the signal channel. Once the operation has been initiated, the counter, a 74ALS869, drives the D/A converter in a linear fashion providing a small correction voltage to either the gain or offset trim point of the AD574. The output of the A/D converter is then compared to the value preset in the 74ALS528 to determine a match. Once a match is detected, the 74ALS528 produces a low going pulse which stops the counter. The code at the D/A converter is latched until the next calibration cycle. Calibration cycles are under the control of the microprocessor in this application and should be implemented only during periods of converter inactivity.

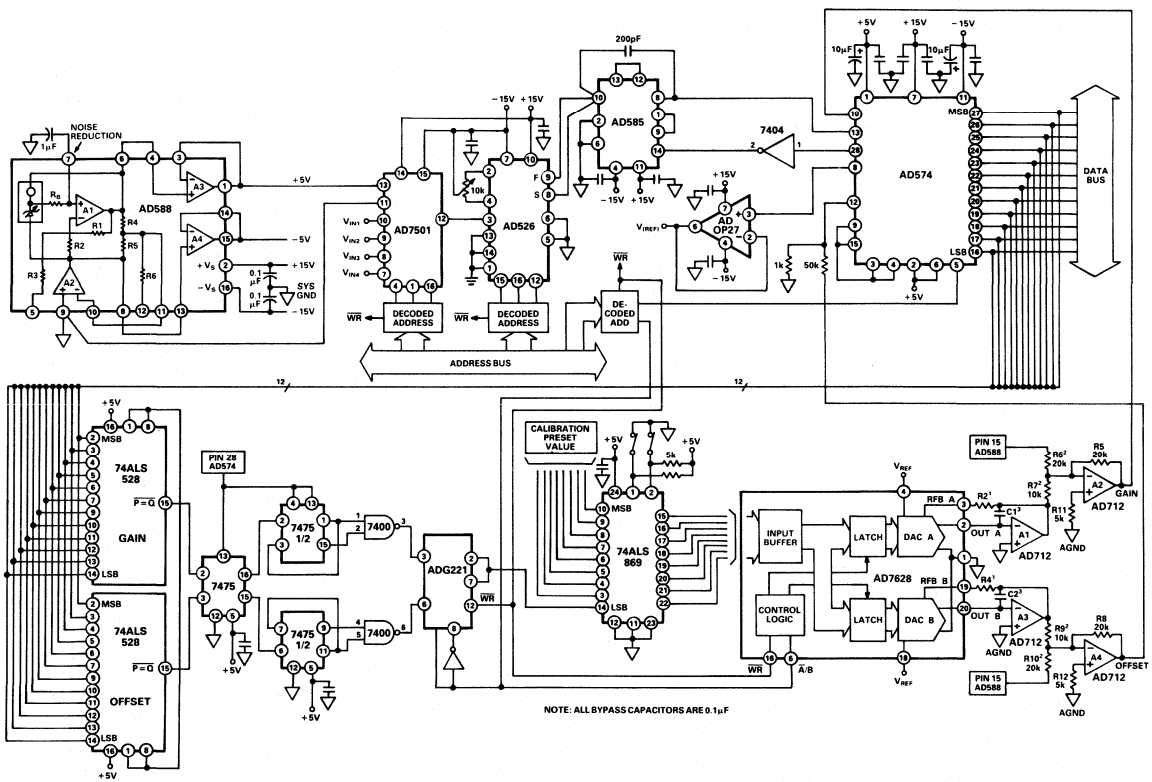


Figure 43. High Accuracy A/D Converter

ANALOG DEVICES

Low Cost, Low Power Instrumentation Amplifier

AD620

FEATURES
EASY TO USE
Gain Set with One External Resistor
(Gain Range 1 to 1000)
Wide Power Supply Range (±2.3 V to ±18 V)
Higher Performance than Three Op Amp IA Designs
Available in 8-Pin DIP and SOIC Packaging
Low Power, 1.3 mA max Supply Current

EXCELLENT DC PERFORMANCE ("A GRADE")
125 μV max, Input Offset Voltage (50 μV max "B" Grade)
1 μV/°C max, Input Offset Drift
2.0 nA max, Input Bias Current
93 dB min Common-Mode Rejection Ratio (G = 10)

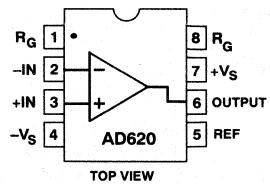
LOW NOISE
9 nV/√Hz, @ 1 kHz, Input Voltage Noise
0.28 μV p–p Noise (0.1 Hz to 10 Hz)

EXCELLENT AC SPECIFICATIONS
120 kHz Bandwidth (G = 100)
15 μs Settling Time to 0.01%

APPLICATIONS
Weigh Scales
ECG and Medical Instrumentation
Transducer Interface
Data Acquisition Systems
Industrial Process Controls
Battery Powered and Portable Equipment

CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP (N), Cerdip (Q) and SOIC (R) Packages



TOP VIEW

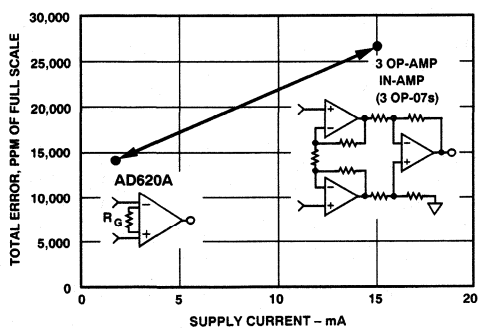
4

PRODUCT DESCRIPTION

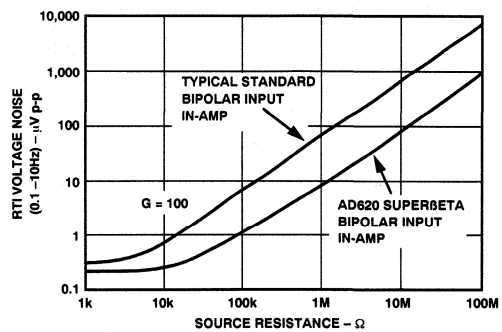
The AD620 is a low cost, high accuracy instrumentation amplifier which requires only one external resistor to set gains of 1 to 1000. Furthermore, the AD620 features 8-pin SOIC and DIP packaging that is smaller than discrete designs, and offers lower power (only 1.3 mA max supply current), making it a good fit for battery powered, portable (or remote) applications.

The AD620, with its high accuracy of 40 ppm maximum nonlinearity, low offset voltage of 50 μV max and offset drift of 0.6 μV/°C max, is ideal for use in precision data acquisition systems, such as weigh scales and transducer interfaces. Furthermore, the low noise, low input bias current, and low power of the AD620 make it well suited for medical applications such as ECG and noninvasive blood pressure monitors.

The low input bias current of 1.0 nA max is made possible with the use of Superβeta processing in the input stage. The AD620 works well as a preamplifier due to its low input voltage noise of 9 nV/√Hz at 1 kHz, 0.28 μV p–p in the 0.1 Hz to 10 Hz band, 0.1 pA/√Hz input current noise. Also, the AD620 is well suited for multiplexed applications with its settling time of 15 μs to 0.01% and its cost is low enough to enable designs with one in amp per channel.



Three Op Amp IA Designs vs. AD620



Total Voltage Noise vs. Source Resistance

AD620—SPECIFICATIONS (typical @ +25°C, V_S = ±15 V, and R_L = 2 kΩ unless otherwise noted)

Model	Conditions	AD620A Min	AD620A Typ	AD620A Max	AD620B Min	AD620B Typ	AD620B Max	AD620S[4] Min	AD620S[4] Typ	AD620S[4] Max	Units
GAIN	G = 1 + (49.4 k/R_G)										
Gain Range		1		10,000	1		10,000	1		10,000	
Gain Error[1]	V_{OUT} = ±10 V										
G = 1			0.03	0.10		0.01	0.02		0.03	0.10	%
G = 10			0.15	0.30		0.10	0.15		0.15	0.30	%
G = 100			0.15	0.30		0.10	0.15		0.15	0.30	%
G = 1000			0.40	0.70		0.35	0.50		0.40	0.70	%
Nonlinearity,	V_{OUT} = −10 V to +10 V,										
G = 1–1000	R_L = 10 kΩ		10	40		10	40		10	40	ppm
G = 1–100	R_L = 2 kΩ		10	95		10	95		10	95	ppm
Gain vs. Temperature	Gain <1000[1]			−50			−50			−50	ppm/°C
VOLTAGE OFFSET	(Total RTI Error = V_{OSI} + V_{OSO}/G)										
Input Offset, V_{OSI}	V_S = ±5 V to ±15 V		30	125		15	50		30	125	µV
over Temperature	V_S = ±5 V to ±15 V			185			85			225	µV
Average TC	V_S = ±5 V to ±15 V		0.3	1.0		0.1	0.6		0.3	1.0	µV/°C
Output Offset, V_{OSO}	V_S = ±15 V		400	1000		200	500		400	1000	µV
	V_S = ±5 V			1500			750			1500	µV
over Temperature	V_S = ±5 V to ±15 V			2000			1000			2000	µV
Average TC	V_S = ±5 V to ±15 V		5.0	15		2.5	7.0		5.0	15	µV/°C
Offset Referred to the Input vs. Supply (PSR)	V_S = ±2.3 V to ±18 V										
G = 1		80	100		80	100		80	100		dB
G = 10		95	120		100	120		95	120		dB
G = 100		110	140		120	140		110	140		dB
G = 1000		110	140		120	140		110	140		dB
INPUT CURRENT											
Input Bias Current			0.5	2.0		0.5	1.0		0.5	2	nA
over Temperature				2.5			1.5			4	nA
Average TC			3.0			3.0			8.0		pA/°C
Input Offset Current			0.3	1.0		0.3	0.5		0.3	1.0	nA
over Temperature				1.5			0.75			2.0	nA
Average TC			1.5			1.5			8.0		pA/°C
INPUT											
Input Impedance											
Differential			10||2			10||2			10||2			GΩ||pF
Common-Mode			10||2			10||2			10||2			GΩ||pF
Input Voltage Range[2]	V_S = ±2.3 V to ±5 V	$-V_S$ + 1.9		$+V_S$ − 1.2	$-V_S$ + 1.9		$+V_S$ − 1.2	$-V_S$ + 1.9		$+V_S$ − 1.2	V
over Temperature		$-V_S$ + 2.1		$+V_S$ − 1.3	$-V_S$ + 2.1		$+V_S$ − 1.3	$-V_S$ + 2.1		$+V_S$ − 1.3	V
	V_S = ±5 V to ±18 V	$-V_S$ + 1.9		$+V_S$ − 1.4	$-V_S$ + 1.9		$+V_S$ − 1.4	$-V_S$ + 1.9		$+V_S$ − 1.4	V
over Temperature		$-V_S$ + 2.1		$+V_S$ − 1.4	$-V_S$ + 2.1		$+V_S$ − 1.4	$-V_S$ + 2.3		$+V_S$ − 1.4	V
Common-Mode Rejection Ratio DC to 60 Hz with 1 kΩ Source Imbalance	V_{CM} = 0 V to ±10 V										
G = 1		73	90		80	90		73	90		dB
G = 10		93	110		100	110		93	110		dB
G = 100		110	130		120	130		110	130		dB
G = 1000		110	130		120	130		110	130		dB
OUTPUT											
Output Swing	R_L = 10 kΩ,										
	V_S = ±2.3 V to ±5 V	$-V_S$ + 1.1		$+V_S$ − 1.2	$-V_S$ + 1.1		$+V_S$ − 1.2	$-V_S$ + 1.1		$+V_S$ − 1.2	V
over Temperature		$-V_S$ + 1.4		$+V_S$ − 1.3	$-V_S$ + 1.4		$+V_S$ − 1.3	$-V_S$ + 1.6		$+V_S$ − 1.3	V
	V_S = ±5 V to ±18 V	$-V_S$ + 1.2		$+V_S$ − 1.4	$-V_S$ + 1.2		$+V_S$ − 1.4	$-V_S$ + 1.2		$+V_S$ − 1.4	V
over Temperature		$-V_S$ + 1.6		$+V_S$ − 1.5	$-V_S$ + 1.6		$+V_S$ − 1.5	$-V_S$ + 2.3		$+V_S$ − 1.5	V
Short Current Circuit			±18			±18			±18		mA

Model	Conditions	AD620A Min	AD620A Typ	AD620A Max	AD620B Min	AD620B Typ	AD620B Max	AD620S[4] Min	AD620S[4] Typ	AD620S[4] Max	Units
DYNAMIC RESPONSE											
Small Signal −3 dB Bandwidth											
G = 1			1000			1000			1000		kHz
G = 10			800			800			800		kHz
G = 100			120			120			120		kHz
G = 1000			12			12			12		kHz
Slew Rate		0.75	1.2		0.75	1.2		0.75	1.2		V/μs
Settling Time to 0.01%	10 V Step										
G = 1–100			15			15			15		μs
G = 1000			150			150			150		μs
NOISE											
Voltage Noise, 1 kHz	Total RTI Noise = $\sqrt{(e_{ni}^2) + (e_{no}/G)^2}$										
Input, Voltage Noise, e_{ni}			9	13		9	13		9	13	nV/$\sqrt{\text{Hz}}$
Output, Voltage Noise, e_{no}			72	100		72	100		72	100	nV/$\sqrt{\text{Hz}}$
RTI, 0.1 Hz to 10 Hz											
G = 1			3.0			3.0	6.0		3.0	6.0	μV p–p
G = 10			0.55			0.55	0.8		0.55	0.8	μV p–p
G = 100–1000			0.28			0.28	0.4		0.28	0.4	μV p–p
Current Noise	f = 1 kHz		100			100			100		fA/$\sqrt{\text{Hz}}$
0.1 Hz to 10 Hz			10			10			10		pA p–p
REFERENCE INPUT											
R_{IN}			20			20			20		kΩ
I_{IN}	V_{IN+}, V_{REF} = 0		+50	+60		+50	+60		+50	+60	μA
Voltage Range		$-V_S$ + 1.6		$+V_S$ − 1.6	$-V_S$ + 1.6		$+V_S$ − 1.6	$-V_S$ + 1.6		$+V_S$ − 1.6	V
Gain to Output			1 ± 0.0001			1 ± 0.0001			1 ± 0.0001		
POWER SUPPLY											
Operating Range[3]		±2.3		±18	±2.3		±18	±2.3		±18	V
Quiescent Current	V_S = ±2.3 V to ±18 V		0.9	1.3		0.9	1.3		0.9	1.3	mA
over Temperature			1.1	1.6		1.1	1.6		1.1	1.6	mA
TEMPERATURE RANGE											
for Specified Performance			−40 to +85			−40 to +85			−55 to +125		°C

NOTES
[1]Does not include effects of external resistor R_G.
[2]One input grounded. G = 1.
[3]This is defined as the same supply range which is used to specify PSR.
[4]See Analog Devices military data sheet for 883B tested specifications.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2] . . . . . 650 mW
Input Voltage (Common Mode) . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±25 V
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range (Q) . . . . . −65°C to +150°C
Storage Temperature Range (N, R) . . . . . −65°C to +125°C
Operating Temperature Range
AD620 (A, B) . . . . . −40°C to +85°C
AD620 (S) . . . . . −55°C to +125°C
Lead Temperature Range
(Soldering 10 seconds) . . . . . 300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air:
8-Pin Plastic Package: θ_{JA} = 95°C/Watt
8-Pin Cerdip Package: θ_{JA} = 110°C/Watt
8-Pin SOIC Package: θ_{JA} = 155°C/Watt

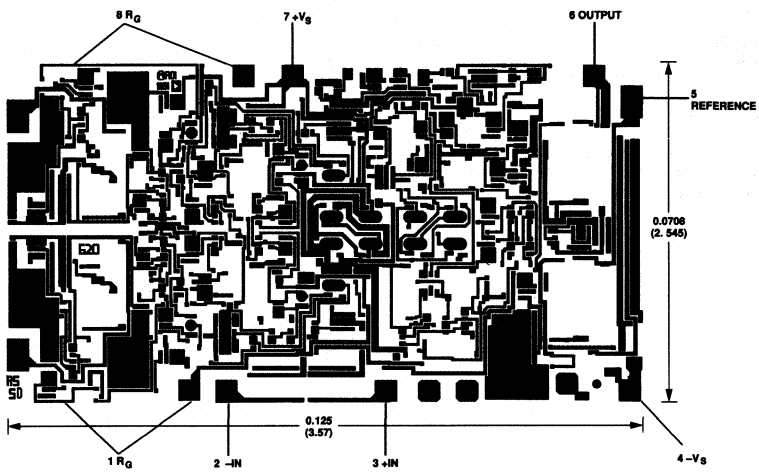
ORDERING GUIDE

Model	Temperature Range	Package Option*
AD620AN	−40°C to +85°C	N-8
AD620BN	−40°C to +85°C	N-8
AD620AR	−40°C to +85°C	R-8
AD620BR	−40°C to +85°C	R-8
AD620A Chips	−40°C to +85°C	Die Form
AD620SQ/883B	−55°C to +125°C	Q-8

*N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.

METALIZATION PHOTOGRAPHY

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



TYPICAL CHARACTERISTICS (@ +25°C, V_S = ±15 V, R_L = 2 kΩ, unless otherwise noted)

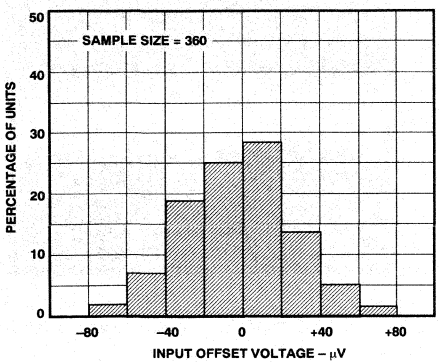


Figure 1. Typical Distribution of Input Offset Voltage

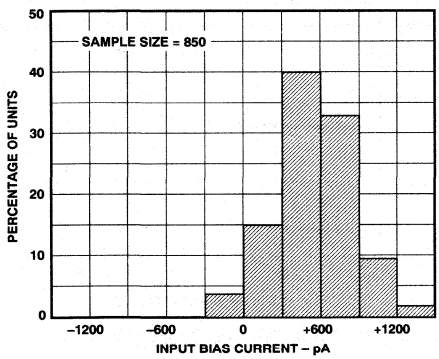


Figure 2. Typical Distribution of Input Bias Current

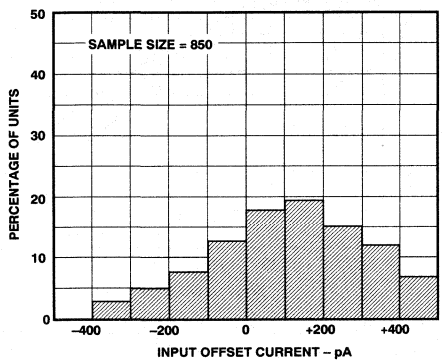


Figure 3. Typical Distribution of Input Offset Current

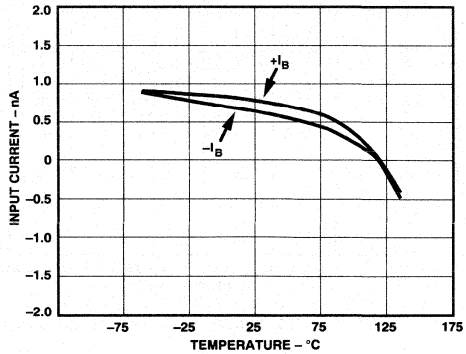


Figure 4. Input Bias Current vs. Temperature

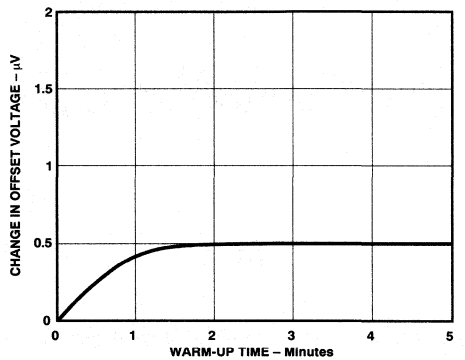


Figure 5. Change in Input Offset Voltage vs. Warm-Up Time

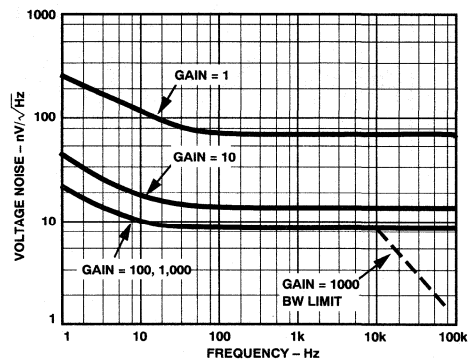


Figure 6. Voltage Noise Spectral Density vs. Frequency, (G = 1–1000)

AD620—Typical Characteristics

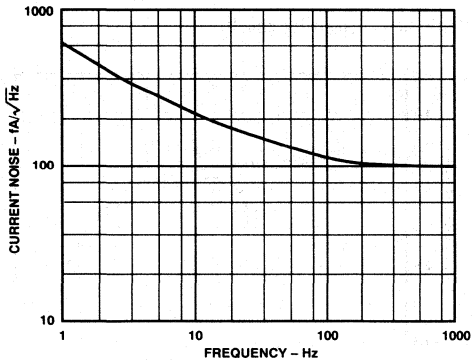


Figure 7. Current Noise Spectral Density vs. Frequency

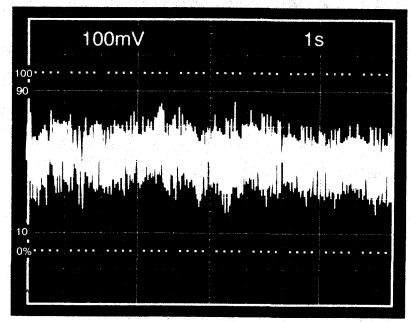


Figure 9. 0.1 Hz to 10 Hz Current Noise, 5 pA/Div

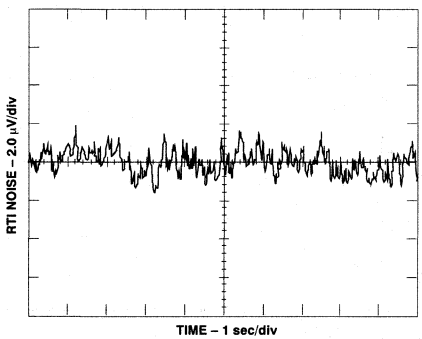


Figure 8a. 0.1 Hz to 10 Hz RTI Voltage Noise (G = 1)

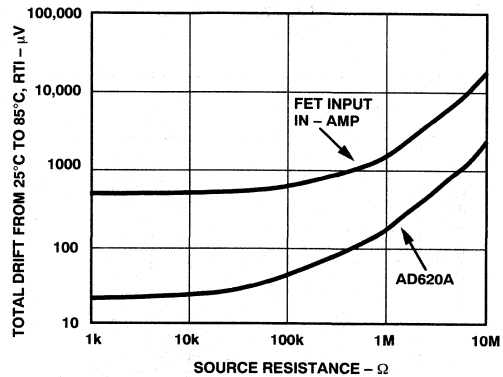


Figure 10. Total Drift vs. Source Resistance

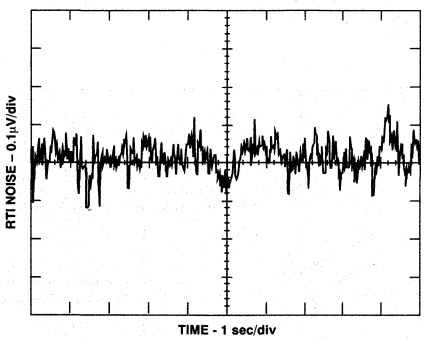


Figure 8b. 0.1 Hz to 10 Hz RTI Voltage Noise (G = 1000)

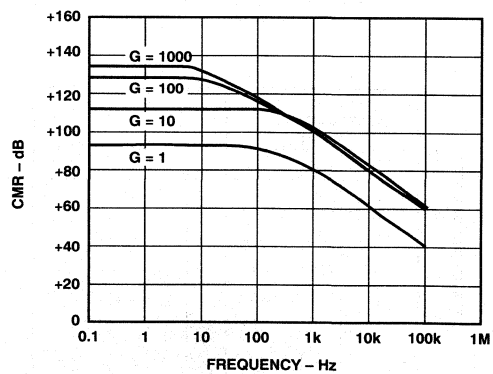


Figure 11. CMR vs. Frequency, RTI, Zero to 1 kΩ Source Imbalance

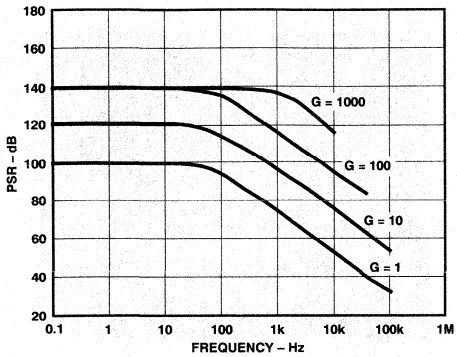


Figure 12. Positive PSR vs. Frequency, RTI (G = 1–1000)

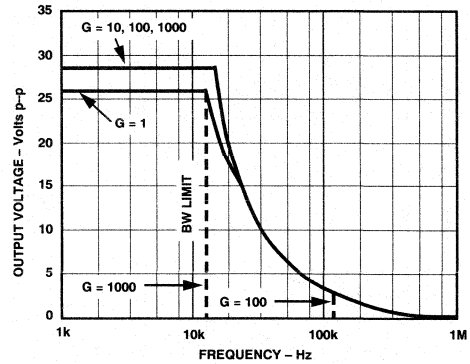


Figure 15. Large Signal Frequency Response

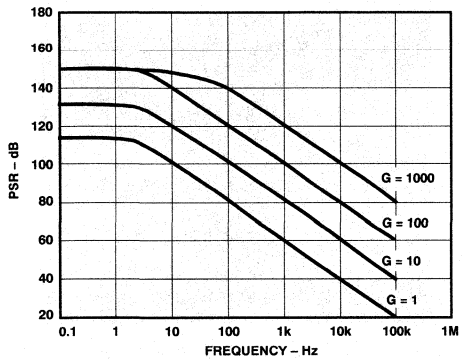


Figure 13. Negative PSR vs. Frequency, RTI (G = 1–1000)

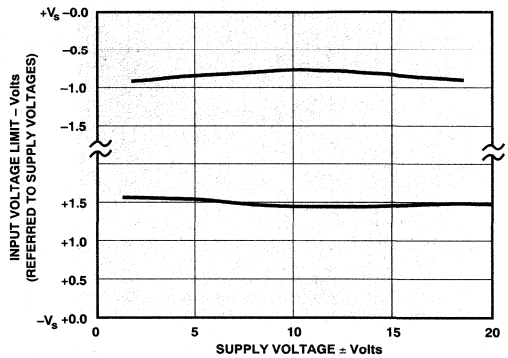


Figure 16. Input Voltage Range vs. Supply Voltage, G = 1

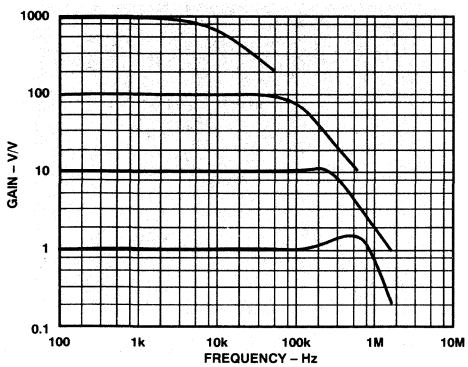


Figure 14. Gain vs. Frequency

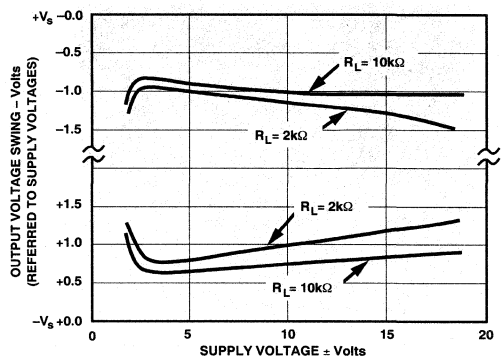


Figure 17. Output Voltage Swing vs. Supply Voltage, G = 10

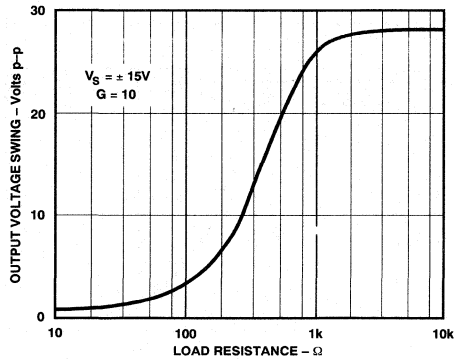


Figure 18. Output Voltage Swing vs. Load Resistance

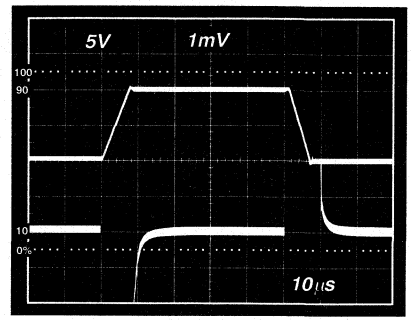


Figure 21. Large Signal Pulse Response and Settling Time, G = 10 (0.5 mV = 0.01%)

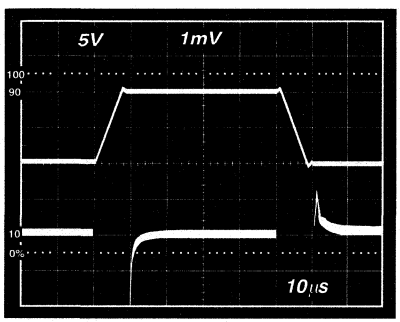


Figure 19. Large Signal Pulse Response and Settling Time G = 1 (0.5 mV = 0.01%)

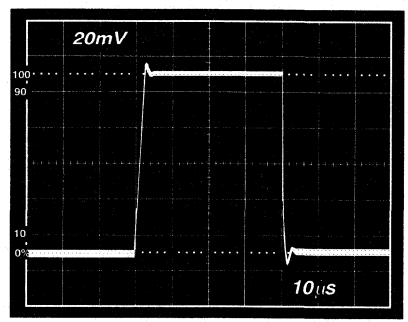


Figure 22. Small Signal Pulse Response, G = 10, R_L =2 kΩ, C_L = 100 pF

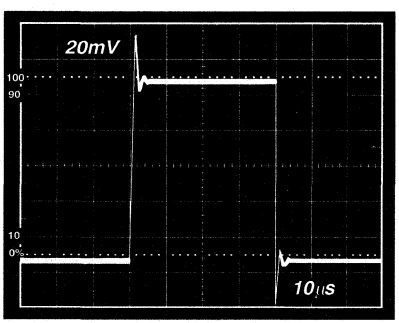


Figure 20. Small Signal Pulse Response, G = 1, R_L = 2 kΩ, C_L = 100 pF

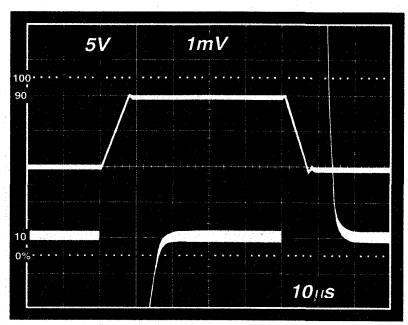


Figure 23. Large Signal Pulse Response and Settling Time, G = 100 (0.5 mV = 0.01%)

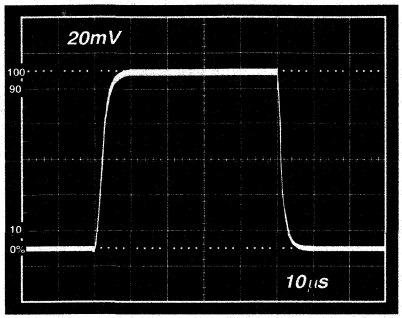


Figure 24. Small Signal Pulse Response, G = 100, R_L = 2 kΩ, C_L = 100 pF

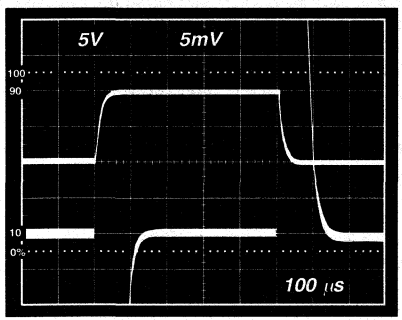


Figure 25. Large Signal Pulse Response and Settling Time, G = 1000 (0.5 mV = 0.01%)

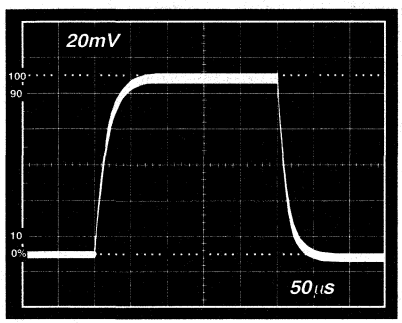


Figure 26. Small Signal Pulse Response, G = 1000, R_L = 2 kΩ, C_L = 100 pF

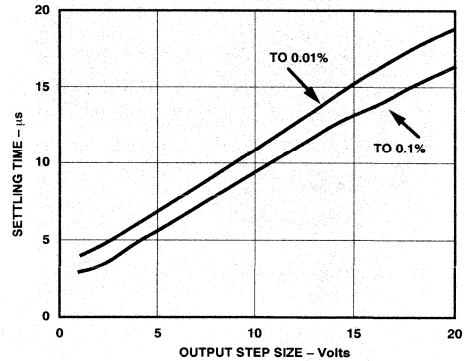


Figure 27. Settling Time vs. Step Size, (G = 1)

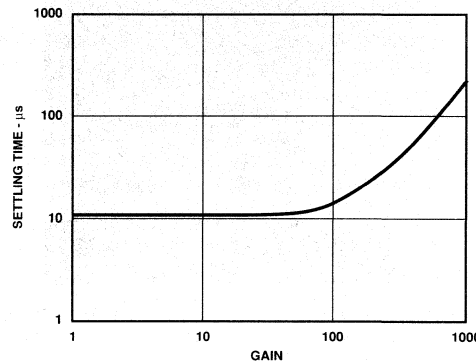


Figure 28. Settling Time to 0.01% vs. Gain, for a 10 V Step

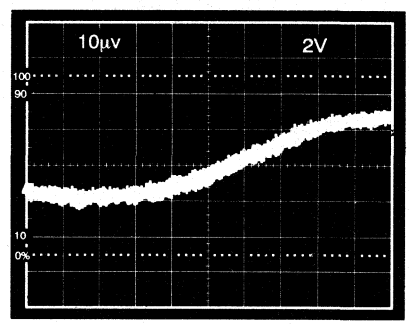


Figure 29a. Gain Nonlinearity, G = 1, R_L = 10 kΩ (10 μV = 1 ppm)

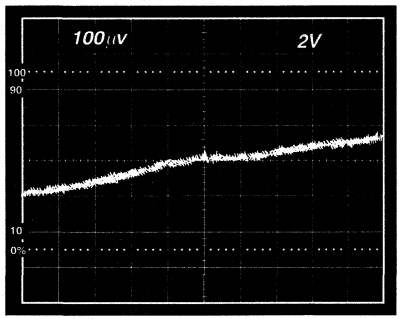


Figure 29b. Gain Nonlinearity, G = 100, R_L = 10 kΩ (100 μV = 10 ppm)

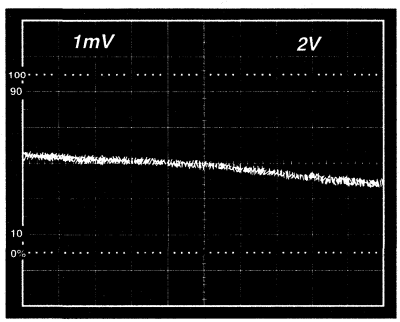


Figure 29c. Gain Nonlinearity, G = 1000, R_L = 10 kΩ (1 mV = 100 ppm)

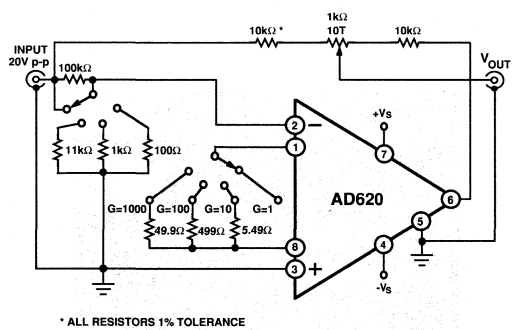


Figure 30. Settling Time Test Circuit

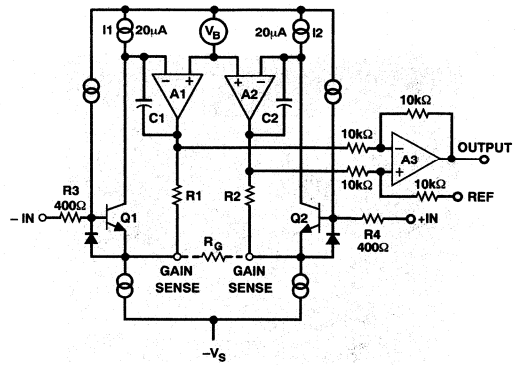


Figure 31. Simplified Schematic of AD620

THEORY OF OPERATION

The AD620 is a monolithic instrumentation amplifier based on a modification of the classic three op amp approach. Absolute-value trimming allows the user to program gain *accurately* (to 0.15% at G = 100) with only one resistor. Monolithic construction and laser wafer trimming allow the tight matching and tracking of circuit components, thus insuring the high level of performance inherent in this circuit.

The input transistors Q1 and Q2 provide a single differential-pair bipolar input for high precision (Figure 31), yet offer 10× lower Input Bias Current thanks to Superβeta processing. Feedback through the Q1-A1-R1 loop and the Q2-A2-R2 loop maintains constant collector current of the input devices Q1, Q2 thereby impressing the input voltage across the external gain-setting resistor R_G. This creates a differential gain from the inputs to the A1/A2 outputs given by G = (R1 + R2)/R_G + 1. The unity-gain subtractor A3 removes any common-mode signal, yielding a single-ended output referred to the REF pin potential.

The value of R_G also determines the transconductance of the preamp stage. As R_G is reduced for larger gains, the transconductance increases asymptotically to that of the input transistors. This has three important advantages: (a) Open-loop gain is boosted for increasing programmed gain, thus reducing gain-related errors. (b) The gain-bandwidth product (determined by C1, C2 and the preamp transconductance) increases with programmed gain, thus optimizing frequency response. (c) The input voltage noise is reduced to a value of 9 nV/$\sqrt{\text{Hz}}$, determined mainly by the collector current and base resistance of the input devices.

The internal gain resistors, R1 and R2, are trimmed to an absolute value of 24.7 kΩ, allowing the gain to be programmed accurately with a single external resistor.

The gain equation is then

$$G = \frac{49.4\ k\Omega}{R_G} + 1$$

so that

$$R_G = \frac{49.4\ k\Omega}{G - 1}$$

Make vs. Buy: A Typical Bridge Application Error Budget

The AD620 offers improved performance over "homebrew" three op amp IA designs, along with smaller size, less components and 10× lower supply current. In the typical application, shown in Figure 32, a gain of 100 is required to amplify a bridge output of 20 mV full scale over the industrial temperature range of −40°C to +85°C. The error budget table below shows how to calculate the effect various error sources have on circuit accuracy.

Regardless of the system it is being used in, the AD620 provides greater accuracy, and at low power and price. In simple systems, absolute accuracy and drift errors are by far the most significant contributors to error. In more complex systems with an intelligent processor, an auto-gain/auto-zero cycle will remove all absolute accuracy and drift errors leaving only the resolution errors of gain nonlinearity and noise, thus allowing full 14-bit accuracy.

Note that for the homebrew circuit, the OP-07 specifications for input voltage offset and noise have been multiplied by $\sqrt{2}$. This is because a three op amp type in amp has two op amps at its inputs, both contributing to the overall input error.

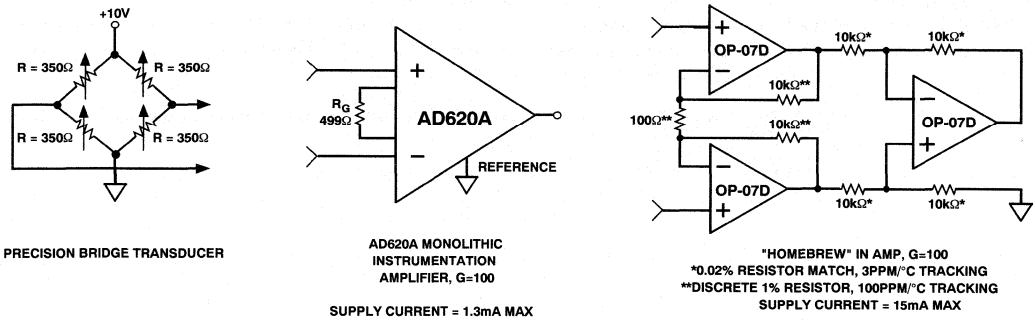


Figure 32. Make vs. Buy

Table I. Make vs. Buy Error Budget

Error Source	AD620 Circuit Calculation	"Homebrew" Circuit Calculation	Error, ppm of Full Scale AD620	Homebrew
ABSOLUTE ACCURACY at T_A = +25°C				
Input Offset Voltage, μV	125 μV/ 20 mV	(150 μV × $\sqrt{2}$)/20 mV	6,250	10,607
Output Offset Voltage, μV	1000 μV/100/20 mV	((150 μV × 2)/100)/20 mV	500	150
Input Offset Current, nA	2 nA × 350 Ω/20 mV	(6 nA × 350 Ω)/20 mV	18	53
CMR, dB	110 dB→3.16 ppm, × 5 V/20 mV	(0.02% Match × 5 V)/20 mV	791	4,988
		Total Absolute Error	7,558	15,797
DRIFT TO +85°C				
Gain Drift, ppm/°C	(50 ppm + 10 ppm) × 60°C	10 ppm/°C Track × 60°C	3,600	600
Input Offset Voltage Drift, μV/°C	1 μV/°C × 60°C/20 mV	(2.5 μV/°C × $\sqrt{2}$ × 60°C)/20 mV	3,000	10,607
Output Offset Voltage Drift, μV/°C	15 μV/°C × 60°C/100/20 mV	(2.5 μV/°C × 2 × 60°C)/100/20 mV	450	150
		Total Drift Error	7,050	11,357
RESOLUTION				
Gain Nonlinearity, ppm of Full Scale	40 ppm	40 ppm	40	40
Typ 0.1 Hz–10 Hz Voltage Noise, μV p–p	0.28 μV p–p/20 mV	(0.38 μV p–p × $\sqrt{2}$)/20 mV	14	27
		Total Resolution Error	54	67
		Grand Total Error	14,662	27,221

G = 100, V_S = ±15 V.
(All errors are min/max and referred to input.)

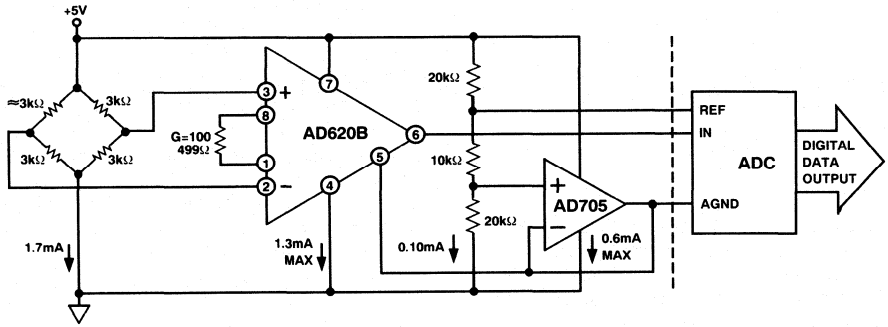


Figure 33. A Pressure Monitor Circuit which Operates on a +5 V Single Supply

Pressure Measurement

Although useful in many bridge applications such as weigh-scales, the AD620 is especially suited for higher resistance pressure sensors powered at lower voltages where small size and low power become more significant.

Figure 33 shows a 3 kΩ pressure transducer bridge powered from +5 V. In such a circuit, the bridge consumes only 1.7 mA. Adding the AD620 and a buffered voltage divider allows the signal to be conditioned for only 3.8 mA of total supply current.

Small size and low cost make the AD620 especially attractive for voltage output pressure transducers. Since it delivers low noise and drift, it will also serve applications such as diagnostic non-invasive blood pressure measurement.

Medical ECG

The low current noise of the AD620 allows its use in ECG monitors (Figure 34) where high source resistances of 1 MΩ or higher are not uncommon. The AD620's low power, low supply voltage requirements, and space-saving 8-pin mini-DIP and SOIC package offerings make it an excellent choice for battery powered data recorders.

Furthermore, the low bias currents and low current noise coupled with the low voltage noise of the AD620 improve the dynamic range for better performance.

The value of capacitor C1 is chosen to maintain stability of the right leg drive loop. Proper safeguards, such as isolation, must be added to this circuit to protect the patient from possible harm.

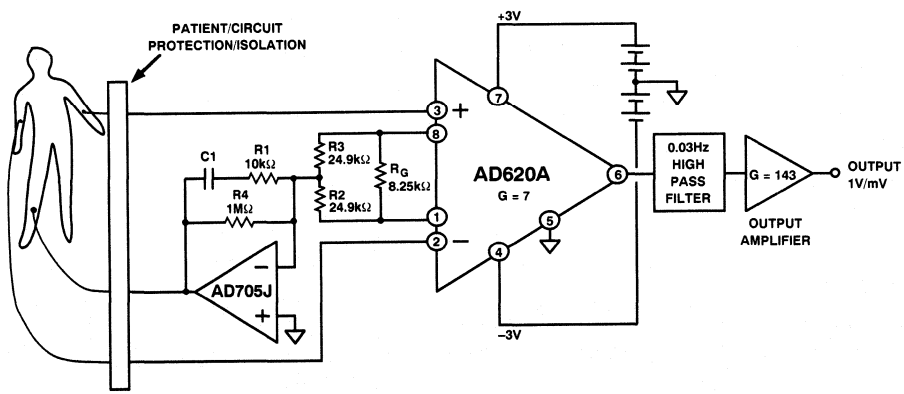


Figure 34. A Medical ECG Monitor Circuit

Precision V-I Converter

The AD620 along with another op amp and two resistors make a precision current source (Figure 35). The op amp buffers the reference terminal to maintain good CMR. The output voltage V_X of the AD620 appears across R1 which converts it to a current. This current less only the input bias current of the op amp then flows out to the load.

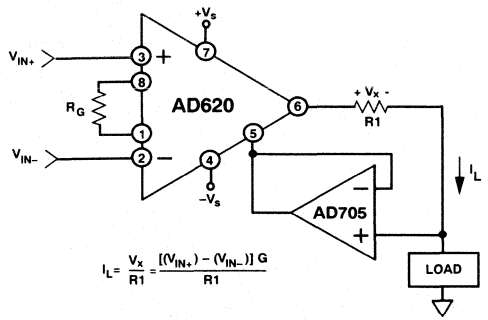


Figure 35. Precision Voltage-to-Current Converter (Operates on 1.8 mA, ±3 V)

GAIN SELECTION

The AD620's gain is resistor programmed by R_G, or more precisely, by whatever impedance appears between Pins 1 and 8. The AD620 is designed to offer accurate gains using 0.1%–1% resistors. Table II shows required values of R_G for various gains. Note that for G = 1, the R_G pins are unconnected ($R_G = \infty$). For any arbitrary gain R_G can be calculated by using the formula

$$R_G = \frac{49.4\ k\Omega}{G - 1}$$

To minimize gain error avoid high parasitic resistance in series with R_G, and to minimize gain drift R_G should have a low TC—less than 10 ppm/°C for the best performance.

Table II. Required Values of Gain Resistors

1% Std Table Value of R_G, Ω	Calculated Gain	0.1% Std Table Value of R_G, Ω	Calculated Gain
49.9 k	1.990	49.3 k	2.002
12.4 k	4.984	12.4 k	4.984
5.49 k	9.998	5.49 k	9.998
2.61 k	19.93	2.61 k	19.93
1.00 k	50.40	1.01 k	49.91
499	100.0	499	100.0
249	199.4	249	199.4
100	495.0	98.8	501.0
49.9	991.0	49.3	1,003

INPUT AND OUTPUT OFFSET VOLTAGE

The low errors of the AD620 are attributed to two sources, input and output errors. The output error is divided by G when referred to the input. In practice, the input errors dominate at high gains and the output errors dominate at low gains. The total V_{OS} for a given gain is calculated as:

Total Error RTI = input error + (output error/G)

Total Error RTO = (input error × G) + output error

REFERENCE TERMINAL

The reference terminal potential defines the zero output voltage, and is especially useful when the load does not share a precise ground with the rest of the system. It provides a direct means of injecting a precise offset to the output, with an allowable range of 2 V within the supply voltages. Parasitic resistance should be kept to a minimum for optimum CMR.

INPUT PROTECTION

The AD620 features 400 Ω of series thin film resistance at its inputs, and will safely withstand input overloads of up to ±15 V or ±60 mA for several hours. This is true for all gains, and power on and off, which is particularly important since the signal source and amplifier may be powered separately. For longer time periods, the current should not exceed 6 mA ($I_{IN} \leq V_{IN}/400\ \Omega$). For input overloads beyond the supplies, clamping the inputs to the supplies (using a low leakage diode such as an FD333) will reduce the required resistance, yielding lower noise.

RF INTERFERENCE

All instrumentation amplifiers can rectify out of band signals, and when amplifying small signals, these rectified voltages act as small dc offset errors. The AD620 allows direct access to the input transistor bases and emitters enabling the user to apply some first order filtering to unwanted RF signals (Figure 36), where RC ≈ 1/(2 πf) and where f is the bandwidth of the AD620. Matching the extraneous capacitance at Pins 1 and 8, and Pins 2 and 3 helps to maintain high CMR.

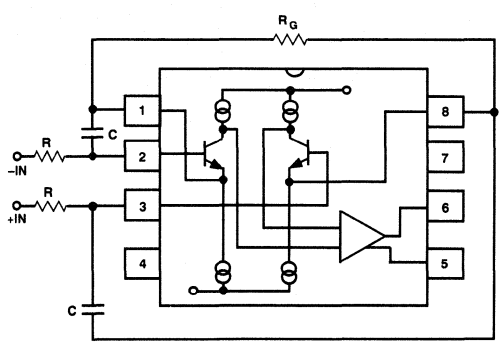


Figure 36. Circuit to Attenuate RF Interference

COMMON-MODE REJECTION

Instrumentation amplifiers like the AD620 offer high CMR which is a measure of the change in output voltage when both inputs are changed by equal amounts. These specifications are usually given for a full-range input voltage change and a specified source imbalance.

For optimal CMR the reference terminal should be tied to a low impedance point, and differences in capacitance and resistance should be kept to a minimum between the two inputs. In many applications shielded cables are used to minimize noise, and for best CMR over frequency the shield should be properly driven. Figures 37 and 38 show active data guards which are configured to improve ac common-mode rejections by "bootstrapping" the capacitances of input cable shields, thus minimizing the capacitance mismatch between the inputs.

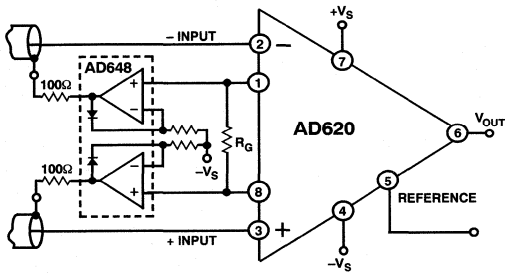


Figure 37. Differential Shield Driver

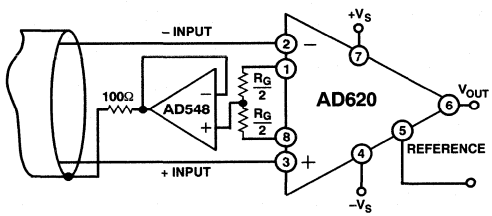


Figure 38. Common-Mode Shield Driver

GROUNDING

Since the AD620 output voltage is developed with respect to the potential on the reference terminal, it can solve many grounding problems by simply tying the REF pin to the appropriate "local ground."

In order to isolate low level analog signals from a noisy digital environment, many data-acquisition components have separate analog and digital ground pins (Figure 39). It would be convenient to use a single ground line, however, current through ground wires and PC runs of the circuit card can cause hundreds of millivolts of error. Therefore, separate ground returns should be provided to minimize the current flow from the sensitive points to the system ground. These ground returns must be tied together at some point, usually best at the ADC package as shown.

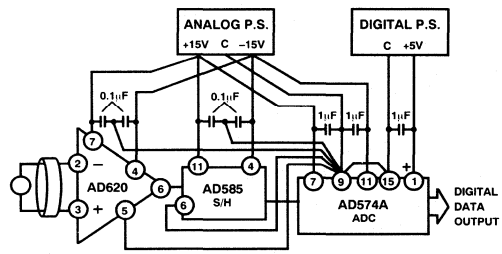


Figure 39. Basic Grounding Practice

GROUND RETURNS FOR INPUT BIAS CURRENTS

Input bias currents are those currents necessary to bias the input transistors of an amplifier. There must be a direct return path for these currents; therefore when amplifying "floating" input sources such as transformers, or ac-coupled sources, there must be a dc path from each input to ground as shown in Figure 40. Refer to the *Instrumentation Amplifier Application Guide* (free from Analog Devices) for more information regarding in amp applications.

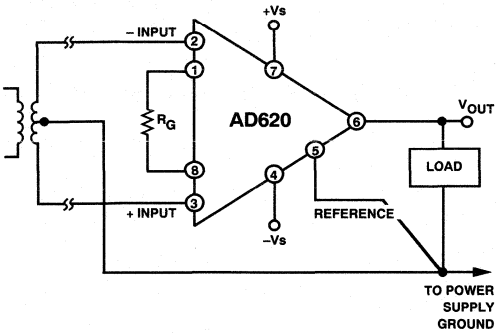


Figure 40a. Ground Returns for Bias Currents with Transformer Coupled Inputs

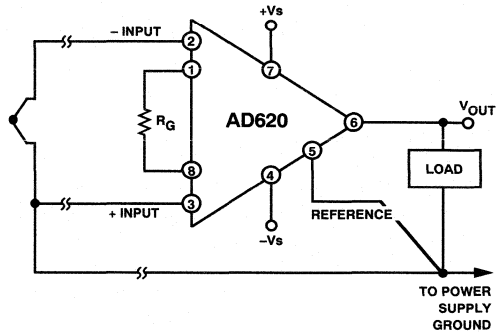


Figure 40b. Ground Returns for Bias Currents with Thermocouple Inputs

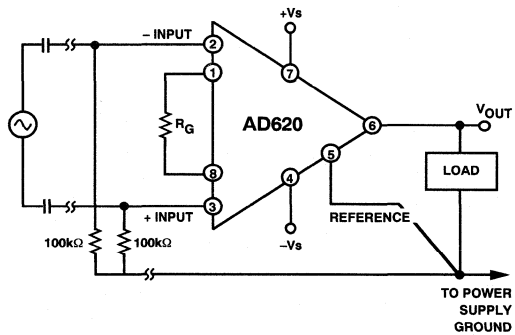


Figure 40c. Ground Returns for Bias Currents with AC Coupled Inputs

Low Drift, Low Power Instrumentation Amplifier

AD621

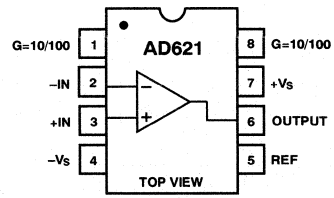
FEATURES
EASY TO USE
Pin-Strappable Gains of 10 & 100
All Errors Specified for Total System Performance
Higher Performance than Discrete In-Amp Designs
Available in 8-Pin DIP and SOIC
Low Power, 1.3 mA max Supply Current
Wide Power Supply Range (±2.3 V to ±18 V)
EXCELLENT DC PERFORMANCE
0.15% max, Total Gain Error
±5 ppm/°C, Total Gain Drift
125 μV max, Total Offset Voltage
1.0 μV/°C max, Offset Voltage Drift
LOW NOISE
9 nV/√Hz, @ 1 kHz, Input Voltage Noise
0.28 μV p–p Noise (0.1 Hz to 10 Hz)
EXCELLENT AC SPECIFICATIONS
800 kHz Bandwidth (G = 10), 200 kHz (G = 100)
12 μs Settling Time to 0.01%
APPLICATIONS
Weigh Scales
Transducer Interface & Data Acquisition Systems
Industrial Process Controls
Battery Powered and Portable Equipment

PRODUCT DESCRIPTION

The AD621 is an easy to use, low cost, low power, high accuracy instrumentation amplifier which is ideally suited for a wide range of applications. Its unique combination of high performance, small size and low power, outperforms discrete in amp implementations. High functionality, low gain errors and low gain drift errors are achieved by the use of internal gain setting resistors. Fixed gains of 10 and 100 can be easily set via external pin strapping. The AD621 is fully specified as a total system, therefore, simplifying the design process.

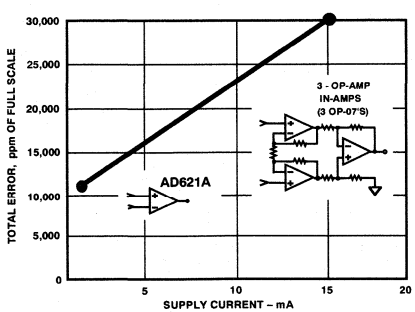
CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP (N), Cerdip (Q) and SOIC (R) Packages

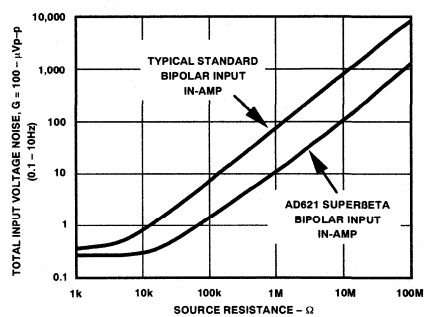


For portable or remote applications, where power dissipation, size and weight are critical, the AD621 features a very low supply current of 1.3 mA max and is packaged in a compact 8-pin SOIC, 8-pin plastic DIP or 8-pin cerdip. The AD621 also excels in applications requiring high total accuracy, such as precision data acquisition systems used in weigh scales and transducer interface circuits. Low maximum error specifications including nonlinearity of 10 ppm, gain drift of 5 ppm/°C, 50 μV offset voltage and 0.6 μV/°C offset drift ("B" grade), make possible total system performance at a lower cost than has been previously achieved with discrete designs or with other monolithic instrumentation amplifiers.

When operating from high source impedances, as in ECG and blood pressure monitors, the AD621 features the ideal combination of low noise and low input bias currents. Voltage noise is specified as 9 nV/√Hz at 1 kHz and 0.28 μV p–p from 0.1 Hz to 10 Hz. Input current noise is also extremely low at 0.1 pA/√Hz. The AD621 outperforms FET input devices with an input bias current specification of 1.5 nA max over the full industrial temperature range.



Three Op Amp IA Designs vs. AD621



Total Voltage Noise vs. Source Resistance

This is an abridged version of the data sheet. To obtain a complete data sheet, contact your nearest sales office.

AD621—SPECIFICATIONS

Gain = 10 (typical @ +25°C, V_S = ±15 V, and R_L = 2 kΩ unless otherwise specified)

Parameter	Conditions	AD621A Min	AD621A Typ	AD621A Max	AD621B Min	AD621B Typ	AD621B Max	AD621S[1] Min	AD621S[1] Typ	AD621S[1] Max	Units
GAIN											
Gain Error	V_{OUT} = ±10 V			0.15			0.05			0.15	%
Nonlinearity											
V_{OUT} = −10 V to +10 V	R_L = 2 kΩ		2	10		2	10		2	10	ppm of FS
Gain vs. Temperature			−1.5	±5		−1.5	±5		−1	±5	ppm/°C
TOTAL VOLTAGE OFFSET											
Offset (RTI)	V_S = ±15 V		75	250		50	125		75	250	µV
over Temperature	V_S = ±5 V to ±15 V			400			215			500	µV
Average TC	V_S = ±5 V to ±15 V		1.0	2.5		0.6	1.5		1.0	2.5	µV/°C
Offset Referred to the											
Input vs. Supply (PSR)[2]	V_S = ±2.3 V to ±18 V	95	120		100	120		95	120		dB
TOTAL NOISE											
Voltage Noise, (RTI)	1 kHz		13	17		13	17		13	17	nV/√Hz
RTI	0.1 Hz to 10 Hz		0.55			0.55	0.8		0.55	0.8	µV p–p
Current Noise	f = 1 kHz		100			100			100		fA/√Hz
	0.1 Hz–10 Hz		10			10			10		pA p–p
INPUT CURRENT	V_S = ±15 V										
Input Bias Current			0.5	2.0		0.5	1.0		0.5	2	nA
over Temperature				2.5			1.5			4	nA
Average TC			3.0			3.0			8.0		pA/°C
Input Offset Current			0.3	1.0		0.3	0.5		0.3	1.0	nA
over Temperature				1.5			0.75			2.0	nA
Average TC			1.5			1.5			8.0		pA/°C
INPUT											
Input Impedance											
Differential			10||2			10||2			10||2		GΩ||pF
Common-Mode			10||2			10||2			10||2		GΩ||pF
Input Voltage Range[3]	V_S = ±2.3 V to ±5 V	$-V_S$ + 1.9		$+V_S$ − 1.2	$-V_S$ + 1.9		$+V_S$ − 1.2	$-V_S$ + 1.9		$+V_S$ − 1.2	V
over Temperature		$-V_S$ + 2.1		$+V_S$ − 1.3	$-V_S$ + 2.1		$+V_S$ − 1.3	$-V_S$ + 2.1		$+V_S$ − 1.3	V
	V_S = ±5 V to ±18 V	$-V_S$ + 1.9		$+V_S$ − 1.4	$-V_S$ + 1.9		$+V_S$ − 1.4	$-V_S$ + 1.9		$+V_S$ − 1.4	V
over Temperature		$-V_S$ + 2.1		$+V_S$ − 1.4	$-V_S$ + 2.1		$+V_S$ − 1.4	$-V_S$ + 2.3		$+V_S$ − 1.4	V
Common-Mode Rejection											
Ratio DC to 60 Hz with											
1 kΩ Source Imbalance	V_{CM} = 0 V to ±10 V	93	110		100	110		93	110		dB
OUTPUT											
Output Swing	R_L = 10 kΩ,										
	V_S = ±2.3 V to ±5 V	$-V_S$ + 1.1		$+V_S$ − 1.2	$-V_S$ + 1.1		$+V_S$ − 1.2	$-V_S$ + 1.1		$+V_S$ − 1.2	V
over Temperature		$-V_S$ + 1.4		$+V_S$ − 1.3	$-V_S$ + 1.4		$+V_S$ − 1.3	$-V_S$ + 1.6		$+V_S$ − 1.3	V
	V_S = ±5 V to ±18 V	$-V_S$ + 1.2		$+V_S$ − 1.4	$-V_S$ + 1.2		$+V_S$ − 1.4	$-V_S$ + 1.2		$+V_S$ − 1.4	V
over Temperature		$-V_S$ + 1.6		$+V_S$ − 1.5	$-V_S$ + 1.6		$+V_S$ − 1.5	$-V_S$ + 2.3		$+V_S$ − 1.5	V
Short Current Circuit			±18			±18			±18		mA
DYNAMIC RESPONSE											
Small Signal,											
−3 dB Bandwidth			800			800			800		kHz
Slew Rate		0.75	1.2		0.75	1.2		0.75	1.2		V/µs
Settling Time to 0.01%	10 V Step		12			12			12		µs
REFERENCE INPUT											
R_{IN}			20			20			20		kΩ
I_{IN}	V_{IN}+, V_{REF} = 0		+50	+60		+50	+60		+50	+60	µA
Voltage Range		$-V_S$ + 1.6		$+V_S$ − 1.6	$-V_S$ + 1.6		$+V_S$ − 1.6	$-V_S$ + 1.6		$+V_S$ − 1.6	V
Gain to Output			1 ± 0.0001			1 ± 0.0001			1 ± 0.0001		
POWER SUPPLY											
Operating Range		±2.3		±18	±2.3		±18	±2.3		±18	V
Quiescent Current	V_S = ±2.3 V to ±18 V		0.9	1.3		0.9	1.3		0.9	1.3	mA
over Temperature			1.1	1.6		1.1	1.6		1.1	1.6	mA
TEMPERATURE RANGE											
For Specified Performance			−40 to +85			−40 to +85			−55 to +125		°C

NOTES

[1]See Analog Devices military data sheet for 883B tested specifications.

[2]This is defined as the supply range over which PSRR is defined.

[3]Input Voltage Range = CMV + (Gain × V_{DIFF}).

Specifications subject to change without notice.

Gain = 100 (typical @ +25°C, V_S = ±15 V, and R_L = 2 kΩ unless otherwise specified)

Parameter	Conditions	AD621A Min	AD621A Typ	AD621A Max	AD621B Min	AD621B Typ	AD621B Max	AD621S[1] Min	AD621S[1] Typ	AD621S[1] Max	Units
GAIN											
Gain Error	V_{OUT} = ±10 V			0.15			0.05			0.15	%
Nonlinearity											
V_{OUT} = −10 V to +10 V	R_L = 2 kΩ		2	10		2	10		2	10	ppm of FS
Gain vs. Temperature			−1	±5		−1	±5		−1	±5	ppm/°C
TOTAL VOLTAGE OFFSET											
Offset (RTI)	V_S = ±5 V ±15 V		35	125		25	50		35	125	µV
over Temperature	V_S = ±5 V to ±15 V			185			215			225	µV
Average TC	V_S = ±5 V to ±15 V		0.3	1.0		0.1	0.6		0.3	1.0	µV/°C
Offset Referred to the Input vs. Supply (PSR)[2]	V_S = ±2.3 V to ±18 V	110	140		120	140		110	140		dB
TOTAL NOISE											
Voltage Noise, (RTI)	1 kHz		9	13		9	13		9	13	nV/√Hz
RTI	0.1 Hz to 10 Hz		0.28			0.28	0.4		0.28	0.4	µV p-p
Current Noise	f = 1 kHz		100			100			100		fA/√Hz
	0.1 Hz–10 Hz		10			10			10		pA p-p
INPUT CURRENT	V_S = ±15 V										
Input Bias Current			0.5	2.0		0.5	1.0		0.5	2	nA
over Temperature				2.5			1.5			4	nA
Average TC			3.0			3.0			8.0		pA/°C
Input Offset Current			0.3	1.0		0.3	0.5		0.3	1.0	nA
over Temperature				1.5			0.75			2.0	nA
Average TC			1.5			1.5			8.0		pA/°C
INPUT											
Input Impedance											
Differential			10||2			10||2			10||2		GΩ||pF
Common-Mode			10||2			10||2			10||2		GΩ||pF
Input Voltage Range[3]	V_S = ±2.3 V to ±5 V	$-V_S$ + 1.9		$+V_S$ − 1.2	$-V_S$ + 1.9		$+V_S$ − 1.2	$-V_S$ + 1.9		$+V_S$ − 1.2	V
over Temperature		$-V_S$ + 2.1		$+V_S$ − 1.3	$-V_S$ + 2.1		$+V_S$ − 1.3	$-V_S$ + 2.1		$+V_S$ − 1.3	V
	V_S = ±5 V to ±18 V	$-V_S$ + 1.9		$+V_S$ − 1.4	$-V_S$ + 1.9		$+V_S$ − 1.4	$-V_S$ + 1.9		$+V_S$ − 1.4	V
over Temperature		$-V_S$ + 2.1		$+V_S$ − 1.4	$-V_S$ + 2.1		$+V_S$ − 1.4	$-V_S$ + 2.3		$+V_S$ − 1.4	V
Common-Mode Rejection Ratio DC to 60 Hz with 1 kΩ Source Imbalance	V_{CM} = 0 V to ±10 V	110	130		120	130		110	130		dB
OUTPUT											
Output Swing	R_L = 10 kΩ,										
	V_S = ±2.3 V to ±5 V	$-V_S$ + 1.1		$+V_S$ − 1.2	$-V_S$ + 1.1		$+V_S$ − 1.2	$-V_S$ + 1.1		$+V_S$ − 1.2	V
over Temperature		$-V_S$ + 1.4		$+V_S$ − 1.3	$-V_S$ + 1.4		$+V_S$ − 1.3	$-V_S$ + 1.6		$+V_S$ − 1.3	V
	V_S = ±5 V to ±18 V	$-V_S$ + 1.2		$+V_S$ − 1.4	$-V_S$ + 1.2		$+V_S$ − 1.4	$-V_S$ + 1.2		$+V_S$ − 1.4	V
over Temperature		$-V_S$ + 1.6		$+V_S$ − 1.5	$-V_S$ + 1.6		$+V_S$ − 1.5	$-V_S$ + 2.3		$+V_S$ − 1.5	V
Short Current Circuit			±18			±18			±18		mA
DYNAMIC RESPONSE											
Small Signal, −3 dB Bandwidth			200			200			200		kHz
Slew Rate		0.75	1.2		0.75	1.2		0.75	1.2		V/µs
Settling Time to 0.01%	10 V Step		12			12			12		µs
REFERENCE INPUT											
R_{IN}			20			20			20		kΩ
I_{IN}	V_{IN}+, V_{REF} = 0		+50	+60		+50	+60		+50	+60	µA
Voltage Range		$-V_S$ + 1.6		$+V_S$ − 1.6	$-V_S$ + 1.6		$+V_S$ − 1.6	$-V_S$ + 1.6		$+V_S$ − 1.6	V
Gain to Output			1 ± 0.0001			1 ± 0.0001			1 ± 0.0001		
POWER SUPPLY											
Operating Range		±2.3		±18	±2.3		±18	±2.3		±18	V
Quiescent Current	V_S = ±2.3 V to ±18 V		0.9	1.3		0.9	1.3		0.9	1.3	mA
over Temperature			1.1	1.6		1.1	1.6		1.1	1.6	mA
TEMPERATURE RANGE											
For Specified Performance			−40 to +85			−40 to +85			−55 to +125		°C

NOTES
[1]See Analog Devices military data sheet for 883B tested specifications.
[2]This is defined as the supply range over which PSRR is defined.
[3]Input Voltage Range = CMV + (Gain × V_{DIFF}).
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2] . . . . . 650 mW
Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±25 V
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range (Q) . . . . . −65°C to +150°C
Storage Temperature Range (N, R) . . . . . −65°C to +125°C
Operating Temperature Range
AD621A, B . . . . . −40°C to +85°C
AD621S[3] . . . . . −55°C to +125°C
Lead Temperature Range
(Soldering 10 seconds) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air:
8-Pin Plastic DIP Package: θ_{JA} = 95°C/Watt
8-Pin Cerdip Package: θ_{JA} = 110°C/Watt
8-Pin SOIC Package: θ_{JA} = 155°C/Watt
[3]See Analog Devices' military data sheet for 883B specifications.

ESD SUSCEPTIBILITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although the AD621 features proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

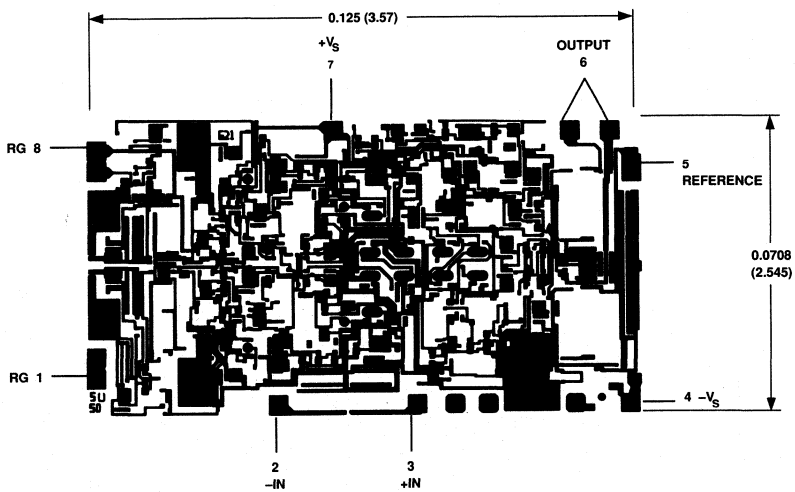
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option[1]
AD621AN	−40°C to +85°C	8-Pin Plastic DIP	N-8
AD621BN	−40°C to +85°C	8-Pin Plastic DIP	N-8
AD621AR	−40°C to +85°C	8-Pin Plastic SOIC	R-8
AD621BR	−40°C to +85°C	8-Pin Plastic SOIC	R-8
AD621SQ/883B[2]	−55°C to +125°C	8-Pin Cerdip	Q-8
AD621ACHIPS	−40°C to +85°C	Die	

[1]For outline information see Package Information section
[2]See Analog Devices' military data sheet for 883B specifications.

METALIZATION PHOTOGRAPHY

Dimensions shown in inches and (mm)
Contact factory for latest dimensions



ANALOG DEVICES

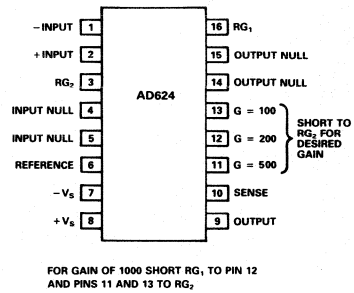
Precision Instrumentation Amplifier

AD624

FEATURES

Low Noise: 0.2μV p-p 0.1Hz to 10Hz
Low Gain TC: 5ppm max (G = 1)
Low Nonlinearity: 0.001% max (G = 1 to 200)
High CMRR: 130dB min (G = 500 to 1000)
Low Input Offset Voltage: 25μV, max
Low Input Offset Voltage Drift: 0.25μV/°C max
Gain Bandwidth Product: 25MHz
Pin Programmable Gains of 1, 100, 200, 500, 1000
No External Components Required
Internally Compensated

CONNECTION DIAGRAM



4

PRODUCT DESCRIPTION

The AD624 is a high precision low noise instrumentation amplifier designed primarily for use with low level transducers, including load cells, strain gauges and pressure transducers. An outstanding combination of low noise, high gain accuracy, low gain temperature coefficient and high linearity make the AD624 ideal for use in high resolution data acquisition systems.

The AD624C has an input offset voltage drift of less than 0.25μV/°C, output offset voltage drift of less than 10μV/°C, CMRR above 80dB at unity gain (130dB at G = 500) and a maximum nonlinearity of 0.001% at G = 1. In addition to these outstanding dc specifications the AD624 exhibits superior ac performance as well. A 25MHz gain bandwidth product, 5V/μs slew rate and 15μs settling time permit the use of the AD624 in high speed data acquisition applications.

The AD624 does not need any external components for pre-trimmed gains of 1, 100, 200, 500 and 1000. Additional gains such as 250 and 333 can be programmed within one percent accuracy with external jumpers. A single external resistor can also be used to set the 624's gain to any value in the range of 1 to 10,000.

PRODUCT HIGHLIGHTS

1. The AD624 offers outstanding noise performance. Input noise is typically less than $4nV/\sqrt{Hz}$ at 1kHz.
2. The AD624 is a functionally complete instrumentation amplifier. Pin programmable gains of 1, 100, 200, 500 and 1000 are provided on the chip. Other gains are achieved through the use of a single external resistor.
3. The offset voltage, offset voltage drift, gain accuracy and gain temperature coefficients are guaranteed for all pre-trimmed gains.
4. The AD624 provides totally independent input and output offset nulling terminals for high precision applications. This minimizes the effect of offset voltage in gain ranging applications.
5. A sense terminal is provided to enable the user to minimize the errors induced through long leads. A reference terminal is also provided to permit level shifting at the output.

AD624 — SPECIFICATIONS (@ V_S = ±15V, R_L = 2kΩ and T_A = +25°C unless otherwise specified)

Model	AD624A Min	AD624A Typ	AD624A Max	AD624B Min	AD624B Typ	AD624B Max	AD624C Min	AD624C Typ	AD624C Max	AD624S Min	AD624S Typ	AD624S Max	Units
GAIN													
Gain Equation (External Resistor Gain Programming)		$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$		
Gain Range (Pin Programmable)		1 to 1000			1 to 1000			1 to 1000			1 to 1000		
Gain Error													
G = 1			±0.05			±0.03			±0.02			±0.05	%
G = 100			±0.25			±0.15			±0.1			±0.25	%
G = 200, 500			±0.5			±0.35			±0.25			±0.5	%
G = 1000			±1.0			±1.0			±1.0			±1.0	%
Nonlinearity													
G = 1			±0.005			±0.003			±0.001			±0.005	%
G = 100, 200			±0.005			±0.003			±0.001			±0.005	%
G = 500, 1000			±0.005			±0.005			±0.005			±0.005	%
Gain vs. Temperature													
G = 1			5			5			5			5	ppm/°C
G = 100, 200			10			10			10			10	ppm/°C
G = 500, 1000			25			15			15			15	ppm/°C
VOLTAGE OFFSET (May be Nulled)													
Input Offset Voltage			200			75			25			75	µV
vs. Temperature			2			0.5			0.25			2.0	µV/°C
Output Offset Voltage			5			3			2			3	mV
vs. Temperature			50			25			10			50	µV/°C
Offset Referred to the Input vs. Supply													
G = 1	70			75			80			75			dB
G = 100, 200	95			105			110			105			dB
G = 500, 1000	100			110			115			110			dB
INPUT CURRENT													
Input Bias Current			±50			±25			±15			±50	nA
vs. Temperature		±50			±50			±50			±50		pA/°C
Input Offset Current			±35			±15			±10			±35	nA
vs. Temperature		±20			±20			±20			±20		pA/°C
INPUT													
Input Impedance													
Differential Resistance		10^9			10^9			10^9			10^9		Ω
Differential Capacitance		10			10			10			10		pF
Common-Mode Resistance		10^9			10^9			10^9			10^9		Ω
Common-Mode Capacitance		10			10			10			10		pF
Input Voltage Range[1]													
Max Differ. Input Linear (V_{DL})	±10			±10			±10			±10			V
Max Common-Mode Linear (V_{CM})		$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$		V
Common-Mode Rejection dc to 60Hz with 1kΩ Source Imbalance													
G = 1	70			75			80			70			dB
G = 100, 200	100			105			110			100			dB
G = 500, 1000	110			120			130			110			dB
OUTPUT RATING													
V_{OUT}, R_L = 2kΩ		±10			±10			±10			±10		V
DYNAMIC RESPONSE													
Small Signal −3dB													
G = 1		1			1			1			1		MHz
G = 100		150			150			150			150		kHz
G = 200		100			100			100			100		kHz
G = 500		50			50			50			50		kHz
G = 1000		25			25			25			25		kHz
Slew Rate		5.0			5.0			5.0			5.0		V/µs
Settling Time to 0.01%, 20V Step													
G = 1 to 200		15			15			15			15		µs
G = 500		35			35			35			35		µs
G = 1000		75			75			75			75		µs
NOISE													
Voltage Noise, 1kHz													
R.T.I.		4			4			4			4		$nV/\sqrt{Hz}$
R.T.O.		75			75			75			75		$nV/\sqrt{Hz}$
R.T.I., 0.1 to 10Hz													
G = 1		10			10			10			10		µV p-p
G = 100		0.3			0.3			0.3			0.3		µV p-p
G = 200, 500, 1000		0.2			0.2			0.2			0.2		µV p-p
Current Noise													
0.1Hz to 10Hz		60			60			60			60		pA p-p
SENSE INPUT													
R_{IN}	8	10	12	8	10	12	8	10	12	8	10	12	kΩ
I_{IN}		30			30			30			30		µA
Voltage Range	±10			±10			±10			±10			V
Gain to Output		1			1			1			1		%
REFERENCE INPUT													
R_{IN}	16	20	24	16	20	24	16	20	24	16	20	24	kΩ
I_{IN}		30			30			30			30		µA
Voltage Range	±10			±10			±10			±10			V
Gain to Output		1			1			1			1		%

Model	AD624A Min	AD624A Typ	AD624A Max	AD624B Min	AD624B Typ	AD624B Max	AD624C Min	AD624C Typ	AD624C Max	AD624S Min	AD624S Typ	AD624S Max	Units
TEMPERATURE RANGE													
Specified Performance	−25		+85	−25		+85	−25		+85	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
POWER SUPPLY													
Power Supply Range	**±6**	±15	**±18**	**±6**	±15	**±18**	**±6**	±15	**±18**	**±6**	±15	**±18**	V
Quiescent Current		3.5	5		3.5	5		3.5	5		3.5	5	mA
PACKAGE OPTION[2]													
Ceramic (D-16)		AD624AD			AD624BD			AD624CD			AD624SD, AD624SD/883B		
Chips Available		AD624AChips									AD624SChips		

NOTES

[1] V_{DL} is the maximum differential input voltage at G = 1 for specified nonlinearity. V_{DL} at other gains = 10V/G. V_D = actual differential input voltage. Example: G = 10, V_D = 0.50. V_{CM} = 12V − (10/2 × 0.50V) = 9.5V.

[2] For outline information see Package Information section.

Specifications subject to change without notice.

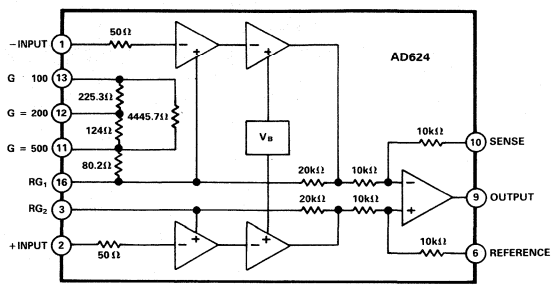
Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . ±18V
Internal Power Dissipation 420mW
Input Voltage . . . . . ±V_S
Differential Input Voltage . . . . . ±V_S
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range
AD624A/B/C . . . . . −25°C to +85°C
AD624S . . . . . −55°C to +125°C
Lead Temperature (Soldering, 60secs) . . . . . +300°C

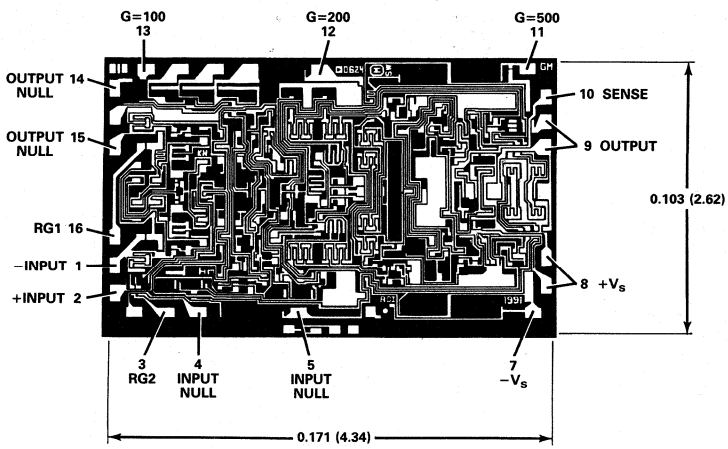
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

FUNCTIONAL BLOCK DIAGRAM



METALIZATION PHOTOGRAPH

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



AD624—Typical Characteristics

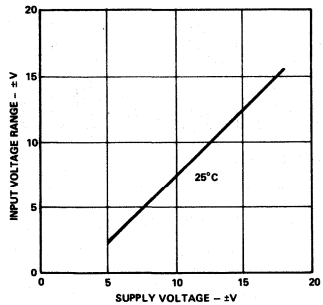


Figure 1. Input Voltage Range vs. Supply Voltage, G = 1

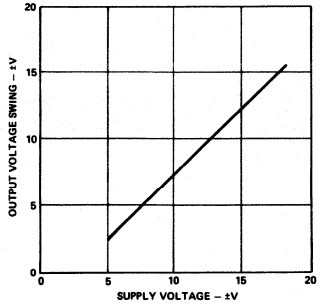


Figure 2. Output Voltage Swing vs. Supply Voltage

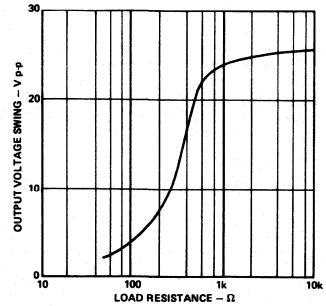


Figure 3. Output Voltage Swing vs. Load Resistance

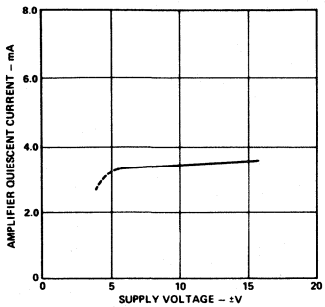


Figure 4. Quiescent Current vs. Supply Voltage

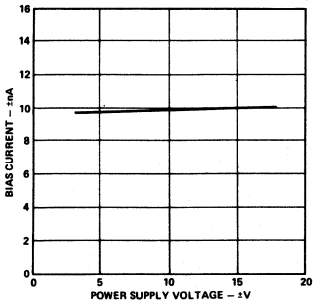


Figure 5. Input Bias Current vs. Supply Voltage

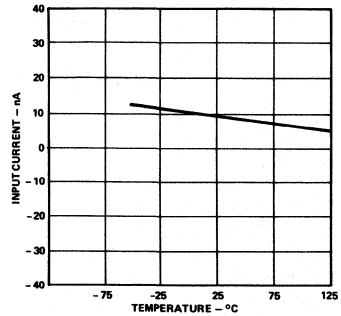


Figure 6. Input Bias Current vs. Temperature

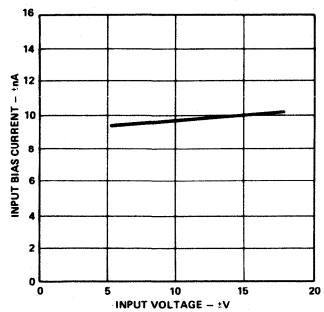


Figure 7. Input Bias Current vs. CMV

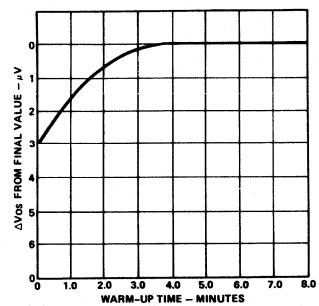


Figure 8. Offset Voltage, RTI, Turn On Drift

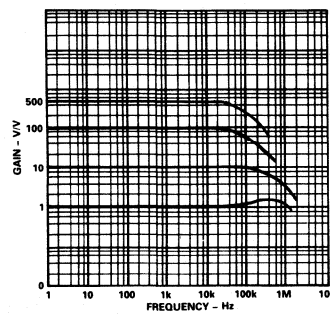


Figure 9. Gain vs. Frequency

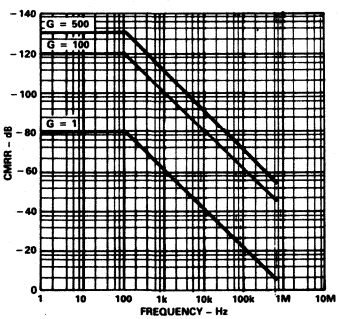


Figure 10. CMRR vs. Frequency RTI, Zero to 1k Source Imbalance

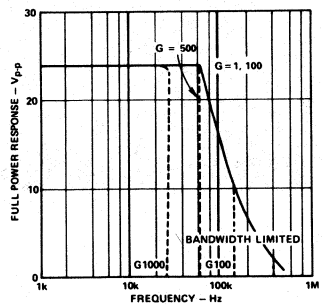


Figure 11. Large Signal Frequency Response

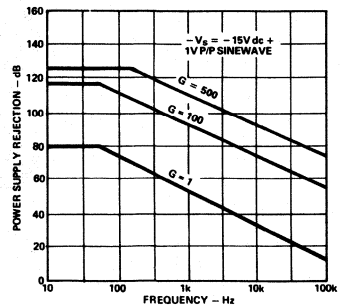


Figure 12. Positive PSRR vs. Frequency

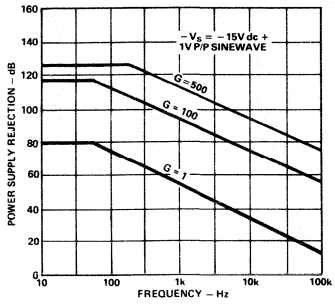


Figure 13. Negative PSRR vs. Frequency

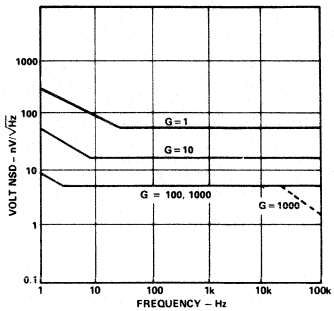


Figure 14. RTI Noise Spectral Density vs. Gain

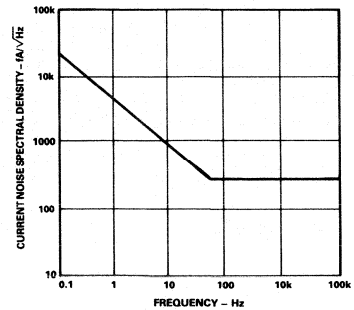


Figure 15. Input Current Noise

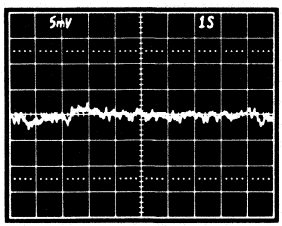


Figure 16. Low Frequency Voltage Noise – G = 1 (System Gain = 1000)

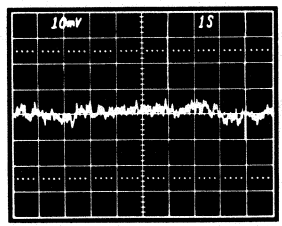


Figure 17. Low Frequency Voltage Noise – G = 1000 (System Gain = 100,000)

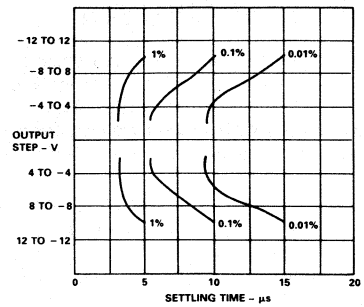


Figure 18. Settling Time Gain = 1

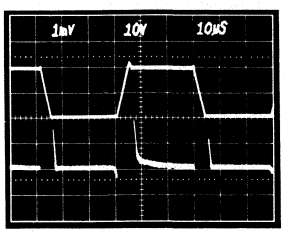


Figure 19. Large Signal Pulse Response and Settling Time – G = 1

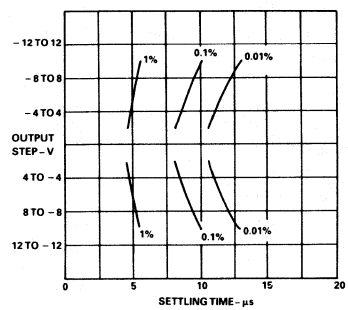


Figure 20. Settling Time Gain = 100

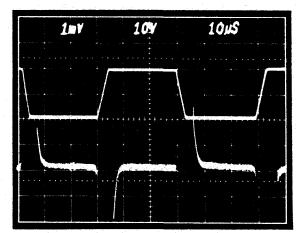


Figure 21. Large Signal Pulse Response and Settling Time G = 100

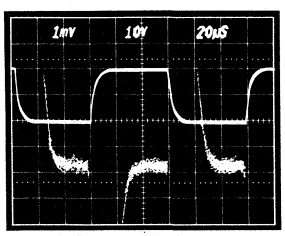


Figure 22. Range Signal Pulse Response and Settling Time G = 500

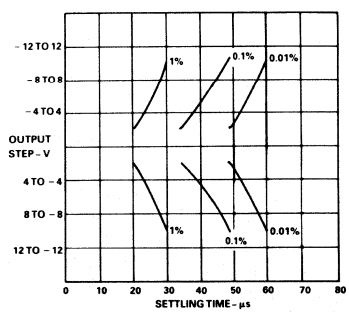


Figure 23. Settling Time Gain = 1000

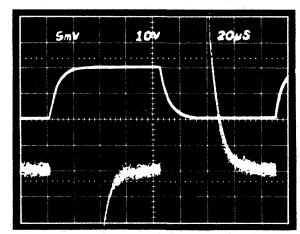


Figure 24. Large Signal Pulse Response and Settling Time G = 1000

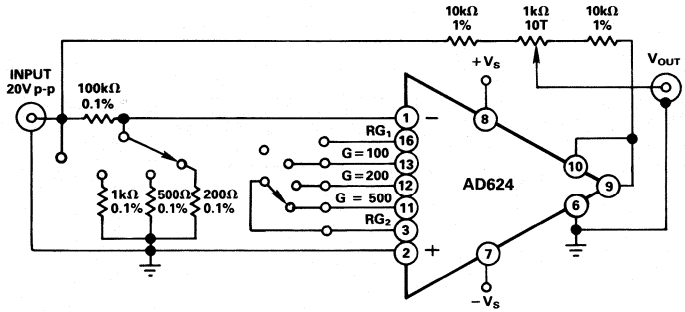


Figure 25. Settling Time Test Circuit

Theory of Operation

The AD624 is a monolithic instrumentation amplifier based on a modification of the classic three-op-amp instrumentation amplifier. Monolithic construction and laser-wafer-trimming allow the tight matching and tracking of circuit components and the high level of performance that this circuit architecture is capable of.

A preamp section (Q1–Q4) develops the programmed gain by the use of feedback concepts. Feedback from the outputs of A1 and A2 forces the collector currents of Q1–Q4 to be constant thereby impressing the input voltage across R_G.

The gain is set by choosing the value of R_G from the equation, $\text{Gain} = \frac{40k}{R_G} + 1$. The value of R_G also sets the transconductance of the input preamp stage increasing it asymptotically to the transconductance of the input transistors as R_G is reduced for larger gains. This has three important advantages. First, this approach allows the circuit to achieve a very high open loop gain of 3×10^8 at a programmed gain of 1000 thus reducing gain related errors to a negligible 3ppm. Second, the gain bandwidth product which is determined by C3 or C4 and the input transconductance, reaches 25MHz. Third, the input voltage noise reduces to a value determined by the collector current of the input transistors for an RTI noise of $4nV/\sqrt{Hz}$ at G ≥ 500.

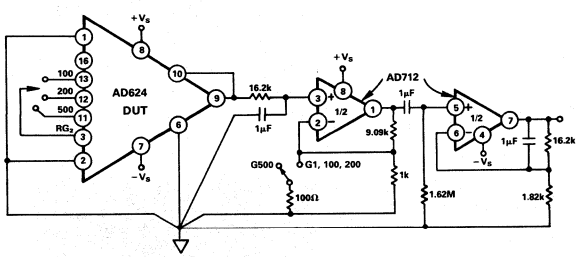


Figure 26. Noise Test Circuit

INPUT CONSIDERATIONS

Under input overload conditions the user will see $R_G + 100\Omega$ and two diode drops (~1.2V) between the plus and minus inputs, in either direction. If safe overload current under all conditions is assumed to be 10mA, the maximum overload voltage is ~ ±2.5V. While the AD624 can withstand this continuously, momentary overloads of ±10V will not harm the device. On the other hand the inputs should never exceed the supply voltage.

The AD524 should be considered in applications that require protection from severe input overload. If this is not possible, external protection resistors can be put in series with the inputs of the AD624 to augment the internal (50Ω) protection resistors. This will most seriously degrade the noise performance. For this reason the value of these resistors should be chosen to be as low as possible and still provide 10mA of current limiting under maximum continuous overload conditions. In selecting the value of these resistors, the internal gain setting resistor and the 1.2 volt drop need to be considered. For example, to protect the device from a continuous differential overload of 20V at a gain of 100, 1.9kΩ of resistance is required. The internal gain resistor is 404Ω; the internal protect resistor is 100Ω. There is a 1.2V drop across D1 or D2 and the base-emitter junction of either Q1 and Q3 or Q2 and Q4 as shown in Figure 27, 1400Ω of external resistance would be required (700Ω in series with each input). The RTI noise in this case would be $\sqrt{4KTR_{ext.} + (4nV/\sqrt{Hz})^2} = 6.2nV/\sqrt{Hz}$.

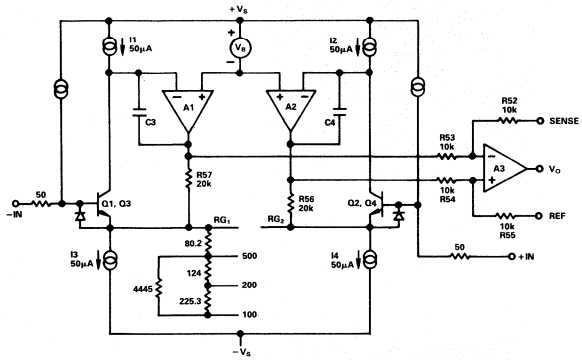


Figure 27. Simplified Circuit of Amplifier; Gain is Defined as ((R56 + R57)/(R_G) + 1. For a Gain of 1, R_G is an Open Circuit.

INPUT OFFSET AND OUTPUT OFFSET

Voltage offset specifications are often considered a figure of merit for instrumentation amplifiers. While initial offset may be adjusted to zero, shifts in offset voltage due to temperature variations will cause errors. Intelligent systems can often correct for this factor with an auto-zero cycle, but there are many small-signal high-gain applications that don't have this capability.

Voltage offset and offset drift each have two components; input and output. Input offset is that component of offset that is

directly proportional to gain i.e., input offset as measured at the output at G = 100 is 100 times greater than at G = 1. Output offset is independent of gain. At low gains, output offset drift is dominant, while at high gains input offset drift dominates. Therefore, the output offset voltage drift is normally specified as drift at G = 1 (where input effects are insignificant), while input offset voltage drift is given by drift specification at a high gain (where output offset effects are negligible). All input-related numbers are referred to the input (RTI) which is to say that the effect on the output is "G" times larger. Voltage offset vs. power supply is also specified at one or more gain settings and is also RTI.

By separating these errors, one can evaluate the total error independent of the gain setting used. In a given gain configuration both errors can be combined to give a total error referred to the input (R.T.I.) or output (R.T.O.) by the following formula:

Total Error R.T.I. = input error + (output error/gain)

Total Error R.T.O. = (Gain × input error) + output error

As an illustration, a typical AD624 might have a +250μV output offset and a −50μV input offset. In a unity gain configuration, the *total* output offset would be 200μV or the sum of the two. At a gain of 100, the output offset would be −4.75mV or: +250μV + 100(−50μV) = −4.75mV.

The AD624 provides for both input and output offset adjustment. This optimizes nulling in very high precision applications and minimizes offset voltage effects in switched gain applications. In such applications the input offset is adjusted first at the highest programmed gain, then the output offset is adjusted at G = 1.

GAIN

The AD624 includes high accuracy pre-trimmed internal gain resistors. These allow for single connection programming of gains of 1, 100, 200 and 500. Additionally, a variety of gains including a pre-trimmed gain of 1000 can be achieved through series and parallel combinations of the internal resistors. Table I shows the available gains and the appropriate pin connections and gain temperature coefficients.

The gain values achieved via the combination of internal resistors are extremely useful. The temperature coefficient of the gain is dependent primarily on the mismatch of the temperature coefficients of the various internal resistors. Tracking of these resistors is extremely tight resulting in the low gain TC's shown in Table I.

If the desired value of gain is not attainable using the internal resistors, a single external resistor can be used to achieve any gain between 1 and 10,000. This resistor connected between

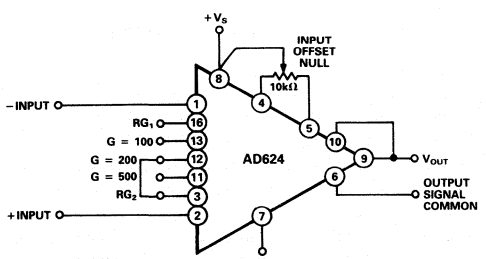


Figure 28. Operating Connections for G =200

Gain (Nominal)	Temperature Coefficient (Nominal)	Pin 3 to Pin	Connect Pins
1	−0ppm/°C	–	–
100	−1.5ppm/°C	13	–
125	−5ppm/°C	13	11 to 16
137	−5.5ppm/°C	13	11 to 12
186.5	−6.5ppm/°C	13	11 to 12 to 16
200	−3.5ppm/°C	12	–
250	−5.5ppm/°C	12	11 to 13
333	−15ppm/°C	12	11 to 16
375	−0.5ppm/°C	12	13 to 16
500	−10ppm/°C	11	–
624	−5ppm/°C	11	13 to 16
688	−1.5ppm/°C	11	11 to 12; 13 to 16
831	+4ppm/°C	11	16 to 12
1000	0ppm/°C	11	16 to 12; 13 to 11

Table I.

pins 3 and 16 programs the gain according to the formula $R_G = \frac{40k}{G-1}$ (see Figure 29). For best results R_G should be a precision resistor with a low temperature coefficient. An external R_G affects both gain accuracy and gain drift due to the mismatch between it and the internal thin-film resistors R56 and R57. Gain accuracy is determined by the tolerance of the external R_G and the absolute accuracy of the internal resistors (±20%). Gain drift is determined by the mismatch of the temperature coefficient of R_G and the temperature coefficient of the internal resistors (−15ppm/°C typ), and the temperature coefficient of the internal interconnections.

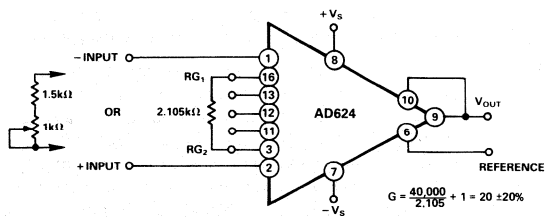


Figure 29. Operating Connections for G = 20

The AD624 may also be configured to provide gain in the output stage. Figure 30 shows an H pad attenuator connected to the reference and sense lines of the AD624. The values of R1, R2 and R3 should be selected to be as low as possible to minimize the gain variation and reduction of CMRR. Varying R2 will precisely set the gain without affecting CMRR. CMRR is determined by the match of R1 and R3.

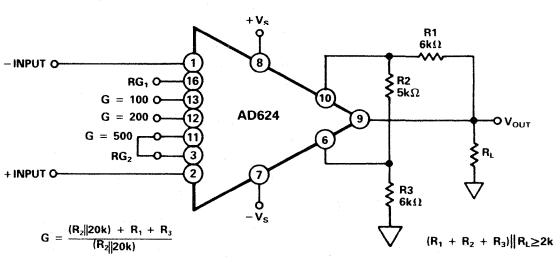


Figure 30. Gain of 2500

NOISE

The AD624 is designed to provide noise performance near the theoretical noise floor. This is an extremely important design criteria as the front end noise of an instrumentation amplifier is the ultimate limitation on the resolution of the data acquisition system it is being used in. There are two sources of noise in an instrument amplifier, the input noise, predominantly generated by the differential input stage, and the output noise, generated by the output amplifier. Both of these components are present at the input (and output) of the instrumentation amplifier. At the input, the input noise will appear unaltered; the output noise will be attenuated by the closed loop gain (at the output, the output noise will be unaltered; the input noise will be amplified by the closed loop gain). Those two noise sources must be root sum squared to determine the total noise level expected at the input (or output).

The low frequency (0.1 to 10Hz) voltage noise due to the output stage is 10μV p-p, the contribution of the input stage is 0.2μV p-p. At a gain of 10, the RTI voltage noise would be 1μV p-p, $\sqrt{\left(\frac{10}{G}\right)^2 + (0.2)^2}$. The RTO voltage noise would be 10.2μV p-p, $\sqrt{10^2 + (0.2\ (G))^2}$. These calculations hold for applications using either internal or external gain resistors.

INPUT BIAS CURRENTS

Input bias currents are those currents necessary to bias the input transistors of a dc amplifier. Bias currents are an additional source of input error and must be considered in an total error budget. The bias currents when multiplied by the source resistance imbalance appear as an additional offset voltage. (What is of concern in calculating bias current errors is the change in bias current with respect to signal voltage and temperature.) Input offset current is the difference between the two input bias currents. The effect of offset current is an input offset voltage whose magnitude is the offset current times the source resistance.

Although instrumentation amplifiers have differential inputs, there must be a return path for the bias currents. If this is not provided, those currents will charge stray capacitances, causing the output to drift uncontrollably or to saturate. Therefore, when amplifying "floating" input sources such as transformers and thermocouples, as well as ac-coupled sources, there must still be a dc path from each input to ground, (see Figure 31).

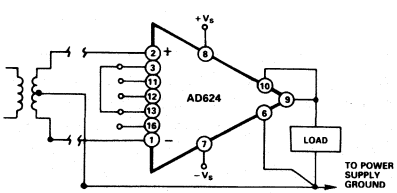


Figure 31a. Transformer Coupled

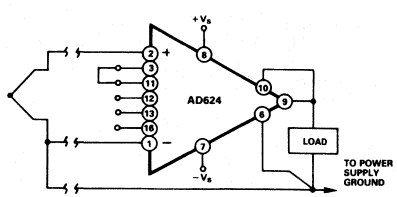


Figure 31b. Thermocouple

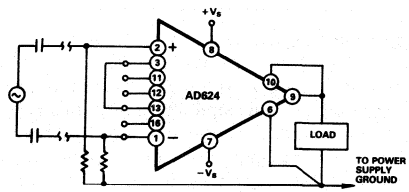


Figure 31c. AC Coupled

Figure 31. Indirect Ground Returns for Bias Currents

COMMON-MODE REJECTION

Common-mode rejection is a measure of the change in output voltage when both inputs are changed by equal amounts. These specifications are usually given for a full-range input voltage change and a specified source imbalance. "Common-Mode Rejection Ratio" (CMRR) is a ratio expression while "Common-Mode Rejection" (CMR) is the logarithm of that ratio. For example, a CMRR of 10,000 corresponds to a CMR of 80dB.

In an instrumentation amplifier, ac common-mode rejection is only as good as the differential phase shift. Degradation of ac common-mode rejection is caused by unequal drops across differing track resistances and a differential phase shift due to varied stray capacitances or cable capacitances. In many applications shielded cables are used to minimize noise. This technique can create common-mode rejection errors unless the shield is properly driven. Figures 32 and 33 shows active data guards which are configured to improve ac common-mode rejection by "bootstrapping" the capacitances of the input cabling, thus minimizing differential phase shift.

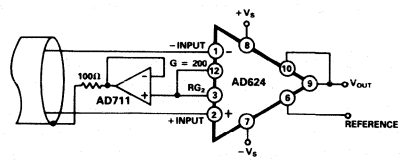


Figure 32. Shield Driver, G ≥ 100

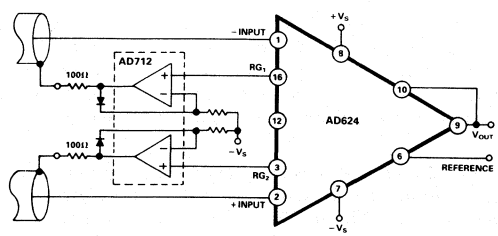


Figure 33. Differential Shield Driver

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These grounds must be tied together at one point, usually at the system power supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the data acquisition components. Separate ground returns should be provided to

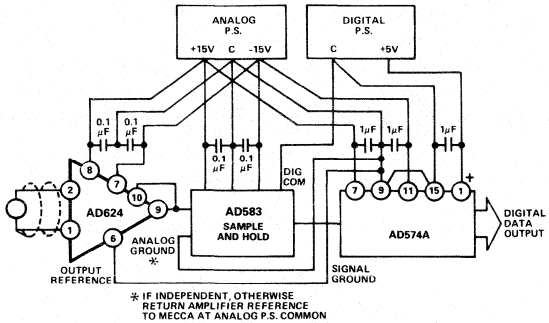


Figure 34. Basic Grounding Practice

minimize the current flow in the path from the most sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors (see Figure 34).

Since the output voltage is developed with respect to the potential on the reference terminal an instrumentation amplifier can solve many grounding problems.

SENSE TERMINAL

The sense terminal is the feedback point for the instrument amplifier's output amplifier. Normally it is connected to the instrument amplifier output. If heavy load currents are to be drawn through long leads, voltage drops due to current flowing through lead resistance can cause errors. The sense terminal can be wired to the instrument amplifier at the load thus putting the IxR drops "inside the loop" and virtually eliminating this error source.

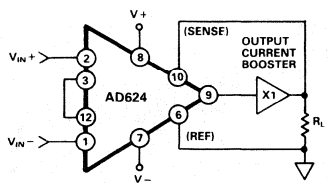


Figure 35. AD624 Instrumentation Amplifier with Output Current Booster

Typically, IC instrumentation amplifiers are rated for a full ± 10 volt output swing into 2kΩ. In some applications, however, the need exists to drive more current into heavier loads. Figure 35 shows how a current booster may be connected "inside the loop" of an instrumentation amplifier to provide the required current without significantly degrading overall performance. The effects of nonlinearities, offset and gain inaccuracies of the buffer are reduced by the loop gain of the IA output amplifier. Offset drift of the buffer is similarly reduced.

REFERENCE TERMINAL

The reference terminal may be used to offset the output by up to ± 10V. This is useful when the load is "floating" or does not share a ground with the rest of the system. It also provides a direct means of injecting a precise offset. It must be remembered that the total output swing is ± 10 volts, from ground, to be shared between signal and reference offset.

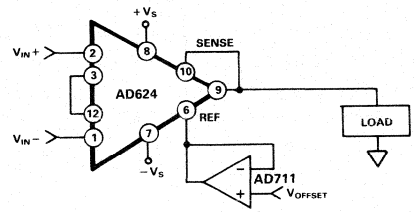


Figure 36. Use of Reference Terminal to Provide Output Offset

When the IA is of the three-amplifier configuration it is necessary that nearly zero impedance be presented to the reference terminal. Any significant resistance, including those caused by PC layouts or other connection techniques, which appears between the reference pin and ground will increase the gain of the noninverting signal path, thereby upsetting the common-mode rejection of the IA. Inadvertent thermocouple connections created in the sense and reference lines should also be avoided as they will directly affect the output offset voltage and output offset voltage drift.

In the AD624 a reference source resistance will unbalance the CMR trim by the ratio of $10k\Omega/R_{REF}$. For example, if the reference source impedance is 1Ω, CMR will be reduced to 80dB (10kΩ/1Ω = 80dB). An operational amplifier may be used to provide that low impedance reference point as shown in Figure 36. The input offset voltage characteristics of that amplifier will add directly to the output offset voltage performance of the instrumentation amplifier.

An instrumentation amplifier can be turned into a voltage-to-current converter by taking advantage of the sense and reference terminals as shown in Figure 37.

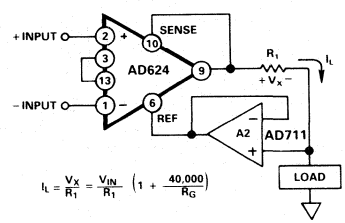


Figure 37. Voltage-to-Current Converter

By establishing a reference at the "low" side of a current setting resistor, an output current may be defined as a function of input voltage, gain and the value of that resistor. Since only a small current is demanded at the input of the buffer amplifier A_2, the forced current I_L will largely flow through the load. Offset and drift specifications of A_2 must be added to the output offset and drift specifications of the IA.

PROGRAMMABLE GAIN

Figure 38 shows the AD624 being used as a software programmable gain amplifier. Gain switching can be accomplished with mechanical switches such as DIP switches or reed relays. It should be noted that the "on" resistance of the switch in series with the internal gain resistor becomes part of the gain equation and will have an effect on gain accuracy.

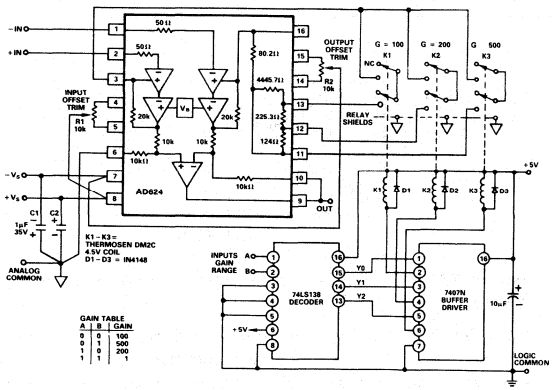


Figure 38. Gain Programmable Amplifier

A significant advantage in using the internal gain resistors in a programmable gain configuration is the minimization of thermocouple signals which are often present in multiplexed data acquisition systems.

If the full performance of the AD624 is to be achieved, the user must be extremely careful in designing and laying out his circuit to minimize the remaining thermocouple signals.

The AD624 can also be connected for gain in the output stage. Figure 39 shows an AD547 used as an active attenuator in the output amplifier's feedback loop. The active attenuation presents a very low impedance to the feedback resistors therefore minimizing the common-mode rejection ratio degradation.

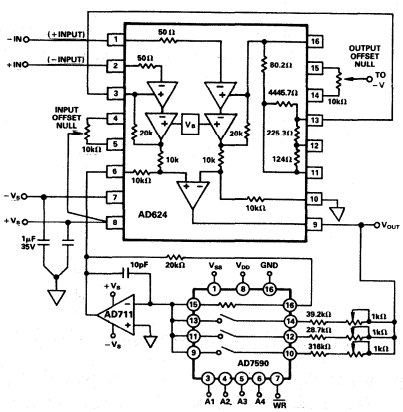


Figure 39. Programmable Output Gain

Another method for developing the switching scheme is to use a DAC. The AD7528 dual DAC which acts essentially as a pair of switched resistive attenuators having high analog linearity and symmetrical bipolar transmission is ideal in this application. The multiplying DAC's advantage is that it can handle inputs of either polarity or zero without affecting the programmed gain. The circuit shown uses an AD7528 to set the gain (DAC A) and to perform a fine adjustment (DAC B).

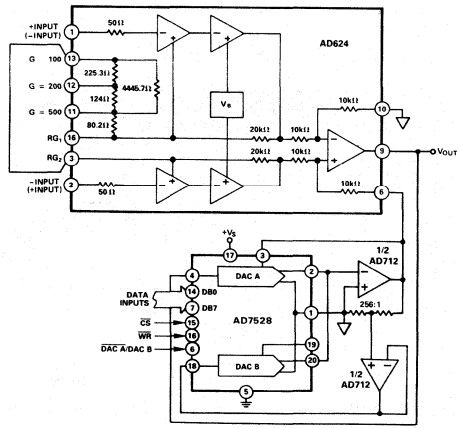


Figure 40. Programmable Output Gain Using a DAC

AUTO-ZERO CIRCUITS

In many applications it is necessary to provide very accurate data in high gain configurations. At room temperature the offset effects can be nulled by the use of offset trimpots. Over the operating temperature range, however, offset nulling becomes a problem. The circuit of Figure 41 shows a CMOS DAC operating in the bipolar mode and connected to the reference terminal to provide software controllable offset adjustments.

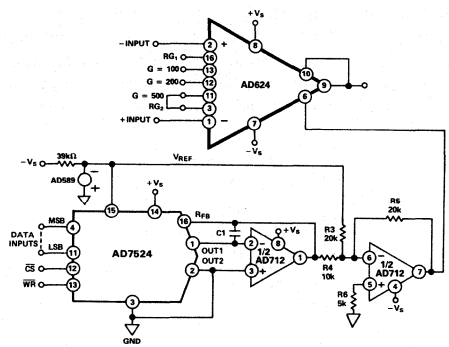


Figure 41. Software Controllable Offset

In many applications complex software algorithms for auto-zero applications are not available. For these applications Figure 42 provides a hardware solution.

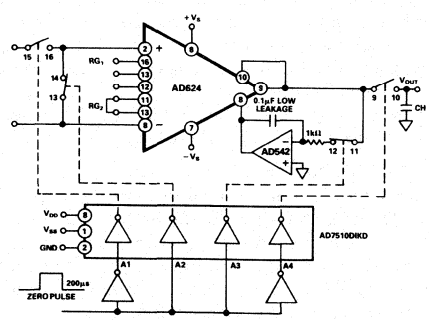


Figure 42. Auto-Zero Circuit

The microprocessor controlled data acquisition system shown in Figure 43 includes includes both auto-zero and auto-gain capability. By dedicating two of the differential inputs, one to ground and one to the A/D reference, the proper program calibration cycles can eliminate both initial accuracy errors and accuracy errors over temperature. The auto-zero cycle, in this application, converts a number that appears to be ground and then writes that same number (8 bit) to the AD7524 which eliminates the zero error since its output has an inverted scale. The auto-gain cycle converts the A/D reference and compares it with full scale. A multiplicative correction factor is then computed and applied to subsequent readings.

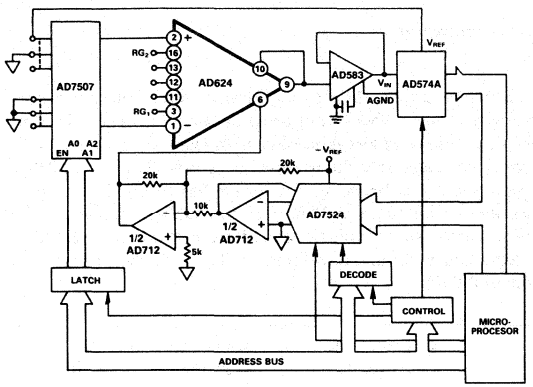


Figure 43. Microprocessor Controlled Data Acquisition System

WEIGH SCALE

Figure 44 shows an example of how an AD624 can be used to condition the differential output voltage from a load cell. The 10% reference voltage adjustment range is required to accommodate the 10% transducer sensitivity tolerance. The high linearity and low noise of the AD624 make it ideal for use in applications of this type particularly where it is desirable to measure small changes in weight as opposed to the absolute value. The addition of an auto gain/auto tare cycle will enable the system to remove offsets, gain errors, and drifts making possible true 14-bit performance.

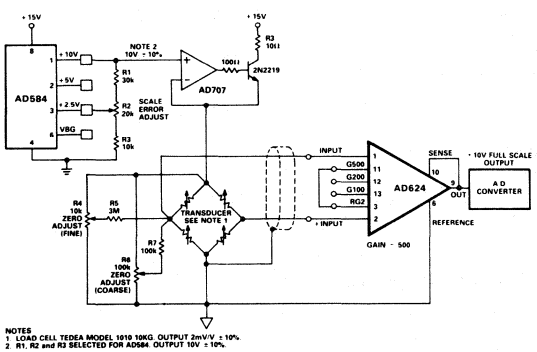


Figure 44. AD624 Weigh Scale Application

AC BRIDGE

Bridge circuits which use dc excitation are often plagued by errors caused by thermocouple effects, 1/f noise, dc drifts in the electronics, and line noise pick-up. One way to get around these problems is to excite the bridge with an ac waveform, amplify the bridge output with an ac amplifier, and synchronously demodulate the resulting signal. The ac phase and amplitude information from the bridge is recovered as a dc signal at the output of the synchronous demodulator. The low frequency system noise, dc drifts, and demodulator noise all get mixed to the carrier frequency and can be removed by means of a low pass filter. Dynamic response of the bridge must be traded off against the amount of attenuation required to adequately suppress these residual carrier components in the selection of the filter.

Figure 45 is an example of an ac bridge system with the AD630 used as a synchronous demodulator. The oscilloscope photograph shows the results of a 0.05% bridge imbalance caused by the 1Meg resistor in parallel with one leg of the bridge. The top trace represents the bridge excitation, the upper middle trace is the amplified bridge output, the lower-middle trace is the output of the synchronous demodulator and the bottom trace is the filtered dc system output.

This system can easily resolve a 0.5ppm change in bridge impedance. Such a change will produce a 6.3mV change in the low pass filtered dc output, well above the RTO drifts and noise.

The AC-CMRR of the AD624 decreases with the frequency of the input signal. This is due mainly to the package-pin capacitance associated with the AD624's internal gain resistors. If AC-CMRR is not sufficient for a given application, it can be trimmed by using a variable capacitor connected to the amplifier's RG_2 pin as shown in Figure 45.

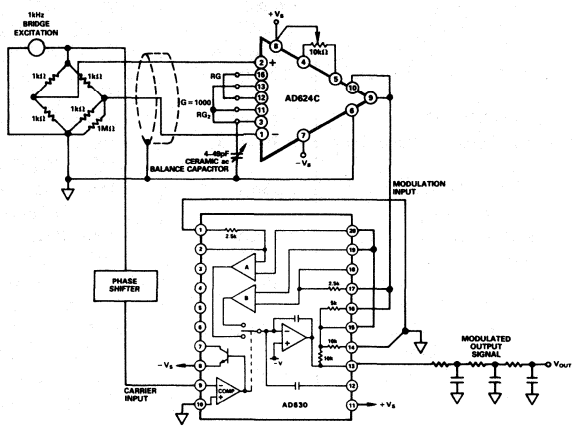


Figure 45. AC Bridge

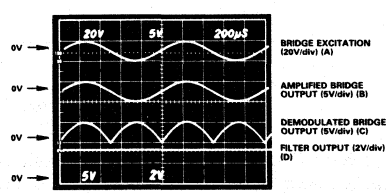


Figure 46. AC Bridge Waveforms

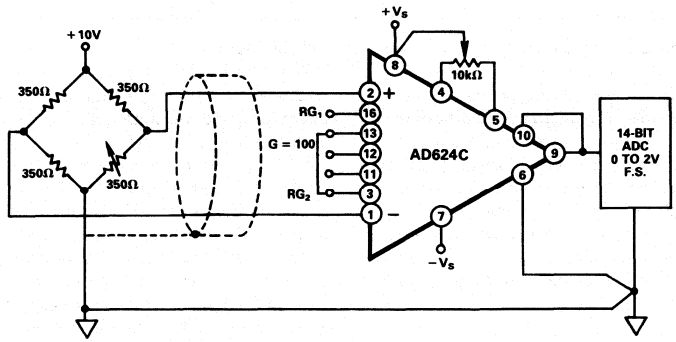


Figure 47. Typical Bridge Application

ERROR BUDGET ANALYSIS

To illustrate how instrumentation amplifier specifications are applied, we will now examine a typical case where an AD624 is required to amplify the output of an unbalanced transducer. Figure 47 shows a differential transducer, unbalanced by ≈5Ω, supplying a 0 to 20mV signal to an AD624C. The output of the IA feeds a 14-bit A to D converter with a 0 to 2 volt input voltage range. The operating temperature range is −25°C to +85°C. Therefore, the largest change in temperature ΔT within the operating range is from ambient to +85°C (85°C − 25°C = 60°C).

In many applications, differential linearity and resolution are of prime importance. This would be so in cases where the absolute value of a variable is less important than changes in value. In these applications, only the irreducible errors (20ppm = 0.002%) are significant. Furthermore, if a system has an intelligent processor monitoring the A to D output, the addition of a auto-gain/auto-zero cycle will remove all reducible errors and may eliminate the requirement for initial calibration. This will also reduce errors to 0.002%.

Error Source	AD624C Specifications	Calculation	Effect on Absolute Accuracy at T_A = 25°C	Effect on Absolute Accuracy at T_A = 85°C	Effect on Resolution
Gain Error	±0.1%	±0.1% = 1000ppm	1000ppm	1000ppm	–
Gain Instability	10ppm	(10ppm/°C)(60°C) = 600ppm	–	600ppm	–
Gain Nonlinearity	±0.001%	±0.001% = 10ppm	–	–	10ppm
Input Offset Voltage	±25μV, RTI	±25μV/20mV = ±1250ppm	1250ppm	1250ppm	–
Input Offset Voltage Drift	±0.25μV/°C	(±0.25μV/°C)(60°C) = 15μV 15μV/20mV = 750ppm	–	750ppm	–
Output Offset Voltage[1]	±2.0mV	±2.0mV/20mV = 1000ppm	1000ppm	1000ppm	–
Output Offset Voltage Drift[1]	±10μV/°C	(±10μV/°C)(60°C) = 600μV 600μV/20mV = 300ppm	–	300ppm	–
Bias Current – Source Imbalance Error	±15nA	(±15nA)(5Ω) = 0.075μV 0.075μV/20mV = 3.75ppm	3.75ppm	3.75ppm	–
Offset Current – Source Imbalance Error	±10nA	(±10nA)(5Ω) = 0.050μV 0.050μV/20mV = 2.5ppm	2.5ppm	2.5ppm	–
Offset Current – Source Resistance – Error	±10nA	(10nA)(175Ω) = 1.75μV 1.75μV/20mV = 87.5ppm	87.5ppm	87.5ppm	–
Offset Current – Source Resistance – Drift	±100pA/°C	(100pA/°C)(175Ω)(60°C) = 1μV 1μV/20mV = 50ppm	–	50ppm	–
Common Mode Rejection 5V dc	115dB	115dB = 1.8ppm × 5V = 9μV 9μV/20mV = 444ppm	450ppm	450ppm	–
Noise, RTI (0.1–10Hz)	0.22μV p-p	0.22μV p-p/20mV = 10ppm	–	–	10ppm
		Total Error	3793.75ppm	5493.75ppm	20ppm

[1]Output offset voltage and output offset voltage drift are given as RTI figures.

Table II. Error Budget Analysis of AD624CD in Bridge Application

For a comprehensive study of instrumentation amplifier design and applications, refer to the Instrumentation Amplifier Application Guide, available free from Analog Devices.

ANALOG DEVICES

Programmable Gain Instrumentation Amplifier

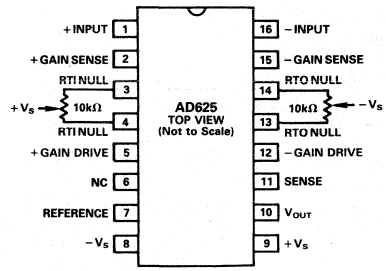
AD625

FEATURES

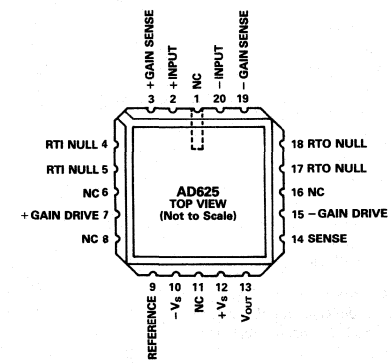
User Programmed Gains of 1 to 10,000
Low Gain Error: 0.02% max
Low Gain TC: 5ppm/°C max
Low Nonlinearity: 0.001% max
Low Offset Voltage: 25μV
Low Noise 4nV/√Hz (at 1kHz) RTI
Gain Bandwidth Product: 25MHz
16-Pin Ceramic or Plastic DIP Package, 20-Pin LCC Package
Standard Military Drawing Available
MIL-Standard Parts Available
Low Cost

CONNECTION DIAGRAMS

Ceramic DIP (D) and Plastic DIP (N) Packages



Leadless Chip Carrier (E) Package



PRODUCT DESCRIPTION

The AD625 is a precision instrumentation amplifier specifically designed to fulfill two major areas of application:
1) Circuits requiring nonstandard gains (i.e., gains not easily achievable with devices such as the AD524 and AD624).
2) Circuits requiring a low cost, precision software programmable gain amplifier.

For low noise, high CMRR, and low drift the AD625JN is the most cost effective instrumentation amplifier solution available. An additional three resistors allow the user to set any gain from 1 to 10,000. The error contribution of the AD625JN is less than 0.05% gain error and under 5ppm/°C gain TC; performance limitations are primarily determined by the external resistors. Common-mode rejection is independent of the feedback resistor matching.

A software programmable gain amplifier (SPGA) can be configured with the addition of a CMOS multiplexer (or other switch network), and a suitable resistor network. Because the ON resistance of the switches is removed from the signal path, an AD625 based SPGA will deliver 12-bit precision, and can be programmed for any set of gains between 1 and 10,000, with completely user selected gain steps.

For the highest precision the AD625C offers an input offset voltage drift of less than 0.25μV/°C, output offset drift below 15μV/°C, and a maximum nonlinearity of 0.001% at G = 1. All grades exhibit excellent ac performance; a 25MHz gain bandwidth product, 5Vμs slew rate and 15μs settling time.

The AD625 is available in three accuracy grades (A, B, C) for industrial (−25°C to +85°C) temperature range, two grades (J, K) for commercial (0 to +70°C) temperature range, and one (S) grade rated over the extended (−55°C to +125°C) temperature range.

PRODUCT HIGHLIGHTS

1. The AD625 affords up to 16-bit precision for user selected fixed gains from 1 to 10,000. Any gain in this range can be programmed by 3 external resistors.
2. A 12-bit software programmable gain amplifier can be configured using the AD625, a CMOS multiplexer and a resistor network. Unlike previous instrumentation amplifier designs, the ON resistance of a CMOS switch does not affect the gain accuracy.
3. The gain accuracy and gain temperature coefficient of the amplifier circuit are primarily dependent on the user selected external resistors.
4. The AD625 provides totally independent input and output offset nulling terminals for high precision applications. This minimizes the effects of offset voltage in gain-ranging applications.
5. The proprietary design of the AD625 provides input voltage noise of 4nV/√Hz at 1kHz.
6. External resistor matching is not required to maintain high common-mode rejection.

AD625—SPECIFICATIONS (typical @ V_S = ±15V, R_L = 2kΩ and T_A = +25°C unless otherwise specified)

Model	AD625A/J/S Min	AD625A/J/S Typ	AD625A/J/S Max	AD625B/K Min	AD625B/K Typ	AD625B/K Max	AD625C Min	AD625C Typ	AD625C Max	Units
GAIN										
Gain Equation		$\frac{2R_F}{R_G}+1$			$\frac{2R_F}{R_G}+1$			$\frac{2R_F}{R_G}+1$		
Gain Range	1		10,000	1		10,000	1		10,000	
Gain Error[1]		±.035	**±0.05**		±0.02	**±0.03**		±0.01	**±0.02**	%
Nonlinearity, Gain = 1-256			±0.005			±0.002			±0.001	%
Gain>256			±0.01			±0.008			±0.005	%
Gain vs. Temp. Gain<1000[1]			5			5			5	ppm/°C
GAIN SENSE INPUT										
Gain Sense Current		300	**500**		150	**250**		50	**100**	nA
vs. Temperature		5	20		2	15		2	10	nA/°C
Gain Sense Offset Current		150	**500**		75	**250**		50	**100**	nA
vs. Temperature		2	15		1	10		1	5	nA/°C
VOLTAGE OFFSET (May be Nulled)										
Input Offset Voltage		50	**200**		25	**50**		10	**25**	µV
vs. Temperature		1	**2/2**		0.25	**0.50/1**		0.1	**0.25**	µV/°C
Output Offset Voltage		4	**5**		2	**3**		1	**2**	mV
vs. Temperature		20	**50/50**		10	**25/40**		10	**15**	µV/°C
Offset Referred to the										
Input vs. Supply										
G = 1	**70**	75		**75**	85		**80**	90		dB
G = 10	85	95		90	100		95	105		dB
G = 100	95	100		105	110		110	120		dB
G = 1000	**100**	110		**110**	120		**115**	140		dB
INPUT CURRENT										
Input Bias Current		±30	**±50**		±20	**±25**		±10	**±15**	nA
vs. Temperature		±50			±50			±50		pA/°C
Input Offset Current		±2	**±35**		±1	**±15**		±1	**±5**	nA
vs. Temperature		±20			±20			±20		pA/°C
INPUT										
Input Impedance										
Differential Resistance		1			1			1		GΩ
Differential Capacitance		4			4			4		pF
Common-Mode Resistance		1			1			1		GΩ
Common-Mode Capacitance		4			4			4		pF
Input Voltage Range										
Differ. Input Linear (V_{DL})[2]	±10			±10			±10			V
Common-Mode Linear (V_{CM})		$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$		
Common-Mode Rejection Ratio dc to 60Hz with 1kΩ Source Imbalance										
G = 1	**70**	75		**75**	85		**80**	90		dB
G = 10	90	95		95	105		100	115		dB
G = 100	100	105		105	115		110	125		dB
G = 1000	**110**	115		**115**	125		**120**	140		dB
OUTPUT RATING		±10V @5mA			±10V @5mA			±10V @5mA		
DYNAMIC RESPONSE										
Small Signal −3dB										
G = 1 (R_F = 20kΩ)		650			650			650		kHz
G = 10		400			400			400		kHz
G = 100		150			150			150		kHz
G = 1000		25			25			25		kHz
Slew Rate		5.0			5.0			5.0		V/µs
Settling Time to 0.01%, 20V Step										
G = 1 to 200		15			15			15		µs
G = 500		35			35			35		µs
G = 1000		75			75			75		µs
NOISE										
Voltage Noise, 1kHz										
R.T.I.		4			4			4		$nV/\sqrt{Hz}$
R.T.O.		75			75			75		$nV/\sqrt{Hz}$
R.T.I., 0.1 to 10Hz										
G = 1		10			10			10		µV p-p
G = 10		1.0			1.0			1.0		µV p-p
G = 100		0.3			0.3			0.3		µV p-p
G = 1000		0.2			0.2			0.2		µV p-p
Current Noise										
0.1Hz to 10Hz		60			60			60		pA p-p

Model	AD625A/J/S Min	AD625A/J/S Typ	AD625A/J/S Max	AD625B/K Min	AD625B/K Typ	AD625B/K Max	AD625C Min	AD625C Typ	AD625C Max	Units
SENSE INPUT										
R_{IN}		10			10			10		kΩ
I_{IN}		30			30			30		μA
Voltage Range	±10			±10			±10			V
Gain to Output		1±0.01			1±0.01			1±0.01		%
REFERENCE INPUT										
R_{IN}		20			20			20		kΩ
I_{IN}		30			30			30		μA
Voltage Range	±10			±10			±10			V
Gain to Output		1±0.01			1±0.01			1±0.01		%
TEMPERATURE RANGE										
Specified Performance										
J/K Grades	0		+70	0		+70				°C
A/B/C Grades	−25		+85	−25		+85	−25		+85	°C
S Grade	−55		+125							
Storage	−65		+150	−65		+150	−65		+150	°C
POWER SUPPLY										
Power Supply Range		±6 to ±18			±6 to ±18			±6 to ±18		V
Quiescent Current		3.5	5		3.5	5		3.5	5	mA

NOTES
[1]Gain Error and Gain TC are for the AD625 only. Resistor network errors will add to the specified errors.
[2]V_{DL} is the maximum differential input voltage at G = 1 for specified nonlinearity.
V_{DL} at other gains = 10V/G.
V_D = actual differential input voltage.
Example: G = 10, V_D = 0.50
V_{CM} = 12V–(10/2 × 0.50V) = 9.5V.

Specifications subject to change without notice.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18V
Internal Power Dissipation 450mW
Input Voltage . . . . . ±V_S
Differential Input Voltage . . . . . ±V_S
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range (D, E) . . . . . −65°C to +150°C
(N) . . . . . −65°C to +125°C
Operating Temperature Range
AD625J/K . . . . . 0 to +70°C
AD625A/B/C . . . . . −25°C to +85°C
AD625S . . . . . −55°C to +125°C
Lead Temperature Range
(Soldering, 60 seconds) . . . . . +300°C

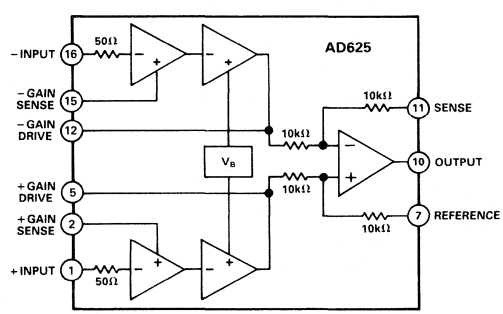
NOTE
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD625AD	−40°C to +85°C	16-Pin Ceramic DIP	D-16
AD625BD	−40°C to +85°C	16-Pin Ceramic DIP	D-16
AD625CD	−40°C to +85°C	16-Pin Ceramic DIP	D-16
AD625SD	−55°C to +125°C	16-Pin Ceramic DIP	D-16
AD625SD/883B	−55°C to +125°C	16-Pin Ceramic DIP	D-16
AD625AE	−40°C to +85°C	20-Pin Leadless Chip Carrier	E-20A
AD625SE/883B	−55°C to +125°C	20-Pin Leadless Chip Carrier	E-20A
AD625JN	−40°C to +85°C	16-Pin Plastic DIP	N-16
AD625KN	−40°C to +85°C	16-Pin Plastic DIP	N-16
AD625AChips	−40°C to +85°C	Die	
AD625CChips	−40°C to +85°C	Die	
AD625SChips	−55°C to +125°C	Die	
5962–8771901EA	Standard Military Drawing Available		

*For outline information see Package Information section.

FUNCTIONAL BLOCK DIAGRAM
("N" AND "D" PACKAGE PINOUT)



AD625—Typical Characteristics

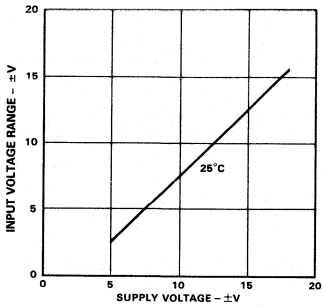


Figure 1. Input Voltage Range vs. Supply Voltage, G = 1

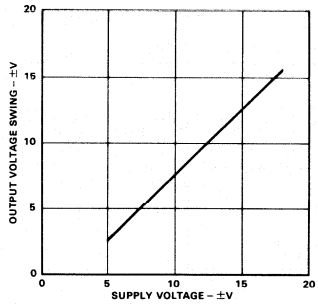


Figure 2. Output Voltage Swing vs. Supply Voltage

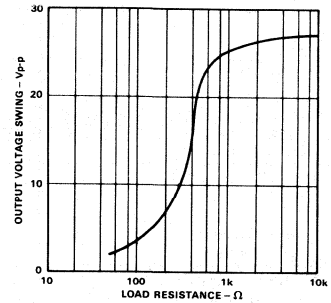


Figure 3. Output Voltage Swing vs. Load Resistance

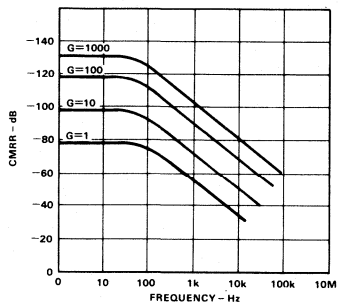


Figure 4. CMRR vs. Frequency RTI, Zero to 1kΩ Source Imbalance

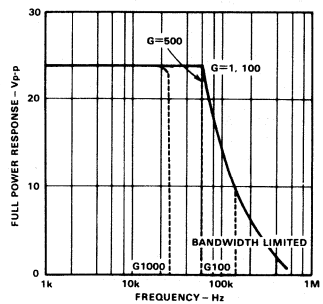


Figure 5. Large Signal Frequency Response

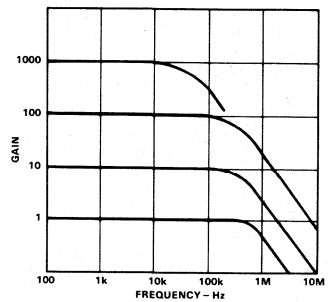


Figure 6. Gain vs. Frequency

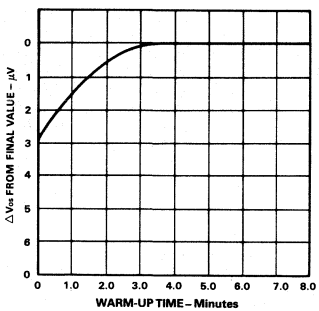


Figure 7. Offset Voltage, RTI, Turn On Drift

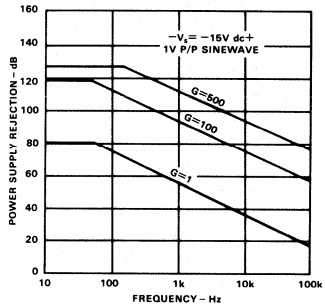


Figure 8. Negative PSRR vs. Frequency

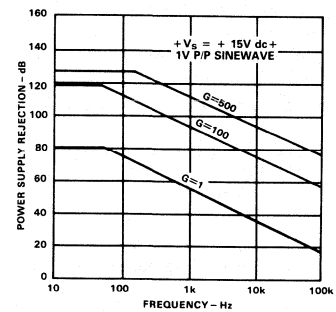


Figure 9. Positive PSRR vs. Frequency

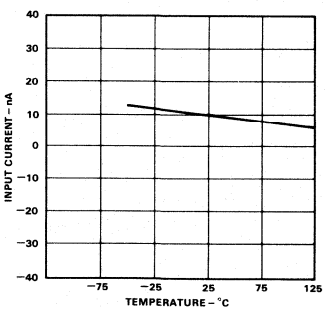


Figure 10. Input Bias Current vs. Temperature

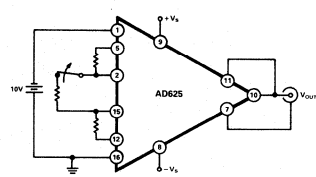


Figure 11. Overrange and Gain Switching Test Circuit (G = 8, G = 1)

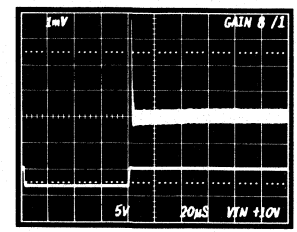


Figure 12. Gain Overrange Recovery

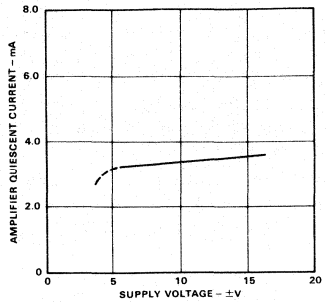


Figure 13. Quiescent Current vs. Supply Voltage

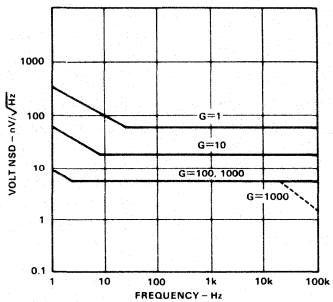


Figure 14. RTI Noise Spectral Density vs. Gain

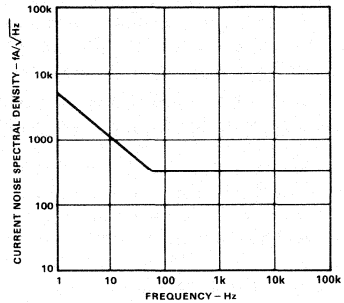


Figure 15. Input Current Noise

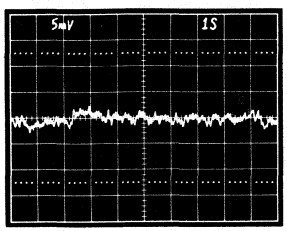


Figure 16. Low Frequency Voltage Noise, G=1 (System Gain=1000)

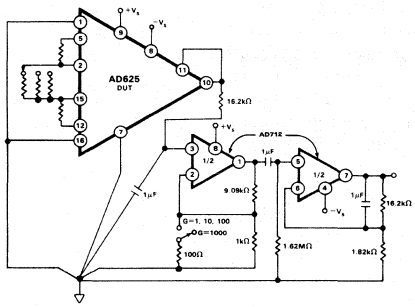


Figure 17. Noise Test Circuit

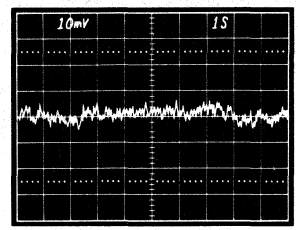


Figure 18. Low Frequency Voltage Noise, G=1000 (System Gain=100,000)

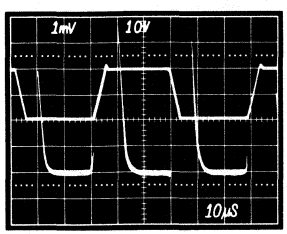


Figure 19. Large Signal Pulse Response and Settling Time, G=1

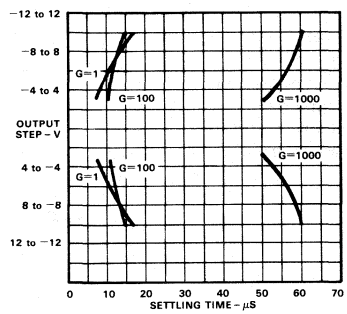


Figure 20. Settling Time to 0.01%

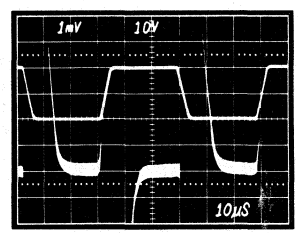


Figure 21. Large Signal Pulse Response and Settling Time, G=100

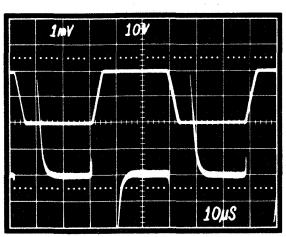


Figure 22. Large Signal Pulse Response and Settling Time, G=10

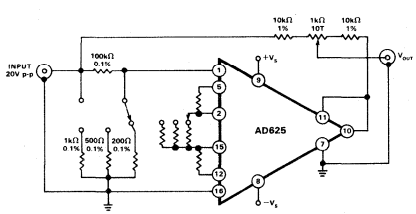


Figure 23. Settling Time Test Circuit

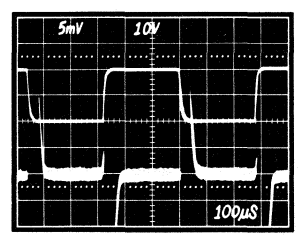


Figure 24. Large Signal Pulse Response and Settling Time, G=1000

AD625—Theory of Operation

The AD625 is a monolithic instrumentation amplifier based on a modification of the classic three-op-amp approach. Monolithic construction and laser-wafer-trimming allow the tight matching and tracking of circuit components. This insures the high level of performance inherent in this circuit architecture.

A preamp section (Q1-Q4) provides additional gain to A1 and A2. Feedback from the outputs of A1 and A2 forces the collector currents of Q1-Q4 to be constant, thereby, impressing the input voltage across R_G. This creates a differential voltage at the outputs of A1 and A2 which is given by the gain ($2R_F/R_G + 1$) times the differential portion of the input voltage. The unity gain subtractor, A3, removes any common-mode signal from the output voltage yielding a single ended output, V_{OUT}, referred to the potential at the reference pin.

The value of R_G is the determining factor of the transconductance of the input preamp stage. As R_G is reduced for larger gains the transconductance increases. This has three important advantages. First, this approach allows the circuit to achieve a very high open-loop gain of (3×10^8 at programmed gains $\geq$ 500) thus reducing gain related errors. Second, the gain-bandwidth product, which is determined by C3, C4, and the input transconductance, increases with gain, thereby, optimizing frequency response. Third, the input voltage noise is reduced to a value determined by the collector current of the input transistors ($4nV/\sqrt{Hz}$).

INPUT PROTECTION

Differential input amplifiers frequently encounter input voltages outside of their linear range of operation. There are two considerations when applying input protection for the AD625; 1) that continuous input current must be limited to less than 10mA and 2) that input voltages must not exceed either supply by more than one diode drop (approximately 0.6V @ 25°C).

Under differential overload conditions there is ($R_G + 100$)Ω in series with two diode drops (approximately 1.2V) between the plus and minus inputs, in either direction. With no external protection and R_G very small (i.e., 40Ω), the maximum overload voltage the AD625 can withstand, continuously, is approximately ±2.5V. Figure 26A shows the external components necessary to protect the AD625 under all overload conditions at any gain.

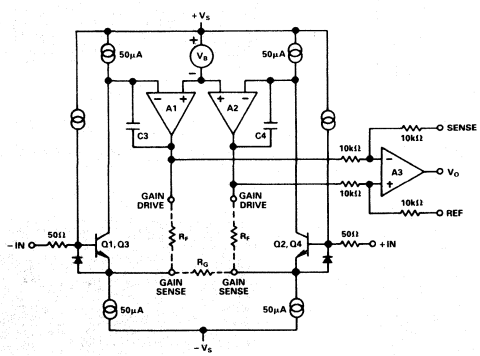


Figure 25. Simplified Circuit of the AD625

The diodes to the supplies are only necessary if input voltages outside of the range of the supplies are encountered. In higher gain applications where differential voltages are small, back-to-back zener diodes and smaller resistors, as shown in Figure 26b, provides adequate protection. Figure 26c shows low cost FETs with a maximum ON resistance of 300Ω configured to offer input protection with minimal degradation to noise, ($5.2nV/\sqrt{Hz}$ compared to normal noise performance of $4nV/\sqrt{Hz}$).

During differential overload conditions, excess current will flow through the gain sense lines (pins 2 and 15). This will have no effect in fixed gain applications. However, if the AD625 is being used in an SPGA application with a CMOS multiplexer, this current should be taken into consideration. The current capabilities of the multiplexer may be the limiting factor in allowable overflow current. The ON resistance of the switch should be included as part of R_G when calculating the necessary input protection resistance.

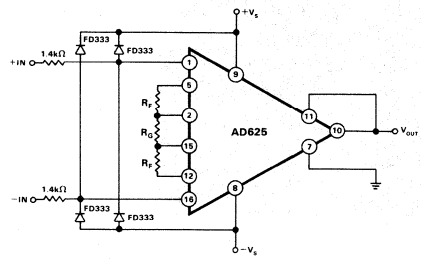


Figure 26a. Input Protection Circuit

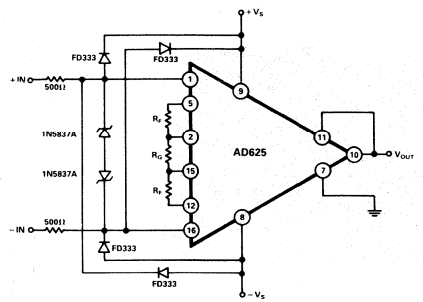


Figure 26b. Input Protection Circuit for G>5

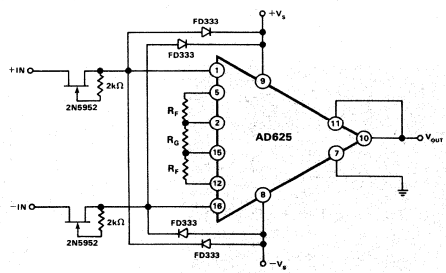


Figure 26c. Input Protection Circuit

Any resistors in series with the inputs of the AD625 will degrade the noise performance. For this reason the circuit in Figure 26b should be used if the gains are all greater than 5. For gains less than 5, either the circuit in Figure 26a or in Figure 26c can be used. The two 1.4kΩ resistors in Figure 26a will degrade the noise performance to:

$$\sqrt{4kTR_{ext} + (4nV/\sqrt{Hz})^2} = 7.9nV/\sqrt{Hz}$$

RESISTOR PROGRAMMABLE GAIN AMPLIFIER

In the resistor-programmed mode (Figure 27), only three external resistors are needed to select any gain from 1 to 10,000. Depending on the application, discrete components or a pretrimmed network can be used. The gain accuracy and gain TC are primarily determined by the external resistors since the AD625C contributes less than 0.02% to gain error and under 5ppm/°C gain TC. The gain sense current is insensitive to common-mode voltage, making the CMRR of the resistor programmed AD625 independent of the match of the two feedback resistors, R_F.

Selecting Resistor Values

As previously stated each R_F provides feedback to the input stage and sets the unity gain transconductance. These feedback resistors are provided by the user. The AD625 is tested and specified with a value of 20kΩ for R_F. Since the magnitude of RTO errors increases with increasing feedback resistance, values much above 20kΩ are not recommended (values below 10kΩ for R_F may lead to instability). Refer to the graph of RTO noise, offset, drift, and bandwidth (Figure 28) when selecting the feedback resistors. The gain resistor (R_G) is determined by the formula $R_G = 2R_F/(G-1)$.

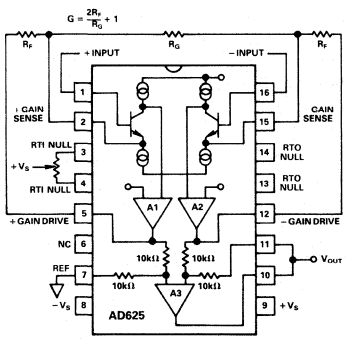


Figure 27. AD625 in Fixed Gain Configuration

A list of standard resistors which can be used to set some common gains is shown in Table I.

For single gain applications, only one offset null adjust is necessary; in these cases the RTI null should be used.

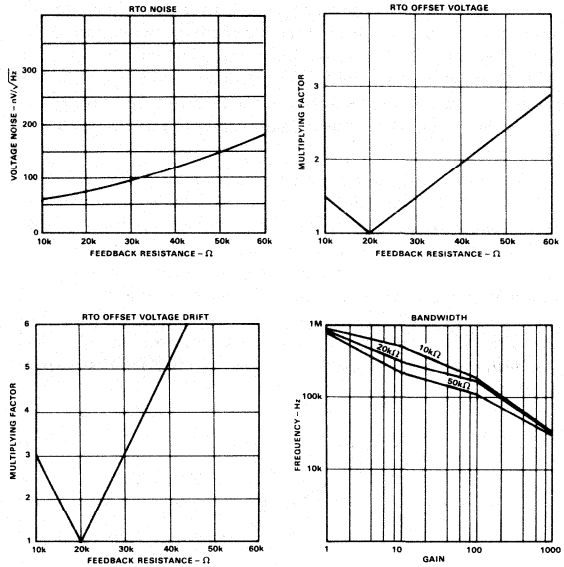


Figure 28. RTO Noise, Offset, Drift, and Bandwidth vs. Feedback Resistance Normalized to 20kΩ

GAIN	R_F	R_G
1	20kΩ	∞
2	19.6kΩ	39.2kΩ
5	20kΩ	10kΩ
10	20kΩ	4.42kΩ
20	20kΩ	2.1kΩ
50	19.6kΩ	806Ω
100	20kΩ	402Ω
200	20.5kΩ	205Ω
500	19.6kΩ	78.7Ω
1000	19.6kΩ	39.2Ω
4	20kΩ	13.3kΩ
8	19.6kΩ	5.62kΩ
16	20kΩ	2.67kΩ
32	19.6kΩ	1.27kΩ
64	20kΩ	634Ω
128	20kΩ	316Ω
256	19.6kΩ	154Ω
512	19.6kΩ	76.8Ω
1024	19.6kΩ	38.3Ω

Table I. Common Gains Nominally within ±0.5% Error Using Standard 1% Resistors

SENSE TERMINAL

The sense terminal is the feedback point for the AD625 output amplifier. Normally it is connected directly to the output. If heavy load currents are to be drawn through long leads, voltage drops through lead resistance can cause errors. In these instances the sense terminal can be wired to the load thus putting the I × R drops "inside the loop" and virtually eliminating this error source.

Typically, IC instrumentation amplifiers are rated for a full ± 10 volt output swing into 2kΩ. In some applications, however, the need exists to drive more current into heavier loads. Figure 29 shows how a high-current booster may be connected "inside the loop" of an instrumentation amplifier. By using an external power boosting circuit, the power dissipated by the AD625 will remain low, thereby, minimizing the errors induced by self-heating. The effects of nonlinearities, offset and gain inaccuracies of the buffer are reduced by the loop gain of the AD625's output amplifier.

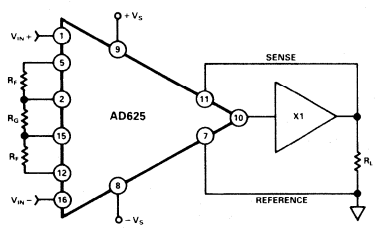


Figure 29. AD625 Instrumentation Amplifier with Output Current Booster

REFERENCE TERMINAL

The reference terminal may be used to offset the output by up to ± 10V. This is useful when the load is "floating" or does not share a ground with the rest of the system. It also provides a direct means of injecting a precise offset. However, it must be remembered that the total output swing is ± 10 volts, from ground, to be shared between signal and reference offset.

The AD625 reference terminal must be presented with nearly zero impedance. Any significant resistance, including those caused by PC layouts or other connection techniques, will increase the gain of the noninverting signal path, thereby, upsetting the common-mode rejection of the In-Amp. Inadvertent thermocouple connections created in the sense and reference lines should also be avoided as they will directly affect the output offset voltage and output offset voltage drift.

In the AD625 a reference source resistance will unbalance the CMR trim by the ratio of $10k\Omega/R_{REF}$. For example, if the reference source impedance is 1Ω, CMR will be reduced to 80dB ($10k\Omega/1\Omega$ = 80dB). An operational amplifier may be used to provide the low impedance reference point as shown in Figure 30. The input offset voltage characteristics of that amplifier will add directly to the output offset voltage performance of the instrumentation amplifier.

The circuit of Figure 30 also shows a CMOS DAC operating in the bipolar mode and connnected to the reference terminal to provide software controllable offset adjustments. The total offset range is equal to $\pm(V_{REF}/2 \times R_5/R_4)$, however, to be symmetrical about 0V $R_3 = 2 \times R_4$.

The offset per bit is equal to the total offset range divided by 2^N, where N = number of bits of the DAC. The range of offset for Figure 30 is ± 120mV, and the offset is incremented in steps of 0.9375mV/LSB.

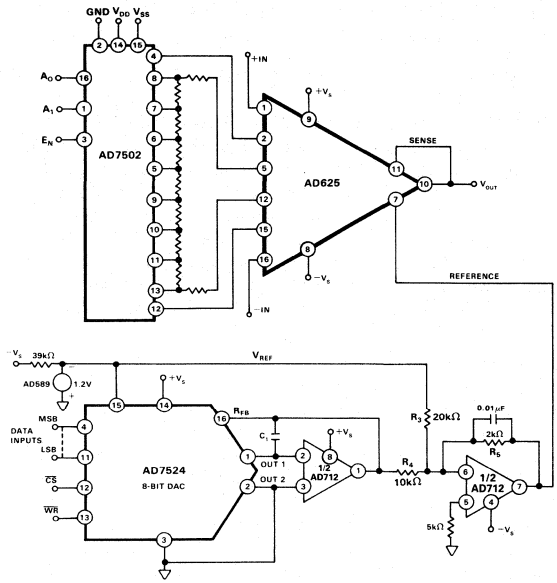


Figure 30. Software Controllable Offset

An instrumentation amplifier can be turned into a voltage-to-current converter by taking advantage of the sense and reference terminals as shown in Figure 31.

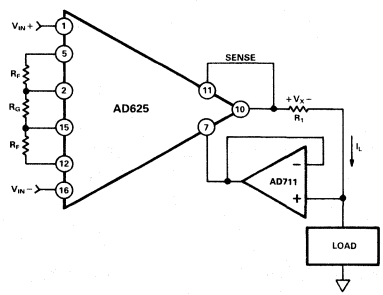


Figure 31. Voltage-to-Current Converter

By establishing a reference at the "low" side of a current setting resistor, an output current may be defined as a function of input voltage, gain and the value of that resistor. Since only a small current is demanded at the input of the buffer amplifier A1, the forced current I_L will largely flow through the load. Offset and drift specifications of A2 must be added to the output offset and drift specifications of the In-Amp.

INPUT AND OUTPUT OFFSET VOLTAGE

Offset voltage specifications are often considered a figure of merit for instrumentation amplifiers. While initial offset may be adjusted to zero, shifts in offset voltage due to temperature variations will cause errors. Intelligent systems can often correct for this factor with an auto-zero cycle, but this requires extra circuitry.

Offset voltage and offset voltage drift each have two components: input and output. Input offset is that component of offset that is generated at the input stage. Measured at the output it is directly proportional to gain, i.e., input offset as measured at the output at G = 100 is 100 times greater than that measured at G = 1. Output offset is generated at the output and is constant for all gains.

The input offset and drift are multiplied by the gain, while the output terms are independent of gain, therefore, input errors dominate at high gains and output errors dominate at low gains. The output offset voltage (and drift) is normally specified at G = 1 (where input effects are insignificant), while input offset (and drift) is given at a high gain (where output effects are negligible). All input-related parameters are specified referred to the input (RTI) which is to say that the effect on the output is "G" times larger. Offset voltage vs. power supply is also specified as an RTI error.

By separating these errors, one can evaluate the total error independent of the gain. For a given gain, both errors can be combined to give a total error referred to the input (RTI) or output (RTO) by the following formula:

Total Error RTI = input error + (output error/gain)

Total Error RTO = (Gain × input error) + output error

The AD625 provides for both input and output offset voltage adjustment. This simplifies nulling in very high perecision applications and minimizes offset voltage effects in switched gain applications. In such applications the input offset is adjusted first at the highest programmed gain, then the output offset is adjusted at G = 1. If only a single null is desired, the input offset null should be used. The most additional drift when using only the input offset null is 0.9μV/°C, RTO.

COMMON-MODE REJECTION

Common-mode rejection is a measure of the change in output voltage when both inputs are changed by equal amounts. These specifications are usually given for a full-range input voltage change and a specified source imbalance.

In an instrumentation amplifier, degradation of common-mode rejection is caused by a differential phase shift due to differences in distributed stray capacitances. In many applications shielded cables are used to minimize noise. This technique can create common-mode rejection errors unless the shield is properly driven. Figures 32 and 33 show active data guards which are configured to improve ac common-mode rejection by "bootstrapping" the capacitances of the input cabling, thus minimizing differential phase shift.

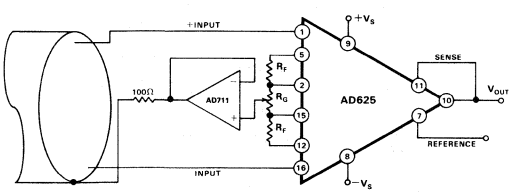


Figure 32. Common-Mode Shield Driver

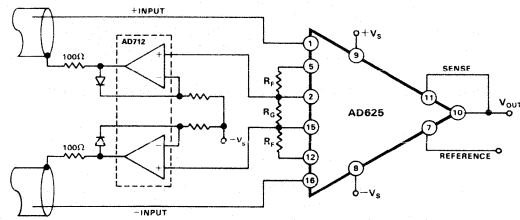


Figure 33. Differential Shield Driver

4

GROUNDING

In order to isolate low level analog signals from a noisy digital environment, many data-acquisition components have two or more ground pins. These grounds must eventually be tied together at one point. It would be convenient to use a single ground line, however, current through ground wires and pc runs of the circuit card can cause hundreds of millivolts of error. Therefore, separate ground returns should be provided to minimize the current flow from the sensitive points to the system ground (see Figure 34). Since the AD625 output voltage is developed with respect to the potential on the reference terminal, it can solve many grounding problems.

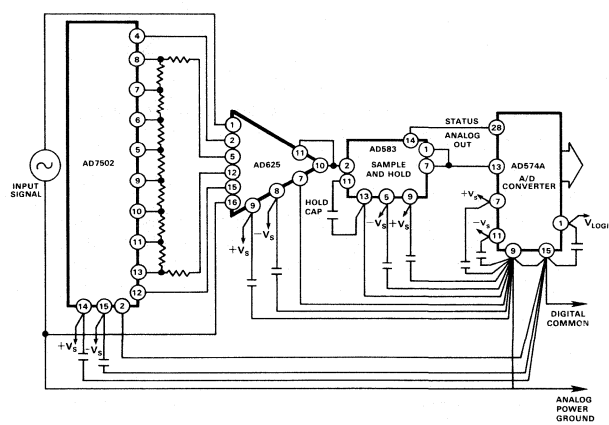


Figure 34. Basic Grounding Practice for a Data Acquisition System

GROUND RETURNS FOR BIAS CURRENTS

Input bias currents are those currents necessary to bias the input transistors of a dc amplifier. There must be a direct return path for these currents, otherwise they will charge external capacitances, causing the output to drift uncontrollably or saturate. Therefore, when amplifying "floating" input sources such as transformers, or ac-coupled sources, there must be a dc path from each input to ground as shown in Figure 35.

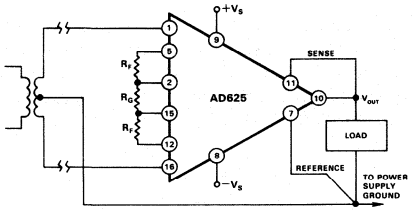


Figure 35a. Ground Returns for Bias Currents with Transformer Coupled Inputs

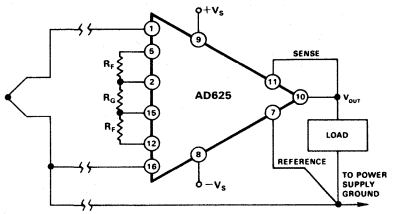


Figure 35b. Ground Returns for Bias Currents with Thermocouple Input

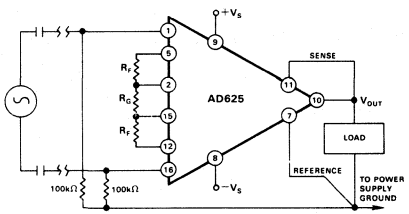


Figure 35c. Ground Returns for Bias Currents with AC Coupled Inputs

AUTO-ZERO CIRCUITS

In many applications it is necessary to maintain high accuracy. At room temperature, offset effects can be nulled by the use of offset trimpots. Over the operating temperature range, however, offset nulling becomes a problem. For these applications the auto-zero circuit of Figure 36 provides a hardware solution.

OTHER CONSIDERATIONS

One of the more overlooked problems in designing ultra-low-drift dc amplifiers is thermocouple induced offset. In a circuit comprised of two dissimilar conductors (i.e., copper, kovar), a current flows when the two junctions are at different temperatures. When this circuit is broken, a voltage known as the "Seebeck" or thermocouple emf can be measured. Standard IC lead material (kovar) and copper form a thermocouple with a high thermoelectric potential (about 35μV°C). This means that care must be taken to insure that all connections (especially those in the input circuit of the AD625) remain isothermal. This includes the input leads (1, 16) and the gain sense lines (2, 15). These pins were chosen for symmetry, helping to desensitize the input circuit to thermal gradients. In addition, the user should also avoid air currents

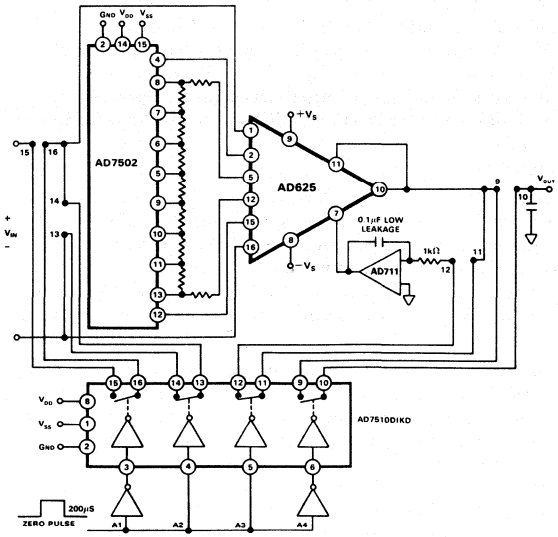


Figure 36. Auto-Zero Circuit

over the circuitry since slowly fluctuating thermocouple voltages will appear as "flicker" noise. In SPGA applications relay contacts and CMOS mux leads are both potential sources of additional thermocouple errors.

The base emitter junction of an input transistor can rectify out of band signals (i.e., RF interference). When amplifying small signals, these rectified voltages act as small dc offset errors. The AD625 allows direct access to the input transistors' bases and emitters enabling the user to apply some first order filtering to these unwanted signals. In Figure 37, the RC time constant should be chosen for desired attenuation of the interfering signals. In the case of a resistive transducer, the capacitance alone working against the internal resistance of the transducer may suffice.

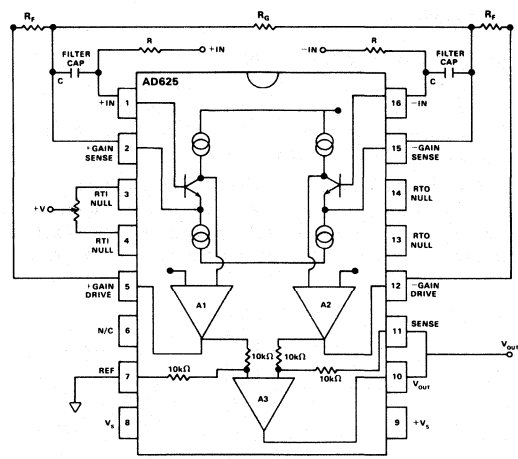


Figure 37. Circuit to Attenuate RF Interference

These capacitances may also be incorporated as part of the external input protection circuit (see section on input protection). As a general practice every effort should be made to match the extraneous capacitance at pins 15 and 2, and pins 1 and 16, to preserve high ac CMR.

SOFTWARE PROGRAMMABLE GAIN AMPLIFIER

An SPGA provides the ability to externally program precision gains from digital inputs. Historically, the problem in systems requiring electronic switching of gains has been the ON resistance (R_{ON}) of the multiplexer, which appears in series with the gain setting resistor R_G. This can result in substantial gain errors and gain drifts. The AD625 eliminates this problem by making the gain drive and gain sense pins available (pins 2, 15, 5, 12; see Figure 39). Consequently the multiplexer's ON resistance is removed from the signal current path. This transforms the ON resistance error into a small nullable offset error. To clarify this point, an error budget analysis has been performed in Table II based on the SPGA configuration shown in Figure 39.

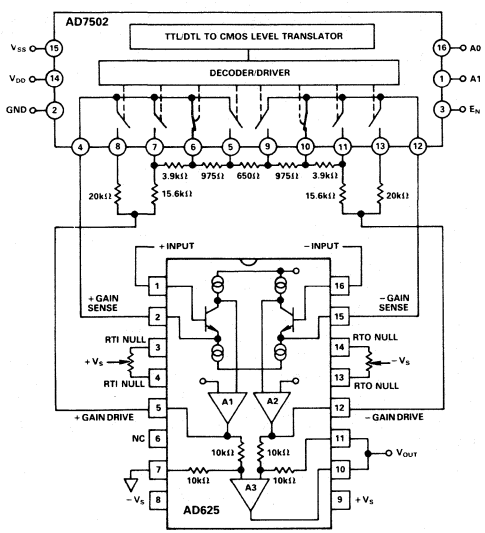


Figure 38. SPGA in a Gain of 16

Figure 38 shows an AD625 based SPGA with possible gains of 1, 4, 16, 64. R_G equals the resistance between the gain sense lines (pins 2 and 15) of the AD625. In Figure 38, R_G equals the sum of the two 975Ω resistors and the 650Ω resistor, or 2600Ω. R_F equals the resistance between the gain sense and the gain drive pins (pins 12 and 15, or pins 2 and 5), that is R_F equals the 15.6kΩ resistor plus the 3.9kΩ resistor, or 19.5kΩ. The gain, therefore equals:

$$\frac{2R_F}{R_G} + 1 = \frac{2(19.5k\Omega)}{(2.6k\Omega)} + 1 = 16$$

As the switches of the differential multiplexer proceed synchronously, R_G and R_F change, resulting in the various programmed gain settings.

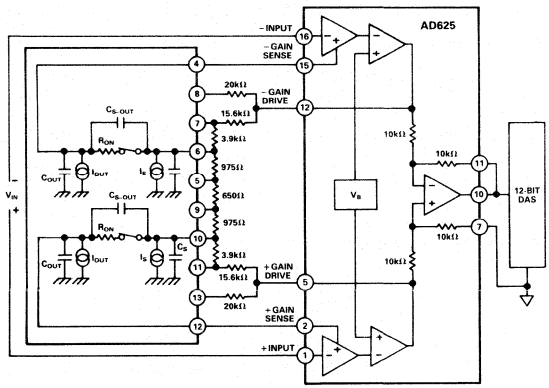


Figure 39. SPGA with Multiplexer Error Sources

Figure 39 shows a complete SPGA feeding a 12-bit DAS with a 0–10V input range. This configuration was used in the error budget analysis shown in Table II. The gain used for the RTI calculations is set at 16. As the gain is changed, the ON resistance of the multiplexer and the feedback resistance will change, which will slightly alter the values in the table.

Induced Error	Specification AD625C	Specification AD7502KN	Calculation	Voltage Offset Induced RTI
RTI Offset Voltage	Gain Sense Offset Current 40nA	Switch Resistance 170Ω	40nA × 170Ω = 6.8μV	6.8μV
RTI Offset Voltage	Gain Sense Current 60nA	Differential Switch Resistance 6.8Ω	60nA × 6.8Ω = 0.41μV	0.41μV
RTO Offset Voltage	Feedback Resistance 20kΩ[1]	Differential Leakage Current (I_S)[2] +0.2nA −0.2nA	2(0.2nA × 20kΩ) = 8μV/16	0.5μV
RTO Offset Voltage	Feedback Resistance 20kΩ[1]	Differential Leakage Current (I_{OUT})[2] +1nA −1nA	2(1nA × 20kΩ) = 40μV/16	2.5μV
Total error induced by a typical CMOS multiplexer to an SPGA at 25°C				**10.21μV**

NOTES

[1]The resistor for this calculation is the user provided feedback resistance (R_F). 20kΩ is recommended value (see resistor programmable gain amplifier section).

[2]The leakage currents (I_S and I_{OUT}) will induce an offset voltage, however, the offset will be determined by the difference between the leakages of each "half" of the differential multiplexer. The differential leakage current is multiplied by the feedback resistance (see Note 1),to determine offset voltage. Because differential leakage curent is not a parameter specified on multiplexer data sheets, the most extreme difference (one most positive and one most negative) was used for the calculations in Table II. Typical performance will be much better.

*The frequency response and settling will be affected by the ON resistance and internal capacitance of the multiplexer. Figure 40 shows the settling time vs. ON resistance at different gain settings for an AD625 based SPGA.

**Switch resistance and leakage current errors can be reduced by using relays.

Table II. Errors Induced by Multiplexer to an SPGA

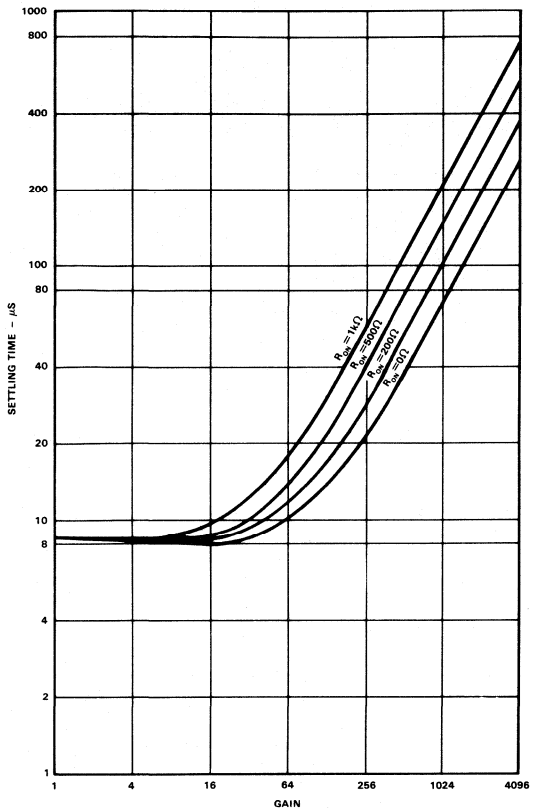


Figure 40. Settling Time to 0.01% of a 20V Step Input for SPGA with AD625

DETERMINING SPGA RESISTOR NETWORK VALUES

The individual resistors in the gain network can be calculated sequentially using the formula given below. The equation determines the resistors as labeled in Figure 41. The feedback resistors and the gain setting resistors are interactive, therefore; the formula must be a series where the present term is dependent on the preceding term(s). The formula

$$R_{F_{i+1}} = (20k\Omega - \sum_{j=0}^{i} R_{F_j})\left(1 - \frac{G_i}{G_{i+1}}\right) \qquad \begin{matrix} G_0 = 1 \\ R_{F_0} = 0 \end{matrix}$$

can be used to calculate the necessary feedback resistors for any set of gains. This formula yields a network with a total resistance of 40kΩ. A dummy variable (j) serves as a counter to keep a running total of the preceding feedback resistors. To illustrate how the formula can be applied, an example similar to the calculation used for the resistor network in Figure 38 is examined below.

1) Unity gain is treated as a separate case. It is implemented with separate 20kΩ feedback resistors as shown in Figure 41. It is then ignored in further calculations.

2) Before making any calculations it is advised to draw a resistor network similar to the network in Figure 41. The network will have (2 × M) + 1 resistors, where M = number of gains. For Figure 38 M = 3 (4, 16, 64), therefore, the resistor string will have 7 resistors (plus the two 20kΩ "side" resistors for unity gain).

3) Begin all calculations with $G_0 = 1$ and $R_{F_0} = 0$.

$R_{F_1} = (20k\Omega - R_{F_0})\,(1 - 1/4)$: $R_{F_0} = 0 \therefore R_{F_1} = 15k\Omega$

$R_{F_2} = [20k\Omega - (R_{F_0} + R_{F_1})]\,(1 - 4/16)$:

$R_{F_0} + R_{F_1} = 15k\Omega \therefore R_{F_2} = 3.75k\Omega$

$R_{F_3} = [20k\Omega - (R_{F_0} + R_{F_1} + R_{F_2})]\,(1 - 16/64)$:

$R_{F_0} + R_{F_1} + R_{F_2} = 18.75k\Omega \therefore R_{F_3} = 937.5\Omega$

4) The center resistor (R_G of the highest gain setting), is determined last. Its value is the remaining resistance of the 40kΩ string, and can be calculated with the equation:

$$R_G = (40k\Omega - 2\sum_{j=0}^{M} R_{F_j})$$

$$R_G = 40k\Omega - 2(R_{F_0} + R_{F_1} + R_{F_2} + R_{F_3})$$

$$40k\Omega - 39.375k\Omega = 625\Omega$$

5) If different resistor values are desired, all the resistors in the network can be scaled by some convenient factor. However, raising the impedance will increase the RTO errors, lowering the total network resistance below 20kΩ can result in amplifier instability. More information on this phenomenon is given in the RPGA section of the data sheet. The scale factor will not affect the unity gain feedback resistors. The resistor network in Figure 38 has a scaling factor of 650/625 = 1.04, if this factor is used on R_{F_1}, R_{F_2}, R_{F_3}, and R_G, then the resistor values will match exactly.

6) Round off errors can be cumulative, therefore, it is advised to carry as many significant digits as possible until all the values have been calculated.

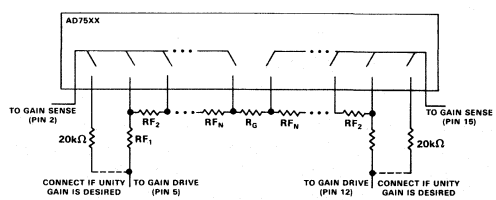


Figure 41. Resistors for a Gain Setting Network

Low Cost, Single Supply Differential Amplifier

AD626

FEATURES

Pin Selectable Gains of 10 and 100
True Single Supply Operation
- **Single Supply Range of +2.4 V to +10 V**
- **Dual Suppy Range of ±1.2 V to ±6 V**
- **Wide Output Voltage Range of 30 mV to 4.7 V**

Optional Low-Pass Filtering
Excellent DC Performance
- **Low Input Offset Voltage: 500 μV max**
- **Large Common-Mode Range: 0 V to +54 V**
- **Low Power: 1.2 mW (V_S = +5 V)**
- **Good CMR of 90 dB typ**

AC Performance
- **Fast Settling Time: 24 μs (0.01%)**

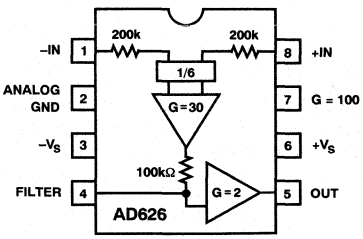
Includes Input Protection
- **Series Resistive Inputs (R_{IN} = 200 kΩ)**
- **RFI Filters Included**
- **Allows 50 V Continuous Overload**

APPLICATIONS

Current Sensing
Interface for Pressure Transducers, Position Indicators, Strain Gages, and Other Low Level Signal Sources

CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP (N) and SOIC (R) Packages



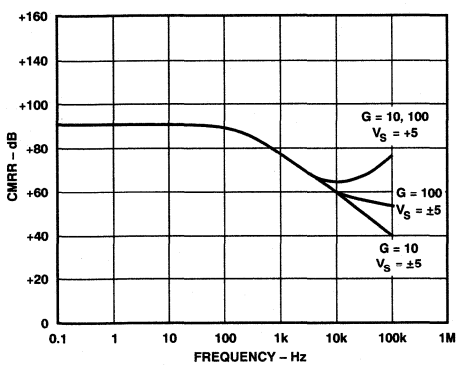
PRODUCT DESCRIPTION

The AD626 is a low cost, true single supply differential amplifier designed for amplifying and low-pass filtering small differential voltages from sources having a large common-mode voltage.

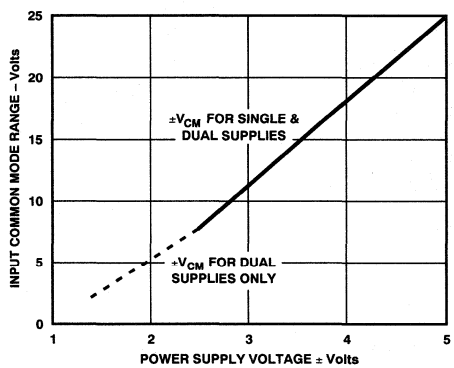
The AD626 can operate from either a single supply of +2.4 V to +10 V, or dual supplies of ±1.2 V to ±6 V. The input common-mode range of this amplifier is equal to 6 (+V_S −1 V) which provides a +24 V CMR while operating from a +5 V supply. Furthermore, the AD626 features a CMR of 90 dB typ.

The amplifier's inputs are protected against continuous overload of up to 50 V, and RFI filters are included in the attenuator network. The output range is +0.03 V to +4.9 V using a +5 V supply. The amplifier provides a preset gain of 10, but gains between 10 to 100 can be easily configured with an external resistor. Furthermore, a gain of 100 is available by connecting the G = 100 pin to analog ground. The AD626 also offers low- pass filter capability by connecting a capacitor between the filter pin and analog ground.

The AD626A and AD626B operate over the industrial temperature range of −40°C to +85°C. The AD626 is available in two 8-pin packages: a plastic mini-DIP and SOIC.



Common-Mode Rejection vs. Frequency



Input Common-Mode Range vs. Supply

AD626—SPECIFICATIONS

SINGLE SUPPLY (@ $+V_S$ = +5 V and T_A = +25°C)

Model	Conditions	AD626A Min	AD626A Typ	AD626A Max	AD626B Min	AD626B Typ	AD626B Max	Units
GAIN								
Gain Accuracy	Total Error							
Gain = 10	@ V_{OUT} ≥ 100 mV dc		0.04	1.0		0.2	0.6	%
Gain = 100	@ V_{OUT} ≥ 100 mV dc		0.1	1.0		0.5	0.6	%
Over Temperature, T_A = T_{MIN}–T_{MAX}	G = 10			50			30	ppm/°C
	G = 100			150			120	ppm/°C
Gain Linearity								
Gain = 10	@ V_{OUT} ≥ 100 mV dc		0.014	0.016		0.014	0.016	%
Gain = 100	@ V_{OUT} ≥ 100 mV dc		0.014	0.02		0.014	0.02	%
OFFSET VOLTAGE								
Input Offset Voltage			1.9	2.5		1.9	2.5	mV
vs. Temperature	T_{MIN}–T_{MAX}, G = 10 or 100			2.9			2.9	mV
vs. Temperature	T_{MIN}–T_{MAX}, G = 10 or 100			6			6	µV/°C
vs. Supply Voltage (PSR)								
+PSR		74	80		74	80		dB
–PSR		64	66		64	66		dB
COMMON-MODE REJECTION	R_L = 10 kΩ							
+CMR Gain = 10, 100	f = 100 Hz, V_{CM} = +24 V	66	90		80	90		dB
±CMR Gain = 10, 100	f = 10 kHz, V_{CM} = 6 V	55	64		55	64		dB
–CMR Gain = 10, 100[1]	f = 100 Hz, V_{CM} = –2 V	60	85		73	85		dB
COMMON-MODE VOLTAGE RANGE								
+CMV Gain = 10	CMR > 85 dB		+24			+24		V
–CMV Gain = 10	CMR > 85 dB		–2			–2		V
INPUT								
Input Resistance								
Differential			200			200		kΩ
Common Mode			100			100		kΩ
Input Voltage Range (Common Mode)			6 (V_S–1)			6 (V_S–1)		V
OUTPUT								
Output Voltage Swing	R_L = 10 kΩ							
Positive	Gain = 10	4.7	4.90		4.7	4.90		V
	Gain = 100	4.7	4.90		4.7	4.90		V
Negative	Gain = 10	0.03			0.03			V
	Gain = 100	0.03			0.03			V
Short Circuit Current								
$+I_{SC}$			12			12		mA
NOISE								
Voltage Noise RTI								
Gain = 10	f = 0.1 Hz–10 Hz		2			2		µV p–p
Gain = 100	f = 0.1 Hz–10 Hz		2			2		µV p–p
Gain = 10	f = 1 kHz		0.25			0.25		$\mu V/\sqrt{Hz}$
Gain = 100	f = 1 kHz		0.25			0.25		$\mu V/\sqrt{Hz}$
DYNAMIC RESPONSE								
–3 dB Bandwidth	V_{OUT} = +1 V dc		100			100		kHz
Slew Rate, T_{MIN} to T_{MAX}	Gain = 10	0.17	0.22		0.17	0.22		V/µs
	Gain = 100	0.1	0.17		0.1	0.17		V/µs
Settling Time	to 0.01%, 1 V Step		24			22		µs
POWER SUPPLY								
Operating Range	T_A = T_{MIN}–T_{MAX}	2.4	5	10	2.4	5	10	V
Quiescent Current	Gain = 10		0.16	0.20		0.16	0.20	mA
	Gain = 100		0.23	0.29		0.23	0.29	mA
TRANSISTOR COUNT	# of Transistors		46			46		

NOTES

[1]At temperatures above +25°C, –CMV degrades at the rate of 12 mV/°C; i.e., @ +25°C CMV = –2 V, @ +85°C CMV = –1.28 V.

Specifications subject to change without notice.

DUAL SUPPLY (@ $+V_S$ = ±5 V and T_A = +25°C)

Model	Conditions	AD626A Min	AD626A Typ	AD626A Max	AD626B Min	AD626B Typ	AD626B Max	Units
GAIN								
Gain Accuracy	Total Error							
Gain = 10	R_L = 10 kΩ		0.2	0.5		0.1	0.3	%
Gain = 100			0.25	1.0		0.15	0.6	%
Over Temperature, $T_A = T_{MIN}$–T_{MAX}								
	G = 10			50			30	ppm/°C
	G = 100			100			80	ppm/°C
Gain Linearity								
Gain = 10			0.045	0.055		0.045	0.055	%
Gain = 100			0.01	0.015		0.01	0.015	%
OFFSET VOLTAGE								
Input Offset Voltage			50	500		50	250	μV
vs. Temperature	T_{MIN}–T_{MAX}, G = 10 or 100			1.0			0.5	mV
vs. Temperature	T_{MIN}–T_{MAX}, G = 10 or 100		1.0			0.5		μV/°C
vs. Supply Voltage (PSR)								
+PSR		74	80		74	80		dB
−PSR		64	66		64	66		dB
COMMON-MODE REJECTION	R_L = 10 kΩ							
±CMR Gain = 10, 100	f = 100 Hz, V_{CM} = 24 V	66	90		80	90		dB
±CMR Gain = 10, 100	f = 10 kHz, V_{CM} = 6 V	55	60		55	60		dB
COMMON-MODE VOLTAGE RANGE								
+CMV Gain = 10	CMR > 85 dB		26.5			26.5		V
−CMV Gain = 10	CMR > 85 dB		32.5			32.5		V
INPUT								
Input Resistance								
Differential			200			200		kΩ
Common Mode			110			110		kΩ
Input Voltage Range (Common Mode)			6 (V_S−1)			6 (V_S−1)		V
OUTPUT								
Output Voltage Swing	R_L = 10 kΩ							
Positive	Gain = 10, 100	4.7	4.90		4.7	4.90		V
Negative	Gain = 10	1.65	2.1		1.65	2.1		V
	Gain = 100	1.45	1.8		1.45	1.8		V
Short Circuit Current								
$+I_{SC}$			12			12		mA
$-I_{SC}$			0.5			0.5		mA
NOISE								
Voltage Noise RTI								
Gain = 10	f = 0.1 Hz–10 Hz		2			2		μV p–p
Gain = 100	f = 0.1 Hz–10 Hz		2			2		μV p–p
Gain = 10	f = 1 kHz		0.25			0.25		$\mu V/\sqrt{Hz}$
Gain = 100	f = 1 kHz		0.25			0.25		$\mu V/\sqrt{Hz}$
DYNAMIC RESPONSE								
−3 dB Bandwidth	V_{OUT} = +1 V dc		100			100		kHz
Slew Rate, T_{MIN} to T_{MAX}	Gain = 10	0.17	0.22		0.17	0.22		V/μs
	Gain = 100	0.1	0.17		0.1	0.17		V/μs
Settling Time	to 0.01%, 2 V Step		24			24		μs
POWER SUPPLY								
Operating Range	$T_A = T_{MIN}$–T_{MAX}	±1.2	±5	±6	±1.2	±5	±6	V
Quiescent Current	Gain = 10		1.5	2		1.5	2	mA
	Gain = 100		1.5	2		1.5	2	mA
TRANSISTOR COUNT	# of Transistors		46			46		

4

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . +36 V
Internal Power Dissipation[2]
Peak Input Voltage . . . . . 60 V
Maximum Reversed Supply Voltage Limit . . . . . −34 V
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range (N, R) . . . . . −65°C to +125°C
Operating Temperature Range
AD626A/B . . . . . −40°C to +85°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]8-Pin Plastic Package: θ_{JA} = 100°C/Watt, θ_{JC} = 50°C/Watt
8-Pin Plastic SOIC Package: θ_{JA} = 160°C/Watt, θ_{JC} = 42°C/Watt

ESD SUSCEPTIBILITY

An ESD classification per method 3015.6 of MIL STD 883C has been performed on the AD626, which is a Class 1 device.

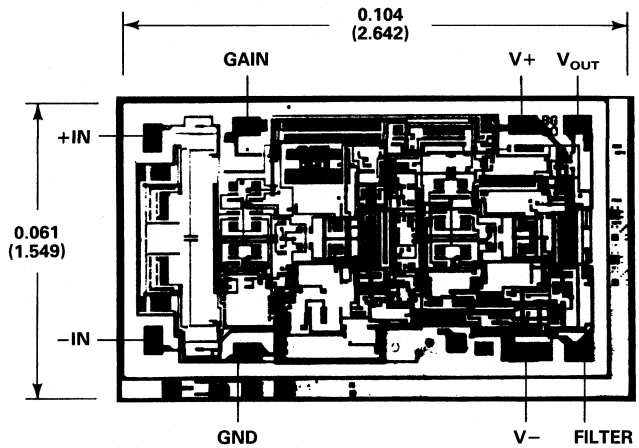
ORDERING GUIDE

Model	Temperature Range	Package Options*
AD626AN	−40°C to +85°C	N-8
AD626AR	−40°C to +85°C	R-8
AD626BN	−40°C to +85°C	N-8

*N = Plastic DIP; R = Small Outline IC. For outline information see Package Information section.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



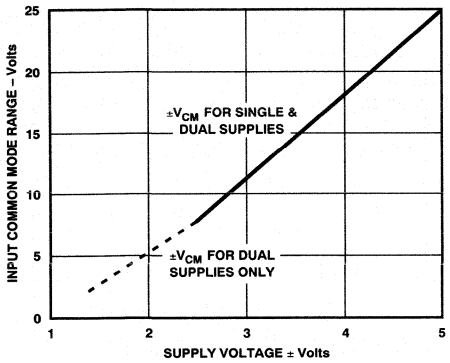


Figure 1. Input Common-Mode Range vs. Supply

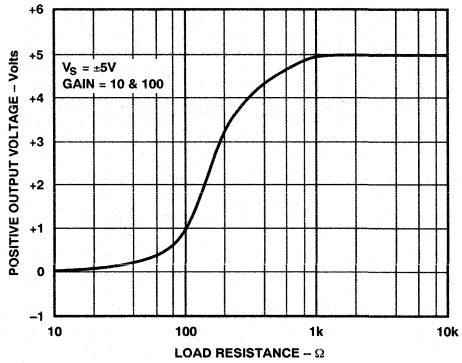


Figure 4. Positive Output Voltage Swing vs. Resistive Load

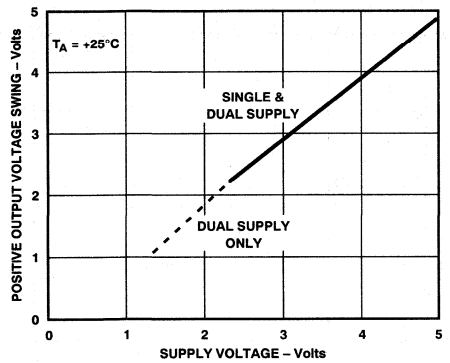


Figure 2. Positive Output Voltage Swing vs. Supply Voltage

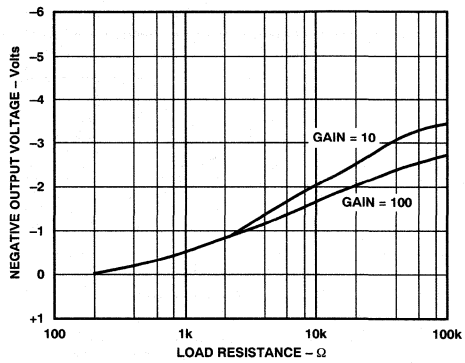


Figure 5. Negative Output Voltage Swing vs. Resistive Load

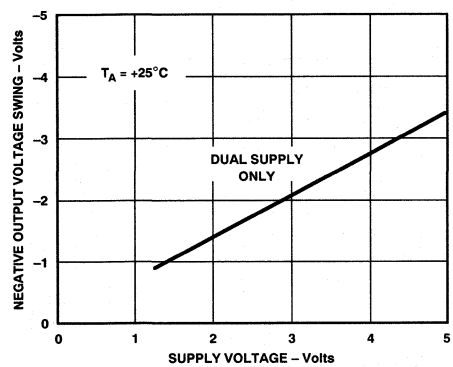


Figure 3. Negative Output Voltage Swing vs. Supply Voltage

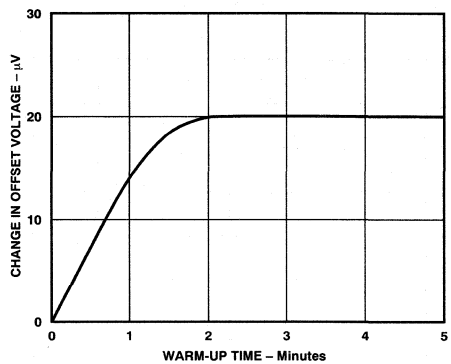


Figure 6. Change in Input Offset Voltage vs. Warm-Up Time

AD626—Typical Characteristics

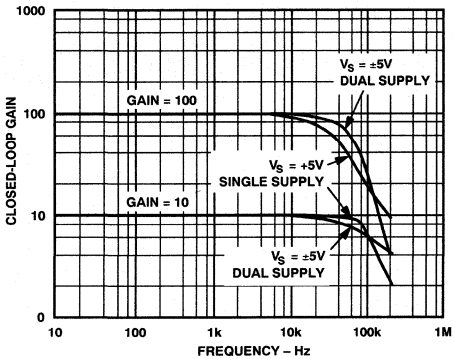


Figure 7. Closed-Loop Gain vs. Frequency

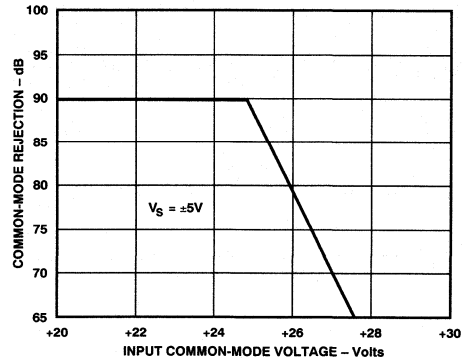


Figure 10. Common-Mode Rejection vs. Input Common-Mode Voltage for Dual Supply Operation

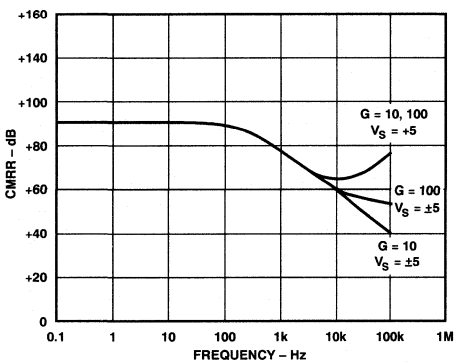


Figure 8. Common-Mode Rejection vs. Frequency

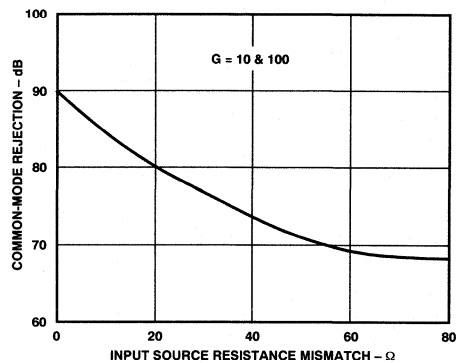


Figure 11. Common-Mode Rejection vs. Input Source Resistance Mismatch

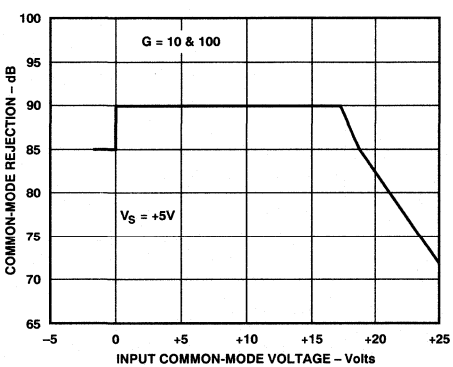


Figure 9. Common-Mode Rejection vs. Input Common-Mode Voltage for Single Supply Operation

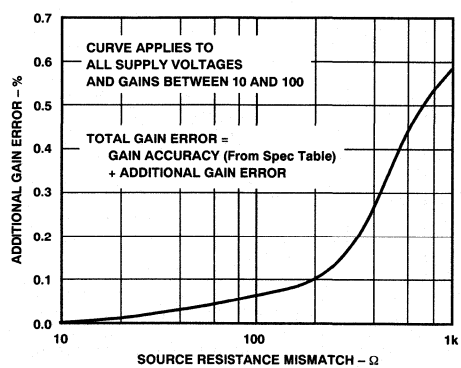


Figure 12. Additional Gain Error vs. Source Resistance Mismatch

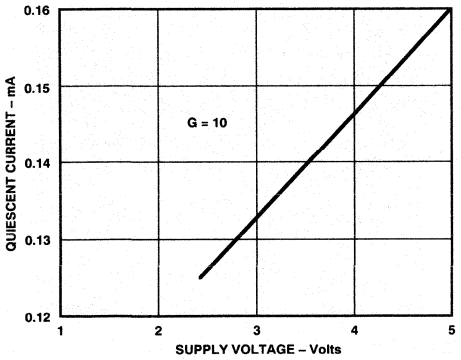


Figure 13. Quiescent Supply Current vs. Supply Voltage for Single Supply Operation

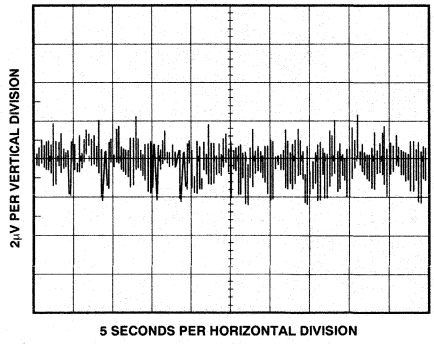


Figure 16. 0.1 Hz to 10 Hz RTI Voltage Noise. V_S = ±5 V, Gain = 100

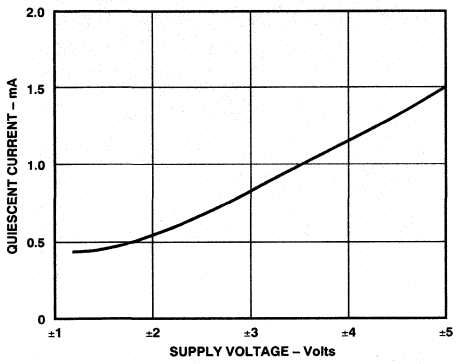


Figure 14. Quiescent Supply Current vs. Supply Voltage for Dual Supply Operation

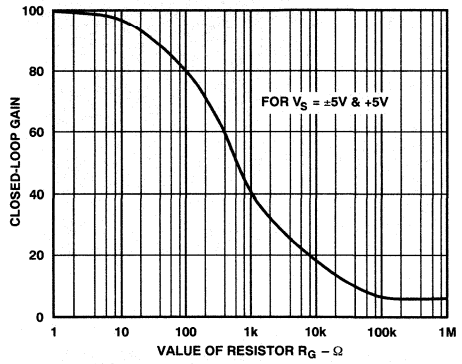


Figure 17. Closed-Loop Gain vs. R_G

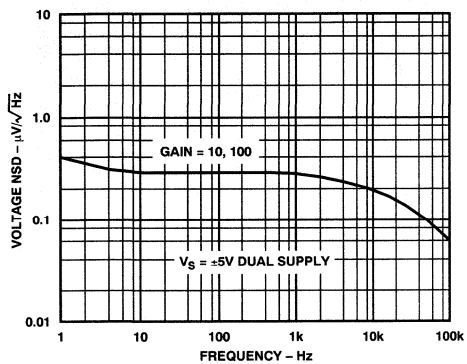


Figure 15. Noise Voltage Spectral Density vs. Frequency

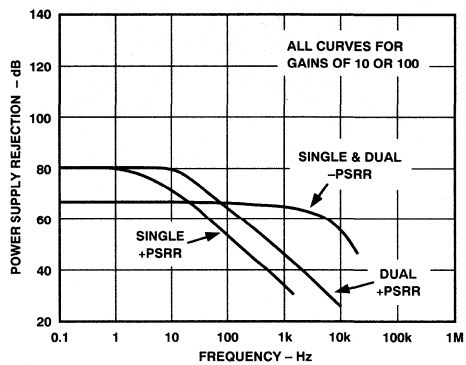


Figure 18. Power Supply Rejection vs. Frequency

AD626—Typical Characteristics

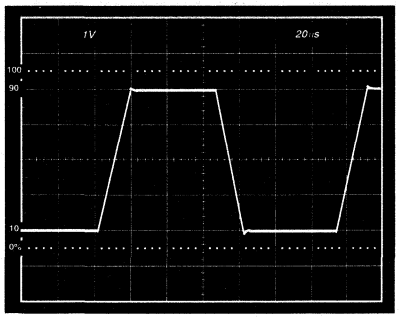


Figure 19. Large Signal Pulse Response. V_S = ±5 V, G = 10

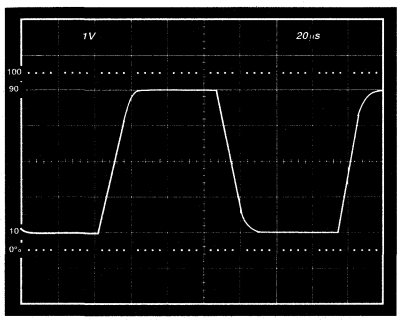


Figure 20. Large Signal Pulse Response. V_S = ±5 V, G = 100

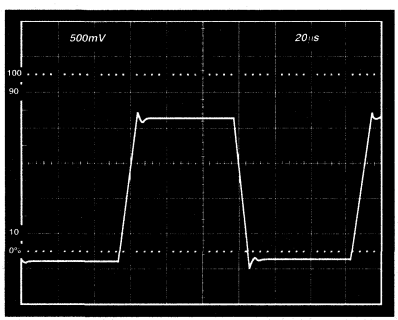


Figure 21. Large Signal Pulse Response. V_S = +5 V, G = 10

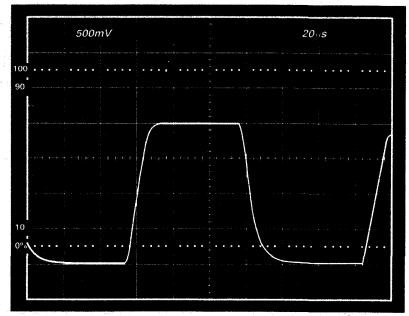


Figure 22. Large Signal Pulse Response. V_S = +5 V, G = 100

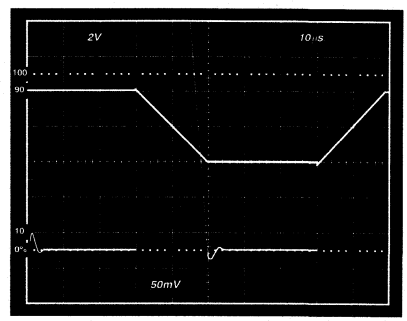


Figure 23. Settling Time. V_S = ±5 V, G = 10

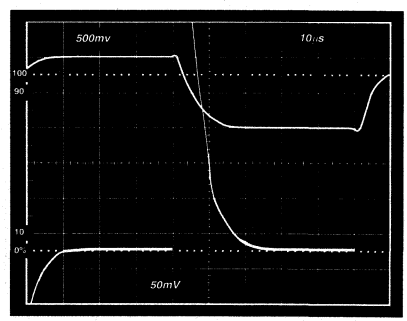


Figure 24. Settling Time. V_S = ±5 V, G = 100

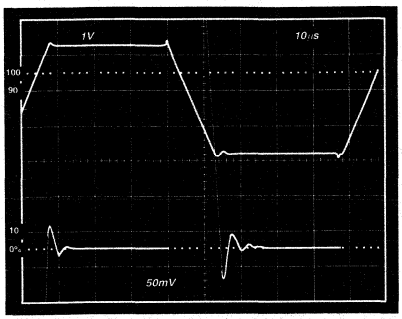


Figure 25. Settling Time. V_S = +5 V, G = 10

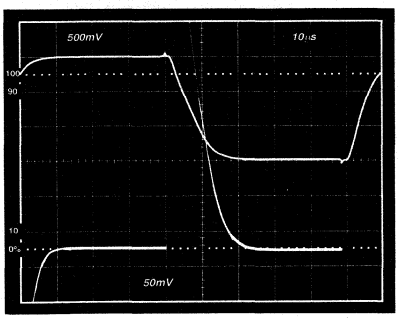


Figure 26. Settling Time. V_S = +5 V, G = 100

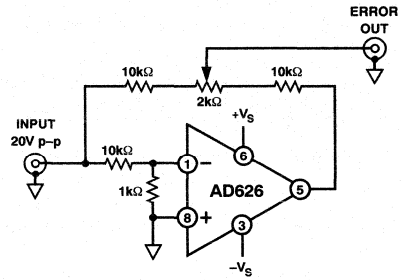


Figure 27. Settling Time Test Circuit

THEORY OF OPERATION

The AD626 is a differential amplifier consisting of a precision balanced attenuator, a very low drift preamplifier (A1), and an output buffer amplifier (A2). It has been designed so that small differential signals can be accurately amplified and filtered in the presence of large common-mode voltages (V_{CM}), without the use of any other active components.

Figure 28 shows the main elements of the AD626. The signal inputs at pins 1 and 8 are first applied to dual resistive attenuators R1 through R4 whose purpose is to reduce the peak common-mode voltage at the input to the preamplifier—a feedback stage based on the very low drift op amp A1. This allows the differential input voltage to be accurately amplified in the presence of large common-mode voltages six times greater than that which can be tolerated by the actual input to A1. As a result, the input CMR extends to six times the quantity (V_S − 1 V). The overall common-mode error is minimized by precise laser-trimming of R3 and R4, thus giving the AD626 a common-mode rejection ratio (CMRR) of at least 10,000:1 (80 dB).

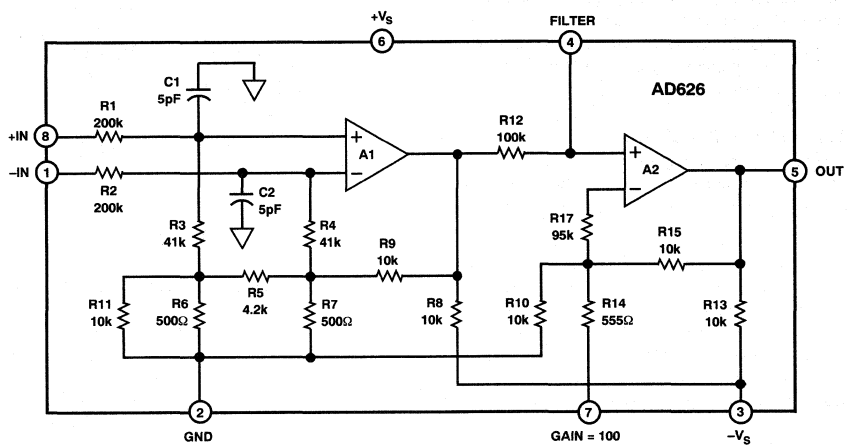


Figure 28. Simplified Schematic

To minimize the effect of spurious RF signals at the inputs due to rectification at the input to A1, small filter capacitors C1 and C2 are included.

The output of A1 is connected to the input of A2 via a 100 kΩ (R12) resistor to facilitate the low-pass filtering of the signal of interest (see low-pass filtering section).

The 200 kΩ input impedance of the AD626 requires that the source resistance driving this amplifier be low in value (<1 kΩ)—this is necessary to minimize gain error. Also, any mismatch between the total source resistance at each input will affect gain accuracy and common-mode rejection (CMR). For example: when operating at a gain of 10, an 80 Ω mismatch in the source resistance between the inputs will degrade CMR to 68 dB.

The output buffer, A2, operates at a gain of 2 or 20, thus setting the overall, precalibrated gain of the AD626 (with no external components) at 10 or 100. The gain is set by the feedback network around amplifier A2.

The output of amplifier A2 relies on a 10 kΩ resistor to $-V_S$ for "pulldown." For single supply operation, ($-V_S$ = "GND"), A2 can drive a 10 kΩ ground referenced load to at least +4.7 V. The minimum, nominally "zero," output voltage will be 30 mV. For dual supply operation (±5 V), the positive output voltage swing will be the same as for a single supply. The negative swing will be to −2.5 V, at G = 100, limited by the ratio:

$$-V_S \times \frac{R15 + R14}{R13 + R14 + R15}.$$

The negative range can be extended to −3.3 V (G = 100) & −4 V (G = 10) by adding an external 10 kΩ pulldown resistor from the output to $-V_S$. This will add 0.5 mA to the AD626's quiescent current, bringing the total to 2 mA.

The AD626's 100 kHz bandwidth at G = 10 & 100 (a 10 MHz gain bandwidth) is much higher than can be obtained with low power op amps in discrete differential amplifier circuits. Furthermore, the AD626 is stable driving capacitive loads up to 50 pF (G10) or 200 pF (G100). Capacitive load drive can be increased to 200 pF (G10) by connecting a 100 Ω resistor in series with the AD626's output and the load.

ADJUSTING THE GAIN OF THE AD626

The AD626 is easily configured for gains of 10 or 100. Figure 29 shows that for a gain of 10, Pin 7 is simply left unconnected; similarly, for a gain of 100, Pin 7 is grounded, as shown in Figure 30.

Gains between 10 and 100 are easily set by connecting a variable resistance between Pin 7 and Analog GND, as shown in Figure 31. Because the on-chip resistors have an absolute tolerance of ±20% (although they are ratio matched to within 0.1%), at least a 20% adjustment range must be provided. The values shown in the table in Figure 31 provide a good trade-off between gain set range and resolution, for gains from 11 to 90.

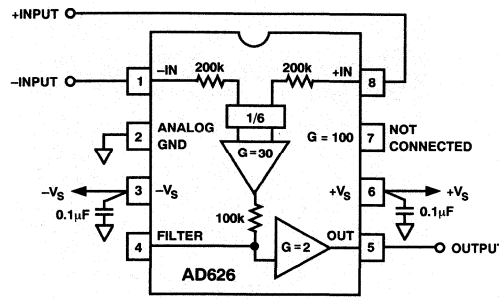


Figure 29. AD626 Configured for a Gain of 10

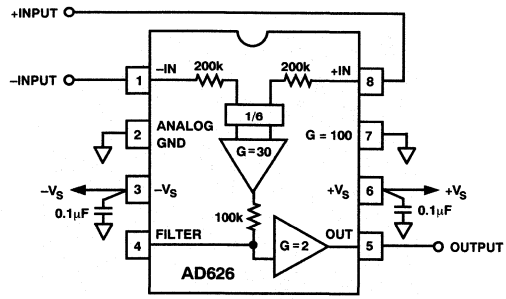
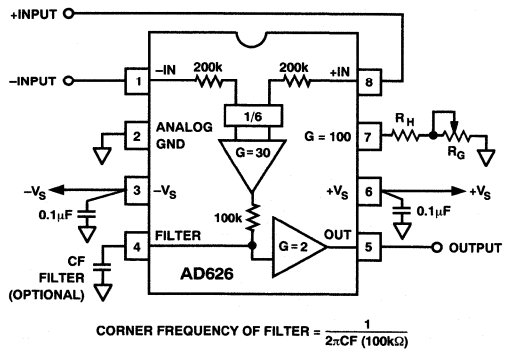


Figure 30. AD626 Configured for a Gain of 100



$$\text{CORNER FREQUENCY OF FILTER} = \frac{1}{2\pi CF\,(100k\Omega)}$$

RESISTOR VALUES FOR GAIN ADJUSTMENT

GAIN RANGE	R_G	R_H
11 – 20	100k	4.99k
20 – 40	10k	802
40 – 80	1k	80
80 – 100	100Ω	2

Figure 31. Recommended Circuit for Gain Adjustment

SINGLE-POLE LOW-PASS FILTERING

A low-pass filter can be easily implemented by using the features provided by the AD626.

By simply connecting a capacitor between Pin 4 and ground, a single-pole low-pass filter is created, as shown in Figure 32.

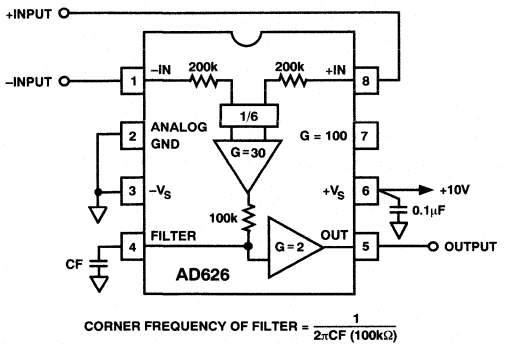


Figure 32. A One-Pole Low-Pass Filter Circuit Which Operates from a Single +10 V Supply

CURRENT SENSOR INTERFACE

A typical current sensing application, making use of the large common-mode range of the AD626, is shown in Figure 33. The current being measured is sensed across resistor R_S. The value of R_S should be less than 1 kΩ and should be selected so that the average differential voltage across this resistor is typically 100 mV.

To produce a full-scale output of +4 V, a gain of 40 is used, adjustable by ±20% to absorb the tolerance in the sense resistor. Note that there is sufficient headroom to allow at least a 10% overrange (to +4.4 V).

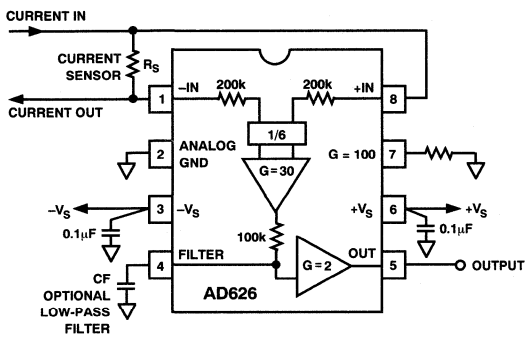


Figure 33. Current Sensor Interface

BRIDGE APPLICATIONS

Figure 34 shows the AD626 in a typical bridge application. Here, the AD626 is set to operate at a gain of 100, using dual supply voltages and offering the option of low-pass filtering.

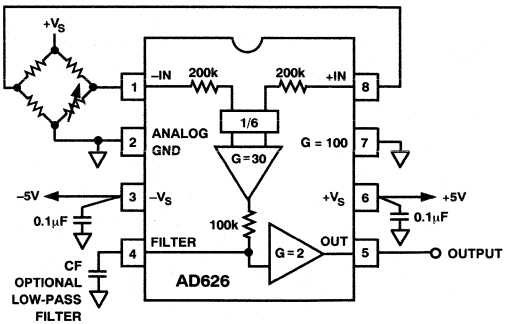


Figure 34. A Typical Bridge Application

4

Multiple 2 MHz PGAs

AD75062/AD75068

FEATURES

Two or Eight Programmable Gain Amps in a Monolithic IC
Wideband: 2 MHz Bandwidth at All Gain Settings
Low Phase Shift: < 2.5° Up to 10 kHz, < 0.25° Up to 1 kHz
Independent PGA Gains of 1, 2, 4, 8, 16, 32, 64, or 128
Low Nonlinearity: < 0.04% at All Gains
Low Input Bias Current: < 4 pA
Small Size: 16-Pin DIP or 44-Pin JLCC Package
Operates from ±12 V Supplies

APPLICATIONS

Sonar
Instrumentation

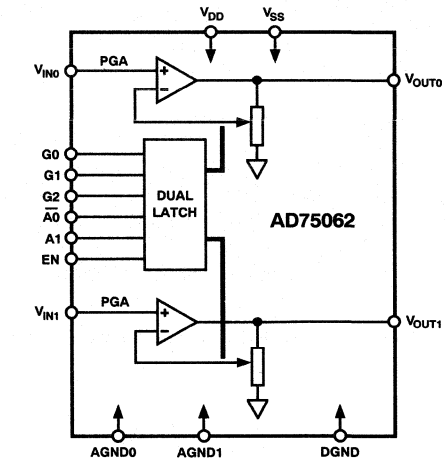
PRODUCT DESCRIPTION

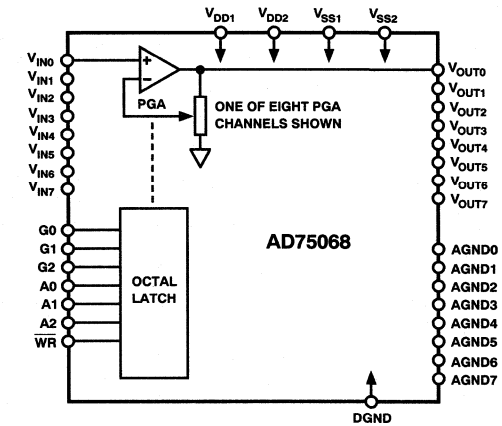
The AD75062 and AD75068 contain multiple programmable-gain amplifiers in one monolithic circuit. The AD75062 has two channels; the AD75068 has eight. Each PGA is complete, including amplifier, gain-setting network, and control latch, and requires no external components. Each PGA may be independently programmed for gains of 1 to 128, in powers of two. A unique circuit design keeps the bandwidth constant at all gains: the −3 dB point is 2 MHz (minimum, small signal).

On-chip voltage regulators for each channel ensure high channel-to-channel isolation (88 dB minimum, dc to 1 kHz) and excellent power supply rejection (65 dB minimum, dc to 10 kHz). To reduce the effects of the impedance of external circuit interconnect between the chip and power supplies, the AD75068 includes two pins for each power supply voltage.

The high performance and functionality of the AD75062 and AD75068 result in part from their fabrication in Analog Devices' BiMOS II process. This epitaxial BiCMOS process features bipolar transistors for precise analog circuitry; CMOS transistors for high impedance inputs, dense logic and analog switches; laser-trimmed thin-film resistors; and double-level metal interconnects.

FUNCTIONAL BLOCK DIAGRAMS





4

AD75062/AD75068—SPECIFICATIONS (T_A = operating temperature range; V_{DD}, V_{SS} = ±12 V; R_L = 2 kΩ; C_L = 400 pF; unless otherwise noted)

Parameter	AD75062A/AD75068A Min	Typ	Max	Units
GAIN AND GAIN ACCURACY				
Gain Settings (G)		1, 2, 4, 8, 16, 32, 64, 128		V/V
Gain Error				
G = 1 to 16		±0.4	**±1.0**	%
G = 32 or 64		±0.5	**±1.5**	%
G = 128		±1.5	**±2.5**	%
Phase Shift, Input to Output (All Gains)				
f_{IN} = DC to 1 kHz		0.1	0.25	Degree
f_{IN} = DC to 10 kHz		1.0	**2.5**	Degree
Gain Matching Error Between Channels[1]				
G = 1		0.4	**0.75**	%
G = 2 to 128		0.75	**2.0**	%
DYNAMIC RESPONSE				
Small-Signal Bandwidth (V_{OUT} = ±0.5 V, −3 dB)				
All Gains	2	3		MHz
Full-Power Bandwidth (V_{OUT} = ±5.0 V, −3 dB)				
G = 1	100	500		kHz
G = 128	400	1,000		kHz
Settling Time to 0.01 % (ΔV_{OUT} = ±5.0 V)				
G = 1			4	µs
G = 128			2	µs
Gain Change Settling Time to 0.01%				
(V_{OUT} ≤ ±5.0 V, All Gains; See Test Circuit 1)		3.5	4	µs
Slew Rate				
G = 1	5	10		V/µs
G = 128	50	70		V/µs
Overload Recovery Time to 1%				
(V_{IN} = ±5.0 V, All Gains; See Test Circuit 2)			6	µs
NONLINEARITY				
(V_{OUT} = ±4 V)				
G = 1		0.01	**0.04**	% FSR
G = 2 to 32		0.005	**0.01**	% FSR
G = 64		0.01	**0.02**	% FSR
G = 128		0.01	**0.04**	% FSR
(V_{OUT} = ±5 V)				
G = 1		0.1	**0.3**	% FSR
G = 2 to 32		0.005	**0.01**	% FSR
G = 64		0.01	**0.05**	% FSR
G = 128		0.03	**0.07**	% FSR
INPUT CHARACTERISTICS				
Input Bias Current (All Gains, T_A = +25°C)		2	4	pA
Input Bias Current (All Gains, T_A = T_{MIN} to T_{MAX})		60	100	pA
Input Capacitance			20	pF
Input Offset Voltage (G = 1 to 32)		±6	**±20**	mV
Input Offset Voltage (G = 64 or 128)		±4	**±10**	mV
OUTPUT CHARACTERISTICS				
Voltage Range	±5.0			V
Current (Per Channel)	±2.5			mA
CROSSTALK				
Isolation Between Any 2 Channels[2]				
600 Ω‖150 pF Input (See Test Circuit 3)				
DC to 1 kHz	88			dB
10 kHz	73			dB
100 kHz	55			dB
Grounded Input (See Test Circuit 4)				
DC to 100 kHz	100			dB

Parameter	AD75062A/AD75068A Min	Typ	Max	Units
NOISE				
Voltage Noise (RTI, 0.1 Hz to 10 Hz)				
G = 1		7		μV p–p
G = 16		3		μV p–p
G = 128		1		μV p–p
Voltage Noise Density (RTI, G = 1)				
f = 10 Hz		400	650	nV/√Hz
f = 100 Hz		125	180	nV/√Hz
f = 1 kHz		95	125	nV/√Hz
f = 10 kHz		85	110	nV/√Hz
Voltage Noise Density (RTI, G = 128)				
f = 10 Hz		85	170	nV/√Hz
f = 100 Hz		25	45	nV/√Hz
f = 1 kHz		15	35	nV/√Hz
f = 10 kHz		10	12	nV/√Hz
TOTAL HARMONIC DISTORTION				
THD (DC to 10 kHz, ±4 V Output, G = 128)		−83	−75	dB
POWER SUPPLY REJECTION				
PSRR (V_{DD}, V_{SS} = ±11.4 V to ±13.2 V)				
DC	**70**	75		dB
10 kHz	65	70		dB
DIGITAL INPUTS				
Logic "1" Voltage	2		V_{DD}	V
Logic "0" Voltage	0		0.8	V
Logic "1" Current			1	μA
Logic "0" Current			1	μA
POWER SUPPLY REQUIREMENTS				
Voltage Range, V_{DD} and V_{SS}	±11.4	±12	±13.2	V
Supply Current, I_{DD}[3]				
AD75062		14	17	mA
AD75068		42	**66**	mA
Supply Current, I_{SS}[3]				
AD75062		−12	−14	mA
AD75068		−42	**−60**	mA
OPERATING TEMPERATURE				
T_{MIN}, T_{MAX}	−40		+85	°C

NOTES

[1]Gain matching error is determined by finding the maximum, minimum, and average of the gains of all channels on a chip and then calculating: gain matching error = (maximum gain − minimum gain)/(average gain).

[2]Crosstalk isolation is determined by driving one channel with V_{OUT} = ±5 V, R_L = 2 kΩ‖400 pF, G = 1; and measuring a second channel with G = 128.

[3]Maximum supply current occurs when all channels are set to maximum gain. I_{DD} and I_{SS} are measured at V_{DD} and V_{SS} = ±12 V.

All minimum and maximum specifications are guaranteed, and specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

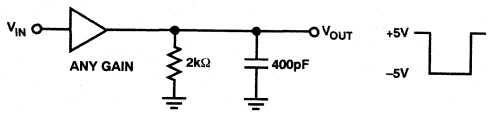
Specifications subject to change without notice.

ORDERING GUIDE

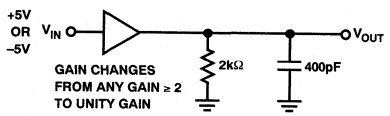
Model	Temperature Range	Number of Channels	Package Description	Package Option*
AD75062AD	−40°C to +85°C	2	Ceramic DIP	D-16
AD75068AJ	−40°C to +85°C	8	Ceramic JLCC	J-44

*For outline information see Package Information section.

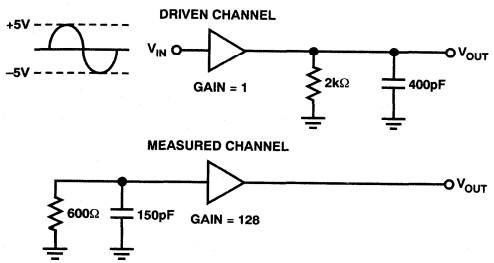
TEST CIRCUITS



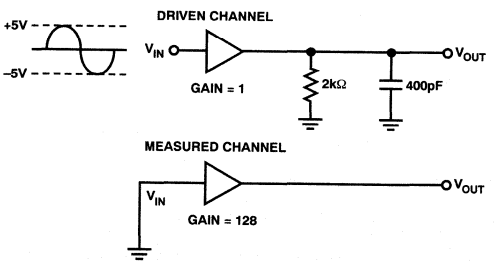
Test Circuit 1. Gain Change Settling Time



Test Circuit 2. Overload Recovery Time



Test Circuit 3. Crosstalk, Ungrounded Inputs

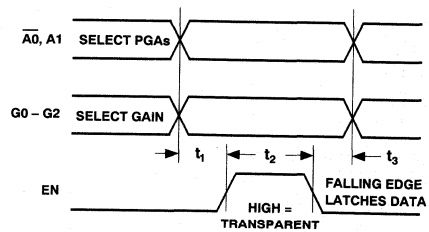


Test Circuit 4. Crosstalk, Grounded Inputs

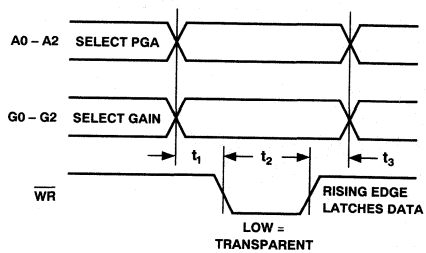
TIMING CHARACTERISTICS[1] (T_A = operating temperature range; V_{DD}, V_{SS} = ±12 V unless otherwise noted)

Parameter	Symbol	Value	Units	Condition
Data Setup Time	t_1	0	ns	min
Write Pulse Width	t_2	80	ns	min
Data Hold Time	t_3	80	ns	min

NOTE
[1]Timing measurement reference level is 1.5 V.
Specifications subject to change without notice.



Timing Diagram 1. AD75062



Timing Diagram 2. AD75068

ABSOLUTE MAXIMUM RATINGS*

(T_A = operating temperature range unless otherwise noted)

V_{DD} to DGND or AGND . . . . . −0.3 V, +18 V
V_{SS} to DGND or AGND . . . . . −18 V, +0.3 V
V_{DD} to V_{SS} . . . . . −0.3 V, +26.4 V
V_{IN} to AGND . . . . . V_{SS}, V_{DD}
Digital Inputs to DGND . . . . . −0.3 V, V_{DD}
AGND to DGND . . . . . −0.3 V, +0.3 V
Power Dissipation ($T_A \leq +85°C$) . . . . . 1.7 W
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Short Circuit Duration . . . . . Indefinite
(Output Connected to Ground, Power Dissipation <max)

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The AD75062 and AD75068 have been characterized in accordance with MIL-STD-883C, Method 3015 (Human Body Model), with no degradation in performance observed for levels up to ±1,000 V. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination potential before devices are removed.

CONFIGURING THE AD75062 AND AD75068

The gain of each channel in the AD75062 may be programmed individually or both channels may be set to the same gain simultaneously. To set gains in the AD75062, apply the address(es) to the address inputs and the desired gain value to the gain inputs G0–G2, and then activate the ENable input by pulsing it high. This operation is summarized in Table IA and the timing is illustrated in Timing Diagram 1.

The gain of each channel in the AD75068 is individually programmable. To set the gain of a channel, apply its address to inputs A0–A2 and the desired gain to inputs G0–G2, and then activate the WR/ input by pulsing it low. This operation is summarized in Table IB and the timing is illustrated in Timing Diagram 2.

Table IA. Operation Truth Table—AD75062

Gain Selection			
G2	G1	G0	Gain
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

Channel Addressing		
A1	$\overline{A0}$	Channel
0	0	0
0	1	Neither
1	0	Both
1	1	1

Write Modes	
EN	Operation
0	Latched
1	Transparent

Table IB. Operation Truth Table—AD75068

Gain Selection			
G2	G1	G0	Gain
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

Channel Addressing			
A2	A1	A0	Channel
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Write Modes	
$\overline{WR}$	Operation
0	Transparent
1	Latched

ANALOG CIRCUIT CONSIDERATIONS

Please refer to the Recommended Circuit Schematics when reading the following section.

Grounding Recommendations

The AD75062 has three pins and the AD75068 has nine pins for analog and digital grounds, designated AGND and DGND. The AGND pins are the ground return pins for the amplifiers. They should be connected to the analog ground point in the system. Any external loads should be returned to system ground.

The DGND pin returns current from the bus interface and logic circuitry of the AD75062/AD75068 to ground. This pin should be connected to the digital ground point in the circuit.

Analog and digital grounds should be connected at one point in the system. If there is a possibility that this connection may be broken or otherwise disconnected, then two diodes should be connected in inverse parallel between the analog and digital ground pins of the AD75062/AD75068 to limit the maximum ground voltage difference.

Power Supplies and Decoupling

The AD75062/AD75068 requires two power supplies for proper operation. V_{DD} and V_{SS} are nominally ±12 V.

Decoupling capacitors should be used on the power supply pins. Good engineering practice dictates locating the bypass capacitors as near as possible to the package pins. Recommended values are 4.7 μF tantalum and 0.1 μF ceramic at each of two places: V_{DD} and V_{SS} to analog ground.

Input Considerations

Input pins have a small amount of capacitance to ground and to adjacent inputs. To maximize bandwidth and minimize crosstalk, each input should be driven by as low a source impedance as possible.

Output Considerations

Each amplifier output can source or sink ±2.5 mA of current to an external load. Short-circuit protection limits load current to a maximum load current of 40 mA. Load capacitance of up to 400 pF can be accommodated with no effect on stability.

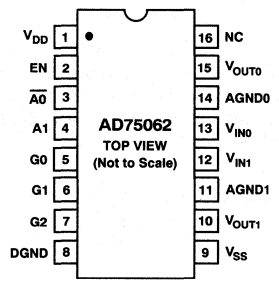
Transistor Count

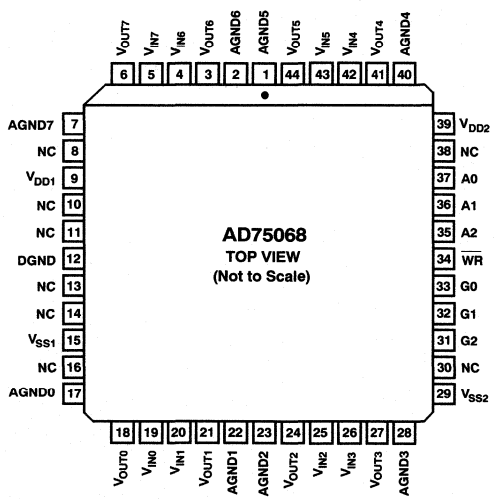
The AD75062 contains 1,170 transistors. The AD75068 contains 4,680 transistors.

PIN DESCRIPTION—AD75062

Pin	Name	Description
1	V_{DD}	+12 V Power Supply
2	EN	Enable (Active High)
3	$\overline{A0}$	Select Channel 0 (Active Low)
4	A1	Select Channel 1 (Active High)
5	G0	Gain Input Bit 0 (LSB)
6	G1	Gain Input Bit 1
7	G2	Gain Input Bit 2 (MSB)
8	DGND	Digital Ground
9	V_{SS}	−12 V Power Supply
10	V_{OUT1}	Output of PGA 1
11	AGND1	Analog Ground for PGA 1
12	V_{IN1}	Input of PGA 1
13	V_{IN0}	Input of PGA 0
14	AGND0	Analog Ground for PGA 0
15	V_{OUT0}	Output of PGA 0
16	NC	No Internal Connection

PIN CONFIGURATIONS

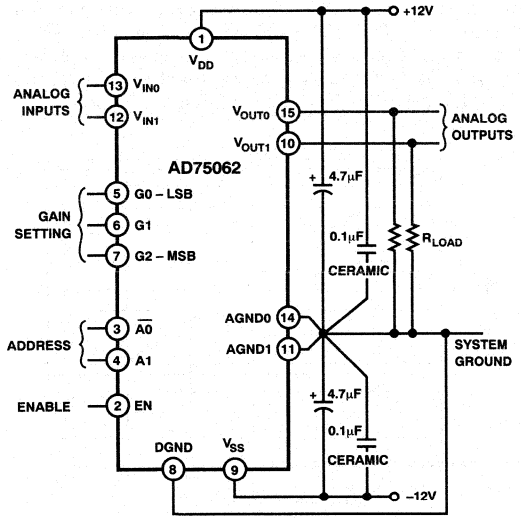




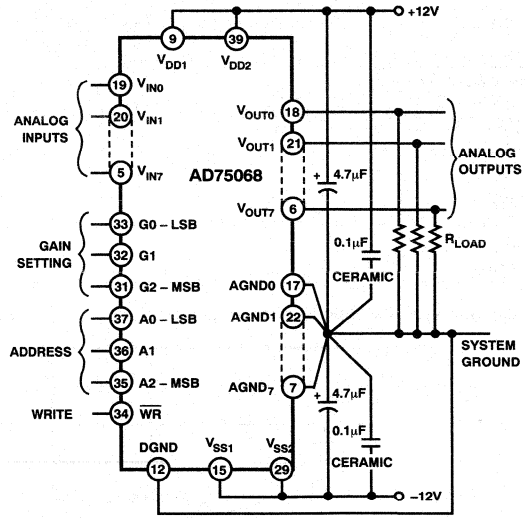
NC = NO INTERNAL CONNECTION

PIN DESCRIPTION—AD75068

Pin	Name	Description
1	AGND5	Analog Ground for PGA 5
2	AGND6	Analog Ground for PGA 6
3	V_{OUT6}	Output of PGA 6
4	V_{IN6}	Input of PGA 6
5	V_{IN7}	Input of PGA 7
6	V_{OUT7}	Output of PGA 7
7	AGND7	Analog Ground for PGA 7
8	NC	No Internal Connection
9	V_{DD1}	+12 V Power Supply
10	NC	No Internal Connection
11	NC	No Internal Connection
12	DGND	Digital Ground
13	NC	No Internal Connection
14	NC	No Internal Connection
15	V_{SS1}	−12 V Power Supply
16	NC	No Internal Connection
17	AGND0	Analog Ground for PGA 0
18	V_{OUT0}	Output of PGA 0
19	V_{IN0}	Input of PGA 0
20	V_{IN1}	Input of PGA 1
21	V_{OUT1}	Output of PGA 1
22	AGND1	Analog Ground for PGA 1
23	AGND2	Analog Ground for PGA 2
24	V_{OUT2}	Output of PGA 2
25	V_{IN2}	Input of PGA 2
26	V_{IN3}	Input of PGA 3
27	V_{OUT3}	Output of PGA 3
28	AGND3	Analog Ground for PGA 3
29	V_{SS2}	−12 V Power Supply
30	NC	No Internal Connection
31	G2	Gain Input Bit 2 (MSB)
32	G1	Gain Input Bit 1
33	G0	Gain Input Bit 0 (LSB)
34	$\overline{WR}$	Write Input; Active Low
35	A2	Address Input 2 (MSB)
36	A1	Address Input 1
37	A0	Address Input 0 (LSB)
38	NC	No Internal Connection
39	V_{DD2}	+12 V Power Supply
40	AGND4	Analog Ground for PGA 4
41	V_{OUT4}	Output of PGA 4
42	V_{IN4}	Input of PGA 4
43	V_{IN5}	Input of PGA 5
44	V_{OUT5}	Output of PGA 5



Recommended Circuit Schematic – AD75062



Recommended Circuit Schematic – AD75068

OPERATING PRINCIPLES

To maintain a fixed closed-loop bandwidth, each channel's amplifier input-stage transconductance changes as its gain setting changes. This is done by engaging more PMOS devices in parallel to form the input stage: with the gain set to 1×, two devices make up the input stage; at a gain of 8×, 16 devices; finally, with gain set to 128×, 256 devices operate in parallel. When the gain is set to 1×, approximately 20 µA flow in the input stage; at a gain of 128, about 3 mA flow.

The noise and input offset specifications reflect this input-stage design. Generally, the input offset falls as the gain is increased, due to the averaging effect of more devices in the input stage. The input noise will fall also, since it has a thermal component proportional to the square root of the input transresistance. As the gain increases, more devices are paralleled, the active gate area increases, and the 1/f noise component decreases. The input capacitance and leakage are not affected by gain changes, because the sources of the PMOS devices are switched, not their gates.

The AD75062/AD75068 is a conventional two-stage amplifier in other respects. An output integrator with a fixed-value capacitor sets the bandwidth. Because the input-stage current increases with gain, the amplifier's slew rate greatly increases and the settling time decreases at higher gains. Furthermore, the full-power bandwidth is almost constant for gains from 1× to 128×.

To give high channel-to-channel isolation and good power-supply rejection, the chip individually regulates the supplies to each amplifier. These regulators require some voltage headroom, so the input and output voltage ranges are restricted to ±5 volts at low supply voltages (±11.4 V).

THERMAL DESIGN CONSIDERATIONS—AD75068

The AD75068, due to its wide gain-independent bandwidth and high integration, may dissipate up to 1.6 W of power in certain operating modes. The reliability of the AD75068 will be significantly enhanced by keeping it as cool as possible, and by not exceeding the maximum junction temperature of 175°C.

Certain applications may require an external heatsink, forced air, or other cooling.

The power dissipation of the AD75068 is a function of the gains selected for all of the channels. The worst-case power dissipation (P_D) can be estimated from this equation:

$$P_D = 600\ mW + \sum_{ch=0}^{7} (G_{CH} \times 1\ mW)$$

where G_{CH} is the gain (1, 2, 4, 8, 16, 32, 64, or 128) of the respective channel (0 through 7). With all eight channels set at minimum (1 ×) gain, the AD75068 will typically dissipate less than 600 mW. For each doubling of gain, the gain-dependent portion of the power dissipation per channel will also double. For example, if all channel gains are set to 2 ×, the power dissipation could increase to 600 mW + 8 × (2 × 1 mW) = 616 mW. If all channels are operated at maximum gain (128×), the power dissipation could increase to 600 mW + 8 × (128 × 1 mW) = 1.62 W.

The junction temperature of the device in a specific application can be computed from the thermal resistance of the package and the estimated power dissipation, e.g.,

$$T_{JUNCTION}\ [°C] = T_{AMBIENT}\ [°C] + P_D\ [W] \times \theta_{JA}\ [°C/W]$$

or

$$T_{JUNCTION}\ [°C] = T_{CASE}\ [°C] + P_D\ [W] \times \theta_{JC}\ [°C/W]$$

where θ_{JA} is the junction-ambient and θ_{JC} is the junction-case thermal resistance.

The actual thermal resistance depends on the mounting configuration of the device and the air flow over it. The thermal resistance of the AD75068 has been measured in the following conditions for devices soldered to a printed-wiring board operating near the maximum power dissipation, with and without a heatsink. The heatsink was an EG&G Wakefield Engineering part #651-B (6 × 10 × 19 mm) attached with cyanoacrylate adhesive.

Table II. AD75068 Thermal Resistance

Condition	Thermal Resistance (°C/W)	
	θ_{JA}	θ_{JC}
Without Heatsink		
Still Air	40	17
200 lfpm	30	15
With Heatsink		
Still Air	37	14
200 lfpm	24	10
400 lfpm	19	8
600 lfpm	17	7
800 lfpm	15	7

The data in the above table is graphed in Figure 1.

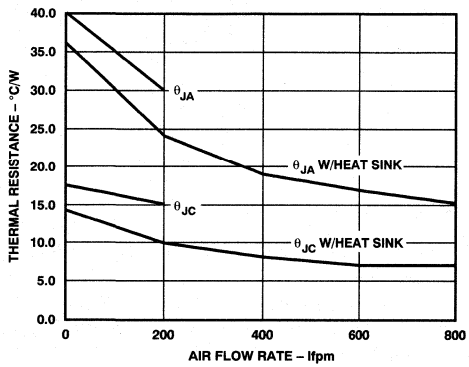


Figure 1. Thermal Resistance

The reliability of the AD75062/AD75068, as measured by the mean-time-to-failure (MTTF), is directly dependent on the junction temperature. The MTTF will increase by approximately 50% for each 13°C decrease in junction temperature, as shown in Figure 2 below. This calculation was based on Military Handbook 217E, "Reliability Prediction of Electronic Equipment."

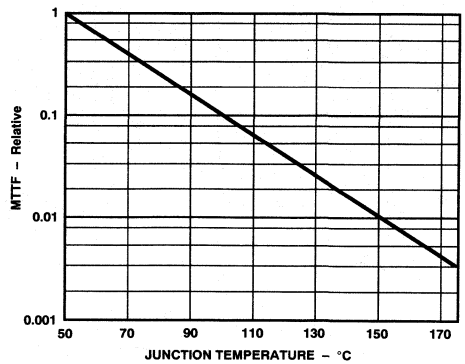


Figure 2. Relative Reliability vs. Temperature

ANALOG DEVICES

Low Noise Precision Instrumentation Amplifier

AMP-01

FEATURES

- Low Offset Voltage ..... 50μV Max
- Very Low Offset Voltage Drift ..... 0.3μV/°C Max
- Low Noise ..... 0.12μV_{p-p} (0.1Hz to 10Hz)
- Excellent Output Drive ..... ±10V at ±50mA
- Capacitive Load Stability ..... to 1μF
- Gain Range ..... 0.1 to 10,000
- Excellent Linearity ..... 16-Bit at G = 1000
- High CMR ..... 125dB Min (G = 1000)
- Low Bias Current ..... 4nA Max
- May be Configured as a Precision Op-Amp
- Output-Stage Thermal Shutdown
- Available in Die Form

ORDERING INFORMATION†

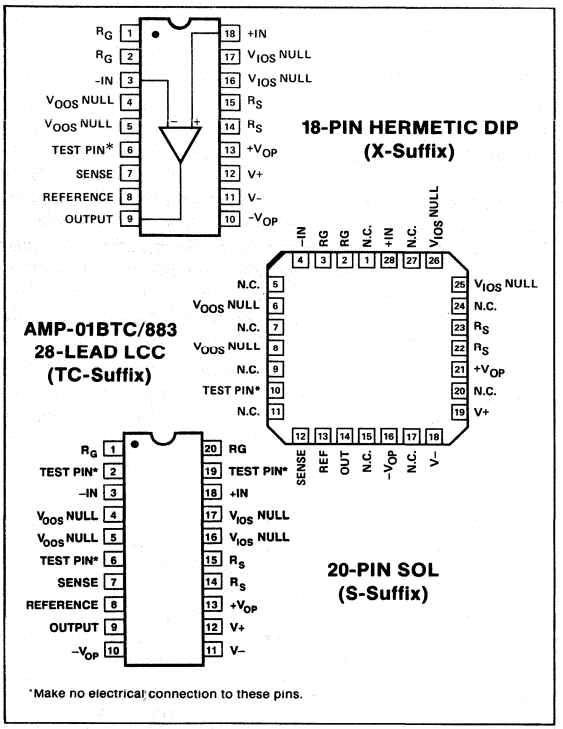
PACKAGE			OPERATING TEMPERATURE RANGE
CERDIP 18-PIN	LCC	PLASTIC 20-PIN	
AMP01AX*	—	—	MIL
AMP01BX*	AMP01BTC/883	—	MIL
AMP01EX	—	—	IND
AMP01FX	—	—	IND
—	—	AMP01GS††	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

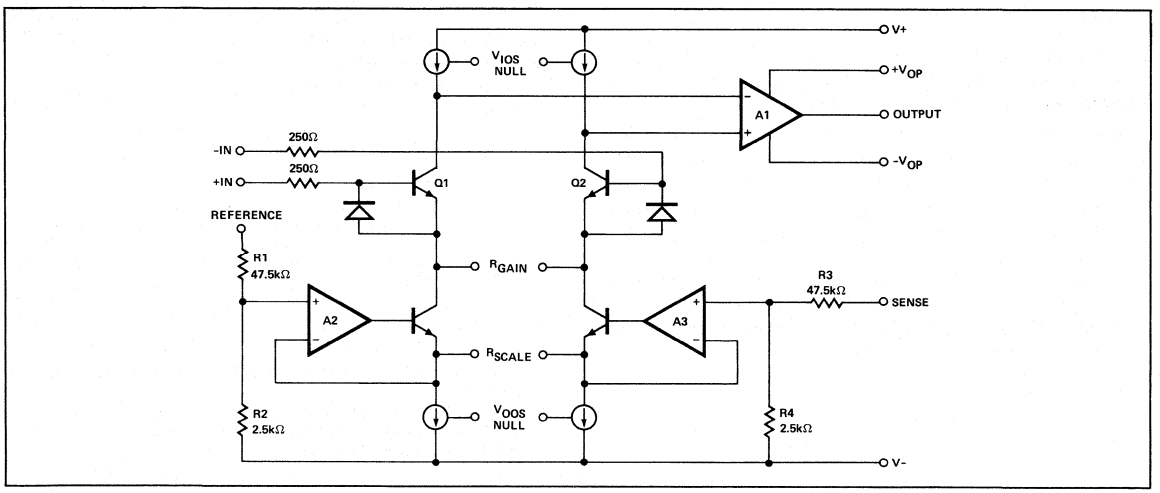
† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



Manufactured under the following U.S. patents: 4,471,321 and 4,503,381.

AMP-01

GENERAL DESCRIPTION

The AMP-01 is a monolithic instrumentation amplifier designed for high-precision data acquisition and instrumentation applications. The design combines the conventional features of an instrumentation amplifier with a high-current output stage. The output remains stable with high capacitance loads (1μF), a unique ability for an instrumentation amplifier. Consequently, the AMP-01 can amplify low-level signals for transmission through long cables without requiring an output buffer. The output stage may be configured as a voltage or current generator.

Input offset voltage is very low (20μV) which generally eliminates the external null potentiometer. Temperature changes have minimal effect on offset; TCV_{IOS} is typically 0.15μV/°C. Excellent low-frequency noise performance is achieved with a minimal compromise on input protection. Bias current is very low, less than 10nA over the military temperature range. High common-mode rejection of 130dB, 16-bit linearity at a gain of 1000, and 50mA peak output current are achievable simultaneously. This combination takes the instrumentation amplifier one step further towards the ideal amplifier.

AC performance complements the superb DC specifications. The AMP-01 slews at 4.5V/μs into capacitive loads of up to 15nF, settles in 50μs to 0.01% at a gain of 1000, and boasts a healthy 26MHz gain-bandwidth product. These features make the AMP-01 ideal for high-speed data-acquisition systems.

Gain is set by the ratio of two external resistors over a range of 0.1 to 10,000. A very low gain-temperature-coefficient of 10ppm/°C is achievable over the whole gain range. Output voltage swing is guaranteed with three load resistances; 50Ω, 500Ω, and 2kΩ. Loaded with 500Ω, the output delivers ±13.0V minimum. A thermal shutdown circuit prevents destruction of the output transistors during overload conditions.

The AMP-01 can also be configured as a high-performance operational amplifier. In many applications, the AMP-01 can be used in place of op-amp/power-buffer combinations.

THEORY OF OPERATION

An instrumentation amplifier, unlike an op amp, requires precise internal feedback. The two techniques presently in use are resistive and current feedback.

The AMP-01 employs the current feedback approach which has significant advantages over resistive feedback. Advantages of current-feedback are:

a. The technique yields a very high common-mode rejection ratio. The AMP-01 CMR is in excess of 130dB at a gain of 1000.
b. The gain of the current feedback design is set by the ratio of two external resistors. Using external resistors allows any practical gain to be set with high precision and very low gain temperature coefficient.
c. The current-feedback design is immune to CMR degradation when series resistance is added to the reference input. A small (trimmable) offset change results from added resistance, e.g. a printed circuit track.

The AMP-01 utilizes low-drift thin-film resistors to minimize output offset temperature drift. A feedback voltage-to-current converter is employed having high linearity and low noise, particularly at low frequencies. Parameter shifts during packaging are eliminated by a post-assembly trimming technique which electronically adjusts the output offset voltage.

The AMP-01 input transistors Q1 and Q2 feed active loads, yielding stage gain in excess of 4000 (see simplified schematic) The output amplifier, A1, is a two-stage design having a gain of about 50,000 driving a 100Ω load. Overall gain of 2×10^8 yields excellent linearity, even at high closed-loop gains.

Low bias current is achieved by using Ion-implanted superbeta transistors combined with a new bias-current cancellation system, patents applied for. Input bias current remains below 10nA over the military temperature range, −55°C to +125°C.

Superbeta transistors use a new transistor geometry resulting in an input noise of only $5nV/\sqrt{Hz}$ at G = 1000. Noise includes contributions from the gain-setting resistor and internal overload-protection resistor. The input stage achieves an offset voltage drift of less than 0.3μV/°C (E Grade).

The AMP-01 uses a unique two-pole compensation scheme where the load capacitance is incorporated into the dominate pole. Stable operation results even with high capacitance loads. The high output current capability (90mA peak) allows the 4.5V/μs slew-rate to be maintained with load capacitance as high as 15nF.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Common-Mode Input Voltage ..... Supply Voltage
Differential Input Voltage, $R_G \geq 2k\Omega$ ..... ±20V
$R_F < 2k\Omega$ ..... ±10V
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range
AMP-01A, B ..... −55°C to +125°C
AMP-01E, F ..... −25°C to +85°C
AMP-01G ..... 0°C to +70°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
Junction Temperature (T_j) ..... −65°C to +150°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
18-Pin Hermetic DIP (Z)	79	11	°C/W
28-Contact LCC (TC)	78	30	°C/W
20-Pin SOL (S)	88	25	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $R_S = 10k\Omega$, $R_L = 2k\Omega$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	AMP-01A MIN	AMP-01A TYP	AMP-01A MAX	AMP-01B MIN	AMP-01B TYP	AMP-01B MAX	UNITS
OFFSET VOLTAGE									
Input Offset Voltage	V_{IOS}	$T_A = 25°C$	—	20	50	—	40	100	μV
		$-55°C \le T_A \le +125°C$	—	40	80	—	60	150	
Input Offset Voltage Drift	TCV_{IOS}	$-55°C \le T_A \le +125°C$	—	0.15	0.3	—	0.3	1.0	μV/°C
Output Offset Voltage	V_{OOS}	$T_A = 25°C$	—	1	3	—	2	6	mV
		$-55°C \le T_A \le +125°C$	—	3	6	—	6	10	
Output Offset Voltage Drift	TCV_{OOS}	$R_G = \infty$							
		$-55°C \le T_A \le +125°C$	—	20	50	—	50	120	μV/°C
Offset Referred to Input vs. Positive Supply V+ = +5V to +15V	PSR	G = 1000	120	130	—	110	120	—	dB
		G = 100	110	130	—	100	120	—	
		G = 10	95	110	—	90	100	—	
		G = 1	75	90	—	70	80	—	
		$-55°C \le T_A \le +125°C$							
		G = 1000	120	130	—	110	120	—	dB
		G = 100	110	130	—	100	120	—	
		G = 10	95	110	—	90	100	—	
		G = 1	75	90	—	70	80	—	
Offset Referred to Input vs. Negative Supply V− = −5V to −15V	PSR	G = 1000	105	125	—	105	115	—	dB
		G = 100	90	105	—	90	95	—	
		G = 10	70	85	—	70	75	—	
		G = 1	50	65	—	50	60	—	
		$-55°C \le T_A \le +125°C$							
		G = 1000	105	125	—	105	115	—	dB
		G = 100	90	105	—	90	95	—	
		G = 10	70	85	—	70	75	—	
		G = 1	50	65	—	50	60	—	
Input Offset Voltage Trim Range		$V_S = \pm 4.5V$ to $\pm 18V$ (Note 1)	—	±6	—	—	±6	—	mV
Output Offset Voltage Trim Range		$V_S = \pm 4.5V$ to $\pm 18V$ (Note 1)	—	±100	—	—	±100	—	mV
INPUT CURRENT									
Input Bias Current	I_B	$T_A = 25°C$	—	1	4	—	2	6	nA
		$-55°C \le T_A \le +125°C$	—	4	10	—	6	15	
Input Bias Current Drift	TCI_B	$-55°C \le T_A \le +125°C$	—	40	—	—	50	—	pA/°C
Input Offset Current	I_{OS}	$T_A = 25°C$	—	0.2	1.0	—	0.5	2.0	nA
		$-55°C \le T_A \le +125°C$	—	0.5	3.0	—	1.0	6.0	
Input Offset Current Drift	TCI_{OS}	$-55°C \le T_A \le +125°C$	—	3	—	—	5	—	pA/°C
INPUT									
Input Resistance	R_{IN}	Differential, G = 1000	—	1	—	—	1	—	GΩ
		Differential, G ≤ 100	—	10	—	—	10	—	
		Common-Mode, G = 1000	—	20	—	—	20	—	
Input Voltage Range	IVR	$T_A = 25°C$ (Note 2)	±10.5	—	—	±10.5	—	—	V
		$-55°C \le T_A \le +125°C$	±10.0	—	—	±10.0	—	—	
Common-Mode Rejection	CMR	$V_{CM} = \pm 10V$, 1kΩ source imbalance							
		G = 1000	125	130	—	115	125	—	dB
		G = 100	120	130	—	110	125	—	
		G = 10	100	120	—	95	110	—	
		G = 1	85	100	—	75	90	—	
		$-55°C \le T_A \le +125°C$							
		G = 1000	120	125	—	110	120	—	dB
		G = 100	115	125	—	105	120	—	
		G = 10	95	115	—	90	105	—	
		G = 1	80	95	—	75	90	—	

NOTES:
1. V_{IOS} and V_{OOS} nulling has minimal affect on TCV_{IOS} and TCV_{OOS}, respectively.
2. Refer to section on common-mode rejection.

AMP-01

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $R_S = 10k\Omega$, $R_L = 2k\Omega$, $T_A = +25°C$, $-25°C \le T_A \le +85°C$ for E,F grades, $0°C \le T_A \le +70°C$ for G grade,unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	AMP-01E MIN	AMP-01E TYP	AMP-01E MAX	AMP-01F/G MIN	AMP-01F/G TYP	AMP-01F/G MAX	UNITS
OFFSET VOLTAGE									
Input Offset Voltage	V_{IOS}	$T_A = +25°C$	–	20	50	–	40	100	µV
		$T_{MIN} \le T_A \le T_{MAX}$	–	40	80	–	60	150	
Input Offset Voltage Drift	TCV_{IOS}	$T_{MIN} \le T_A \le T_{MAX}$ (Note 2)	–	0.15	0.3	–	0.3	1.0	µV/°C
Output Offset Voltage	V_{OOS}	$T_A = +25°C$	–	1	3	–	2	6	mV
		$T_{MIN} \le T_A \le T_{MAX}$	–	3	6	–	6	10	
Output Offset Voltage Drift	TCV_{OOS}	RG = ∞ (Note 2)	–	20	100	–	50	120	µV/°C
		$T_{MIN} \le T_A \le T_{MAX}$							
Offset Referred to Input vs. Positive Supply V+ = +5V to +15V	PSR	G = 1000	120	130	–	110	120	–	dB
		G = 100	110	130	–	100	120	–	
		G = 10	95	110	–	90	100	–	
		G = 1	75	90	–	70	80	–	
		$T_{MIN} \le T_A \le T_{MAX}$							
		G = 1000	120	130	–	110	120	–	dB
		G = 100	110	130	–	100	120	–	
		G = 10	95	110	–	90	100	–	
		G = 1	75	90	–	70	80	–	
Offset Referred to Input vs. Negative Supply V– = –5V to –15V	PSR	G = 1000	110	125	–	105	115	–	dB
		G = 100	95	105	–	90	95	–	
		G = 10	75	85	–	70	75	–	
		G = 1	55	65	–	50	60	–	
		$T_{MIN} \le T_A \le T_{MAX}$							
		G = 1000	110	125	–	105	115	–	dB
		G = 100	95	105	–	90	95	–	
		G = 10	75	85	–	70	75	–	
		G = 1	55	65	–	50	60	–	
Input Offset Voltage Trim Range		$V_S = \pm4.5V$ to $\pm18V$ (Note 1)	–	±6	–	–	±6	–	mV
Output Offset Voltage Trim Range		$V_S = \pm4.5V$ to $\pm18V$ (Note 1)	–	±100	–	–	±100	–	mV
INPUT CURRENT									
Input Bias Current	I_B	$T_A = +25°C$	–	1	4	–	2	6	mV
		$T_{MIN} \le T_A \le T_{MAX}$	–	4	10	–	6	15	
Input Bias Current Drift	TCI_B	$T_{MIN} \le T_A \le T_{MAX}$	–	40	–	–	50	–	pA/°C
Input Offset Current	I_B	$T_A = +25°C$	–	0.2	1.0	–	0.5	2.0	mV
		$T_{MIN} \le T_A \le T_{MAX}$	–	0.5	3.0	–	1.0	6.0	
Input Offset Current Drift	TCI_{OS}	$T_{MIN} \le T_A \le T_{MAX}$	–	3	–	–	5	–	pA/°C
INPUT									
Input Resistance	R_{IN}	Differential, G = 1000	–	1	–	–	1	–	GΩ
		Differential, G ≤ 100	–	10	–	–	10	–	
		Common-Mode, G = 1000	–	20	–	–	20	–	
Input Voltage Range	IVR	$T_A = +25°C$ (Note 3)	±10.5	–	–	±10.5	–	–	V
		$T_{MIN} \le T_A \le T_{MAX}$	±10.0	–	–	±10.0	–	–	
Common-Mode Rejection	CMR	$V_{CM} = \pm10V$, 1kΩ source imbalance							
		G = 1000	125	130	–	115	125	–	dB
		G = 100	120	130	–	110	125	–	
		G = 10	100	120	–	95	110	–	
		G = 1	85	100	–	75	90	–	
		$T_{MIN} \le T_A \le T_{MAX}$							
		G = 1000	120	125	–	110	120	–	dB
		G = 100	115	125	–	105	120	–	
		G = 10	95	115	–	90	105	–	
		G = 1	80	95	–	75	90	–	

NOTES:

1. V_{IOS} and V_{OOS} nulling has minimal effect on TCV_{IOS} and TCV_{OOS}, respectively.
2. Sample tested.
3. Refer to section on common-mode rejection.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $R_S = 10k\Omega$, $R_L = 2k\Omega$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	AMP-01A/E MIN	AMP-01A/E TYP	AMP-01A/E MAX	AMP-01B/F/G MIN	AMP-01B/F/G TYP	AMP-01B/F/G MAX	UNITS
GAIN									
Gain Equation Accuracy		$G = \frac{20 \times R_S}{R_G}$ Accuracy Measured from G = 1 to 1000	—	0.3	0.6	—	0.5	0.8	%
Gain Range	G		0.1	—	10k	0.1	—	10k	V/V
Nonlinearity		G = 1000	—	0.0007	0.005	—	0.0007	0.005	%
		G = 100 (Note 1)	—	—	0.005	—	—	0.005	
		G = 10 (Note 1)	—	—	0.005	—	—	0.007	
		G = 1	—	—	0.010	—	—	0.015	
Temperature Coefficient	G_{TC}	$1 \le G \le 1000$ (Notes 1, 2)	—	5	10	—	5	15	ppm/°C
OUTPUT RATING									
Output Voltage Swing	V_{OUT}	$R_L = 2k\Omega$	±13.0	±13.8	—	±13.0	±13.8	—	V
		$R_L = 500\Omega$	±13.0	±13.5	—	±13.0	±13.5	—	
		$R_L = 50\Omega$	±2.5	±4.0	—	±2.5	±4.0	—	
		$R_L = 2k\Omega$ Over Temp.	±12.0	±13.8	—	±12.0	±13.8	—	V
		$R_L = 500\Omega$ (Note 3)	±12.0	±13.5	—	±12.0	±13.5	—	
Positive Current Limit		Output-to-Ground Short	60	100	120	60	100	120	mA
Negative Current Limit		Output-to-Ground Short	60	90	120	60	90	120	mA
Capacitive Load Stability		$1 \le G \le 1000$ No Oscillations, (Note 1)	0.1	1	—	0.1	1	—	μF
Thermal Shutdown Temperature		Junction Temperature	—	165	—	—	165	—	°C
NOISE									
Voltage Density, RTI	e_n	f_O = 1kHz							
		G = 1000	—	5	—	—	5	—	$nV/\sqrt{Hz}$
		G = 100	—	10	—	—	10	—	
		G = 10	—	59	—	—	59	—	
		G = 1	—	540	—	—	540	—	
Noise Current Density, RTI	i_n	f_O = 1kHz, G = 1000	—	0.15	—	—	0.15	—	$pA/\sqrt{Hz}$
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz							
		G = 1000	—	0.12	—	—	0.12	—	μV_{p-p}
		G = 100	—	0.16	—	—	0.16	—	
		G = 10	—	1.4	—	—	1.4	—	
		G = 1	—	13	—	—	13	—	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz, G = 1000	—	2	—	—	2	—	pA_{p-p}
DYNAMIC RESPONSE									
Small-Signal Bandwidth (−3dB)	BW	G = 1	—	570	—	—	570	—	kHz
		G = 10	—	100	—	—	100	—	
		G = 100	—	82	—	—	82	—	
		G = 1000	—	26	—	—	26	—	
Slew Rate	SR	G = 10	3.5	4.5	—	3.0	4.5	—	V/μs
Settling Time	t_S	To 0.01%, 20V step							
		G = 1	—	12	—	—	12	—	μs
		G = 10	—	13	—	—	13	—	
		G = 100	—	15	—	—	15	—	
		G = 1000	—	50	—	—	50	—	

NOTES:
1. Guaranteed by design.
2. Gain tempco does not include the effects of gain and scale resistor tempco match.
3. $-55°C \le T_A \le +125°C$ for A/B grades, $-25°C \le T_A \le +85°C$ for E/F grades, $0°C \le T_A \le 70°C$ FOR G grades.

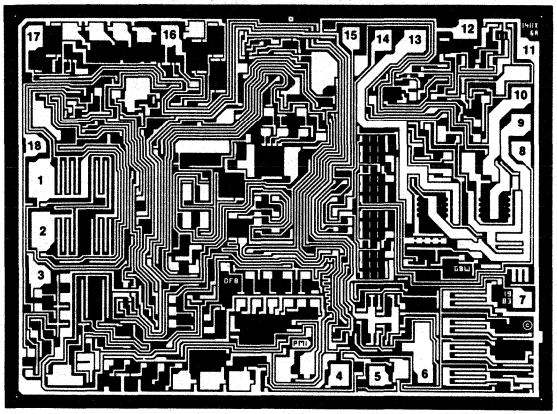
AMP-01

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $R_S = 10k\Omega$, $R_L = 2k\Omega$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	AMP-01A/E MIN	AMP-01A/E TYP	AMP-01A/E MAX	AMP-01B/F/G MIN	AMP-01B/F/G TYP	AMP-01B/F/G MAX	UNITS
SENSE INPUT									
Input Resistance	R_{IN}		35	50	65	35	50	65	kΩ
Input Current	I_{IN}	Referenced to V–	—	280	—	—	280	—	μA
Voltage Range		(Note 1)	−10.5	—	+15	−10.5	—	+15	V
REFERENCE INPUT									
Input Resistance	R_{IN}		35	50	65	35	50	65	kΩ
Input Current	I_{IN}	Referenced to V–	—	280	—	—	280	—	μA
Voltage Range		(Note 1)	−10.5	—	+15	−10.5	—	+15	V
Gain to Output			—	1	—	—	1	—	V/V
POWER SUPPLY $-25°C \le T_A \le +85°C$ for E/F Grades, $-55°C \le T_A \le +125°C$ for A/B Grades									
Supply Voltage Range	V_S	+V linked to $+V_{OP}$ −V linked to $-V_{OP}$	±4.5	—	±18	±4.5	—	±18	V
Quiescent Current	I_Q	+V linked to $+V_{OP}$ −V linked to $-V_{OP}$	— —	3.0 3.4	4.8 4.8	— —	3.0 3.4	4.8 4.8	mA

NOTE:
1. Guaranteed by design.

DICE CHARACTERISTICS



DIE SIZE 0.111 × 0.149 inch, 16,539 sq. mils
(2.82 × 3.78 mm, 10.67 sq. mm)

1. R_G
2. R_G
3. −INPUT
4. V_{OOS} NULL
5. V_{OOS} NULL
6. TEST PIN*
7. SENSE
8. REFERENCE
9. OUTPUT
10. V− (OUTPUT)
11. V−
12. V+
13. V+ (OUTPUT)
14. R_S
15. R_S
16. V_{IOS} NULL
17. V_{IOS} NULL
18. +INPUT

*** Make no electrical connection**

4

WAFER TEST LIMITS at $V_S = \pm 15V$, $R_S = 10k\Omega$, $R_L = 2k\Omega$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	AMP-01NBC LIMIT	AMP-01GBC LIMIT	UNITS
Input Offset Voltage	V_{IOS}		60	120	μV MAX
Output Offset Voltage	V_{OOS}		4	8	mV MAX
Offset Referred to Input vs. Positive Supply	PSR	V+ = +5V to +15V			
		G = 1000	120	110	dB MIN
		G = 100	110	100	
		G = 10	95	90	
		G = 1	75	70	
Offset Referred to Input vs. Negative Supply	PSR	V− = −5V to −15V			
		G = 1000	105	105	dB MIN
		G = 100	90	90	
		G = 10	70	70	
		G = 1	50	50	
Input Bias Current	I_B		4	8	nA MAX
Input Offset Current	I_{OS}		1	3	nA MAX
Input Voltage Range	IVR	Guaranteed by CMR Tests	±10	±10	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 10V$			
		G = 1000	125	115	dB MIN
		G = 100	120	110	
		G = 10	100	95	
		G = 1	85	75	
Gain Equation Accuracy		$G = \frac{20 \times R_S}{R_G}$	0.6	0.8	% MAX
Output Voltage Swing	V_{OUT}	$R_L = 2k\Omega$	±13	±13	V MIN
		$R_L = 500\Omega$	±13	±13	
		$R_L = 50\Omega$	±2.5	±2.5	
Output-Current Limit		Output-to-Ground Short	±60	±60	mA MIN
Output-Current Limit		Output-to-Ground Short	±120	±120	mA MAX
Quiescent Current	I_Q	+V Linked to $+V_{OP}$ −V Linked to $-V_{OP}$	4.8	4.8	mA MAX

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

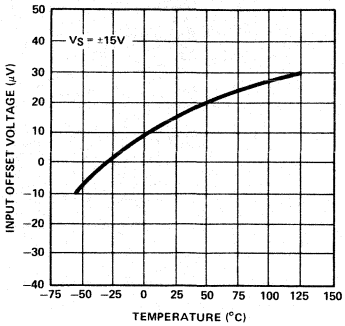
AMP-01

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $R_S = 10k\Omega$, $R_L = 2k\Omega$, $T_A = 25°C$, unless otherwise noted.

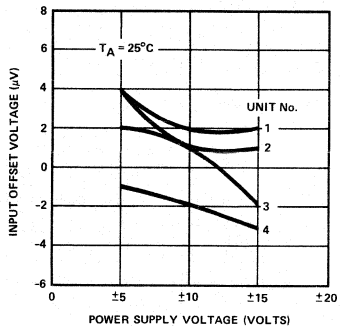
PARAMETER	SYMBOL	CONDITIONS	AMP-01NBC TYPICAL	AMP-01GBC TYPICAL	UNITS
Input Offset Voltage Drift	TCV_{IOS}		0.15	0.30	$\mu V/°C$
Output Offset Voltage Drift	TCV_{OOS}	$R_G = \infty$	20	50	$\mu V/°C$
Input Bias Current Drift	TCI_B		40	50	$pA/°C$
Input Offset Current Drift	TCI_{OS}		3	5	$pA/°C$
Nonlinearity		G = 1000	0.0007	0.0007	%
Voltage Noise Density	e_n	G = 1000 f_O = 1kHz	5	5	$nV/\sqrt{Hz}$
Current Noise Density	i_n	G = 1000 f_O = 1kHz	0.15	0.15	$pA/\sqrt{Hz}$
Voltage Noise	e_{np-p}	G = 1000 0.1Hz to 10Hz	0.12	0.12	μV_{p-p}
Current Noise	i_{np-p}	G = 1000 0.1Hz to 10Hz	2	2	pA_{p-p}
Small-Signal Bandwidth (−3dB)	BW	G = 1000	26	26	kHz
Slew Rate	SR	G = 10	4.5	4.5	$V/\mu s$
Settling Time	t_S	To 0.01%, 20V Step G = 1000	50	50	μs

TYPICAL PERFORMANCE CHARACTERISTICS

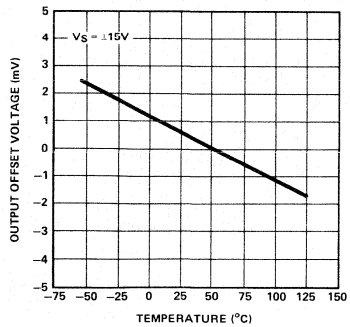
INPUT OFFSET VOLTAGE vs TEMPERATURE



INPUT OFFSET VOLTAGE vs SUPPLY VOLTAGE



OUTPUT OFFSET VOLTAGE vs TEMPERATURE



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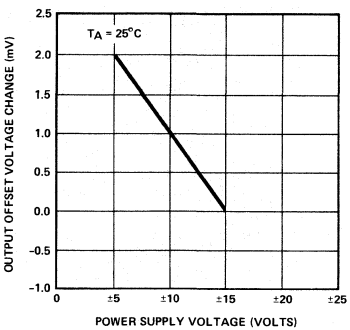
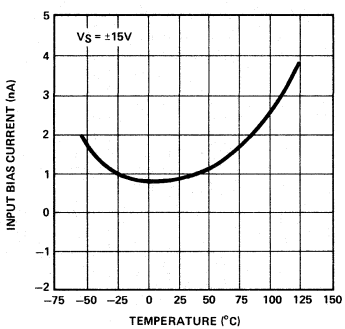
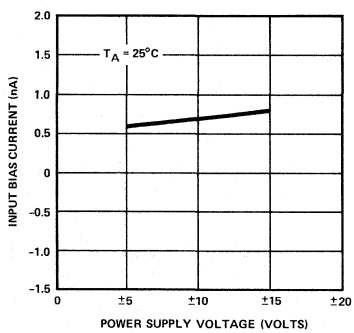
OUTPUT OFFSET VOLTAGE CHANGE vs SUPPLY VOLTAGE



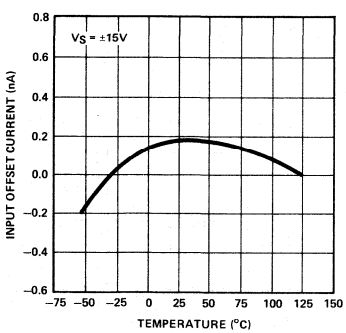
INPUT BIAS CURRENT vs TEMPERATURE



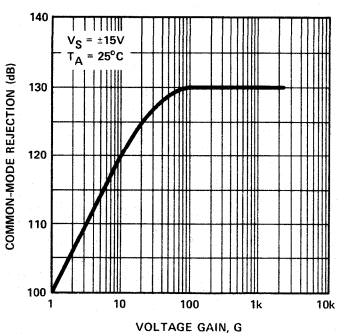
INPUT BIAS CURRENT vs SUPPLY VOLTAGE



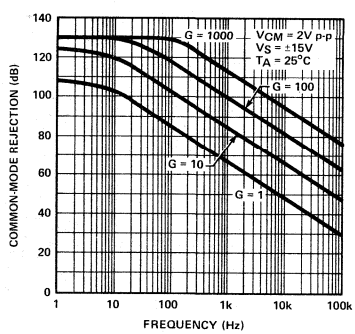
INPUT OFFSET CURRENT vs TEMPERATURE



COMMON-MODE REJECTION vs VOLTAGE GAIN



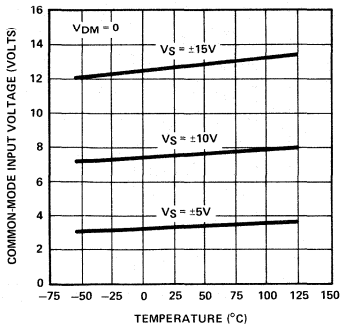
COMMON-MODE REJECTION vs FREQUENCY



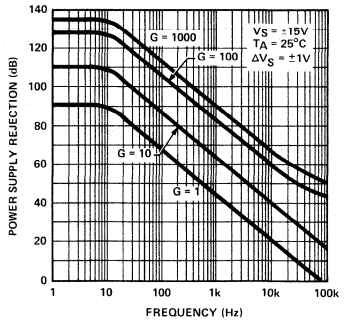
AMP-01

TYPICAL PERFORMANCE CHARACTERISTICS

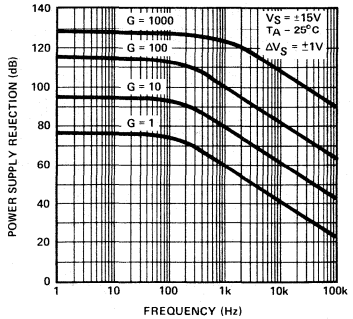
COMMON-MODE VOLTAGE RANGE vs TEMPERATURE



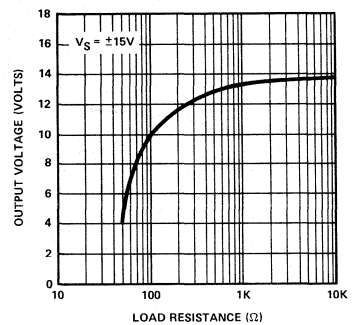
POSITIVE PSR vs FREQUENCY



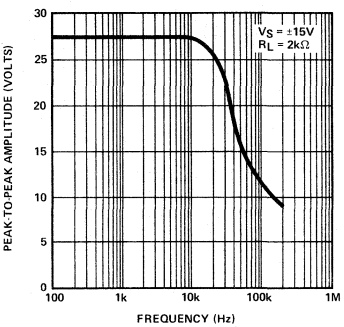
NEGATIVE PSR vs FREQUENCY



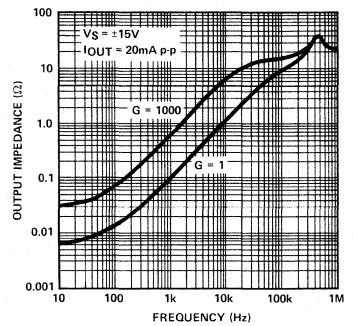
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



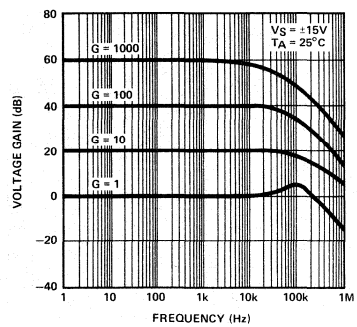
MAXIMUM OUTPUT SWING vs FREQUENCY



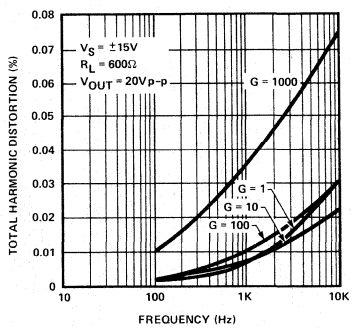
CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



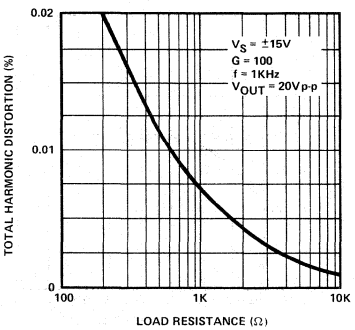
CLOSED-LOOP VOLTAGE GAIN vs FREQUENCY



TOTAL HARMONIC DISTORTION vs FREQUENCY

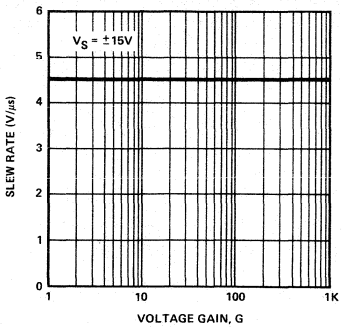


TOTAL HARMONIC DISTORTION vs LOAD RESISTANCE

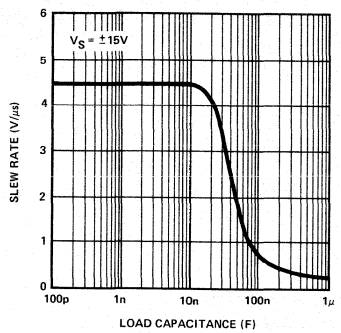


TYPICAL PERFORMANCE CHARACTERISTICS

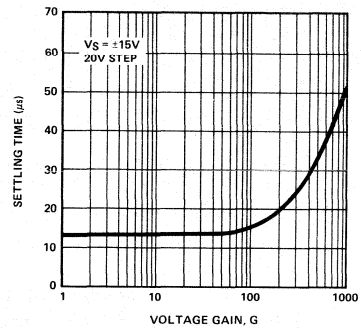
SLEW RATE vs VOLTAGE GAIN



SLEW RATE vs LOAD CAPACITANCE



SETTLING TIME TO 0.01% vs VOLTAGE GAIN



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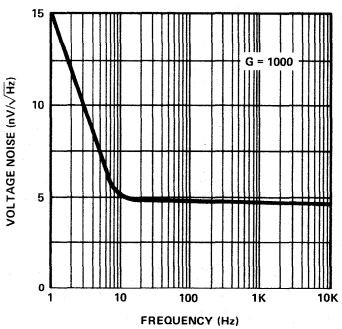
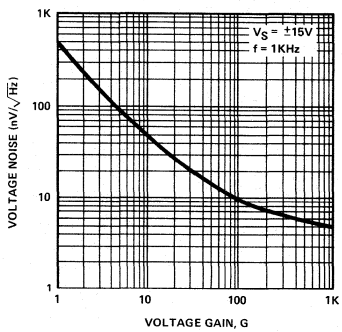
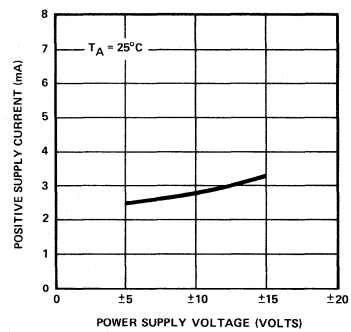
VOLTAGE NOISE DENSITY vs FREQUENCY



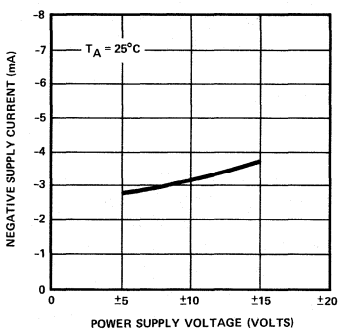
RTI VOLTAGE NOISE DENSITY vs GAIN



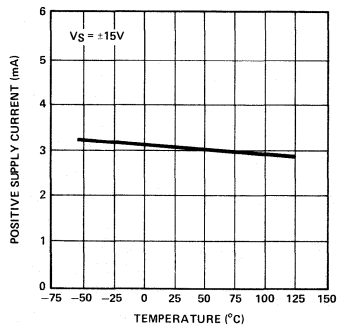
POSITIVE SUPPLY CURRENT vs SUPPLY VOLTAGE



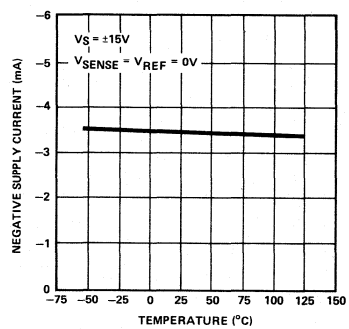
NEGATIVE SUPPLY CURRENT vs SUPPLY VOLTAGE



POSITIVE SUPPLY CURRENT vs TEMPERATURE



NEGATIVE SUPPLY CURRENT vs TEMPERATURE



INPUT AND OUTPUT OFFSET VOLTAGES

Instrumentation amplifiers have independent offset voltages associated with the input and output stages. While the initial offsets may be adjusted to zero, temperature variations will cause shifts in offsets. Systems with auto-zero can correct for offset errors, so initial adjustment would be unnecessary. However, many high-gain applications don't have auto zero. For these applications, both offsets can be nulled, which has minimal effect on TCV_{IOS} and TCV_{OOS}.

The input offset component is directly multiplied by the amplifier gain, whereas output offset is independent of gain. Therefore, at low gain, output-offset-errors dominate, while at high gain, input-offset-errors dominate. Overall offset voltage, V_{OS}, referred to the output (RTO) is calculated as follows;

$$V_{OS}(RTO) = (V_{IOS} \times G) + V_{OOS} \quad \cdots\cdots (1)$$

where V_{IOS} and V_{OOS} are the input and output offset voltage specifications and G is the amplifier gain. Input offset nulling alone is recommended with amplifiers having fixed gain above 50. Output offset nulling alone is recommended when gain is fixed at 50 or below.

In applications requiring both initial offsets to be nulled, the input offset is nulled first by short-circuiting R_G, then the output offset is nulled with the short removed.

The overall offset voltage drift TCV_{OS}, referred to the output, is a combination of input and output drift specifications. Input offset voltage drift is multiplied by the amplifier gain, G, and summed with the output offset drift;

$$TCV_{OS}(RTO) = (TCV_{IOS} \times G) + TCV_{OOS} \quad \cdots\cdots (2)$$

where TCV_{IOS} is the input offset voltage drift, and TCV_{OOS} is the output offset voltage specification. Frequently, the amplifier drift is referred back to the input (RTI) which is then equivalent to an input signal change;

$$TCV_{OS}(RTI) = TCV_{IOS} + \frac{TCV_{OOS}}{G} \quad \cdots\cdots (3)$$

For example, the maximum input-referred drift of an AMP-01EX set to G = 1000 becomes;

$$TCV_{OS}(RTI) = 0.3\mu V/^\circ C + \frac{100\mu V/^\circ C}{1000} = 0.4\mu V/^\circ C \text{ max.}$$

INPUT BIAS AND OFFSET CURRENTS

Input transistor bias currents are additional error sources which can degrade the input signal. Bias currents flowing through the signal source resistance appear as an additional offset voltage. Equal source resistance on both inputs of an IA will minimize offset changes due to bias current variations with signal voltage and temperature. However, the difference between the two bias currents, the input offset current, produces a non-trimmable error. The magnitude of the error is the offset current times the source resistance.

A current path must always be provided between the differential inputs and analog ground to ensure correct amplifier operation. Floating inputs, such as thermocouples, should be grounded close to the signal source for best common-mode rejection.

GAIN

The AMP-01 uses two external resistors for setting voltage gain over the range 0.1 to 10,000. The magnitudes of the scale resistor, R_S, and gain-set resistor, R_G, are related by the formula: $G = 20 \times R_S/R_G$, where G is the selected voltage gain (Refer to Figure 1).

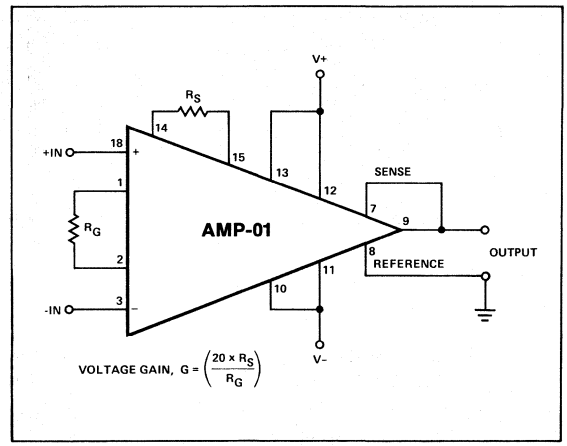
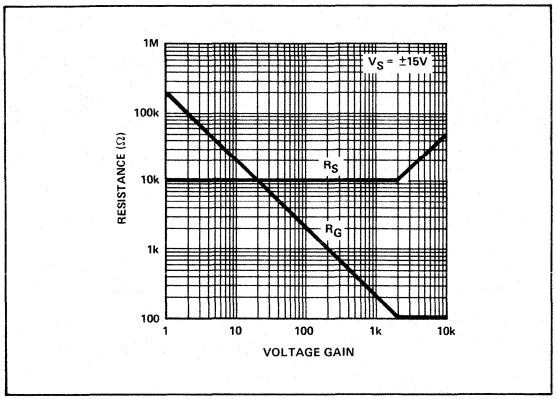


Figure 1. Basic AMP-01 connections for gains 0.1 to 10,000.

The magnitude of R_S affects linearity and output referred errors. Circuit performance is characterized using $R_S = 10k\Omega$ when operating on ±15 volt supplies and driving a ±10 volt output. R_S may be reduced to 5kΩ in many applications particularly when operating on ±5 volt supplies or if the output voltage swing is limited to ±5 volts. Bandwidth is improved with $R_S = 5k\Omega$ and this also increases common-mode rejection by approximately 6dB at low gain. Lowering the value below 5kΩ can cause instability in some circuit configurations and usually has no advantage. High voltage gains between two and ten thousand would require very low values of R_G. For $R_S = 10k\Omega$ and $A_V = 2000$ we get $R_G = 100\Omega$; this value is the practical lower limit for R_G. Below 100Ω, mismatch of wirebond and resistor temperature coefficients will introduce significant gain tempco errors. Therefore, for gains above 2,000, R_G should be kept constant at 100Ω and R_S increased. The maximum gain of 10,000 is obtained with R_S set to 50kΩ.

Metal-film or wirewound resistors are recommended for best results. The absolute values and TC's are not too important, only the ratiometric parameters.

AC amplifiers require good gain stability with temperature and time, but DC performance is unimportant. Therefore, low cost metal-film types with TC's of 50ppm/°C are usually adequate for R_S and R_G. Realizing the full potential of the AMP-01's offset voltage and gain stability requires precision metal-film or wirewound resistors. Achieving a 15ppm/°C gain tempco at all gains requires R_S and R_G temperature coefficient matching to 5ppm/°C or better.



R_G AND R_S SELECTION

Gain accuracy is determined by the ratio accuracy of R_S and R_G combined with the gain equation error of the AMP-01 (0.6% max for A/E grades).

All instrumentation amplifiers require attention to layout so thermocouple effects are minimized. Thermocouples formed between copper and dissimilar metals can easily destroy the TCV_{OS} performance of the AMP-01 which is typically 0.15μV/° C. Resistors themselves can generate thermoelectric EMF's when mounted parallel to a thermal gradient. "Vishay" resistors are recommended because a maximum value for thermoelectric generation is specified. However, where thermal gradients are low and gain TC's of 20-50ppm are sufficient, general-purpose metal-film resistors can be used for R_G and R_S.

COMMON-MODE REJECTION

Ideally, an instrumentation amplifier responds only to the difference between the two input signals and rejects common-mode voltages and noise. In practice, there is a small change in output voltage when both inputs experience the same common-mode voltage change; the ratio of these voltages is called the common-mode gain. Common-mode rejection (CMR) is the logarithm of the ratio of differential-mode gain to common-mode gain, expressed in dB. CMR specifications are normally measured with a full-range input voltage change and a specified source resistance unbalance.

The current-feedback design used in the AMP-01 inherently yields high common-mode rejection. Unlike resistive feedback designs, typified by the three-op-amp IA, the CMR is not degraded by small resistances in series with the reference input. A slight, but trimmable, output offset voltage change results from resistance in series with the reference input.

The common-mode input voltage range, CMVR, for linear operation may be calculated from the formula:

$$CMVR = \pm \left(IVR - \frac{|V_{OUT}|}{2G} \right) \ldots\ldots (4)$$

IVR is the data sheet specification for input voltage range; V_{OUT} is the maximum output signal; and G is the chosen voltage gain. For example, at 25° C, IVR is specified as ±10.5 volt minimum with ±15 volt supplies. Using a ±10 volt maximum swing output and substituting the figures in (4) simplifies the formula to:

$$CMVR = \pm \left(10.5 - \frac{5}{G} \right) \ldots\ldots (5)$$

For all gains greater than or equal to 10, CMVR is ±10 volt minimum; at gains below 10, CMVR is reduced.

ACTIVE GUARD DRIVE

Rejection of common-mode noise and line pick-up can be improved by using shielded cable between the signal source and the IA. Shielding reduces pick-up, but increases input capacitance, which in turn degrades the settling-time for signal changes. Further, any imbalance in the source resistance between the inverting and noninverting inputs, when capacitively loaded, converts the common-mode voltage into a differential voltage. This effect reduces the benefits of shielding. AC common-mode rejection is improved by "bootstrapping" the input cable capacitance to the input signal, a technique called "guard driving". This technique effectively reduces the input capacitance. A single guard-driving signal is adequate at gains above 100 and should be the average value of the two inputs. The value of external gain resistor R_G is split between two resistors R_{G1} and R_{G2}; the center tap provides the required signal to drive the buffer amplifier (Figure 2).

GROUNDING

The majority of instruments and data acquisition systems have separate grounds for analog and digital signals. Analog ground may also be divided into two or more grounds which will be tied together at one point, usually the analog power-supply ground. In addition, the digital and analog grounds may be joined, normally at the analog ground pin on the A-to-D converter. Following this basic grounding practice is essential for good circuit performance (Figure 3).

Mixing grounds causes interactions between digital circuits and the analog signals. Since the ground returns have finite resistance and inductance, hundreds of millivolts can be developed between the system ground and the data acquisition components. Using separate ground returns minimizes the current flow in the sensitive analog return path to the system ground point. Consequently, noisy ground currents from logic gates do not interact with the analog signals.

Inevitably, two or more circuits will be joined together with their grounds at differential potentials. In these situations, the differential input of an instrumentation amplifier, with its high CMR, can accurately transfer analog information from one circuit to another.

SENSE AND REFERENCE TERMINALS

The sense terminal completes the feedback path for the instrumentation amplifier output stage and is normally connected directly to the output. The output signal is specified with respect to the reference terminal, which is normally connected to analog ground.

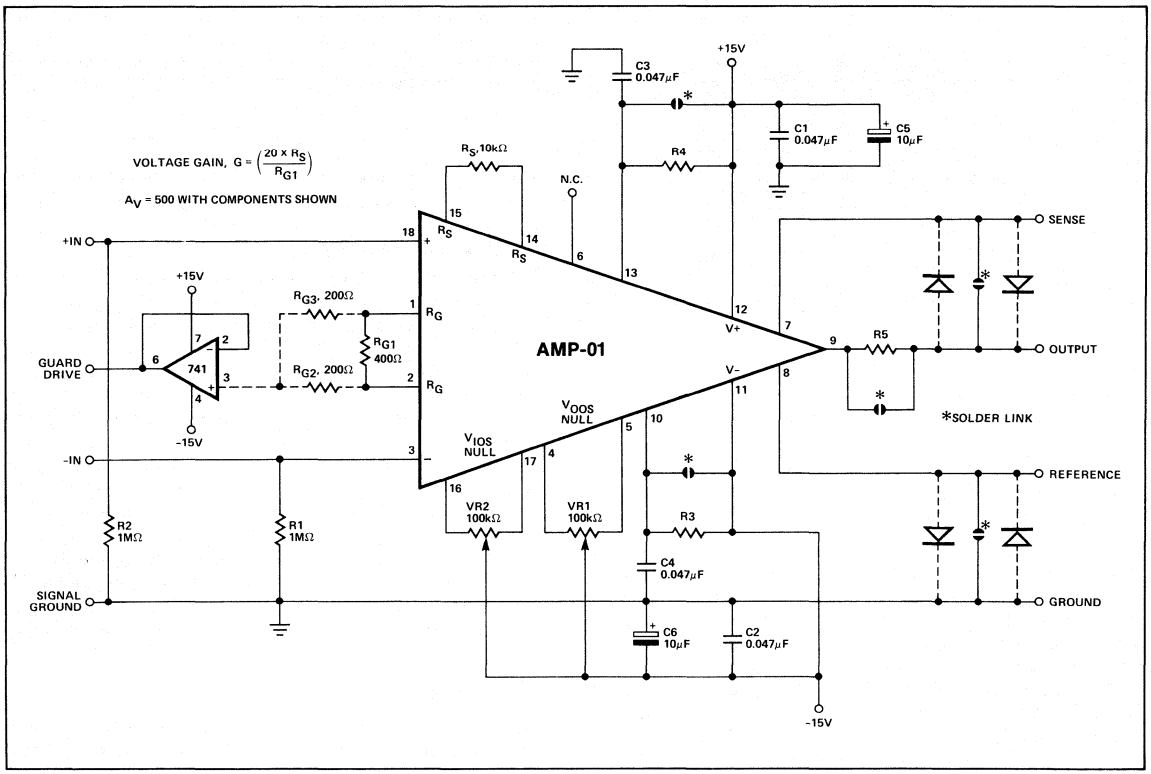


Figure 2. AMP-01 evaluation circuit showing guard-drive connection.

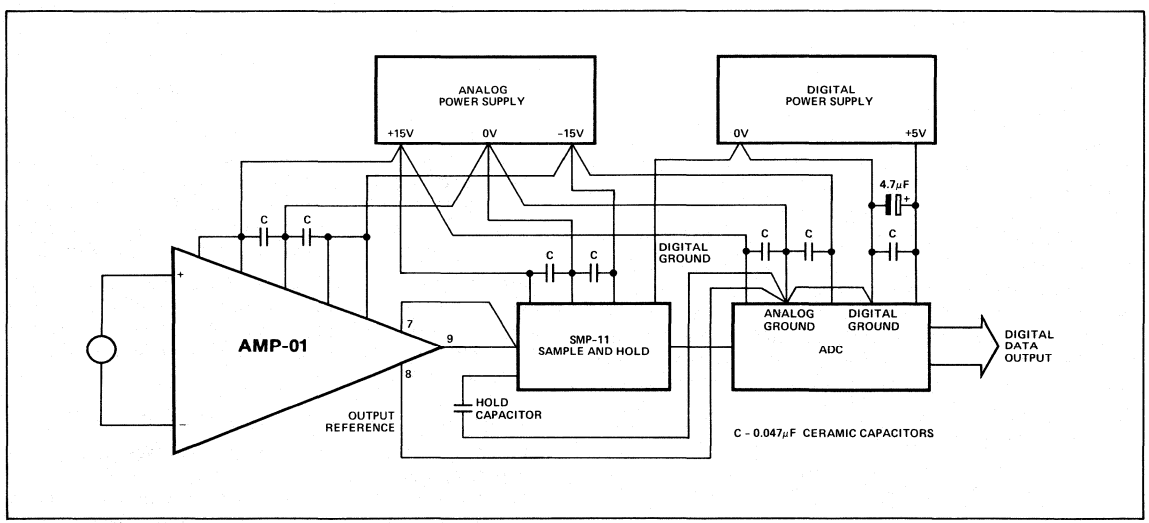


Figure 3. Basic grounding practice.

If heavy output currents are expected and the load is situated some distance from the amplifier, voltage drops due to track or wire resistance will cause errors. Voltage drops are particularly troublesome when driving 50Ω loads. Under these conditions, the sense and reference terminals can be used to "remote sense" the load as shown in Figure 4. This method of connection puts the I×R drops inside the feedback loop and virtually eliminates the error. An unbalance in the lead resistances from the sense and reference pins does not degrade CMR, but will change the output offset voltage. For example, a large unbalance of 3Ω will change the output offset by only 1mV.

DRIVING 50Ω LOADS

Output currents of 50mA are guaranteed into loads of up to 50Ω and 26mA into 500Ω. In addition, the output is stable and free from oscillation even with a high load capacitance. The combination of these unique features in an instrumentation amplifier allows low-level transducer signals to be conditioned and directly transmitted through long cables in voltage or current form. Increased output current brings increased internal dissipation, especially with 50Ω loads. For this reason, the power-supply connections are split into two pairs; pins 10 and 13 connect to the output stage only and pins 11 and 12 provide power to the input and following stages. Dual supply pins allow dropper resistors to be connected in series with the output stage so excess power is dissipated outside the package. Additional decoupling is necessary between pins 10 and 13 to ground to maintain stability when dropper resistors are used. Figure 5 shows a complete circuit for driving 50Ω loads.

HEATSINKING

To maintain high reliability, the die temperature of any IC should be kept as low as practicable, preferably below 100°C. Although most AMP-01 application circuits will produce very little internal heat — little more than the quiescent dissipation of 90mW — some circuits will raise that

4

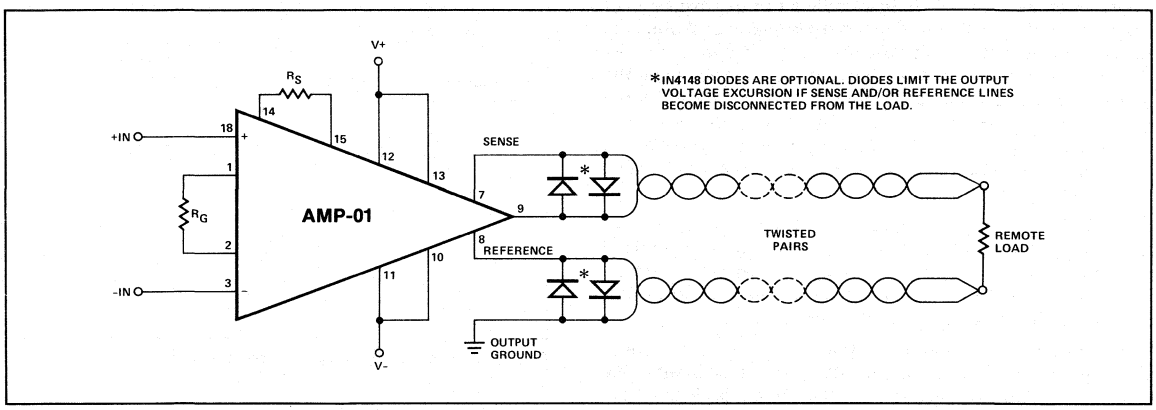


Figure 4. Remote load sensing.

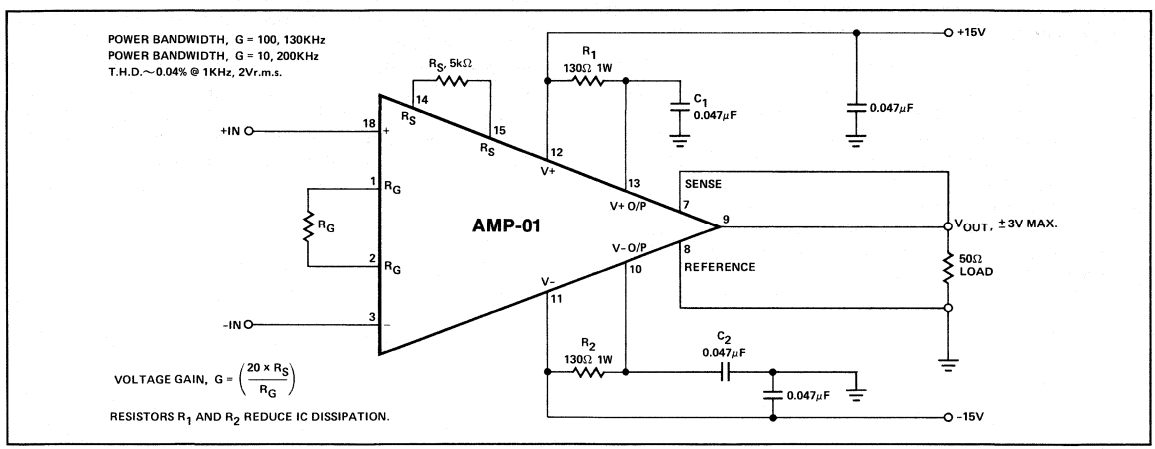


Figure 5. Driving 50Ω loads.

to several hundred milliwatts (for example, the 4-20mA current transmitter application, Figure 8). Excessive dissipation will cause thermal shutdown of the output stage thus protecting the device from damage. A heatsink is recommended in power applications to reduce the die temperature.

Several appropriate heatsinks are available; the Thermalloy 6010B is especially easy to use and is inexpensive. Intended for dual-in-line packages, the heatsink may be attached with a cyanoacrylate adhesive. This heatsink reduces the thermal resistance between the junction and ambient environment to approximately 80° C/W. Junction (die) temperature can then be calculated by using the relationship:

$$P_d = \frac{T_j - T_a}{\theta_{ja}}$$

where T_j and T_a are the junction and ambient temperatures respectively, θ_{ja} is the thermal resistance from junction to ambient, and P_d is the device's internal dissipation.

OVERVOLTAGE PROTECTION

Instrumentation amplifiers invariably sit at the front end of instrumentation systems where there is a high probability of exposure to overloads. Voltage transients, failure of a transducer, or removal of the amplifier power supply while the signal source is connected may destroy or degrade the performance of an unprotected amplifier. Although it is impractical to protect an IC internally against connection to power lines, it is relatively easy to provide protection against typical system overloads.

The AMP-01 is internally protected against overloads for gains of up to 100. At higher gains, the protection is reduced and some external measures may be required. Limited internal overload protection is used so that noise performance would not be significantly degraded.

AMP-01 noise level approaches the theoretical noise floor of the input stage which would be $4nV/\sqrt{Hz}$ at 1kHz when the gain is set at 1000. Noise is the result of shot noise in the input devices and Johnson noise in the resistors. Resistor noise is calculated from the values of R_G (200Ω at a gain of 1000) and the input protection resistors (250Ω). Active loads for the input transistors contribute less than $1nV/\sqrt{Hz}$ of noise. The measured noise level is typically $5nV/\sqrt{Hz}$.

Diodes across the input transistor's base-emitter junctions, combined with 250Ω input resistors and R_G, protect against differential inputs of up to ±20V for gains of up to 100. The diodes also prevent avalanche breakdown that would degrade the I_B and I_{OS} specifications. Decreasing the value of R_G for gains above 100 limits the maximum input overload protection to ±10V. External series resistors could be added to guard against higher voltage levels at the input, but resistors alone increase the input noise and degrade the signal-to-noise ratio, especially at high gains.

Protection can also be achieved by connecting back-to-back 9.1V zener diodes across the differential inputs. This technique does not affect the input noise level and can be used down to a gain of 2 with minimal increase in input current. Although voltage-clamping elements look like short circuits at the limiting voltage, the majority of signal sources provide less than 50mA, producing power levels that are easily handled by low-power zeners.

Simultaneous connection of the differential inputs to a low-impedance signal above 10V during normal circuit operation is unlikely. However, additional protection involves adding 100Ω current-limiting resistors in each signal path prior to the voltage clamp; the resistors increase the input noise level to just $5.4nV/\sqrt{Hz}$ (refer to Figure 6).

Input components, be they multiplexers or resistors, should be carefully selected to prevent the formation of thermocouple junctions which would degrade the input signal.

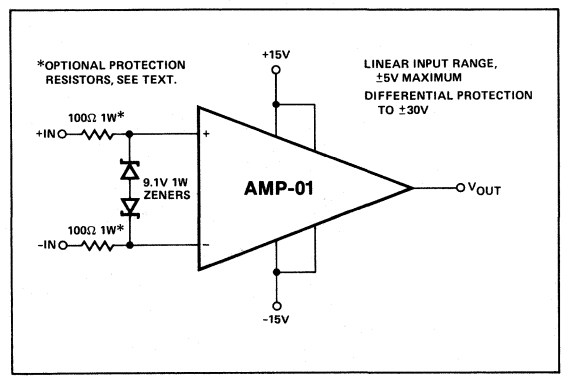


Figure 6. Input overvoltage protection for gains 2 to 10,000.

POWER SUPPLY CONSIDERATIONS

Achieving the rated performance of precision amplifiers in a practical circuit requires careful attention to external influences. For example, supply noise and changes in the nominal voltage directly affect the input offset voltage. A PSR of 80dB means that a change of 100mV on the supply, not an uncommon value, will produce a 10μV input offset change. Consequently, care should be taken in choosing a power unit that has a low output noise level, good line and load regulation, and good temperature stability.

APPLICATIONS INFORMATION

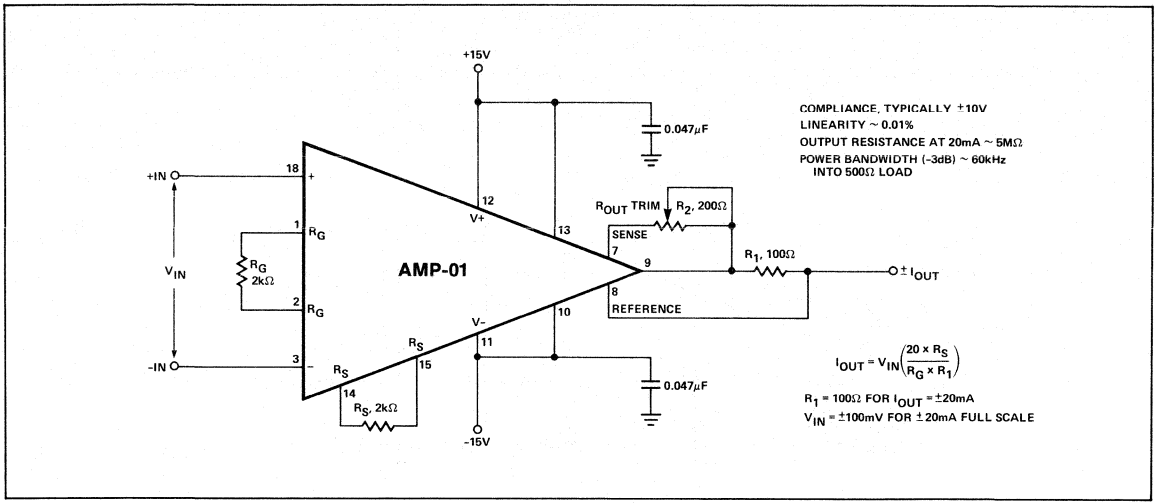


Figure 7. High-compliance bipolar current source with 13-bit linearity.

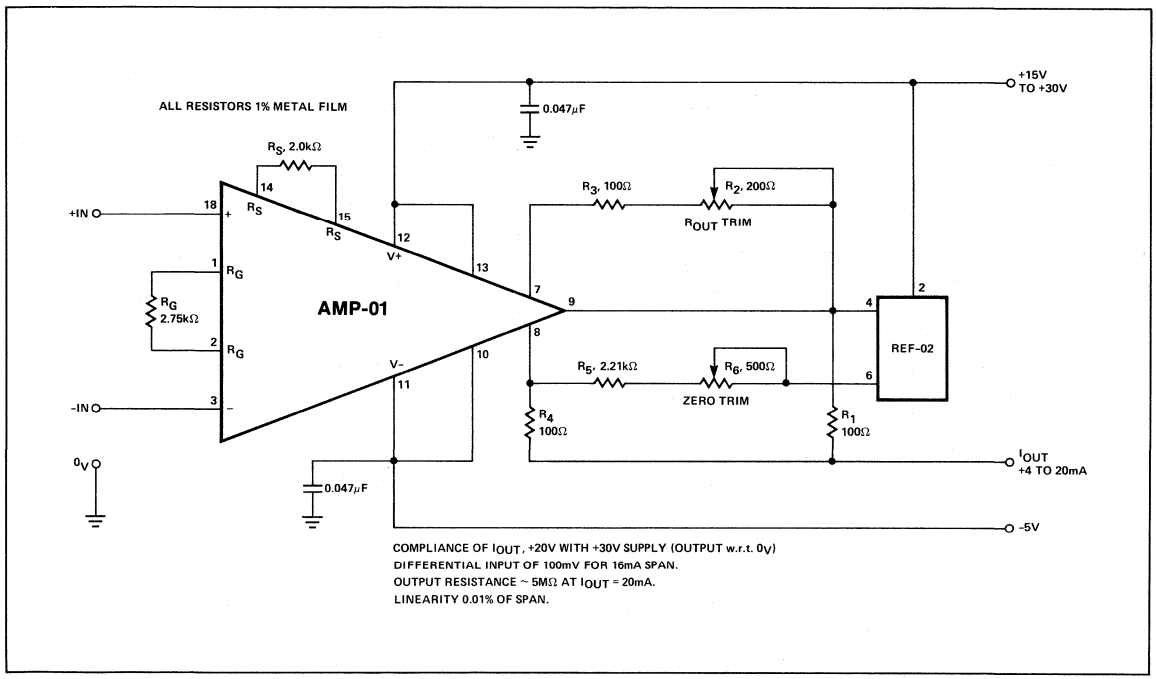


Figure 8. 13-bit linear 4-20mA transmitter constructed by adding a voltage reference. Thermocouple signals can be accepted without preamplification.

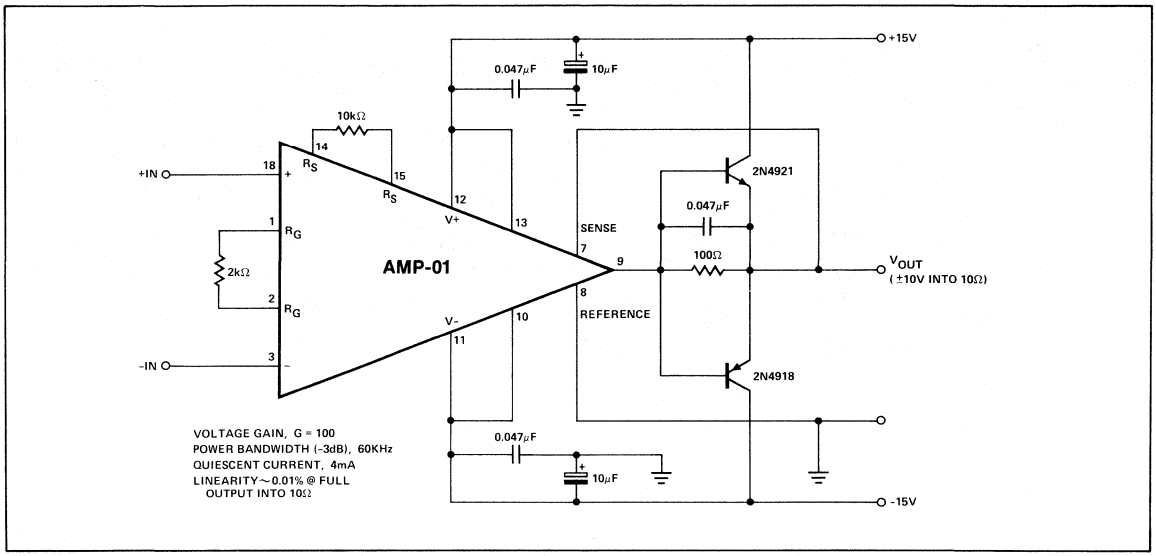


Figure 9. Adding two transistors increases output current to ±1A without affecting the quiescent current of 4mA. Power bandwidth is 60kHz.

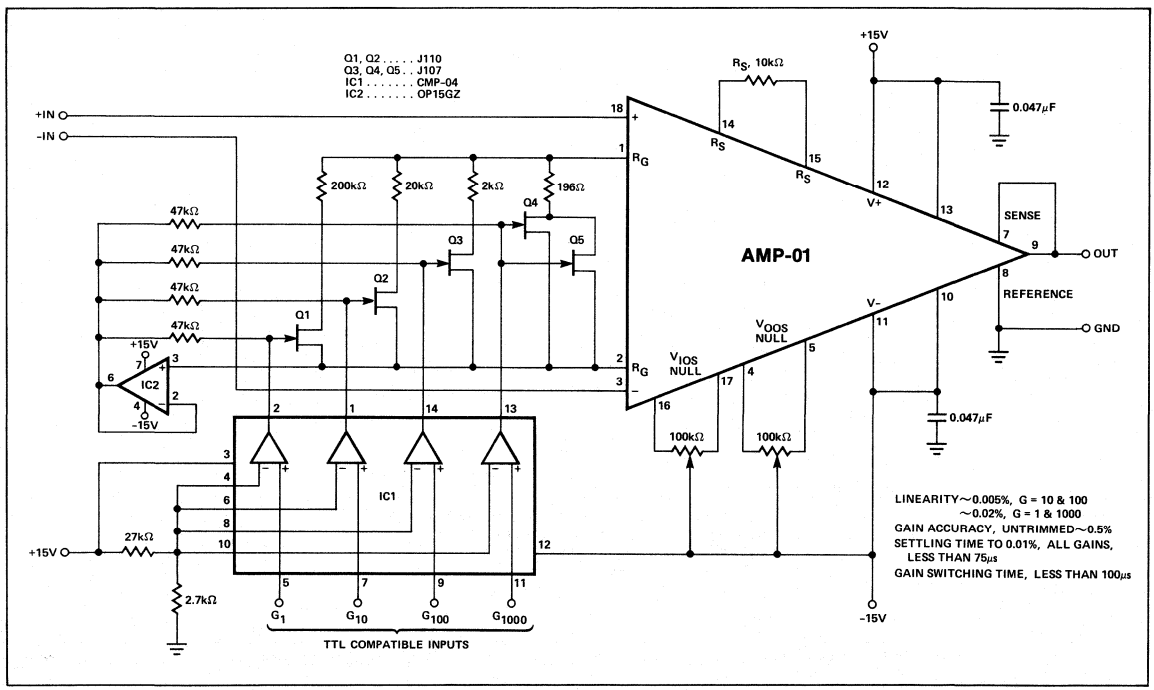


Figure 10. The AMP-01 makes an excellent programmable-gain instrumentation amplifier. Combined gain-switching and settling time to 13-bits falls below 100μs. Linearity is better than 12-bits over a gain range 1 to 1000.

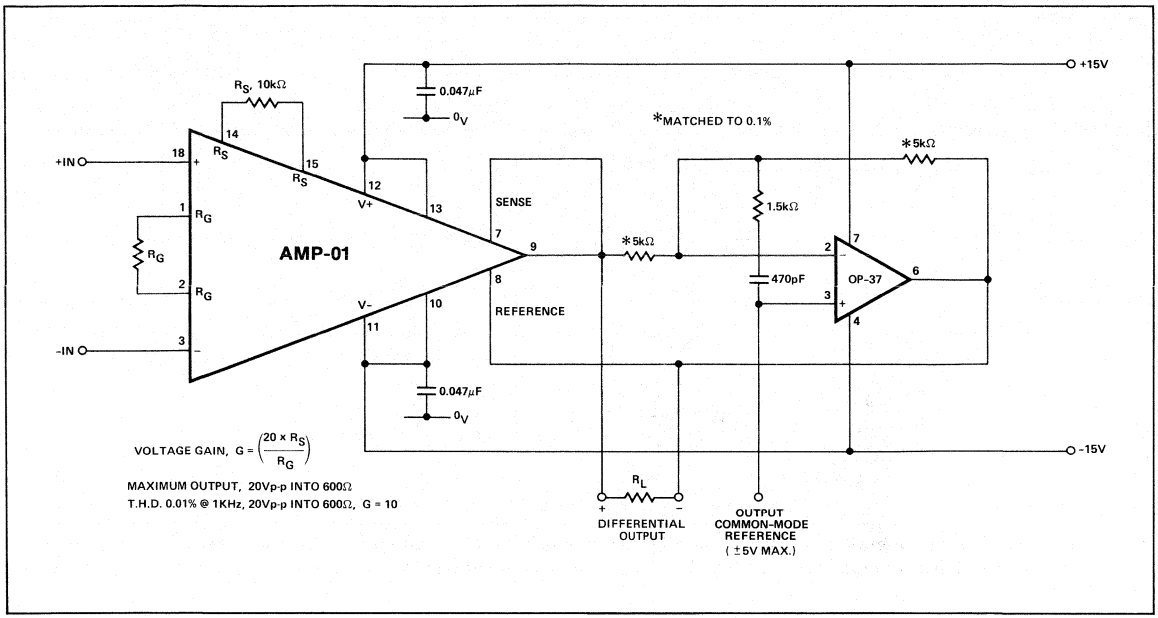


Figure 11. A differential input instrumentation amplifier with differential output replaces a transformer in many applications. The output will drive a 600Ω load at low distortion, (0.01%).

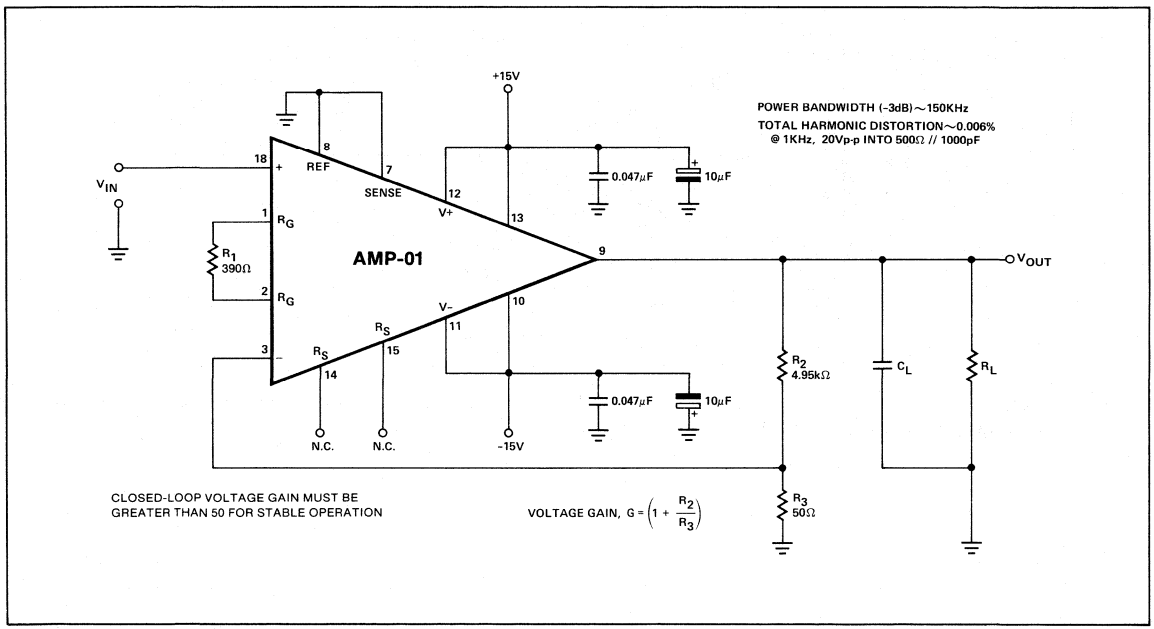


Figure 12. Configuring the AMP-01 as a noninverting operational amplifier provides exceptional performance. The output handles low load impedances at very low distortion, 0.006%.

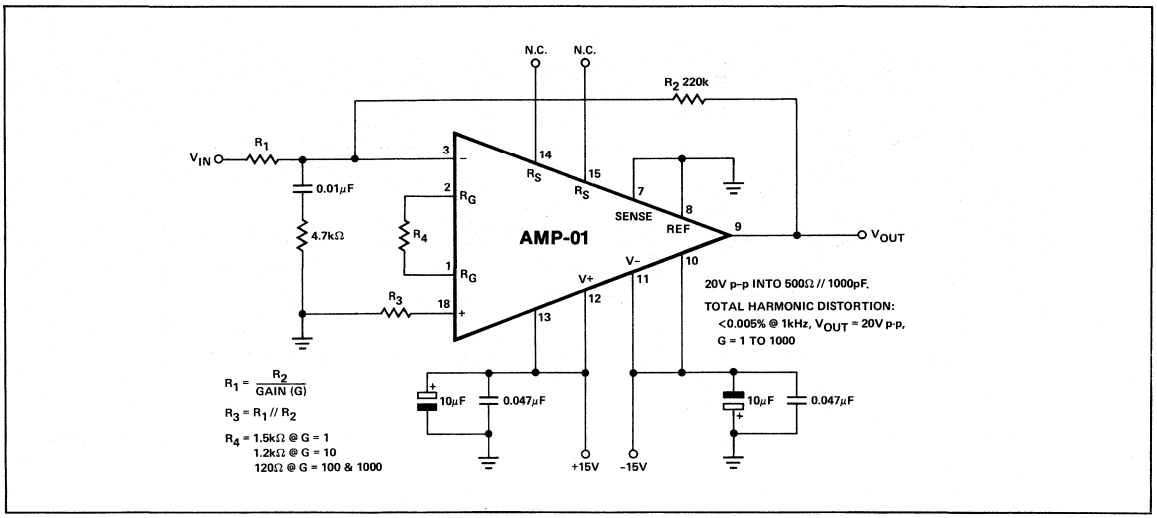


Figure 13. The inverting operational amplifier configuration has excellent linearity over the gain range 1 to 1000, typically 0.005%. Offset voltage drift at unity gain is improved over the drift in the instrumentation amplifier configuration.

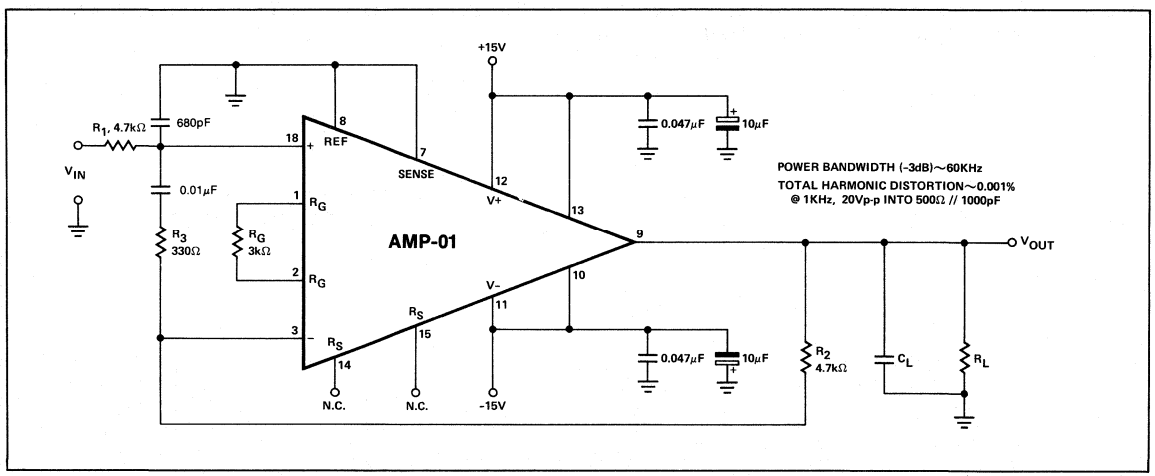
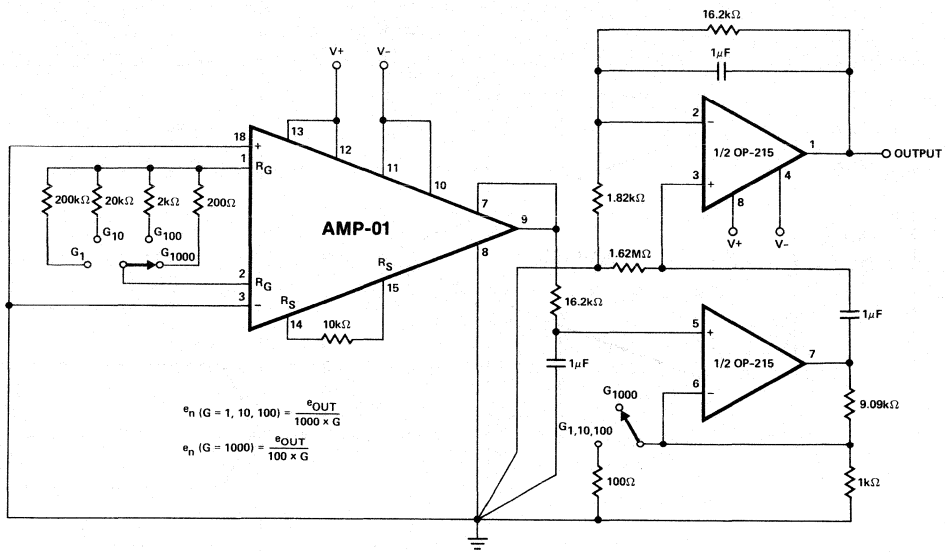
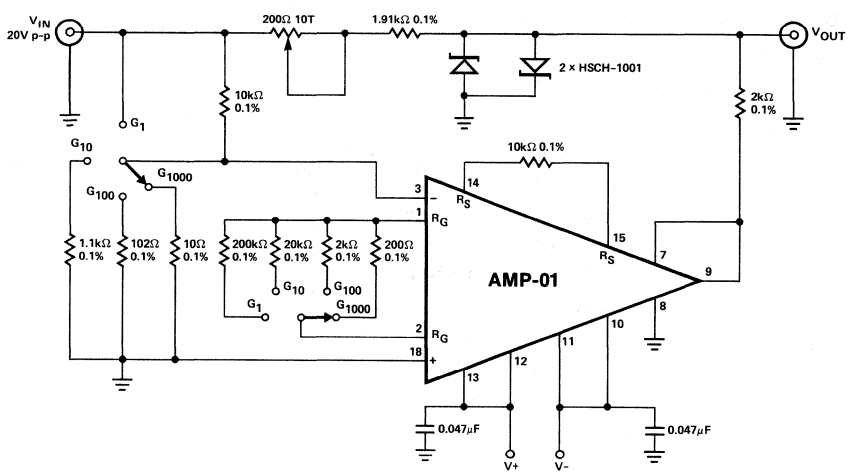


Figure 14. Stability with large capacitive loads combined with high output current capability make the AMP-01 ideal for line driving applications. Offset voltage drift approaches the TCV_{IOS} limit, (0.3μV/° C).

NOISE TEST CIRCUIT (0.1Hz to 10Hz)

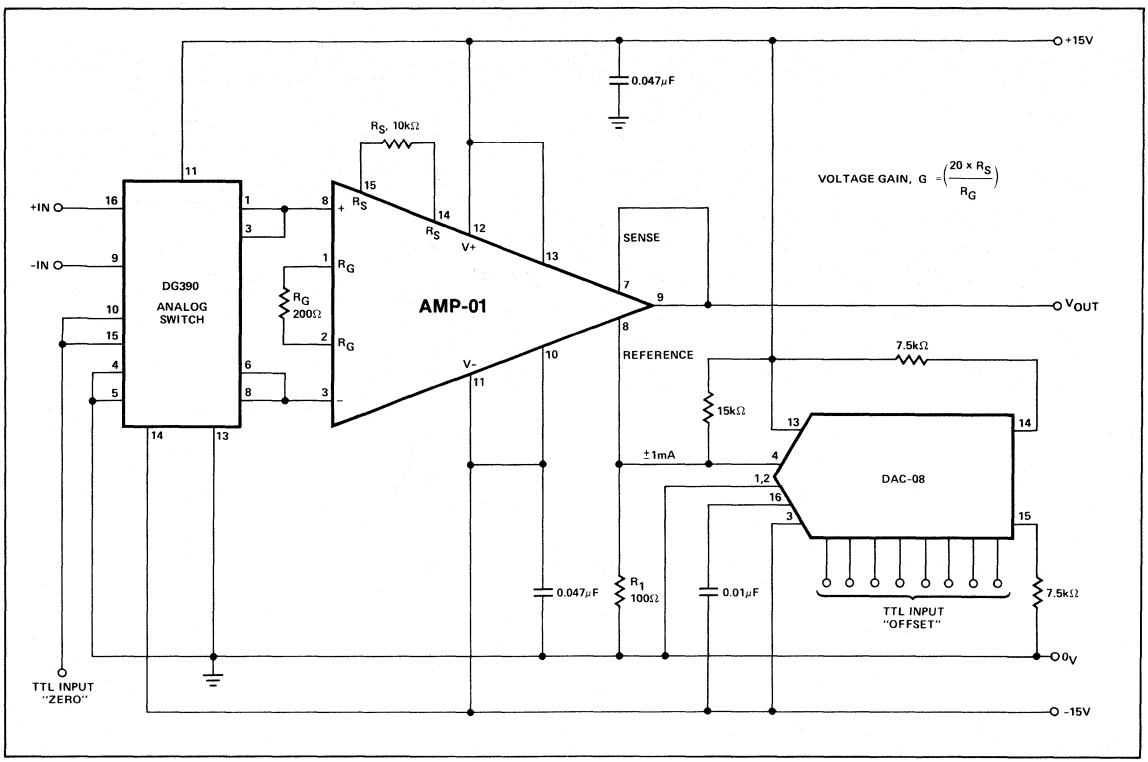


SETTLING-TIME TEST CIRCUIT

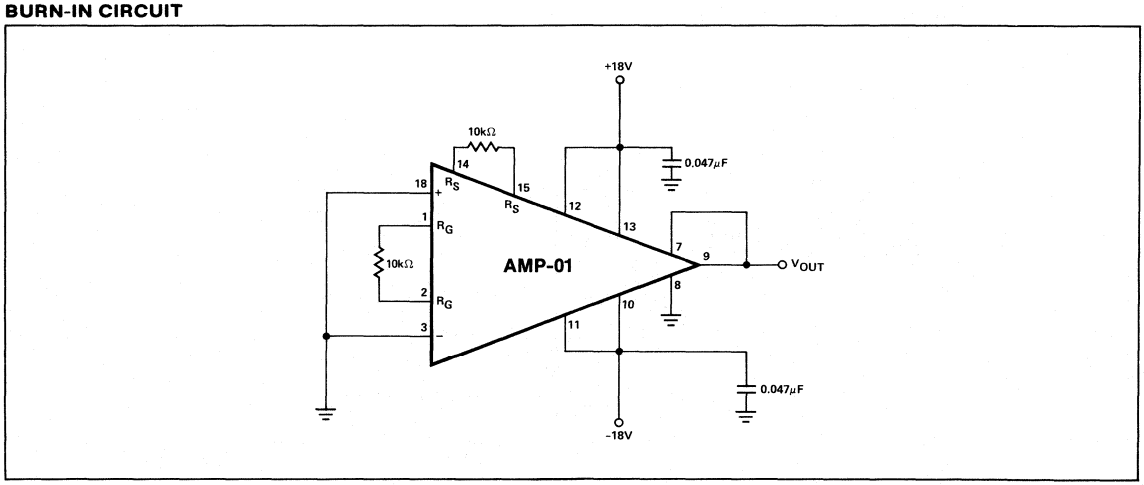


AMP-01

INSTRUMENTATION AMPLIFIER WITH AUTO-ZERO



BURN-IN CIRCUIT



ANALOG DEVICES

High Accuracy 8-Pin Instrumentation Amplifier

AMP-02

FEATURES

- Low Offset Voltage ..... 100μV Max
- Low Drift ..... 2μV/°C Max
- Wide Gain Range ..... 1 to 10,000
- High Common-Mode Rejection ..... 115dB Min
- High Bandwidth (G = 1000) ..... 200kHz Typ
- Gain Equation Accuracy ..... 0.5% Max
- Single Resistor Gain Set
- Input Overvoltage Protection
- Low Cost
- Available in Die Form

APPLICATIONS

- Differential Amplifier
- Strain Gauge Amplifier
- Thermocouple Amplifier
- RTD Amplifier
- Programmable Gain Instrumentation Amplifier
- Medical Instrumentation
- Data Acquisition Systems

ORDERING INFORMATION †

T_A = +25°C V_{IOS} MAX (μV)	T_A = +25°C V_{OOS} MAX (mV)	PLASTIC 8-PIN	OPERATING TEMPERATURE RANGE
100	4	AMP02EP	XIND
200	8	AMP02FP	XIND

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

The AMP-02 is the first precision instrumentation amplifier available in an 8-pin package. Gain of the AMP-02 is set by a single external resistor, and can range from 1 to 10,000. No gain set resistor is required for unity gain. The AMP-02 includes an input protection network that allows the inputs to be taken 60V beyond either supply rail without damaging the device.

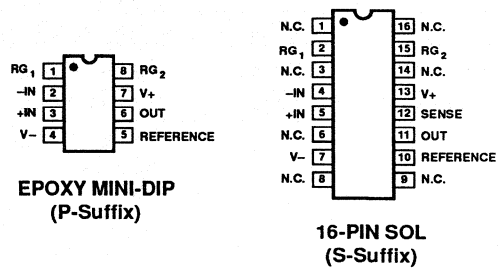
Laser trimming reduces the input offset voltage to under 100μV. Output offset voltage is below 4mV and gain accuracy is better than 0.5% for gain of 1000. PMI's proprietary thin-film resistor process keeps the gain temperature coefficient under 50 ppm/°C.

Due to the AMP-02's design, its bandwidth remains very high over a wide range of gain. Slew rate is over 4V/μs making the AMP-02 ideal for fast data acquisition systems.

A reference pin is provided to allow the output to be referenced to an external DC level. This pin may be used for offset correction or level shifting as required. In the 8-pin package, sense is internally connected to the output.

For an instrumentation amplifier with the highest precision, consult the AMP-01 data sheet. For the highest input impedance and speed, consult the AMP-05 data sheet.

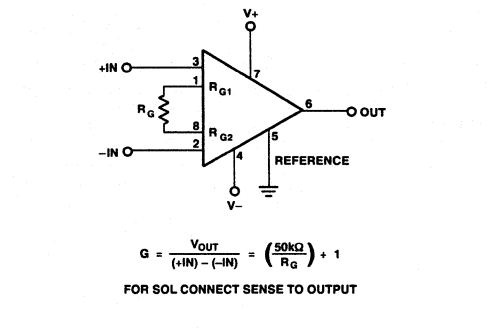
PIN CONNECTIONS



EPOXY MINI-DIP (P-Suffix)

16-PIN SOL (S-Suffix)

BASIC CIRCUIT CONNECTIONS



$$G = \frac{V_{OUT}}{(+IN) - (-IN)} = \left(\frac{50k\Omega}{R_G}\right) + 1$$

FOR SOL CONNECT SENSE TO OUTPUT

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
Common-Mode Input Voltage ..... [(V–) – 60V] to [(V+) + 60V]
Differential Input Voltage ..... [(V–) – 60V] to [(V+) + 60V]
Output Short-Circuit Duration ..... Continuous
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
8-Pin Plastic DIP (P)	96	37	°C/W
16-Pin SOL (S)	92	27	°C/W

NOTE:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP package; Θ_{JA} is specified for device soldered to printed circuit board for SOL package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $V_{CM} = 0V$, $T_A = +25°C$, unless otherwise noted.

			AMP-02E			AMP-02F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
OFFSET VOLTAGE									
Input Offset Voltage	V_{IOS}	$T_A = +25°C$	–	20	100	–	40	200	µV
		$-40°C \le T_A \le +85°C$	–	50	200	–	100	350	
Input Offset Voltage Drift	TCV_{IOS}	$-40°C \le T_A \le +85°C$	–	0.5	2	–	1	4	µV/°C
Output Offset Voltage	V_{OOS}	$T_A = +25°C$	–	1	4	–	2	8	mV
		$-40°C \le T_A \le +85°C$	–	4	10	–	9	20	
Output Offset Voltage Drift	TCV_{OOS}	$-40°C \le T_A \le +85°C$	–	50	100	–	100	200	µV/°C
Power Supply Rejection	PSR	$V_S = \pm4.8V$ to $\pm18V$							
		G = 1000	115	128	–	110	115	–	dB
		G = 100	115	125	–	110	115	–	
		G = 10	100	110	–	95	100	–	
		G = 1	80	90	–	75	80	–	
		$V_S = \pm4.8V$ to $\pm18V$, $-40°C \le T_A \le +85°C$							
		G = 1000	110	120	–	105	110	–	dB
		G = 100	110	120	–	105	110	–	
		G = 10	95	110	–	90	95	–	
		G = 1	75	90	–	70	75	–	
INPUT CURRENT									
Input Bias Current	I_B	$T_A = +25°C$	–	2	10	–	4	20	nA
		$-40°C \le T_A \le +85°C$	–	12	30	–	20	40	
Input Bias Current Drift	TCI_B	$-40°C \le T_A +85°C$	–	150	–	–	250	–	pA/°C
Input Offset Current	I_{OS}	$T_A = +25°C$	–	1.2	5	–	2	10	nA
		$-40°C \le T_A \le +85°C$	–	1.8	15	–	3	20	
Input Offset Current Drift	TCI_{OS}	$-40°C \le T_A \le +85°C$	–	9	–	–	15	–	pA/°C
INPUT									
Input Resistance	R_{IN}	Differential, G ≤ 1000	–	10	–	–	10	–	GΩ
		Common-Mode, G = 1000	–	16.5	–	–	16.5	–	
Input Voltage Range	IVR	$T_A = +25°C$ (Note 3)	±11	–	–	±11	–	–	V
		$-40°C \le T_A \le +85°C$	±11	–	–	±11	–	–	
Common-Mode Rejection	CMR	$V_{CM} = \pm11V$							
		G = 1000	115	120	–	110	115	–	dB
		G = 100	115	120	–	110	115	–	
		G = 10	100	115	–	95	110	–	
		G = 1	80	95	–	75	90	–	
		$V_{CM} = \pm11V$, $-40°C \le T_A \le +85°C$							
		G = 1000	110	120	–	105	115	–	dB
		G = 100	110	120	–	105	115	–	
		G = 10	95	110	–	90	105	–	
		G = 1	75	90	–	70	85	–	

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = +25°C$, unless otherwise noted. *Continued*

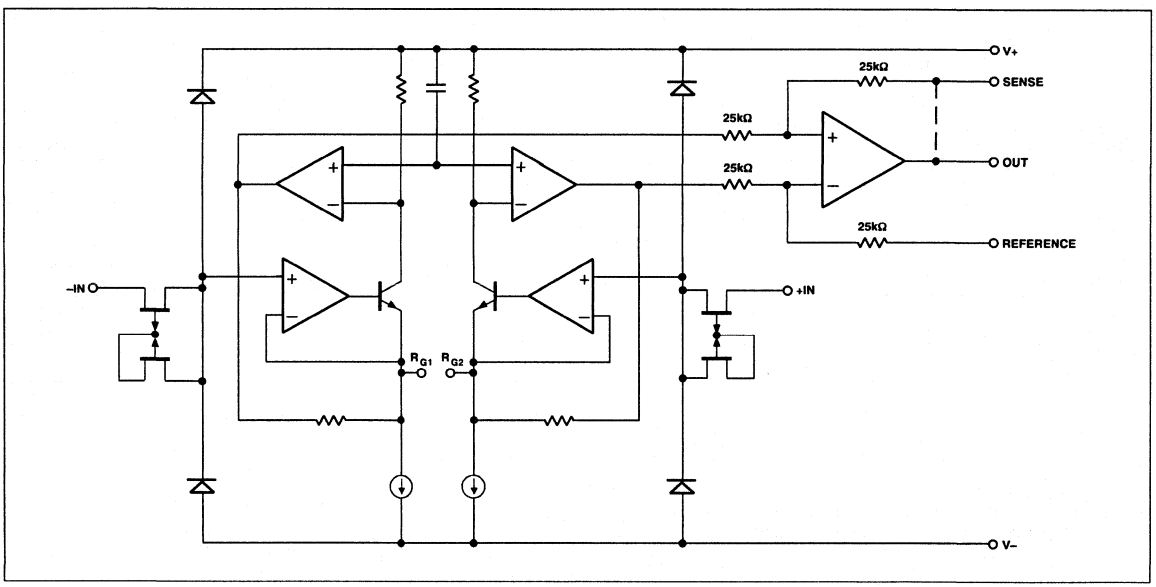
PARAMETER	SYMBOL	CONDITIONS	AMP-02E MIN	AMP-02E TYP	AMP-02E MAX	AMP-02F MIN	AMP-02F TYP	AMP-02F MAX	UNITS
GAIN									
Gain Equation Accuracy	$G = \frac{50k\Omega}{R_G} + 1$	G = 1000	–	–	0.50	–	–	0.70	%
		G = 100	–	–	0.30	–	–	0.50	
		G = 10	–	–	0.25	–	–	0.40	
		G = 1	–	–	0.02	–	–	0.05	
Gain Range	G		1	–	10k	1	–	10k	V/V
Nonlinearity		G = 1 to 1000	–	0.006	–	–	0.006	–	%
Temperature Coefficient	G_{TC}	$1 \le G \le 1000$ (Notes 1, 2)	–	20	50	–	20	50	ppm/°C
OUTPUT RATING									
Output Voltage Swing	V_{OUT}	$T_A = +25°C$, $R_L = 1k\Omega$	±12	±13	–	±12	±13	–	V
		$R_L = 1k\Omega$, $-40°C \le T_A \le +85°C$	±11	±12	–	±11	±12	–	
Positive Current Limit		Output-to-Ground Short	–	22	–	–	22	–	mA
Negative Current Limit		Output-to-Ground Short	–	32	–	–	32	–	mA
NOISE									
Voltage Density, RTI	e_n	f_O = 1kHz G = 1000	–	9	–	–	9	–	nV/√Hz
		G = 100	–	10	–	–	10	–	
		G = 10	–	18	–	–	18	–	
		G = 1	–	120	–	–	120	–	
Noise Current Density, RTI	i_n	f_O = 1kHz, G = 1000	–	0.4	–	–	0.4	–	pA/√Hz
Input Noise Voltage	$e_{n\ p\text{-}p}$	0.1Hz to 10Hz G = 1000	–	0.4	–	–	0.4	–	$\mu V_{p\text{-}p}$
		G = 100	–	0.5	–	–	0.5	–	
		G = 10	–	1.2	–	–	1.2	–	
		G = 1	–	10	–	–	10	–	
DYNAMIC RESPONSE									
Small-Signal Bandwidth (–3dB)	BW	G = 1	–	1200	–	–	1200	–	kHz
		G = 10	–	300	–	–	300	–	
		G = 100	–	200	–	–	200	–	
		G = 1000	–	200	–	–	200	–	
Slew Rate	SR	G = 10, $R_L = 1k\Omega$	4	6	–	4	6	–	V/µs
Settling Time	t_S	To 0.01% ±10V Step G = 1 to 1000	–	10	–	–	10	–	µs

NOTES:
1. Guaranteed by design.
2. Gain tempco does not include the effects of external component drift.
3. Input voltage range guaranteed by common-mode rejection test.

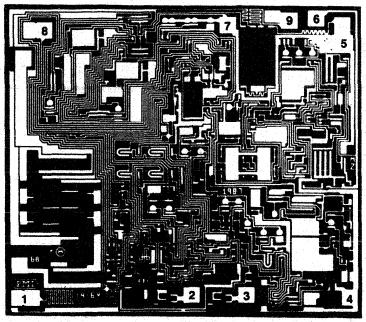
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = +25°C$, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	AMP-02E MIN	AMP-02E TYP	AMP-02E MAX	AMP-02F MIN	AMP-02F TYP	AMP-02F MAX	UNITS
SENSE INPUT									
Input Resistance	R_{IN}		–	25	–	–	25	–	kΩ
Voltage Range			–	±11	–	–	±11	–	V
REFERENCE INPUT									
Input Resistance	R_{IN}		–	50	–	–	50	–	kΩ
Voltage Range			–	±11	–	–	±11	–	V
Gain to Output			–	1	–	–	1	–	V/V
POWER SUPPLY									
Supply Voltage Range	V_S		±4.5	–	±18	±4.5	–	±18	V
Supply Current	I_{SY}	$T_A = +25°C$ $-40°C \le T_A \le +85°C$	– –	5 5	6 6	– –	5 5	6 6	mA

SIMPLIFIED SCHEMATIC



DICE CHARACTERISTICS



DIE SIZE 0.103 x 0.116 inch, 11,948 sq. mils
(2.62 x 2.95 mm, 7.73 sq. mm)

1. RG_1
2. –IN
3. +IN
4. V–
5. REFERENCE
6. OUT
7. V+
8. RG_2
9. SENSE

Connect Substrate to V–

4

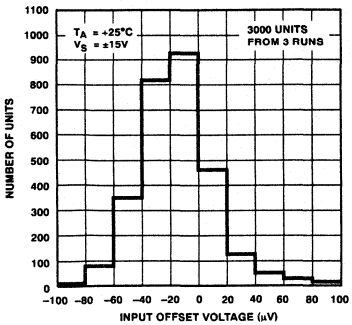
WAFER TEST LIMITS at $V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	AMP-02GBC LIMITS	UNITS
Input Offset Voltage	V_{IOS}		200	µV MAX
Output Offset Voltage	V_{OOS}		8	mV MAX
Power Supply Rejection	PSR	$V_S = \pm 4.8V$ to $\pm 18V$		
		G = 1000	110	dB MIN
		G = 100	110	
		G = 10	95	
		G = 1	75	
Input Bias Current	I_B		20	nA MAX
Input Offset Current	I_{OS}		10	nA MAX
Input Voltage Range	IVR	Guaranteed by CMR Tests	±11	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$		
		G = 1000	110	dB MIN
		G = 100	110	
		G = 10	95	
		G = 1	75	
Gain Equation Accuracy		$G = \frac{50k\Omega}{R_G} + 1$, G = 1000	0.7	% MAX
Output Voltage Swing	V_{OUT}	$R_L = 1k\Omega$	±12	V MIN
Supply Current	I_{SY}		6	mA MAX

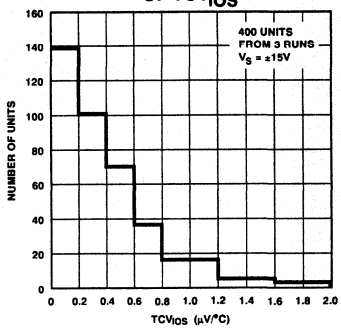
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

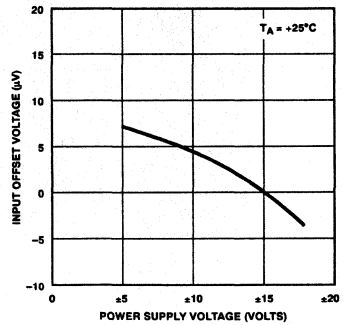
TYPICAL DISTRIBUTION OF INPUT OFFSET VOLTAGE



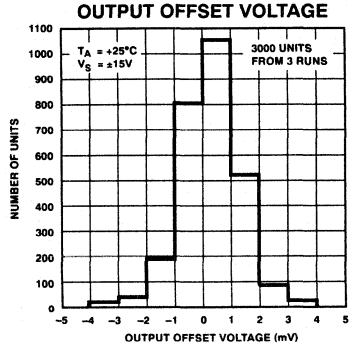
TYPICAL DISTRIBUTION OF TCV_{IOS}



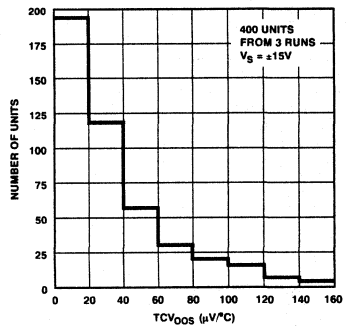
INPUT OFFSET VOLTAGE CHANGE vs SUPPLY VOLTAGE



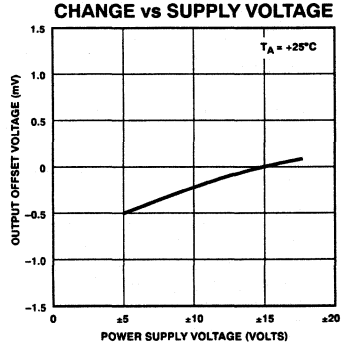
TYPICAL DISTRIBUTION OF OUTPUT OFFSET VOLTAGE



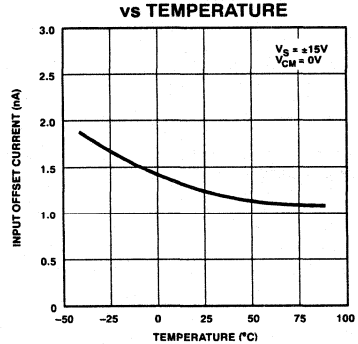
TYPICAL DISTRIBUTION OF TCV_{OOS}



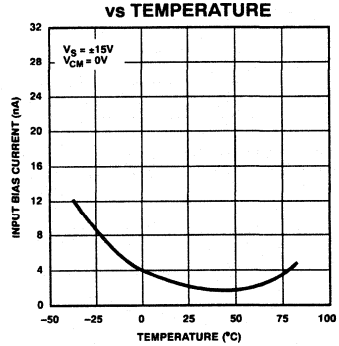
OUTPUT OFFSET VOLTAGE CHANGE vs SUPPLY VOLTAGE



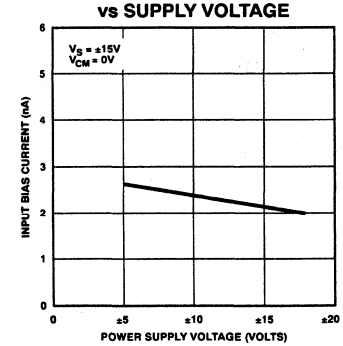
INPUT OFFSET CURRENT vs TEMPERATURE



INPUT BIAS CURRENT vs TEMPERATURE

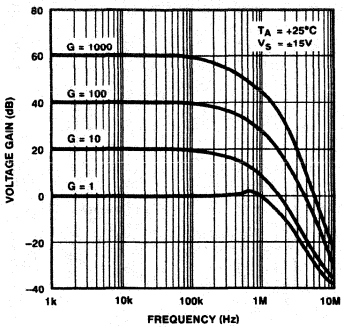


INPUT BIAS CURRENT vs SUPPLY VOLTAGE

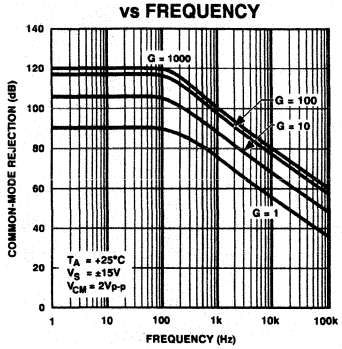


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

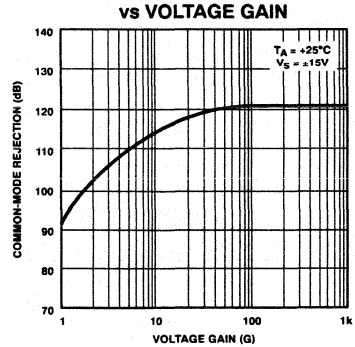
CLOSED-LOOP VOLTAGE GAIN vs FREQUENCY



COMMON-MODE REJECTION vs FREQUENCY

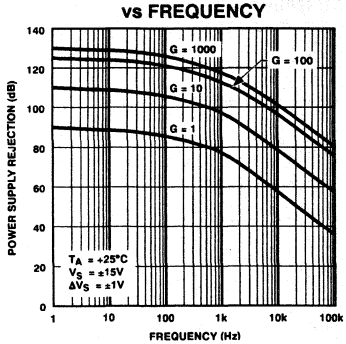


COMMON-MODE REJECTION vs VOLTAGE GAIN

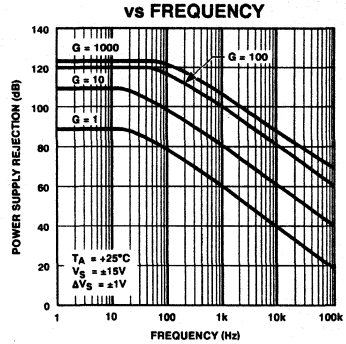


4

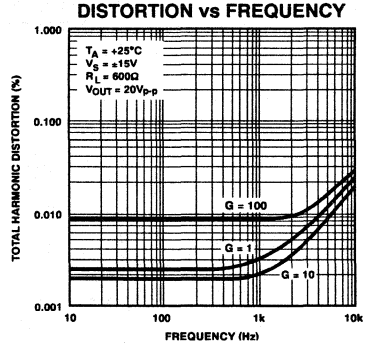
POSITIVE PSR vs FREQUENCY



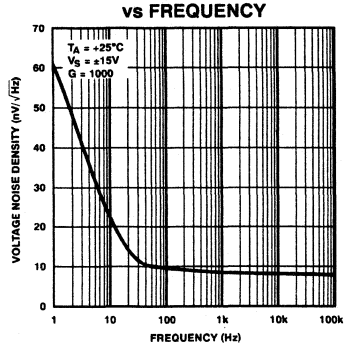
NEGATIVE PSR vs FREQUENCY



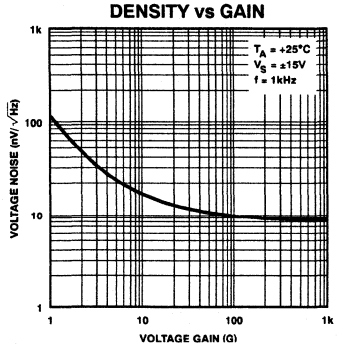
TOTAL HARMONIC DISTORTION vs FREQUENCY



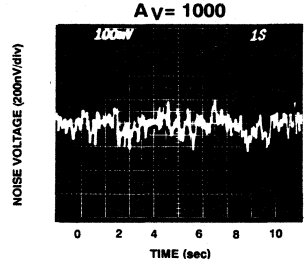
VOLTAGE NOISE DENSITY vs FREQUENCY



RTI VOLTAGE NOISE DENSITY vs GAIN

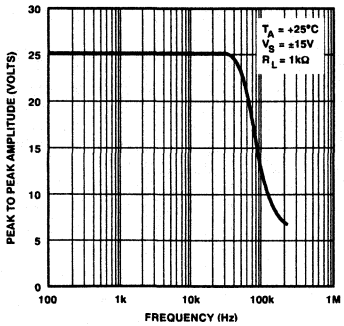


0.1Hz TO 10Hz NOISE A_V = 1000

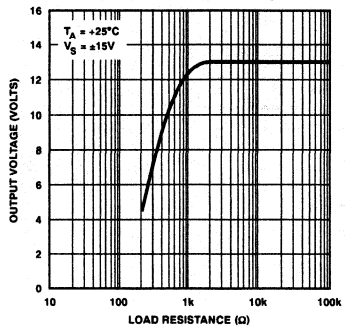


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

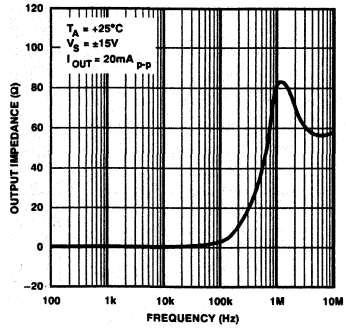
MAXIMUM OUTPUT SWING vs FREQUENCY



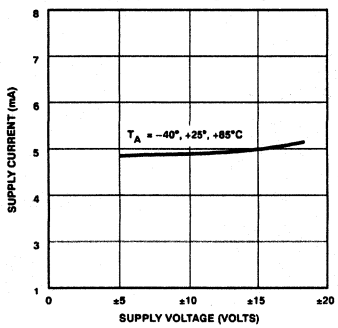
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



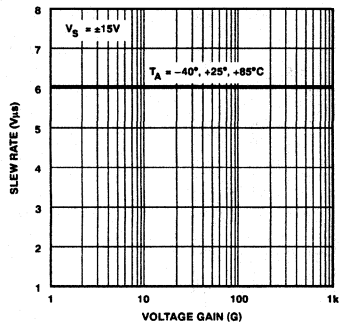
CLOSED LOOP OUTPUT IMPEDANCE vs FREQUENCY



SUPPLY CURRENT vs SUPPLY VOLTAGE



SLEW RATE vs VOLTAGE GAIN



APPLICATIONS INFORMATION

INPUT AND OUTPUT OFFSET VOLTAGES

Instrumentation amplifiers have independent offset voltages associated with the input and output stages. The input offset component is directly multiplied by the amplifier gain, whereas output offset is independent of gain. Therefore, at low gain, output-offset-errors dominate, while at high gain, input-offset-errors dominate. Overall offset voltage, V_{OS}, referred to the output (RTO) is calculated as follows:

$$V_{OS}\,(RTO) = (V_{IOS} \times G) + V_{OOS}$$

where V_{IOS} and V_{OOS} are the input and output offset voltage specifications and G is the amplifier gain.

The overall offset voltage drift TCV_{OS}, referred to the output, is a combination of input and output drift specifications. Input offset voltage drift is multiplied by the amplifier gain, G, and summed with the output offset drift:

$$TCV_{OS}\,(RTO) = (TCV_{IOS} \times G) + TCV_{OOS}$$

where TCV_{IOS} is the input offset voltage drift, and TCV_{OOS} is the output offset voltage drift. Frequently, the amplifier drift is referred back to the input (RTI) which is then equivalent to an input signal change:

$$TCV_{OS}\,(RTI) = TCV_{IOS} + \frac{TCV_{OOS}}{G}$$

For example, the maximum input-referred drift of an AMP-02EP set to G = 1000 becomes:

$$TCV_{OS}\,(RTI) = 2\mu V/°C + \frac{100\mu V/°C}{1000} = 2.1\mu V/°C$$

INPUT BIAS AND OFFSET CURRENTS

Input transistor bias currents are additional error sources which can degrade the input signal. Bias currents flowing through the signal source resistance appear as an additional offset voltage. Equal source resistance on both inputs of an IA will minimize offset changes due to bias current variations with signal voltage and temperature. However, the difference between the two bias currents, the input offset current, produces an error. The magnitude of the error is the offset current times the source resistance.

A current path must always be provided between the differential inputs and analog ground to ensure correct amplifier operation. Floating inputs, such as thermocouples, should be grounded close to the signal source for best common-mode rejection.

GAIN

The AMP-02 only requires a single external resistor to set the voltage gain. The voltage gain, G, is:

$$G = \frac{50k\Omega}{R_G} + 1$$

and

$$R_G = \frac{50k\Omega}{G - 1}$$

The voltage gain can range from 1 to 10,000. A gain set resistor is not required for unity-gain applications. Metal-film or wire-wound resistors are recommended for best results.

The total gain accuracy of the AMP-02 is determined by the tolerance of the external gain set resistor, R_G, combined with the gain equation accuracy of the AMP-02. Total gain drift combines the mismatch of the external gain set resistor drift with that of the internal resistors (20ppm/°C typ). Maximum gain drift of the AMP-02 independent of the external gain set resistor is 50 ppm/°C.

All instrumentation amplifiers require attention to layout so thermocouple effects are minimized. Thermocouples formed between copper and dissimilar metals can easily destroy the TCV_{OS} performance of the AMP-02 which is typically 0.5μV/°C. Resistors themselves can generate thermoelectric EMFs when mounted parallel to a thermal gradient.

The AMP-02 uses the triple op amp instrumentation amplifier configuration with the input stage consisting of two transimpedance amplifiers followed by a unity-gain differential amplifier. The input stage and output buffer are laser-trimmed to increase gain accuracy. The AMP-02 maintains wide bandwidth at all gains as shown in Figure 1. For voltage gains greater than 10, the bandwidth is over 200kHz. At unity-gain, the bandwidth of the AMP-02 exceeds 1MHz.

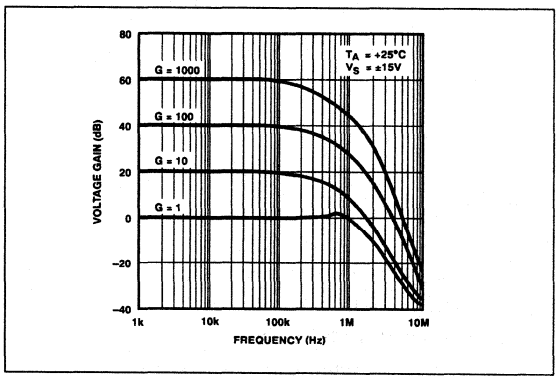


FIGURE 1: *The AMP-02 keeps its bandwidth at high gains.*

COMMON-MODE REJECTION

Ideally, an instrumentation amplifier responds only to the difference between the two input signals and rejects common-mode voltages and noise. In practice, there is a small change in output voltage when both inputs experience the same common-mode voltage change; the ratio of these voltages is called the common-mode gain. Common-mode rejection (CMR) is the logarithm of the ratio of differential-mode gain to common-mode gain, expressed in dB. Laser trimming is used to achieve the high CMR of the AMP-02.

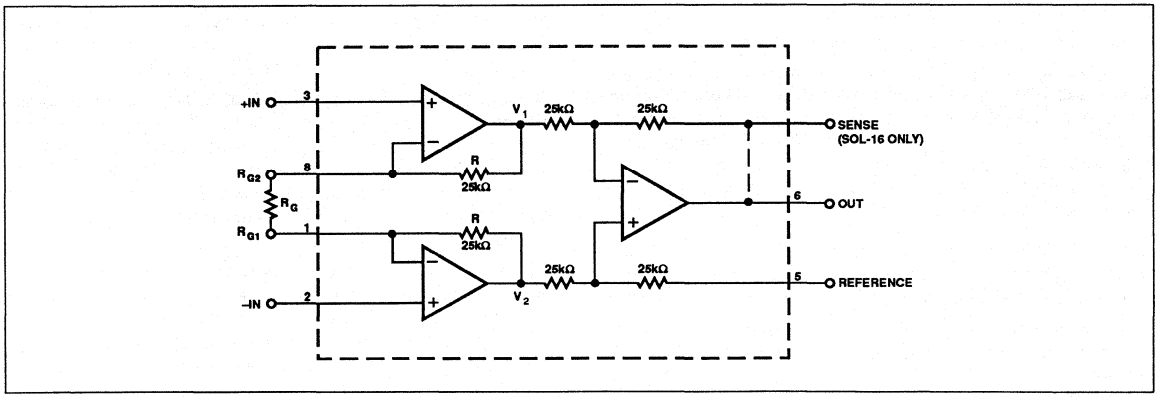


FIGURE 2: *Triple Op Amp Topology of the AMP-02*

Figure 2 shows the triple op amp configuration of the AMP-02. With all instrumentation amplifiers of this type, it is critical not to exceed the dynamic range of the input amplifiers. The amplified differential input signal and the input common-mode voltage must not force the amplifier's output voltage beyond ±12V (V_S = ±15V) or nonlinear operation will result.

The input stage amplifier's output voltages at V_1 and V_2 equals:

$$V_1 = -\left(1 + \frac{2R}{R_G}\right)\frac{V_D}{2} + V_{CM}$$

$$= -G\frac{V_D}{2} + V_{CM}$$

$$V_2 = \left(1 + \frac{2R}{R_G}\right)\frac{V_D}{2} + V_{CM}$$

$$= G\frac{V_D}{2} + V_{CM}$$

where

V_D = Differential input voltage
= (+IN) – (–IN)

V_{CM} = Common-mode input voltage

G = Gain of instrumentation amplifier

If V_1 and V_2 can equal ±12V maximum, then the common-mode input voltage range is:

$$CMVR = \pm\left(12V - \frac{GV_D}{2}\right)$$

GROUNDING

The majority of instruments and data acquisition systems have separate grounds for analog and digital signals. Analog ground may also be divided into two or more grounds which will be tied together at one point, usually the analog power-supply ground. In addition, the digital and analog grounds may be joined, normally at the analog ground pin on the A to D converter. Following this basic practice is essential for good circuit performance.

Mixing grounds causes interactions between digital circuits and the analog signals. Since the ground returns have finite resistance and inductance, hundreds of millivolts can be developed between the system ground and the data acquisition components. Using separate ground returns minimizes the current flow in the sensitive analog return path to the system ground point. Consequently, noisy ground currents from logic gates do not interact with the analog signals.

Inevitably, two or more circuits will be joined together with their grounds at differential potentials. In these situations, the differential input of an instrumentation amplifier, with its high CMR, can accurately transfer analog information from one circuit to another.

SENSE AND REFERENCE TERMINALS

The sense terminal completes the feedback path for the instrumentation amplifier output stage and is internally connected directly to the output. For SOL devices, connect the sense terminal to the output. The output signal is specified with respect to the reference terminal, which is normally connected to analog ground. The reference may also be used for offset correction or level shifting. A reference source resistance will reduce the common-mode rejection by the ratio of 25kΩ/R_{REF}. If the reference source resistance is 1Ω, then the CMR will be reduced to 88dB (25kΩ/1Ω = 88dB).

OVERVOLTAGE PROTECTION

Instrumentation amplifiers invariably sit at the front end of instrumentation systems where there is a high probability of exposure to overloads. Voltage transients, failure of a transducer, or removal of the amplifier power supply while the signal source is connected may destroy or degrade the performance of an unprotected device. A common technique used is to place limiting resistors in series with each input, but this adds noise. The AMP-02 includes internal protection circuitry that limits the input current to ±4mA for a 60V differential overload (see Figure 3) with power off, ±2.5mA with power on.

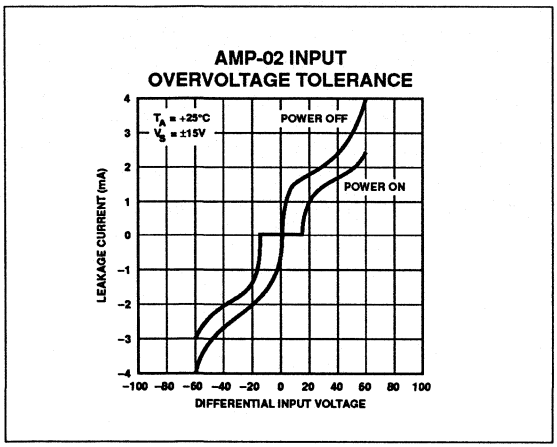


FIGURE 3: *AMP-02's input protection circuitry limits input current during overvoltage conditions.*

POWER SUPPLY CONSIDERATIONS

Achieving the rated performance of precision amplifiers in a practical circuit requires careful attention to external influences. For example, supply noise and changes in the nominal voltage directly affect the input offset voltage. A PSR of 80dB means that a change of 100mV on the supply, not an uncommon value, will produce a 10μV input offset change. Consequently, care should be taken in choosing a power unit that has a low output noise level, good line and load regulation, and good temperature stability. In addition, each power supply should be properly bypassed.

ANALOG DEVICES

Precision, Unity-Gain Differential Amplifier

AMP-03

FEATURES

- High CMRR ..... 100dB Typ
- Low Nonlinearity ..... 0.001% Max
- Low Distortion ..... 0.001% Typ
- Wide Bandwidth ..... 3MHz Typ
- Fast Slew Rate ..... 9.5V/μs Typ
- Fast Settling (0.01%) ..... 1μs Typ
- Low Cost

APPLICATIONS

- Summing Amplifiers
- Instrumentation Amplifiers
- Balanced Line Receivers
- Current-Voltage Conversion
- Absolute Value Amplifier
- 4-20mA Current Transmitter
- Precision Voltage Reference Applications
- Lower Cost and Higher Speed Version of INA105

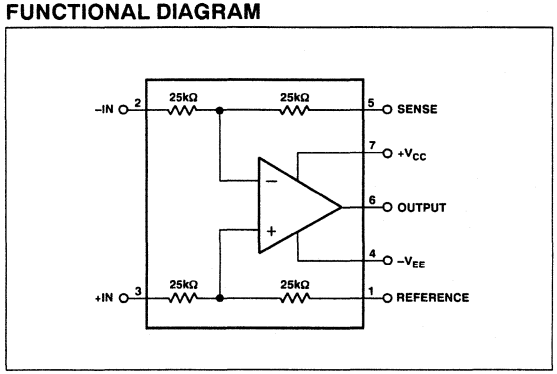
ORDERING INFORMATION †

PACKAGE		OPERATING TEMPERATURE RANGE
TO-99	PLASTIC 8-PIN	
AMP03BJ*	–	MIL
AMP03FJ	AMP03GP	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in plastic DIP, and TO-can packages.

FUNCTIONAL DIAGRAM



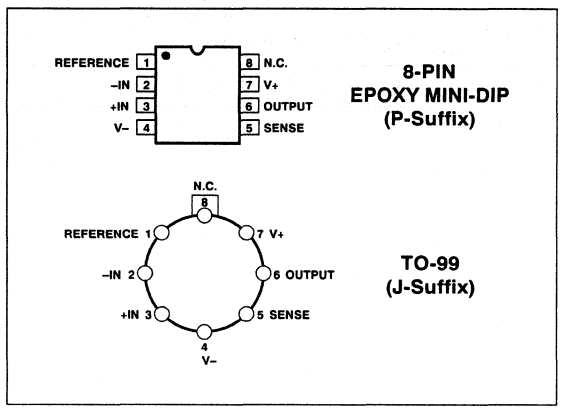
GENERAL DESCRIPTION

The AMP-03 is a monolithic unity-gain, high-speed differential amplifier. Incorporating a matched thin-film resistor network, the AMP-03 features stable operation over temperature without requiring expensive external matched components. The AMP-03 is a basic analog building block for differential amplifier and instrumentation applications.

The differential amplifier topology of the AMP-03 serves to both amplify the difference between two signals and provide extremely high rejection of the common-mode input voltage. By providing common-mode rejection (CMR) of 100dB typical, the AMP-03 solves common problems encountered in instrumentation design. As an example, the AMP-03 is ideal for performing either addition or subtraction of two signals without using expensive externally-matched precision resistors. The large common-mode rejection is made possible by matching the internal resistors to better than 0.002% and maintaining a thermally symmetric layout. Additionally, due to high CMR over frequency, the AMP-03 is an ideal general amplifier for buffering signals in a noisy environment into data acquisition systems.

The AMP-03 is a higher speed alternative to the INA105. Featuring slew rates of 9.5V/μs, and a bandwidth of 3MHz, the AMP-03 offers superior performance for high speed current sources, absolute value amplifiers, and summing amplifiers than the INA105.

PIN CONNECTIONS



AMP-03

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Input Voltage (Note 2) ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous
Storage Temperature Range
P, J Package ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C
Junction Temperature ..... +150°C
Operating Temperature Range
AMP-03B ..... –55°C to +125°C
AMP-03F, AMP-03G ..... –40°C to +85°C

PACKAGE TYPE	Θ_{JA} (Note 3)	Θ_{JC}	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO and P-DIP packages.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

			AMP-03F			AMP-03B			AMP-03G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Offset Voltage	V_{OS}	V_{CM} = 0V	–400	10	400	–700	20	700	–750	25	750	µV
Gain Error		No Load, V_{IN} = ±10V, R_S = 0Ω	–	0.00004	0.008	–	0.00004	0.008	–	0.001	0.008	%
Input Voltage Range	IVR		±20	–	–	±20	–	–	±20	–	–	V
Common-Mode Rejection	CMR	V_{CM} = ±10V	85	100	–	80	95	–	80	95	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±6V to ±18V	–	0.6	10	–	0.6	10	–	0.7	10	µV/V
Output Swing	V_O	R_L = 2kΩ	±12	±13.7	–	±12	±13.7	–	±12	±13.7	–	V
Short-Circuit Current Limit	I_{SC}	Output Shorted To Ground	+45/–15	–	–	+45/–15	–	–	+45/–15	–	–	mA
Small-Signal Bandwidth (–3dB)	BW	R_L = 2kΩ	–	3	–	–	3	–	–	3	–	MHz
Slew Rate	SR	R_L = 2kΩ	6	9.5	–	6	9.5	–	6	9.5	–	V/µs
Capacitive Load Drive Capability	C_L	No Oscillation	–	300	–	–	300	–	–	300	–	pF
Supply Current	I_{SY}	No Load	–	2.5	3.5	–	2.5	3.5	–	2.5	3.5	mA

ELECTRICAL CHARACTERISTICS at V_S = ±15V , –55°C ≤T_A ≤ +125°C for B grade. Continued

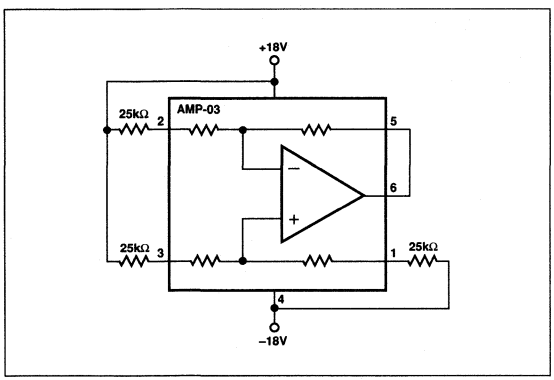
			AMP-03B			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Offset Voltage	V_{OS}	V_{CM} = 0V	–1500	150	1500	µV
Gain Error		No Load, V_{IN} = ±10V, R_S = 0Ω	–	0.0014	0.02	%
Input Voltage Range	IVR		±20	–	–	V
Common-Mode Rejection	CMR	V_{CM} = ±10V	75	95	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±6V to ±18V	–	0.7	20	µV/V
Output Swing	V_O	R_L = 2kΩ	±12	±13.7	–	V
Slew Rate	SR	R_L = 2kΩ	–	9.5	–	V/µs
Supply Current	I_{SY}	No Load	–	3.0	4.0	mA

4

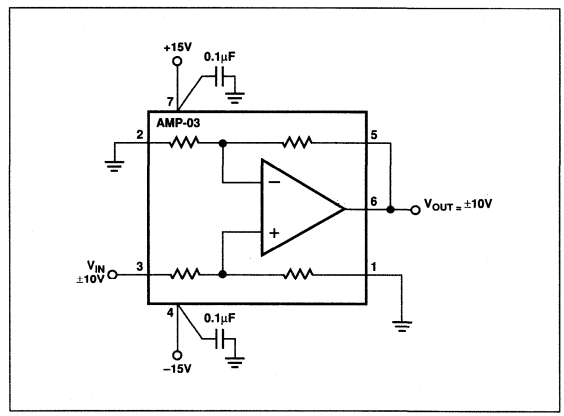
ELECTRICAL CHARACTERISTICS at V_S = ±15V, –40°C ≤ T_A ≤ +85°C for F and G grades.

			AMP-03F			AMP-03G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Offset Voltage	V_{OS}	V_{CM} = 0V	–1000	100	1000	–2000	200	2000	µV
Gain Error		No Load, V_{IN} = ±10V, R_S = 0Ω	–	0.0008	0.015	–	0.002	0.02	%
Input Voltage Range	IVR		±20	–	–	±20	–	–	V
Common-Mode Rejection	CMR	V_{CM} = ±10V	80	95	–	75	90	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±6V to ±18V	–	0.7	15	–	1.0	15	µV/V
Output Swing	V_O	R_L = 2kΩ	±12	±13.7	–	±12	±13.7	–	V
Slew Rate	SR	R_L = 2kΩ	–	9.5	–	–	9.5	–	V/µs
Supply Current	I_{SY}	No Load	–	2.6	4.0	–	2.6	4.0	mA

BURN-IN CIRCUIT

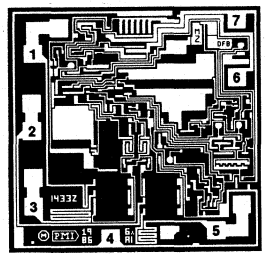


SLEW RATE TEST CIRCUIT



AMP-03

DICE CHARACTERISTICS



DIE SIZE 0.076 x 0.076 inch, 5,776 sq. mils
(1.93 x 1.93 mm, 3.73 sq. mm)

1. **REFERENCE**
2. **–IN**
3. **+IN**
4. **V–**
5. **SENSE**
6. **OUTPUT**
7. **V+**
8. **N.C.**

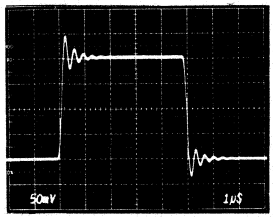
WAFER TEST LIMITS at V_S = ±15V, T_A = +25°C unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	AMP-03BC LIMITS	UNITS
Offset Voltage	V_{OS}	V_S = ±18V	0.5	mV MAX
Gain Error		No Load, V_{IN} = ±10V, R_S = 0Ω	0.008	% MAX
Input Voltage Range	IVR		±10	V MIN
Common-Mode Rejection	CMR	V_{CM} = ±10V	80	dB MIN
Power Supply Rejection Ratio	PSRR	V_S = ±6V to ±18V	8	µV/V MAX
Output Swing	V_O	R_L = 2kΩ	±12	V MAX
Short-Circuit Current Limit	I_{SC}	Output Shorted To Ground	+45/–15	mA MIN
Supply Current	I_{SY}	No Load	3.5	mA MAX

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

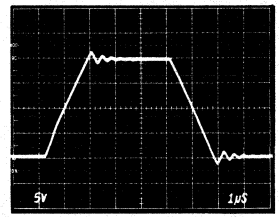
TYPICAL PERFORMANCE CHARACTERISTICS

SMALL-SIGNAL TRANSIENT RESPONSE



T_A = +25°C
V_S = ±15V

LARGE-SIGNAL TRANSIENT RESPONSE



T_A = +25°C
V_S = ±15V

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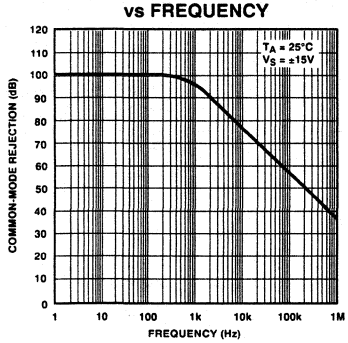
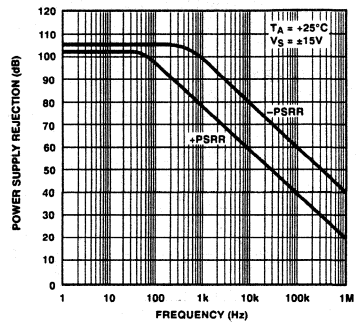
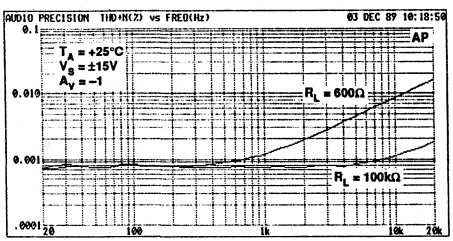
COMMON-MODE REJECTION vs FREQUENCY



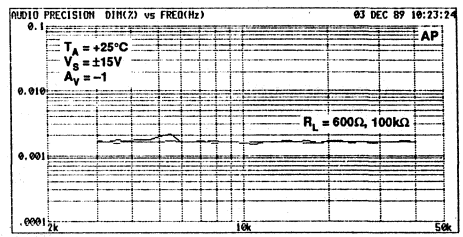
POWER SUPPLY REJECTION vs FREQUENCY



TOTAL HARMONIC DISTORTION vs FREQUENCY

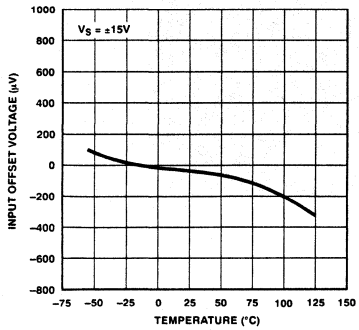


DYNAMIC INTERMODULATION DISTORTION vs FREQUENCY

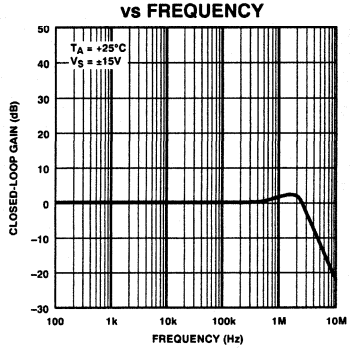


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

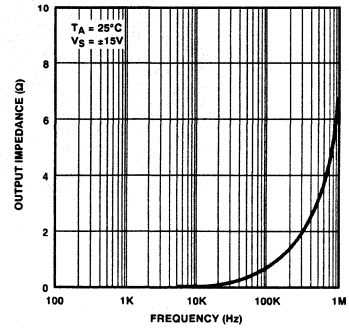
INPUT OFFSET VOLTAGE vs TEMPERATURE



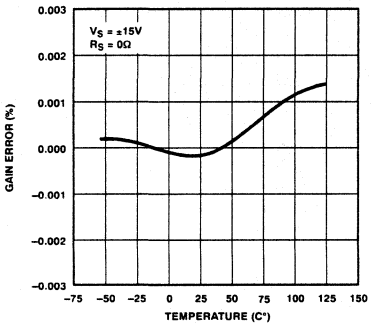
CLOSED-LOOP GAIN vs FREQUENCY



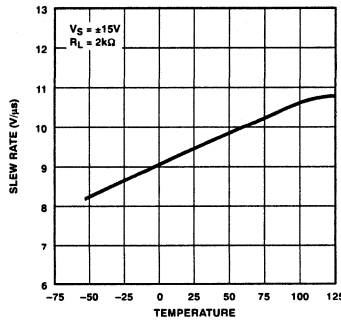
CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



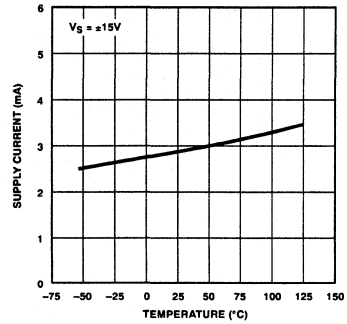
GAIN ERROR vs TEMPERATURE



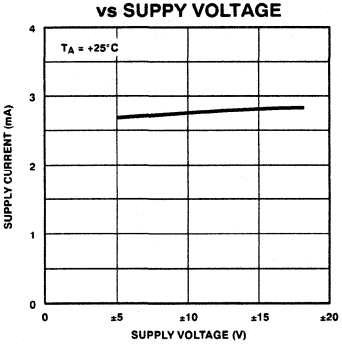
SLEW RATE vs TEMPERATURE



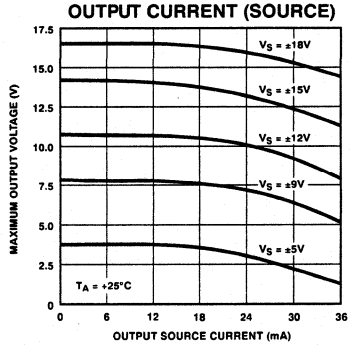
SUPPLY CURRENT vs TEMPERATURE



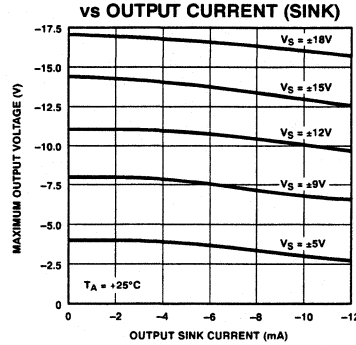
SUPPLY CURRENT vs SUPPY VOLTAGE



MAXIMUM OUTPUT VOLTAGE vs OUTPUT CURRENT (SOURCE)

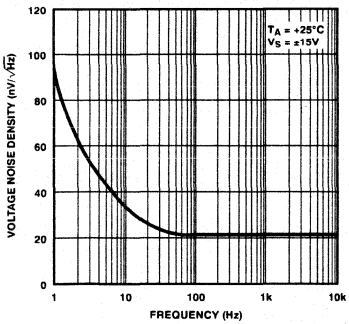


MAXIMUM OUTPUT VOLTAGE vs OUTPUT CURRENT (SINK)

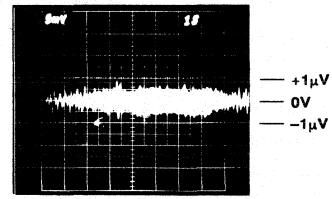


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

VOLTAGE NOISE DENSITY vs FREQUENCY

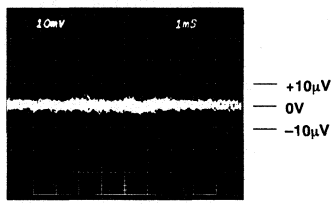


LOW FREQUENCY VOLTAGE NOISE



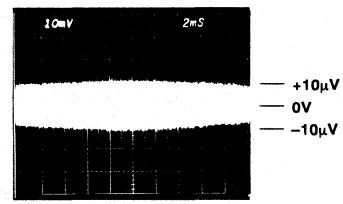
0.1 TO 10Hz PEAK-TO-PEAK NOISE

VOLTAGE NOISE FROM 0 TO 1kHz



T_A = +25°C
V_S = ±15V
NOTE: EXTERNAL AMPLIFIER GAIN = 1000;
THEREFORE, VERTICAL SCALE = 10μV/DIV.

VOLTAGE NOISE FROM 0 TO 10kHz



T_A = +25°C
V_S = ±15V
NOTE: EXTERNAL AMPLIFIER GAIN = 1000;
THEREFORE, VERTICAL SCALE = 10μV/DIV.

4

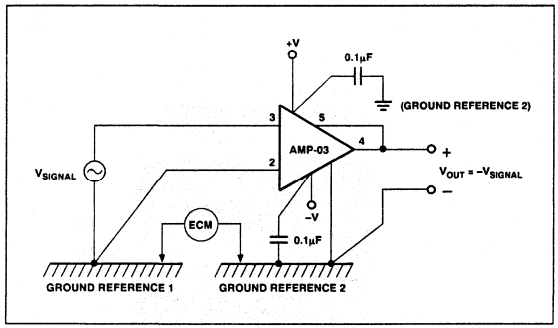


FIGURE 1: *AMP-03 serves to reject common-mode voltages in instrumentation systems. Common-mode voltages occur due to ground current returns. V_{SIGNAL} and E_{CM} must be within the common-mode range of AMP-03.*

APPLICATIONS INFORMATION

The AMP-03 represents a versatile analog building block. In order to capitalize on fast settling time, high slew rate, and high CMR, proper decoupling and grounding techniques must be employed. Figure 1 illustrates the use of 0.1μF decoupling capacitors and proper ground connections.

MAINTAINING COMMON-MODE REJECTION

In order to achieve the full common-mode rejection capability of the AMP-03, the source impedance must be carefully controlled. Slight imbalances of the source resistance will result in a degradation of DC CMR - even a 5Ω imbalance will degrade CMR by 20dB. Also, the matching of the reactive source impedance must be matched in order to preserve theCMRR over frequency.

APPLICATION CIRCUITS

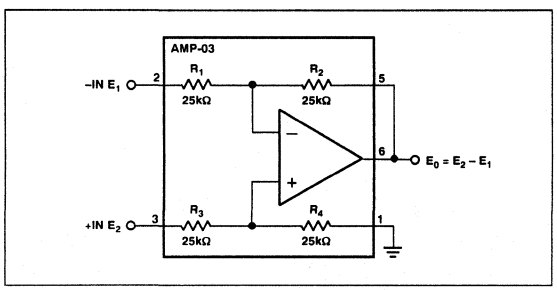


FIGURE 2: *Precision Difference Amplifier. Rejects Common-Mode Signal =* $\frac{[E_1 + E_2]}{2}$ *by 100dB*

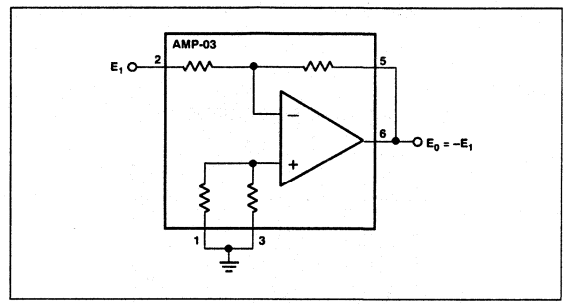


FIGURE 3: *Precision Unity-Gain Inverting Amplifier*

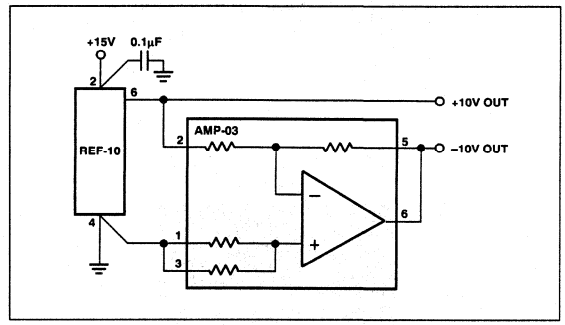


FIGURE 4: *±10V Precision Voltage Reference*

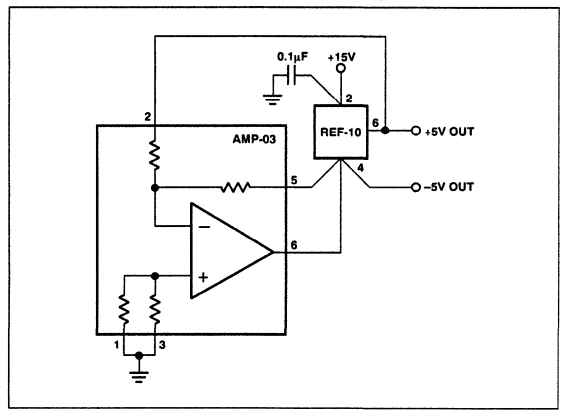


FIGURE 5: *±5V Precision Voltage Reference*

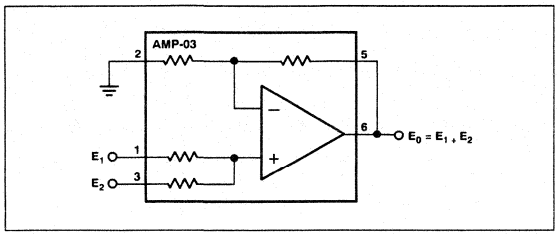


FIGURE 6: *Precision Summing Amplifier*

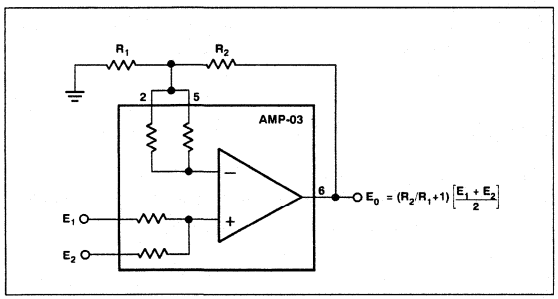


FIGURE 7: *Precision Summing Amplifier with Gain*

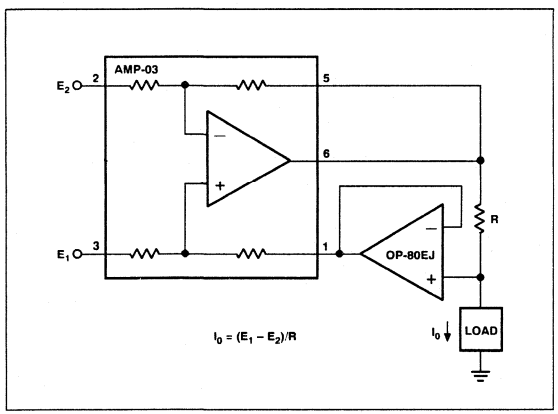


FIGURE 8: *Differential input voltage-to-current converter for low I_{OUT}. OP-80EJ maintains 250fA max. input current, allowing I_O to be less than 1pA.*

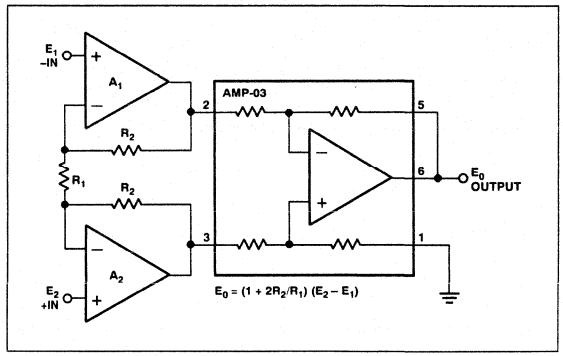


FIGURE 9: *Suitable instrumentation amplifier requirements can be addressed by using an input stage consisting of A_1, A_2, R_1 and R_2. The following matrix suggests a suitable amplifier.*

4

SYSTEM DESIGN REQUIREMENT	SUGGESTED OP AMP FOR A_1 AND A_2
Source impedance low, need low voltage noise performance	OP-27, OP-37 OP-227 (Dual Matched) OP-270 (Dual) OP-271 OP-470 OP-471
Source impedance high ($R_S \geq 15K\Omega$), need low current noise	OP-80 OP-41 OP-43 OP-249 OP-97
Require ultra-high input impedance	OP-80 OP-97 OP-41 OP-43
Need wider bandwidth and high speed	OP-42 OP-43 OP-249

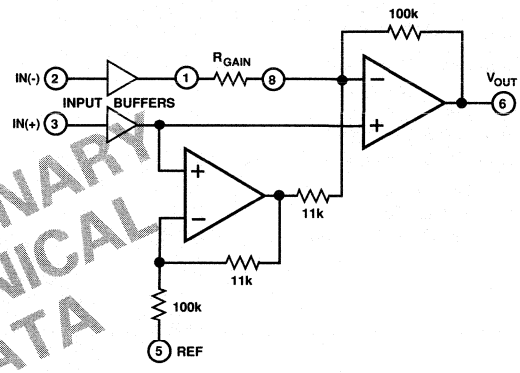
Low Power, 8-Pin, Single-Supply Instrumentation Amplifier

AMP-04*

FEATURES
- High Common-Mode Rejection: 105 dB min
- Low Supply Current: 800 μA max
- Wide Gain Range: 1 to 1000
- Low Offset Voltage: 200 μV max
- High Bandwidth: 300 kHz typ
- Excellent Gain Nonlinearity: 0.003% max
- Zero-In/Zero-Out
- Single-Resistor Gain Set
- Low Cost
- 8-Pin Mini-DIP and SOIC Packages

APPLICATIONS
- Strain Gages
- Thermocouples
- RTDs
- Battery-Powered Equipment
- Medical Instrumentation
- Data Acquisition Systems
- PC Based Instruments
- Portable Instrumentation

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

4

GENERAL DESCRIPTION

The AMP-04 is a low power instrumentation amplifier intended for single-supply applications. It offers an excellent combination of low power consumption, wide voltage range, and excellent gain performance in an 8-pin package. Gain between 1 and 1000 is set by an external resistor. Operating from +5 V to ±15 V supplies, the input and output common-mode voltage ranges allow the AMP-04 to handle signals with full accuracy from ground to within 1.5 volts of the positive supply. Gain Bandwidth is over 300 kHz. In addition to being easy to use, the AMP-04 draws only 800 μA (max) of supply current and is available in both plastic and ceramic 8-pin Mini-DIP and plastic SOIC (small outline) packages.

For high resolution data acquisition systems, laser trimming of low drift thin-film resistors limits the input offset voltage to under 200 μV, and allows the AMP-04 to offer gain nonlinearity of 0.003% and a gain tempco of less than 50 ppm/°C.

A proprietary input structure limits input bias currents to less than 20 nA with drift under 200 pA/°C, allowing direct connection of the AMP-04 to high impedance transducers and other signal sources.

The AMP-04 is specified over the extended industrial (−40°C to +85°C) temperature range. AMP-04s are available in plastic and ceramic DIP plus SOIC-8 surface mount packages. Contact your local sales office for MIL-STD-883 data sheet.

*Protected by Patent No. 5,075,633.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AMP-04—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_S = +5 V, V_{CM} = 2.5 V, −40°C ≤ T_A ≤ +85°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT OFFSET VOLTAGE						
Input Offset Voltage	V_{IOS}	"E" Grade		30	200	μV
Input Offset Voltage	V_{IOS}	"F" Grade		30	400	μV
Input Offset Voltage Drift	TCV_{IOS}			5		μV/°C
Output Offset Voltage	V_{OOS}			0.5	3.0	mV
Output Offset Voltage Drift	TCV_{OOS}			10		μV/°C
INPUT CURRENT						
Input Bias Current	I_B			15	25	nA
Input Bias Current Drift	TCI_B					pA/°C
Input Offset Current	I_{OS}			0.5	5	nA
Input Offset Current Drift	TCI_{OS}					pA/°C
INPUT						
Input Resistance	Z_{IN}					MΩ
Input Voltage Range	IVR		0		3.5	V
Common-Mode Rejection	CMR	G = 1	60	75		dB
		G = 10	80	100		dB
		G = 100	85	105		dB
		G = 1000		105		dB
Power Supply Rejection	PSRR	G = 1	80	100		dB
		G = 10	90	110		dB
		G = 100	100	115		dB
		G = 1000		115		dB
GAIN (G = 100 k/R_{GAIN})						
Gain Equation Accuracy		G = 1			0.5	%
		G = 10			0.5	%
		G = 100			0.5	%
		G = 1000		0.4		%
Gain Range	G		1		1000	V/V
Nonlinearity		G = 1 to 1000		0.012		%
Temperature Coefficient	TC_G					ppm/°C
OUTPUT						
Output Voltage Swing	V_{OUT}	R_L = 2 kΩ		4.2		V
Output Current Limit			−30		+10	mA
NOISE						
Noise Voltage Density, RTI	e_N	f_O = 1 kHz				
		G = 1				nV/√Hz
		G = 10				nV/√Hz
		G = 100				nV/√Hz
		G = 1000				nV/√Hz
Noise Current Density, RTI	i_N	f_O = 1 kHz				
		G = 1				pA/√Hz
		G = 10				pA/√Hz
		G = 100				pA/√Hz
		G = 1000				pA/√Hz
Input Noise Voltage	e_N p–p	0.1 Hz to 10 Hz				
		G = 1				μV
		G = 10				μV
		G = 100				μV
		G = 1000				μV
DYNAMIC RESPONSE						
Small Signal Bandwidth	BW	G = 1, −3 dB		300		kHz
Slew Rate				0.12		V/μs
POWER SUPPLY						
Supply Current	I_{SY}			550		μA

PRELIMINARY TECHNICAL DATA

Specifications subject to change without notice.

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ELECTRICAL CHARACTERISTICS (V_S = ±15 V, V_{CM} = 0 V, −40°C ≤ T_A ≤ +85°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
OFFSET VOLTAGE						
Input Offset Voltage	VI_{OS}			0.5	1	mV
Input Offset Voltage Drift	TCV_{IOS}			5		µV/°C
Output Offset Voltage	V_{OOS}				5.0	mV
Output Offset Voltage Drift	TCV_{OOS}			10		µV/°C
INPUT CURRENT						
Input Bias Current	I_B			15	25	nA
Input Bias Current Drift	TCI_B					pA/°C
Input Offset Current	I_{OS}			0.5	5	nA
Input Offset Current Drift	TC_{IOS}					pA/°C
INPUT						
Input Resistance	Z_{IN}					MΩ
Input Voltage Range	IVR		15		13.5	V
Common-Mode Rejection	CMR	G = 1	60	75		dB
		G = 10	80	95		dB
		G = 100	85	100		dB
		G = 1000	85	105		dB
Power Supply Rejection	PSRR	G = 1	75	90		dB
		G = 10	90	105		dB
		G = 100	90	110		dB
		G = 1000	90	110		dB
GAIN (G = 100 k/R_{GAIN})						
Gain Equation Accuracy		G = 1		0.2	0.5	%
		G = 10		0.2	0.5	%
		G = 100		0.2	0.5	%
		G = 1000		0.4		%
Gain Range	G		1		1000	V/V
Nonlinearity		G = 1 to 1000		0.012		%
Temperature Coefficient	TC_G					ppm/°C
OUTPUT						
Output Voltage Swing	V_{OUT}	R_L = 2 kΩ		−13.2/+14.6		V
Output Current Limit			−30		+10	mA
NOISE						
Noise Voltage Density, RTI	e_N	f_O = 1 kHz				
		G = 1		272		nV/√Hz
		G = 10		44		nV/√Hz
		G = 100		28		nV/√Hz
		G = 1000		10		nV/√Hz
Noise Current Density, RTI	i_N	f_O = 1 kHz				
		G = 1				pA/√Hz
		G = 10				pA/√Hz
		G = 100				pA/√Hz
		G = 1000				pA/√Hz
Input Noise Voltage	e_N p-p	0.1 to 10 Hz				
		G = 1				µV
		G = 10				µV
		G = 100				µV
		G = 1000				µV
DYNAMIC RESPONSE						
Small Signal Bandwidth	BW	G = 1, (−3 dB)		300		kHz
Slew Rate				0.12		V/µs
POWER SUPPLY						
Supply Current	I_{SY}			750		µA

PRELIMINARY TECHNICAL DATA

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WAFER TEST LIMITS (@ V_S = +5.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Limit	Units
OFFSET VOLTAGE				
Input Offset Voltage	V_{IOS}		200	μV
Output Offset Voltage	V_{OOS}		3.0	mV
INPUT CURRENT				
Input Bias Current	I_B		25	nA
Input Offset Current	I_{OS}		5	nA
OUTPUT				
Output Voltage Swing	V_{OUT}	R_L = 2 kΩ	+4	V
Output Current Limit			−30/+10	mA
POWER SUPPLY				
Supply Current	I_{SY}		550	μA

NOTE
Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

PRELIMINARY TECHNICAL DATA

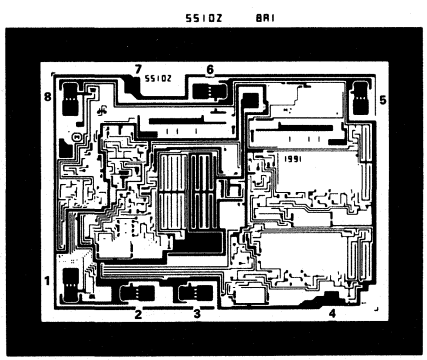
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Common-Mode Input Voltage[2] . . . . . ± 18 V
Differential Input Voltage . . . . . 36 V
Output Short-Circuit Duration to GND[2] . . . . . Indefinite
Storage Temperature Range
Z, RC Package . . . . . −65°C to +175°C
P, S Package . . . . . −65°C to +150°C
Operating Temperature Range
AMP-04A . . . . . −55°C to +125°C
AMP-04G . . . . . −40°C to +85°C
Junction Temperature Range
Z, RC Package . . . . . −65°C to +175°C
P, S Package . . . . . −65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C

Package Type	θ_{JA}[3]	θ_{JC}	Units
8-Pin Cerdip (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.
[3]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered in circuit board for SOIC package.

DICE CHARACTERISTICS



AMP-04 Die Size 0.075 in. × 0.99 in. (7,425 sq. mils)

ORDERING GUIDE

V_{OS} @ +5 V T_A = +25°C	Temperature Range	Cerdip 8-Pin*	Plastic 8-Pin*
500	MIL	AMP04AZ/883	
200	XIND		AMP04EP
400	XIND		AMP04FP
400	XIND		AMP04FS
200	+25°C		AMP04GBC

*For outline information see Package Information section.

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APPLICATIONS

Common-Mode Rejection

The purpose of the instrumentation amplifier is to amplify the difference between the two input signals, but to ignore the offset and noise voltage common to both, the common-mode voltage. One way of judging the device's ability to reject this offset is the common-mode gain, which is the ratio between a change in the common-mode voltage and the resulting output voltage change. Instrumentation amplifiers are often judged by the common-mode rejection ratio, which is equal to $20 \times \log_{10}$ of the ratio of the user-selected differential signal gain to the common-mode gain, commonly called the CMRR. The AMP-04 offers excellent CMRR with very low temperature drift through the use of proprietary laser-trimmed thin-film resistors and high gain amplifiers, see the CMRR Test Circuit.

Programming the Gain

The gain of the AMP-04 is programmed by the user by selecting an external resistor according to the following relationship: Gain $= 100\ k\Omega/R_{GAIN}$.

Grounding

The most common problems encountered in high performance analog instrumentation and data acquisition system design are found in the management of offset errors and ground noise. Primarily, the designer must consider temperature differentials and thermocouple effects due to dissimilar metals, IR voltage drops, and the effects of stray capacitance. The problem is greatly compounded when high speed digital circuitry, such as that accompanying data conversion components, is brought into the proximity of the analog section. Considerable noise and error contributions such as fast moving logic signals which easily propagate into sensitive analog lines, and the unavoidable noise common to digital supply lines must all be dealt with if the accuracy of the carefully designed analog section is to be preserved.

In addition to the temperature drift errors encountered in the amplifier, thermal errors due to the supporting discrete components should be evaluated. The use of high quality, low TC components where appropriate is encouraged. More importantly, large thermal gradients can create not only unexpected changes in component values, but also generate significant thermoelectric voltages due to the interface between dissimilar metals such as lead solder, copper wire, gold socket contacts, kovar lead frames, etc. Thermocouple voltages developed at these junctions commonly exceed the TC_{VOS} contribution of the AMP-04. Component layout which takes into account the power dissipation at critical locations in the circuit and minimizes gradient effects and differential common-mode voltages by taking advantage of input symmetry will minimize many of these errors.

High accuracy circuitry can experience considerable error contributions due to the coupling of stray voltages into sensitive areas, including high impedance amplifier inputs which benefit from such techniques as ground planes, guard rings, and shields.

Careful circuit layout, including good grounding and signal routing practice to minimize stray coupling and ground loops is recommended. Leakage currents can be minimized by using high quality socket and circuit board materials, and by carefully cleaning and coating complete board assemblies.

As mentioned above, the high speed transition noise found in logic circuitry is the sworn enemy of the analog circuit designer. Great care must be taken to maintain separation between them in order to minimize coupling. A major path for these error voltages will be found in the power supply lines. Although low impedance, load-related variations and noise levels which are completely acceptable in the high thresholds of the digital domain make the digital supply unusable in nearly all high performance analog applications. The user is encouraged to maintain separate power and ground between the analog and digital systems wherever possible, joining only at the supply itself if necessary, and to observe careful grounding layout and bypass capacitor scheduling in sensitive areas.

Input Shield Drivers

High impedance sources and long cable runs from remote transducers in noisy industrial environments commonly experience significant amounts of noise coupled to the inputs. Both stray capacitance errors and noise coupling from external sources can be minimized by running the input signal through shielded cable. The cable shield is often grounded at the analog input common, however improved dynamic noise rejection and a reduction in effective cable capacitance is achieved by driving the shield with a buffer amplifier at a potential equal to the voltage seen at the input. Driven shields are easily realized with the AMP-04. Examination of the simplified schematic shows that the potentials at the Gain Set Resistor pins of the AMP-04 follow the inputs precisely. Shield drivers are easily realized by buffering the potential at these pins by a dual high slew rate op amp such as the OP-249. Alternatively, applications with single-ended sources or those utilizing twisted-pair cable could drive a single shield with the OP-42. In order to minimize error contributions due to this additional circuitry, all components and wiring should remain in close proximity to the AMP-04 and careful grounding and bypassing techniques should be observed.

Compensating for Input and Output Errors

In order to achieve optimal performance, the user needs to take into account a number of error sources found in instrumentation amplifiers. These consist primarily of input and output offset voltages and leakage currents.

The input and output offset voltages are independent from one another, and must be considered separately. The input offset component will of course be directly multiplied by the gain of the amplifier, in contrast to the output offset voltage which is independent of gain. Therefore, the output error is the dominant factor at low gains, and the input error grows to become the greater problem as gain is increased. The overall equation

PRELIMINARY TECHNICAL DATA

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for offset voltage error referred to the output (RTO) is:

$$V_{OS}\ (RTO) = (V_{IOS} \times G) + V_{OOS}$$

where V_{IOS} is the input offset voltage and V_{OOS} the output offset voltage, and G is the programmed amplifier gain.

The change in these error voltages with temperature must also be taken into account. The specification TCV_{OS}, referred to the output, is a combination of the input and output drift specifications. Again, the gain influences the input error but not the output, and the equation is:

$$TCV_{OS}\ (RTO) = (TCV_{IOS} \times G) + TCV_{OOS}$$

In some applications the user may wish to define the error contribution as referred to the input, and treat it as an input error. The relationship is:

$$TCV_{OS}\ (RTI) = TCV_{IOS} + (TCV_{OOS}/G)$$

The bias and offset currents of the input transistors also have an impact on the overall accuracy of the input signal. The input leakage, or bias currents of both inputs will generate an additional offset voltage when flowing through the signal source resistance. Changes in this error component due to variations with signal voltage and temperature can be minimized if both input source resistances are equal, reducing the error to a common-mode voltage which can be rejected. The difference in bias current between the inputs, the offset current, generates a differential error voltage across the source resistance which should be taken into account in the user's design.

In applications utilizing floating sources such as thermocouples, transformers, and some photodetectors, the user must take care to provide some current path between the high impedance inputs and analog ground. The input bias currents of the AMP-04, although extremely low, will charge the stray capacitance found in nearby circuit traces, cables, etc., and cause the input to drift erratically or to saturate unless given a bleed path to the analog common. Again, the use of equal resistance values will create a common input error voltage which is rejected by the amplifier.

PRELIMINARY TECHNICAL DATA

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ANALOG DEVICES

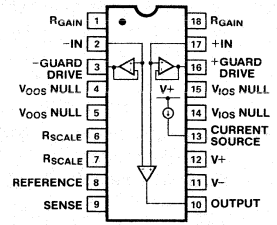
Fast Settling JFET Instrumentation Amplifier

AMP-05

FEATURES

- Settling-Time to 12-Bit Accuracy, G ≤ 2000 ..... 15μs Max
- Overload Recovery Time, G = 1000 ..... 15μs
- 14-Bit Gain Linearity at G ≤ 1000
- On-Board Dual Guard Drivers
- On-Board 100μA Precision Current Source
- Low Bias Current ..... 50pA Max @ 25°C
  ..... 20nA Max @ 125°C
- Temperature Stable CMR
  ..... 105dB Min Over −55°C to +125°C
- High Slew-Rate with 500pF Load ..... 5V/μs Min
- Input Overload Protected to ±30V Differential
- Available in Die Form

PIN CONNECTIONS



18-PIN HERMETIC DIP
(X-Suffix)

4

ORDERING INFORMATION†

CERDIP 18-PIN PACKAGE	OPERATING TEMPERATURE RANGE
AMP05AX*	MIL
AMP05BX*	MIL
AMP05EX	IND
AMP05FX	IND

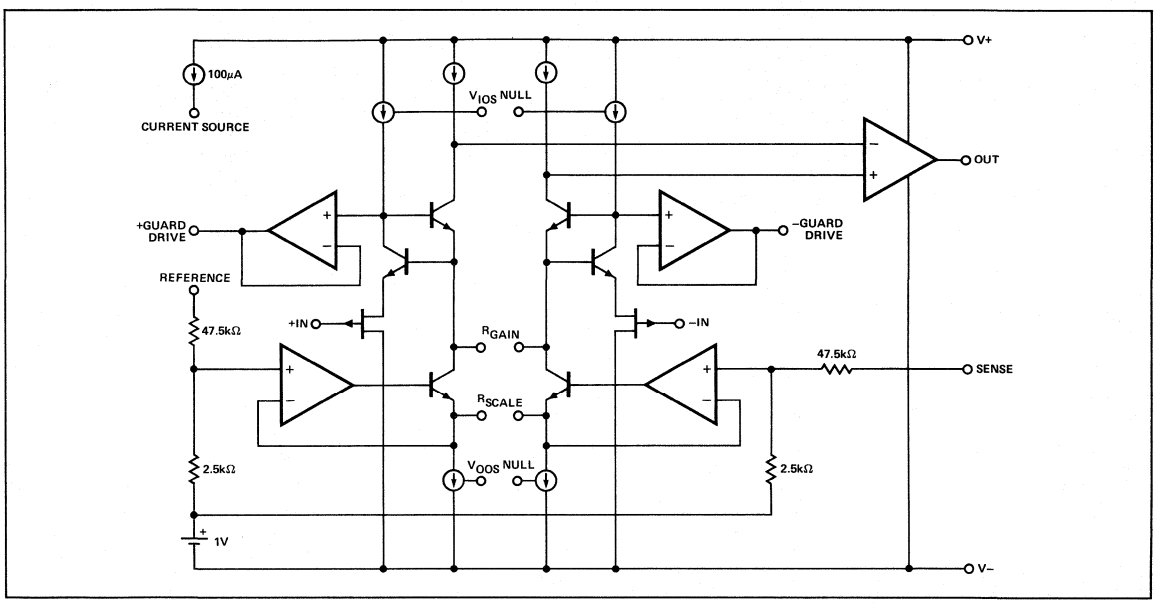
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

The AMP-05 is a fast JFET instrumentation amplifier designed for high-speed analog signal-processing and analog-multiplexed data acquisition systems. Settling-time to 12-bits is 15μs maximum, with better than 14-bit linearity at all gains up to 1000. Two functions are added to the instrumentation amplifier that reduce external component count in many applications. On-board dual guard drivers maintain good settling-time and common-mode rejection performance when shielded cable connects the input signal to the AMP-05. A precision 100μA current source is also provided for transducer excitation, powering a low-current voltage reference, and other functions.

SIMPLIFIED SCHEMATIC



AMP-05

The AMP-05 employs a current-feedback technique which provides a high and stable common-mode rejection, 105dB minimum over the military temperature range. JFET inputs reduce bias current to 50pA maximum at 25°C and only 20nA maximum at 125°C; low bias current reduces errors due to signal-source resistance. Internal input protection allows a 30V differential overload at all gain settings. The AMP-05 recovers rapidly when an input overload is removed. Recovery time is typically 15μs following a 1000:1 overload, voltage gain set to 1000. AMP-05 voltage gain is set by the ratio of two external resistors over the range 0.1 to 2000 and a low gain temperature-coefficient of 20ppm/°C maximum is achievable in the range 1 to 1000.

The AMP-05's outputs can all drive large capacitive loads without oscillation. The amplifier output is guaranteed stable with loads up to 2,000pF and the guard drivers can tolerate up to 10,000pF without oscillation.

Sense and reference pins complete the output feedback-loop and provide an output ground reference, respectively. The reference pin may be used for zeroing system offsets, where auto-zero hardware is employed. Resistance in series with the reference terminal does not degrade common-mode rejection on PMI's AMP-05, which is a significant problem with instrumentation amplifiers employing the three op-amp configuration.

For applications requiring very low input offset voltage and low offset drift, or higher output drive capability, refer to the AMP-01 data sheet.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Common-Mode Input Voltage ..... Supply Voltage
Differential Input Voltage ..... ±30V
(Inputs must not exceed supply voltages.)
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range ..... –65°C to +150°C
Operating Temperature Range
AMP-05A, B ..... –55°C to +125°C
AMP-05E, F ..... –25°C to +85°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
Junction Temperature (T_J) ..... –65°C to +150°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
18-Pin Hermetic DIP (X)	74	7	°C/W

NOTES:
1. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $R_S = 5k\Omega$, $R_L = 2k\Omega$, $T_A = 25°C$, unless otherwise noted.

			AMP-05A/E			AMP-05B/F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
GAIN									
Gain Range	G_R		0.1	—	2000	0.1	—	2000	
Gain Equation Accuracy		$G = 20 \times R_S/R_G$ $G = 1$ to 1000	—	0.25	0.5	—	0.4	1.0	%
Gain Nonlinearity	G_{NL}	$G = 1$	—	0.001	—	—	0.001	—	%
		$G = 10$	—	0.002	—	—	0.002	—	
		$G = 100$	—	0.007	—	—	0.007	—	
		$G = 1000$	—	0.020	—	—	0.020	—	
		$R_L = 10k\Omega$							
		$G = 100$	—	0.004	—	—	0.004	—	%
		$G = 1000$	—	0.004	—	—	0.004	—	
Gain Temperature Coefficient	G_{TC}	$G = 1$ to 100	—	1.7	10	—	1.7	10	ppm/°C
		$G = 1000$	—	8	20	—	8	20	
		(Notes 1, 2)							
OUTPUT RATING									
Output Voltage Swing	V_{OUT}	$R_L = 1k\Omega$	±11	±12	—	±11	±12	—	V
		Over Temperature	±10.5	±12	—	±10.5	±12	—	
Short Circuit Current	I_{SC}	Output Shorted to Ground	±20	±35	—	±20	±35	—	mA
Capacitive Load Stability		Full Gain Range No Oscillations	2	10	—	2	10	—	nF

NOTES:
1. Gain tempco does not include the effects of gain and scale resistor tempco match.
2. Guaranteed but not 100% production tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $R_S = 5k\Omega$, $R_L = 2k\Omega$, $T_A = 25°C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	AMP-05A/E MIN	AMP-05A/E TYP	AMP-05A/E MAX	AMP-05B/F MIN	AMP-05B/F TYP	AMP-05B/F MAX	UNITS
INPUT									
Input Bias Current	I_B	$T_A \leq 25°C$	—	20	50	—	30	100	pA
		$T_A = 85°C$ (E/F Grades)	—	0.5	4	—	1	8	nA
		$T_A = 125°C$ (A/B Grades)	—	7	20	—	12	30	nA
Input Offset Current	I_{OS}	$T_A \leq 25°C$	—	5	25	—	10	50	pA
		$T_A = 85°C$ (E/F Grades)	—	0.05	0.5	—	0.1	1	nA
		$T_A = 125°C$ (A/B Grades)	—	1	5	—	2	10	nA
Input Resistance	R_{IN}		—	10^{12}	—	—	10^{12}	—	Ω
Input Capacitance	C_{IN}		—	8	—	—	8	—	pF
Input Voltage Range	IVR	$T_A = 25°C$	±11	±11.5	—	±11	±11.5	—	V
		Over Temperature	±10	±11	—	±10	±11	—	
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$							
		G = 1000	110	115	—	100	110	—	dB
		G = 100	105	115	—	95	110	—	
		G = 10	100	110	—	90	100	—	
		G = 1	90	98	—	80	90	—	
		$V_{CM} = \pm 10V$, Over Temperature							
		G = 1000	105	110	—	95	105	—	dB
		G = 100	100	110	—	90	105	—	
		G = 10	95	105	—	85	95	—	
		G = 1	85	95	—	75	85	—	
OFFSET VOLTAGE									
Input Offset Voltage	V_{IOS}	$V_{CM} = 0V$							
		$T_A = 25°C$	—	0.3	1.0	—	0.5	2.0	mV
		Over Temperature	—	0.8	2.0	—	1.0	4.0	
Input Offset Voltage Drift	TCV_{IOS}		—	5	10	—	7	20	µV/°C
Output Offset Voltage	V_{OOS}	$T_A = 25°C$	—	3	15	—	5	25	mV
		Over Temperature	—	9	25	—	11	40	
Output Offset Voltage Drift	TCV_{OOS}		—	50	100	—	70	150	µV/°C
Offset Referred to Input vs. Positive Supply V+ = +5V to +15V	+PSR	G = 1000	115	120	—	110	115	—	dB
		G = 100	110	118	—	105	110	—	
		G = 10	95	105	—	90	100	—	
		G = 1	75	85	—	70	80	—	
		Over Temperature							
		G = 1000	110	116	—	105	110	—	dB
		G = 100	105	114	—	100	105	—	
		G = 10	90	102	—	85	98	—	
		G = 1	75	84	—	70	80	—	
Offset Referred to Input vs. Negative Supply V− = −5V to −15V	−PSR	G = 1000	110	118	—	105	110	—	dB
		G = 100	95	104	—	90	98	—	
		G = 10	75	84	—	70	80	—	
		G = 1	55	64	—	50	60	—	
		Over Temperature							
		G = 1000	105	113	—	100	105	—	dB
		G = 100	95	104	—	90	95	—	
		G = 10	75	84	—	70	80	—	
		G = 1	55	64	—	50	60	—	

AMP-05

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $R_S = 5k\Omega$, $R_L = 2k\Omega$, $T_A = 25°C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	AMP-05A/E MIN	AMP-05A/E TYP	AMP-05A/E MAX	AMP-05B/F MIN	AMP-05B/F TYP	AMP-05B/F MAX	UNITS
Input Offset Voltage Trim Range		$V_S = \pm 4.5V$ to $\pm 18V$	±2.5	±5	—	±2.5	±5	—	mV
Output Offset Voltage Trim Range		$V_S = \pm 4.5V$ to $\pm 18V$	±25	±40	—	±25	±40	—	mV
SENSE INPUT									
Input Resistance	R_{IN}		40	50	60	40	50	60	kΩ
Input Current	I_{IN}	Referenced to V–	—	280	—	—	280	—	μA
REFERENCE INPUT									
Input Resistance	R_{IN}		40	50	60	40	50	60	kΩ
Input Current	I_{IN}	Referenced to V–	—	280	—	—	280	—	μA
Voltage Range			−10.5	—	+20	−10.5	—	+20	V
Gain to Output			—	1	—	—	1	—	V/V
NOISE									
Voltage Density RTI	e_n	$f_O = 1kHz$ $G \geq 100$ $G = 10$ $G = 1$	— — —	16 38 350	— — —	— — —	16 38 350	— — —	$nV/\sqrt{Hz}$
Noise Current Density	i_n	$f_O = 1kHz$	—	10	—	—	10	—	$fA/\sqrt{Hz}$
Input Noise Voltage	e_{np-p}	Measured at G = 1000, 0.1Hz to 10Hz Bandwidth	—	4	—	—	4	—	μV_{p-p}
Output Noise Voltage	e_{np-p}	Measured at G = 0, 0.1Hz to 10Hz Bandwidth	—	7	—	—	7	—	μV_{p-p}
Input Noise Current	i_{np-p}	0.1Hz to 10Hz Bandwidth	—	0.12	—	—	0.12	—	pA_{p-p}
DYNAMIC RESPONSE									
Small Signal Bandwidth (−3dB)	BW	$G = 1$ $G \geq 10$	— —	3 120	— —	— —	3 120	— —	MHz kHz
Slew Rate	SR	$C_L = 500pF$ $G \geq 10$ Over Temperature	5 3.5	7.5 5.5	— —	5 3.5	7.5 5.5	— —	V/μs
Settling Time	t_S	$1 \leq G \leq 2000$ −10V to +10V Step (Note 1) to 0.1% to 0.05% to 0.025%	 — — —	 5 7 10	 7 10 15	 — — —	 5 7 10	 7 10 15	μs
Overload Recovery Time	t_{rec}	$G = 1000$ $V_{IN} = 10V$ to 10mV	—	15	—	—	15	—	μs

NOTE:
1. Guaranteed but not 100% production tested.

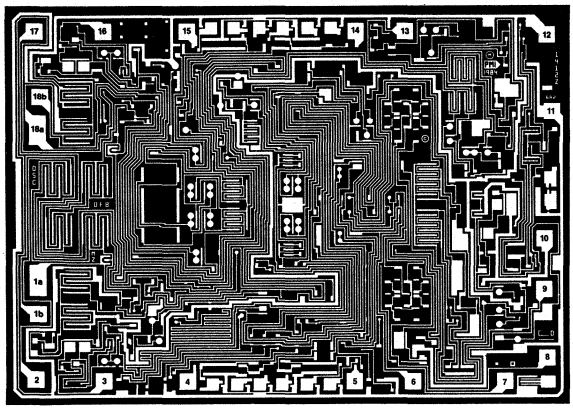
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $R_S = 5k\Omega$, $R_L = 2k\Omega$, $T_A = 25°C$, unless otherwise noted. (Continued)

			AMP-05A/E			AMP-05B/F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
GUARD DRIVERS									
Output Voltage	V_O	Volts above respective input over temperature.	0.5	1.2	2.0	0.5	1.2	2.0	V
Peak Output Current			8	15	—	8	15	—	mA
Slew Rate	SR	C_L = 1000pF	—	16	—	—	16	—	V/μs
Capacitive Load Stability		No Oscillations (Note 1)	10	100	—	10	100	—	nF
CURRENT SOURCE									
Current Output	I_{OUT}	Over Full Compliance Range	90	100	120	90	100	120	μA
Output Compliance Range		V_{OC} Volts Below V+ (Irrespective of V−)	4	—	30	4	—	30	V
Output Impedance	R_{OUT}	Over Full Compliance Range (Note 1)	1	3	—	1	3	—	GΩ
Temperature Coefficient			—	100	—	—	100	—	ppm/°C
Power Supply Rejection			—	150	—	—	150	—	nA/V
POWER SUPPLY $-25°C \le T_A \le +85°C$ for E/F Grades, $-55°C \le T_A \le +125°C$ for A/B Grades									
Supply Voltage Range	V_S		±4.5	—	±18	±4.5	—	±18	V
Quiescent Current	I_Q		—	7.0	9.0	—	7.5	10.0	mA

NOTE:
1. Guaranteed but not 100% production tested.

AMP-05

DICE CHARACTERISTICS



DIE SIZE 0.127 × 0.176 inch, 22,352 sq. mils
(3.23 × 4.47mm, 14.42 sq. mm)

1a. R_{GAIN} SENSE
1b. R_{GAIN} FORCE
2. −INPUT
3. −GUARD DRIVE
4. V_{OOS} NULL
5. V_{OOS} NULL
6. R_{SCALE}
7. R_{SCALE}
8. REFERENCE
9. SENSE
10. OUTPUT
11. V−
12. V+
13. CURRENT SOURCE
14. V_{IOS} NULL
15. V_{IOS} NULL
16. +GUARD DRIVE
17. +INPUT
18a. R_{GAIN} SENSE
18b. R_{GAIN} FORCE

WAFER TEST LIMITS at $V_S = \pm 15V$, $R_S = 5k\Omega$, $R_L = 2k\Omega$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	AMP-05GBC LIMIT	UNITS
Input Offset Voltage	V_{IOS}	$V_{CM} = 0$	2.0	mV MAX
Output Offset Voltage	V_{OOS}		25	mV MAX
Offset Referred to Input vs. Positive Supply	PSR	V+ = +5V to +15V G = 1000 G = 100 G = 10 G = 1	 110 105 90 70	dB MIN
Offset Referred to Input vs. Negative Supply	PSR	V− = −5V to −15V G = 1000 G = 100 G = 10 G = 1	 105 90 70 50	dB MIN
Input Bias Current	I_B		100	pA MAX
Input Offset Current	I_{OS}		50	pA MAX
Input Voltage Range	IVR	Guaranteed by CMR Tests	±11	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$ G = 1000 G = 100 G = 10 G = 1	 100 95 90 80	dB MIN
Gain Equation Accuracy		$G = 20 \times R_S/R_G$ G = 1 to 100	1.0	% MAX
Output Voltage Swing	V_{OUT}	$R_L = 1k\Omega$	±11	V MIN
Output-Current Limit		Output-to-Ground Short	±20	mA MIN
Current Source	I_{OUT}		90 120	μA MIN μA MAX
Quiescent Current	I_Q		±10.0	mA MAX

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

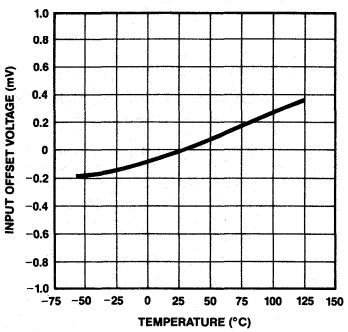
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $R_S = 5k\Omega$, $R_L = 2k\Omega$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	AMP-05GBC TYPICAL	UNITS
Input Offset Voltage Drift	TCV_{IOS}		7	$\mu V/°C$
Output Offset Voltage Drift	TCV_{OOS}	$R_G = \infty$	70	$\mu V/°C$
Nonlinearity		G = 1000 $R_L = 10k\Omega$	0.004	%
Voltage Noise Density	e_n	G = 1000 $f_O = 1kHz$	16	$nV/\sqrt{Hz}$
Current Noise Density	i_n	G = 1000 $f_O = 1kHz$	10	$fA/\sqrt{Hz}$
Voltage Noise	e_{np-p}	G = 1000 0.1Hz to 10Hz	4	μV_{p-p}
Current Noise	i_{np-p}	G = 1000 0.1Hz to 10Hz	0.12	pA_{p-p}
Small-Signal Bandwidth (−3dB)	BW	G = 1000	120	kHz
Slew Rate	SR	G = 10	7.5	$V/\mu s$
Settling Time	t_S	To 0.025% −10V to +10V Step $1 \le G \le 2000$	10	μs
Overload Recovery Time	t_{rec}	G = 1000 V_{IN} = 10V to 10mV	15	μs

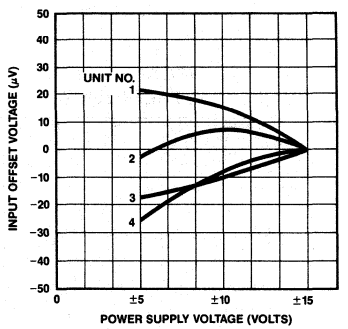
4

TYPICAL PERFORMANCE CHARACTERISTICS

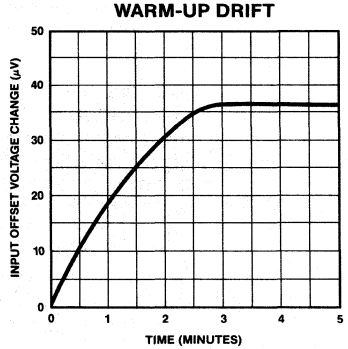
INPUT OFFSET VOLTAGE vs TEMPERATURE



INPUT OFFSET VOLTAGE vs SUPPLY VOLTAGE

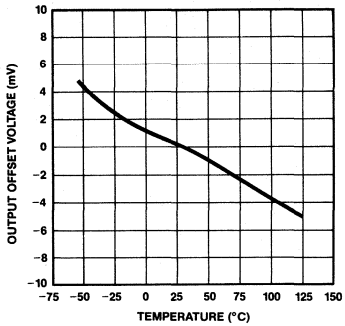


INPUT OFFSET VOLTAGE WARM-UP DRIFT

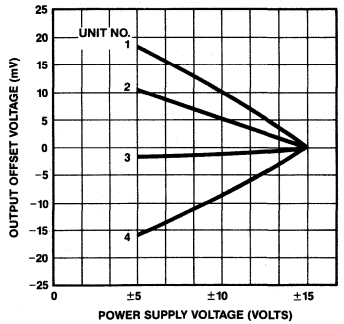


TYPICAL PERFORMANCE CHARACTERISTICS

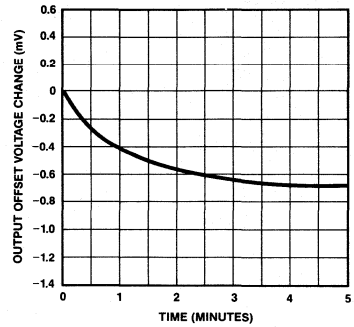
OUTPUT OFFSET VOLTAGE vs TEMPERATURE



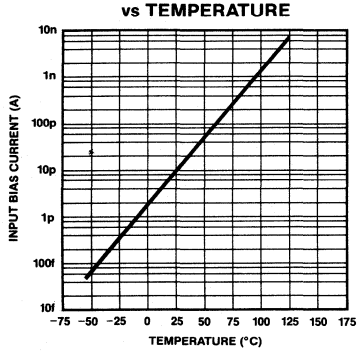
OUTPUT OFFSET VOLTAGE vs SUPPLY VOLTAGE



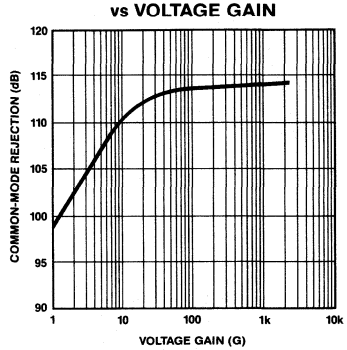
OUTPUT OFFSET VOLTAGE WARM-UP DRIFT



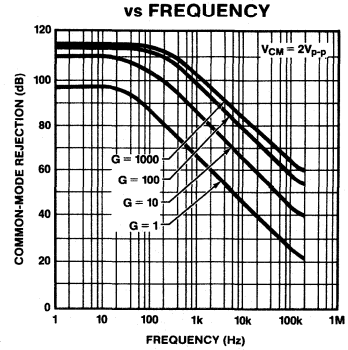
INPUT BIAS CURRENT vs TEMPERATURE



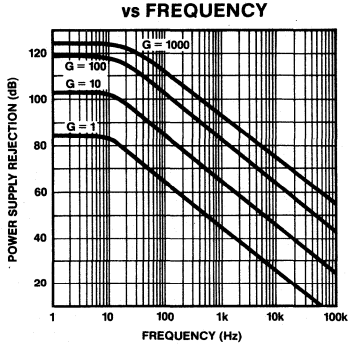
COMMON-MODE REJECTION vs VOLTAGE GAIN



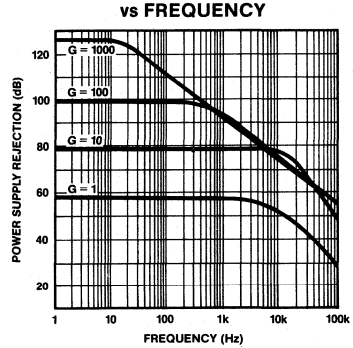
COMMON-MODE REJECTION vs FREQUENCY



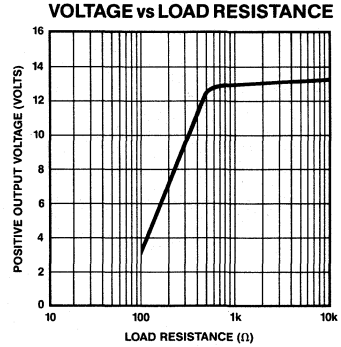
POSITIVE PSR vs FREQUENCY



NEGATIVE PSR vs FREQUENCY

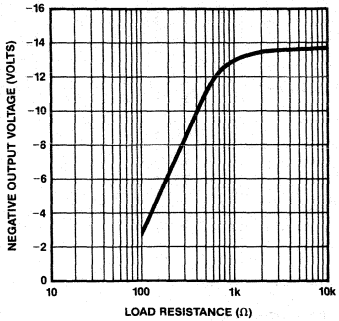


MAXIMUM POSITIVE OUTPUT VOLTAGE vs LOAD RESISTANCE

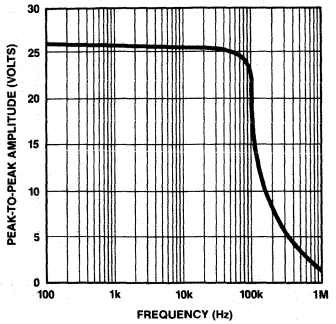


TYPICAL PERFORMANCE CHARACTERISTICS

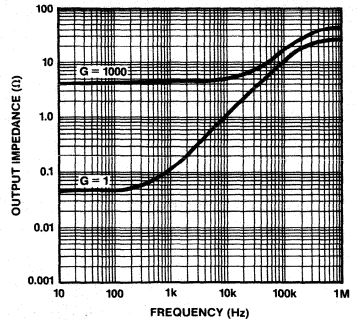
MAXIMUM NEGATIVE OUTPUT VOLTAGE vs LOAD RESISTANCE



MAXIMUM OUTPUT SWING vs FREQUENCY

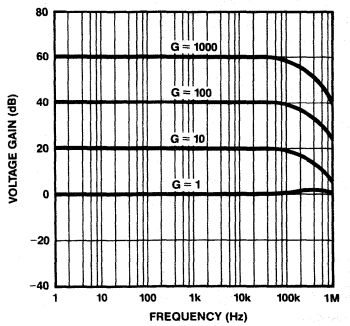


CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

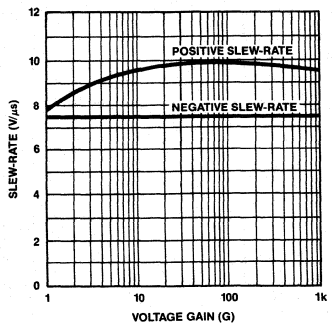


4

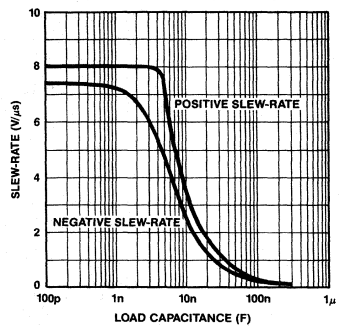
VOLTAGE GAIN vs FREQUENCY



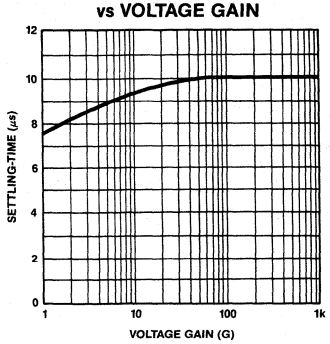
OUTPUT SLEW-RATE vs VOLTAGE GAIN



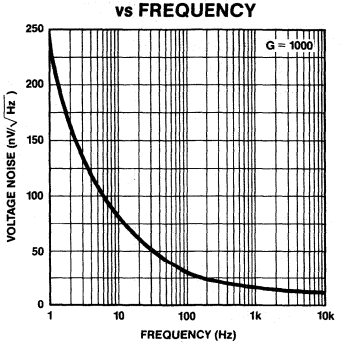
OUTPUT SLEW-RATE vs LOAD CAPACITANCE



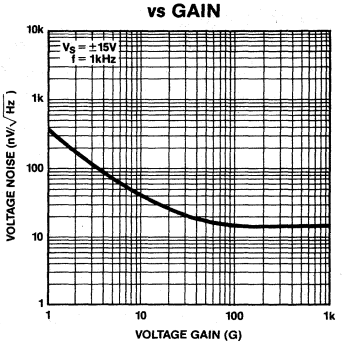
SETTLING-TIME TO 0.025% vs VOLTAGE GAIN



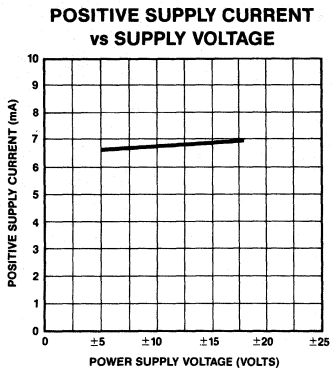
VOLTAGE NOISE DENSITY vs FREQUENCY

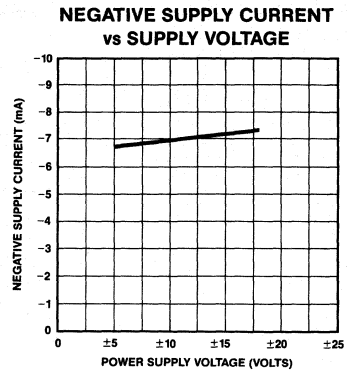


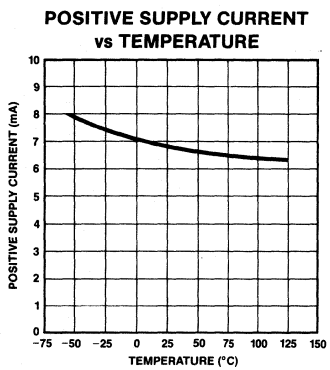
VOLTAGE NOISE DENSITY vs GAIN

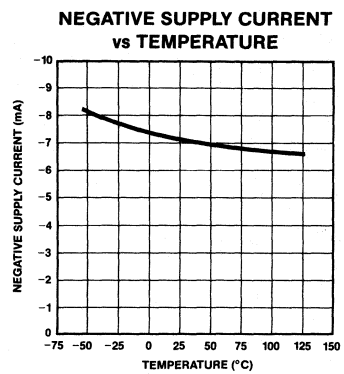


TYPICAL PERFORMANCE CHARACTERISTICS









APPLICATIONS INFORMATION

VOLTAGE GAIN

The AMP-05 uses two external resistors for setting voltage gain over the range 0.1 to 2000. The magnitudes of the scale resistor, R_S, and gain-set resistor, R_G, are related by the formula: $G = 20 \times R_S/R_G$, where G is the selected voltage gain. Figure 1 shows the amplifier connections. R_G can be selected using the graph in Figure 2.

Circuit performance is characterized using $R_S = 5k\Omega$ operating on ±15 volt supplies and driving a ±10 volt output.

Metal-film or wirewound resistors are recommended for R_S and R_G. The absolute resistance values and temperature coefficients of resistance are not too important; only the ratiometric parameters are important for gain accuracy and stability.

FIGURE 1: Basic AMP-05 Connections For Gains 0.1 to 2000

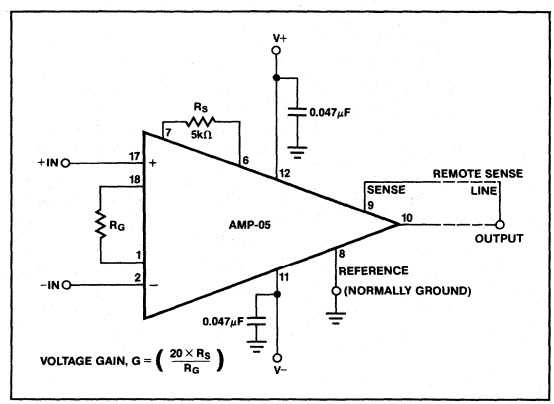
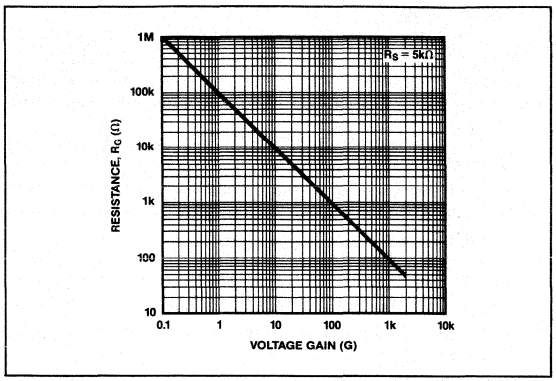


FIGURE 2: Selection of R_{GAIN}



AC amplifiers require good gain stability with temperature and time, but DC performance is unimportant. Therefore, low cost metal-film types with TCs of 50ppm/°C are usually adequate for R_S and R_G. Realizing the full potential of the AMP-05's gain stability requires precision metal-film or wirewound resistors. Achieving a 25ppm/°C max. gain tempco at all gains will require R_S and R_G temperature coefficient matching to 5ppm/°C max.

Gain accuracy is determined by the ratio accuracy of R_S and R_G combined with the gain equation error of the AMP-05 (0.5% for A/E grades).

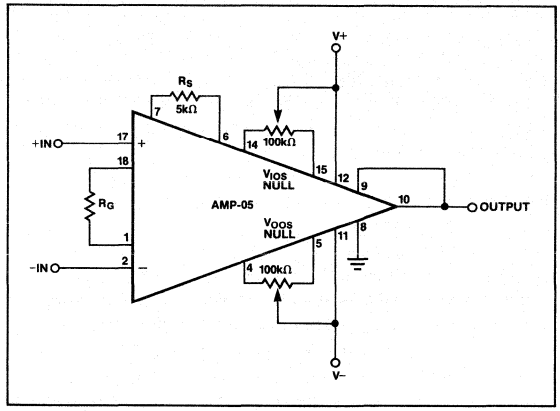
Note: The AMP-05 is inherently stable at all gains. However, like all amplifiers with a high gain-bandwidth product, instability can occur if layout precautions are not observed: (a) the amplifier should be decoupled close to the supply pins, and (b) the output must be kept well away from the inputs, the null pins, and R_{GAIN}.

The AMP-05 is capable of gain-bandwidth products in the hundreds of megahertz when operated at its highest gain settings. Under these conditions, even a few picofarads of stray feedback to the inputs can cause instability, and the situation is exacerbated if the input signal has a high source impedance. If instability does occur, the problem is easily eliminated by placing a small capacitor directly between the AMP-05's input pins, 2 and 17.

INPUT AND OUTPUT OFFSET VOLTAGES

Instrumentation amplifiers have independent offset voltages associated with the input and output stages. While the initial offsets may be adjusted to zero, temperature variations will cause shifts in offsets. Systems with auto-zero can correct for offset errors, so initial adjustment would be unnecessary. However, many high-gain applications do not have auto-zero. For these applications both offsets can be nulled. Nulling has minimal effect on TCV_{IOS} and TCV_{OOS} (refer to Figure 3 for connections).

FIGURE 3: Input and Output Offset Voltage Nulling



The input offset component is directly multiplied by the amplifier gain, whereas output offset is independent of gain. Therefore, at low gain, output offset errors dominate, while at high gain, input offset errors dominate. Overall offset voltage, V_{OS}, referred to the output (RTO) is calculated as follows:

$$V_{OS}\,(RTO) = (V_{IOS} \times G) + V_{OOS} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

where V_{IOS} and V_{OOS} are the input and the output offset voltage specifications and G is the amplifier gain. Input offset nulling alone can be used for fixed gains above 50. Otherwise, both nulls are required. When nulling both initial offsets, the input offset is nulled first by short-circuiting R_G, then the output offset is nulled with the short removed.

The overall offset voltage drift, TCV_{OS}, referred to the output, is a combination of input and output drift specifications. Input offset voltage drift is multiplied by the amplifier gain, G, and summed with the output offset drift;

$$TCV_{OS}\,(RTO) = (TCV_{IOS} \times G) + TCV_{OOS} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

where TCV_{IOS} is the input offset voltage drift, and TCV_{OOS} is the output offset voltage drift specification. Frequently, the amplifier drift is referred back to the input (RTI) which is then equivalent to an input signal change;

$$TCV_{OS}\,(RTI) = TCV_{IOS} + \frac{TCV_{OOS}}{G} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3)$$

For example, the maximum input-referred drift of an AMP-05EX set to G = 100 becomes:

$$TCV_{OS}\,(RTI) = 10\mu V/°C + \frac{100\mu V/°C}{100} = 11\mu V/°C \text{ max.}$$

INPUT BIAS AND OFFSET CURRENTS

Input bias currents are additional error sources which can degrade the input signal. Bias currents flowing through the signal source resistance appear as an additional offset voltage. Equal source resistance on both inputs of an instrumentation amplifier will minimize offset changes due to bias current variations with signal voltage and temperature. However, the difference between the two bias currents, the input offset current, produces a nontrimmable error. The magnitude of the error is the offset current times the source resistance.

The AMP-05 has FET inputs which have negligible bias and offset currents at room temperature and consequently can accurately measure signals from high source impedances. However, like all FET devices, the bias current doubles approximately every 10°C increase in junction temperature and therefore bias and offset currents must be carefully considered when operating up to +125°C.

Note: If very high source impedances (~1MΩ) are used and the AMP-05 is used at high gain, then it is recommended that a small capacitor is connected across the inputs to prevent instability.

A current path must always be provided between the differential inputs and analog ground to ensure correct amplifier operation. Floating inputs, such as thermocouples, should be grounded close to the signal source for best common-mode rejection.

OVERVOLTAGE PROTECTION

The AMP-05 features a unique internal protection circuit which permits differential input voltages of up to ±30V even when set for high gain operation. It should be noted however, that the output state during such an overload is not defined. Typically, at gains above 10, severe overloads (≃1000% overrange) will cause the output to sit at about +10V with a low-level oscillation apparent.

Additionally, gross overdriving will cause input currents of up to 100μA to flow in the lower of the two inputs. The increased input current should be borne in mind if interfacing to extremely delicate transducers.

OVERLOAD RECOVERY TIME

Following an input overload, an amplifier takes a finite time to recover, i.e. the amplifier's output has to return to the linear operating region after limiting at one or other supply. The AMP-05 is designed to recover rapidly from input overloads; typically recovery time is 15μs following a 1000:1 overload; voltage gain set to 1000.

Rapid overload recovery is particularly important in a multiplexed data acquisition system using programmable gain. In this application, it is possible for the input to be switched to a high-level signal with gain set high, thus overloading the amplifier. To maintain system speed, it is vital for the amplifier to recover quickly once the overload is removed by reprogramming the gain.

COMMON-MODE REJECTION

Ideally, an instrumentation amplifier responds only to the difference between the two input signals and rejects common-mode voltages and noise. In practice, there is a small change in output voltage when both inputs experience the same common-mode voltage change; the ratio of these voltages is called the common-mode gain. Common-mode rejection (CMR) is the logarithm of the ratio of differential-mode gain to common-mode gain, expressed in dB. CMR specifications are normally measured with a full-range input voltage change and a specified source resistance unbalance.

The current-feedback design used in the AMP-05 inherently yields high common-mode rejection. Unlike resistive feedback designs typified by the three-op-amp IA, the CMR is not degraded by small resistances in series with the reference input. A slight, but trimmable, output offset voltage change results from resistance in series with the reference input.

The common-mode input voltage range, CMVR, for linear operation may be calculated from the formula:

$$CMVR = \pm \left(IVR - \frac{|V_{OUT}|}{2G} \right) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4)$$

IVR is the data sheet specification for input voltage range; V_{OUT} is the maximum output signal; and G is the chosen voltage gain. For example, at 25°C, IVR is specified as ±11 volts minimum with ±15 volt supplies. Using a ±10 volt maximum swing output and substituting the figures in (4) simplifies the formula to:

$$CMVR = \pm \left(11 - \frac{5}{G} \right) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (5)$$

For all gains greater than or equal to 5, CMVR is ±10 volt minimum; at gains below 5, CMVR is reduced.

GUARD DRIVERS

Dual guard drivers are included to restore bandwidth, settling-time, and high frequency common-mode rejection (CMR) when shielded cable is used at the input. The guard drivers can handle large capacitive loads and transient currents, but they are not intended for large DC loads. The DC path to ground should be 30kΩ or greater; lower values can upset the AMP-05's internal biasing circuits.

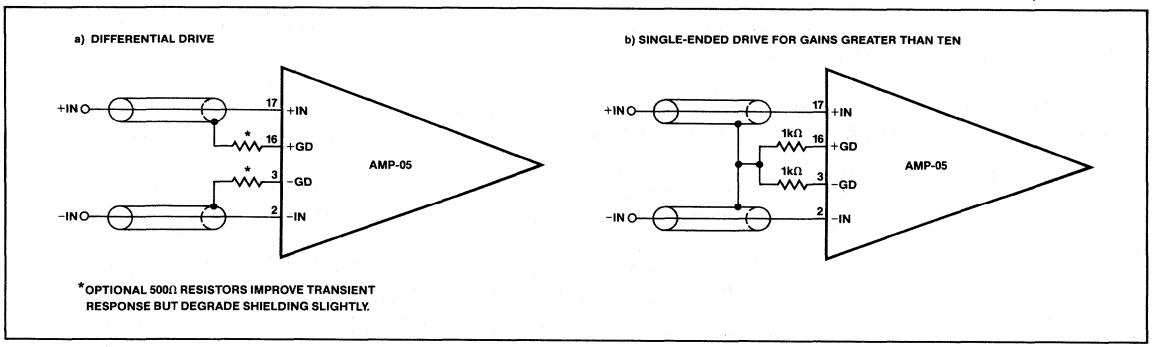
Shielded cable is often employed to minimize capacitively coupled noise pickup along the signal path from source to amplifier. When coaxial cable connects a transducer to the amplifier's input, the cable's capacitance interacts with the transducer's source impedance to form a low-pass filter. This filter function reduces the amplifier's bandwidth and degrades settling-time and CMR. The AMP-05's differential guard drivers act as an AC "bootstrap" when attached to the coaxial shields. In bootstrapping, each driver follows its corresponding input, and the driver output signals are buffered to handle large capacitive loads. Each driver will typically slew at 16V/μs with a 1000pF load. Bootstrapping reduces the effective input capacitance, since no AC voltage appears between the shield and inner conductor.

The AMP-05's guard drivers can form either a differential or single-ended drive (refer to Figures 4(a) and (b)). In the single-ended arrangement, the two input cable shields are held at the same potential, the common-mode voltage (Figure 4(b)). As such, the connection is also appropriate for one shielded twisted-pair cable. The single-ended arrangement maintains a high CMR even at high frequencies, but does not reduce high frequency gain degradation as it does not counteract differential-mode capacitance. Single-ended drive is acceptable for gains greater than ten using the circuit in Figure 4(b). However the differential connection, Figure 4(a), offers better overall performance because it effectively reduces both differential and common-mode capacitance. Reduction in these capacitances improves high-frequency CMR, settling-time, and gain.

It should be noted that all shield drive arrangements are potentially positive feedback configurations and under some conditions high frequency ringing may occur. If this proves troublesome, small resistors (500Ω-1kΩ) in series with the cable shield outputs will improve transient response and settling-time but reduce the effectiveness of the cable shield, particularly at high frequency.

Short circuits from the cable drives to ground will not damage the AMP-05 but will result in malfunction of the AMP-05 until the short is removed. The package pins adjacent to the two inputs, R_G connections and guard drives, sit within 2 volts of the input signals. This feature reduces leakage currents to the input terminals and eliminates the need for guard-rings which are necessary on many FET input amplifiers.

FIGURE 4: Applying the Guard Drivers to shield the inputs, guard driving reduces the effective input capacitance and improves CMR.



GROUNDING

The majority of instruments and data acquisition systems have separate grounds for analog and digital signals. Analog ground may also be divided into two or more grounds which will be tied together at one point, usually the analog power-supply ground. In addition, the digital and analog grounds may be joined, normally at the analog ground pin on the A-to-D converter. Following this basic grounding practice is essential for good circuit performance (Figure 5).

Mixing grounds causes interactions between digital circuits and the analog signals. Since the ground returns have finite resistance and inductance, hundreds of millivolts can be developed between the system ground and the data acquisition components. Using separate ground returns minimizes the current flow in the sensitive analog return path to the system ground point. Consequently, noisy ground currents from logic gates do not interact with the analog signals.

Inevitably, two or more circuits will be joined together with their grounds at differential potentials. In these situations, the differential input of an instrumentation amplifier, with its high CMR, can accurately transfer analog information from one circuit to another.

MAXIMIZING NEGATIVE PSR

Using well stabilized, low-noise power supplies is always recommended for precision analog circuits. However even with good supplies, there will be small changes in output voltage due to temperature variations and line voltage variations. In turn, these voltage changes will affect the amplifier output due to finite power-supply rejection (PSR).

The AMP-05's PSR can be maximized in critical applications by adding a trim potentiometer (see Figure 6). Positive PSR cannot be trimmed by external means but this is better than negative PSR by as much as 20dB, and therefore trimming should not be necessary. Adjusting the negative PSR trim potentiometer also affects output offset voltage, V_{OOS}. Therefore in systems where offset correction is not employed, a V_{OOS} null potentiometer can be added if needed. In practice, the interaction between these two potentiometers is not a problem.

PSR/V_{OOS} trimming procedure: 1) adjust both potentiometers to mid-position; 2) superimpose a low-frequency 1V peak-to-peak sinewave on the negative supply; 3) adjust PSR trim potentiometer for minimum output ripple; 4) remove AC signal from the power supply and null the AMP-05's output offset voltage using the V_{OOS} null potentiometer. Steps 1 and 4 are deleted when only PSR trimming is required.

FIGURE 6: Additional Trim Potentiometer Maximizes Negative PSR

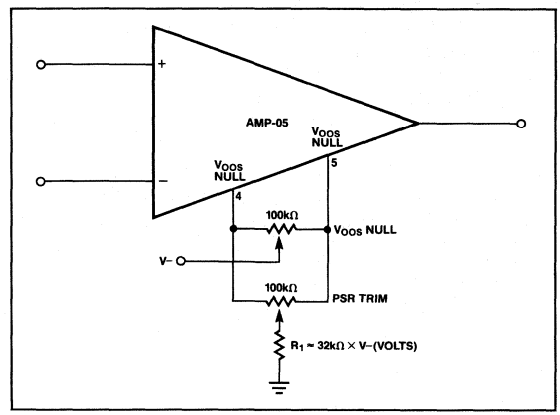
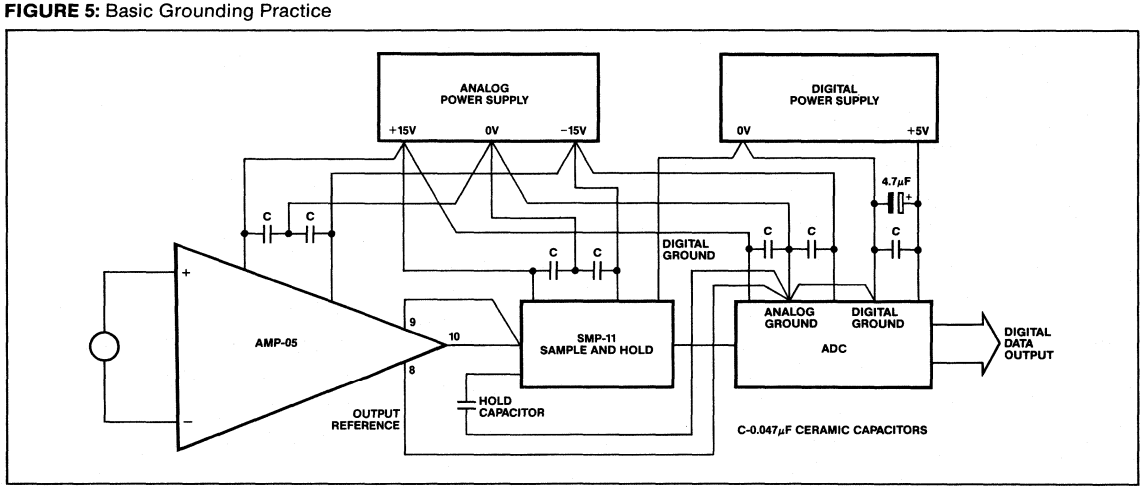


FIGURE 5: Basic Grounding Practice



CURRENT SOURCE

The on-board 100μA current source is provided for transducer excitation, powering a low-current voltage reference diode, and other functions. The current source is referenced from the positive supply rail (V+), and provides a high voltage compliance from 4 to 30V below V+. The output should not be pulled below V−. Output resistance is typically 3GΩ. Simple positive and negative voltage references can be generated by adding two resistors and an inexpensive op amp (Figures 7(a) and (b)). Temperature stability can be improved by replacing R1 with a low-current zener or voltage reference diode such as the LM185. The output reference voltage can be increased beyond the zener voltage by adding resistor R3 to add gain around the OP-77.

If the current source is not used it may be left floating or connected to V−.

SENSE AND REFERENCE TERMINALS

The sense terminal completes the feedback path for the instrumentation amplifier output stage and is normally connected directly to the output. The output signal is specified with respect to the reference terminal, which is normally connected to analog ground.

If high output currents are expected and/or the load is situated some distance from the amplifier, voltage drops due to trace or wire resistance will cause errors. Under these conditions, the sense and reference terminals can be used to "remote sense" the load as shown in Figure 8. This method of connection puts the I × R drops inside the feedback loop and virtually eliminates the error. An unbalance in the lead resistances from the sense and reference pins does not degrade CMR, but will change the output offset voltage. For example, a large unbalance of 3Ω will change the output offset by only 1mV.

FIGURE 7: Generating a Reference Voltage Using the On-Board Current-Source

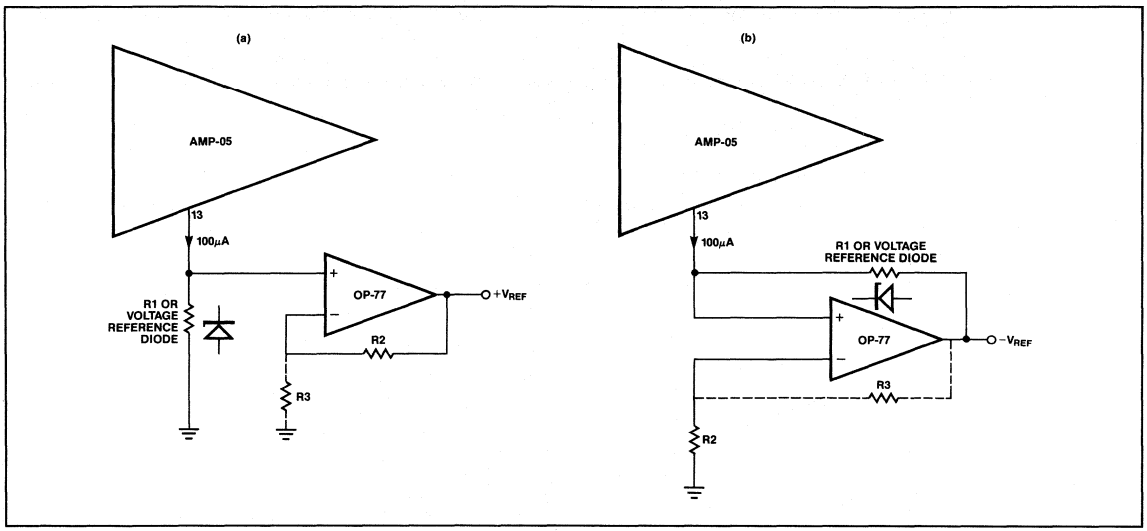
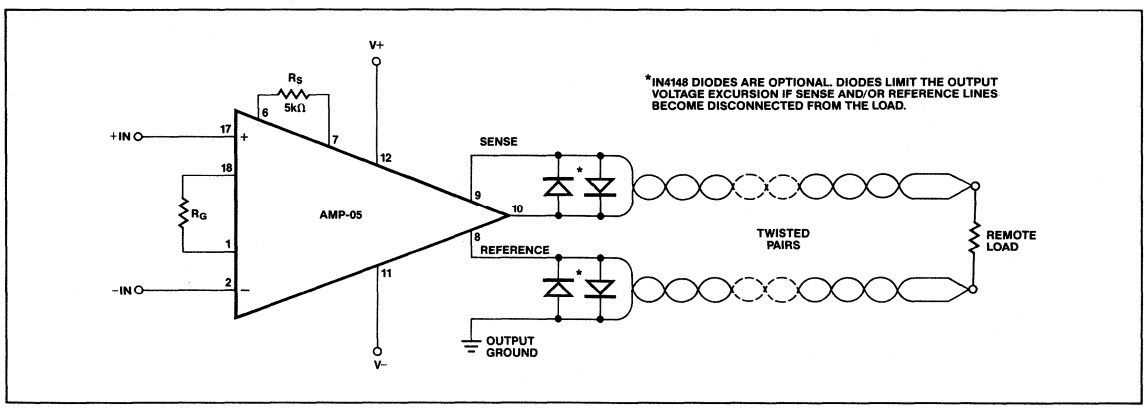


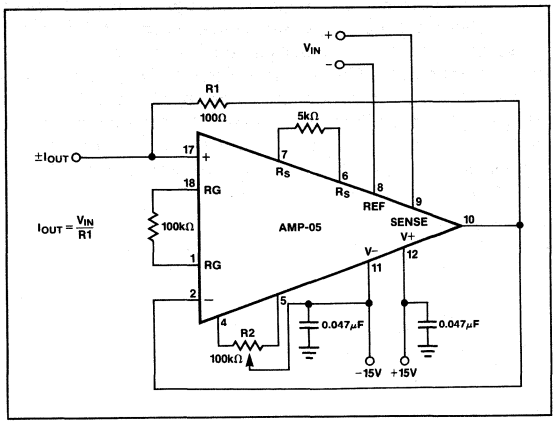
FIGURE 8: Remote Load Sensing



HIGH-COMPLIANCE CURRENT SOURCE

The inputs and outputs of the AMP-05 can be transposed to make a precision bipolar current source (refer to Figure 9). Reference and sense pins become differential inputs and the "old" input now monitors the voltage across a precision current-sense resistor, R1. Voltage gain is set at unity, so the transfer function is simply $I_{OUT} = V_{IN\ (differential)}/R1$. Using a 100Ω resistor for R1 and limiting output current to ±10mA, a reasonable limit for power dissipation reasons, gives a ±1V input requirement for full-scale output. Voltage compliance for ±10mA output is ±10V with a typical output resistance of 50MΩ. Linearity is better than 16-bits at this current level. Potentiometer R2 will trim the output current to zero with the two inputs grounded, and fine gain adjustment is accomplished by trimming R_S or R_G.

FIGURE 9: High-Compliance Current Source With 16-Bit Linearity

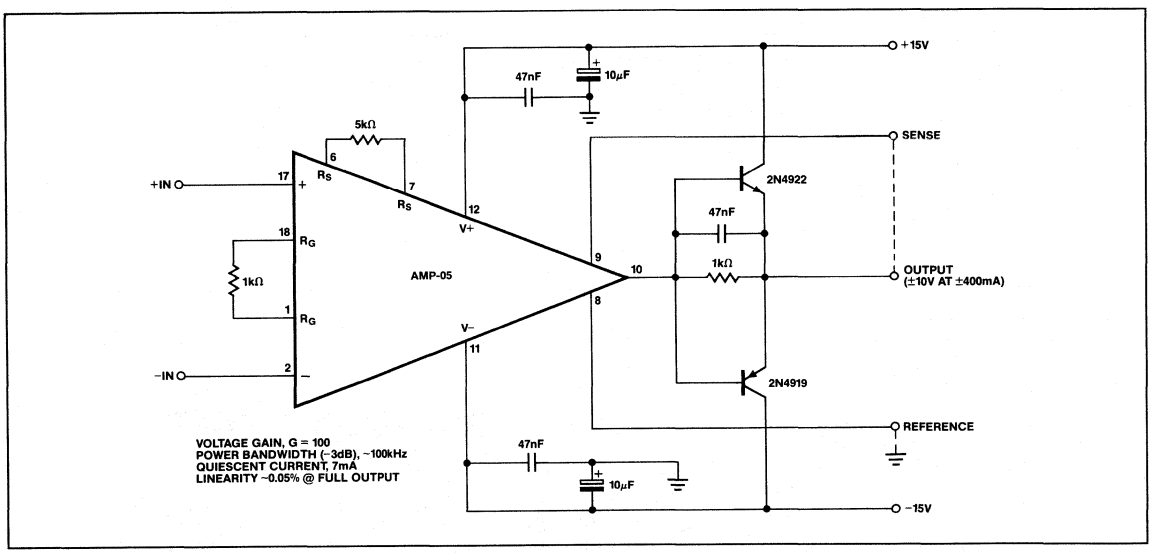


If the class B output stage shown in Figure 10 is added to the basic current-source, then the output current capability is increased to over 100mA with excellent linearity.

SERVO AMPLIFIER

The AMP-05's output power can be boosted by adding a simple class B output stage without increasing the amplifier's quiescent current of 7mA (refer to Figure 10). The 47nF capacitor connected across the transistor's base-emitter junctions prevents instability at V_{OUT} near ground, and reduces high-frequency crossover distortion. DC linearity is typically 0.05% when driving ±10V at ±400mA.

FIGURE 10: Adding two transistors increases output current to ±400mA without affecting the quiescent current of 7mA. Power bandwidth is 100kHz.



ANALOG-MULTIPLEXED DATA ACQUISITION SYSTEMS

For conditioning and digitizing multiple analog signals, there are two traditional system approaches. One dedicates an instrumentation amplifier to condition each input signal, then the high-level outputs are multiplexed and fed to an analog-to-digital converter (ADC). This system is expensive on a "per-channel" basis. A more economical approach is to multiplex unconditioned analog signals and feed them to a programmable-gain instrumentation amplifier, which conditions them before conversion. The per-channel cost drops as the number of channels increases. For this system to have a scan rate comparable to the first, the amplifier's settling-time should be less than the ADC's conversion time. The AMP-05, with its fast settling-time of 15μs maximum to 12 bits, is ideal for this single IA data acquisition system.

A digitally-controlled gain network can easily be added to the AMP-05 as described below.

PROGRAMMABLE-GAIN INSTRUMENTATION AMPLIFIER (PGIA)

Figure 11 shows a programmable gain instrumentation amplifier with digitally selectable gains of 1, 10, 100, and 1000. Each gain set resistor has two MOSFET switches connected back-to-back to prevent all but leakage current from flowing when a switch is OFF. In the high gain positions of 100 and 1000, the calculated values of gain resistor, R_G, are reduced to compensate for the switch ON resistance. The nonlinear switch resistance introduces a slight gain nonlinearity at high gain settings. The PGIA selects gain values in 20μs, including the amplifier settling-time. Gain temperature coefficient depends on R_S, R_G, and on the temperature coefficient of the MOSFET's ON resistance. Values of 15 and 30ppm/°C can be achieved at gains of 1 and 1000, respectively, despite the effect of the high tempco switches.

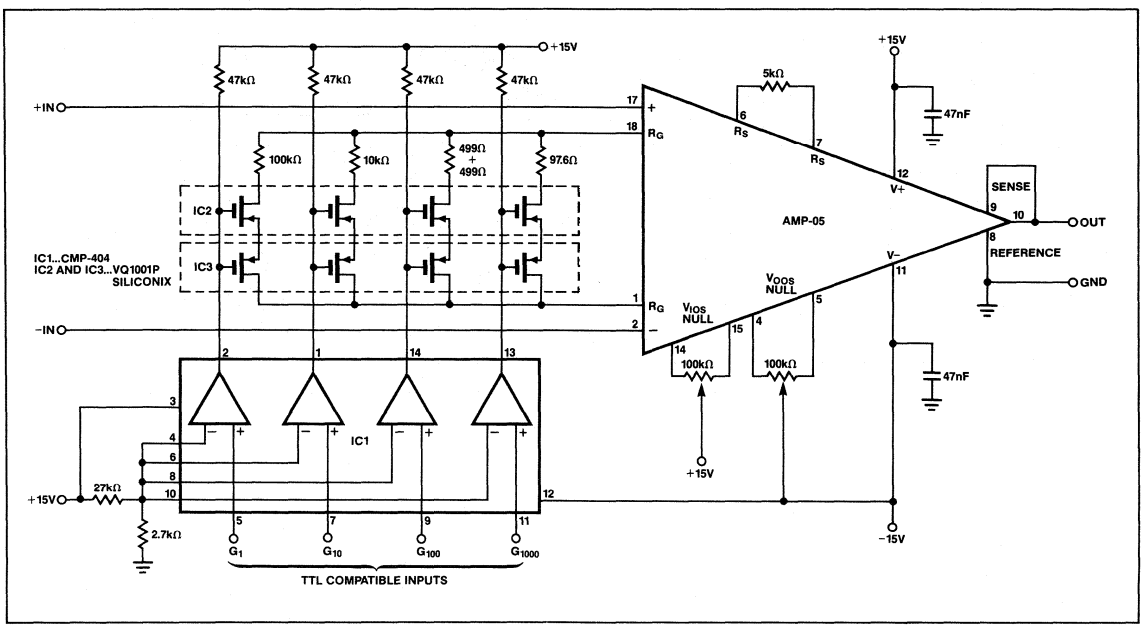
Where fast gain switching is not required, reed relays can substitute for the MOSFET switches. Reed relays have lower ON resistance and OFF leakage current errors. For gains of 100 and 1000, the values of R_G should be increased to 1kΩ and 100Ω respectively, because of lower switch ON resistance. Gain linearity is improved over the original circuit.

AUTO-ZERO SYSTEMS

Offset voltage and drift can be a major error source in high-accuracy systems of 12 bits and above. To minimize initial offset voltage and its associated temperature drift, an auto-zero system can be employed. The technique can potentially keep offset errors well below 1 LSB on a 12-bit system over wide variations in ambient temperature.

For example, consider an instrumentation amplifier set to a gain of 1000 and driving a 12-bit analog-to-digital converter. The input offset voltage drift is 2.5μV/°C, and the output offset voltage drift is negligible. The equivalent output drift is 1000 × 2.5μV/°C, or 2.5mV/°C—more than 1 LSB/°C for a 10V full-scale range. An ambient temperature change from 25°C to 125°C would produce 102 LSBs of drift, excluding the ADC's drift.

FIGURE 11: The AMP-05 makes an excellent programmable-gain instrumentation amplifier. Combined gain-switching and settling-time to 12 bits falls below 20μs. Linearity is better than 12 bits over a gain range 1 to 1000.



Obviously, to limit drift to 1 LSB or less over temperature demands some means of offset correction. Usually both hardware and software are employed to generate an error correction signal which is fed into the reference input of the instrumentation amplifier. Software alone could remove the system's offset error, but at the expense of the full-scale range for very large errors. Part of a typical auto-zero system is shown in Figure 12.

The sequence of events for auto-zeroing a system starts with switching the multiplexer so that the amplifier's two inputs are grounded. The amplifier is given time to settle, and the ADC (not shown) digitizes any system offset. The computer reads the offset and feeds a digital correction to the digital-to-analog converter. To verify that the offset is nulled, a second conversion may be performed, and the multiplexer then switches to measure the input signal.

For a system with a digitally programmable gain, the auto-zeroing process should be repeated for each gain setting. Each correction value can be stored in memory and recalled and refreshed as needed to correct for system drift with time and temperature.

SETTLING-TIME MEASUREMENT

Figure 13 is the test circuit used to measure settling-time. The circuit technique is similar to the "false sum-node" technique used to measure op amp settling-time. For simplicity, the connections for input and output offset nulling are not shown on the circuit, but null pots are required. Measurement set-up:

1. Set switches to G = 1, ground V_{IN}, and short-circuit R_G.
2. Adjust V_{IOS} null pot for minimum output voltage on pin 10.
3. Remove short-circuit from R_G and adjust V_{OOS} null pot for minimum output voltage on pin 10.
4. Apply a low frequency (~100Hz) $20V_{p-p}$ square-wave to V_{IN} and adjust 200Ω pot for minimum square-wave on V_{OUT}.
5. Increase square-wave input frequency and monitor V_{OUT} with an oscilloscope. Settling-time to a 0.025% error band for a 20V input step is measured with limits of ±2.5mV at V_{OUT}.
6. Change switch gain-positions and repeat settling-time measurements for G = 10, 100, and 1000.

FIGURE 12: Instrumentation Amplifier with Offset Correction System

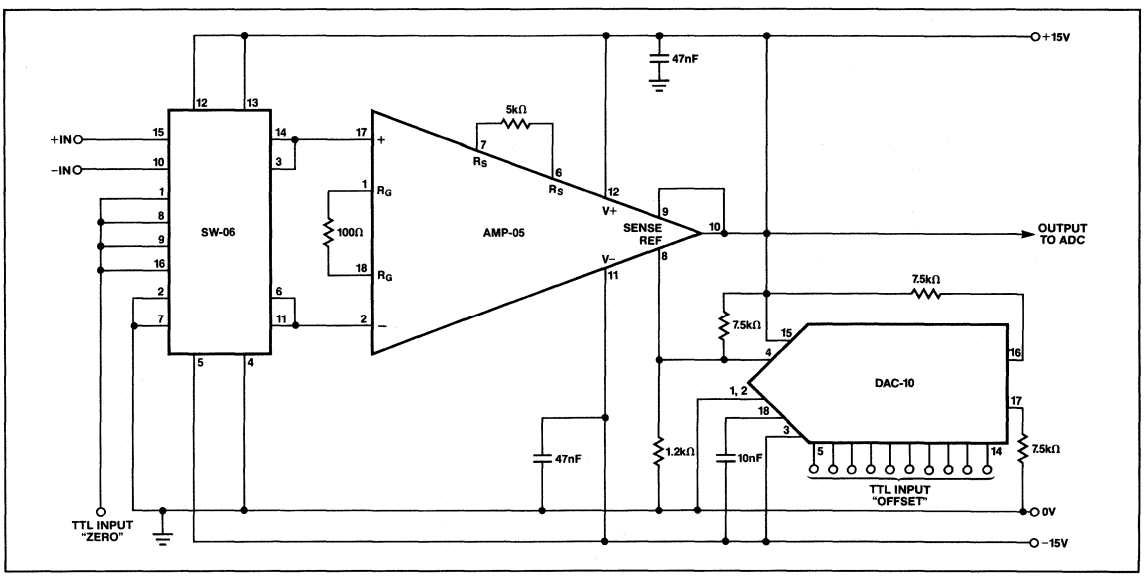


FIGURE 13: Settling-Time Test Circuit

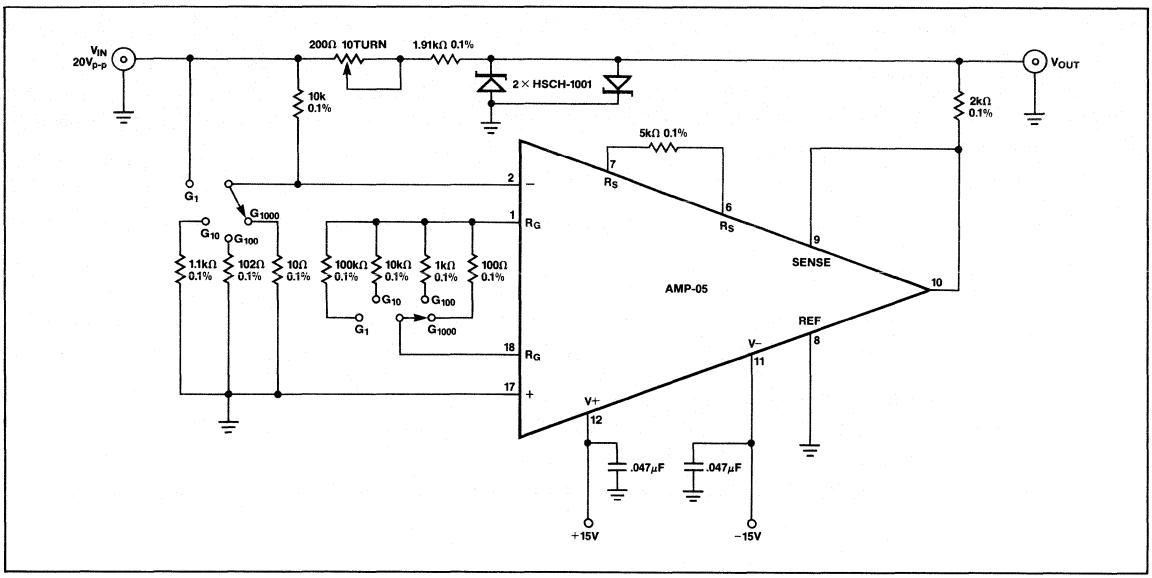
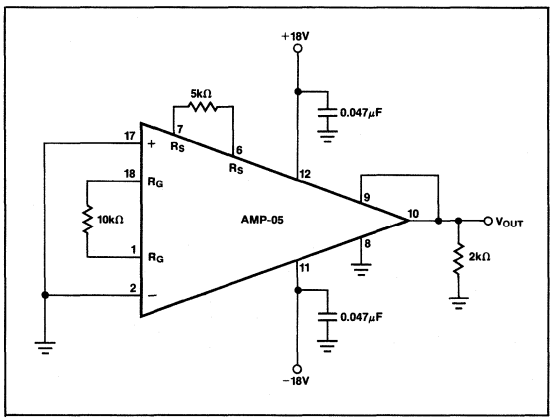


FIGURE 14: Burn-In Circuit



Ultra Low Noise Differential Audio Preamplifier

SSM-2016

FEATURES

- Ultra Low Voltage Noise ..... 800pV/$\sqrt{Hz}$ Typ
- High Slew Rate ..... 10V/μs Typ
- Very Low Harmonic Distortion ..... @ G = 1000 0.009% Typ
- Wide Bandwidth ..... @ G = 1000 650kHz Typ
- Very Wide Supply Voltage Range ..... ±9V to ±36V
- High Output Drive Capability ..... ±40mA Min
- High Common-Mode Rejection ..... 100dB Typ
- Low Cost

APPLICATIONS

- Low Noise High-Gain Microphone Preamplifier
- Bus Summing Amplifier
- Differential Line Receiver
- Low Noise Instrumentation Amplifier

ORDERING INFORMATION

PACKAGE PLASTIC 16-PIN	OPERATING TEMPERATURE RANGE
SSM2016P	–25°C to +55°C

GENERAL DESCRIPTION

The SSM-2016 is an ultra low noise, low distortion differential audio preamplifier. The input referred noise of the SSM-2016 is about 800pV/$\sqrt{Hz}$ which will result in a noise figure of 1dB when operated with a 150Ω source impedance. This ensures that a large number of inputs can be paralleled without seriously degrading the signal-to-noise ratio. In addition, this device provides exceptionally low harmonic distortion of only 0.009%(G = 1000, f = 1kHz) Typ.

Fabricated on a high voltage process, the SSM-2016 is capable of operating from a wide supply voltage range of ±9V to ±36V. A copper lead- frame DIP package is used to permit 1.5W of dissipation when driving heavy loads or operating from elevated supplies.

Continued

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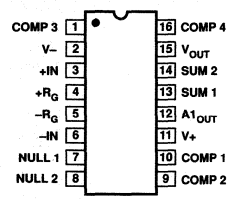
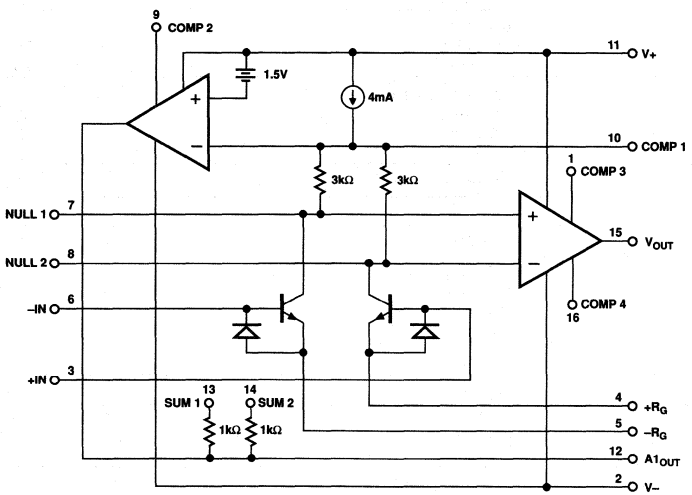
PIN CONNECTIONS



16-PIN PLASTIC DIP (P-Suffix)

BLOCK DIAGRAM



The SSM-2016 has been granted mask work protection under the Semiconductor Chip Protection Act of 1983.

GENERAL DESCRIPTION *Continued*

The SSM-2016 can source or sink a minimum of 40mA allowing a jack-field to be driven directly.

At low gains, the SSM-2016 offers a bandwidth of about 1MHz and 650kHz at 60dB of gain. Slew rate is typically 10V/µs at all gains.

The SSM-2016 is packaged in a 16-pin epoxy DIP and performance and characteristics are guaranteed over the operating temperature range of –25°C to +55°C.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±38V
Recommended Supply Voltage Range ..... ±9V to ±36V
Current Into Any Pin (Except Pins 2, 11, and 15) 40mA
Lead Temperature (Soldering, 60 sec) ..... 300°C
Storage Temperature ..... –65°C to +150°C
Package Dissipation 2W
Short-Circuit Duration (Note 1) ..... Indefinite
Operating Temperature Range ..... –25°C to 55°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
16-Pin Plastic DIP (P)	76	33	°C/W

NOTES:
1. Short-circuit duration is indefinite, provided dissipation limit is not exceeded.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm18V$, $R_1 = R_2 = 5k\Omega$, $R_3 = R_4 = 2k\Omega$, $T_A = +25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SSM-2016 MIN	SSM-2016 TYP	SSM-2016 MAX	UNITS
Total Harmonic Distortion	THD	$V_O = 10V_{RMS}$, $R_L = 2k\Omega$				%
		G = 1000				
		f = 1kHz	–	0.009	0.015	
		f = 10kHz	–	0.015	0.02	
		G = 100				
		f = 1kHz	–	0.003	0.005	
		f = 10kHz	–	0.005	0.007	
		G = 10				
		f = 1kHz	–	0.002	0.003	
		f = 10kHz	–	0.003	0.005	
		$V_O = 10V_{RMS}$, $R_L = 600\Omega$, $V_S = \pm20V$				
		G = 1000				
		f = 1kHz	–	0.025	0.04	
		f = 10kHz	–	0.06	0.09	
		G = 100				
		f = 1kHz	–	0.008	0.015	
		f = 10kHz	–	0.02	0.04	
		G = 10				
		f = 1kHz	–	0.005	0.008	
		f = 10kHz	–	0.008	0.015	
Input Referred Voltage Noise (Note 1)	e_n	20kHz Bandwidth				μV_{RMS}
		G = 1000	–	0.11	0.16	
		G = 100	–	0.20	0.30	
		G = 10	–	0.80	1.2	
Input Current Noise (Note 1)	I_n	20 kHz Bandwidth	–	350	550	$pA/_{RMS}$
Slew Rate	SR		–	10	–	V/µs
–3dB Bandwidth (Note 2)	GBW	G = 1000	–	0.55	–	MHz
		G ≤ 100	–	1	–	
Input Offset Voltage	V_{OS}	G = 1000	–	0.5	2.5	mV
		G = 100	–	1.5	10	
		G = 10	–	5	8	
Input Bias Current	I_B	$V_{CM} = 0V$	–	9	25	µA
Input Offset Current	I_{OS}	$V_{CM} = 0V$	–	1.5	5.0	µA
Common-Mode Rejection Ratio	CMRR	G = 1000	96	100	–	dB
		G = 100	80.5	95	–	
		G = 10	64	75	–	
Power Supply Rejection Ratio	PSRR	$V_S = \pm9V$ to ±36V	90	100	–	dB
Common-Mode Voltage Range	CMVR		±7	±10	–	V

ELECTRICAL CHARACTERISTICS at $V_S = \pm 18V$, $R_1 = R_2 = 5k\Omega$, $R_3 = R_4 = 2k\Omega$, $T_A = +25°C$, unless otherwise noted.
Continued

PARAMETER	SYMBOL	CONDITIONS	SSM-2016 MIN	SSM-2016 TYP	SSM-2016 MAX	UNITS
Common-Mode Input Impedance	R_{INEM}		–	20	–	MΩ
Differential-Mode Input Impedance	R_{IN}	G = 1000	–	0.3	–	MΩ
		G = 100	–	3	–	
		G = 10	–	10	–	
Output Voltage Swing (Note 1)	V_O	$R_L = 2k\Omega$	±15	±17	–	V
		$R_L = 600\Omega$, $V_S = \pm 20V$	±15	±17	–	
Output Current (Note 3)	I_{OUT}	Source	40	70	–	mA
		Sink	40	70	–	
Supply Current	I_{SY}	$V_{CM} = 0V$	10	12	16	mA
Error From Gain Equation			–	0.1	0.3	dB

NOTES:
1. Sample tested.
2. Bandwidth will be slew-rate limited at high output levels.
3. Output is protected from short circuits to ground or either supply.

Specifications subject to change; consult latest data sheet.

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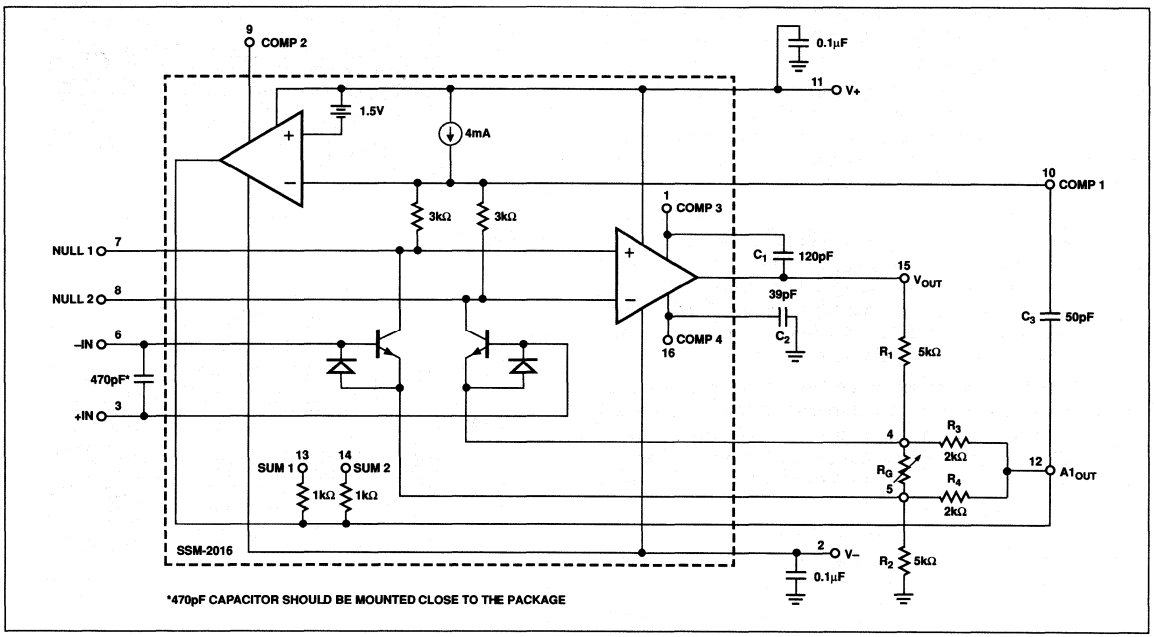


FIGURE 1: *Typical Preamplifier Amplification*

APPLICATIONS INFORMATION

PRINCIPLE OF OPERATION

The SSM-2016 operates as a true differential amplifier with feedback returned directly to the emitters of the input stage transistors by R_1 (See Figure 1). The differential pair is fed by a current source at the collectors and the required emitter current is supplied by a nulling (servo) amplifier through the external resistors R_3 and R_4 (Figure 1). This system produces both optimum noise and common-mode rejection while retaining a very high input impedance. The internal "servo" amplifier is used to control the input stage current independently of common-mode voltage and its output is accessible via pin 12.

GAIN SETTING

The nominal gain of the SSM-2016 is given by:

$$G = \frac{R_1 + R_2}{R_g} + \frac{R_1 + R_2}{R_3 + R_4} + 1$$

or

$$G = \frac{10k\Omega}{R_g} + 3.5 \quad \text{For } R_1 = R_2 = 5k\Omega,\ R_3 = R_4 = 2k\Omega$$

R_1 and R_2 should be equal to 5kΩ for best results. It is vital that good quality resistors be used in the gain setting network, since low quality types (notably carbon composition) can generate significant amounts of distortion and, under some conditions, low frequency noise.

The SSM-2016 is capable of operating at gains down to 3.5 at full performance. Gain range can be extended further by increasing R_3 and R_4 in Figure 1, but at the penalty of reduced common-mode input range. Gains below 2.5 are not practical unless the negative supply voltage is increased.

Note that tolerance of R_1 - R_4 directly affects the gain error and that good matching between R_1 - R_4 is essential to prevent degradation of the common-mode rejection performance.

The SSM-2016 provides internal 1kΩ resistors to replace R_3 and R_4 in applications where distortion is not too critical.

FREQUENCY COMPENSATION

The SSM-2016's internal "servo" amplifier is compensated by C_3, while C_1 and C_2 (see Figure 1) compensate the overall amplifier. The values shown maintain a very wide bandwidth with a good symmetrical slew rate. If desired, the bandwidth can be reduced by increasing the value of C_1.

NOISE PERFORMANCE

The SSM-2016's input referred noise is $0.11\mu V_{RMS}$ (20kHz bandwidth) at 60dB of gain, $0.2\mu V_{RMS}$ at 40dB, and $0.8\mu V_{RMS}$ at 20dB. The apparent increase at low gains is due to noise incurred in the feedback resistors and second stage becoming dominant. This noise is actually present at all times but becomes masked by input stage noise as the gain is increased.

The SSM-2016 is optimized for source impedances of 1kΩ or less and under these conditions, the noise performance is equal to the best discrete component designs. Considering that a "standard" microphone with impedance of 150Ω generates 1.6nV/$\sqrt{Hz}$ of thermal noise, the SSM-2016's 800pV/$\sqrt{Hz}$ of voltage noise or the corresponding noise figure of typically 1dB make the device virtually transparent to the user.

In applications where higher source impedances than 1kΩ are desired, the SSM-2015 preamplifier is recommended.

Another source of noise degradation is the chip's total power dissipation, since any increase in temperature will increase the noise. This effect is more pronounced at higher gains. As a result, the SSM-2016 uses a copper lead-frame package which greatly helps the power dissipation and the noise performance. The best noise performance of the SSM-2016 can be achieved at low supply voltages while driving light loads.

TOTAL HARMONIC DISTORTION

Figures 2 - 5 show the distortion behavior of SSM-2016. All measurements were taken at a $10V_{RMS}$ output to ensure a true "worst case" condition. No crossover distortion is observed at lower ouput levels. At 20dB of gain (Figure 2) total harmonic distortion (plus noise) is well below 0.01% at all audio frequencies. At 40dB of gain (Figure 3) some loading effects are evident, especially at higher frequencies, but the overall THD is still very low. The measurements at 60dB of gain (Figure 4) are a little misleading because the noise floor is at an equivalent level of 0.0085% at this gain. In fact, the real distortion components are not greatly increased from the 40dB case.

Figure 5 shows the intermodulation distortion performance of the SSM-2016. A basic SMPTE type test was performed with the main generator swept from 2.5kHz to 20kHz. The 60dB reading is once more mostly noise.

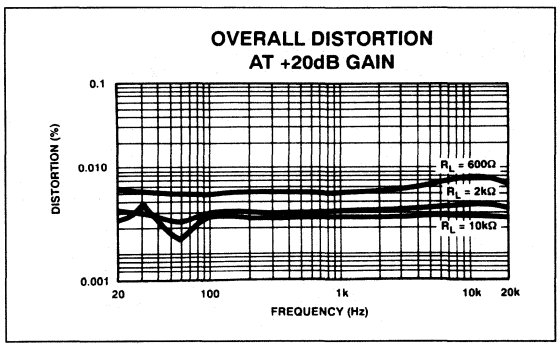


FIGURE 2

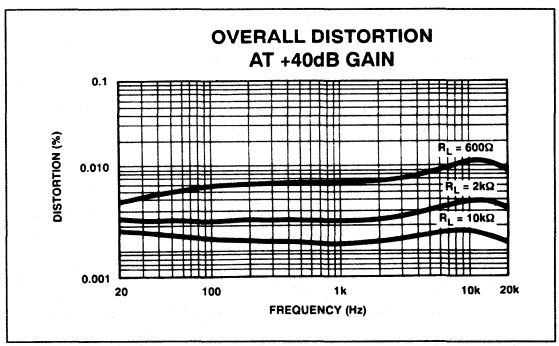


FIGURE 3

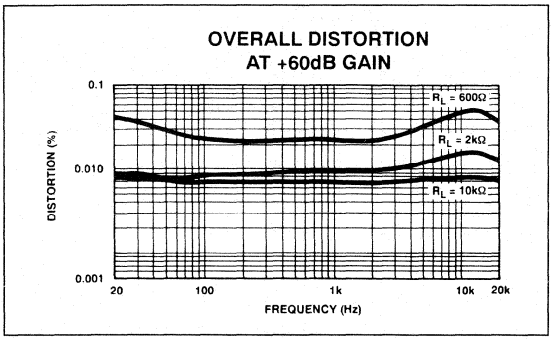


FIGURE 4

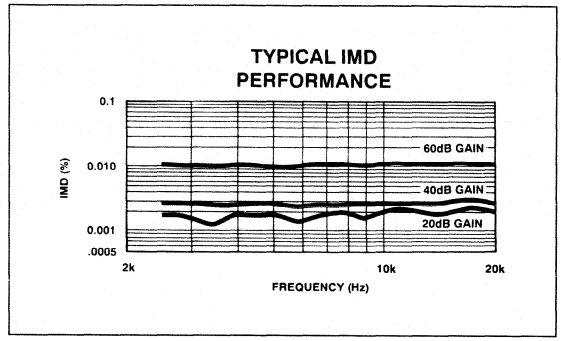


FIGURE 5

4

DRIVE CAPABILITY

Fabricated on a high voltage process, the SSM-2016 is capable of operating from ±9V to ±36V supplies. In addition, the powerful output stage is designed to drive a jack-field directly. The SSM-2016 is capable of driving a $10V_{RMS}$ sine wave into 600Ω load using ±18V supplies. However, ±20V or greater supplies are recommended to give a more comfortable headroom. A copper lead-frame DIP package is used to permit 1.5W of dissipation when driving heavy loads or operating from elevated supplies.

INPUTS

The SSM-2016 offers protection diodes across the base-emitter junctions of the input transistors. These prevent accidental avalanche breakdown which could seriously degrade noise performance. Additional clamp diodes are also provided to prevent the inputs from being forced too far beyond the supplies.

Although the SSM-2016's inputs are fully floating, care must be exercised to ensure that both inputs have a DC bias connection capable of maintaining them within the input common-mode range. The usual method of achieving this is to ground one side of the transducer as in Figure 6a, but an alternative way is to float the transducer and use two resistors to set the bias point as in figure 6b. The value of these resistors can be up to 10kΩ, but they should be kept as small as possible to limit common-mode pickup. Noise contribution by resistors themselves is negligible since it is attenuated by the transducer's impedance. Balanced transducers give the best noise immunity, and interface directly as in Figure 6c.

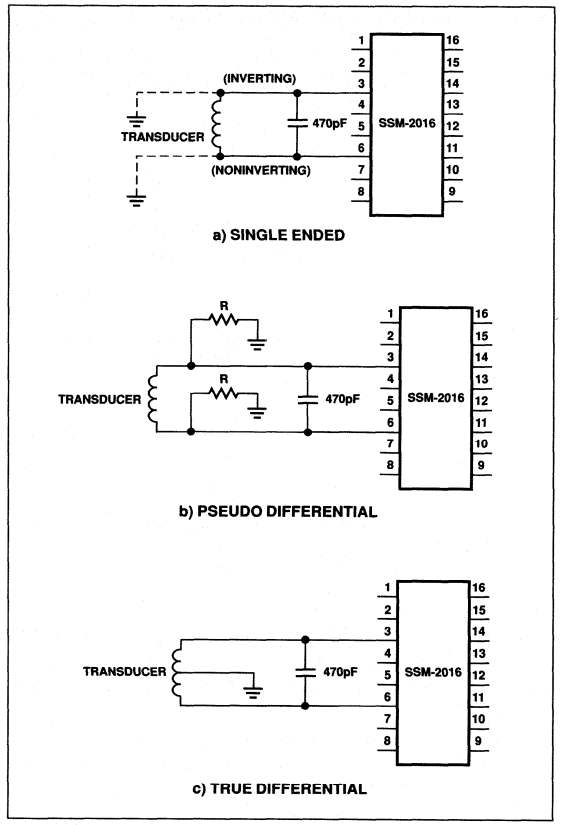


FIGURE 6: *Three Ways of Interfacing Transducers for High-Noise Immunity*

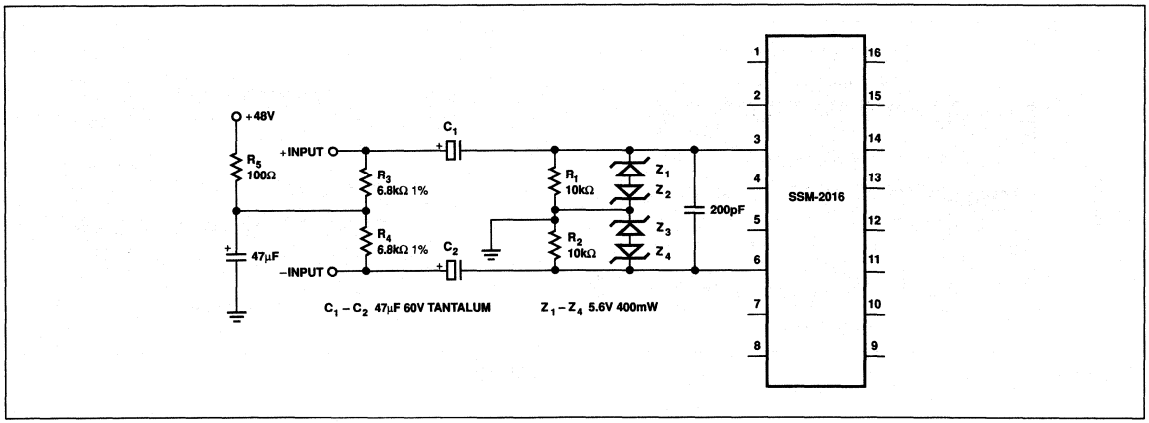


FIGURE 7: *SSM-2016 with Phantom Power*

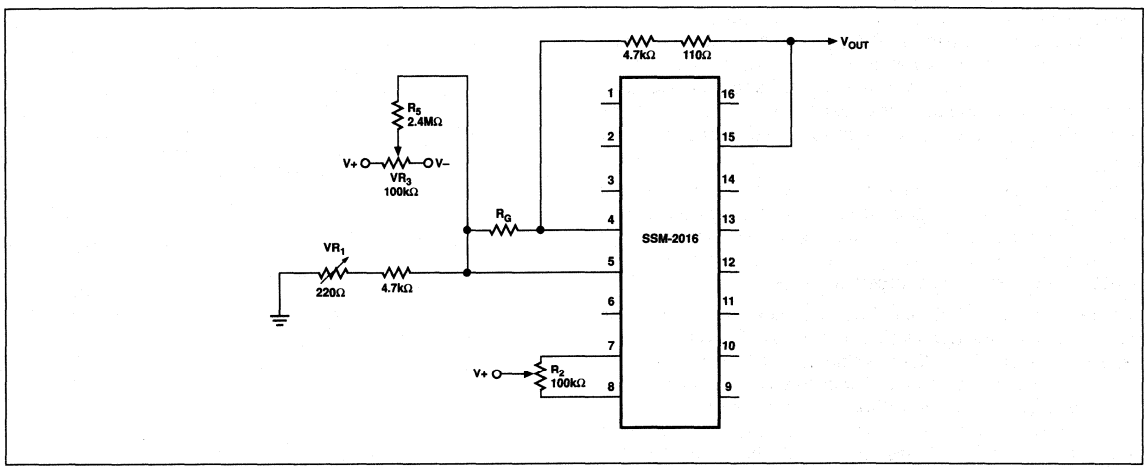


FIGURE 8: *Trimming Circuit*

PHANTOM POWERING

A typical phantom microphone powering circuit is shown in Figure 7. Z_1 through Z_4 provide transient overvoltage protection for the SSM-2016 whenever microphones are plugged in and out.

TRIMMING

The SSM-2016 accommodates four types of trimming: gain, high-gain offset, low-gain offset, and common-mode rejection. All four can be accomplished with the circuits shown in Figure 8.

Gain trim on the SSM-2016 is readily accomplished by adjusting R_G. VR_1 adjusts the common-mode rejection, VR_2 the high-gain offset, and VR_3 the low-gain offset. Common-mode rejection is best adjusted by applying an $8V_{p-p}$ 60Hz (50Hz in Europe) sine wave to both inputs and adjusting VR_1 for minimum output. Interaction is minimized by trimming the high-gain offset first, followed by the CMR and finally the low-gain offset. A two-pass trim is recommended for best results. Note that the overall gain has been reduced slightly to allow convenient values of resistors.

If the low-gain offset trim is not used, then gain control feedthrough can still be reduced by adjusting the high-gain offset to equal the low-gain offset by means of VR_2.

BUS SUMMING AMPLIFIER

In addition to its use as a microphone preamplifier, the SSM-2016 can be used as a very low noise summing amplifier. Such a circuit is particularly useful when many medium impedance outputs are summed together to produce a high effective noise gain.

The principle of the summing amplifier is to ground the SSM-2016 inputs . Under these conditions, pins 4 and 5 are AC virtual grounds sitting about 0.65V below ground. Any current injected into these points must flow through the feedback resistor (R_1) and hence are amplified to appear in the the output. Moreover, both positive (pin 5) and negative (pin 6) transfer characteristics are available simultaneously in contrast to the usual "inverting only" configuration.

To remove the 0.65V offset, the circuit of Figure 9 is recommended.

A_2 forms a "servo" amplifier feeding the SSM-2016's inputs. This places pins 4 and 5 at a true DC virtual ground. R_6 in conjunction with C_6 remove the voltage noise of A_2 and in fact just about any operational amplifier will work well here since it is removed from the signal path. If the DC offset at pins 4 and 5 is not too critical, then the servo loop can be replaced by the diode biasing scheme of Figure 9a. If AC coupling is used throughout, then pins 3 and 6 may be directly grounded.

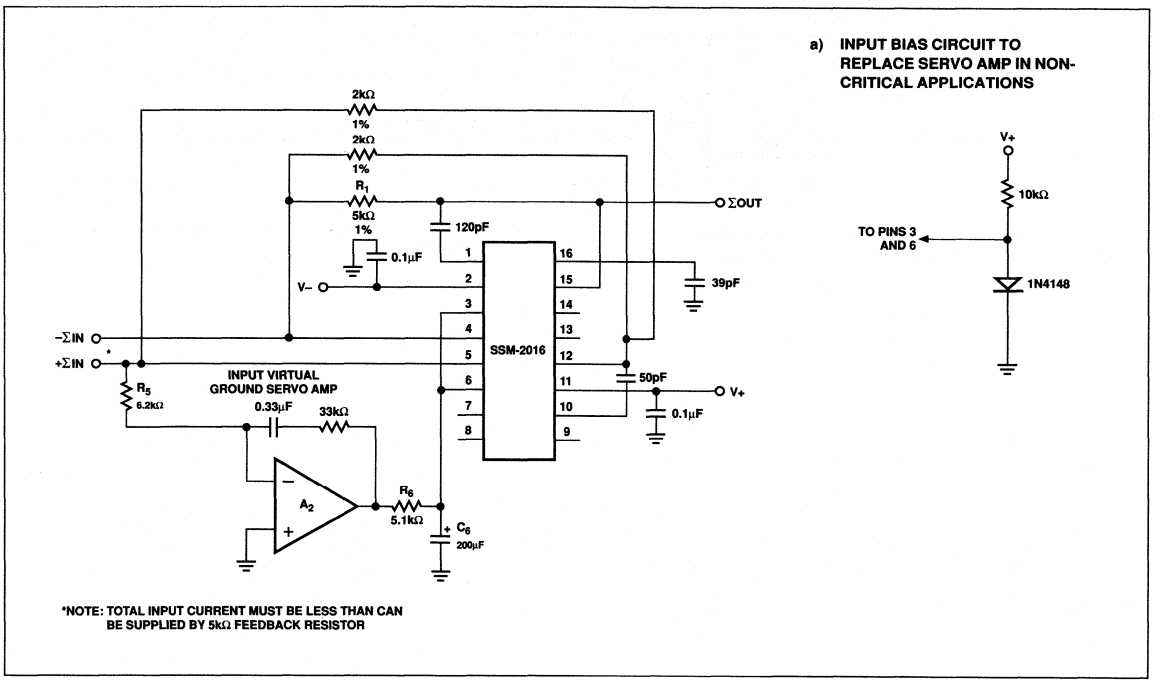


FIGURE 9: *Bus Summing Amplifier*

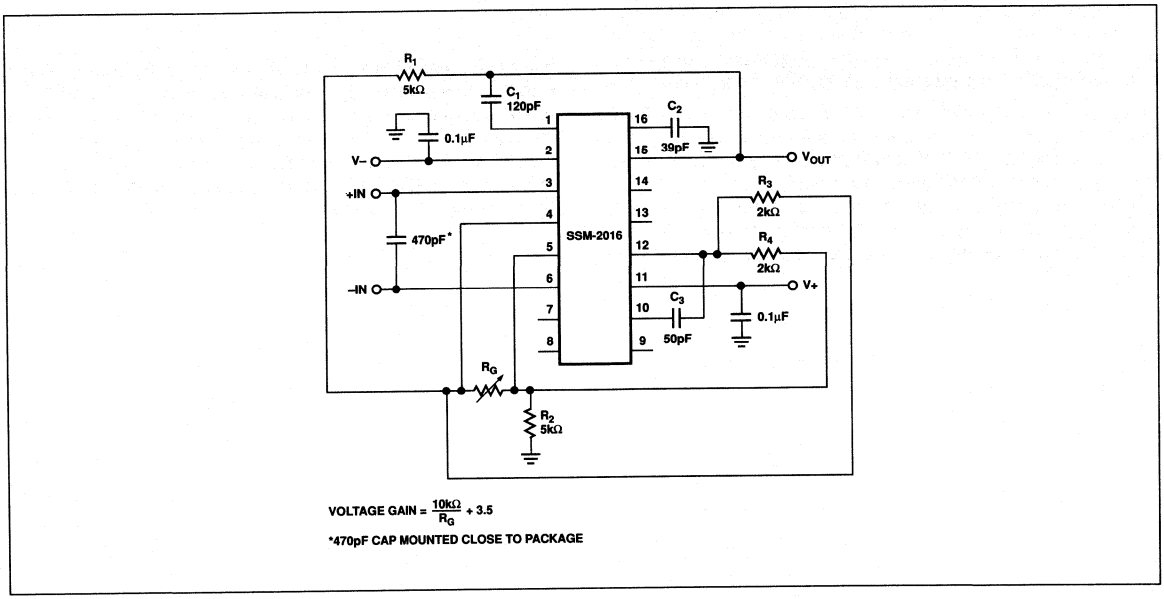


FIGURE 10: *Typical Connection for Breadboarding Purposes*

Self-Contained Audio Preamplifier

SSM-2017

FEATURES

- Excellent Noise Performance: 950 pV/$\sqrt{Hz}$ or 1.5 dB Noise Figure
- Ultralow THD: <0.01% @ G = 100 Over the Full Audio Band
- Wide Bandwidth: 1 MHz @ G = 100
- High Slew Rate: 17 V/μs typ
- Unity Gain Stable
- True Differential Inputs
- Subaudio 1/f Noise Corner
- 8-Pin Mini-DIP with Only One External Component Required
- Very Low Cost
- Extended Temperature Range: −40°C to +85°C

APPLICATIONS

- Audio Mix Consoles
- Intercom/Paging Systems
- Two-Way Radio
- Sonar
- Digital Audio Systems

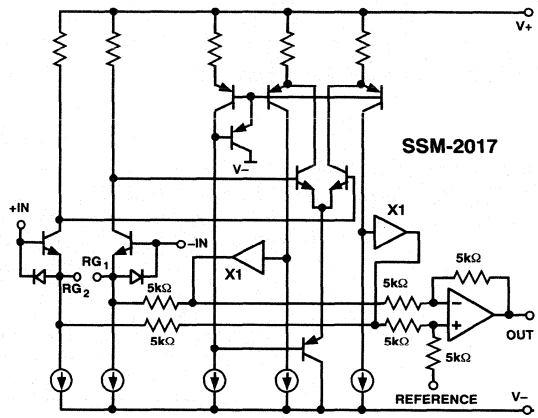
GENERAL DESCRIPTION

The SSM-2017 is a latest generation audio preamplifier combining SSM preamplifier design expertise with advanced processing. The result is excellent audio performance from a self-contained 8-pin mini-DIP device, requiring only one external gain set resistor or potentiometer. The SSM-2017 is further enhanced by its unity gain stability.

Key specifications include ultralow noise (1.5 dB noise figure) and THD (<0.01% at G = 100), complemented by wide bandwidth and high slew rate.

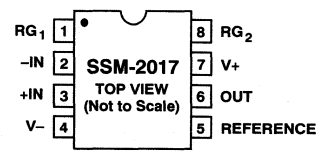
Applications for this low cost device include microphone preamplifiers and bus summing amplifiers in professional and consumer audio equipment, sonar, and other applications requiring a low noise instrumentation amplifier with high gain capability.

FUNCTIONAL BLOCK DIAGRAM

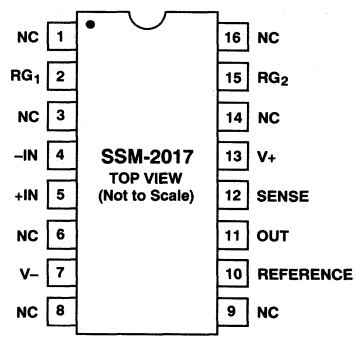


PIN CONNECTIONS

Epoxy Mini-DIP (P Suffix)
and
Hermetic DIP (Z Suffix)



16-Pin SOIC (S Suffix)



NC = NO CONNECT

SSM-2017—SPECIFICATIONS

(V_S = ±15 V and −40°C ≤ T_A ≤ +85°C, unless otherwise specified. Typical specifications apply at T_A = +25°C.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
DISTORTION PERFORMANCE		T_A = +25°C V_O = 7 V_{RMS} R_L = 5 kΩ				
Total Harmonic Distortion Plus Noise	THD+N	G = 1000, f = 1 kHz		0.012		%
		G = 100, f = 1 kHz		0.005		%
		G = 10, f = 1 kHz		0.004		%
		G = 1, f = 1 kHz		0.008		%
NOISE PERFORMANCE						
Input Referred Voltage Noise Density	e_n	f = 1 kHz, G = 1000		0.95		nV/√Hz
		f = 1 kHz; G = 100		1.95		nV/√Hz
		f = 1 kHz; G = 10		11.83		nV/√Hz
		f = 1 kHz; G = 1		107.14		nV/√Hz
Input Current Noise Density	i_n	f = 1 kHz, G = 1000		2		pA/√Hz
DYNAMIC RESPONSE						
Slew Rate	SR	G = 10 R_L = 4.7 kΩ C_L = 50 pF T_A = +25°C	10	17		V/μs
Small Signal Bandwidth	$BW_{-3\ dB}$	G = 1000		200		kHz
		G = 100		1000		kHz
		G = 10		2000		kHz
		G = 1		4000		kHz
INPUT						
Input Offset Voltage	V_{IOS}			0.1	1.2	mV
Input Bias Current	I_B	V_{CM} = 0 V		6	25	μA
Input Offset Current	I_{OS}	V_{CM} = 0 V		±0.002	±2.5	μA
Common-Mode Rejection	CMR	V_{CM} = ±8 V				
		G = 1000	80	112		dB
		G = 100	60	92		dB
		G = 10	40	74		dB
		G = 1, T_A = +25°C	26	54		dB
		G = 1, T_A = −40°C to +85°C	20	54		dB
Power Supply Rejection	PSR	V_S = ±6 V to ±18 V				
		G = 1000	80	124		dB
		G = 100	60	118		dB
		G = 10	40	101		dB
		G = 1	26	82		dB
Input Voltage Range	IVR		±8			V
Input Resistance	R_{IN}	Differential, G = 1000		1		MΩ
		G = 1		30		MΩ
		Common Mode, G = 1000		5.3		MΩ
		G = 1		7.1		MΩ
OUTPUT						
Output Voltage Swing	V_O	R_L = 2 kΩ; T_A = +25°C	±11.0	±12.3		V
Output Offset Voltage	V_{OOS}			−40	500	mV
Minimum Resistive Load Drive		T_A = +25°C		2		kΩ
		T_A = −40°C to +85°C		4.7		kΩ
Maximum Capacitive Load Drive				50		pF
Short Circuit Current Limit	I_{SC}	Output-to-Ground Short		±50		mA
Output Short Circuit Duration					10	sec
GAIN						
Gain Accuracy	$R_G = \frac{10\ k\Omega}{G-1}$	T_A = +25°C				
		R_G = 10 Ω, G = 1000		0.25	1	dB
		R_G = 101 Ω, G = 100		0.20	1	dB
		R_G = 1.1 kΩ, G = 10		0.20	1	dB
		R_G = ∞, G = 1		0.05	0.5	dB
Maximum Gain	G			70		dB

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
REFERENCE INPUT						
Input Resistance				10		kΩ
Voltage Range				±8		V
Gain to Output				1		V/V
POWER SUPPLY						
Supply Voltage Range	V_S		±6		±22	V
Supply Current	I_{SY}	V_{CM} = 0 V, R_L = ∞		±10.6	±14.0	mA

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±22 V
Input Voltage . . . . . Supply Voltage
Output Short Circuit Duration . . . . . 10 sec
Storage Temperature Range (P, Z Packages) . −65°C to +150°C
Junction Temperature (T_J) . . . . . −65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . 300°C
Operating Temperature Range . . . . . −40°C to +85°C
Thermal Resistance[1]
8-Pin Hermetic DIP (Z): θ_{JA} = 134; θ_{JC} = 12 . . . . . °C/W
8-Pin Plastic DIP (P): θ_{JA} = 96; θ_{JC} = 37 . . . . . °C/W
16-Pin SOIC (S): θ_{JA} = 92; θ_{JC} = 27 . . . . . °C/W

NOTE
[1]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for cerdip and plastic DIP; θ_{JA} is specified for device soldered to printed circuit board for SOIC package.

ORDERING GUIDE

Model	Operating Temperature Range*	Package
SSM-2017P	−40°C to +85°C	8-Pin Plastic DIP
SSM-2017Z	−40°C to +85°C	8-Pin Hermetic DIP
SSM-2017S	−40°C to +85°C	16-Lead SOIC

*XIND = −40°C to +85°C.

4

Typical Performance Characteristics

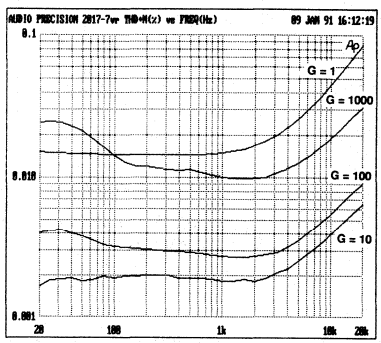


Figure 1. Typical THD+Noise at G = 1, 10, 100, 1000; V_O = 7 V_{RMS}, V_S = ±15 V, R_L = 5 kΩ; T_A = +25°C*

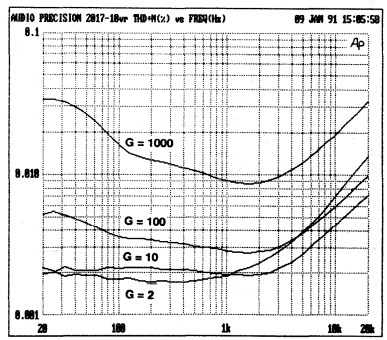


Figure 2. Typical THD+Noise at G = 2, 10, 100, 1000; V_O = 10 V_{RMS}, V_S = ±18 V, R_L = 5 kΩ; T_A = +25°C*

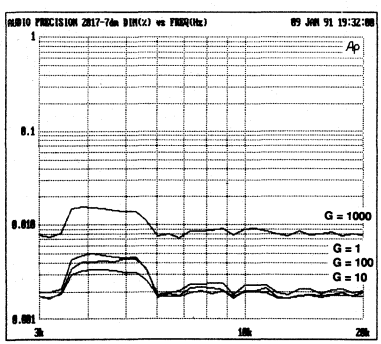


Figure 3. Typical DIM at G = 1, 10, 100, 1000; V_O = 7 V_{RMS}, V_S = ±15 V, R_L = 5 kΩ; T_A = +25°C

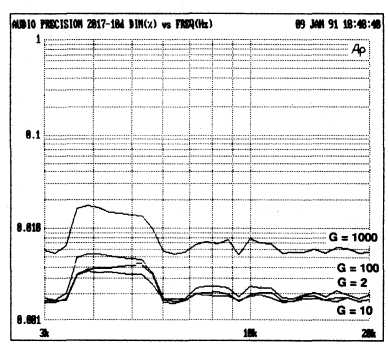


Figure 4. Typical DIM at G = 2, 10, 100, 1000; V_O = 10 V_{RMS}, V_S = ±18 V, R_L = 5 kΩ; T_A = +25°C

*80 kHz low-pass filter used for Figures 1–2.

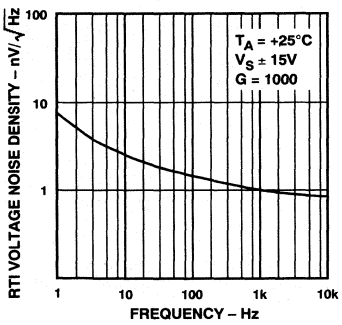


Figure 5. Voltage Noise Density vs. Frequency

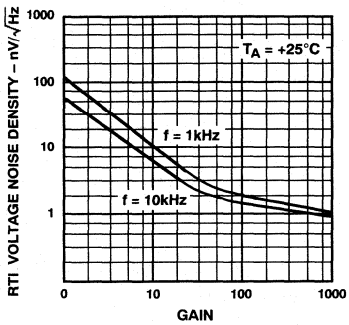


Figure 6. RTI Voltage Noise Density vs. Gain

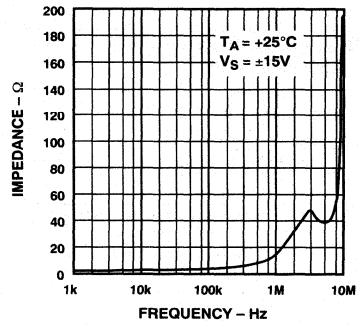


Figure 7. Output Impedance vs. Frequency

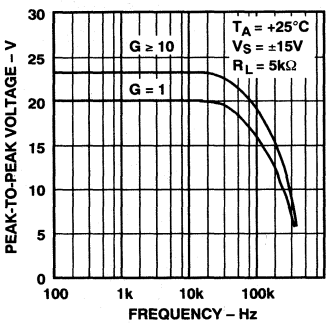


Figure 8. Maximum Output Swing vs. Frequency

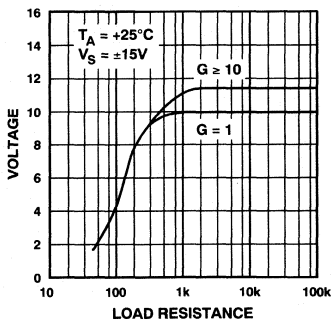


Figure 9. Maximum Output Voltage vs. Load Resistance

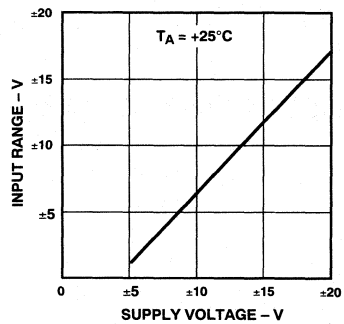


Figure 10. Input Voltage Range vs. Supply Voltage

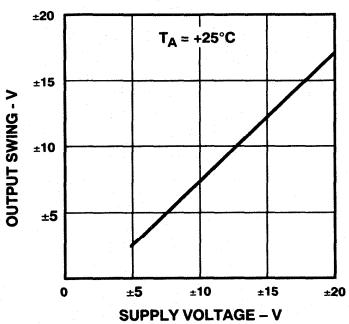


Figure 11. Output Voltage Range vs. Supply Voltage

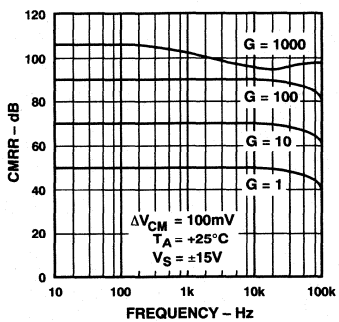


Figure 12. CMRR vs. Frequency

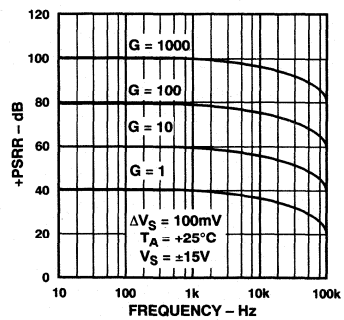


Figure 13. +PSRR vs. Frequency

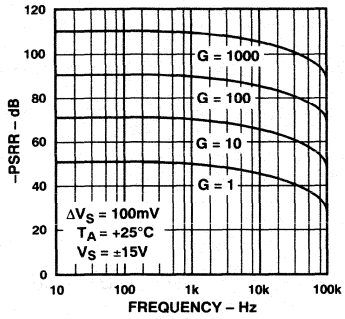


Figure 14. –PSRR vs. Frequency

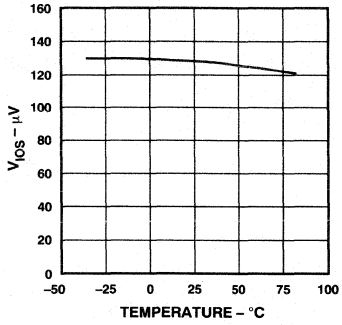


Figure 15. V_{IOS} vs. Temperature

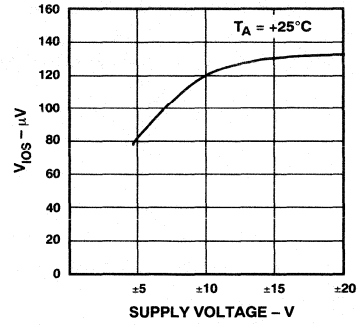


Figure 16. V_{IOS} vs. Supply Voltage

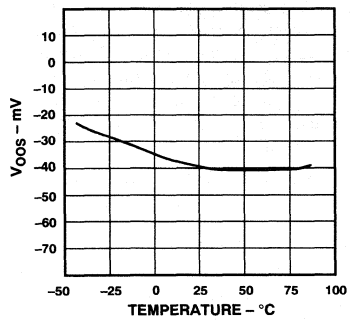


Figure 17. V_{OOS} vs. Temperature

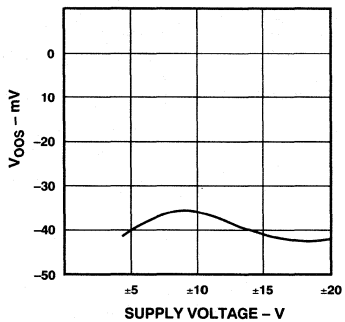


Figure 18. V_{OOS} vs. Supply Voltage

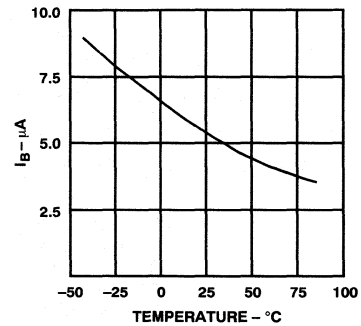


Figure 19. I_B vs. Temperature

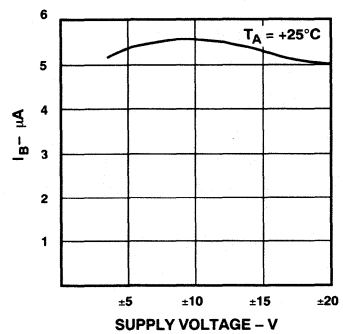


Figure 20. I_B vs. Supply Voltage

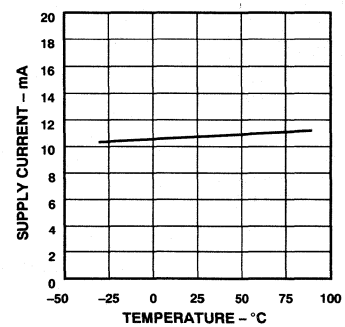


Figure 21. I_{SY} vs. Temperature

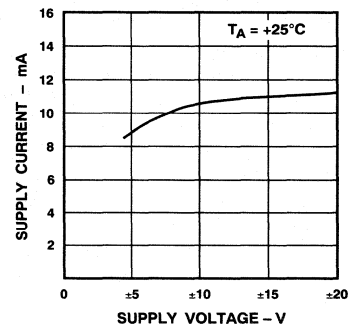
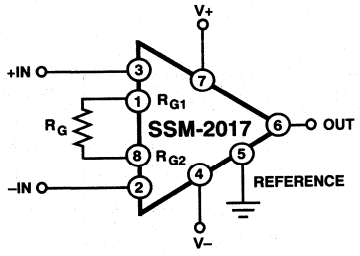


Figure 22. I_{SY} vs.Supply Voltage

SSM-2017—Applications Information



$$G = \frac{V_{OUT}}{(+IN) - (-IN)} = \left(\frac{10k\Omega}{R_G}\right) + 1$$

Basic Circuit Connections

GAIN

The SSM-2017 only requires a single external resistor to set the voltage gain. The voltage gain, G, is:

$$G = \frac{10\ k\Omega}{R_G} + 1$$

and

$$R_G = \frac{10\ k\Omega}{G - 1}$$

For convenience, Table I lists various values of R_G for common gain levels.

Table I. Values of R_G for Various Gain Levels

A_V	dB	R_G
1	0	NC
3.2	10	4.7k
10	20	1.1k
31.3	30	330
100	40	100
314	50	32
1000	60	10

The voltage gain can range from 1 to 3500. A gain set resistor is not required for unity gain applications. Metal-film or wire-wound resistors are recommended for best results.

The total gain accuracy of the SSM-2017 is determined by the tolerance of the external gain set resistor, R_G, combined with the gain equation accuracy of the SSM-2017. Total gain drift combines the mismatch of the external gain set resistor drift with that of the internal resistors (20 ppm/°C typ).

Bandwidth of the SSM-2017 is relatively independent of gain as shown in Figure 23. For a voltage gain of 1000, the SSM-2017 has a small-signal bandwidth of 200 kHz. At unity gain, the bandwidth of the SSM-2017 exceeds 4 MHz.

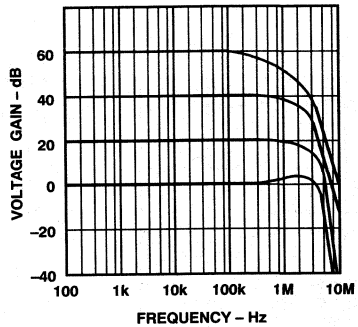


Figure 23. Bandwidth of the SSM-2017 for Various Values of Gain

NOISE PERFORMANCE

The SSM-2017 is a very low noise audio preamplifier exhibiting a typical voltage noise density of only 1 nV/$\sqrt{Hz}$ at 1 kHz. The exceptionally low noise characteristics of the SSM-2017 are in part achieved by operating the input transistors at high collector currents since the voltage noise is inversely proportional to the square root of the collector current. Current noise, however, is directly proportional to the square root of the collector current. As a result, the outstanding voltage noise performance of the SSM-2017 is obtained at the expense of current noise performance. At low preamplifier gains, the effect of the SSM-2017's voltage and current noise is insignificant.

The total noise of an audio preamplifier channel can be calculated by:

$$E_n = \sqrt{e_n^2 + (i_n R_s)^2 + e_t^2}$$

where:

E_n = total input referred noise

e_n = amplifier voltage noise

i_n = amplifier current noise

R_s = source resistance

e_t = source resistance thermal noise.

For a microphone preamplifier, using a typical microphone impedance of 150 Ω the total input referred noise is:

e_n = 1 $nV/\sqrt{Hz}$ @ 1 *kHz, SSM-2017* e_n

i_n = 2 $pA/\sqrt{Hz}$ @ 1 *kHz, SSM-2017* i_n

R_S = 150 Ω, *microphone source impedance*

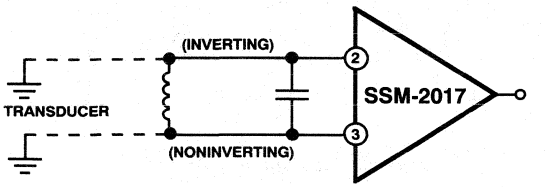
e_t = 1.6 $nV/\sqrt{Hz}$ @ 1 *kHz, microphone thermal noise*

$E_n = \sqrt{(1\ nV/\sqrt{Hz})^2 + 2\,(2\ pA/\sqrt{Hz} \times 150\ \Omega)^2 + (1.6\ nV/\sqrt{Hz})^2} = 1.93\ nV/\sqrt{Hz}$ @ 1 *kHz*.

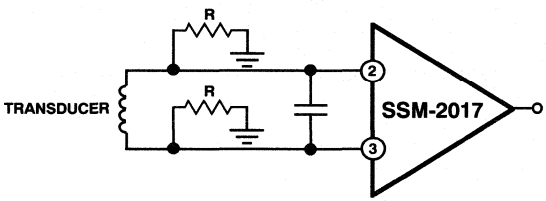
This total noise is extremely low and makes the SSM-2017 virtually transparent to the user.

INPUTS

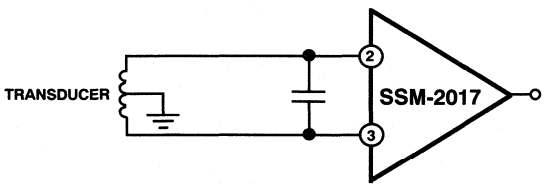
The SSM-2017 has protection diodes across the base emitter junctions of the input transistors. These prevent accidental avalanche breakdown which could seriously degrade noise performance. Additional clamp diodes are also provided to prevent the inputs from being forced too far beyond the supplies.



a. Single Ended



b. Pseudo Differential



c. True Differential

Figure 24. Three Ways of Interfacing Transducers for High Noise Immunity

Although the SSM-2017's inputs are fully floating, care must be exercised to ensure that both inputs have a dc bias connection capable of maintaining them within the input common-mode range. The usual method of achieving this is to ground one side of the transducer as in Figure 24a, but an alternative way is to float the transducer and use two resistors to set the bias point as in Figure 24b. The value of these resistors can be up to 10 kΩ, but they should be kept as small as possible to limit common-mode pickup. Noise contribution by resistors themselves is negligible since it is attenuated by the transducer's impedance. Balanced transducers give the best noise immunity and interface directly as in Figure 24c.

REFERENCE TERMINAL

The output signal is specified with respect to the reference terminal, which is normally connected to analog ground. The reference may also be used for offset correction or level shifting. A reference source resistance will reduce the common-mode rejection by the ratio of 5 kΩ/R_{REF}. If the reference source resistance is 1 Ω, then the CMR will be reduced to 74 dB (5 kΩ/1 Ω = 74 dB).

COMMON-MODE REJECTION

Ideally, a microphone preamplifier responds only to the difference between the two input signals and rejects common-mode voltages and noise. In practice, there is a small change in output voltage when both inputs experience the same common-mode voltage change; the ratio of these voltages is called the common-mode gain. Common-mode rejection (CMR) is the logarithm of the ratio of differential-mode gain to common-mode gain, expressed in dB.

PHANTOM POWERING

A typical phantom microphone powering circuit is shown in Figure 25. Z_1 through Z_4 provide transient overvoltage protection for the SSM-2017 whenever microphones are plugged in or unplugged.

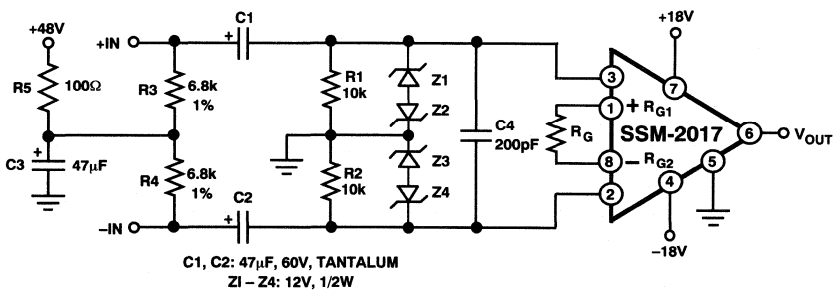


Figure 25. SSM-2017 in Phantom Powered Microphone Circuit

BUS SUMMING AMPLIFIER

In addition to is use as a microphone preamplifier, the SSM-2017 can be used as a very low noise summing amplifier. Such a circuit is particularly useful when many medium impedance outputs are summed together to produce a high effective noise gain.

The principle of the summing amplifier is to ground the SSM-2017 inputs. Under these conditions, Pins 1 and 8 are ac virtual grounds sitting about 0.55 V below ground.

To remove the 0.55 V offset, the circuit of Figure 26 is recommended.

A_2 forms a "servo" amplifier feeding the SSM-2017's inputs. This places Pins 1 and 8 at a true dc virtual ground. R4 in conjunction with C2 remove the voltage noise of A_2, and in fact just about any operational amplifier will work well here since it is removed from the signal path. If the dc offset at Pins 1 and 8 is not too critical, then the servo loop can be replaced by the diode biasing scheme of Figure 26. If ac coupling is used throughout, then Pins 2 and 3 may be directly grounded.

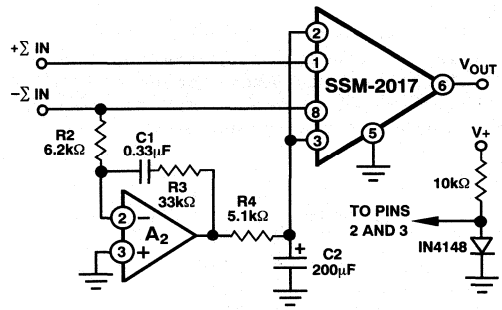


Figure 26. Bus Summing Amplifier

ANALOG DEVICES

High Common-Mode Rejection Differential Line Receiver

SSM-2141

FEATURES

- **High Common-Mode Rejection**
  - DC ..... 100dB Typ
  - 60Hz ..... 100dB Typ
  - 20kHz ..... 70dB Typ
  - 40kHz ..... 62dB Typ
- **Low Distortion** ..... 0.001% Typ
- **Fast Slew Rate** ..... 9.5V/μs Typ
- **Wide Bandwidth** ..... 3MHz Typ
- **Low Cost**
- **Complements SSM-2142 Differential Line Driver**

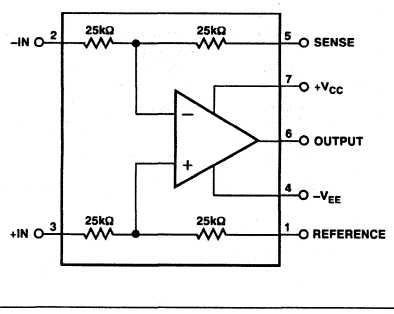
APPLICATIONS

- **Line Receivers**
- **Summing Amplifiers**
- **Buffer Amplifiers – Drives 600Ω Load**

ORDERING INFORMATION

PACKAGE	OPERATING TEMPERATURE RANGE
PLASTIC 8-PIN	
SSM2141P	XIND ($-40°C \leq T_A \leq +85°C$)

FUNCTIONAL DIAGRAM



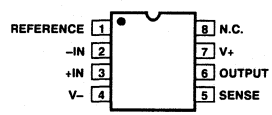
GENERAL DESCRIPTION

The SSM-2141 is an integrated differential amplifier intended to receive balanced line inputs in audio applications requiring a high level of noise immunity and optimum common-mode rejection. The SSM-2141 typically achieves 100dB of common-mode rejection (CMR), whereas implementing an op amp with four off-the-shelf precision resistors will typically achieve only 40dB of CMR – inadequate for high-performance audio.

The SSM-2141 achieves low distortion performance by maintaining a large slew rate of 9.5V/μs and high open-loop gain. Distortion is less than 0.002% over the full audio bandwidth. The SSM-2141 complements the SSM-2142 balanced line driver. Together, these devices comprise a fully integrated solution for equivalent transformer balancing of audio signals without the problems of distortion, EMI fields, and high cost.

Additional applications for the SSM-2141 include summing signals, differential preamplifiers, and 600Ω low distortion buffer amplifiers.

PIN CONNECTIONS



8-PIN EPOXY MINI-DIP (P-Suffix)

4

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Input Voltage (Note 1) ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous
Storage Temperature Range
P Package ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C
Junction Temperature ..... +150°C
Operating Temperature Range .....–40°C to +85°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
8-Pin Plastic DIP (P)	103	43	°C/W

NOTES:
1. For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP package.

ELECTRICAL CHARACTERISTICS at V_S = ±18V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SSM-2141 MIN	SSM-2141 TYP	SSM-2141 MAX	UNITS
Offset Voltage	V_{OS}	V_{CM} = 0V	–1000	25	1000	µV
Gain Error		No Load, V_{IN} = ±10V, R_S = 0Ω	–	0.001	0.01	%
Input Voltage Range	IVR	(Note 1)	±10	–	–	V
Common-Mode Rejection	CMR	V_{CM} = ±10V	80	100	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±6V to ±18V	–	0.7	15	µV/V
Output Swing	V_O	R_L = 2kΩ	±13	±14.7	–	V
Short-Circuit Current Limit	I_{SC}	Output Shorted To Ground	+45/–15	–	–	mA
Small-Signal Bandwidth (–3dB)	BW	R_L = 2kΩ	–	3	–	MHz
Slew Rate	SR	R_L = 2kΩ	6	9.5	–	V/µs
Total Harmonic Distortion	THD	R_L = 100kΩ R_L = 600Ω	– –	0.001 0.01	– –	%
Capacitive Load Drive Capability	C_L	No Oscillation	–	300	–	pF
Supply Current	I_{SY}	No Load	–	2.5	3.5	mA

NOTE:
1. Input voltage range guaranteed by CMR test.

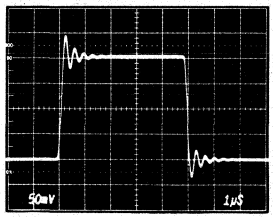
ELECTRICAL CHARACTERISTICS at V_S = ±18V, –40°C ≤ T_A ≤ +85°C.

PARAMETER	SYMBOL	CONDITIONS	SSM-2141 MIN	SSM-2141 TYP	SSM-2141 MAX	UNITS
Offset Voltage	V_{OS}	V_{CM} = 0V	–2500	200	2500	µV
Gain Error		No Load, V_{IN} = ±10V, R_S = 0Ω	–	0.002	0.02	%
Input Voltage Range	IVR	(Note 1)	±10	–	–	V
Common-Mode Rejection	CMR	V_{CM} = ±10V	75	90	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±6V to ±18V	–	1.0	20	µV/V
Output Swing	V_O	R_L = 2kΩ	±13	±14.7	–	V
Slew Rate	SR	R_L = 2kΩ	–	9.5	–	V/µs
Supply Current	I_{SY}	No Load	–	2.6	4.0	mA

NOTE:
1. Input voltage range guaranteed by CMR test.

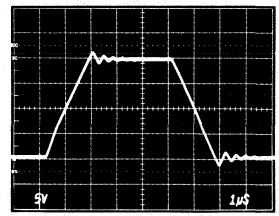
TYPICAL PERFORMANCE CHARACTERISTICS

SMALL-SIGNAL TRANSIENT RESPONSE



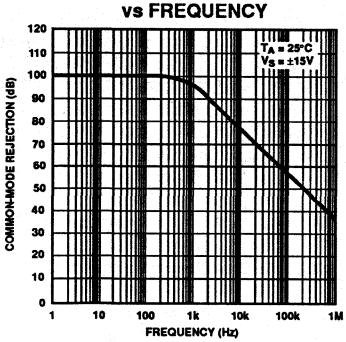
$T_A = +25°C$
$V_S = \pm 15V$

LARGE-SIGNAL TRANSIENT RESPONSE

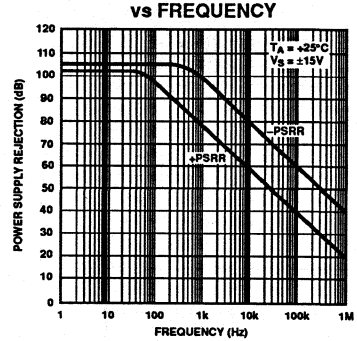


$T_A = +25°C$
$V_S = \pm 15V$

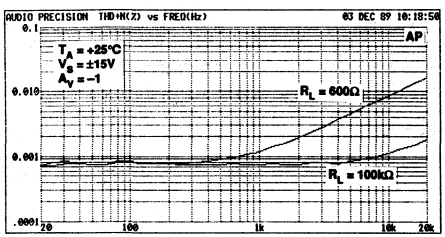
COMMON-MODE REJECTION vs FREQUENCY



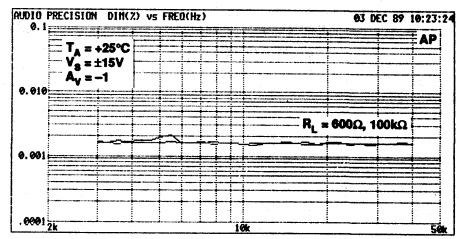
POWER SUPPLY REJECTION vs FREQUENCY



TOTAL HARMONIC DISTORTION vs FREQUENCY



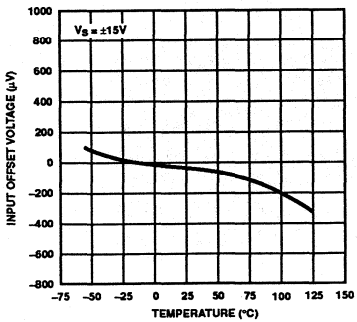
DYNAMIC INTERMODULATION DISTORTION vs FREQUENCY



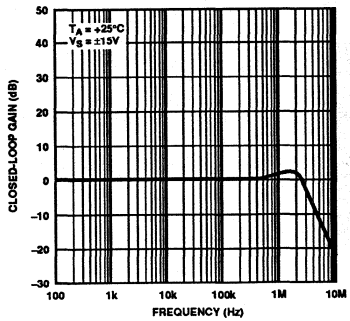
4

TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

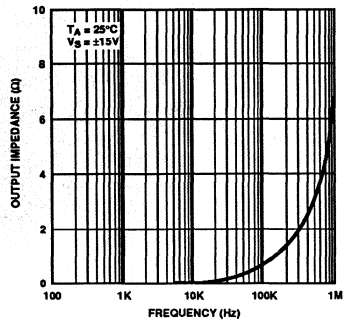
INPUT OFFSET VOLTAGE vs TEMPERATURE



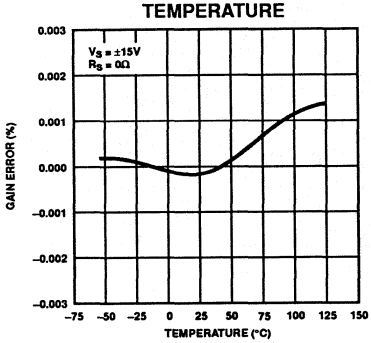
CLOSED-LOOP GAIN vs FREQUENCY



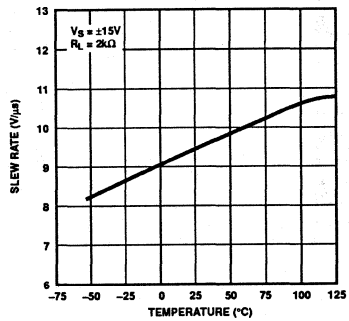
CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



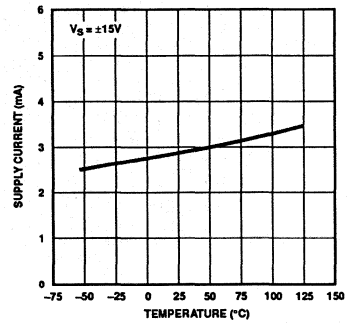
GAIN ERROR vs TEMPERATURE



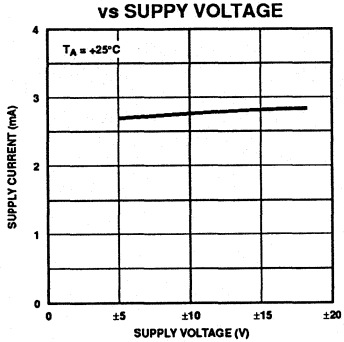
SLEW RATE vs TEMPERATURE



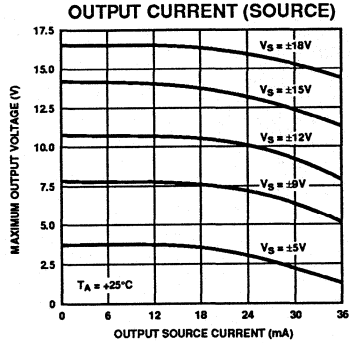
SUPPLY CURRENT vs TEMPERATURE



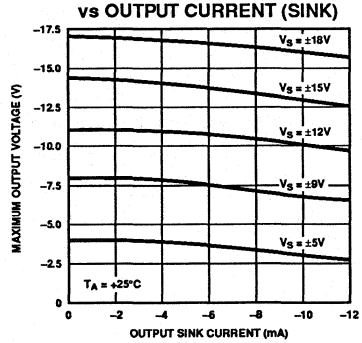
SUPPLY CURRENT vs SUPPY VOLTAGE



MAXIMUM OUTPUT VOLTAGE vs OUTPUT CURRENT (SOURCE)

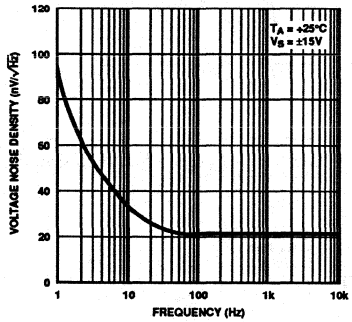


MAXIMUM OUTPUT VOLTAGE vs OUTPUT CURRENT (SINK)

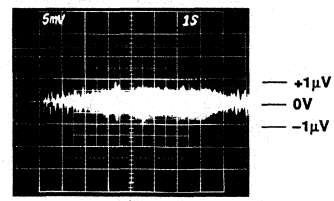


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

VOLTAGE NOISE DENSITY vs FREQUENCY

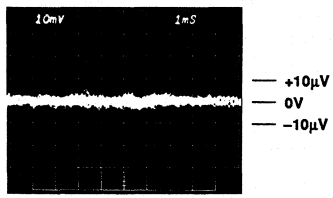


LOW FREQUENCY VOLTAGE NOISE



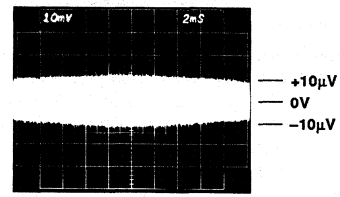
0.1 TO 10Hz PEAK-TO-PEAK NOISE

VOLTAGE NOISE FROM 0 TO 1kHz



T_A = +25°C
V_S = ±15V
NOTE: EXTERNAL AMPLIFIER GAIN = 1000;
THEREFORE, VERTICAL SCALE = 10μV/DIV.

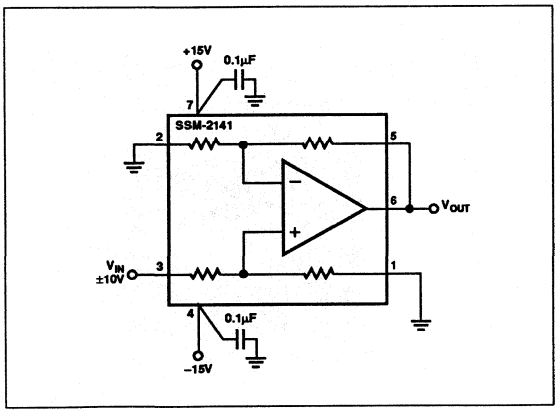
VOLTAGE NOISE FROM 0 TO 10kHz



T_A = +25°C
V_S = ±15V
NOTE: EXTERNAL AMPLIFIER GAIN = 1000;
THEREFORE, VERTICAL SCALE = 10μV/DIV.

4

SLEW RATE TEST CIRCUIT



APPLICATIONS INFORMATION

The SSM-2141 represents a versatile analog building block. In order to capitalize on fast settling time, high slew rate, and high CMR, proper decoupling and grounding techniques must be employed. For decoupling, place 0.1µF capacitor located within close proximity from each supply pin to ground.

MAINTAINING COMMON-MODE REJECTION

In order to achieve the full common-mode rejection capability of the SSM-2141, the source impedance must be carefully controlled. Slight imbalances of the source resistance will result in a degradation of DC CMR – even a 5Ω imbalance will degrade CMR by 20dB. Also, the matching of the reactive source impedance must be matched in order to preserve theCMRR over frequency.

APPLICATION CIRCUITS

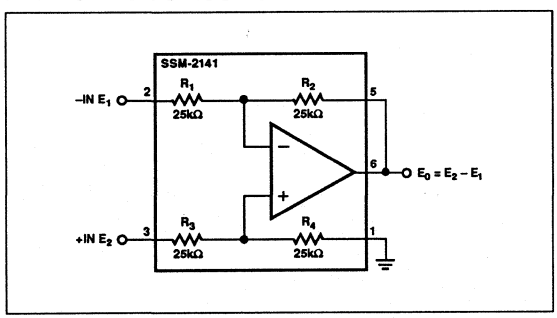


FIGURE 1: *Precision Difference Amplifier. Rejects Common-Mode Signal =* $\frac{[E_1 + E_2]}{2}$ *by 100dB*

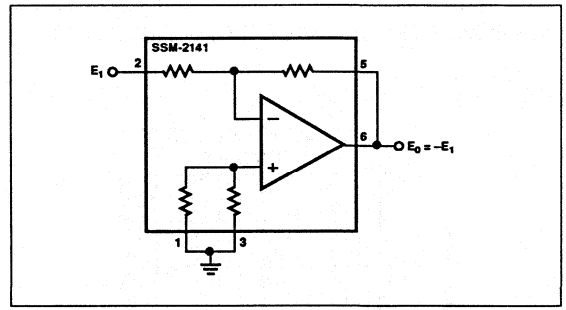


FIGURE 2: *Precision Unity-Gain Inverting Amplifier*

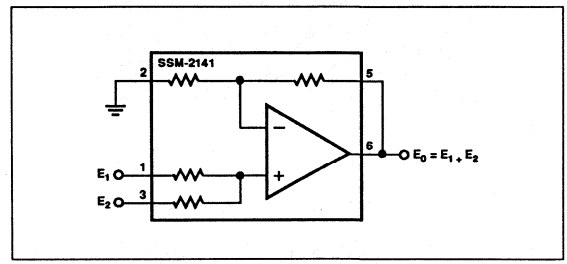


FIGURE 3: *Precision Summing Amplifier*

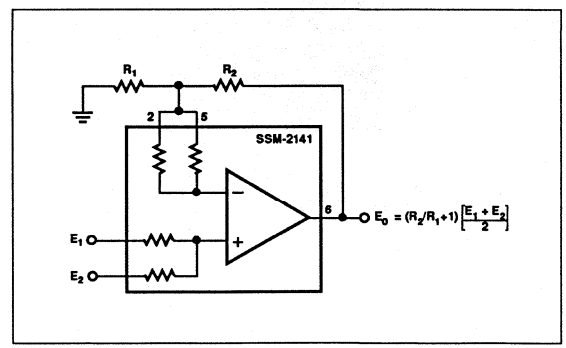


FIGURE 4: *Precision Summing Amplifier with Gain*

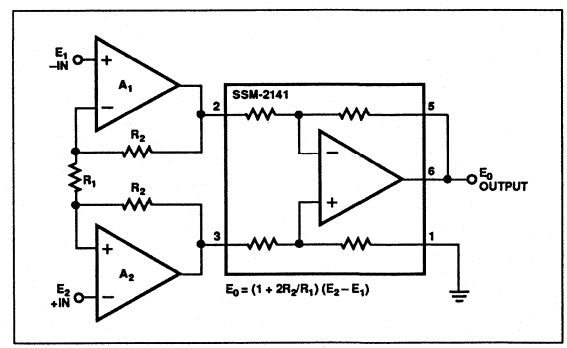


FIGURE 5: *Suitable instrumentation amplifier requirements can be addressed by using an input stage consisting of* A_1, A_2, R_1 *and* R_2.

ANALOG DEVICES

Balanced Line Driver

SSM-2142

FEATURES

- Transformer-Like Balanced Output
- Drives 10 V RMS Into a 600 Ω Load
- Stable When Driving Large Capacitive Loads and Long Cables
- Low Distortion
  - 0.006% typ 20 Hz-20 kHz, 10 V RMS into 600 Ω
- High Slew Rate
  - 15 V/μs typ
- Low Gain Error
  - (Differential or Single-Ended); 0.7% typ
- Outputs Short-Circuit Protected
- Available In Space-Saving 8-Pin Mini-DIP Package
- Low Cost

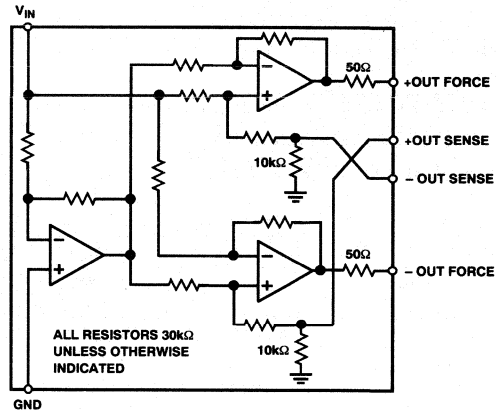
APPLICATIONS

- Audio Mix Consoles
- Distribution Amplifiers
- Graphic and Parametric Equalizers
- Dynamic Range Processors
- Digital Effects Processors
- Telecommunications Systems
- Industrial Instrumentation
- Hi-Fi Equipment

GENERAL DESCRIPTION

The SSM-2142 is an integrated differential-output buffer amplifier that converts a single-ended input signal to a balanced output signal pair with high output drive. By utilizing low noise thermally matched thin film resistors and high slew rate amplifiers, the SSM-2142 helps maintain the sonic quality of audio systems by eliminating power line hum, RF interference, voltage drops, and other externally generated noise commonly encountered with long audio cable runs. Excellent rejection of common-mode noise and offset errors is achieved by laser trimming of the onboard resistors, assuring high gain accuracy. The carefully designed output stage of the SSM-2142 is capable of driving difficult loads, yielding low-distortion performance despite extremely long cables or loads as low as 600 Ω, and is stable over a wide range of operating conditions.

FUNCTIONAL BLOCK DIAGRAM



Based on a cross-coupled, electronically balanced topology, the SSM-2142 mimics the performance of fully balanced transformer-based solutions for line driving. However, the SSM-2142 maintains lower distortion and occupies much less board space than transformers while achieving comparable common-mode rejection performance with reduced parts count.

The SSM-2142 in tandem with the SSM-2141 differential receiver establishes a complete, reliable solution for driving and receiving audio signals over long cables. The SSM-2141 features an Input Common-Mode Rejection Ratio of 100 dB at 60 Hz. Specifications demonstrating the performance of this typical system are included in the data sheet.

SSM-2142—SPECIFICATIONS

(V_S = ±18 V, −40°C ≤ T_A ≤ +85°C, operating in differential mode unless indicated otherwise. Typical characteristics apply to operation at T_A = +25°C.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT IMPEDANCE	Z_{IN}			10		kΩ
INPUT CURRENT	I_{IN}	V_{IN} = ±7.071 V		±750	±900	μA
GAIN, DIFFERENTIAL			5.8	5.98		dB
GAIN, SINGLE-ENDED		Single-Ended Mode	5.7	5.94		dB
GAIN ERROR, DIFFERENTIAL		R_L = 600 Ω		0.7	2	%
POWER SUPPLY REJECTION RATIO STATIC	PSRR	V_S = ±13 V to ±18 V	60	80		dB
OUTPUT COMMON-MODE REJECTION	OCMR	See Test Circuit; f = 1 kHz	−38	−45		dB
OUTPUT SIGNAL BALANCE RATIO	SBR	See Test Circuit; f = 1 kHz	−35	−40		dB
TOTAL HARMONIC DISTORTION Plus Noise	THD+N	20 Hz to 20 kHz, V_O = 10 V rms, R_L = 600 Ω		0.006		%
SIGNAL-TO-NOISE RATIO	SNR	V_{IN} = 0 V		−93.4		dBu
HEADROOM	HR	CLIP Level = 10.5 V rms		+93.4		dBu
SLEW RATE	SR			15		V/μs
OUTPUT COMMON-MODE VOLTAGE OFFSET[1]	V_{OOS}	R_L = 600 Ω	−250	25	250	mV
DIFFERENTIAL OUTPUT VOLTAGE OFFSET	V_{OOD}	R_L = 600 Ω	−50	15	50	mV
DIFFERENTIAL OUTPUT VOLTAGE SWING		V_{IN} = ±7.071 V	±13.8	±14.14		V
OUTPUT IMPEDANCE	Z_O		45	50	55	Ω
SUPPLY CURRENT	I_{SY}	Unloaded, V_{IN} = 0 V		5.5	7.0	mA
OUTPUT CURRENT, SHORT CIRCUIT	I_{SC}		60	70		mA

NOTE

[1]Output common-mode offset voltage can be removed by inserting dc blocking capacitors in the sense lines. See the Applications Information.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±18 V
Storage Temperature . . . . . −60°C to +150°C
Lead Temperature (Soldering, 60 sec) . . . . . +300°C
Junction Temperature . . . . . +150°C
Operating Temperature Range . . . . . −40°C to +85°C
Output Short Circuit Duration (Both Outputs) . . . . . Indefinite

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

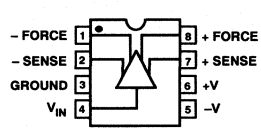
ORDERING GUIDE

Model	Operating Temperature Range	Package Option
SSM2142P	−40°C to +85°C	Plastic DIP
SSM2142Z	−40°C to +85°C	Cerdip
SSM2142S*	−40°C to +85°C	SOIC

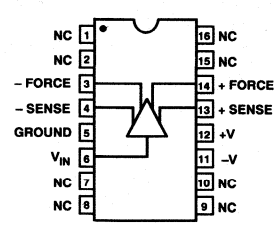
*For availability of SOIC package, contact your local sales office.

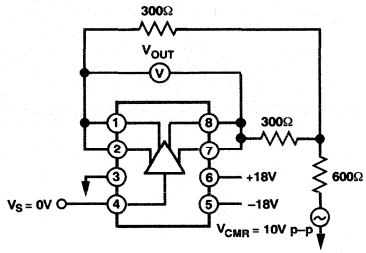
PIN CONNECTIONS

8-Pin Plastic DIP (P Suffix) 8-Pin Cerdip (Z Suffix)



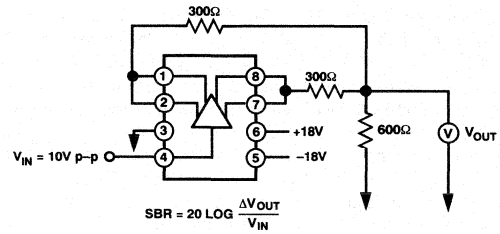
16-Pin SOIC (S Suffix)





$$OCMR = 20 \log \frac{\Delta V_{OUT}}{V_{CMR}}$$

Figure 1. Output CMR Test Circuit



$$SBR = 20 \log \frac{\Delta V_{OUT}}{V_{IN}}$$

Figure 2. Signal Balance Ratio (BBC Method) Test Circuit

4

Typical Performance Characteristics

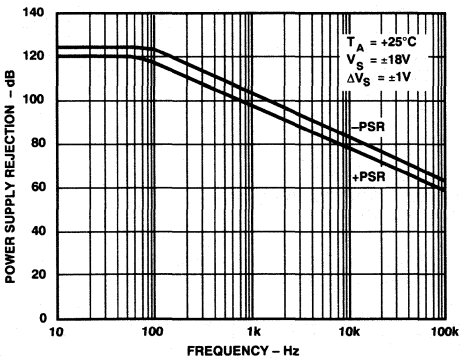


Figure 3. Power Supply Rejection vs. Frequency

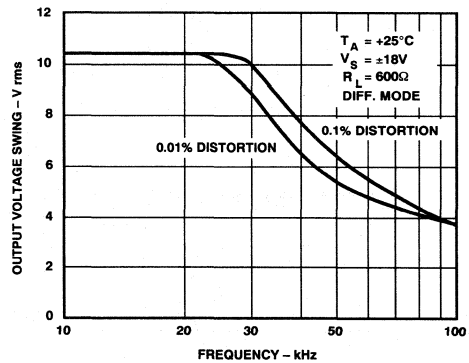


Figure 4. Maximum Output Voltage Swing vs. Frequency

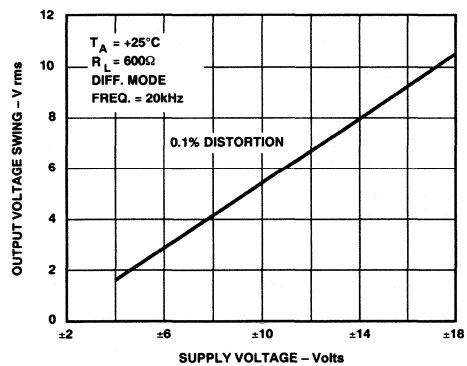


Figure 5. Output Voltage Swing vs. Supply Voltage

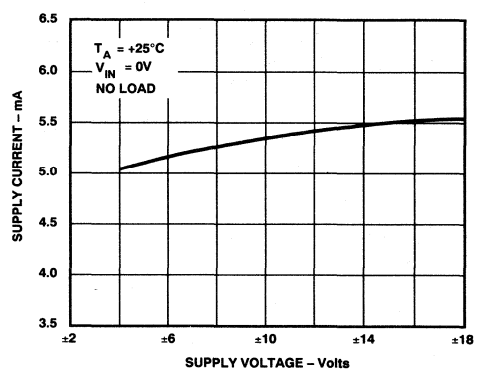
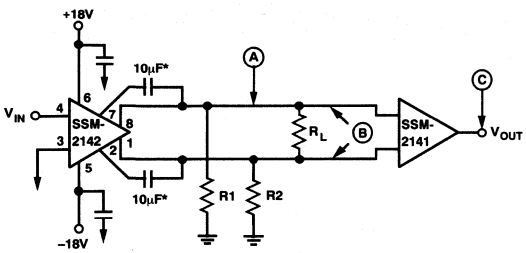


Figure 6. Supply Current vs. Supply Voltage

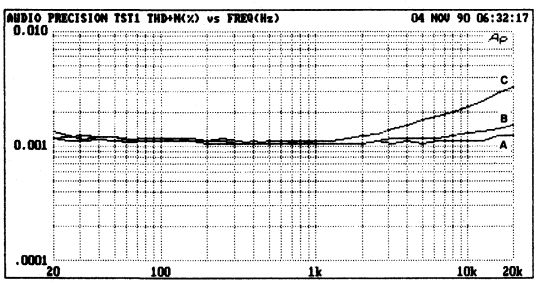
THD PERFORMANCE

The following data, taken from the THD test circuit on an Audio Precision System One using the internal 80 kHz noise filter, demonstrates the typical performance of a balanced-pair system based on the SSM-2142/SSM-2141 chip set. Both differential and single-ended modes of operation are shown, under a number of output load conditions which simulate various application situations. Note also that there is no adverse effect on system performance when using the optional series feedback capacitors, which reject dc cable offsets in order to maintain optimal ac noise rejection. The large signal transient response of the system to a 100 kHz square wave input is also shown, demonstrating the stability of the SSM-2142 under load.



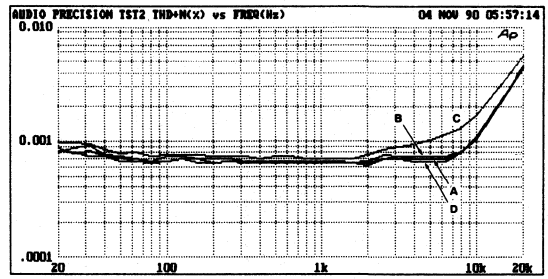
*USED ONLY IN THD PLOTS AS NOTED.
ALL CABLE MEASUREMENTS USE BELDEN 8451 CABLE.

Figure 7. THD Test Circuit



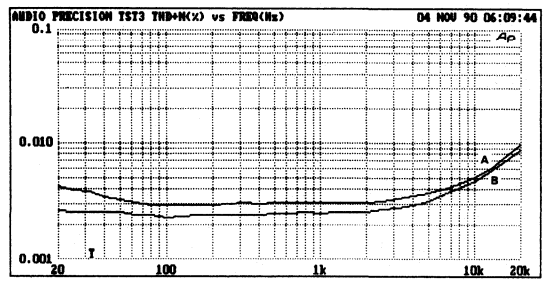
V_O = 10 V rms, NO CABLE
A: R1 = R2 = R_L = ∞
B: R1 = R2 = 600 Ω, R_L = ∞
C: R1 = R2 = ∞, R_L = 600 Ω

Figure 8. THD+N vs. Frequency at Point B (Differential Mode)



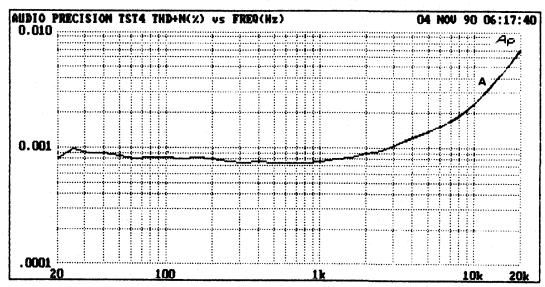
V_O = 10 V rms, WITH 500 FEET CABLE
A: R1 = R2 = R_L = ∞
B: R1 = R2 = 600 Ω, R_L = ∞
C: R1 = R2 = ∞, R_L = 600 Ω
D: R1 = R2 = R_L = ∞, WITH SERIES FEEDBACK CAPACITORS

Figure 9. THD+N vs. Frequency at Point B (Differential Mode)



V_O = 10 V rms, R2 = 0 Ω, R_L = ∞
A: R1 = 600 Ω, WITH 250 FEET CABLE
B: R1 = ∞, NO CABLE

Figure 10. THD+N vs. Frequency at Point A (Single Ended)



V_O = 10 V rms, NO CABLE
A: R1 = R2 = ∞, R_L = 600 Ω

Figure 11. THD+N vs. Frequency at Point C (SSM-2141 Output)

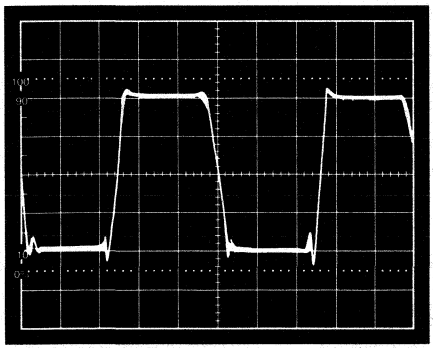


Figure 12. 100 kHz Square Wave Observed at Point B (Differential Mode). V_O = 10 V rms, R1 = R2 = ∞, R_L = 600 Ω

Figure 13. 100 kHz Square Wave at Point B (Differential Mode). V_O = 10 V rms, R1 = R2 = ∞, R_L = 600 Ω, with Series Feedback Capacitors

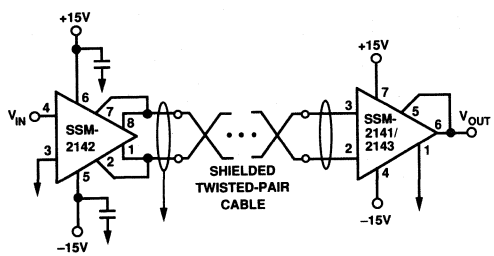


Figure 14. Typical Application of the SSM-2142 and SSM-2141

APPLICATIONS INFORMATION

The SSM-2142 is designed to provide excellent common-mode rejection, high output drive, and low signal distortion and noise in a balanced line-driving system. The differential output stage consists of twin cross-coupled unity-gain buffer amplifiers with on-chip 50 Ω series damping resistors. The impedances in the output buffer pair are precisely balanced by laser trimming during production. This results in the high gain accuracy needed to obtain good common-mode noise rejection, and excellent separation between the offset error voltages common to the cable pair and the desired differential input signal. As shown in the test circuit, it is suggested that a suitable balanced, high input-impedance differential amplifier such as the SSM-2141 be used at the receiving end for best system performance. The SSM-2141 receiver output is configured for a gain of one half following the 6 dB gain of the SSM-2142, in order to maintain an overall system gain of unity.

In applications encountering a large dc offset on the cable or those wishing to ensure optimal rejection performance by avoiding differential offset error sources, dc blocking capacitors may be employed at the sense outputs of the SSM-2142. As shown in the test circuit, these components should present as little impedance as possible to minimize low-frequency errors, such as 10 μF NP (or tantalum if the polarity of the offset is known).

4

SYSTEM GROUNDING CONSIDERATIONS

Due to ground currents, supply variations, and other factors, the ground potentials of the circuits at each end of a signal cable may not be exactly equal. The primary purpose of a balanced-pair line is to reject this voltage difference, commonly called "longitudinal error." A measure of the ability of the system to reject longitudinal error voltage is output common-mode rejection. In order to obtain the optimal OCMR and noise rejection performance available with the SSM-2142, the user should observe the following precautions:

1. The quality of the differential output is directly dependent upon the accuracy of the input voltage presented to the device. Input voltage errors developed across the impedance of the source must be avoided in order to maintain system performance. The input of the SSM-2142 should be driven directly by an operational amplifier or buffer offering low source impedance and low noise.
2. The ground input should be in close proximity to the single-ended input's source common. Ground offset errors encountered in the source circuitry also impair system performance.
3. Make sure that the SSM-2142 is adequately decoupled with 0.1 μF bypass capacitors located close to each supply pin.
4. Avoid the use of passive circuitry in series with the SSM-2142 outputs. Any reactive difference in the line pair will cause significant imbalances and affect the gain error of the device. Snubber networks or series load resistors are not required to maintain stability in SSM-2142-based systems, even when driving signals over extremely long cables.
5. Efforts should be made to maintain a physical balance in the arrangement of the signal pair wiring. Capacitive differences due to variations in routing or wire length may cause unequal noise pickup between the pair, which will degrade the system OCMR. Shielded twisted-pair cable is the preferred choice in all applications. The shield should not be utilized as a signal conductor. Grounding the shield at one end, near the output common, avoids ground loop currents flowing in the shield which increase noise coupling and longitudinal errors.

THE CABLE PAIR

The SSM-2142 is capable of driving a 10 V rms signal into 600 Ω and will remain stable despite cable capacitances of up to 0.16 μF in either balanced or single-ended configurations. Low-impedance shielded audio cable such as the standard Belden 8451 or similar is recommended, especially in applications traversing considerable distances. The user is cautioned that the so-called "audiophile" cables may incur four times the capacitance per unit length of the standard industrial-grade product. In situations of extreme load and/or distance, adding a second parallel cable allows the user to trade off half of the total line resistance against a doubling in capacitive load.

SINGLE-ENDED OPERATION

The SSM-2142 is designed to be compatible with existing balanced-pair interface systems. Just as in transformer-based circuits, identical but opposite currents are generated by the output pair which can be ground-referenced if desired and transmitted on a single wire. Single-ended operation requires that the unused side of the output pair be grounded to a solid return path in order to avoid voltage offset errors at the nearby input common. The signal quality obtained in these systems is directly dependent on the quality of the ground at each end of the wire. Also note that in single-ended operation the gain through the device is still 6 dB, and that the SSM-2142 incurs no significant degradation in signal distortion or output drive capability, although the noise rejection inherent in balanced-pair systems is lost.

POWER SUPPLY SEQUENCING

A problem occasionally encountered in the interface system environment involves irregular application of the supplies. The user is cautioned that applying power erratically can inadvertently bias parts of the circuit into a latchup condition. The small geometries of an integrated circuit are easily breached and damaged by short-risetime spikes on a supply line, which usually demonstrate considerable overshoot. The questionable practice of exchanging components or boards while under power can create such an undesirable sequence as well. Possible options which offer improved board-level device protection include: additional bypass capacitors, high-current reverse-biased steering diodes between both supplies and ground, various transient surge suppression devices, and safety grounding connectors.

Likewise, power should be applied to the device before the output is connected to "live" systems which may carry voltages of sufficient magnitude to turn on the output devices of the SSM-2142 and damage the device. In any case, of course, the user must always observe the absolute maximum ratings shown in the specifications.

ANALOG DEVICES

−6 dB Differential Line Receiver

SSM-2143

FEATURES

High Common-Mode Rejection
- **DC: 90 dB typ**
- **60 Hz: 90 dB typ**
- **20 kHz: 85 dB typ**

Ultralow THD: 0.0006% typ @ 1 kHz
Fast Slew Rate: 10 V/μs typ
Wide Bandwidth: 7 MHz typ (G = 1/2)
Two Gain Levels Available: G = 1/2 or 2
Low Cost

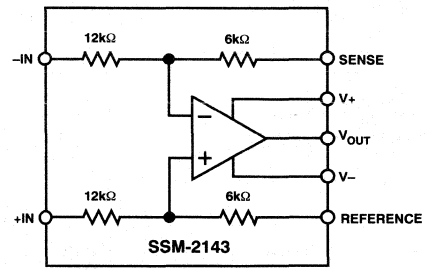
GENERAL DESCRIPTION

The SSM-2143 is an integrated differential amplifier intended to receive balanced line inputs in audio applications requiring a high level of immunity from common-mode noise. The device provides a typical 90 dB of common-mode rejection (CMR), which is achieved by laser trimming of resistances to better than 0.005%.

Additional features of the device include a slew rate of 10 V/μs and wide bandwidth. Total harmonic distortion (THD) is less than 0.004% over the full audio band, even while driving low impedance loads. The SSM-2143 input stage is designed to handle input signals as large as +28 dBu at G = 1/2. Although primarily intended for G = 1/2 applications, a gain of 2 can be realized by reversing the +IN/−IN and SENSE/REFERENCE connections.

When configured for a gain of 1/2, the SSM-2143 and SSM-2142 Balanced Line Driver provide a fully integrated, unity gain solution to driving audio signals over long cable runs.

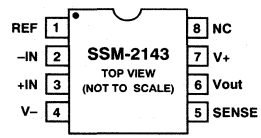
FUNCTIONAL BLOCK DIAGRAM



4

PIN CONNECTIONS

Epoxy Mini-DIP (P Suffix)
and
SOIC (S Suffix)



NC = NO CONNECT

SSM-2143—SPECIFICATIONS (V_S = ±15 V, −40°C ≤ T_A ≤ +85°C, G = 1/2, unless otherwise specified. Typical specifications apply at T_A = +25°C.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
AUDIO PERFORMANCE						
Total Harmonic Distortion Plus Noise	THD+N	V_{IN} = 10 V rms, R_L = 10 kΩ, f = 1 kHz		0.0006		%
Signal-to-Noise Ratio	SNR	0 dBu = 0.775 V rms, 20 kHz BW, RTI		−107.3		dBu
Headroom	HR	Clip Point = 1% THD+N		+28.0		dBu
DYNAMIC RESPONSE						
Slew Rate	SR	R_L = 2 kΩ, C_L = 200 pF	6	10		V/μs
Small Signal Bandwidth	$BW_{-3\ dB}$	R_L = 2 kΩ, C_L = 200 pF				
		G = 1/2		7		MHz
		G = 2		3.5		MHz
INPUT						
Input Offset Voltage	V_{IOS}	V_{CM} = 0 V, RTI, G = 2	−1.2	0.05	+1.2	mV
Common-Mode Rejection	CMR	V_{CM} = ±10 V, RTO				
		f = dc	70	90		dB
		f = 60 Hz		90		dB
		f = 20 kHz		85		dB
		f = 400 kHz		60		dB
Power Supply Rejection	PSR	V_S = ±6 V to ±18 V	90	110		dB
Input Voltage Range	IVR	Common Mode		±15		V
		Differential		±28		V
OUTPUT						
Output Voltage Swing	V_O	R_L = 2 kΩ	±13	±14		V
Minimum Resistive Load Drive				2		kΩ
Maximum Capacitive Load Drive				300		pF
Short Circuit Current Limit	I_{SC}			+45, −20		mA
GAIN						
Gain Accuracy			−0.1	0.03	0.1	%
REFERENCE INPUT						
Input Resistance				18		kΩ
Voltage Range				±10		V
POWER SUPPLY						
Supply Voltage Range	V_S		±6		±18	V
Supply Current	I_{SY}	V_{CM} = 0 V, R_L = ∞		±2.7	±4.0	mA

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±18 V
Common-Mode Input Voltage . . . . . ±22 V
Differential Input Voltage . . . . . ±44 V
Output Short Circuit Duration . . . . . Continuous
Operating Temperature Range . . . . . −40°C to +85°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature (Tj) . . . . . +150°C
Lead Temperature (Soldering, 60 sec.) . . . . . +300°C
Thermal Resistance[1]
8-Pin Plastic DIP (P): θ_{JA} = 103, θ_{JC} = 43 . . . . . °C/W
8-Pin SOIC (S): θ_{JA} = 150, θ_{JC} = 43 . . . . . °C/W

ORDERING GUIDE

Model	Operating Temperature Range	Package
SSM-2143P	−40°C to +85°C	8-Pin Plastic DIP
SSM-2143S*	−40°C to +85°C	8-Pin SOIC

*Contact sales office for availability.

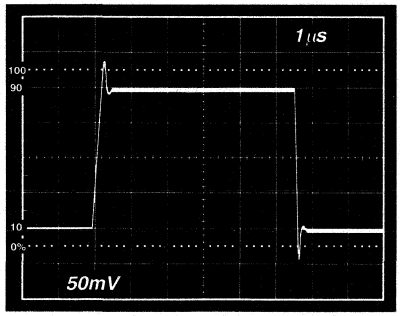


Figure 1. Small-Signal Transient Response (V_{IN} = ±200mV, G = 1/2, R_L = 2 kΩ,V_S = ±15 V, T_A = +25°C)

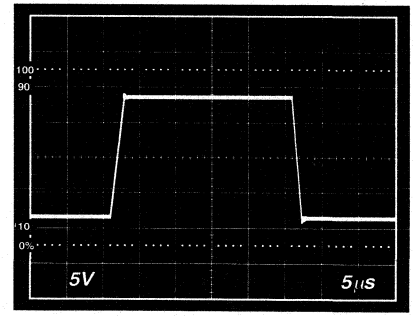


Figure 2. Large Signal Transient Response (V_{IN} = +24 dBu, G = 1/2, R_L = 2kΩ, V_S = ±15 V, T_A = +25°C)

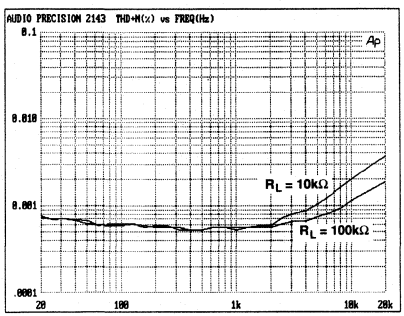


Figure 3. THD+N vs. Frequency (V_S = ±15 V, V_{IN} = 10 V rms, with 80 kHz Filter)

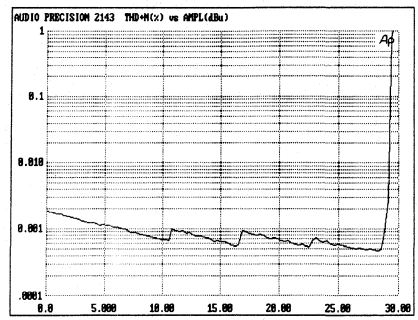


Figure 4. Headroom (V_S = ±15 V, R_L = 10 kΩ, with 80 kHz Filter)

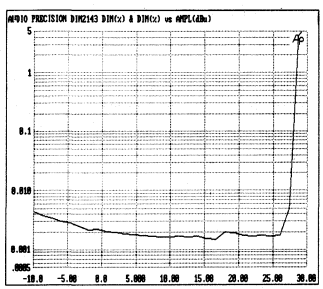


Figure 5. Dynamic Intermodulation Distortion, DIM-100 (V_S = ±15 V, R_L = 100 kΩ)

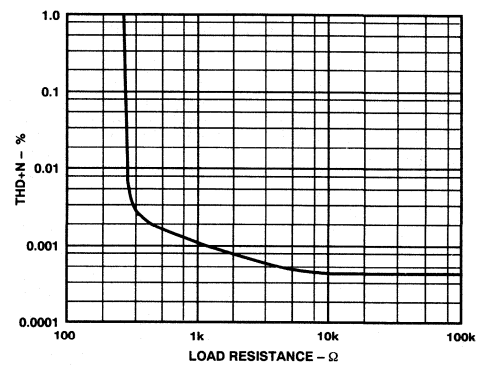


Figure 6. THD+N vs. Load (V_S = ±15 V, V_{IN} = 10 V rms, with 1 kHz Sine, 80 kHz Filter)

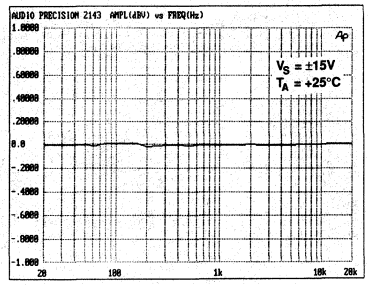


Figure 7. Closed-Loop Gain vs. Frequency, 20 Hz to 20 kHz (Gain of 1/2 Normalized to 0 dB)

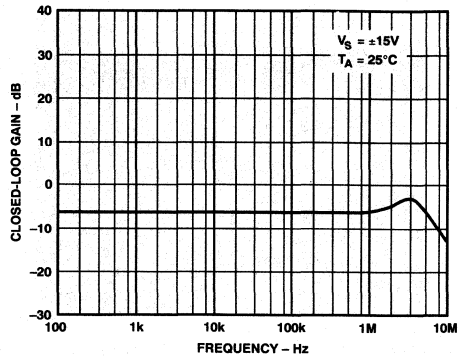


Figure 8. Closed-Loop Gain vs. Frequency, 100 Hz to 10 MHz

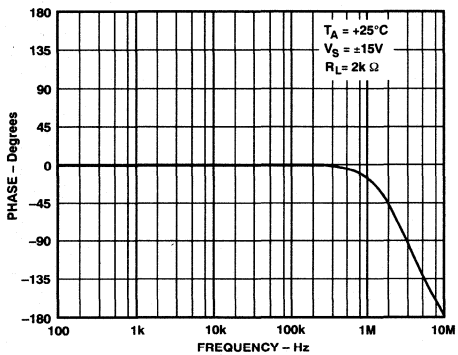


Figure 9. Closed-Loop Phase vs. Frequency

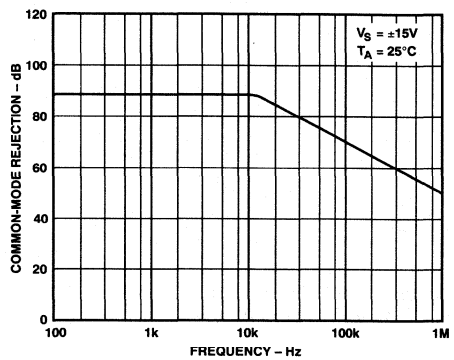


Figure 10. Common-Mode Rejection vs. Frequency

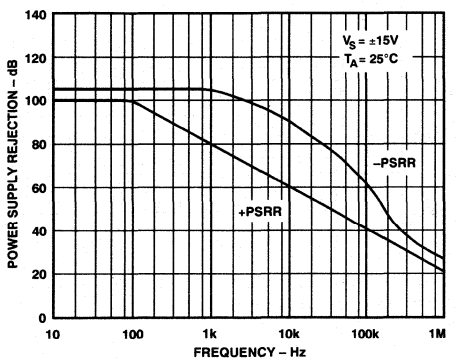


Figure 11. Power Supply Rejection vs. Frequency

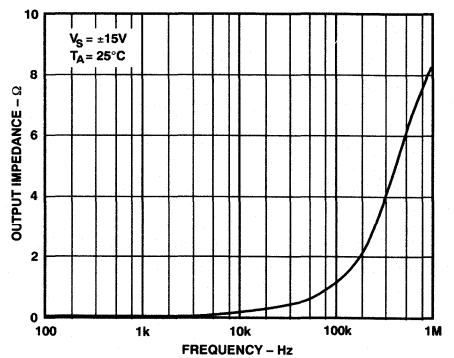


Figure 12. Closed-Loop Output Impedance vs. Frequency

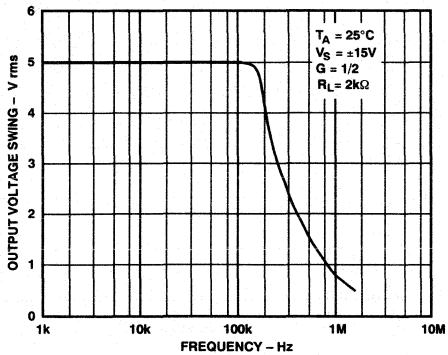


Figure 13. Output Voltage Swing vs. Frequency

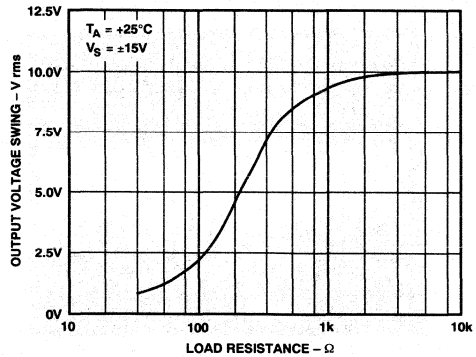


Figure 14. Output Voltage Swing vs. Load Resistance

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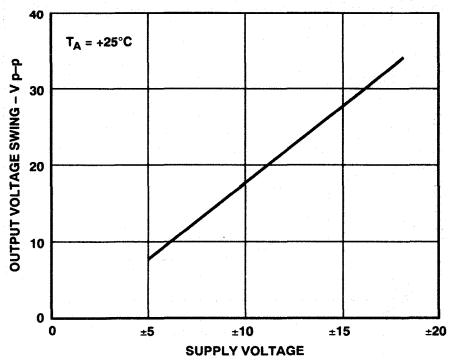

Figure 15. Output Voltage Swing vs. Supply Voltage

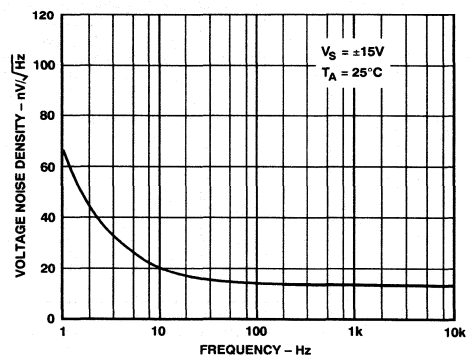

Figure 16. Voltage Noise Density vs. Frequency

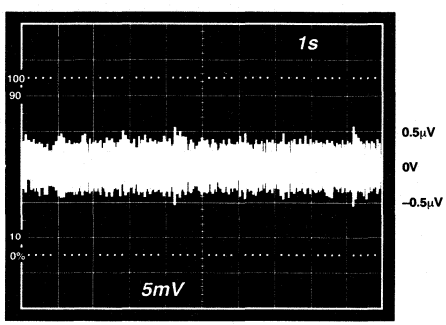

*Figure 17. Low Frequency Voltage Noise from 0.1 Hz to 10 Hz**

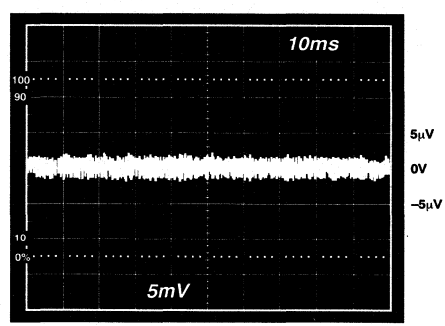

*Figure 18. Voltage Noise from 0 kHz to 1 kHz**

*The photographs in Figure 17 through Figure 19 were taken at V_S = ±15 V and T_A = +25°C, using an external amplifier with a gain of 1000.

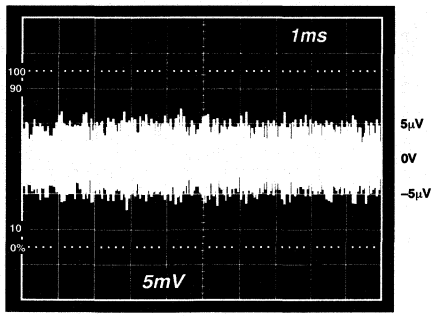

Figure 19. Voltage Noise from 0 kHz to 10 kHz*

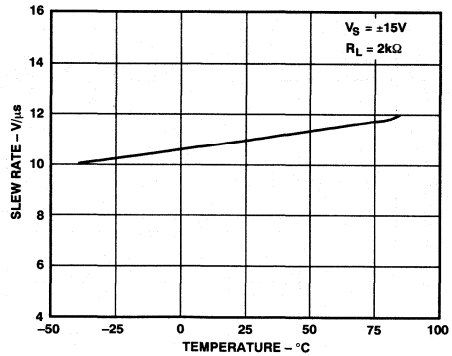

Figure 20. Slew Rate vs. Temperature

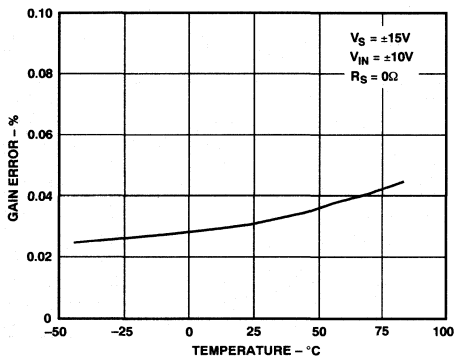

Figure 21. Gain Error vs. Temperature

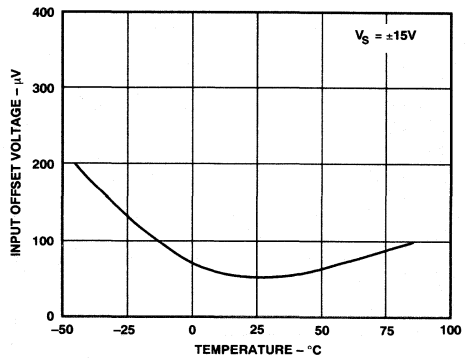

Figure 22. Input Offset Voltage vs. Temperature

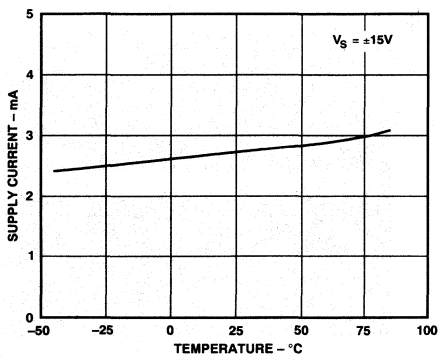

Figure 23. Supply Current vs. Temperature

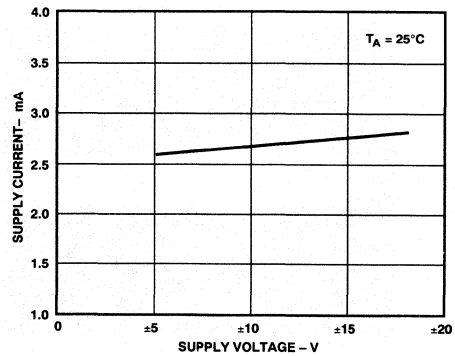

Figure 24. Supply Current vs. Supply Voltage

*The photographs in Figure 17 through Figure 19 were taken at V_S = ±15 V and T_A = +25°C, using an external amplifier with a gain of 1000.

APPLICATIONS INFORMATION

The SSM-2143 is designed as a balanced differential line receiver. It uses a high speed, low noise audio amplifier with four precision thin film resistors to maintain excellent common-mode rejection and ultralow THD. Figure 25 shows the basic differential receiver application where the SSM-2143 yields a gain of 1/2. The placement of the input and feedback resistors can be switched to achieve a gain of +2, as shown in Figure 26. For either circuit configuration, the SSM-2143 can also be used unbalanced by grounding one of the inputs. In applications requiring a gain of +1, use the SSM-2141.

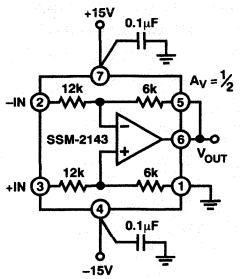

Figure 25. Standard Configuration for Gain of 1/2

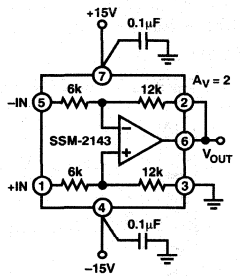

Figure 26. Reversing the Resistors Results in a Gain of 2.

CMRR

The internal thin film resistors are precisely trimmed to achieve a CMRR of 90 dB. Any imbalances introduced by the external circuitry will cause a significant reduction in the overall CMRR performance. For example, a 5 Ω source imbalance will result in a CMRR of 71 dB at dc. This is also true for any reactive source impedances that may affect the CMRR over the audio frequency range. These error sources need to be minimized to maintain the excellent CMRR.

To quantify the required accuracy of the thin film resistor matching, the source of CMRR error can be analyzed. A resistor mismatch can be modelled as shown in Figure 27. By assuming a tolerance on one of the 12 kΩ resistors of ΔR, the equation for the common-mode gain becomes:

$$\frac{V_{OUT}}{V_{IN}} = \frac{6k}{6k + 12k}\left(\frac{6k}{12k + \Delta R} + 1\right) - \frac{6k}{12k + \Delta R}$$

which reduces to:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1/3\ \Delta R}{12k + \Delta R}$$

This gain error leads to a common-mode rejection ratio of:

$$CMRR = \frac{|A_{DM}|}{|A_{CM}|} \cong \frac{18k}{\Delta R}$$

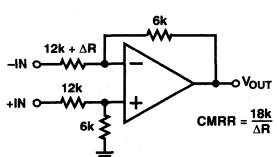

Figure 27. A Small Mismatch in Resistance Results in a Large Common-Mode Error.

Setting ΔR to 5 Ω results in the CMRR of 71 dB, as stated above. To achieve the SSM-2143's CMRR of 90 dB, the resistor mismatch can be at most 0.57 Ω. In other words, to build this circuit discretely, the resistors would have to be matched to better than 0.005%!

The following table shows typical resistor accuracies and the resulting CMRR for a differential amplifier.

% Mismatch	CMRR
5%	30 dB
1%	44 dB
0.1%	64 dB
0.005%	90 dB

DC OUTPUT LEVEL ADJUST

The reference node of the SSM-2143 is normally connected to ground. However, it can be used to null out any dc offsets in the system or to introduce a dc reference level other than ground. As shown in Figure 28, the reference node needs to be

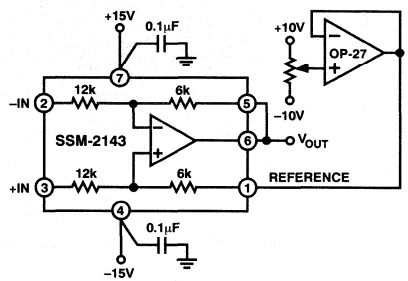

Figure 28. A Low Impedance Buffer Is Required to Adjust the Reference Voltage.

buffered with an op amp to maintain very low impedance to achieve high CMRR. The same reasoning as above applies such that the 6 kΩ resistor has to be matched to better than 0.005% or 0.3 Ω. The op amp maintains very low output impedance over the entire audio frequency range, as long as its bandwidth is well above 20 kHz. The reference input can be adjusted over a ±10 V range. The gain from the reference to the output is unity so the resulting dc output adjustment range is also ±10 V.

INPUT ERRORS

The main dc input offset error specified for the SSM-2143 is the Input Offset Voltage. The Input Bias Current and Input Offset Current are not specified as for a normal operational amplifier. Because the SSM-2143 has built-in resistors, any bias current related errors are converted into offset voltage errors. Thus, the offset voltage specification is a combination of the amplifier's offset voltage plus its offset current times the input impedance.

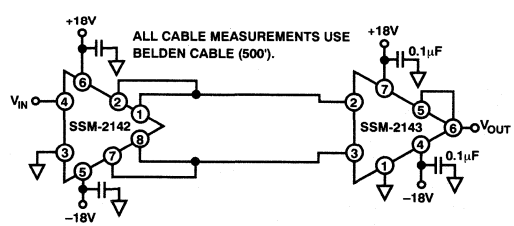

Figure 29. SSM-2142/SSM-2143 Balanced Line Driver/ Receiver System

LINE DRIVER/RECEIVER SYSTEM

The SSM-2143 and SSM-2142 provide a fully integrated line driver/receiver system. The SSM-2142 is a high performance balanced line driver IC that converts an unbalanced input into a balanced output signal. It can drive large capacitive loads on long cables making it ideal for transmitting balanced audio signals. When combined with an SSM-2143 on the receiving end of the cable, the system maintains high common-mode rejection and ultralow THD. The SSM-2142 is designed with a gain of +2 and the SSM-2143 with a gain of 1/2, providing an overall system gain of unity.

The following data demonstrates the typical performance of the two parts together, measured on an Audio Precision at the SSM-2143's output. This configuration was tested with 500 feet of cable between the ICs as well as no cable. The combination of the two parts results in excellent THD+N and SNR and a noise floor of typically −105 dB over a 20 Hz to 20 kHz bandwidth.

A comment on SSM-2142/SSM-2143 system headroom is necessary. Figure 31 shows a maximum signal handling of approximately ±22 dBu, but it must be kept in mind that this is measured between the SSM-2142's input and SSM-2143's output, which has been attenuated by one half. Normally, the system would be shown as actually used in a piece of equipment, whereby the SSM-2143 is at the input and SSM-2142 at the output. In this case, the system could handle differential signals in excess of +24 dBu at the input and output, which is consistent with headroom requirements of most professional audio equipment.

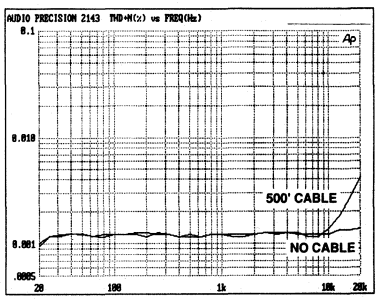

Figure 30. THD+N vs. Frequency of SSM-2142/SSM-2143 System (V_S = ±18 V, V_{IN} = 5 V rms, with 80 kHz Filter)

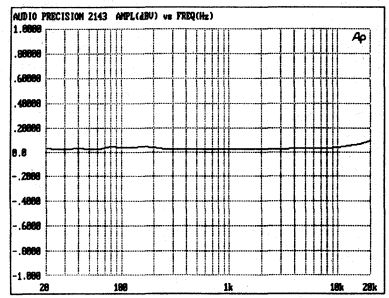

Figure 33. SSM-2142/SSM-2143 System Frequency Response (V_S = ±18 V, V_{IN} = 0 dBV, 500′ Cable)

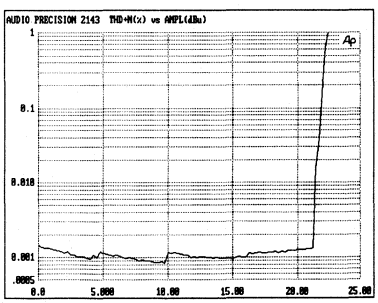

Figure 31. SSM-2142/SSM-2143 System Headroom—See Text—(V_S = ±18 V, R_L = 10 kΩ, 500′ Cable)

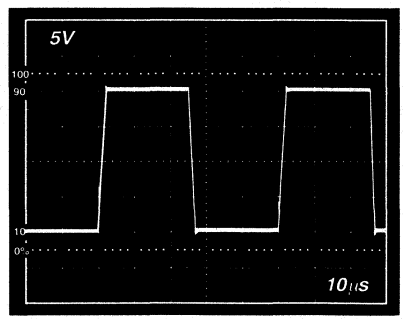

Figure 34. SSM-2142/SSM-2143 System Large Signal Pulse Response (V_S = ±18 V, R_L = 10 kΩ, No Cable)

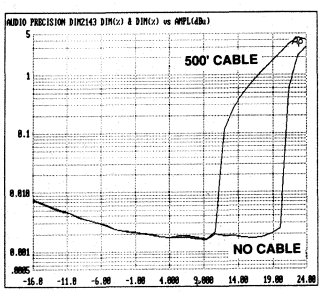

Figure 32. SSM-2142/SSM-2143 System DIM-100 Dynamic Intermodulation Distortion (V_S = ±18 V, R_L = 10 kΩ)

Isolation Amplifiers
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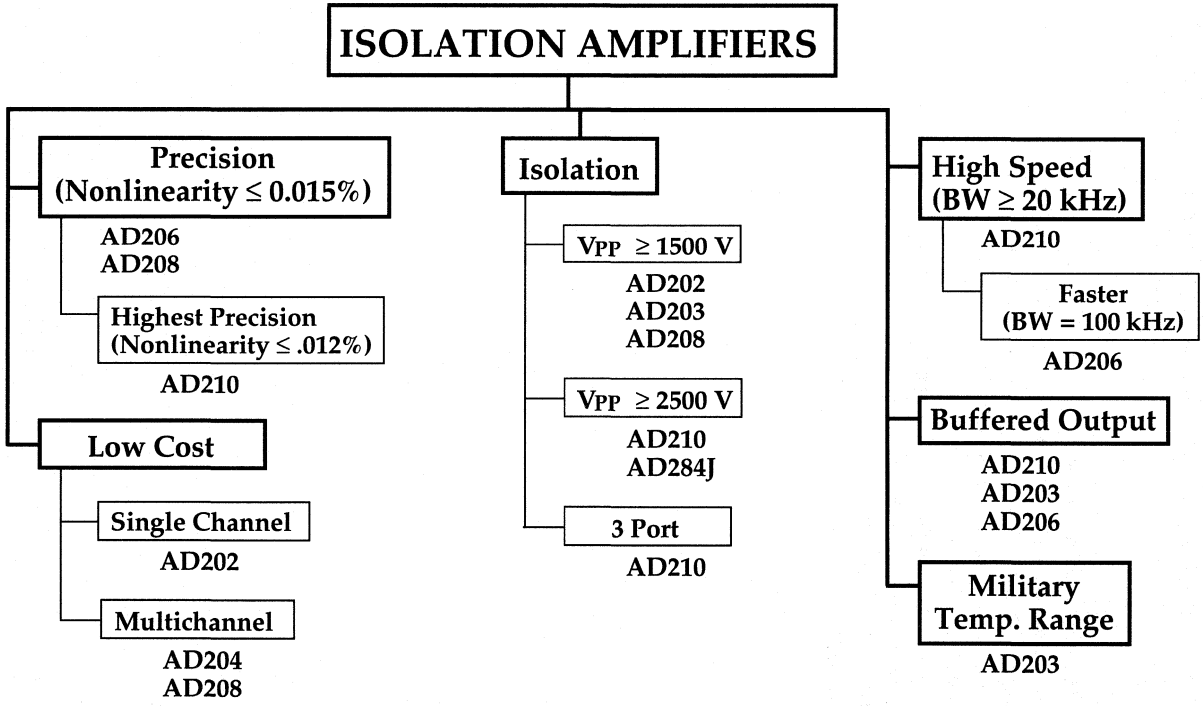
Selection Tree
Isolation Amplifiers



Selection Guide
Isolation Amplifiers

Model	Peak Volt Iso V pk	Gain Range V/V	Gain Nonlin % max	Freq Resp kHz	Package Options[1]	Temp Range[2]	Page	Comments
284J	2500	1–10	0.05	1	Module	C	5-63	Single Channel, Low Cost
286J	2500	1–100	0.05-0.2	1	Module	C	5-69	Multichannel, Low Cost
289	2500	1–100	0.012–0.05	20	Module	C	5-75	Precision, Wide Bandwidth, Synchronized
290A	1500	1–100	0.1–0.25	2.5	Module	I	5-81	Single Channel, General Purpose
292A	1500	1–100	0.1–0.25	2.5	Module	I	5-81	Multichannel, General Purpose
AD202	**1000–2000**	**1–100**	**0.025–0.05**	**2**	**2, 11**	**I**	**5-7**	**Lowest Cost, Small Size, Single Channel, −40°C to +85°C**
AD203	**2000**	**1–100**	**0.025**	**10**	**2**	**M**	**5-19**	**Rugged, Military Temperature Range, Wide Bandwidth**
AD204	**1000–2000**	**1–100**	**0.025-0.05**	**5**	**2, 11**	**I**	**5-7**	**Lowest Cost, Small Size, Multichannel, −40°C to +85°C**
AD206	**2000**	**1–10**	**0.015–0.03**	**100 kHz**	**11**	**I**	**5-31**	**100 kHz Bandwidth, Low Distortion Isolation Amplifier**
AD208	**1000–2000**	**1–1000**	**0.015–0.03**	**0.4–4 kHz**	**11**	**I**	**5-41**	**Precision, Low Cost, Single Channel, mV Input**
AD210	**3500**	**1–100**	**0.012–0.025**	**20**	**2**	**I**	**5-55**	**Precision, 3-Port Isolation, Wide Bandwidth**
281					Module	C	5-69	External Oscillator for 286J and 292A Isolation Amplifiers

[1]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack, 11 = Single-in-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92; 17 = Plastic Pin Grid Array.
[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.
Boldface Type: Product recommended for new design.
*New product.

Orientation
Isolation Amplifiers

The *isolation amplifier* (or isolator) has an input circuit that is galvanically isolated from the power supply and the output circuit. In the basic *two-port* form, the output and power circuits are not isolated from one another; in *three-port* isolators (see the figure), the input circuits, output circuits, and power source are all isolated from one another. In some 3-port isolators, the power for the output stage must be furnished from the signal's destination; however, in the device shown in Figure 1, all internal power is furnished by its own power source; in addition, a modicum of auxiliary power is available to power external input *and output* circuitry.

Isolators are intended for applications requiring safe, accurate measurement of voltage or current signals in the presence of high common-mode voltage (to thousands of volts) with high CMR, line-receiving of signals transmitted at high impedance in noisy environments, and for safety in general-purpose measurements where dc and line-frequency leakage must be maintained at levels well below certain mandated minima.* Principal applications are in electrical environments of the kind associated with medical equipment, conventional and nuclear power plants, automatic test equipment and industrial process-control systems.

Analog Devices Isolators described in this section (and in the *Signal Conditioner* section) use transformer coupled high-frequency carrier techniques for the transmission of power to and signals from the input (and in some cases the *output*) circuit.

CHOOSING AN ISOLATOR

The choice of isolator depends on the desired *functional characteristics* and the required *specifications*. Functional characteristics include such considerations as number of channels in the system, range of output common-mode (output to power supply), nature of the front-end amplifier (amplification only or general op-amp functioning) and the availability of isolated power for additional external front-end (or back-end) circuitry. Key specifications include performance specs and "absolute max/min" mandated safety specifications. Definitions of specifications follow this section. In addition to the products listed here, which are recommended for new designs, a number of older products are still available; data sheets are available upon request. In addition to the useful applications information on the data sheets published here, an applications guide,[1] available upon request, provides information useful to the circuit designer.

The devices described in this section are all voltage-output isolation amplifiers, useful in general-purpose circuit applications for instrumentation amplifiers or op amps where isolation is a necessity. In addition to these devices, there are a growing number of isolators available from Analog Devices that perform dedicated functions, for use where isolation is necessary or desirable. Some of their applications can be seen in the Signal Conditioner section of this book and the *Transducer Interfacing Handbook*.[2] Power Supplies and DC-DC Converters, usually transformer-coupled, also provide isolation.

***Examples of such requirements may be found in UL STD 544 and SWC. (Surge Withstand Capability) in IEEE Standard for Transient Voltage Protection 472-1974.**

[1]*Analog Devices Applications Guide to Isolation Amplifiers and Signal Conditioners.*

[2]Sheingold, D.H., ed, *Transducer Interfacing Handbook – A guide to analog signal conditioning*. Norwood, MA 02062 (P.O. Box 9106): Analog Devices, Inc., 1980, $14.50.

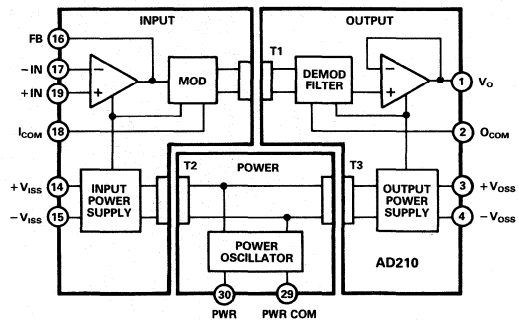


Figure 1. AD210 Block Diagram

Functional Characteristics: The figure shows the circuit architecture of a self-contained isolator, Model AD210. The various models differ, but their properties can be discussed in terms of the device shown. An isolator of this type requires power from a two-terminal dc supply. An internal oscillator converts the dc power to ac, which is transformer-coupled to the shielded input section, then converted to dc for the input stage and the auxiliary power output. The ac carrier is also modulated by the amplifier output, transformer-coupled to the output stage, demodulated by a phase-sensitive demodulator (using the carrier as the reference), filtered and buffered, using isolated dc power (also available for auxiliary circuitry) derived from the carrier.

The amplifier in this example is an uncommitted op amp, specified for programmable gains from 1 to 100V/V, as determined by its feedback circuitry. Since both input terminals are floating, the amplifier functions effectively as an instrumentation amplifier. Most of the other devices in this series require just a single external resistor to set the gain.

In the figure it can be seen that ac power is magnetically coupled from the oscillator to the output stage. This permits the output to operate at a dc common-mode potential with respect to power common. An isolator of this type is said to provide *three-port* isolation, because there are three isolated ports: input, power supply and output. Two-port devices are those in which there is a dc connection between the oscillator power supply and the output stage.

The AD210, as can be seen, is a completely self-contained device. There are applications for which a degree of "unbundling" can lead to economy and improved performance. For example, if there are many input channels to be isolated, economies can be realized by the use of a common oscillator. In addition, the common oscillator makes it possible to avoid the possibility of small errors due to beat frequencies developed by small amounts of crosstalk in older amplifier designs.

Several synchronized multichannel devices are available. Model 204 is essentially a 202 with a power converter instead of an oscillator. It requires a pair of leads for an oscillator input, which can be furnished by an AD246 clock.

SPECIFICATIONS

The illustration on the next page shows a typical specification block; the specifications of key interest are defined.

For an initial choice of data sheets to inspect for a given application, the Selection Guide permits comparison on the basis of these key characteristics: common-mode voltage, specified gain range and frequency response. The "Notes" column indicates which devices require external oscillators (for lower cost in many-channel applications) and identifies devices that are three-port isolated. Good starting points are: for high performance, the AD210; for lowest cost, the AD202 and AD204, depending on whether the application calls for few or many channels; for military temperature, the AD203; for maximum precision, the AD208; and for the widest bandwidth, the AD206.

SPECIFICATIONS (typical @ + 25°C, & V_S = +15V unless otherwise specified)

Model	AD210AN	AD210BN
GAIN		
Range	1V/V – 100V/V	*
Error	± 2% max	± 1% max
vs. Temperature (0 to + 70°C)	± 25ppm/°C max	*
(– 25°C to + 85°C)	± 50ppm/°C max	*
vs. Supply Voltage	± 0.002%/V	*
Nonlinearity[1]	± 0.025% max	± 0.012% max
Nonlinearity vs. Isolated Supply Load	± 0.002%/mA	*
INPUT VOLTAGE RATINGS		
Linear Differential Range	± 10V	*
Maximum Safe Differential Input	± 15V	*
Max. CMV Input-to-Output		
ac, 60Hz, Continuous	2500V rms	*
dc, Continuous	± 3500V peak	*
Common-Mode Rejection		
60Hz, G = 100V/V		
$R_S \leq 500\Omega$ Impedance Imbalance	120dB	*
Leakage Current Input-to-Output		
@ 240Vrms, 60Hz	2μA rms max	*
INPUT IMPEDANCE		
Differential	$10^{12}\Omega$	*
Common Mode	$5G\Omega \| 5pF$	*
INPUT BIAS CURRENT		
Initial, @ + 25°C	30pA typ (400pA max)	*
vs. Temperature (0 to + 70°C)	10nA max	*
(– 25°C to + 85°C)	30nA max	*
INPUT DIFFERENCE CURRENT		
Initial, @ + 25°C	5pA typ (200pA max)	*
vs. Temperature (0 to + 70°C)	2nA max	*
(– 25°C to + 85°C)	10nA max	*
INPUT NOISE		
Voltage (1kHz)	$18nV/\sqrt{Hz}$	*
(10Hz to 10kHz)	4μV rms	*
Current (1kHz)	$0.01pA/\sqrt{Hz}$	*
FREQUENCY RESPONSE		
Bandwidth (– 3dB)		
G = 1V/V	20kHz	*
G = 100V/V	15kHz	*
Settling Time (± 10mV, 20V Step)		
G = 1V/V	150μs	*
G = 100V/V	500μs	*
Slew Rate (G = 1V/V)	1V/μs	*
OFFSET VOLTAGE (RTI)[2]		
Initial, @ + 25°C	(± 15 ± 45/G)mV max	(± 5 ± 15/G)mV max
vs. Temperature (0 to + 70°C)	(± 10 ± 30/G)μV/°C	*
(– 25°C to + 85°C)	(± 10 ± 50/G)μV/°C	*
RATED OUTPUT[3]		
Voltage, 2kΩ Load	± 10V min	*
Impedance	1Ω max	*
Ripple, (Bandwidth = 100kHz)	10mV p-p max	*
ISOLATED POWER OUTPUTS[4]		
Voltage, No Load	± 15V	*
Accuracy	± 10%	*
Current	± 5mA	*
Regulation, No Load to Full Load	See Text	*
Ripple	See Text	*
POWER SUPPLY		
Voltage, Rated Performance	+ 15V dc ± 5%	*
Voltage, Operating	+ 15V dc ± 10%	*
Current, Quiescent	50mA	*
Current, Full Load – Full Signal	80mA	*
TEMPERATURE RANGE		
Rated Performance	– 25°C to + 85°C	*
Operating	– 40°C to + 85°C	*
Storage	– 40°C to + 85°C	*
PACKAGE DIMENSIONS		
Inches	1.00 × 2.10 × 0.350	*
Millimeters	25.4 × 53.3 × 8.9	*

NOTES
*Specifications same as AD210AN.
[1]Nonlinearity is specified as a % deviation from a best straight line.
[2]RTI – Referred to Input
[3]A reduced signal swing is recommended when both $\pm V_{ISS}$ and $\pm V_{OSS}$ supplies are fully loaded, due to supply voltage reduction.
[4]See text for detailed information.
Specifications subject to change without notice.

NONLINEARITY – This is the peak deviation from a best straight line, expressed as a % of peak-to-peak output. Should be considered when signal fidelity is of prime importance.

MAX SAFE DIFFERENTIAL INPUT – Max voltage that can be safely applied across input terminals. Important to consider for fail-safe designs in the presence of high voltages.

INPUT NOISE – Total noise, referred to the input. Facilitates comparison with expected signal input levels.

ISOLATED POWER OUTPUTS – Dual supply voltages, completely isolated from the input power supply terminals, provide the capability to excite floating input and output signal conditioners, front-end amplifiers, as well as remote transducers.

CMV, INPUTS TO OUTPUTS – Voltage that may be safely applied to *both* inputs with respect to outputs or power common. Necessary consideration in applications with high CMV input or when high voltage transients may occur at the input.

CMR, INPUTS TO OUTPUTS – Indicates ability to reject common-mode voltages between inputs and outputs. Important when processing small signals riding on high common-mode voltages.

LEAKAGE CURRENT – Maximum input leakage current when power-line voltage is impressed on inputs. Vital consideration for patient safety in medical applications.

OFFSET VOLTAGE REFERRED TO INPUT – Total input drift is composed of two sources (input and output stage drifts) and is gain (G) dependent. Referring offsets to the input allows them to be compared to signal levels.

Figure 2. Typical Isolator Specifications

ANALOG DEVICES

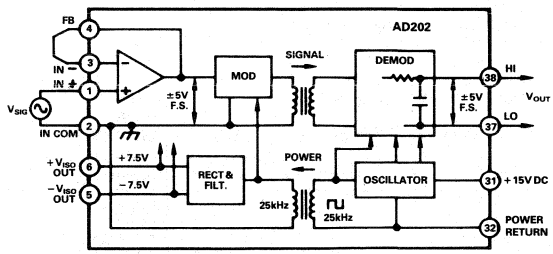
Low Cost, Miniature Isolation Amplifiers

AD202/AD204

FEATURES
Small Size: 4 Channels/Inch
Low Power: 35mW (AD204)
High Accuracy: ±0.025% max Nonlinearity (K Grade)
High CMR: 130dB (Gain = 100V/V)
Wide Bandwidth: 5kHz Full-Power (AD204)
High CMV Isolation: ±2000V pk Continuous (K Grade) (Signal and Power)
Isolated Power Outputs
Uncommitted Input Amplifier

APPLICATIONS
Multichannel Data Acquisition
Current Shunt Measurements
Motor Controls
Process Signal Isolation
High Voltage Instrumentation Amplifier

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD202 and AD204 are general purpose, two-port, transformer-coupled isolation amplifiers that may be used in a broad range of applications where input signals must be measured, processed and/or transmitted without a galvanic connection. These industry standard isolation amplifiers offer a complete isolation function, with both signal and power isolation provided for in a single compact plastic SIP or DIP style package. The primary distinction between the AD202 and the AD204 is that the AD202 is powered directly from a +15V dc supply while the AD204 is powered by an externally supplied clock, such as the recommended AD246 Clock Driver.

The AD202 and AD204 provide total galvanic isolation between the input and output stages of the isolation amplifier through the use of internal transformer-coupling. The functionally complete AD202 and AD204 eliminate the need for an external, user-supplied dc/dc converter. This permits the designer to minimize the necessary circuit overhead and consequently reduce the overall design and component costs.

The design of the AD202 and AD204 emphasizes maximum flexibility and ease of use, including the availability of an uncommitted op amp on the input stage. They feature a bipolar ±5V output range, an adjustable gain range of from 1 to 100V/V, ±0.025% max nonlinearity (K grade), 130dB of CMR and the AD204 consumes a low 35mW of power.

PRODUCT HIGHLIGHTS

The AD202 and AD204 are full-featured isolators offering numerous benefits to the user:

Small Size: The AD202 and AD204 are available in SIP and DIP form packages. The SIP package is just 0.25″ wide, giving the user a channel density of four channels per inch. The isolation barrier is positioned to maximize input to output spacing. For applications requiring a low profile, the DIP package provides a height of just 0.350″.

High Accuracy: With a maximum nonlinearity of ±0.025% for the AD202K/AD204K (±0.05% for the AD202J/AD204J) and low drift over temperature, the AD202 and AD204 provide high isolation without loss of signal integrity.

Low Power: Power consumption of 35mW (AD204) and 75mW (AD202) over the full signal range makes these isolators ideal for use in applications with large channel counts or tight power budgets.

Wide Bandwidth: The AD204's full-power bandwidth of 5kHz makes it useful for wideband signals. It is also effective in applications like control loops, where limited bandwidth could result in instability.

Excellent Common-Mode Performance: The AD202K/AD204K provide ±2000V pk continuous common-mode isolation, while the AD202J/AD204J provide ±1000V pk continuous common-mode isolation. All models have a total common-mode input capacitance of less than 5pF inclusive of power isolation. This results in CMR ranging from 130dB at a gain of 100 to 104dB (minimum at unity gain) and very low leakage current (2μA maximum).

Flexible Input: An uncommitted op amp is provided at the input of all models. This provides buffering and gain as required, and facilitates many alternative input functions including filtering, summing, high-voltage ranges, and current (transimpedance) input.

Isolated Power: The AD204 can supply isolated power of ±7.5V at 2mA. This is sufficient to operate a low-drift input preamp, provide excitation to a semiconductor strain gage, or to power any of a wide range of user-supplied ancillary circuits. The AD202 can supply ±7.5V at 0.4mA which is sufficient to operate adjustment networks or low-power references and op amps, or to provide an open-input alarm.

5

AD202/AD204—SPECIFICATIONS (typical @ +25°C and V_S = +15 V unless otherwise noted)

Model	AD204J	AD204K	AD202J	AD202K
GAIN				
Range	1V/V-100V/V	*	*	*
Error	±0.5% typ (±4% max)	*	*	*
vs. Temperature	±20ppm/°C typ (±45ppm/°C max)	*	*	*
vs. Time	±50ppm/1000 Hours	*	*	*
vs. Supply Voltage	±0.01%/V	±0.01%/V	±0.01%/V	±0.01%/V
Nonlinearity (G = 1V/V)[1]	±0.05% max	±0.025% max	±0.05% max	±0.025% max
Nonlinearity vs. Isolated Supply Load	±0.0015%/mA	*	*	*
INPUT VOLTAGE RATINGS				
Input Voltage Range	±5V	*	*	*
Max Isolation Voltage (Input to Output)				
AC, 60Hz, Continuous	750V rms	1500V rms	750V rms	1500V rms
Continuous (AC and DC)	±1000V peak	±2000V peak	±1000V peak	±2000V peak
Isolation-Mode Rejection Ratio (IMRR) @ 60Hz				
$R_S \leq 100\Omega$ (HI & LO Inputs) G = 1V/V	110dB	110dB	105dB	105dB
G = 100V/V	130dB	*	*	*
$R_S \leq 1k\Omega$ (Input HI, LO, or Both) G = 1V/V	104dB min	104dB min	100dB min	100dB min
G = 100V/V	110dB min	*	*	*
Leakage Current Input to Output @ 240V rms, 60Hz	2μA rms max	*	*	*
INPUT IMPEDANCE				
Differential (G = 1V/V)	$10^{12}\Omega$	*	*	*
Common Mode	$2G\Omega \| 4.5pF$	*	*	*
INPUT BIAS CURRENT				
Initial, @ +25°C	±30pA	*	*	*
vs. Temperature (0 to +70°C)	±10nA	*	*	*
INPUT DIFFERENCE CURRENT				
Initial, @ +25°C	±5pA	*	*	*
vs. Temperature (0 to +70°C)	±2nA	*	*	*
INPUT NOISE				
Voltage, 0.1 to 100Hz	4μV p-p	*	*	*
f>200Hz	$50nV/\sqrt{Hz}$	*	*	*
FREQUENCY RESPONSE				
Bandwidth ($V_O \leq 10V$ p-p, G = 1-50V/V)	5kHz	5kHz	2kHz	2kHz
Settling Time, to ±10mV (10V Step)	1ms	*	*	*
OFFSET VOLTAGE (RTI)				
Initial, @ +25°C Adjustable to Zero	(±15 ±15/G)mV max	(±5 ±5/G)mV max	(±15 ±15/G)mV max	(±5 ±5/G)mV max
vs. Temperature (0 to +70°C)	$\left(\pm 10 \pm \frac{10}{G}\right)\mu V/°C$	*	*	*
RATED OUTPUT				
Voltage (Out HI to Out LO)	±5V	*	*	*
Voltage at Out HI or Out LO (Ref. Pin 32)	±6.5V	*	*	*
Output Resistance	3kΩ	3kΩ	7kΩ	7kΩ
Output Ripple, 100kHz Bandwidth	10mV pk-pk	*	*	*
5kHz Bandwidth	0.5mV rms	*	*	*
ISOLATED POWER OUTPUT[2]				
Voltage, No Load	±7.5V	*	*	*
Accuracy	±10%	*	*	*
Current	2mA (Either Output)[3]	2mA (Either Output)[3]	400μA Total	400μA Total
Regulation, No Load to Full Load	5%	*	*	*
Ripple	100mV pk-pk	*	*	*
OSCILLATOR DRIVE INPUT				
Input Voltage	15V pk-pk nominal	15V pk-pk nominal	N/A	N/A
Input Frequency	25kHz nominal	25kHz nominal	N/A	N/A
POWER SUPPLY (AD202 Only)				
Voltage, Rated Performance	N/A	N/A	+15V ±5%	+15V ±5%
Voltage, Operating	N/A	N/A	+15V ±10%	+15V ±10%
Current, No Load (V_S = +15V)	N/A	N/A	5mA	5mA
TEMPERATURE RANGE				
Rated Performance	0 to +70°C	*	*	*
Operating	−40°C to +85°C	*	*	*
Storage	−40°C to +85°C	*	*	*
PACKAGE DIMENSIONS[4]				
SIP Package (Y)	2.08″ × 0.250″ × 0.625″	*	*	*
DIP Package (N)	2.10″ × 0.700″ × 0.350″	*	*	*

NOTES
*Specifications same as AD204J.
[1]Nonlinearity is specified as a % deviation from a best straight line.
[2]1.0μF min decoupling required (see text).
[3]3mA with one supply loaded.
[4]Width is 0.25″ typ, 0.26″ max.
Specifications subject to change without notice.

PIN DESIGNATIONS

AD202/AD204 SIP PACKAGE

PIN	FUNCTION
1	+INPUT
2	INPUT/V_{ISO} COMMON
3	−INPUT
4	INPUT FEEDBACK
5	−V_{ISO} OUTPUT
6	+V_{ISO} OUTPUT
31	+15V POWER IN (AD202 ONLY)
32	CLOCK/POWER COMMON
33	CLOCK INPUT (AD204 ONLY)
37	OUTPUT LO
38	OUTPUT HI

AD202/AD204 DIP PACKAGE

PIN	FUNCTION
1	+INPUT
2	INPUT/V_{ISO} COMMON
3	−INPUT
18	OUTPUT LO
19	OUTPUT HI
20	+15V POWER IN (AD202 ONLY)
21	CLOCK INPUT (AD204 ONLY)
22	CLOCK/POWER COMMON
36	+V_{ISO} OUTPUT
37	−V_{ISO} OUTPUT
38	INPUT FEEDBACK

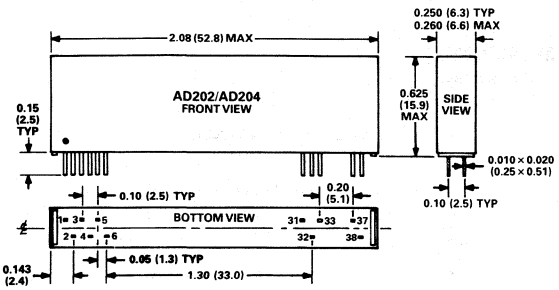
ORDERING GUIDE

Model	Package Option	Max Common-Mode Voltage (Peak)	Max Linearity
AD202JY	SIP	1000V	±0.05%
AD202KY	SIP	2000V	±0.025%
AD202JN	DIP	1000V	±0.05%
AD202KN	DIP	2000V	±0.025%
AD204JY	SIP	1000V	±0.05%
AD204KY	SIP	2000V	±0.025%
AD204JN	DIP	1000V	±0.05%
AD204KN	DIP	2000V	±0.025%

OUTLINE DIMENSIONS

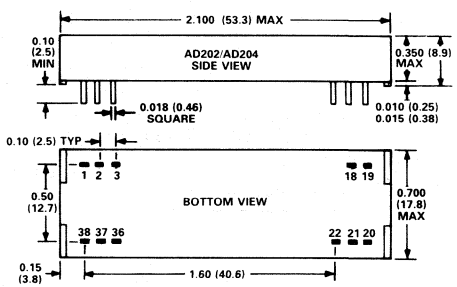
Dimensions shown in inches and (mm).

AD202/AD204 SIP PACKAGE



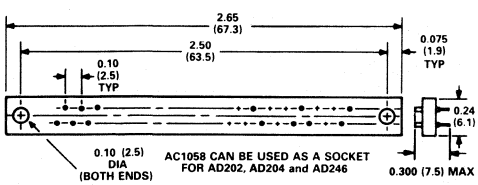
NOTE
PIN 31 IS PRESENT ONLY ON AD202.
PIN 33 IS PRESENT ONLY ON AD204.

AD202/AD204 DIP PACKAGE



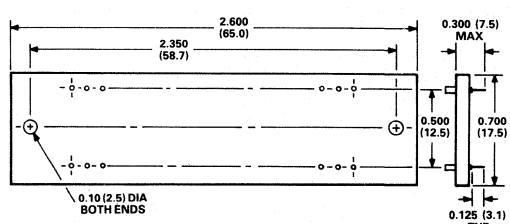
NOTE
PIN 20 IS PRESENT ONLY ON AD202.
PIN 21 IS PRESENT ONLY ON AD204.

AC1058 MATING SOCKET



NOTE: AMP ZP SOCKET (PIN 2 – 382006 – 3) MAY BE USED IN PLACE OF THE AC1058.

AC1060 MATING SOCKET



5

SPECIFICATIONS

(typical @ +25°C & V_S = +15V unless otherwise noted)

Model	AD246JY	AD246JN
OUTPUT[1]		
Frequency	25kHz nominal	*
Voltage	15V p-p nominal	*
Fan-Out	32 max	*
POWER SUPPLY REQUIREMENTS		
Input Voltage	+15V ±5%	*
Supply Current		
Unloaded	3.5mA	*
Each AD204 Adds	2.2mA	*
Each 1mA Load on AD204 +V_{ISO} or −V_{ISO} Adds	0.7mA	*

NOTES
*Specifications the same as the AD246JY.
[1]The high current drive output will not support a short to ground.
Specifications subject to change without notice.

AD246 PIN DESIGNATIONS

PIN (Y)	PIN (N)	FUNCTION
1	12	+15V POWER IN
2	1	CLOCK OUTPUT
12	14	COMMON
13	24	COMMON

CAUTION
ESD (electrostatic discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

DIFFERENCES BETWEEN THE AD202 AND AD204

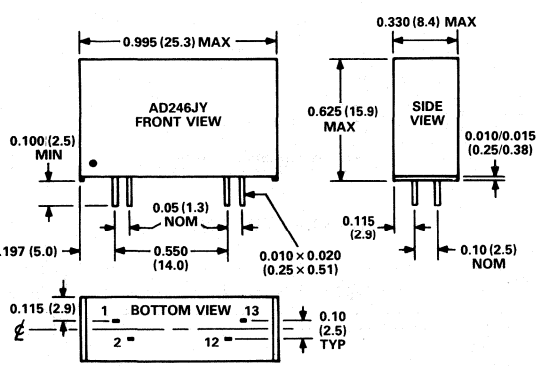
The primary distinction between the AD202 and AD204 is in the method by which they are powered: the AD202 operates directly from +15V dc while the AD204 is powered by a non-isolated externally-supplied clock (AD246) which can drive up to 32 AD204s. The main advantages of using the externally-clocked AD204 over the AD202 are reduced cost in multichannel applications, lower power consumption, and higher bandwidth. In addition, the AD204 can supply substantially more isolated power than the AD202.

Of course, in a great many situations, especially where only one or a few isolators are used, the convenience of stand-alone operation provided by the AD202 will be more significant than any of the AD204's advantages. There may also be cases where it is desirable to accommodate either device interchangeably, so the pinouts of the two products have been designed to make that easy to do.

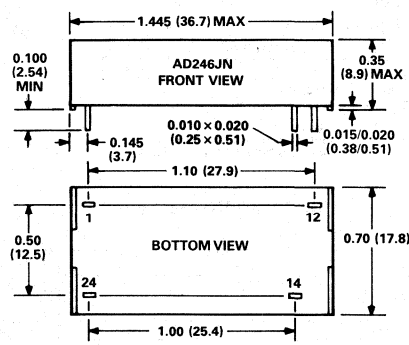
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

AD246JY PACKAGE



AD246JN PACKAGE



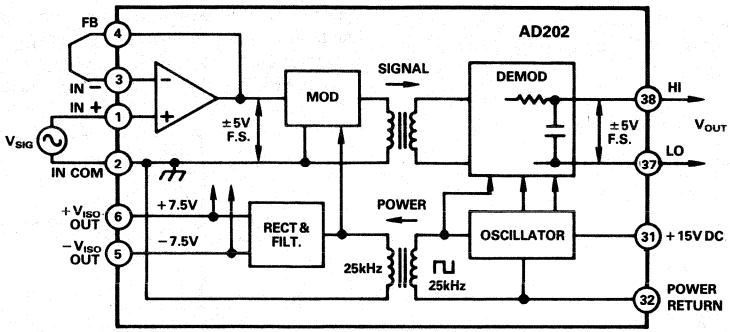


Figure 1a. AD202 Functional Block Diagram

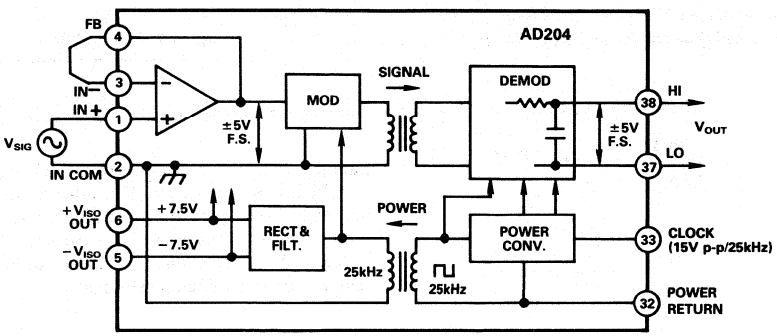


Figure 1b. AD204 Functional Block Diagram
(Pin Designations Apply to the DIP-Style Package.)

INSIDE THE AD202 AND AD204

The AD202 and AD204 use an amplitude modulation technique to permit transformer coupling of signals down to dc (Figure 1a and 1b). Both models also contain an uncommitted input op amp and a power transformer which provides isolated power to the op amp, the modulator, and any external load. The power transformer primary is driven by a 25kHz, 15V p-p square wave which is generated internally in the case of the AD202, or supplied externally for the AD204.

Within the signal swing limits of approximately ±5V, the output voltage of the isolator is equal to the output voltage of the op amp; that is, the isolation barrier has unity gain. The output signal is not internally buffered, so the user is free to interchange the output leads to get signal inversion. Additionally, in multichannel applications, the unbuffered outputs can be multiplexed with one buffer following the mux. This technique minimizes offset errors while reducing power consumption and cost. The output resistance of the isolator is typically 3kΩ for the AD204 (7kΩ for AD202) and varies with signal level and temperature, so it should not be loaded (see Figure 2 for the effects of load upon nonlinearity and gain drift). In many cases a high-impedance load will be present or a following circuit such as an output filter can serve as a buffer, so that a separate buffer function will not often be needed.

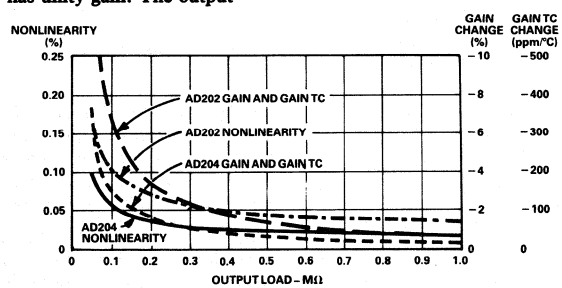


Figure 2. Effects of Output Loading

(Circuit figures shown on this page are for SIP style packages. Refer to third page of this data sheet for proper DIP package pin designations.)

USING THE AD202 AND AD204

Powering the AD202. The AD202 requires only a single +15V power supply connected as shown in Figure 3a. A bypass capacitor is provided in the module.

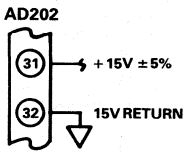


Figure 3a.

Powering the AD204. The AD204 gets its power from an externally supplied clock signal (a 15V p-p square wave with a nominal frequency of 25kHz) as shown in Figure 3b.

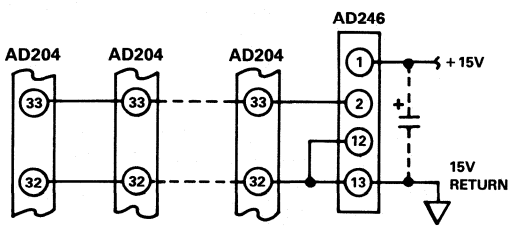


Figure 3b.

AD246 Clock Driver. The AD246 is a compact, inexpensive clock driver that can be used to obtain the required clock from a single 15V supply. Alternatively, the circuit shown in Figure 4 (essentially an AD246) can be used. In either case, one clock circuit can operate at least 32 AD204s at the rated minimum supply voltage of 14.25V and one additional isolator can be operated for each 40mV increase in supply voltage up to 15V. A supply bypass capacitor is included in the AD246, but if many AD204s are operated from a single AD246, an external bypass capacitor should be used with a value of at least 1μF for every five isolators used. Place the capacitor as close as possible to the clock driver.

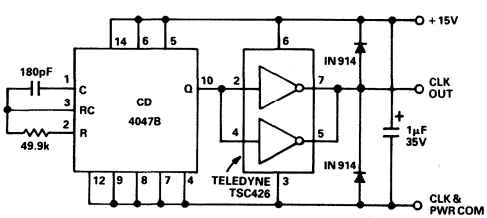


Figure 4. Clock Driver

(Circuit figures shown on this page are for SIP style packages. Refer to third page of this data sheet for proper DIP package pin designations.)

Input Configurations. The AD202 and AD204 have been designed to be very easy to use in a wide range of applications. The basic connection for standard unity gain applications, useful for signals up to ±5V, is shown in Figure 5; some of the possible variations are described below. When smaller signals must be

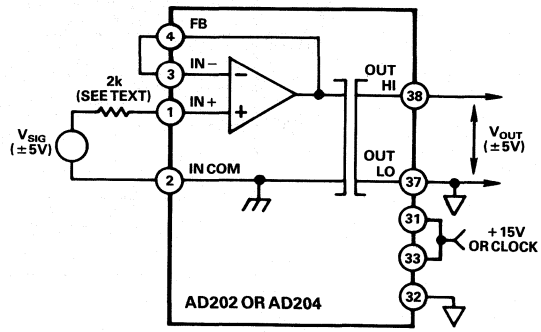


Figure 5. Basic Unity-Gain Application

handled, Figure 6 shows how to get gain while preserving a very high input resistance. The value of feedback resistor R_F should be kept above 20kΩ for best results. Whenever a gain of more than five is taken, a 100pF capacitor from FB to IN COM is required. At lower gains this capacitor is unnecessary, but it will not adversely affect performance if used.

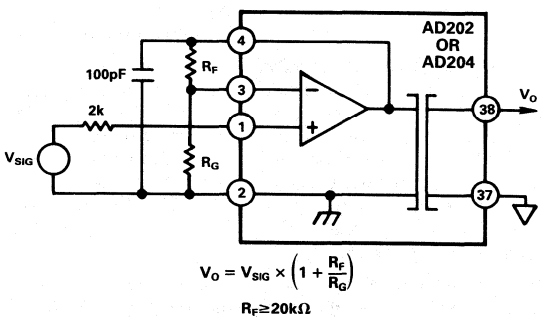


Figure 6. Input Connections for Gain > 1

The "noninverting" circuit of Figures 5 and 6 can also be used to advantage when a signal inversion is needed: just interchange either the input leads or the output leads to get inversion. This approach retains the high input resistance of the "noninverting" circuit, and at unity gain no gain-setting resistors are needed.

When the isolator is not powered, a negative input voltage of more than about 2V will cause an input current to flow. If the signal source can supply more than a few mA under such conditions, the 2kΩ resistor shown in series with IN+ should be used to limit current to a safe value. This is particularly important with the AD202, which may not start if a large input current is present.

Figure 7 shows how to accommodate current inputs or sum currents or voltages. This circuit can also be used when the input signal is larger than the ±5V input range of the isolator; for example, a ±50V input span can be accommodated with R_F = 20k and R_S = 200k. Once again, a capacitor from FB to IN COM is required for gains above 5.

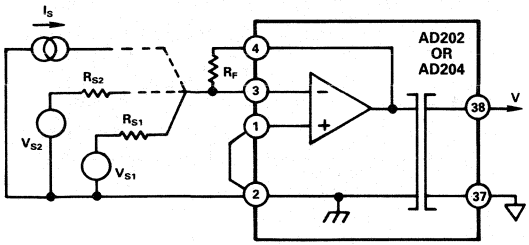


Figure 7. Connections for Summing or Current Inputs

Adjustments. When gain and zero adjustments are needed, the circuit details will depend on whether adjustments are to be made at the isolator input or output, and (for input adjustments) on the input circuit used. Adjustments are usually best done on the input side, because it is better to null the zero ahead of the gain, and because gain adjustment is most easily done as part of the gain-setting network. Input adjustments are also to be preferred when the pots will be near the input end of the isolator (to minimize common-mode strays). Adjustments on the output side might be used if pots on the input side would represent a hazard due to the presence of large common-mode voltages during adjustment.

Figure 8a shows the input-side adjustment connections for use with the "noninverting" connection of the input amplifier. The zero adjustment circuit injects a small adjustment voltage in series with the low side of the signal source. (This will not work if the source has another current path to input common or if current flows in the signal source LO lead). Since the adjustment voltage is injected ahead of the gain, the values shown will work for any gain. Keep the resistance in series with input LO below a few hundred ohms to avoid CMR degradation.

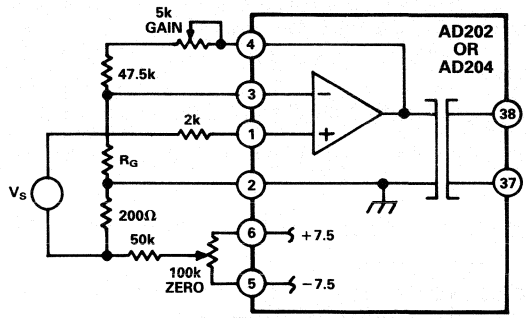


Figure 8a. Adjustments for Noninverting Connection of Op Amp

Also shown in Figure 8a is the preferred means of adjusting the gain-setting network. The circuit shown gives a nominal R_F of 50kΩ, and will work properly for gains of ten or greater. The adjustment becomes less effective at lower gains (its effect is halved at G = 2) so that the pot will have to be a larger fraction of the total R_F at low gain. At G = 1 (follower) the gain cannot be adjusted downward without compromising input resistance; it is better to adjust gain at the signal source or after the output.

Figure 8b shows adjustments for use with inverting input circuits. The zero adjustment nulls the voltage at the summing node. This method is preferable to current injection because it is less affected by subsequent gain adjustment. Gain adjustment is again done in the feedback; but in this case it will work all the way down to unity gain (and below) without alteration.

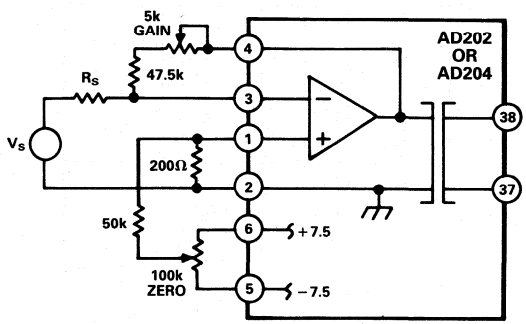


Figure 8b. Adjustments for Summing or Current Input

(Circuit figures shown on this page are for SIP style packages. Refer to third page of this data sheet for proper DIP package pin designations.)

Figure 9 shows how zero adjustment is done at the output by taking advantage of the semi-floating output port. The range of this adjustment will have to be increased at higher gains; if that is done, be sure to use a suitably stable supply voltage for the pot circuit.

There is no easy way to adjust gain at the output side of the isolator itself. If gain adjustment must be done on the output side, it will have to be in a following circuit such as an output buffer or filter.

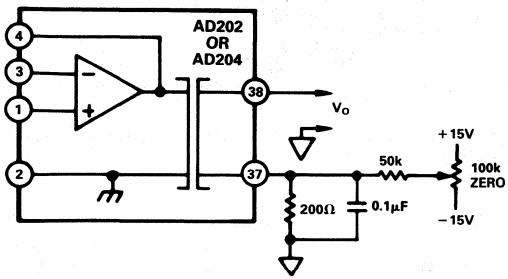


Figure 9. Output-Side Zero Adjustment

Common-Mode Performance. Figures 10a and 10b show how the common-mode rejection of the AD202 and AD204 varies with frequency, gain, and source resistance. For these isolators, the significant resistance will normally be that the path from the source of the common-mode signal to IN COM. The AD202 and AD204 also perform well in applications requiring rejection of fast common-mode steps, as described in the Applications section.

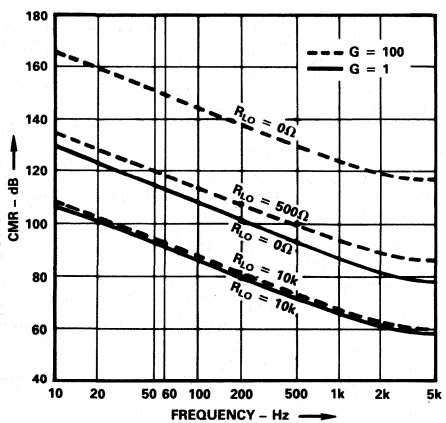


Figure 10a. AD204

(Circuit figures shown on this page are for SIP style packages. Refer to third page of this data sheet for proper DIP package pin designations.)

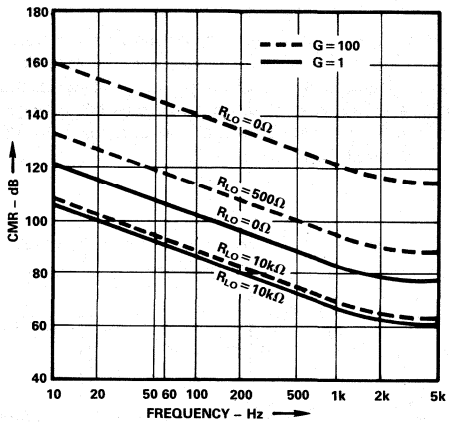


Figure 10b. AD202

Dynamics and Noise. Frequency response plots for the AD202 and AD204 are given in Figure 11. Since neither isolator is slew-rate limited, the plots apply for both large and small signals. Capacitive loads of up to 470pF will not materially affect frequency response. When large signals beyond a few hundred Hz will be present, it is advisable to bypass $-V_{ISO}$ and $+V_{ISO}$ to IN COM with 1μF tantalum capacitors even if the isolated supplies are not loaded.

At 50/60Hz, phase shift through the AD202/AD204 is typically 0.8° (lagging). Typical unit – unit variation is ±0.2° (lagging).

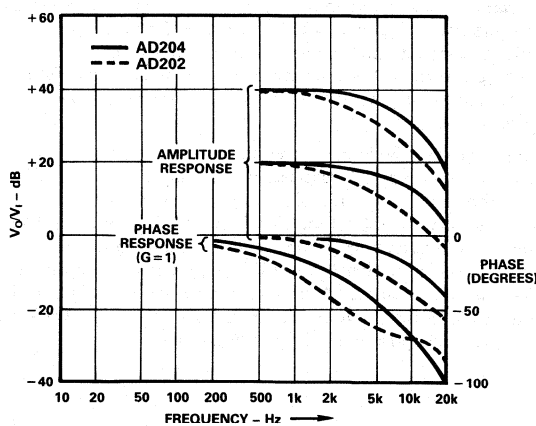


Figure 11. Frequency Response at Several Gains

The step response of the AD204 for very fast input signals can be improved by the use of an input filter, as shown in Figure 12. The filter limits the bandwidth of the input (to about 5.3kHz) so that the isolator does not see fast, out-of-band input terms that can cause small amounts (±0.3%) of internal ringing. The AD204 will then settle to ±0.1% in about 300 microseconds for a 10V step.

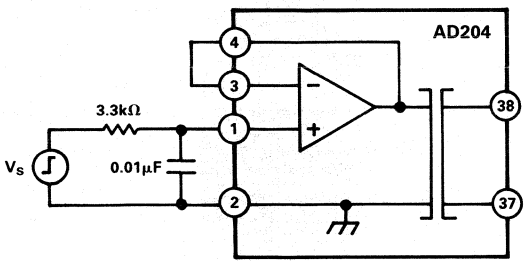


Figure 12. Input Filter for Improved Step Response

Except at the highest useful gains, the noise seen at the output of the AD202 and AD204 will be almost entirely comprised of carrier ripple at multiples of 25kHz. The ripple is typically 2mV p-p near zero output and increases to about 7mV p-p for outputs of ±5V (1MHz measurement bandwidth). Adding a capacitor across the output will reduce ripple at the expense of bandwidth: for example, 0.05μF at the output of the AD204 will result in 1.5mV ripple at ±5V, but signal bandwidth will be down to 1kHz.

When the full isolator bandwidth is needed, the simple two-pole active filter shown in Figure 13 can be used. It will reduce ripple to 0.1mV p-p with no loss of signal bandwith, and also serves as an output buffer.

An output buffer or filter may sometimes show output spikes that do not appear at its input. This is usually due to clock noise appearing at the op amp's supply pins (since most op amps have little or no supply rejection at high frequencies). Another common source of carrier-related noise is the sharing of a ground track by both the output circuit and the power input. Figure 13 shows how to avoid these problems: the clock/supply port of the isolator does not share ground or 15V tracks with any signal circuits, and the op amp's supply pins are bypassed to signal common (note that the grounded filter capacitor goes here as well). Ideally, the output signal LO lead and the supply common meet where the isolator output is actually measured, e.g. at an A/D converter input. If that point is more than a few feet from the isolator, it may be useful to bypass output LO to supply common at the isolator with a 0.1μF capacitor.

In applications where more than a few AD204s are driven by a single clock driver, substantial current spikes will flow in the power return line and in whichever signal out lead returns to a low impedance point (usually output LO). Both of these tracks should be made large to minimize inductance and resistance; ideally, output LO should be directly connected to a ground plane which serves as measurement common.

Current spikes can be greatly reduced by connecting a small inductance (68μH–100μH) in series with the clock pin of each AD204. Molded chokes such as the Dale IM-2 series, with dc resistance of about 5Ω, are suitable.

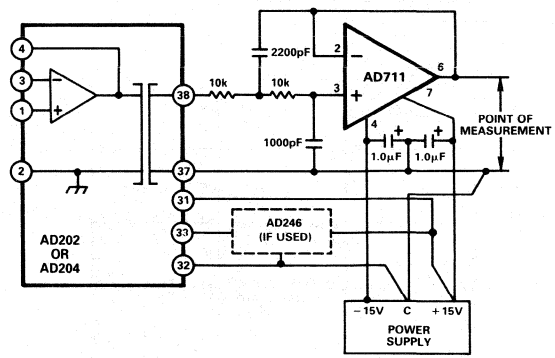


Figure 13. Output Filter Circuit Showing Proper Grounding

Using Isolated Power. Both the AD202 and the AD204 provide ±7.5V power outputs referenced to input common. These may be used to power various accessory circuits which must operate at the input common-mode level; the input zero adjustment pots described above are an example, and several other possible uses are shown in the section titled Application Examples.

The isolated power output of the AD202 (400μA total from either or both outputs) is much more limited in current capacity than that of the AD204, but it is sufficient for operating micropower op amps, low power references (such as the AD589), adjustment circuits, and the like.

The AD204 gets its power from an external clock driver, and can handle loads on its isolated supply outputs of 2mA for each supply terminal (+7.5V and −7.5V) or 3mA for a single loaded output. Whenever the external load on either supply is more than about 200μA, a 1μF tantalum capacitor should be used to bypass each loaded supply pin to input common.

Up to 32 AD204s can be driven from a single AD246 (or equivalent) clock driver when the isolated power outputs of the AD204s are loaded with less than 200μA each, at a worst-case supply voltage of 14.25V at the clock driver. The number of AD204s that can be driven by one clock driver is reduced by one AD204 per 3.5mA of isolated power load current at 7.5V, distributed in any way over the AD204's being supplied by that clock driver. Thus a load of 1.75mA from $+V_{ISO}$ to $-V_{ISO}$ would also count as one isolator because it spans 15V.

(Circuit figures shown on this page are for SIP style packages. Refer to third page of this data sheet for proper DIP package pin designations.)

It is possible to increase clock fanout by increasing supply voltage above the 14.25V minimum required for 32 loads. One additional isolator (or 3.5mA unit load) can be driven for each 40mV of increase in supply voltage up to 15V. Therefore if the minimum supply voltage can be held to 15V – 1%, it is possible to operate 32 AD204's and 52mA of 7.5V loads. Figure 14 shows the allowable combinations of load current and channel count for various supply voltages.

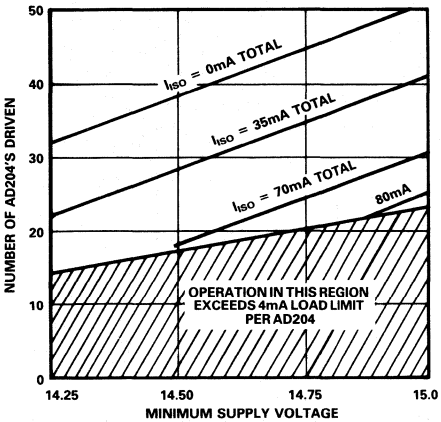


Figure 14. AD246 Fanout Rules

Operation at Reduced Signal Swing. Although the nominal output signal swing for the AD202 and AD204 is ±5V, there may be cases where a smaller signal range may be desirable. When that is done, the fixed errors (principally offset terms and output noise) become a larger fraction of the signal, but nonlinearity is reduced. This is shown in Figure 15.

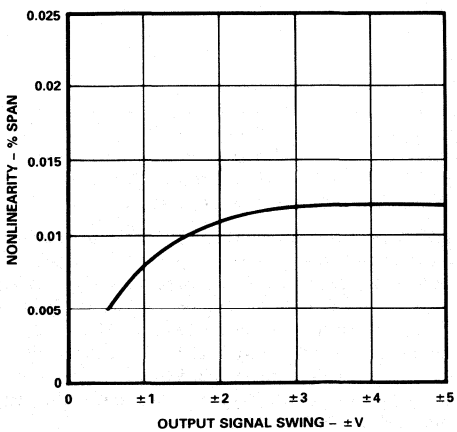


Figure 15. Nonlinearity vs. Signal Swing

PCB Layout for Multichannel Applications. The pinout of the AD204Y has been designed to make very dense packing possible in multichannel applications. Figure 16a shows the recommended printed circuit board (PCB) layout for the simple voltage-follower connection. When gain-setting resistors are present, 0.25″ channel centers can still be achieved, as shown in Figure 16b.

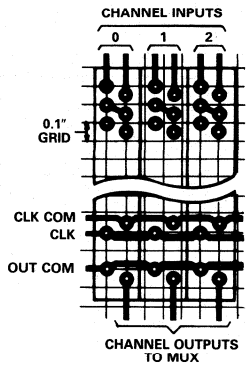


Figure 16a.

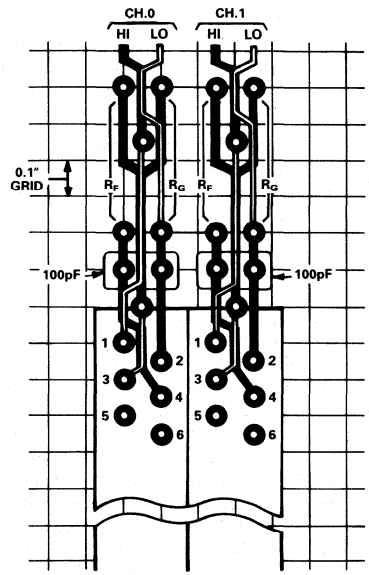


Figure 16b.

(Circuit figures shown on this page are for SIP style packages. Refer to third page of this data sheet for proper DIP package pin designations.)

Synchronization. Since AD204's operate from a common clock, synchronization is inherent. AD202s will normally not interact to produce beat frequencies even when mounted on 0.25-inch centers. Interaction may occur in rare situations where a large number of long, unshielded input cables are bundled together and channel gains are high. In such cases, shielded cable may be required or AD204's can be used.

APPLICATIONS EXAMPLES

Low-Level Sensor Inputs. In applications where the output of low-level sensors such as thermocouples must be isolated, a low-drift input amplifier can be used with an AD204, as shown in Figure 17. A three-pole active filter is included in the design to get normal-mode rejection of frequencies above a few Hz and to provide enhanced common-mode rejection at 60Hz. If offset adjustment is needed, it is best done at the trim pins of the OP-07 itself; gain adjustment can be done at the feedback resistor.

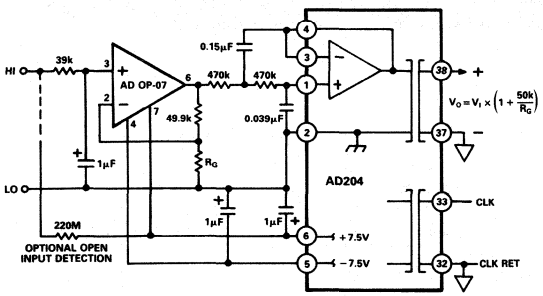


Figure 17. Input Amplifier & Filter for Sensor Signals

Note that the isolated supply current is large enough to mandate the use of 1μF supply bypass capacitors. This circuit can be used with an AD202 if a low-power op amp is used instead of the OP-07.

Process Current Input with Offset. Figure 18 shows an isolator receiver which translates a 4-20mA process current signal into a 0 to +10V output. A 1V to 5V signal appears at the isolator's output, and a −1V reference applied to output LO provides the necessary level shift (in multichannel applications, the reference can be shared by all channels). This technique is often useful for getting offset with a follower-type output buffer.

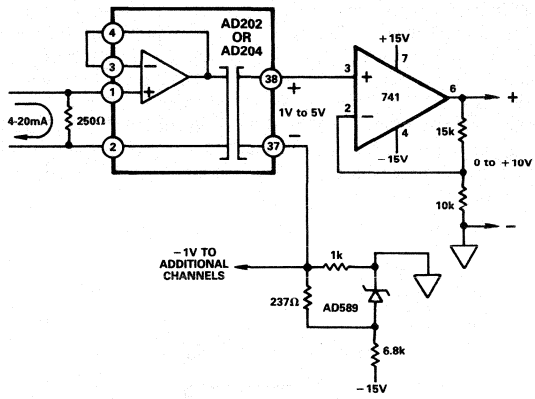


Figure 18. Process Current Input Isolator with Offset

The circuit as shown requires a source compliance of at least 5V, but if necessary that can be reduced by using a lower value of current-sampling resistor and configuring the input amplifier for a small gain.

High-Compliance Current Source. In Figure 19, an isolator is used to sense the voltage across current-sensing resistor R to allow direct feedback control of a high-voltage transistor or FET used as a high-compliance current source. Since the isolator has virtually no response to dc common-mode voltage, the closed-loop current source has a static output resistance greater than $10^{14}\Omega$ even for output currents of several mA. The output current capability of the circuit is limited only by power dissipation in the source transistor.

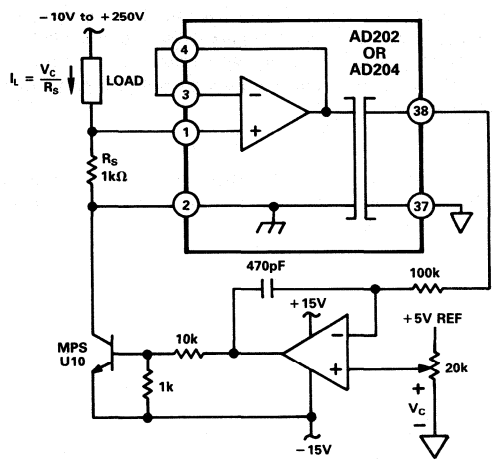


Figure 19. High-Compliance Current Source

(Circuit figures shown on this page are for SIP style packages. Refer to third page of this data sheet for proper DIP package pin designations.)

Motor Control Isolator. The AD202 and AD204 perform very well in applications where rejection of fast common-mode steps is important but bandwidth must not be compromised. Current sensing in a full-wave bridge motor driver (Figure 20) is one example of this class of application. For 200V common-mode steps (1μs rise time) and a gain of 50 as shown, the typical response at the isolator output will be spikes of ±5mV amplitude, decaying to zero in less than 100μs. Spike height can be reduced by a factor of four with output filtering just beyond the isolator's bandwidth.

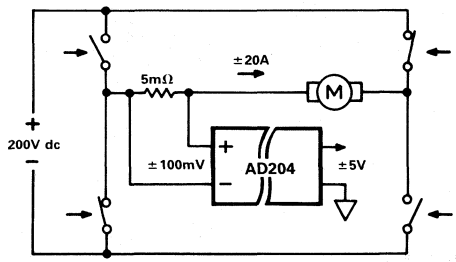


Figure 20. Motor Control Current Sensing

Floating Current Source/Ohmmeter. When a small floating current is needed with a compliance range of up to ±1000V dc, the AD204 can be used to both create and regulate the current. This can save considerable power, since the controlled current does not have to return to ground. In Figure 21, an AD589 reference is used to force a small fixed voltage across R. That sets the current which the input op amp will have to return through the load to zero its input. Note that the isolator's output isn't needed at all in this application; the whole job is done by the input section. However, the signal at the output could be useful: it's the voltage across the load, referenced to ground. Since the load current is known, the output voltage is proportional to load resistance.

(Circuit figures shown on this page are for SIP style packages. Refer to third page of this data sheet for proper DIP package pin designations.)

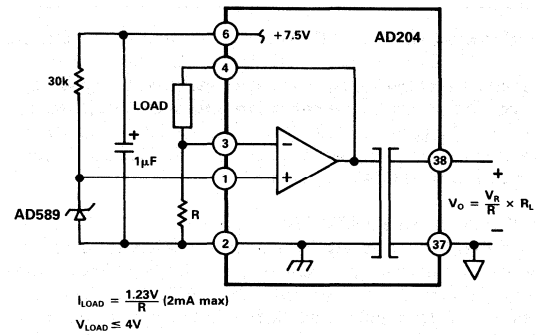


Figure 21. Floating Current Source

Photodiode Amplifier. Figure 22 shows a transresistance connection used to isolate and amplify the output of a photodiode. The photodiode operates at zero bias, and its output current is scaled by R_F to give a +5V full-scale output.

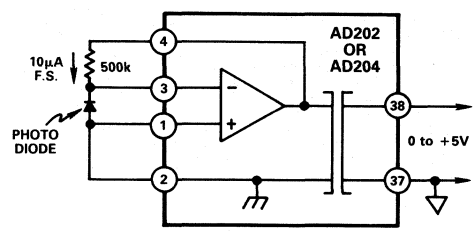


Figure 22. Photodiode Amplifier

ANALOG DEVICES

Rugged, Military Temperature Range, 10 kHz Bandwidth Isolation Amplifier

AD203SN

FEATURES
Rugged Design: Meets Stringent MIL-STD-883C Environmental Test Methods
1004 (Moisture Resistance)
1010 Condition B (Temperature Cycling, −55°C to +125°C)
2002 Condition B (Mechanical Shock @ 1,500 g for 0.5 ms)
2004 (Lead Integrity)
2007 Condition A (Variable Frequency Vibration @ 20 g)
2015 (Resistance to Solvents)
Reliable Design: Conforms to Stringent Quality and Reliability Standards
Characterized to the Full Military Temperature Range −55°C to +125°C Rated Performance
10 kHz Full Power Bandwidth
Low Nonlinearity: ±0.025% max
Wide Output Range: ±10 V min (Into a 2.5 kΩ Load)
High CMV Isolation: 1500 V RMS Continuous
Isolated Power: ±15 V DC @ ±5 mA
Small Size: 2.23″×0.83″×0.65″
56.6 mm×21.1 mm×16.5 mm
Uncommitted Input Amplifier
Two-Port Isolation Through Transformer Coupling

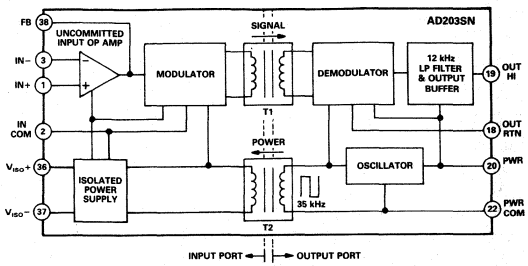
ISOLATION AMPLIFIERS
Provide Galvanic Isolation Between the Input and Output Stages
Eliminate Ground Loops
Reject High Common Mode Voltages and Noise
Protect Sensitive Electronic Signal Processing Systems from Transient and/or Fault Voltages

APPLICATIONS INCLUDE
Engine Monitoring and Control
Mobile Multichannel Data Acquisition Systems
Instrumentation and/or Control Signal Isolation
Current Shunt Measurements
High Voltage Instrumentation Amplifier

GENERAL DESCRIPTION

The AD203SN is designed and built expressly for use in hostile operating environments. The AD203SN is also an integral member of Analog Devices' AD200 Series of low cost, high performance, transformer coupled isolation amplifiers. Technological innovations in circuit design, transformer construction, surface mount components and assembly automation have resulted in a rugged, economical, military temperature range isolator that either retains or improves upon the key performance specifications of the AD202/AD204 line.

FUNCTIONAL BLOCK DIAGRAM



The AD203SN provides total galvanic isolation between the input and output stages of the isolation amplifier, including the power supplies, through the use of internal transformer coupling. The functionally complete design of the AD203SN, powered by a single +15 V dc supply, eliminates the need for an external dc/dc converter. This permits the designer to minimize the necessary circuit overhead and consequently reduce the overall design and component costs. Furthermore, the power consumption, nonlinearity and drift characteristics of transformer coupled devices are vastly superior to those achievable with other isolation technologies, without sacrificing bandwidth or noise performance. Finally, the AD203SN will maintain its high operating performance even under sustained common mode stress.

The design of the AD203SN emphasizes maximum flexibility and ease of use in a broad range of applications where signals must be measured or transmitted under high CMV conditions. The AD203SN has a ±10 V output range, an uncommitted input amplifier, an output buffer, a 10 kHz full power bandwidth and a front-end isolated power supply of ±15 V dc @ ±5 mA.

5

AD203SN—SPECIFICATIONS (typical @ +25°C, V_S = +15 V dc unless otherwise noted)

Parameter	
GAIN	
Range	1 V/V–100 V/V
Error	±1% typ (±4% max)
vs. Temperature[1]	
−55°C to +125°C	50 ppm/°C
−55°C to +25°C	100 ppm/°C
−40°C to +25°C	80 ppm/°C
−25°C to +25°C	60 ppm/°C
+25°C to +125°C	5 ppm/°C
vs. Time	±50 ppm/1000 hours
vs. Supply Voltage	±0.005%/V
Nonlinearity[2], G = 1 V/V, ±10 V Output Swing	±0.012% (±0.025% max)
INPUT VOLTAGE RATINGS	
Linear Differential Range	±10 V
Max CMV Input to Output	
AC, 60 Hz, Continuous	1500 V rms
Continuous (ac and dc)	±2000 V peak
Common Mode Rejection (CMR) @ 60 Hz	
$R_S \leq 100\ \Omega$ (HI & LO Inputs), G = 1 V/V	106 dB
G = 100 V/V	120 dB
$R_S \leq 1\ k\Omega$ (Input, HI, LO or Both), G = 1–100 V/V	96 dB (min)
Leakage Current, Input to Output @ 240 V rms, 60 Hz	4.0 μA rms (max)
INPUT IMPEDANCE	
Differential (G = 1 V/V)	$10^{12}\ \Omega$
Common Mode	2 GΩ‖4.5 pF
INPUT BIAS CURRENT	
Initial @ +25°C	30 pA
Current @ +125°C	30 nA
INPUT DIFFERENCE CURRENT	
Initial @ +25°C	±5 pA
Current @ +125°C	±5 nA
INPUT NOISE	
Voltage, 0.1 Hz to 100 Hz	4 μV p–p
Voltage, Frequency > 200 Hz	50 nV/$\sqrt{\text{Hz}}$
FREQUENCY RESPONSE	
Bandwidth ($V_{OUT} \leq 20$ V p–p, G = 1–100 V/V)	10 kHz
Slew Rate	0.5 V/μs
Settling Time to ±0.10%	160 μs
OFFSET VOLTAGE, REFERRED TO INPUT (RTI)	
Initial @ +25°C (Adjustable to Zero)	± (5 + 25/G) mV (max)
vs. Temperature (−55°C to +125°C)	± (6 + 100/G) μV/°C
RATED OUTPUT[3]	
Voltage (Out HI to Out LO) @ R_L = 5.0 kΩ	±10 V (min)
Current	±4 mA
Maximum Capacitive Load[4]	270 pF
Output Resistance	0.2 Ω
Output Ripple, 100 kHz Bandwidth	15 mV p–p
5 kHz Bandwidth	0.7 mV rms
ISOLATED POWER OUTPUT[5]	
Voltage, No Load	±15 V
Accuracy	±5%
Current (Either Output)	5 mA
Regulation, No Load to Full Load	5%
Ripple, 100 kHz Bandwidth, Full Load	110 mV p–p

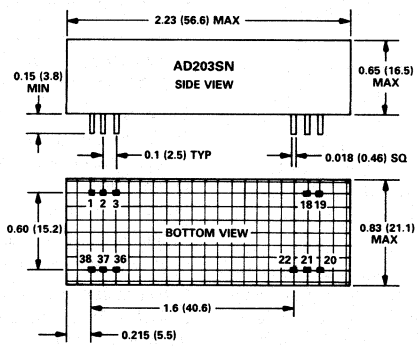
Parameter	
POWER SUPPLY	
Voltage, Rated Performance	+15 V dc (±5%)
Voltage, Operating Performance[6]	+12 V dc to +16 V dc
Current, No Load (V_S = +15 V dc)	20 mA
TEMPERATURE RANGE	
Rated Performance	−55°C to +125°C
Storage	−55°C to +125°C
PACKAGE DIMENSIONS	
Inches	2.23 × 0.83 × 0.65
Millimeters	56.6 × 21.1 × 16.5

NOTES
[1]Refer to Figure 1 for a plot of gain versus temperature.
[2]For gains greater than 50 V/V, a 100 pF capacitor from the feedback terminal of the input op amp (Pin 38) to the input common terminal (Pin 2) is recommended in order to minimize the gain nonlinearity. Refer to Figure 17 for a circuit schematic.
[3]For additional information on the Rated Output parameters, refer to Figure 9 for a plot of the Output Voltage Swing vs. Power Supply Voltage, and Figure 10 for the Output Current vs. Temperature and Power Supply Voltage relationship.
[4]For larger capacitive loads, it is recommended that a 4.7 Ω resistor be placed in series with the load in order to suppress possible output oscillations.
[5]1.0 μF (min) decoupling is required.
[6]Refer to Figure 9 for a plot of output voltage swing versus supply voltage.
Specifications subject to change without notice.

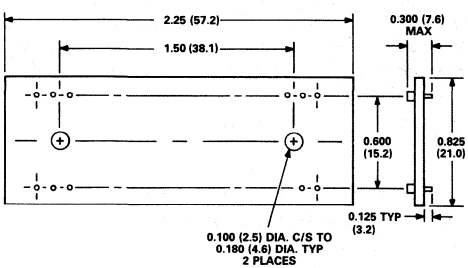
5

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



AC1062 MATING SOCKET



AD203SN PIN DESIGNATIONS

PIN	DESIGNATION	FUNCTION	PORT
1	IN+	INPUT OP AMP: NONINVERTING INPUT	INPUT
2	IN COM	INPUT COMMON	INPUT
3	IN−	INPUT OP AMP: INVERTING INPUT	INPUT
18	OUT RTN	OUTPUT RETURN	OUTPUT
19	OUT HI	OUTPUT SIGNAL	OUTPUT
20	PWR IN	DC POWER SUPPLY INPUT	OUTPUT
21	NONE	NONE	–
22	PWR COM	DC POWER SUPPLY COMMON	OUTPUT
36	V_{ISO}+	ISOLATED POWER: +DC	INPUT
37	V_{ISO}−	ISOLATED POWER: −DC	INPUT
38	FB	INPUT OP AMP: OUTPUT/FEEDBACK	INPUT

CAUTION

ESD (electrostatic discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be discharged to the destination socket before devices are removed.

Note: Per MIL-STD-883C, Method 3015, this device have been classified as a Category 2 ESD sensitive device.

PRODUCT HIGHLIGHTS

Rugged Design. The AD203SN is specifically designed for applications where ruggedness and high performance are the key requirements. The ruggedness of the AD203SN design meets MIL-STD-883C Methods 1004 (Moisture Resistance), 1010 Condition B (Temperature Cycling, −55°C to +125°C), 2002 Condition B (Mechanical Shock @ 1,500 g for 0.5 ms), 2004 (Lead Integrity), 2007 Condition A (Variable Frequency Vibration @ 20 g) and 2015 (Resistance to Solvents).

Engine and vehicular monitor/control systems as well as mobile instrumentation and control systems are some examples of applications for which the AD203SN is well suited.

Military Temperature Range Rating. With its performance rated over the −55°C to +125°C MIL specification temperature range, the AD203SN is an excellent choice in applications where severe environmental conditions may be encountered. Examples include engine monitoring/control systems and remote power line monitoring.

10 kHz Bandwidth. With a full power bandwidth of 10 kHz, the AD203SN is effective in control loop applications where a smaller bandwidth could induce control system instabilities.

Excellent Common Mode Performance. The AD203SN provides a 1.5 kV rms continuous common mode isolation. A low common mode input capacitance of 4.5 pF, inclusive of power isolation, results in a minimum 96 dB of CMR as well as a very low leakage current of 4.0 μA rms (max @ 240 V rms, 60 Hz).

High Accuracy. Exhibiting a maximum nonlinearity of ±0.025% and a low gain temperature coefficient, averaging 50 ppm/°C over the full temperature range, the AD203SN provides high isolation without loss of signal integrity and quality.

Isolated Power. An isolated power supply capable of delivering ±15 V dc @ ±5 mA is available at the input port of the isolator. This permits the AD203SN to power up floating signal conditioners, front-end amplifiers or remote transducers at the input.

Flexible Input Stage. An uncommitted op amp is provided on the input stage. This amplifier provides input buffering and gain as needed. It also facilitates a host of alternative input functions including filtering, summing, high voltage ranges and current (transimpedance) inputs.

DESCRIPTION OF KEY SPECIFICATIONS

Gain Nonlinearity. Nonlinearity is defined as the peak deviation of the output voltage from the best straight line and is expressed as a percent of peak-to-peak output voltage span. The nonlinearity of the model AD203SN, which operates at a 20 V p–p output span, is ±0.025% or ±5 mV. Good nonlinearity is critical for retaining signal fidelity.

Max CMV, Input to Output. Maximum common mode voltage (CMV) describes the amount of voltage that may be applied across both input terminals with respect to the output terminals without degrading the integrity of the isolation barrier. High input-to-output CMV capability is necessary in applications where high CMV inputs exist or high voltage transients may occur at the input.

Common Mode Rejection (CMR). CMR describes the isolator's ability to reject common mode voltages that may exist between the inputs and the outputs. High CMR is required when it is necessary to process small signals riding on high common mode voltages.

Leakage Current. This is the current that flows from the input common across the isolation barrier to the output common when the power-line voltage (either 115 V or 240 V rms, 60 Hz) is impressed on the inputs. Leakage current is dependent on the magnitude of the coupling capacitance between the input and the output ports. Line frequency leakage current levels are unaffected by the power ON or OFF condition of the AD203SN.

Common Mode Input Impedance. This is defined to be the impedance seen across either input terminal (i.e., +IN or −IN) and the input common.

Input Noise. This specification characterizes the voltage noise levels that are generated internally by the isolation amplifier. In order to facilitate a comparison between the "isolator background noise" levels and the expected input signal levels the input noise parameter is referred to the input.

Input noise is a function of the noise bandwidth, i.e., the frequency range over which the noise characteristics are measured.

Offset Voltage, Referred to Input (RTI). The offset voltage describes the isolation amplifier's total dc offset voltage with the inputs grounded. The offset voltage is referred to the input in order to allow for a comparison of the dc offset voltages with the expected input signal levels. The total offset comes from two sources, namely from the input and output stages, and is gain dependent. To compute the offset voltage, RTI, the isolator is modelled as two cascaded amplifier stages. The input stage has a variable gain G while the output isolation stage has a fixed gain of 1. RTI offset is then given by:

$$E_{OS}\,(RTI) = E_{OS1} + E_{OS2}/G$$

where:

E_{OS1} = Total input stage offset voltage

E_{OS2} = Output stage offset voltage

G = Input stage gain.

Offset voltage drift, RTI, is calculated in an identical manner.

Isolated Power Output. Dual supply voltages, completely isolated from the input power supply terminals, provide the capability to excite floating input signal conditioners as well as remote transducers.

PERFORMANCE CHARACTERISTICS

This section details the key specifications of the AD203SN that exhibit a functional dependence on such variables as frequency, power supply load, output voltage swing, bypass capacitance and temperature. Table I summarizes the performance characteristics that will be discussed in this section. For the sake of completeness, a typical dynamic output response of the AD203SN is included.

Gain Temperature Coefficient. Figure 1 presents the AD203SN's gain temperature coefficient over the entire −55°C to +125°C temperature range.

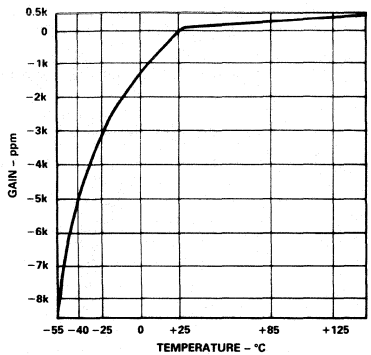


Figure 1. Gain (ppm of Span) vs. Temperature (°C)

Note: 1 ppm (part per million) is equivalent to 0.0001%.

Gain Nonlinearity. The maximum nonlinearity error of the AD203SN, at a gain of 1 V/V, is specified as ±0.025% or ±5 mV. The nonlinearity performance of the AD203SN is dependent on the output voltage swing and this dependency is illustrated in Figure 2. The horizontal axis represents the gain error, expressed either in percent of peak-to-peak output span (i.e., % of 20 V) on the left axis or in mV on the right axis. The vertical axis indicates the magnitude of the output voltage swing.

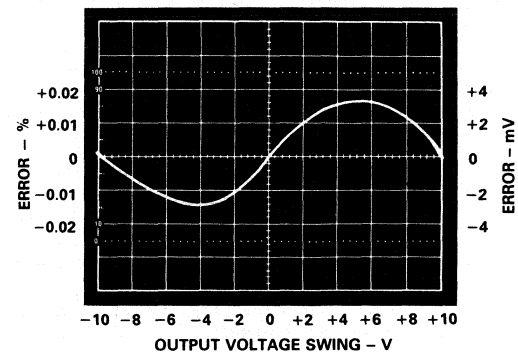


Figure 2. Gain Nonlinearity Error (% p–p Output Range and mV) vs. Output Voltage Swing (V), with a Gain of 1 V/V

Parameter	Key Specifications	As a Function of	Shown In
Gain	Gain (ppm of Span) Gain Nonlinearity (Expressed in mV and % of p–p Output)	Temperature (°C) Output Voltage Swing (V)	Figure 1 Figure 2
Input Voltage Rating	Common Mode Rejection (dB)	Common Mode Signal Frequency (Hz), Amplifier Gain (V/V) and Input Source Resistance (Ω)	Figure 3
Input Noise	Input Noise (nV/$\sqrt{\text{Hz}}$)	Frequency (Hz)	Figure 4
Frequency Response	Frequency Response: Gain (dB) Frequency Response: Phase Shift (Degree) Dynamic Response	Frequency (Hz) Frequency (Hz) N/A	Figure 5 Figure 6 Figure 7
Offset	Output Offset Voltage (mV)	Temperature (°C)	Figure 8
Rated Out	Output Voltage Swing (V) Output Current (mA)	Supply Voltage (V dc) Supply Voltage (V dc)	Figure 9 Figure 10
Isolated Power Supply	Isolated Power Supply Voltage (V) Isolated Power Supply Ripple (mV p–p) Isolated Power Supply Ripple (V p–p)	Current Delivered to the Load (mA) Current Delivered to the Load (mA) Bypass Capacitance (μF)	Figure 11 Figure 12 Figure 13

Table I. Performance Characteristics Detailed in the AD203SN Data Sheet

Common Mode Rejection. Figure 3 illustrates the common mode rejection (CMR), expressed in dB, of the AD203SN versus frequency (Hz), gain (V/V) and source impedance imbalance (Ω). To achieve the optimal common mode rejection of unwanted signals, it is recommended that the source imbalance be kept as low as possible and that the input circuitry be carefully laid out so as to avoid adding excessive stray capacitances at the isolator's input terminals.

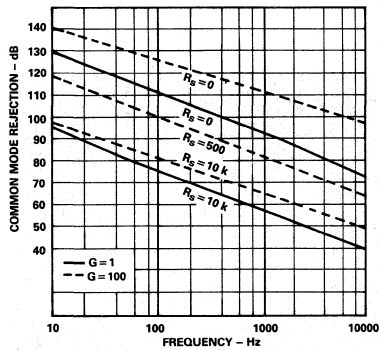


Figure 3. Common Mode Rejection (CMR) vs. Frequency (Hz), Gain (V/V) and Resistance (Ω)

Input Noise. Figure 4 presents the typical input noise characteristics, in nV/$\sqrt{\text{Hz}}$, of the AD203SN for a frequency range from 1 Hz to 100 kHz.

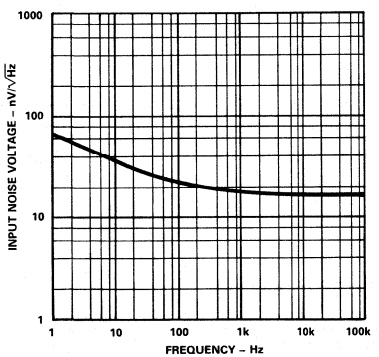


Figure 4. Input Noise (nV/$\sqrt{Hz}$) vs. Frequency (Hz)

Frequency Response: Gain and Phase Shift. Figure 5 illustrates the AD203SN's gain as a function of frequency while Figure 6 illustrates the corresponding phase shift vs. frequency. The AD203SN's low phase shift and 10 kHz bandwidth performance make it ideal in power monitoring and control system applications.

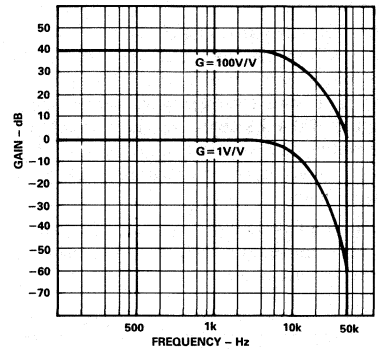


Figure 5. Gain (dB) as a Function of Frequency (Hz)

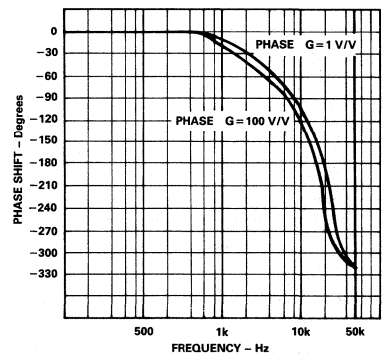


Figure 6. Phase Shift (Δ°) as a Function of Frequency (Hz)

Dynamic Response of the AD203SN. To illustrate the speed, dynamic range and rapid settling time of the AD203SN, the isolator's output response to a 20 V p–p step function is shown in Figure 7.

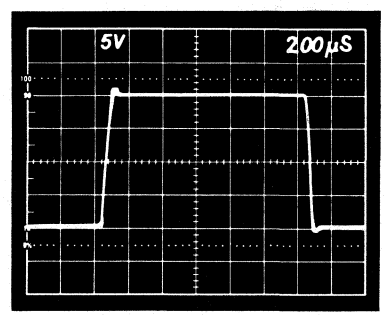


Figure 7. Dynamic Response of the AD203SN (20 V p–p Step)

Output Offset Voltage. The AD203SN exhibits a low output offset voltage temperature coefficient over the +25°C to +125°C temperature range as shown in Figure 8.

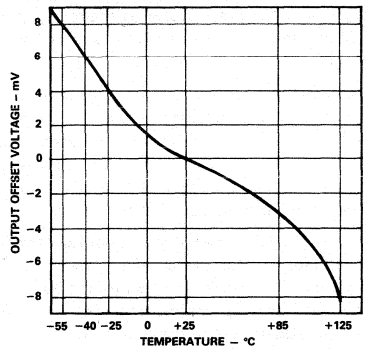


Figure 8. Output Offset Voltage (mV) vs. Temperature (°C) with G=1 V/V

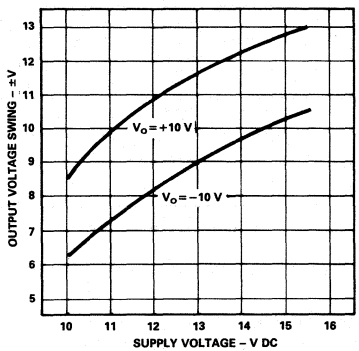


Figure 9. Output Voltage Swing (±V) vs. Power Supply Input Voltage (V DC), with a 2.5 kΩ Load

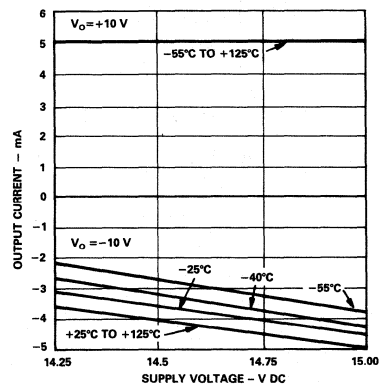


Figure 10. Output Current (mA) vs. Supply Voltage (V DC) and Temperature (°C), with V_{ISO} Loaded at 5 mA

Rated Output. The rated output voltage, across the OUT HI and OUT LO terminals, for the AD203SN is specified at ±10 V. This specification applies when the AD203SN is powered by a +15 V dc supply. The rated output voltage level is, however, affected by the input power supply voltage and the loads placed on the isolated power supply. This dependency is illustrated in Figure 9.

The current delivered by the output terminals of the AD203SN will vary as a function of the supply voltage and operating temperature. These relationships are illustrated in Figure 10.

Isolated Power. The load characteristics of the AD203SN's isolated power supplies (i.e., +15 V dc and −15 V dc) are plotted in Figure 11.

The isolated power supply exhibits some ripple which varies as a function of the load current. Figure 12 demonstrates this relationship. The AD203SN has internal bypass capacitors that optimize the tradeoff between output ripple and power supply performance, even under full load. If a specific application requires more bypassing on the isolated power supplies, external capacitors may be added. Figure 13 plots the isolated power supply ripple as a function of external bypass capacitance under full load conditions (i.e., 5 mA).

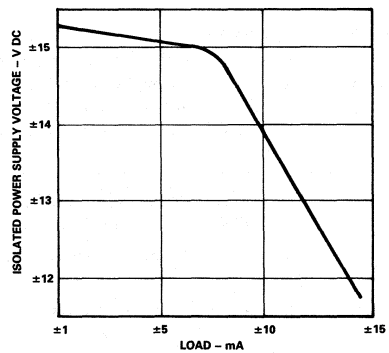


Figure 11. Isolated Power Supply Voltage (V DC) vs. Load (mA)

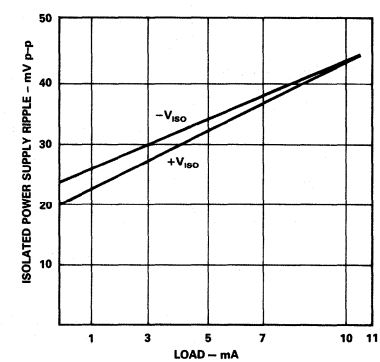


Figure 12. Isolated Power Supply Ripple (mV p–p) vs. Load (mA)

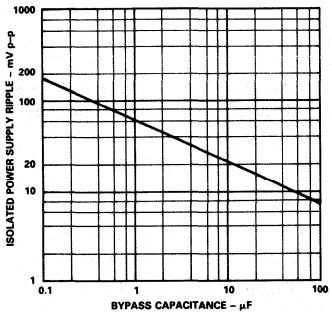


Figure 13. Isolated Power Supply Ripple (mV p–p) vs. Bypass Capacitance (µF), with a 5 mA Load on ±V_{ISO}, and Noise Bandwidth of 1 MHz.

The curves in Figures 12 and 13 were generated by measuring the power supply ripple over a 1 MHz bandwidth.

CAUTION: The AD203SN does not provide for short circuit protection of its isolated power supply. A current limiting resistor may be placed in series with the isolated power terminals and the load in order to protect the supply against inadvertent shorts.

APPLICABLE STANDARDS

The tests and methods employed in the design verification process are summarized in Table II. A copy of the *AD203SN Quality & Reliability Summaries* test report, which documents the results of the tests listed in Table II, is available on request.

Test Method	Test Description
MIL-STD-883C, Method 1004	Moisture Resistance
MIL-STD-883C, Method 1010 Condition B	Temperature Cycling, −55°C to +125°C
MIL-STD-883C, Method 2002, Condition B	Mechanical Shock @ 1,500 g for 0.5 ms
MIL-STD-883C, Method 2003	Solderability of Terminations
MIL-STD-883C, Method 2004	Integrity of Microelectronic Device Leads
MIL-STD-883C, Method 2007, Condition A	Variable Frequency Vibration @ 20 g
MIL-STD-883C, Method 2015	Resistance to Solvents
MIL-STD-883C, Method 3015.5	Electrostatic Discharge Sensitivity Classification
Analog Devices Product Reliability Program	MTBF Calculation (per MIL-HDBK-217D) and Verification

Table II. Tests Used to Verify the Ruggedness, Reliability and Quality of the AD203SN Design

Per 883C Method 3015.5, the AD203SN has been classified as a Class 2 ESD (electrostatic discharge) sensitive device. As a Class 2 device, the AD203SN is insensitive to static discharge voltages of less than 2000 V.

INSIDE THE AD203SN

The functional block diagram of the AD203SN is shown in Figure 14. The AD203SN employs amplitude modulation techniques to implement transformer coupling of signals down to dc.

The 35 kHz, 30 V p–p square wave carrier used by the AD203SN is generated by an internal oscillator located in the output port of the isolator. This oscillator is powered by a +15 V dc supply.

A full wave modulator translates the input signal to the carrier frequency which is then transmitted across transformer T1. The synchronous demodulator in the output port extracts the input signal from the carrier. The 12 kHz two-pole filter is employed to minimize output noise and ripple. Furthermore, the filter serves as a low impedance output buffer.

The input port of the AD203SN contains an uncommitted input op amp, a modulator and the power transformer T2. The primary of the power transformer is driven by the 35 kHz square wave while the secondary, in conjunction with a rectifier network, supplies isolated power to the modulator, input op amp and any external load. The uncommitted input amplifier can be used to supply gain or to buffer the input signals.

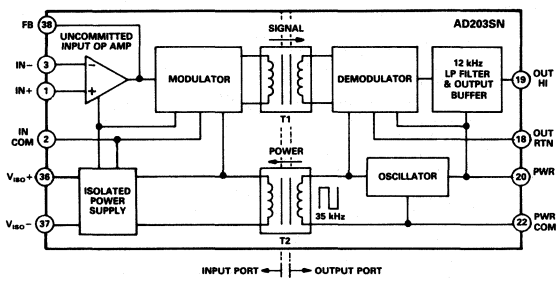


Figure 14. Functional Block Diagram

USING THE AD203SN

Powering the AD203SN. The AD203SN requires only a single +15 V dc power supply connected as shown in Figure 15. A bypass capacitor is provided in the module.

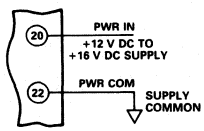


Figure 15. Powering the AD203SN

Unity Gain Input Configuration. The basic unity gain configuration for input signals of up to ±10 V is shown in Figure 16.

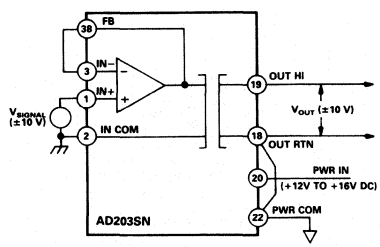


Figure 16. Basic Unity Gain Configuration

Input Configuration for a Gain Greater Than 1 (G>1). When small input signal levels must be amplified and isolated, Figure 17 shows how to get a gain greater than 1 while continuing to preserve a very high input impedance.

In this circuit, the gain equation may be written as:

$$V_O = (1 + R_F/R_G) \times V_{SIG}$$

where

V_O = Output Voltage (V)
V_{SIG} = Input Signal Voltage (V)
R_F = Feedback Resistor Value (Ω)
R_G = Gain Resistor Value (Ω).

Note on the 100 pF Capacitor. Whenever a gain of 50 V/V or greater is required, a 100 pF capacitor from the FB (input op amp feedback) terminal to the IN COM (input common) terminal, as shown with the dotted lines in Figure 17, is highly recommended. The capacitor acts to filter out switching noise and will minimize the isolator's nonlinearity parameter.

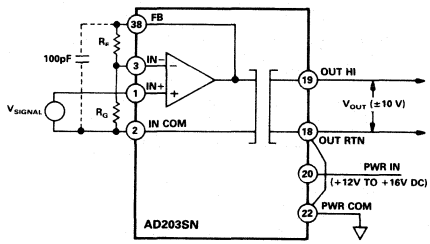


Figure 17. Input Configuration for a Gain Greater than 1

Compensating the Uncommitted Input Op Amp. The open loop gain and phase versus frequency for the uncommitted input op amp are given in Figure 18. These curves are to be used to determine the appropriate values for the feedback resistor and compensation capacitor in order to ensure frequency stability when a gain greater than unity is required. The final values for these components should also be chosen so as to satisfy the following constraints:

- The current drawn in the feedback resistor (R_F) is no greater than 1 mA.
- The feedback (R_F) and gain resistor (R_G) result in the desired amplifier gain.

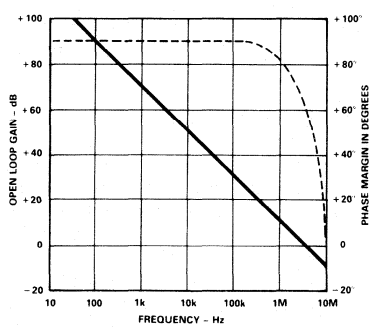


Figure 18. Open Loop Gain and Phase vs. Frequency for the Uncommitted Input Op Amp

Summing or Current Input Configuration. Figure 19 shows how the AD203SN can accommodate current inputs or sum currents or voltages.

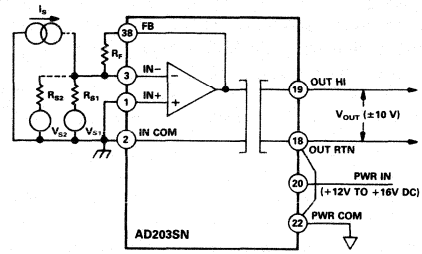


Figure 19. Input Configuration for Summing or Current Input

In this circuit the output voltage equation can be written as:

$$V_O = -R_F \times (I_S + V_{S1}/R_{S1} + V_{S2}/R_{S2} + \ldots)$$

where

V_O = Output Voltage (V)
V_{S1} = Voltage of Input Signal 1 (V)
V_{S2} = Voltage of Input Signal 2 (V)
I_S = Input Current Source (A)
R_F = Feedback Resistor Value (Ω)
R_{S1} = Source Resistance Associated with Input Signal 1 (Ω)
R_{S2} = Source Resistance Associated with Input Signal 2 (Ω).

The circuit of Figure 19 can also be used when the input signal is larger than the ±10 V input range of the isolator. For example, suppose that in Figure 19 only V_{S1}, R_{S1} and R_F are connected to the feedback, input and common terminals as shown by the solid lines in Figure 19. Now, a V_{S1} with a ±100 V span can be accommodated with $R_F = 20$ kΩ and a total $R_{S1} = 200$ kΩ.

GAIN AND OFFSET ADJUSTMENTS

General Comments. When gain and offset adjustments are required, the actual compensation circuit ultimately utilized will depend on:

- The input configuration mode of the isolation amplifier (i.e., noninverting or inverting).
- The placement of the adjusting potentiometer (i.e., on the isolator's input or output side).

As a general rule:

- Offset adjustments are best accomplished on the isolator's input side, as it is much easier and more efficient to null the offset ahead of any gain.
- Gain adjustments are mostly easily accomplished as part of the gain-setting resistor network at the isolator's input side.
- Input adjustments, of the offset and/or gain, are preferred when the adjusting potentiometers are as near as possible to the input end of the isolator (so as to minimize strays).
- Output side adjustments may be necessary under the conditions where adjusting potentiometers placed on the input side would present a hazard to the user due to the presence of high common mode voltages during the adjustment procedure.

- It is recommended that the offset adjustment precedes the gain adjustment.

Adjustments for the Noninverting Mode of Operation
Offset Adjustment. Figure 20 shows the suggested input adjustment connections when the isolator's input amplifier is configured for the noninverting mode of operation. The offset adjustment circuit injects a small voltage in series with the low side of the signal source. The adjustment potentiometer P1 modulates the injection voltage and is therefore responsible for nulling out the offset voltage.

Note: • To minimize CMR degradation it is recommended that the resistor in series with the input LO (i.e., R_C) be below a few hundred ohms.

• The offset adjustment circuit of Figure 20 will not work if the signal source has another current path to input common, or if current flows in the signal source LO lead. If this is the case, use the output adjustment procedure.

Gain Adjustment. Figure 20 also shows the suggested gain adjustment circuit. Note that the gain adjustment potentiometer P2 is incorporated into the gain-setting resistor network at the isolator's input.

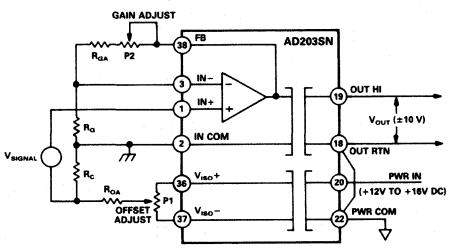


Figure 20. Input Adjustments for the Noninverting Mode of Operation

An R_{GA} of 47.5 kΩ and a 5 kΩ potentiometer, resulting in a median R_F value of 50 kΩ (i.e., R_{GA} + P2/2), will work nicely for gains of 10 V/V or greater. The gain adjustment becomes less effective at lower gains, in fact it is halved at G = 2 V/V, so that potentiometer P2 will have to be a larger fraction of the total R_F. At a gain of 1 V/V attempting to adjust the gain downwards will compromise the isolator's input impedance. In this case it would be better to adjust the gain at the signal source or after the output.

Input Adjustments for the Inverting Mode of Operation
Offset Adjustment. Figure 21 shows the suggested input adjustment connections when the isolator's input amplifier is configured for the inverting mode of operation. Here the offset adjustment potentiometer P1 nulls the voltage at the summing node. This method is preferred over current injection since it is less affected by any subsequent gain adjustments.

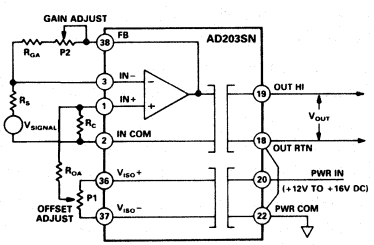


Figure 21. Input Adjustments for the Inverting Mode of Operation

Gain Adjustment. Figure 21 also shows the suggested gain adjustment circuit. In this circuit, the gain adjustment is made in the feedback loop using potentiometer P2. The adjustments will be effective for all gains in the 1 to 100 V/V range.

Output Adjustments
Offset Adjustment. Figure 22 shows the recommended technique for offset adjustment at the output. In this circuit, the ±15 V dc voltage is supplied by an independent source. With reference to the output circuitry shown in Figure 22, the maximum offset adjustment range is given by:

$$E_{OFFSET} = \frac{R_D \times V_S}{R_D + R_O}$$

where, V_S is the power supply voltage. A 20 kΩ potentiometer (P_O) should work well in this adjustment circuit.

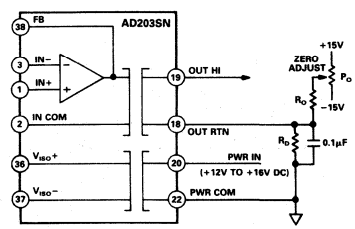


Figure 22. Output Side Offset Adjustment Circuit

Gain Adjustment. Since the AD203SN's output amplifier is fixed at unity, any desired output gain adjustments can only be made in a subsequent stage.

USING ISOLATED POWER

The AD203SN provides ±15 V dc power outputs referred to the input common. These may be used to power various accessory circuits which must operate at the input common mode level. The input offset adjustment circuits of the previous section are examples of this need.

The isolated power supply output has a current capacity of 5 mA which should be sufficient to operate adjustment circuits, references, op amps, signal conditioners and remote transducers.

CAUTION: The AD203SN does not provide for short circuit protection of its isolated power supply. A current limiting resistor may be placed in series with the isolated power terminals and the load in order to protect the supply against inadvertent shorts.

APPLICATIONS EXAMPLES

Isolated Process Current to Voltage Converter
Figure 23 shows how the AD203SN can be utilized as an isolated receiver that translates a 4-20 mA process current signal input into a 0 to +10 V output. The 25 Ω shunt resistor converts the 4-20 mA current into a +100 to +500 mV signal. The signal is then offset by −100 mV via the use of P_O to produce a 0 to +400 mV input. The signal is then amplified by a gain of 25 resulting in the desired 0 to +10 V output. With an open circuit on the input side, the AD203SN will have −2.5 V on the output, corresponding to the −100 mV offset voltage multiplied by a gain of 25 V/V.

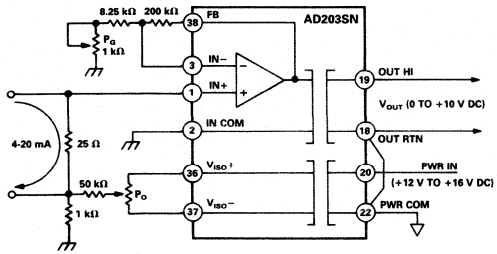


Figure 23. Using the AD203SN as an Isolated Process Current to Voltage Converter

For the circuit of Figure 23, the input to output transfer function can be expressed as:

$$V_{OUT} = 625 \times I_{IN} - 2.5\ V$$

where

V_{OUT} = Output Voltage (V)
I_{IN} = Input Current in milliamps (mA). This current is limited to the 4 to 20 mA range.

Current Shunt Measurements

In addition to isolating and converting process current signals into voltage signals, the AD203SN can be used to indicate the value of any loop current in general. Figure 24 illustrates a typical current shunt measurement application of the AD203SN. A small sensing resistor R_{SHUNT}, placed in series with the current loop, develops a small differential voltage that may be further scaled to provide an isolator output voltage that is directly proportional to the current. The voltage developed across the shunt can potentially be several hundred to a thousand volts above ground. In this circuit, the AD203SN provides the necessary scaling of the shunt signal while providing high common-mode voltage isolation and high common mode rejection of dc and 60 Hz components.

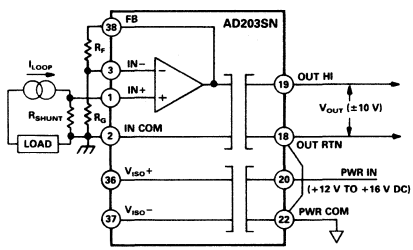


Figure 24. Using the AD203SN for Current Shunt Measurements

The transfer function for the circuit of Figure 24 can be written as:

$$V_{OUT} = R_{SHUNT} \times (1 + R_F/R_G) \times I_{LOOP}$$

where

V_{OUT} = Output Voltage (V)
R_{SHUNT} = Sense or Current Shunt Resistance (Ω)
R_F = Feedback Resistance (Ω)
R_G = Gain Resistance (Ω)
I_{LOOP} = Loop Current (A).

Low Level Inputs

In applications where low level signals need to be isolated (thermocouples are one such application), a low drift input amplifier can be used with the AD203SN. Figure 25 illustrates this implementation of the AD203SN. The circuit design also includes a three-pole active filter which provides for enhanced common mode rejection at 60 Hz and normal mode rejection of frequencies above a few Hz. If any offset adjustments are desired, they are best done at the trim pins of the low drift input amplifier. Gain adjustments can be done at the feedback resistor.

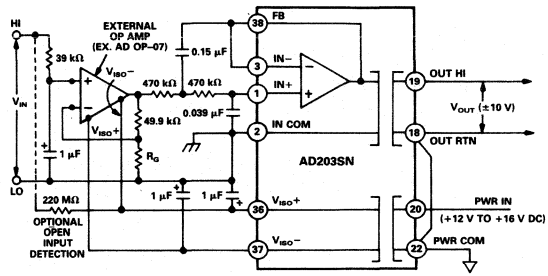


Figure 25. Using the AD203SN with Low Level Inputs

The input-output relationship for the circuit shown in Figure 25 can be written as:

$$V_{OUT} = V_{IN} \times (1 + 50\ k\Omega/R_G)$$

where

V_{OUT} = Output Voltage (V)
V_{IN} = Low Level Input Voltage (V)
R_G = Isolation Amplifier Gain Resistance (Ω).

Noise Reduction in Data Acquisition Systems

The AD203SN uses amplitude modulation techniques with a 35 kHz carrier to pass both ac and dc signals across the isolation barrier. Some of the carrier's harmonics are unavoidably passed through to the isolator output in the form of ripple. In most cases, this noise source is insignificant when compared to the measured signal. However, in some applications, particularly when a fast A/D converter is used following the isolator, it may be desirable to add filtering at the isolator's output in order to reduce the carrier ripple. Figure 26 shows a circuit that will reduce the carrier ripple through the use of a two-pole output filter.

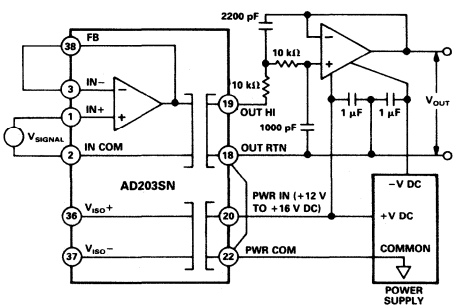


Figure 26. Noise Reduction in Data Acquisition Systems Using the AD203SN

5

ANALOG DEVICES

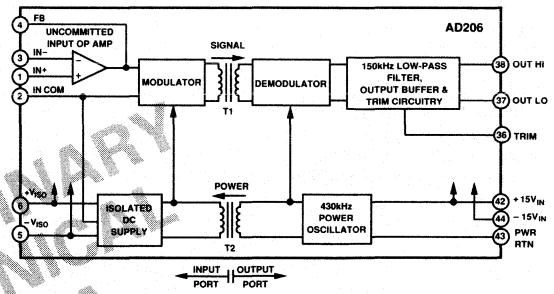
100 kHz Bandwidth, Low Distortion, Internally Powered Isolation Amplifier

AD206

FEATURES
Wide Bandwidth: 100 kHz, min (Full Power)
Rapid Slew Rate: 6 V/μs
Fast Settling Time: 9 μs
Low Harmonic Distortion: −80 dB @ 1 kHz
Low Nonlinearity: ±0.005%
Wide Output Range: ±10 V, min
High Isolation: 1.5 kV rms (B Grade)
Buffered Output
Isolated Power: ±15 V dc @ ±10 mA
Performance Rated over −40°C to +85°C

APPLICATIONS INCLUDE
High Speed Data Acquisition Systems
Transient Monitoring
Power Line Monitoring
Power Supply Control
Vibration Analysis

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

5

GENERAL DESCRIPTION

The AD206 is a high speed, two-port, transformer-coupled isolation amplifier expressly designed for applications that require the amplification and isolation of wideband analog signals. The innovative circuit and transformer design of the AD206 ensures the wideband dynamic characteristics of the AD206 while preserving key dc performance specifications.

The AD206 provides total galvanic isolation between the input and output stages of the isolation amplifier, including the input and output power supplies, through the use of internal transformer coupling. The functionally complete design of the AD206, powered by a bipolar ±15 V dc supply, eliminates the need for a user-supplied isolated dc/dc converter. This permits the designer to minimize the necessary circuit overhead and, consequently, reduce the overall system design and component costs.

The design of the AD206 emphasizes maximum flexibility and ease of use in a broad range of applications where fast analog signals must be measured and transmitted under high common-mode voltage (CMV) conditions. The AD206 has a ±10 V input/output range, a specified gain range of 1 to 10, a buffered output and a front-end power supply of ±15 V dc with ±10 mA of current drive capability.

PRODUCT HIGHLIGHTS

High Speed Dynamic Characteristics: The AD206 features a minimum full power bandwidth of 100 kHz, a typical rise time of 3 μs, and settling time of 9 μs. The high speed performance of the AD206 allows the amplification and isolation of dynamic signals.

Flexible Input and Buffered Output Stages: An uncommitted op amp is provided on the input stage of the AD206. This allows for input buffering and gain as needed. The AD206 also features a buffered output stage, allowing it to drive low impedance loads.

High Accuracy: Exhibiting a typical nonlinearity of ±0.005% (B grade) of full-scale range and a total harmonic distortion of −80 dB (typical @ 1 kHz), the AD206 provides high isolation without loss of signal integrity and quality.

Excellent Common-Mode Performance: The AD206BY (AD206AY) provides 1.5 kV rms (0.75 kV rms) of common-mode protection. Both grades feature a low common-mode capacitance of 4.5 pF, inclusive of power isolation, resulting in a typical common-mode rejection specification of 105 dB (1 kΩ source impedance imbalance) as well as a low leakage current of 2.0 μA rms (max @ 240 V rms, 60 Hz).

Isolated Power: An unregulated isolated ±15 V dc power supply with ±10 mA of current drive capability is available at the input port of the AD206. This permits the isolator to power up floating signal conditioners, front-end amplifiers or remote transducers at the input.

Performance Rated over the −40°C to +85°C Temperature Range: With an extended industrial temperature range rating, the AD206 is an ideal isolation amplifier for use in industrial environments.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

AD206—SPECIFICATIONS (typical @ +25°C, V_S = ±15 V dc, 2 kΩ output load, unless otherwise noted)

	AD206A	AD206B
GAIN		
Range[1]	1 V/V to 10 V/V	*
Error @ Unity Gain	±2%, max	*
vs. Temperature[2]		
0 to +85°C	+15 ppm/°C	*
−40°C to 0°C	+50 ppm/°C	*
vs. Supply Voltage, ± (14.5 V to 16.5 V dc)	100 ppm/V	*
vs. Isolated Supply Load[3]	20 ppm/mA	*
Nonlinearity,[4] ±10 V Output Swing, G = 1 V/V	±0.01% (±0.025%, max)	±0.005%, (±0.015%, max)
G = 10 V/V	±0.025%	±0.01%
INPUT VOLTAGE RATINGS		
Input Voltage Rating of the Uncommitted Input Op Amp, G = 1 V/V	±10 V, min	*
Max Safe Differential Range, IN+/IN− to IN COM	±15 V	*
Common Mode Rejection Ratio of Input Op Amp	100 dB	*
Max Isolation Voltage (Input to Output)[5]		
AC, 60 Hz	750 V rms	1500 V rms
	±1000 V_{PEAK}	±2000 V_{PEAK}
Isolation-Mode Rejection Ratio (IMRR) @ 60 Hz		
R_S ≤ 100 Ω (HI & LO Inputs), G = 1 V/V	120 dB	*
R_S ≤ 1 kΩ (Input, HI, LO or Both), G = 1 V/V	105 dB	*
Isolation-Mode Rejection Ratio (IMRR) @ 1 kHz		
R_S ≤ 100 Ω (HI & LO Inputs), G = 1 V/V	100 dB	*
R_S ≤ 1 kΩ (Input, HI, LO or Both), G = 1 V/V	85 dB	*
Isolation-Mode Rejection Ratio (IMRR) @ 10 kHz		
R_S ≤ 100 Ω (HI & LO Inputs), G = 1 V/V	80 dB	*
R_S ≤ 1 kΩ (Input, HI, LO or Both), G = 1 V/V	65 dB	*
Leakage Current, Input to Output, @ 240 V rms, 60 Hz	2 μA rms, max	*
INPUT IMPEDANCE		
Differential (G = 1 V/V)	16 MΩ	*
Common Mode	2 GΩ‖4.5 pF	*
INPUT OFFSET VOLTAGE		
Initial @ +25°C	±400 μV (±2 mV, max)	*
vs. Temperature		
0 to +85°C	±2 μV/°C (±15 μV/°C, max)	*
−40°C to 0°C	±20 μV/°C	*
OUTPUT OFFSET VOLTAGE		
Initial @ +25°C (Adjustable to Zero)[6]	−45 mV (0 to −80 mV, max)	*
vs. Temperature		
0 to +85°C	±30 μV/°C	*
−40°C to 0°C	±80 μV/°C	*
vs. Supply Voltage	±350 μV/V	*
vs. Isolated Supply Load[3]	−35 μV/mA	*
INPUT BIAS CURRENT		
Initial @ +25°C	300 nA (650 nA, max)	*
vs. Temperature		
−40°C to +85°C	±800 nA, max	*
INPUT DIFFERENCE CURRENT		
Initial @ +25°C	3 nA (±65 nA, max)	*
vs. Temperature		
−40°C to +85°C	±800 nA, max	*
INPUT VOLTAGE NOISE		
Frequency > 10 Hz	20 nV/$\sqrt{Hz}$	*

PRELIMINARY TECHNICAL DATA

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	AD206A	AD206B
DYNAMIC RESPONSE (2 kΩ load)		
Full Signal Bandwidth (3 dB Corner, G = 1 V/V, 20 V pk–pk Signal)	110 kHz (100 kHz, min)	*
DYNAMIC RESPONSE		
Small Signal Bandwidth (3 dB Corner, G = 1 V/V, 100 mV pk–pk Signal)	115 kHz	*
Transport Delay	2.2 μs[6]	*
Slew Rate	6 V/μs	*
Rise Time (10% to 90%)	3 μs	*
Settling Time to ±0.10% on a 10 V Step	9 μs	*
Overshoot	1%	*
Harmonic Distortion Components, @ 1 kHz	−80 dB	*
@ 10 kHz	−65 dB	*
Unity Gain Overload Recovery (±15 V Drive)	5 μs	*
Output Overload Recovery Time (G > 5 V/V)	10 μs	*
RATED OUTPUT		
Voltage (Out HI to Out LO)	±10 V, min	*
Current	±5 mA, min (into 2 kΩ Load)	*
Maximum Capacitive Load	1,000 pF	*
Output Resistance	1 Ω, max	*
Output Ripple and Noise,[8] 1 MHz Bandwidth	10 mV pk–pk	*
50 kHz Bandwidth	2.5 mV pk–pk	*
ISOLATED POWER OUTPUT[9]		
Voltage, No Load	±15 V(−5%, +15%)	*
vs. Temperature, 0 to +85°C	+20 mV/°C	*
−40°C to 0°C	+25 mV/°C	*
Current with Rated Supply Voltage Range[3, 10]	±10 mA	*
Regulation, No Load to Full Load	−90 mV/mA	*
Line Regulation	290 mV/V	*
Ripple, 1 MHz Bandwidth, No Load[3]	50 mV rms	*
Efficiency	75%	*
POWER SUPPLY		
Supply Voltage for Rated Performance	±14.5 V dc to ±16.5 V dc	*
Voltage, Operating[11]	±14.25 V dc to ±17 V dc	*
Current, Quiescent	+40 mA/−18 mA	*
TEMPERATURE RANGE		
Rated Performance	−40°C to +85°C	*
Storage	−40°C to +85°C	*
PACKAGE DIMENSIONS		
SIP Package	2.475″ × 0.3250″ × 0.840″, max	*
	62.9 mm × 8.3 mm × 21.3 mm, max	*

PRELIMINARY TECHNICAL DATA

5

NOTES

[1]The gain range of the AD206 is specified from 1 to 10 V/V. The AD206 can also be used with gains of up to 100 V/V. With a gain of 100 V/V there is a 20% reduction in the 3 dB bandwidth specification, and the nonlinearity degrades to ±0.02% (typ). Refer to Figure 12 for a description on how to implement a gain of 100 using the AD206.

[2]The gain temperature coefficient for the AD206 is illustrated over the entire −40°C to +85°C rated performance temperature range in Figure 1.

[3]When the isolated supply load exceeds ±1 mA, external filter capacitors are required in order to ensure that the gain, offset and nonlinearity specifications are preserved and to maintain the isolated supply full-load ripple below the specified 50 mV rms. A value of 6.8 μF is recommended as shown in Figures 18 and 19b.

[4]Nonlinearity is specified as a percent (of full-scale range) deviation from a best straight line.

[5]The isolation rating of each AD206 is 100% tested in production. The A grade is Hi-Pot tested at 850 V rms for 1 minute. The B grade is tested using a 5 second partial discharge test at 1,800 V rms with a detection threshold of 150 pC.

[6]The AD206 should be allowed to warm-up for approximately 10 minutes before any gain and offset adjustments are made.

[7]Equivalent to a 0.8° phase shift at 1 kHz.

[8]With the ±15 V dc power supply pins bypassed by 2.2 μF capacitors at the AD206 pins, as shown in Figures 10 and 19a.

[9]CAUTION: The AD206 design does not provide short circuit protection of its isolated power supply. A current-limiting resistor may be placed in series with the isolated power terminals and the load in order to protect the supply against inadvertent shorts.

[10]With an input power supply voltage greater than or equal to ±15 V dc the AD206 may supply up to ±15 mA of current from the isolated power supplies. Exceeding these currents will increase the dependence of the gain and offset specifications of the AD206 on both the supply voltage and isolated load current.

[11]Voltages less than 14.25 V dc may cause the AD206 to cease operating properly. Voltages greater than 17.5 V dc may damage the internal components of the AD206 and consequently should not be used.

*Specification is the same as that for the AD206A.

Specifications subject to change without notice.

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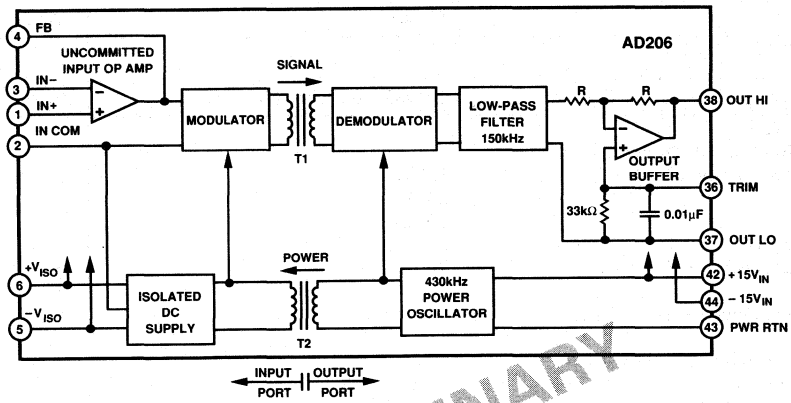


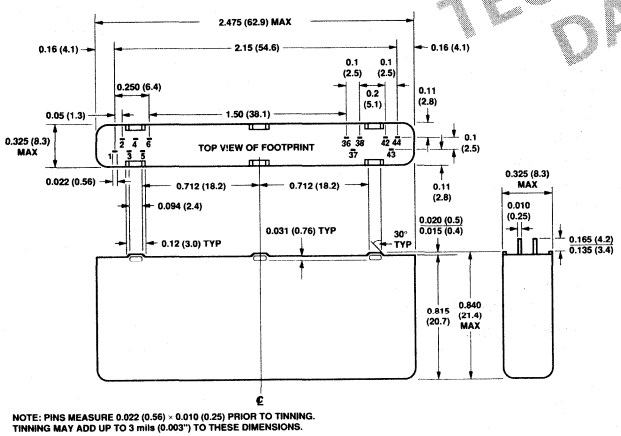
Functional Block Diagram

PRELIMINARY TECHNICAL DATA

OUTLINE DIMENSIONS

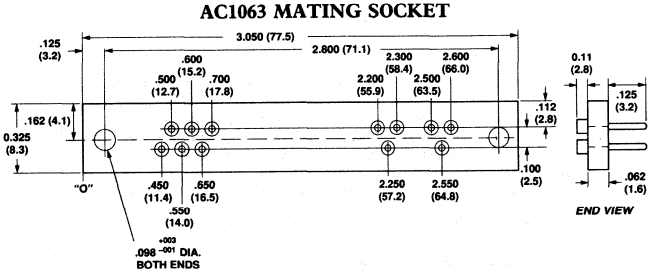
Dimensions shown in inches and (mm).

AD206 SIP PACKAGE



NOTE: PINS MEASURE 0.022 (0.56) × 0.010 (0.25) PRIOR TO TINNING. TINNING MAY ADD UP TO 3 mils (0.003") TO THESE DIMENSIONS.

AC1063 MATING SOCKET



AD206 PIN DESIGNATIONS

Pin	Designation	Function
1	IN+	Input Op Amp: Noninverting Input
2	IN COM	Input Common
3	IN–	Input Op Amp: Inverting Input
4	FB	Input Feedback
5	$-V_{ISO}$ OUT	Isolated Power: –DC
6	$+V_{ISO}$ OUT	Isolated Power: +DC
36	TRIM	Output Offset Trim Adjustment
37	OUT LO	Output Low
38	OUT HI	Output High
42	+15 V IN	DC Power Supply Input: +15 V
43	PWR RTN	DC Power Supply Input Common
44	–15 V IN	DC Power Supply Input: –15 V

ORDERING GUIDE

Model	Temperature Range
AD206AY	–40°C to +85°C
AD206BY	–40°C to +85°C

CAUTION

ESD (electrostatic discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

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INSIDE THE AD206

The functional block diagram of the AD206 has been shown. The AD206 employs a double balanced amplitude modulation technique to implement transformer coupling of signals down to dc. The 430 kHz square wave carrier used by the AD206 is generated by an internal oscillator located on the output side of the isolator. This oscillator is powered by the bipolar 15 V dc supply.

The input port of the AD206 contains an uncommitted input op amp, a modulator and an isolated power supply. The uncommitted input amplifier may be used to supply gain or to buffer the input signals. The primary windings of the power transformer T2 are driven by the 430 kHz square wave while the secondary, in conjunction with a rectifier network, supply isolated power to the modulator, input op amp and any external load.

A full-wave modulator translates the input signal to the carrier frequency which is then transmitted across the signal transformer T1. The synchronous demodulator on the output port extracts the input signal from the carrier. This signal is then passed through a Bessel response low-pass filter to an output buffer and is then made available at the output signal terminals.

PERFORMANCE CHARACTERISTICS

PRELIMINARY TECHNICAL DATA

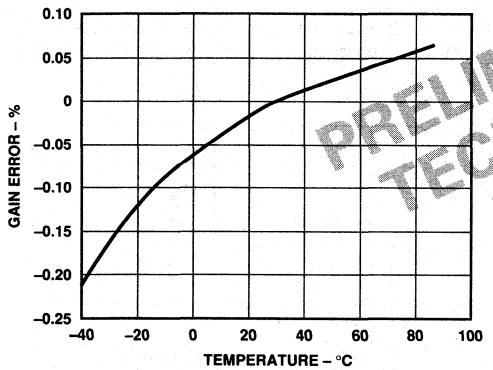

Figure 1. Gain Error vs. Temperature

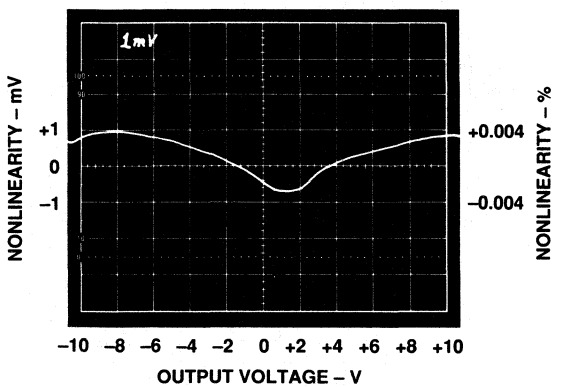

Figure 2. Gain Nonlinearity Error (% of Output Span and mV) vs. Output Voltage Swing for a Gain of 1

Nonlinearity does not change with temperature over the −40°C to +85°C range and is not dependent on the gain setting for gains in the rated 1 V/V to 10 V/V range.

Note: The gain and offset and offset errors will increase when the isolated power supply load exceeds ±10 mA.

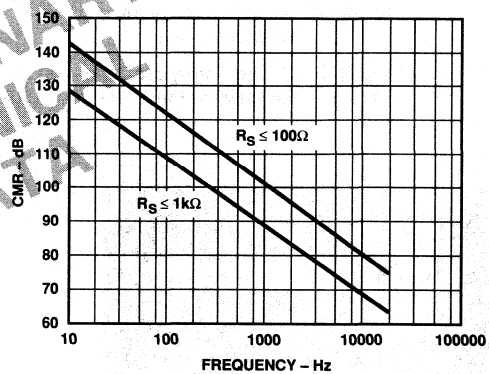

Figure 3. Typical Common-Mode Rejection (dB) vs. Common-Mode Signal Frequency (Hz) and Source Impedance Imbalance (Ω) for the 10 Hz to 20 kHz Frequency Range and with a Gain of 1

To achieve the optimal common-mode rejection of unwanted signals, it is strongly recommended that the source impedance imbalance be kept as low as possible and that the input circuitry be carefully laid out so as to avoid adding excessive stray capacitances at the isolator's input terminals.

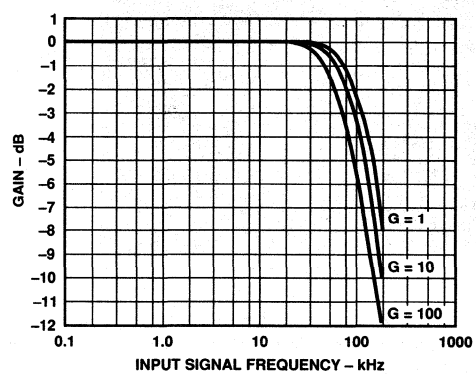

Figure 4. Normalized Gain (dB) as a Function of Input Signal Frequencies (kHz) in the 100 Hz to 150 kHz Range

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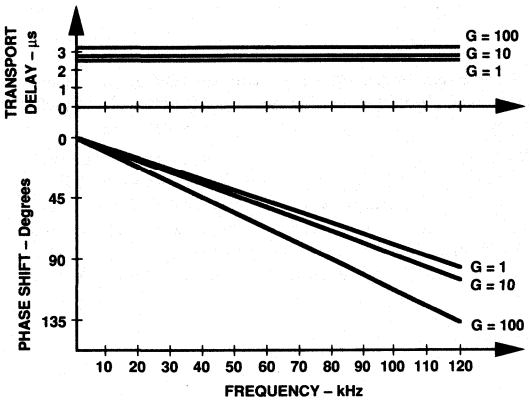

Figure 5. Phase Shift (°) and Transport Delay (µs) vs. Input Signal Frequencies (kHz) in the 10 Hz to 120 kHz Range

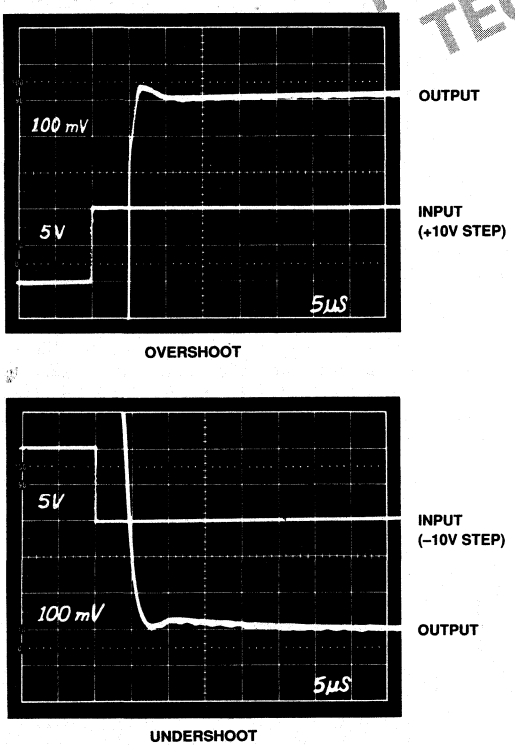

Figure 6. Overshoot/Undershoot Characteristics of the AD206 to a Full-Scale Step at the Isolator's Input and with a Gain of 1 (R_L = 2 kΩ)

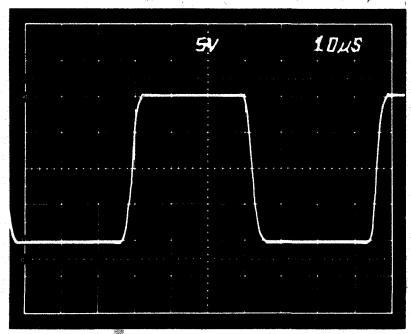

Figure 7. Output Response of the AD206 to a + and – Full-Scale Step at the Isolator's Input, with a Gain of 1 (R_L = 2kΩ)

PRELIMINARY TECHNICAL DATA

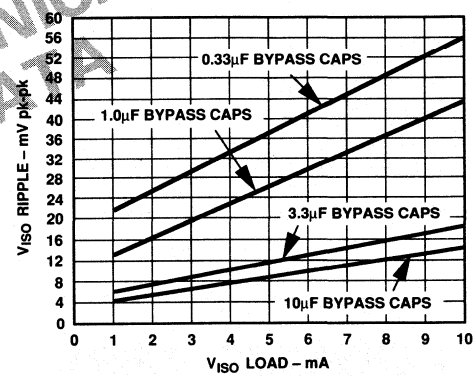

Figure 8. Isolated Power Supply Ripple (mV pk–pk) vs. Load (mA) and Bypass Capacitance (µF)

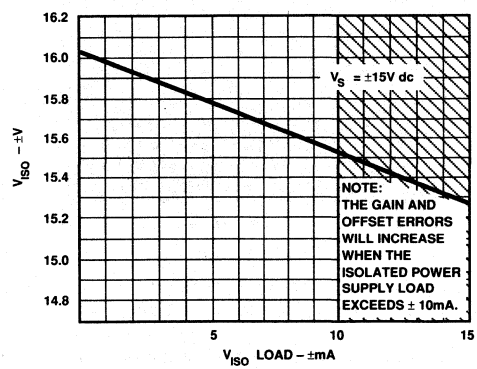

Figure 9. Isolated Power Supply Voltage (V dc) vs. Isolated Power Supply Load (mA)

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POWERING THE AD206

The AD206 is powered by a bipolar ±15 V dc power supply connected as shown in Figure 10. External bypass capacitors should be provided in bused applications. Note that a small signal-related current (50 μA/V_{OUTPUT}) will flow out of the OUT LO pin (Pin 37). Therefore, the OUT LO terminals should be bused together and referenced at a single "Analog Star Ground" to the ±15 V dc supply common as illustrated in Figure 10.

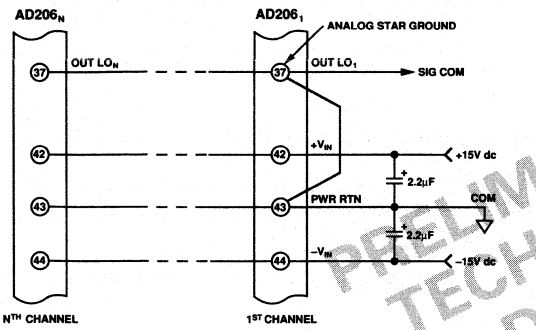

Figure 10. Powering the AD206

Power Supply Voltage Considerations. The rated performance of the AD206 remains unaffected for power supply voltages in the ±14.5 V dc to ±16.5 V dc range. Voltages below ±14.25 V dc may cause the AD206 to cease operating properly.

Note: Power supply voltages greater than 17.5 V dc may damage the internal components of the AD206 and consequently should not be used.

USING THE AD206

Unity Gain Input Configuration. The basic unity gain configuration for input signals of up to ±10 V is shown in Figure 11.

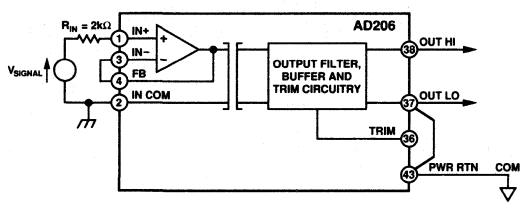

Figure 11. Basic Unity Gain Configuration

Noninverting Input Configuration for a Gain Greater Than One (G>1). When input signal levels must be amplified and isolated, Figure 12 shows how to achieve a gain greater than one while continuing to preserve a very high input impedance.

In this circuit, the gain equation is written as follows:

$$V_O = (1 + R_F/R_G) \times V_{SIG}$$

where:

V_O = Output Voltage (V),
V_{SIG} = Input Signal Voltage (V),
R_F = Feedback Resistor Value (Ω),
R_G = Gain Resistor Value (Ω).

The values for the resistors R_F and R_G are subject to the following constraints:

- The total impedance of the gain network should be less than 10 kΩ.
- The current drawn in the feedback resistor (R_F) is less than 1 mA at ±10 V. Note that for each mA drawn by the feedback resistor, the isolated power supply drive capability decreases by 1 mA.
- The feedback (R_F) and gain resistor (R_G) result in the desired amplifier gain.

Greater than One

It is recommended that the feedback resistor (R_F) is bypassed with a 47 pF capacitor (C_F).

Note on the input resistor (R_{IN}): The 2 kΩ resistor placed in series with the input signal source and the IN+ terminal, designated as R_{IN} in Figures 11 and 12, is recommended so as to limit the current seen at the input terminals of the AD206 to 5.0 mA when the AD206 is not powered.

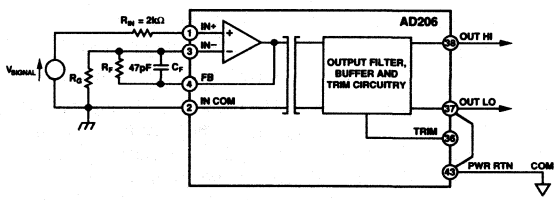

Figure 12. Noninverting Input Configuration for a Gain

Compensating the Uncommitted Input Op Amp. The open-loop gain and phase versus frequency for the uncommitted input op amp are given in Figure 13. These curves can be used to determine the appropriate values for the feedback resistor and compensation capacitor in order to ensure frequency stability when reactive or nonlinear components are used in conjunction with the uncommitted input op amp.

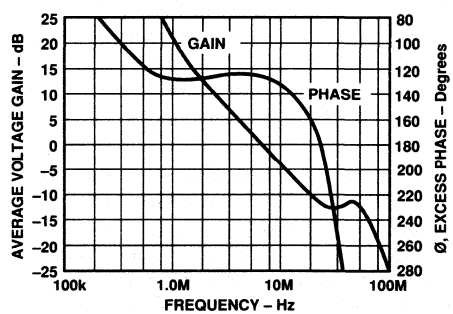

Figure 13. Open-Loop Gain and Phase Response for the Uncommitted Input Op Amp of the AD206

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Inverting, Summing or Current Input Configuration. Figure 14 shows how the AD206 can measure currents or sum currents or voltages.

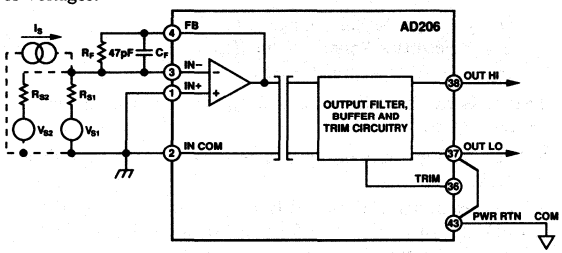


Figure 14. Summing or Current Input Configuration Noninverting Mode of Operation

For this circuit, the output voltage equation is written as follows:

$$V_O = -R_F \times (I_S + V_{S1}/R_{S1} + V_{S2}/R_{S2} + \ldots)$$

where:

V = Output Voltage (V),
V_{S1} = Voltage of Input Signal 1 (V),
V_{S2} = Voltage of input Signal 2 (V),
I_S = Input Current Source (A),
R_F = Feedback Resistor Value (Ω) (10 kΩ, typ)
R_{S1} = Source Resistance Associated with Input Signal 1 (Ω),
R_{S2} = Source Resistance Associated with Input Signal 2 (Ω).

The circuit of Figure 14 can also be used when the input signal is larger than the ±10 V input range of the isolator. For example, suppose that in Figure 14, only V_{S1}, R_{S1} and R_F are connected to the feedback, input and common terminals as shown by the solid lines in Figure 14. Now, a V_{S1} with a ±50 V span can be accommodated with R_F = 10 kΩ and a total R_{S1} = 50 kΩ.

GAIN AND OFFSET ADJUSTMENTS

General Comments. The AD206 features a TRIM pin on the output stage of the isolator. This pin should be used with user-supplied external circuitry to adjust the output offset of the AD206. When gain and offset adjustments are required, the actual compensation circuit ultimately used depends on the following:

- The input configuration mode of the isolation amplifier (i.e., noninverting or inverting).
- The placement of the adjusting potentiometer (i.e., on the isolator's input or output side).

As a general rule:

- Gain Adjustments are most easily accomplished as part of the gain-setting resistor network at the isolator's input side.
- To ensure the highest degree of stability in the gain adjustment, the adjusting potentiometers should be located as close as possible to the isolator's front end and its impedance should be kept low. Adjustment ranges should also be kept to a minimum since their resolution and stability is dependent on the actual trim potentiometers used.
- Output side adjustments may be necessary under the conditions where adjusting potentiometers placed on the input side would present a hazard to the user due to the presence of high common-mode voltages during the adjustment procedure.
- It is recommended that the offset is adjusted prior to the gain adjustment.
- The AD206 should be allowed to warm-up for approximately 10 minutes before any gain and/or offset adjustments are performed.

Input Gain Adjustments for the Noninverting Mode of Operation. Figure 15 shows the suggested gain adjustment circuit. Note that the gain adjustment potentiometer R_P is incorporated into the gain-setting resistor network at the isolator's input.

For a ±1% trim range ($R_P \approx 1$ kΩ), let $R_C \approx 0.02 \dfrac{R_G \times R_F}{R_G + R_F}$.

PRELIMINARY TECHNICAL DATA

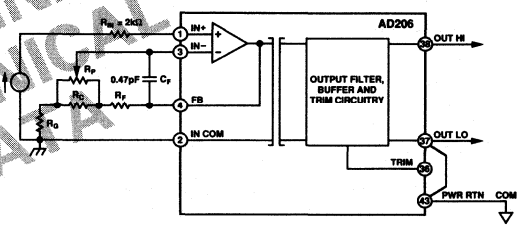


Figure 15. Input Gain Adjustment Circuit for the

Input Gain Adjustments for the Inverting Mode of Operation. Figure 16 shows the suggested gain adjustment circuit. In this circuit, the gain adjustment is made in the feedback loop using potentiometer R_P. The adjustments are effective for all gains in the 1 to 10 range.

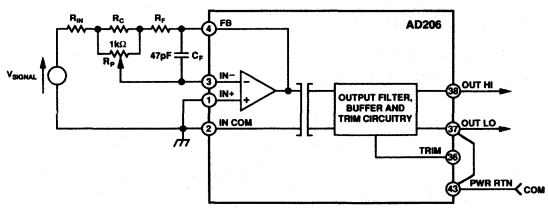


Figure 16. Input Gain Adjustment Circuit for the Inverting Mode of Operation

For an approximate ±1% gain trim range, let

$$R_X = \frac{R_{IN} \times R_F}{R_{IN} + R_F}$$

and select

$$R_C = 0.02 \times R_{IN}$$

while

$$R_F \leq 10\ k\Omega$$

$$C_F = 47\ pF$$

R_F and R_{IN} are selected for a good temperature coefficient match.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Output Offset Adjustments. Figure 17 illustrates one method of adjusting the output offset voltage. Since the AD206 exhibits a nominal output offset of −35 mV, the circuit shown in Figure 17 was chosen to yield an offset correction of 0 to +73 mV for a total output offset range of approximately −35 mV to +38 mV.

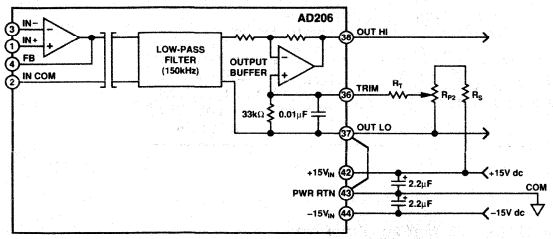


Figure 17. Output Offset Adjustment Circuit

Output Gain Adjustments. Since the output amplifier stage of the AD206 is fixed at unity, any desired output gain adjustments can be made only in a subsequent stage.

USING ISOLATED POWER

The AD206 provides ±15 V dc @ ±10 mA power outputs referred to the input common. These may be used to power various accessory circuits which must operate at the input common-mode level including input adjustment circuits, references, op amps, signal conditioners or remote transducers. Figure 18 shows the recommended connections from the isolated power supplies.

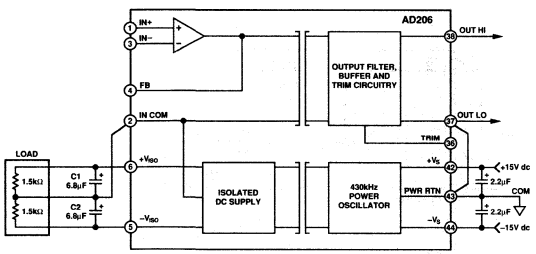


Figure 18. Using the Isolated Power Supplies

PCB LAYOUT FOR MULTICHANNEL APPLICATIONS

The pinout of the AD206 has been designed to facilitate multichannel applications. Figure 19a shows the recommended printed circuit board (PCB) layout for the simple unity gain configuration. When gain setting resistors are present, 0.325″ channel centers can still be achieved as shown in Figure 19b.

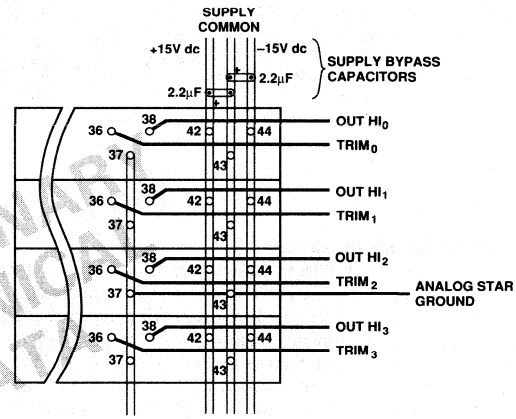


Figure 19a. PCB Layout for Multichannel, Unity Gain Applications

CAUTION: The AD206 design does not provide short-circuit protection of its isolated power supply. A current limiting resistor may be placed in series with the isolated power terminals and the load in order to protect the supply against inadvertent shorts.

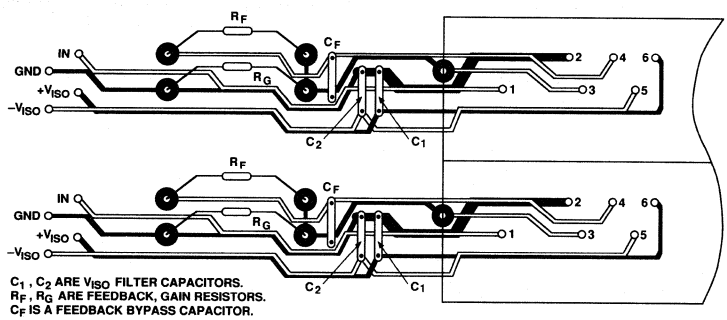


Figure 19b. PCB Layout for Multichannel with Gain Is Required on the AD206s

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

APPLICATION EXAMPLES

Motor Control. Figure 20 shows an AD206 used in a dc motor controller application. The excellent phase characteristics and wide bandwidth of the AD206 are ideal for this type of application.

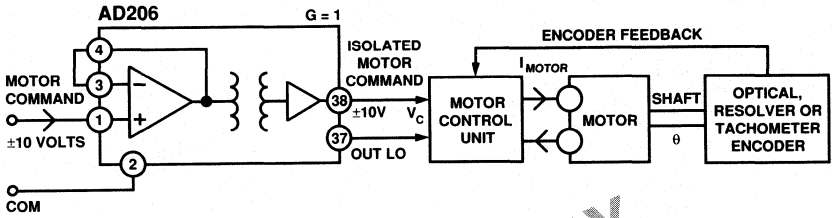


Figure 20. Using the AD206 in a Motor Control Application

Multichannel Data Acquisition

Figure 21 shows the AD206 in a multiplexed, multichannel data acquisition application. The rapid slew rate and settling time performance of the AD206 are ideal in satisfying the demanding signal processing requirements imposed by the sampling nature of the multiplexer output. These specifications ensure that the AD206 is capable of accurately acquiring an analog signal in a limited time period, with minimal signal attenuation and distortion, before the multiplexer switches to the next signal channel.

The current drive capabilities of the AD206's bipolar ±15 V dc isolated power supplies are more than adequate to meet the modest ±800 μA supply current requirements for the AD7502 multiplexer. Digital isolation techniques should be employed to isolate the Enable (EN), A0 and A1 logic control signals.

PRELIMINARY
TECHNICAL
DATA

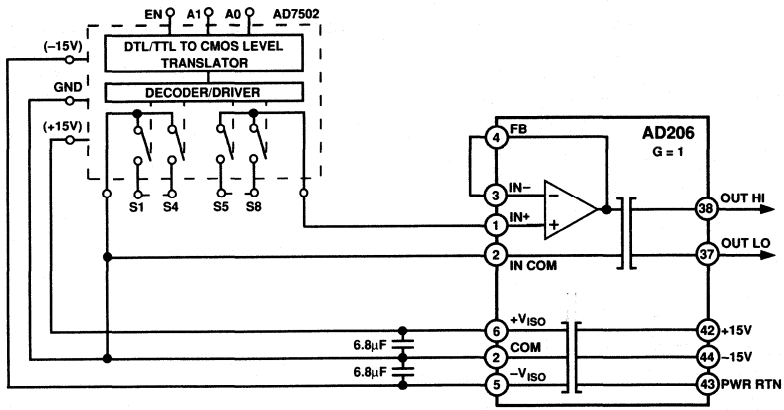


Figure 21. Using the AD206 in Multichannel Data Acquisition Applications

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

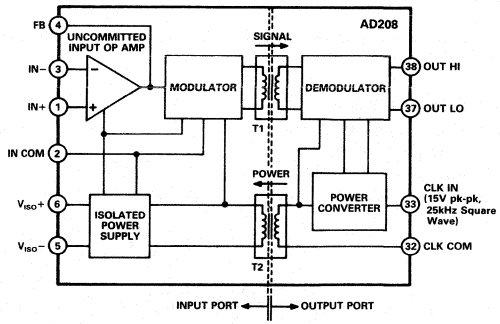
High Precision, Low Offset, mV Input Isolation Amplifier

AD208

FEATURES
Wide Gain Range: 1 to 1000 V/V
Low Nonlinearity: ±0.0125%
Low Input Offset Voltage: ±0.27 mV, max (G = 1000 V/V)
Low Offset Drift: ±1.5 μV/°C , max (G = 1000 V/V)
High CMV Isolation: 1.5 kV RMS (B Grade)
Isolated Power: ±8.0 V DC with up to ±5 mA
Completely Compatible with the AD204 SIP
Small SIP: 2.08" (52.8 mm) × 0.26" (6.6 mm) × 0.625" (15.9 mm)
Performance Rated over −40°C to +85°C

APPLICATIONS
Isolated RTD and Thermocouple Applications
mV Signal Amplification and Isolation
Process Instrumentation and Control
Multichannel Data Acquisition

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD208 is a high precision, two-port, transformer-coupled isolation amplifier expressly designed for applications that require the amplification and isolation of extremely low level (i.e., ±mV) signals. The innovative front-end circuit design of the AD208 ensures the low offset characteristics and stable high gain properties of the AD208. The AD208 is fully compatible with the SIP style packaging of Analog Devices' low cost AD204 family of isolation amplifiers.

The AD208 provides total galvanic isolation between the input and output stages of the isolation amplifier, including the power supplies, through the use of internal transformer coupling. The functionally complete design of the AD208, powered by an externally supplied 15 V pk–pk, 25 kHz clock or the recommended AD246 Clock Driver, eliminates the need for a user supplied dc/dc converter. This permits the designer to minimize the necessary circuit overhead and consequently reduce the overall design and component costs.

The design of the AD208 emphasizes maximum flexibility and ease of use in a broad range of applications where low level signals must be measured and transmitted under high CMV conditions. The AD208 has a ±5 V output range, an adjustable gain range of from 1 to 1,000 V/V and a front-end power supply of ±8.0 V dc with up to ±5 mA of current drive capability.

PRODUCT HIGHLIGHTS

Wide Gain Range. The AD208 features a wide adjustable gain range of from 1 to 1,000 V/V. The stable high gain properties of the AD208 allow for the amplification and isolation of signals in the ±mV range.

Flexible Input Stage. An uncommitted op amp is provided on the input stage of the AD208. This allows for input buffering and gain as needed. It also facilitates a host of alternative input functions including filtering, summing, high voltage ranges and current inputs.

High Accuracy. Exhibiting a typical nonlinearity of ±0.0125% and a low gain temperature coefficient, averaging ±35 ppm/°C over the rated temperature range, the AD208 provides high isolation without loss of signal integrity and quality.

Low Offset Characteristics. With a maximum initial offset of ±(0.25 + 15 /G)mV and a maximum offset drift of ±(1.5 + 20 /G) μV/°C, the AD208 is the ideal isolation amplifier solution when low level, ±mV, signals must be measured and processed.

Excellent Common Mode Performance. The AD208BY provides 1.5 kV rms of common mode protection. Both grades of the AD208 feature a low common mode capacitance of 5.0 pF, inclusive of power isolation, that results in a typical common mode rejection specification of 100 dB (1 kΩ source impedance imbalance) as well as a low leakage current of 2.0 μA rms (max @ 240 V rms, 60 Hz).

Isolated Power. An isolated ±8.0 V dc power supply with the capability of delivering typically up to ±5 mA is available at the input port of the AD208. This permits the isolator to power floating signal conditioners, front-end amplifiers or remote transducers at the input.

Performance Rated Over the −40°C to +85°C Temperature Range. With its performance rated over the −40°C to +85°C temperature range the AD208 is an ideal isolation amplifier for use in industrial environments.

5

AD208—SPECIFICATIONS (typical @ +25°C, Output Load ≥ 1 MΩ, V_S = 15 V pk–pk, 25 kHz square wave, unless noted otherwise)

	AD208AY	AD208BY
GAIN		
Range	1–1000 V/V	*
Error (G = 1 V/V)	−1.0% (±2.5%, max)	*
vs. Temperature[1]		
−40°C to 0°C	±60 ppm/°C, max	*
0°C to +85°C	±20 ppm/°C, max	*
vs. Supply Voltage	±100 ppm/V	*
Nonlinearity[2], ±5 V Output Swing, G = 1–1000 V/V	±0.0125%	*
G = 1 V/V	±0.03%, max	±0.015%, max
INPUT VOLTAGE RATINGS[3]		
Linear Differential Range	±5 V, min	*
Max Safe Differential Range	±6 V	*
Max CMV Input to Output		
AC, 60 Hz, Continuous	750 V rms	1500 V rms
Continuous (AC & DC)	±1000 V peak	±2000 V peak
Common Mode Rejection (CMR) @ 60 Hz		
R_S ≤100 Ω (HI & LO Inputs),		
G = 1 V/V	100 dB	*
G = 1,000 V/V	120 dB	*
Common Mode Rejection (CMR) @ 60 Hz		
R_S≤1 kΩ (Input, HI, LO or Both)		
G = 1 V/V	100 dB	*
G = 1,000 V/V	100 dB	*
Leakage Current, Input to Output, @ 240 V rms, 60 Hz	2 μA rms, max	*
INPUT IMPEDANCE		
Differential (G = 1 V/V)	15 MΩ	*
Common Mode Across the Isolation Barrier	2 GΩ‖5 pF	*
OFFSET VOLTAGE, REFERRED TO INPUT (RTI)		
Initial @ +25°C (Adjustable to Zero)	±(0.25+15 /G) mV, max	*
vs. Temperature (−40°C to +85°C)	±(1.5+20 /G) μV/°C, max	*
vs. Supply Voltage	±(50+150 /G) μV/Volt	*
Voltage Noise, 0.1 Hz to 100 Hz	1.0 μV pk–pk	*
INPUT BIAS CURRENT		
Initial @ +25°C	±10 nA, max	*
vs. Temperature (−40°C to +85°C)	±100 pA/°C, max	*
vs. Supply Voltage	±1 nA/Volt	*
Current Noise, 0.1 Hz to 100 Hz	50 pA pk–pk	*
INPUT DIFFERENCE CURRENT		
Initial @ +25°C	±6 nA	*
vs. Temperature (−40°C to +85°C)	±60 pA/°C	*
FREQUENCY RESPONSE		
Bandwidth[4] (Full Signal, i.e., V_O≤10 V pk–pk)		
G = 1 V/V	4.0 kHz	*
G = 1000 V/V	0.4 kHz	*
Slew Rate	0.1 V/μs	*
Settling Time to ±0.10% on a 10 V Step, G = 1 V/V	2 ms	*
Overload Recovery Time[5], G = 1000 V/V	5 ms	*
RATED OUTPUT		
Voltage (OUT HI to OUT LO)	±5 V	*
Maximum Voltage Difference Between OUT HI		
and OUT LO or CLK COM (Pin 32)	±6.5 V	*
Output Resistance	3 kΩ	*
Output Ripple, 100 kHz Bandwidth	10 mV pk–pk	*
		*
5 kHz Bandwidth	0.8 mV pk–pk	

	AD208AY	AD208BY
ISOLATED POWER OUTPUT		
Voltage, No Load	±8.0 V	*
vs. Temperature (−40°C to +85°C)	±0.025%/°C	*
ISOLATED POWER SUPPLY (Continued)		
Accuracy	±10%	*
Rated Load Current[6]	±2.0 mA, min	*
Regulation, No Load to Rated Load	10%	*
Line Regulation	±10%/Volt	*
Ripple, Rated Load, 100 kHz Bandwidth	100 mV pk–pk	*
CLOCK DRIVE INPUT OF THE AD208[7]		
Input Voltage	15 V pk–pk ± 5%, Square Wave	*
Input Current (No Load on Isolated Supplies)	±10 mA pk	*
Frequency	25 kHz ±5%	*
Duty Cycle	47.5% to 52.5%	*
PACKAGE DIMENSIONS		
SIP Package	2.08" × 0.260" × 0.625", max	*
	52.8 mm × 6.6 mm × 15.9 mm, max	*
TEMPERATURE RANGE		
Rated Performance	−40°C to +85°C	*
Storage	−40°C to +85°C	*

NOTES

*Specification is the same as that for the AD208AY.

[1]This specification represents the average gain drift over the indicated temperature range. Refer to Figure 2 for an illustration of the typical normalized gain drift for the AD208.

[2]Nonlinearity is specified as a % deviation from a best straight line. For gains greater than 50 V/V, a 100 pF capacitor from the feedback terminal of the input op amp (Pin 4) to the input common (Pin 2) is recommended in order to minimize the gain nonlinearity. Refer to Figure 30 for a circuit schematic.

[3]To limit the input current to the AD208 during unpowered or saturated conditions it is recommended that a resistor (typically 2 kΩ) be placed in series with the signal and the input terminal of the AD208. A reasonable value for the current limit would be 2.5 mA.

[4]Refer to Figure 16 for a graph of the AD208's 3 dB Bandwidth versus Gain Setting.

[5]Overload Recovery Time is the time it takes for the isolation amplifier to return to within ±0.10% of its correct value from a saturated condition once the initiating overrange signal has been removed. For the AD208, the overload recovery time is determined by applying a +5 V (−5 V) pulse at the input terminals, when the AD208 is configured for a gain of 1,000 V/V, and then measuring the time it takes for the output to return to zero from its positive (negative) full-scale saturated voltage condition. A 2 kΩ resistor placed in series with the signal and the input terminal will reduce the overload recovery time to approximately 2 ms.

[6]Refer to Figure 17 for a curve illustrating the load drive capabilities of the isolated power supply.

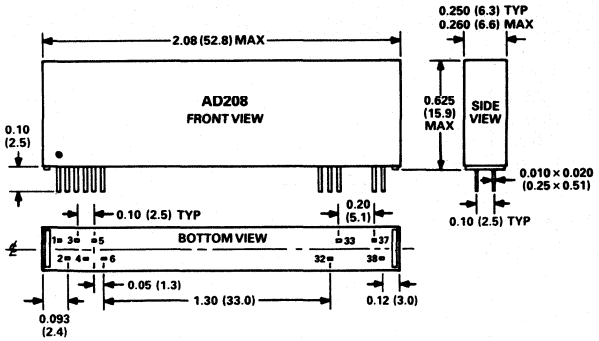
[7]It is recommended that the AD246 Clock Driver be used to drive the AD208. Refer to the "Powering the AD208 Section" of this data sheet for a detailed description of the AD208's clock driver input voltage and current requirements.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

SIP Package



Pin Designations

PIN	DESIGNATION	FUNCTION
1	IN+	NONINVERTING INPUT
2	IN COM	INPUT COMMON
3	IN−	INVERTING INPUT
4	FB	INPUT OP AMP; OUTPUT/FEEDBACK
5	V_{ISO-}	ISOLATED POWER: −DC OUTPUT
6	V_{ISO+}	ISOLATED POWER: +DC OUTPUT
32	CLK COM	CLOCK COMMON
33	CLK IN	CLOCK INPUT
37	OUT LO	OUTPUT LO
38	OUT HI	OUTPUT HI

CAUTION

ESD (electrostatic discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

INSIDE THE AD208

The functional block diagram of the AD208 is shown previously. The AD208 employs amplitude modulation techniques to implement transformer coupling of signals down to dc. The primary side of the power transformer, T2, is driven by the externally supplied 15 V pk–pk, 25 kHz square wave generator or the AD246 Clock Driver.

A full wave modulator translates the input signal to the carrier frequency which is then transmitted across transformer T1. The synchronous demodulator in the output port extracts the input signal from the carrier. The output signal is not internally buffered, therefore the user is free to interchange the output leads to get signal inversion.

The input port of the AD208 contains an uncommitted input op amp, a modulator and the isolated power supply. The uncommitted input amplifier can be used to supply gain or to buffer the input signals.

PERFORMANCE CHARACTERISTICS

Gain Error. Figure 1 shows the typical gain error for the AD208, expressed in % of full scale, as a function of the isolator's output load (Ω). For minimal gain errors, the AD208 is best operated with output loads greater than or equal to 1 MΩ.

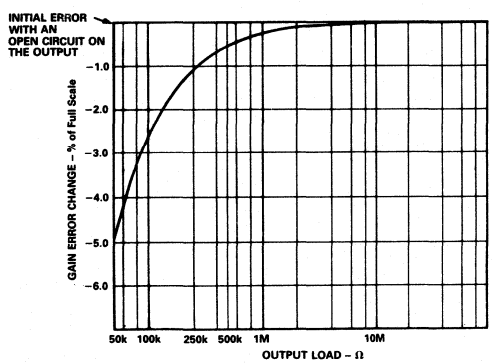


Figure 1. Gain Error Change (% of Full Scale) vs. Output Load (Ω), with V_S = 15 V pk–pk, 25 kHz Square Wave

Gain Drift. Figure 2 presents the normalized gain drift, from the gain error measured at +25°C, of the AD208 over the −40°C to +85°C rated temperature range.

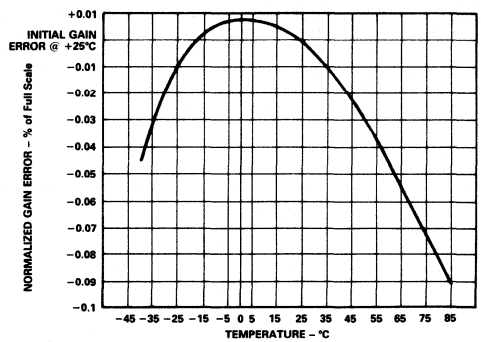


Figure 2. Normalized Gain Error (% of Full Scale) vs. Temperature (°C), with V_S = 15 V pk–pk, 25 kHz Square Wave

The effect of the output load on the AD208's gain temperature coefficient is shown in Figure 3 for the −40°C to 0°C and 0°C to +85°C temperature ranges. To minimize the gain temperature coefficient, the AD208 performs best with output loads of greater than or equal to 1 MΩ.

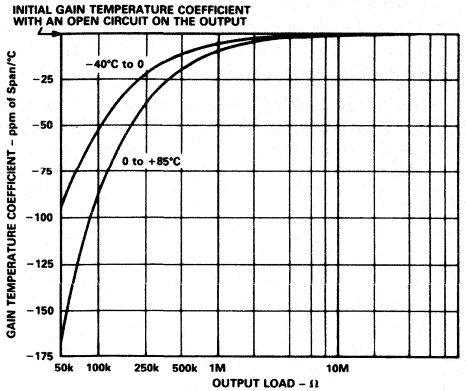


Figure 3. Gain Temperature Coefficient (ppm/°C) vs. Output Load (Ω) and Operating Temperature Range, with V_S = 15 V pk–pk, 25 kHz Square Wave

Gain Nonlinearity. The typical gain nonlinearity error of the AD208, at a gain of 1 V/V, is specified as ±0.0125% or ±1.25 mV. The nonlinearity performance of the AD208 is dependent on the output voltage swing and this dependency is illustrated in Figure 4. The vertical axis represents the nonlinearity error, expressed in % of output span (i.e., % of 10 V) on the left axis or in mV on the right axis. The horizontal axis displays the magnitude of the output voltage swing.

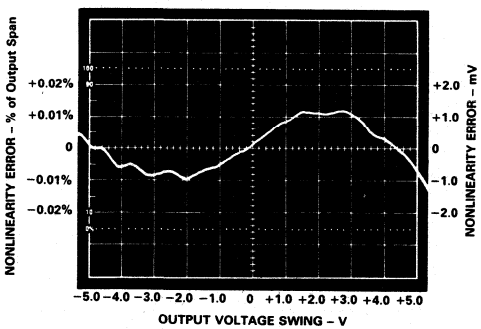


Figure 4. Typical Gain Nonlinearity Error (% of Output Span and mV) vs. Output Voltage Swing for a Gain of 1 V/V and with V_S = 15 V pk–pk, 25 kHz Square Wave

The variation of the AD208's gain nonlinearity, from that measured at +25°C, over the entire −40°C to +85°C rated temperature range is demonstrated by the curve in Figure 5.

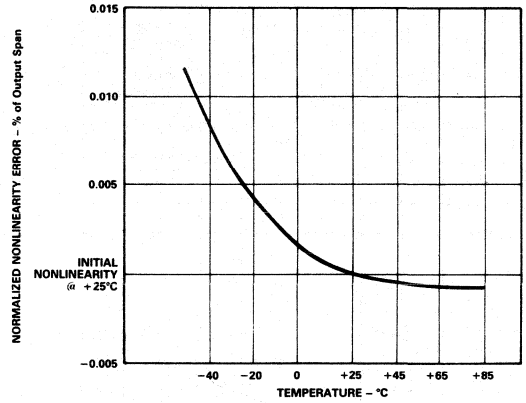


Figure 5. Normalized Gain Nonlinearity (% of Output Span) vs. Temperature (°C), with V_S = 15 V pk–pk, 25 kHz Square Wave

The nonlinearity of the AD208 is minimized when its output load is greater than 1 MΩ, as shown in Figure 6.

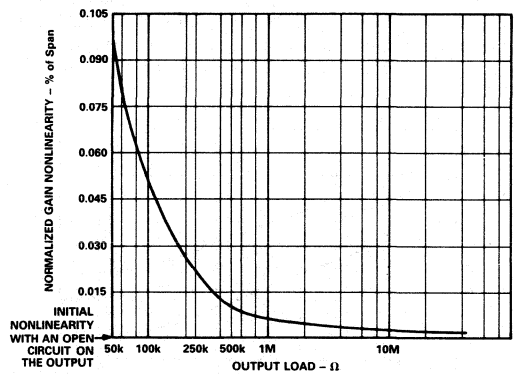


Figure 6. Normalized Gain Nonlinearity (% of Output Span) vs. Output Load (Ω) for a Gain of 1 V/V and with V_S = 15 V pk–pk, 25 kHz Square Wave

Input Voltage Rating. The linear input voltage range for the AD208 is specified as ±5 V. This rating applies when the AD208 is powered by a 15 V pk–pk ±5%, square wave (@ 25 kHz). The specified input voltage range is, however, affected by the clock driver voltage and the load placed on the AD208's front-end isolated power supplies. The variation of the input voltage range as a function of the isolated power supply load and the clock supply voltage are illustrated by the parametric curves in Figure 7.

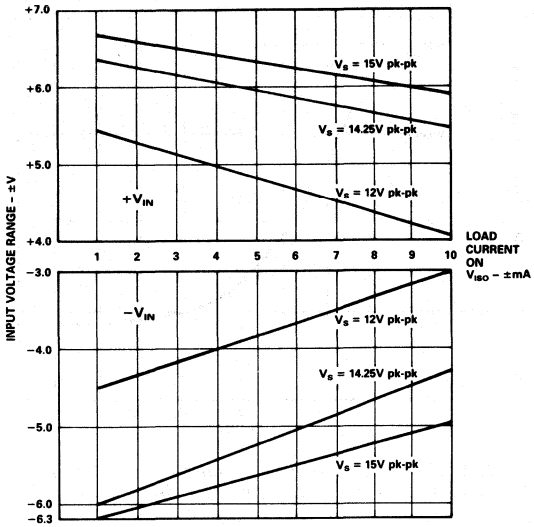


Figure 7. Input Voltage Range (±V) vs. Load Placed on the Isolated Power Supplies (mA) and Clock Driver Voltage (V pk–pk)

Common Mode Rejection. Figures 8 and 9 illustrate the typical common mode rejection, expressed in dB, of the AD208 as a function of the common mode signal frequency (kHz) and source impedance imbalance (kΩ) for gains of 1 V/V and 1,000 V/V, respectively.

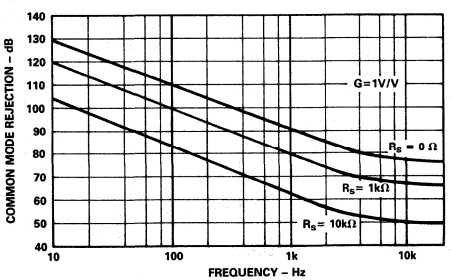


Figure 8. Typical Common Mode Rejection (dB) vs. Common Mode Signal Frequency (kHz) and Source Impedance Imbalance (kΩ) for a Gain of 1 V/V

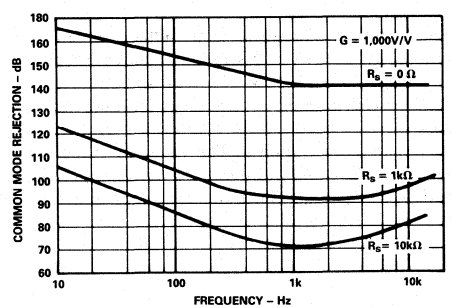


Figure 9. Typical Common Mode Rejection (dB) vs. Common Mode Signal Frequency (kHz) and Source Impedance Imbalance (kΩ) for a Gain of 1,000 V/V

To achieve the optimal common mode rejection of unwanted signals, it is strongly recommended that the source impedance imbalance be kept as low as possible and that the input circuitry be carefully laid out so as to avoid adding excessive stray capacitances at the isolator's input terminals.

Output Offset Voltage. The normalized output offset voltage drift from the initial offset measured at +25°C is presented in Figure 10 over the rated −40°C to +85°C temperature range.

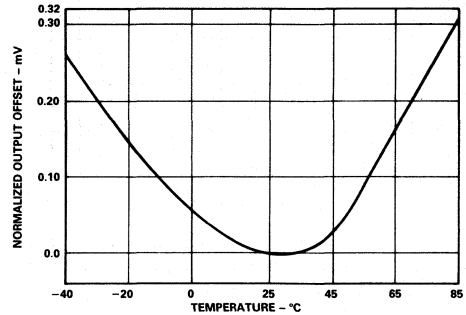


Figure 10. Normalized Output Offset Voltage (mV) vs. Temperature (°C) with an AD208 Gain of 1 V/V, with V_S = 15 V pk–pk, 25 kHz Square Wave

Input Offset Voltage. The AD208 exhibits an extremely low input offset voltage temperature coefficient over the −40°C to +85°C temperature range as indicated in Figure 11.

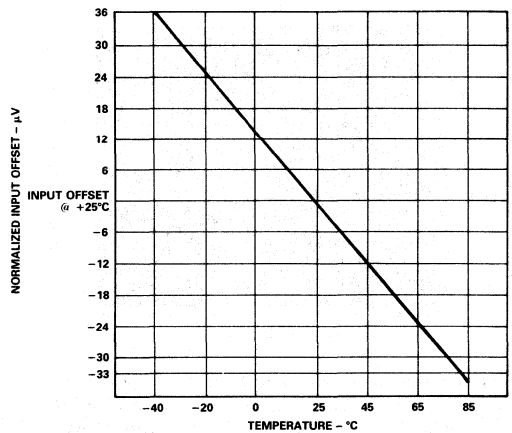


Figure 11. Normalized Input Offset Voltage (µV) vs. Temperature (°C), with V_S = 15 V pk–pk, 25 kHz Square Wave

The typical noise characteristics for the AD208's uncommitted input op amp is summarized in Figure 12.

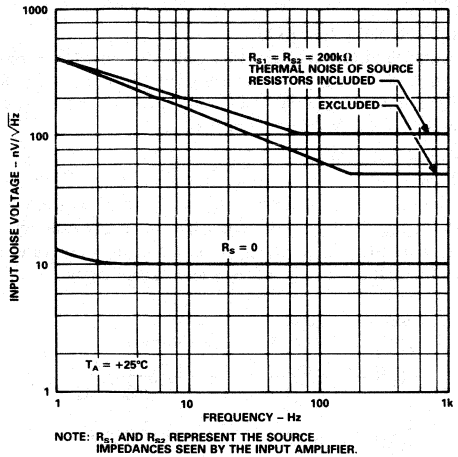


Figure 12. Typical Input Voltage Noise (nV/√Hz) vs. Frequency for the AD208's Uncommitted Input Op Amp

Input Bias Current. The typical input bias current variation from the initial bias current at +25°C as a function of temperature is presented in Figure 13.

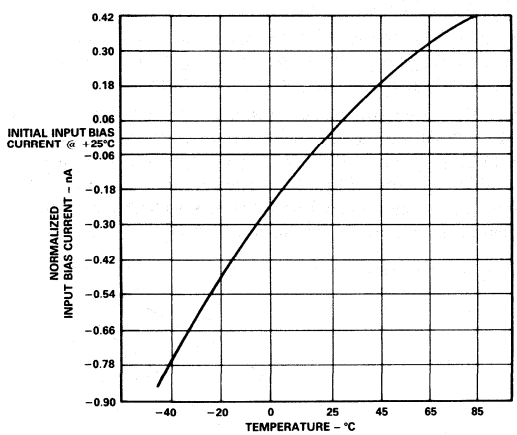


Figure 13. Normalized Input Bias Current (nA) vs. Temperature (°C)

Frequency Response: Gain and Phase Shift. Figure 14 characterizes the AD208's gain as a function of frequency, while Figure 15 illustrates the corresponding phase shift versus frequency.

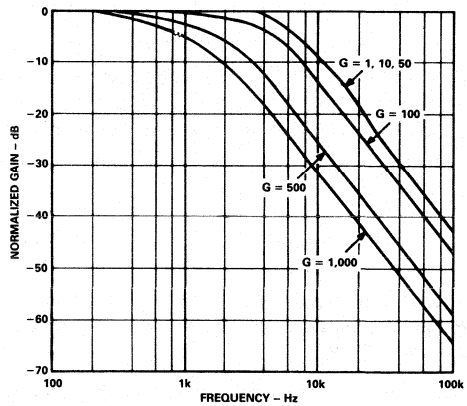


Figure 14. Normalized Gain (dB) as a Function of Input Signal Frequency (Hz)

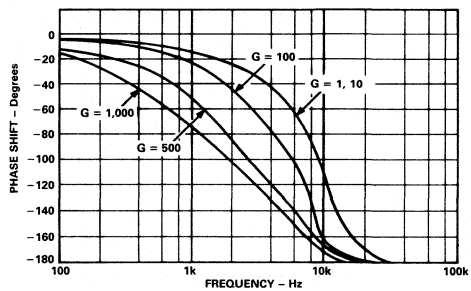


Figure 15. Phase Shift (Degrees) vs. Input Signal Frequency (Hz)

The frequency response performance of the AD208 can also be characterized in terms of its 3 dB bandwidth versus the desired gain setting as plotted in Figure 16.

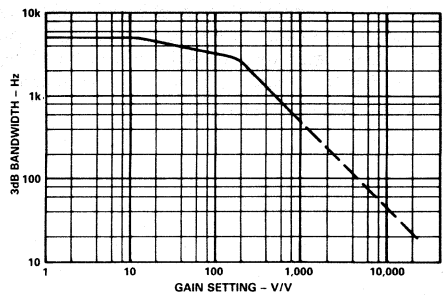


Figure 16. 3 dB Bandwidth (Hz) vs. AD208 Gain Setting (V/V)

Isolated Power Supply. The load characteristics of the AD208's isolated power supplies are plotted in Figure 17. It is recommended that the isolated power supply load not exceed 10 mA as permanent damage to the internal power circuitry of the AD208 may occur.

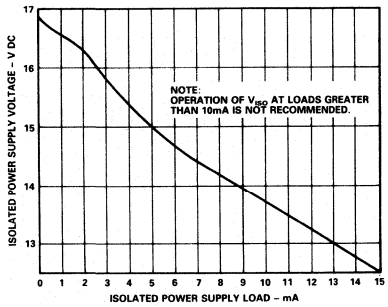


Figure 17. Isolated Power Supply Voltage (V DC) vs. Isolated Power Supply Load (mA), with V_S = 15 V pk–pk, 25 kHz Square Wave

The isolated power supply exhibits some ripple which varies as a function of the load placed on the supply terminals. Figure 18 illustrates the functional relationship between the isolated supply ripple (mV pk–pk) and the resistive load placed on the supplies.

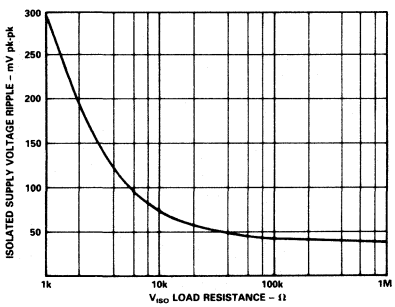


Figure 18. Isolated Power Supply Ripple (mV pk–pk) vs. Resistive Load (Ω), with V_S = 15 V pk–pk, 25 kHz Square Wave

The AD208 has internal bypass capacitors that optimize the tradeoff between output ripple and power supply performance, even under full load conditions. If a specific application requires more bypassing of the isolated power supplies, external capacitors may be added. Figure 19 plots the isolated power supply ripple as a function of the external bypass capacitance under rated load conditions (i.e., ±2 mA).

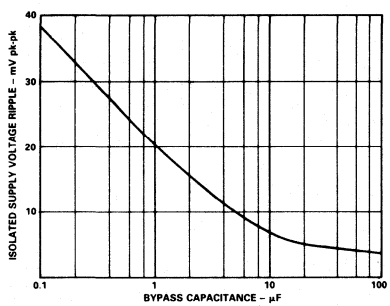


Figure 19. Isolated Power Supply Ripple (mV pk–pk) vs. Bypass Capacitance (µF) with a ±2 mA Load on the Isolated Supplies and a Noise Bandwidth of 100 kHz

CAUTION: The AD208 design does not provide for short circuit protection of its isolated power supply. A current limiting resistor may be placed in series with the isolated power terminals and the load in order to protect the supply against inadvertent shorts.

APPLICABLE STANDARDS

As an assurance of high performance reliability, the CMV rating of each grade of the AD208 is factory tested for one minute to 120% of the appropriate CMV isolation rating (1800 V rms for the B grade and 900 V rms for the A Grade).

POWERING THE AD208

The AD208 is powered by an externally supplied 15 V pk–pk, 25 kHz square wave (50% duty cycle) clock signal connected as shown in Figure 20. An ac coupling capacitor is provided in the AD208 to level shift the clock signal which in turn generates the necessary internal dc supply voltages and carrier signal.

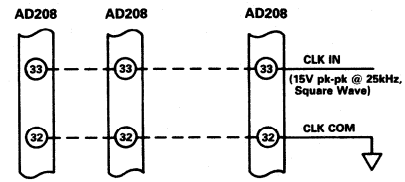


Figure 20. Powering the AD208

The rated performance of the AD208 is specified for a clock driver square wave signal that meets the following requirements:

- 15 V pk–pk ±5%
- 25 kHz ±5%
- 47.5% to 52.5% duty cycle.

Care must be exercised when using a square wave generator whose output does not meet the above requirements as the performance of the AD208 may be adversely affected.

Clock Driver Voltage Considerations. The rated performance of the AD208 will remain unaffected for clock driver voltages in the 14.25 V pk–pk to 15.75 V pk–pk range. Voltage swings below 14.25 V pk–pk will result primarily in the derating of the output voltage and isolated power supply voltage specifications as shown in Figures 21 and 22, respectively.

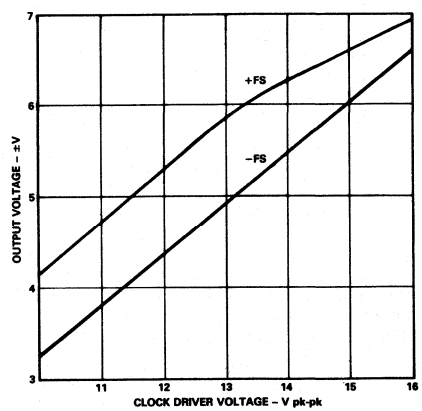


Figure 21. Output Voltage Swing (±V) vs. Clock Driver Voltage (V pk–pk)

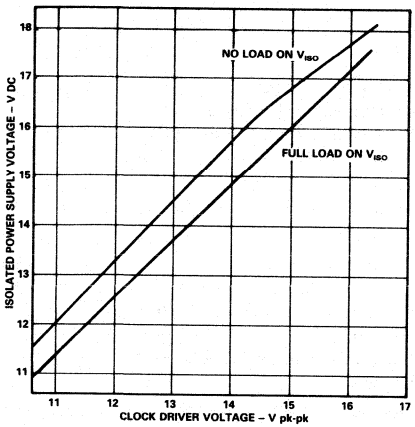


Figure 22. Isolated Power Supply Voltage (V DC) vs. Clock Driver Voltage (V pk–pk)

The reduction in the rated output voltage will increase the values for the nonlinearity and gain error parameters of the AD208 because of the headroom limits placed on the internal circuitry.

Note: Clock driver voltages greater than 16.5 V pk–pk may damage the internal components of the AD208 and consequently should not be used.

Clock Driver Frequency Considerations. The definition of the clock duty cycle for a two-state rectangular waveform is given by:

$$Duty\ Cycle\ (\%) = T_{HI}/(T_{HI} + T_{LO}) \times 100\%$$

where:

T_{HI} = The period of time that the waveform is in the HI state.

T_{LO} = The period of time that the waveform is in the LO state.

The performance of the AD208 will not be adversely affected by off-nominal clock signals so long as these clock signals are in the 47.5% to 52.5% duty cycle range and the 23.75 kHz to 26.25 kHz frequency range. To prevent a significant deterioration of the AD208 performance, it is strongly recommended that the clock driver duty cycle and frequency values ultimately chosen to operate the AD208 do not fall outside of the 40% to 60% and 20 kHz to 30 kHz ranges.

Clock Driver Power Considerations. In selecting and/or designing a clock driver for the AD208 isolation amplifier, it should be noted that the AD208 presents a reactive load to the clock driver. Consequently, both the average and peak drive currents to the AD208 clock input must be considered. Figures 23 and 24 illustrate the typical clock driver input voltage and current waveforms for a single AD208 with its isolated power supplies unloaded and fully loaded.

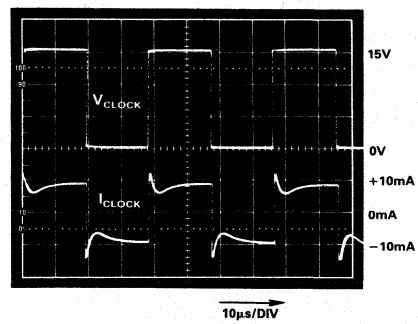


Figure 23. Typical Clock Voltage and Current Waveforms for a Single AD208 with No Load on its Isolated Power Supply

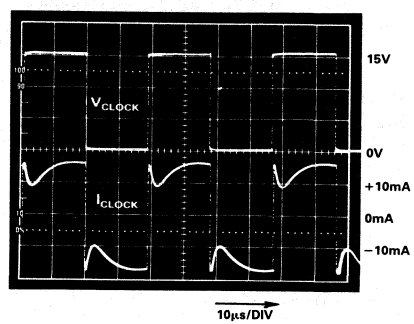


Figure 24. Typical Clock Voltage and Current Waveforms for a Single AD208 with a ±2 mA Load on its Isolated Power Supply

USING THE AD246 CLOCK DRIVER TO POWER THE AD208

To ensure that the power requirements of the AD208 are satisfied, Analog Devices suggests the use of the AD246 Clock Driver. The AD246 is an inexpensive, compact square wave oscillator that can be used to generate the necessary AD208 clock signal from a single +15 V dc supply. Table I lists the key specifications for the AD246.

	AD246JY
OUTPUT	
Frequency	25 kHz
Voltage	15 V pk–pk
Duty Cycle	50%
Maximum Safe Current Drive Capability[1]	120 mA
Fan Out	16
Resistance	15 Ω
POWER SUPPLY REQUIREMENTS	
Input Voltage	+15 V dc ± 5%
Supply Current	
Unloaded	3.5 mA
Each AD208 Adds	4.0 mA
Each 1 mA Load on AD208 $+V_{ISO}$ or $-V_{ISO}$ Adds	1.12 mA

NOTE
[1]The high current drive output of the AD246 will not withstand a short to ground.

Table I. Key Specifications for the AD246 Clock Driver (Specifications typical @ +25°C and V_S = +15 V DC unless otherwise noted)

5

The AD246JY is connected to the AD208 oscillator input(s) as shown in Figure 25. The AC1058 mating socket can be used with the AD246JY as demonstrated in Figure 27.

A supply bypass capacitor is included in the AD246, however it is recommended that an externally supplied bypass capacitor, as indicated by the dotted circuitry in Figure 26, be used if many AD208s are to be driven by a single AD246. The suggested capacitance value is 1 μF for every five AD208s driven. The placement of the bypass capacitor should be as close as possible to the AD246 Clock Driver.

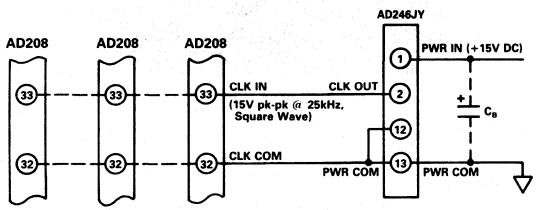


Figure 25. Using the AD246 to Power the AD208

USING THE AD208

Unity Gain Input Configuration. The basic unity gain configuration for input signals of up to ±5 V is shown in Figure 26.

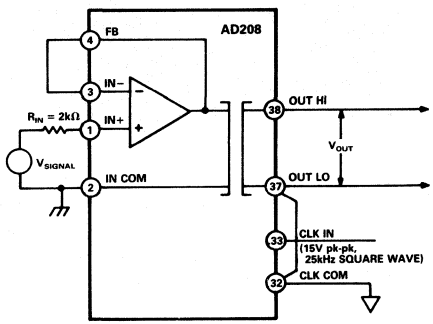


Figure 26. Basic Unity Gain Configuration

Input Configuration for a Gain Greater Than 1 (G>1). When small input signal levels must be amplified and isolated, Figure 27 shows how to get a gain greater than 1 while continuing to preserve a very high input impedance.

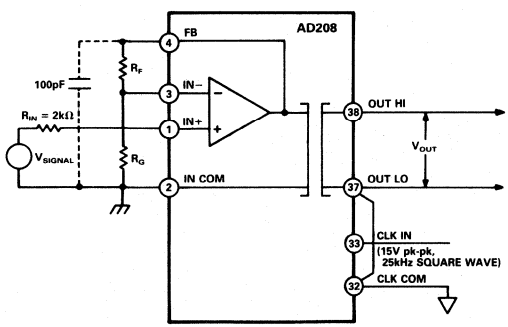


Figure 27. Input Configuration for a Gain Greater Than 1

In this circuit, the gain equation may be written as:

$$V_O = (1 + R_F/R_G) \times V_{SIG}$$

where:

V_O = Output Voltage (V)
V_{SIG} = Input Signal Voltage (V)
R_F = Feedback Resistor Value (Ω)
R_G = Gain Resistor Value (Ω).

The values for the resistors R_F and R_G should be chosen subject to the following constraints:

- The current drawn in the feedback resistor (R_F) is no greater than 1 mA. Note that for each mA drawn by the feedback resistor, the isolated power supply drive capability will decrease by 1 mA.
- The feedback (R_F) and gain resistor (R_G) result in the desired amplifier gain.

Note on the 100 pF Capacitor: Whenever a gain of 50 V/V or greater is required, a 100 pF capacitor from the FB (input op amp feedback) terminal to the IN COM (input common) terminal, as shown with the dotted lines in Figure 27, is highly recommended. The capacitor acts to filter out switching noise and will minimize the isolator's nonlinearity parameter.

Note on the 2 kΩ Resistor: The 2 kΩ resistor placed in series with the input signal source and the IN+ terminal, designated as R_{IN} in Figures 26 and 27, is suggested so as to limit the current seen at the input terminals to 2.5 mA when the AD208 is OFF. The 2 kΩ resistor will also reduce the overload recovery time to 2 ms.

Compensating the Uncommitted Input Op Amp. The open loop gain and phase versus frequency for the uncommitted input op amp is given in Figure 28. These curves can be used to determine the appropriate values for the feedback resistor and compensation capacitor in order to ensure frequency stability when reactive or nonlinear components are used in conjunction with the uncommitted input op amp.

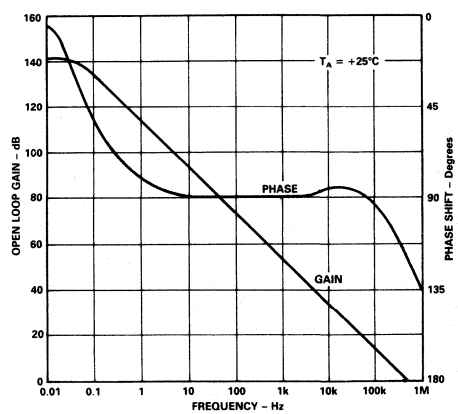


Figure 28. Open Loop Gain and Phase Response for the Uncommitted Input Op Amp of the AD208

A capacitor placed in the feedback loop of the input op amp may increase the nonlinearity of the AD208, particularly for large gains. A resistor (1 kΩ) placed in series with this capacitor should minimize the capacitor's effect on nonlinearity.

Signal Inversion. The circuits illustrated in Figures 26 and 29 are "noninverting." If signal inversion is desired simply interchange the output leads of the circuits shown in Figures 26 or 27 to get inversion. This approach allows for the retention of the high input impedance characteristics of the "noninverting" circuit.

Summing or Current Input Configuration. Figure 29 shows how the AD208 can accommodate current inputs or sum currents or voltages.

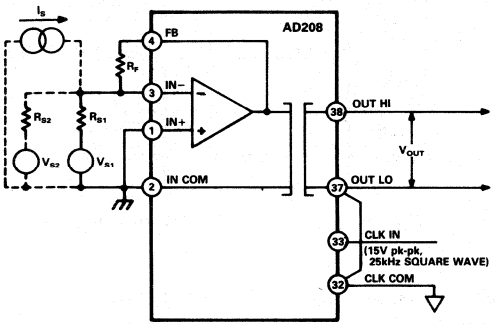


Figure 29. Summing or Current Input Configuration

In this circuit the output voltage equation can be written as:

$$V_O = -R_F \times (I_S + V_{S1}/R_{S1} + V_{S2}/R_{S2} + \ldots)$$

where:

V_O = Output Voltage (V)
V_{S1} = Voltage of Input Signal 1 (V)
V_{S2} = Voltage of Input Signal 2 (V)
I_S = Input Current Source (A)
R_F = Feedback Resistor (Ω)
R_{S1} = Source Resistance Associated with Input Signal 1 (Ω)
R_{S2} = Source Resistance Associated with Input Signal 2 (Ω).

The circuit of Figure 29 can also be used when the input signal is larger than the ±5 V input range of the isolator. For example, suppose that in Figure 29 only V_{S1}, R_{S1} and R_F are connected to the feedback, input and common terminals as shown by the solid lines in Figure 29. Now, a V_{S1} with a ±50 V span can be accommodated with R_F = 20 kΩ and R_{S1} = 200 kΩ.

Output Filter Circuit. Except at the highest useful gains, the noise seen at the output of the AD208 will be almost entirely comprised of the carrier ripple at multiples of 25 kHz. The ripple, when measured over a 100 kHz noise bandwidth, is typically 2 mV pk–pk near zero output and increases to approximately 7 mV pk–pk for outputs of ±5 V. The simple two-pole, 5 kHz low-pass Butterworth filter of Figure 30 can be used to reduce the output ripple of the AD208 to approximately 0.1 mV pk–pk and serve as an output buffer for the AD208.

An output buffer or filter may sometimes exhibit voltage spikes on the output even though none were present on the input signal to the buffer/filter. These spikes are usually due to clock noise appearing at the op amp's power supply pins, since most op amps have little or no supply rejection at high frequencies. Another common source of clock-related noise is from the sharing of the ground track by both the output circuit and the power input. The circuit of Figure 30, shows how to avoid these clock noise related problems.

Ideally, the output signal LO lead and the supply common should be tied together at the final signal measurement point as indicated in Figure 30. It may be useful to bypass the output LO to the output common with a 0.1 μF capacitor should the measurement point be more than a few feet from the isolator.

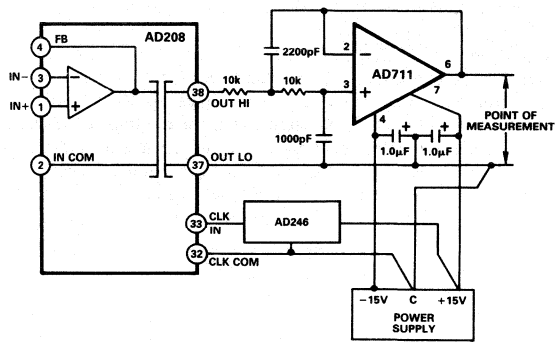


Figure 30. Output Filter Circuit Showing Proper Grounding

In multichannel applications where more than a few AD208s are driven by a single clock driver, substantial current spikes will flow in the power return line and in whichever signal output lead returns to a low impedance point (usually OUT LO). Consequently, both of these tracks should be made as large and as short as possible to minimize the track inductance and resistance. For best results, OUT LO should be connected directly to a ground plane that serves as the measurement common.

Current spikes can be greatly reduced by connecting a small inductance, 68 μHy to 100 μHy, in series with the clock drive input pin of each AD208. Molded chokes, such as the Dale IM-2 series, with a dc resistance of about 5 Ω should be suitable for most applications.

GAIN AND OFFSET ADJUSTMENTS

General Comments. When gain and offset adjustments are required, the actual compensation circuit ultimately utilized will depend on:

- The input configuration mode of the isolation amplifier (i.e., noninverting or inverting).
- The placement of the adjusting potentiometer (i.e., on the isolator's input or output side).

As a general rule:

- Offset Adjustments are best accomplished on the isolator's input side, as it is much easier and more efficient to null the offset ahead of any gain.
- Gain Adjustments are most easily accomplished as part of the gain-setting resistor network at the isolator's input side.
- To ensure the highest degree of stability in the gain and offset adjustments, the adjusting potentiometers should be located

as close as possible to the isolator's front end. Adjustment ranges should be kept to a minimum and high quality multiturn trimming potentiometers should be used.

- Output side adjustments may be necessary under the conditions where adjusting potentiometers placed on the input side would present a hazard to the user due to the presence of high common mode voltages during the adjustment procedure.
- It is recommended that the offset adjustment precedes the gain adjustment.

Input Adjustments for the Noninverting Mode of Operation
Offset Adjustment. Figure 31 shows the suggested input adjustment connections when the isolator's input amplifier is configured for the noninverting mode of operation. The offset adjustment circuit injects a small voltage in series with the low side of the signal source. The adjustment potentiometer P_2 is responsible for nulling out the offset voltage. A 100 kΩ P_2, 50 kΩ R_{OA} and a 100 Ω R_C should provide an offset adjustment range (Referred to Input) of about ±15 mV. Since the offset is zeroed out ahead of the gain, the values given above for P_2, R_{OA} and R_C should work for any gain on the isolator.

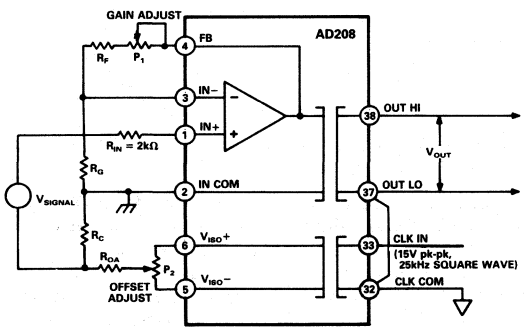


Figure 31. Input Adjustment Circuit for the Noninverting Mode of Operation

Notes:

- To minimize CMR degradation it is recommended that the resistor R_C (shown in Figure 31) be below a few hundred ohms.
- The offset adjustment circuit of Figure 31 will not work if the signal source has another current path to input common, or if current flows in the signal source LO lead. If this is the case, use the output adjustment procedure.

Gain Adjustment. Figure 31 also shows the suggested gain adjustment circuit. Note that the gain adjustment potentiometer P_1 is incorporated into the gain-setting resistor network at the isolator's input.

To maintain gain trim ranges that are independent of the gain setting, the potentiometer P_1 should be proportioned to R_F such that

$$\frac{P_1 \times 100\%}{R_F} = \textit{Desired Gain Adjustment Range (in \% of Output Span)}$$

and

$$(R_F + P_1/2)/R_G + 1 = \textit{Desired Gain Setting}$$

Input Adjustments for the Inverting Mode of Operation
Offset Adjustment. Figure 32 shows the suggested input adjustment connections when the isolator's input amplifier is configured for the inverting mode of operation. Here the offset adjustment potentiometer P_2 nulls the voltage at the summing node. This method may be preferred over current injection since it is less affected by any subsequent gain adjustments. A 100 kΩ P_2, 50 kΩ R_{OA} and a 100 Ω R_C should provide an offset adjustment range (Referred to Input) of about ±15 mV.

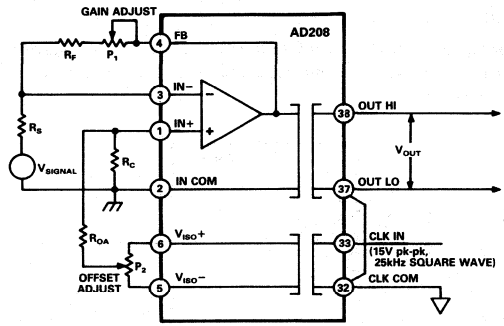


Figure 32. Input Adjustments for the Inverting Mode of Operation

Gain Adjustment. Figure 32 also shows the suggested gain adjustment circuit. In this circuit, the gain adjustment is made in the feedback loop using potentiometer P_1. The adjustments will be effective for all gains in the 1 to 1,000 V/V range.

Output Adjustments
Offset Adjustment. Figure 33 shows the recommended technique for offset adjustment at the output. In this circuit, a ±15 V dc voltage is supplied by an independent source. With reference to the output circuitry shown in Figure 33, the maximum offset adjustment range is given by:

$$E_{OFFSET} = \frac{R_C \times V_S}{R_C + R_O}$$

where, V_S is the power supply voltage. A 100 kΩ P_0, 100 Ω R_C and a 50 kΩ R_O should provide an offset adjustment range of about ±30 mV on the output.

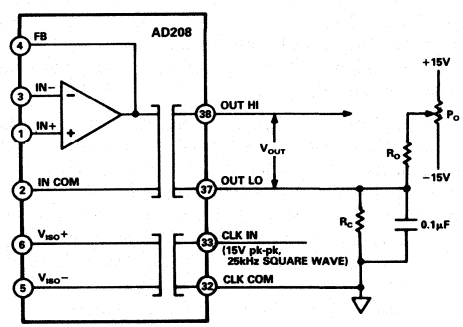


Figure 33. Output Side Offset Adjustment Circuit

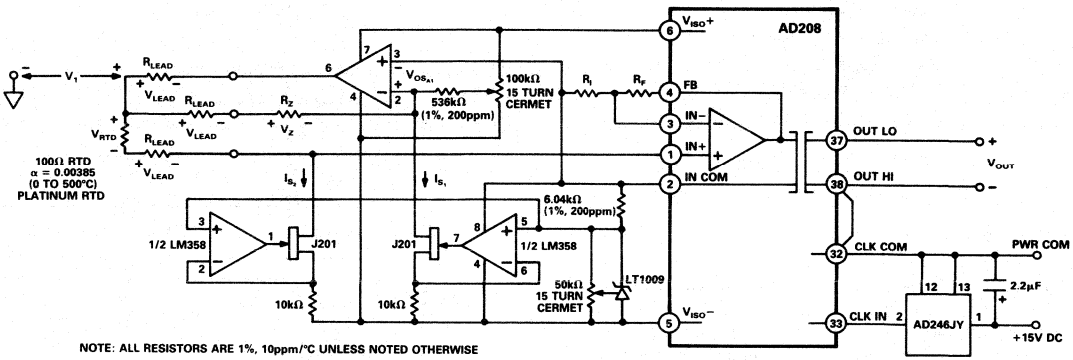


Figure 34. Using the AD208 in an Isolated RTD Application

Gain Adjustment. Since the output stage of the AD208 is unbuffered, any desired output gain adjustments can only be made in a subsequent stage.

USING ISOLATED POWER

The AD208 provides ±8.0 V dc power outputs referred to the input common. These may be used to power various accessory circuits which must operate at the input common mode level. The input offset adjustment circuits of the previous section are examples of this need.

The isolated power output has a current capacity of up to 5 mA which should be sufficient to operate adjustment circuits, references, op amps, signal conditioners or remote transducers.

CAUTION: The AD208 design does not provide for short circuit protection of its isolated power supply. A current limiting resistor may be placed in series with the isolated power terminals and the load in order to protect the supply against inadvertent shorts.

APPLICATION EXAMPLES

Isolated RTD Signal Processing. The stable high gain properties and low offset drift characteristics make the AD208 an ideal component for use in isolated RTD signal processing applications. RTD applications typically require the following three major elements: a stable current excitation source, a lead compensation network and a zero suppression network. The circuit schematic of Figure 34 illustrates how to use the AD208 with a handful of low power external components to condition, amplify and isolate low level RTD signals.

In the RTD application shown in Figure 34, the stable current excitation source needed to drive the RTD consists of a:

- Dual, single supply op amp (LM358)
- Pair of low V_{GSOFF} JFETS (ex. J201)
- Low power 2.5 V reference source
- Several precision 10 kΩ, 1%, 10 ppm/°C resistors.

The dual current sources generate a 250 μA excitation signal for the RTD and they also provide about 5 V of compliance with a ±5% gain adjustment range.

Zero suppression is accomplished in Figure 34 by using a simple ground servo amplifier in combination with the resistor labelled R_Z, while lead wire compensation is realized by remote sensing the RTD with the ground servo. The current, I_{S1} develops a voltage V_1 that is equal to:

$$V_1 = V_{OS_{A1}} + V_Z + V_{LEAD}$$

where the voltages V_1, $V_{OS_{A1}}$, V_Z and V_{LEAD} are as indicated in Figure 34.

The current I_{S2}, in turn, develops the voltage seen by the input amplifier of the AD208 and, with reference to the voltages labelled in Figure 34, V_{IN} is given by:

$$\begin{aligned} V_{IN} &= V_1 - V_{RTD} - V_{LEAD} \\ &= (V_{OS_{A1}} + V_Z + V_{LEAD}) - V_{RTD} - V_{LEAD} \\ &= V_{OS_{A1}} + V_Z - V_{RTD}. \end{aligned}$$

The offset trim circuit can then be used to null out all of the offset terms. Note that a high quality low power, low offset drift amplifier should be used for the ground servo amplifier.

The typical sensitivity of a 100 Ω platinum RTD with a 0.25 mA current excitation is in the 95 μV/°C range. Therefore, using the AD208 isolation amplifier with a gain of 105 V/V will result in an approximate output sensitivity of 10 mV/°C which corresponds to a 0 to 500°C RTD range for a 0 to −5 V output span. If a 0 to +5 V output span is desired, simply reverse the OUT LO (Pin 37) and OUT HI (Pin 38) terminals of the AD208 taking care to ensure that the OUT LO pin is now connected to the CLK COM terminal.

The gain equation for the circuit of Figure 34 is determined by the formula given below.

$$\frac{V_O\,(HI) - V_O\,(LO)}{I_S \cdot (\Omega_{RTD}\,(HI) - \Omega_{RTD}\,(LO))} = R_F/R_I + 1$$

where:

V_O (HI) = AD208 output voltage at the maximum expected temperature seen by the RTD application

V_O (LO) = AD208 output voltage at the minimum expected temperature seen by the RTD application

Ω_{RTD} (HI) = Resistance of the RTD at the maximum expected temperature

Ω_{RTD} (LO) = Resistance of the RTD at the minimum expected temperature

R_Z = RTD resistance at 0°C (100 Ω, typ)

I_S = Current of the stable excitation source (0.25 mA)

R_F = Feedback resistor (10.5 kΩ)

R_I = Input resistor (100 Ω, 1%, 10 ppm/°C).

The circuit of Figure 34 accommodates a 10 mV/°C, unlinearized output for a 100 Ω platinum RTD. The circuit allows for a maximum measured temperature range of 500°C. The initial input offset is ±1.3 mV (max) which is roughly equivalent to 5.2 Ω. The offset adjustment circuit, which has a ±1.5 mV (RTI) adjustment range, can be used to easily trim out this initial offset. The offset drift of the RTD application shown in Figure 34 is ±4 μV/°C (max) or 0.016 Ω/°C.

Thermocouple Applications. Thermocouples provide an inexpensive and reliable way to measure temperature over a wide range. Thermocouples require high gain amplification and in some cases cold junction compensation. The circuit of Figure 35 shows how the stable high gain capability of the AD208 can be effectively utilized to amplify and isolate the low level voltage signals from a thermocouple. The AC1226 Monolithic Cold Junction Compensator is recommended for use in this application. The AC1226 acts to eliminate the cold junction voltage that is formed between the thermocouple wire and the actual measurement circuit. The AC1226 outputs 0 V at 0°C and it provides the correct compensation slope for many thermocouple types through user selected taps off of the internal AC1226 resistor string.

The gain and offset adjustment for the circuit shown in Figure 35 is easily accomplished by first shorting the AD208 inputs to ground (IN COM) and adjusting the offset potentiometer until 0 V is measured at the output. Once the offset has been

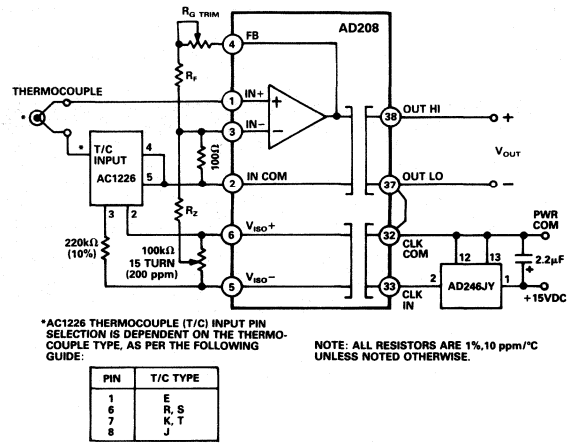


Figure 35. Using the AD208 in an Isolated Thermocouple Application

nulled out, the gain adjustment can then be initiated by applying an appropriate full-scale voltage, for the thermocouple type being used, at the input. Then adjust the gain trim until measuring +5 V out. The offset and gain trim do interact slightly with each other consequently, it would be advisable to recheck the offset error and readjust it if necessary. The residual error that may be introduced by the AC1226 at 25°C will be no more than ±2°C off nominal for all temperature ranges specified in Table II.

Table II lists the most commonly used thermocouple types along with their typical temperature ranges and a suggested AD208 gain setting. The table also includes recommended values for the feedback resistor (R_F), the gain trim resistor ($R_{G_{TRIM}}$) and the offset adjustment resistor (R_Z) all three of which are shown in Figure 35.

Thermocouple Type	Maximum Temperature Range @ 5 V Out (°C)	Maximum V_{IN} (mV)	AD208 Gain Setting (V/V)	SUGGESTED RESISTOR VALUES (With Reference to Figure 38) R_F (kΩ)	$R_{G_{TRIM}}$ (kΩ)	R_Z (MΩ)
E	900	68.783	72.69	6.98	0.5	2.0
J	750	42.283	118.25	11.5	1.0	2.0
K	1,250	50.633	98.75	9.53	1.0	2.0
R	1,450	16.741	298.6	28.7	2.0	2.0
S	1,450	14.973	333.9	32.4	2.0	2.0
T	350	17.816	280.6	27.4	2.0	2.0

Table II. Commonly Used Thermocouple Types, Temperature Ranges, AD208 Gain Settings and Circuit Resistor Values

ANALOG DEVICES

Precision, Wide Bandwidth, 3-Port Isolation Amplifier

AD210*

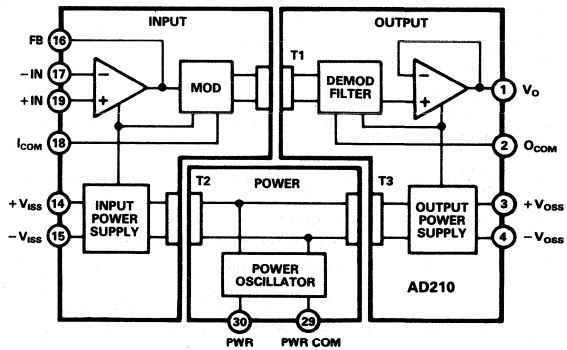
FEATURES

High CMV Isolation: 2500V RMS Continuous
±3500V Peak Continuous
Small Size: 1.00″ × 2.10″ × 0.350″
Three-Port Isolation: Input, Output, and Power
Low Nonlinearity: ±0.012% max
Wide Bandwidth: 20kHz Full-Power (−3dB)
Low Gain Drift: ±25ppm/°C max
High CMR: 120dB (G = 100V/V)
Isolated Power: ±15V @ ±5mA
Uncommitted Input Amplifier

APPLICATIONS

Multichannel Data Acquisition
High Voltage Instrumentation Amplifier
Current Shunt Measurements
Process Signal Isolation

FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

The AD210 is the latest member of a new generation of low cost, high performance isolation amplifiers. This three-port, wide bandwidth isolation amplifier is manufactured with surface-mounted components in an automated assembly process. The AD210 combines design expertise with state-of-the-art manufacturing technology to produce an extremely compact and economical isolator whose performance and abundant user features far exceed those offered in more expensive devices.

The AD210 provides a complete isolation function with both signal and power isolation supplied via transformer coupling internal to the module. The AD210's functionally complete design, powered by a single +15V supply, eliminates the need for an external DC/DC converter, unlike optically coupled isolation devices. The true three-port design structure permits the AD210 to be applied as an input or output isolator, in single or multi-channel applications. The AD210 will maintain its high performance under sustained common-mode stress.

Providing high accuracy and complete galvanic isolation, the AD210 interrupts ground loops and leakage paths, and rejects common-mode voltage and noise that may otherwise degrade measurement accuracy. In addition, the AD210 provides protection from fault conditions that may cause damage to other sections of a measurement system.

PRODUCT HIGHLIGHTS

The AD210 is a full-featured isolator providing numerous user benefits including:

High Common-Mode Performance: The AD210 provides 2500V rms (Continuous) and ±3500V peak (Continuous) common-mode voltage isolation between any two ports. Low input to output capacitance of 5pF results in a 120dB CMR at a gain of 100, and a low leakage current (2μA rms max @ 240V rms, 60Hz).

High Accuracy: With maximum nonlinearity of ±0.012% (B Grade), gain drift of ±25ppm/°C max, and input offset drift of (±10 ± 30/G) μV/°C, the AD210 assures signal integrity while providing high level isolation.

Wide Bandwidth: The AD210's full-power bandwidth of 20kHz makes it useful for wideband signals. It is also effective in applications like control loops, where limited bandwidth could result in instability.

Small Size: The AD210 provides a complete isolation function in a small DIP package just 1.00″ × 2.10″ × 0.350″. The low profile DIP package allows application in 0.5″ card racks and assemblies. The pinout is optimized to facilitate board layout while maintaining isolation spacing between ports.

Three-Port Design: The AD210's three-port design structure allows each port (Input, Output, and Power) to remain independent. This three-port design permits the AD210 to be used as an input or output isolator. It also provides additional system protection should a fault occur in the power source.

Isolated Power: ±15V @ 5mA is available at the input and output sections of the isolator. This feature permits the AD210 to excite floating signal conditioners, front-end amplifiers and remote transducers at the input as well as other circuitry at the output.

Flexible Input: An uncommitted operational amplifier is provided at the input. This amplifier provides buffering and gain as required, and facilitates many alternative input functions as required by the user.

***Covered by U.S. Patent No. 4,703,283.**

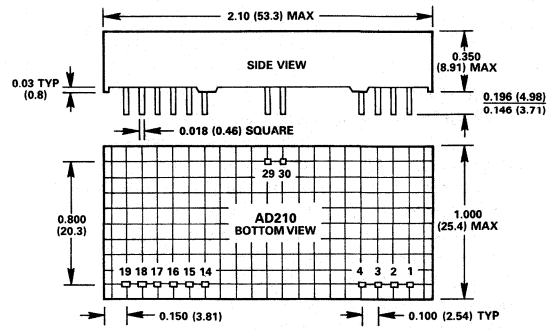
AD210—SPECIFICATIONS (typical @ +25°C, V_S = +15 V unless otherwise noted)

Model	AD210AN	AD210BN	AD210JN
GAIN			
Range	1V/V – 100V/V	*	*
Error	± 2% max	± 1% max	*
vs. Temperature (0 to +70°C)	± 25ppm/°C max	*	*
(–25°C to +85°C)	± 50ppm/°C max	*	*
vs. Supply Voltage	± 0.002%/V	*	*
Nonlinearity[1]	± 0.025% max	± 0.012% max	*
Nonlinearity vs. Isolated Supply Load	± 0.002%/mA	*	*
INPUT VOLTAGE RATINGS			
Linear Differential Range	± 10V	*	*
Maximum Safe Differential Input	± 15V	*	*
Max. CMV Input-to-Output			
ac, 60Hz, Continuous	2500V rms	*	1500V rms
dc, Continuous	± 3500V peak	*	± 2000V peak
Common-Mode Rejection			
60Hz, G = 100V/V			
$R_S \leq 500\Omega$ Impedance Imbalance	120dB	*	*
Leakage Current Input-to-Output			
@ 240Vrms, 60Hz	2μA rms max	*	*
INPUT IMPEDANCE			
Differential	$10^{12}\Omega$	*	*
Common Mode	$5G\Omega \| 5pF$	*	*
INPUT BIAS CURRENT			
Initial, @ +25°C	30pA typ (400pA max)	*	*
vs. Temperature (0 to +70°C)	10nA max	*	*
(–25°C to +85°C)	30nA max	*	*
INPUT DIFFERENCE CURRENT			
Initial, @ +25°C	5pA typ (200pA max)	*	*
vs. Temperature (0 to +70°C)	2nA max	*	*
(–25°C to +85°C)	10nA max	*	*
INPUT NOISE			
Voltage (1kHz)	$18nV/\sqrt{Hz}$	*	*
(10Hz to 10kHz)	4μV rms	*	*
Current (1kHz)	$0.01pA/\sqrt{Hz}$	*	*
FREQUENCY RESPONSE			
Bandwidth (–3dB)			
G = 1V/V	20kHz	*	*
G = 100V/V	15kHz	*	*
Settling Time (± 10mV, 20V Step)			
G = 1V/V	150μs	*	*
G = 100V/V	500μs	*	*
Slew Rate (G = 1V/V)	1V/μs	*	*
OFFSET VOLTAGE (RTI)[2]			
Initial, @ +25°C	(± 15 ± 45/G)mV max	(± 5 ± 15/G)mV max	
vs. Temperature (0 to +70°C)	(± 10 ± 30/G)μV/°C	*	*
(–25°C to +85°C)	(± 10 ± 50/G)μV/°C	*	*
RATED OUTPUT[3]			
Voltage, 2kΩ Load	± 10V min	*	*
Impedance	1Ω max	*	*
Ripple, (Bandwidth = 100kHz)	10mV p-p max	*	*
ISOLATED POWER OUTPUTS[4]			
Voltage, No Load	± 15V	*	*
Accuracy	± 10%	*	*
Current	± 5mA	*	*
Regulation, No Load to Full Load	See Text	*	*
Ripple	See Text	*	*
POWER SUPPLY			
Voltage, Rated Performance	+ 15V dc ± 5%	*	*
Voltage, Operating	+ 15V dc ± 10%	*	*
Current, Quiescent	50mA	*	*
Current, Full Load – Full Signal	80mA	*	*
TEMPERATURE RANGE			
Rated Performance	–25°C to +85°C	*	*
Operating	–40°C to +85°C	*	*
Storage	–40°C to +85°C	*	*
PACKAGE DIMENSIONS			
Inches	1.00 × 2.10 × 0.350	*	*
Millimeters	25.4 × 53.3 × 8.9	*	*

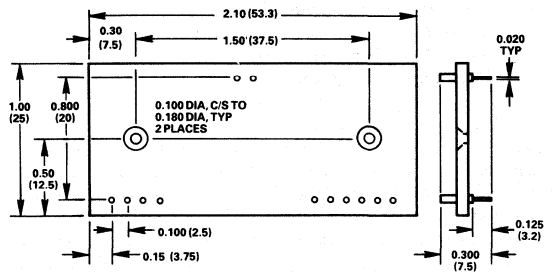
NOTES
*Specifications same as AD210AN.
[1]Nonlinearity is specified as a % deviation from a best straight line.
[2]RTI – Referred to Input
[3]A reduced signal swing is recommended when both $\pm V_{ISS}$ and $\pm V_{OSS}$ supplies are fully loaded, due to supply voltage reduction.
[4]See text for detailed information.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



AC1059 Mating Socket



AD210 Pin Designations

PIN	DESIGNATION	FUNCTION
1	V_O	Output
2	O_{COM}	Output Common
3	$+V_{OSS}$	+Isolated Power @ Output
4	$-V_{OSS}$	–Isolated Power @ Output
14	$+V_{ISS}$	+Isolated Power @ Input
15	$-V_{ISS}$	–Isolated Power @ Input
16	FB	Input Feedback
17	–IN	–Input
18	I_{COM}	Input Common
19	+IN	+Input
29	Pwr Com	Power Common
30	Pwr	Power Input

CAUTION

ESD (electrostatic discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

INSIDE THE AD210

The AD210 basic block diagram is illustrated in Figure 1. A +15V supply is connected to the power port, and ±15V isolated power is supplied to both the input and output ports via a 50kHz carrier frequency. The uncommitted input amplifier can be used to supply gain or buffering of input signals to the AD210. The fullwave modulator translates the signal to the carrier frequency for application to transformer T1. The synchronous demodulator in the output port reconstructs the input signal. A 20kHz, three-pole filter is employed to minimize output noise and ripple. Finally, an output buffer provides a low impedance output capable of driving a 2kΩ load.

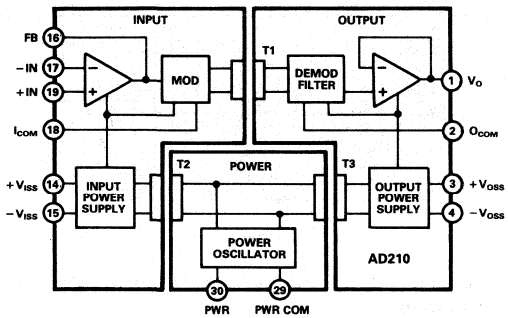


Figure 1. AD210 Block Diagram

USING THE AD210

The AD210 is very simple to apply in a wide range of applications. Powered by a single +15V power supply, the AD210 will provide outstanding performance when used as an input or output isolator, in single and multichannel configurations.

Input Configurations: The basic unity gain configuration for signals up to ±10V is shown in Figure 2. Additional input amplifier variations are shown in the following figures. For smaller signal levels Figure 3 shows how to obtain gain while maintaining a very high input impedance.

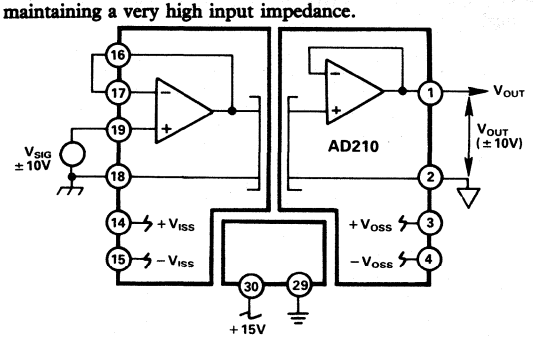


Figure 2. Basic Unity Gain Configuration

The high input impedance of the circuits in Figures 2 and 3 can be maintained in an inverting application. Since the AD210 is a three-port isolator, either the input leads or the output leads may be interchanged to create the signal inversion.

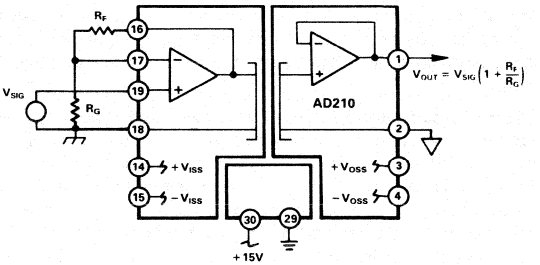


Figure 3. Input Configuration for G>1

Figure 4 shows how to accommodate current inputs or sum currents or voltages. This circuit configuration can also be used for signals greater than ±10V. For example, a ±100V input span can be handled with $R_F = 20k\Omega$ and $R_{S1} = 200k\Omega$.

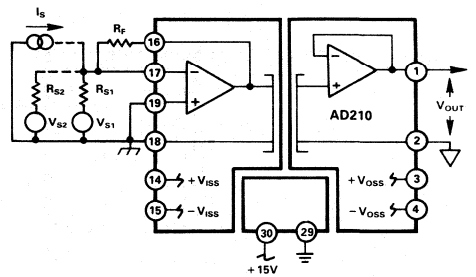


Figure 4. Summing or Current Input Configuration

Adjustments

When gain and offset adjustments are required, the actual circuit adjustment components will depend on the choice of input configuration and whether the adjustments are to be made at the isolator's input or output. Adjustments on the output side might be used when potentiometers on the input side would represent a hazard due to the presence of high common-mode voltage during adjustment. Offset adjustments are best done at the input side, as it is better to null the offset ahead of the gain.

Figure 5 shows the input adjustment circuit for use when the input amplifier is configured in the noninverting mode. This offset adjustment circuit injects a small voltage in series with the

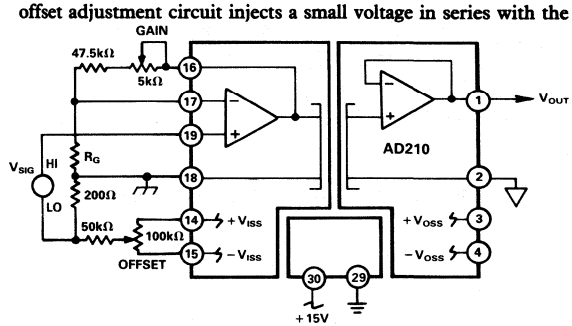


Figure 5. Adjustments for Noninverting Input

low side of the signal source. This will not work if the source has another current path to input common or if current flows in the signal source LO lead. To minimize CMR degradation, keep the resistor in series with the input LO below a few hundred ohms.

Figure 5 also shows the preferred gain adjustment circuit. The circuit shows R_F of 50kΩ, and will work for gains of ten or greater. The adjustment becomes less effective at lower gains (its effect is halved at G = 2) so that the pot will have to be a larger fraction of the total R_F at low gain. At G = 1 (follower) the gain cannot be adjusted downward without compromising input impedance; it is better to adjust gain at the signal source or after the output.

Figure 6 shows the input adjustment circuit for use when the input amplifier is configured in the inverting mode. The offset adjustment nulls the voltage at the summing node. This is preferable to current injection because it is less affected by subsequent gain adjustment. Gain adjustment is made in the feedback and will work for gains from 1 to 100V/V.

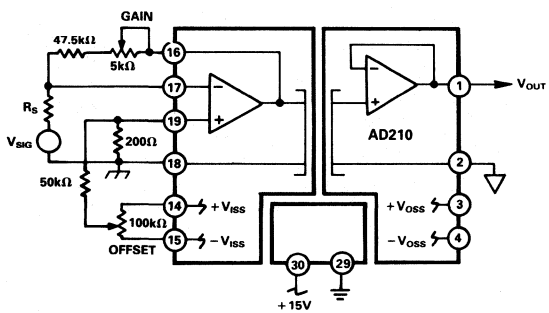


Figure 6. Adjustments for Inverting Input

Figure 7 shows how offset adjustments can be made at the output, by offsetting the floating output port. In this circuit, ±15V would be supplied by a separate source. The AD210's output amplifier is fixed at unity, therefore, output gain must be made in a subsequent stage.

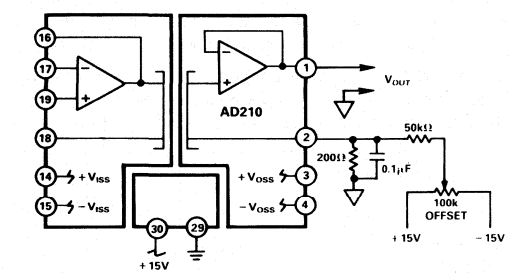


Figure 7. Output-Side Offset Adjustment

PCB Layout for Multichannel Applications: The unique pinout positioning minimizes board space constraints for multichannel applications. Figure 8 shows the recommended printed circuit board layout for a noninverting input configuration with gain.

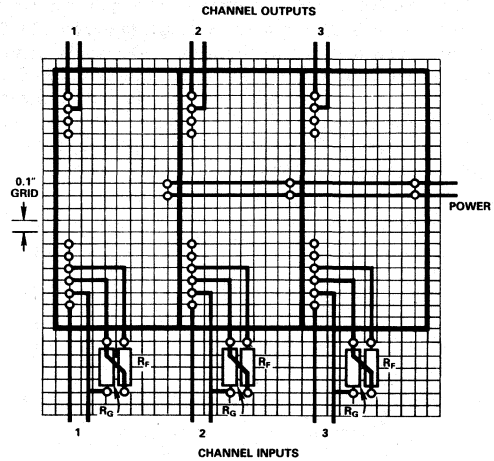


Figure 8. PCB Layout for Multichannel Applications with Gain

Synchronization: The AD210 is insensitive to the clock of an adjacent unit, eliminating the need to synchronize the clocks. However, in rare instances channel to channel pick-up may occur if input signal wires are bundled together. If this happens, shielded input cables are recommended.

PERFORMANCE CHARACTERISTICS

Common-Mode Rejection: Figure 9 shows the common-mode rejection of the AD210 versus frequency, gain and input source resistance. For maximum common-mode rejection of unwanted signals, keep the input source resistance low and carefully lay out the input, avoiding excessive stray capacitance at the input terminals.

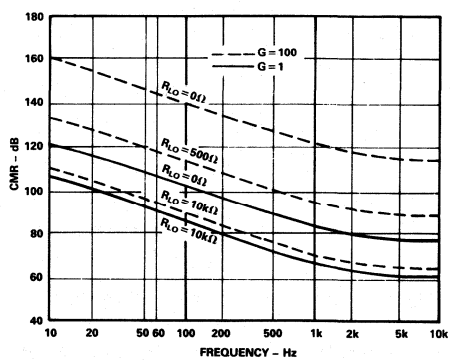


Figure 9. Common-Mode Rejection vs. Frequency

Phase Shift: Figure 10 illustrates the AD210's low phase shift and gain versus frequency. The AD210's phase shift and wide bandwidth performance make it well suited for applications like power monitors and controls systems.

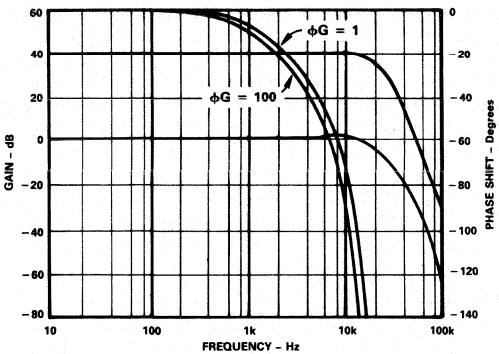


Figure 10. Phase Shift and Gain vs. Frequency

Input Noise vs. Frequency: Voltage noise referred to the input is dependent on gain and signal bandwidth. Figure 11 illustrates the typical input noise in nV/$\sqrt{\text{Hz}}$ of the AD210 for a frequency range from 10 to 10kHz.

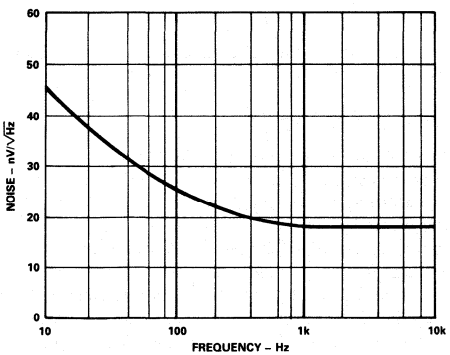


Figure 11. Input Noise vs. Frequency

Gain Nonlinearity vs. Output: Gain nonlinearity is defined as the deviation of the output voltage from the best straight line, and is specified as % peak-to-peak of output span. The AD210B provides guaranteed maximum nonlinearity of ±0.012% with an output span of ±10V. The AD210's nonlinearity performance is shown in Figure 12.

Gain Nonlinearity vs. Output Swing: The gain nonlinearity of the AD210 varies as a function of total signal swing. When the output swing is less than 20 volts, the gain nonlinearity as a fraction of signal swing improves. The shape of the nonlinearity remains constant. Figure 13 shows the gain nonlinearity of the AD210 as a function of total signal swing.

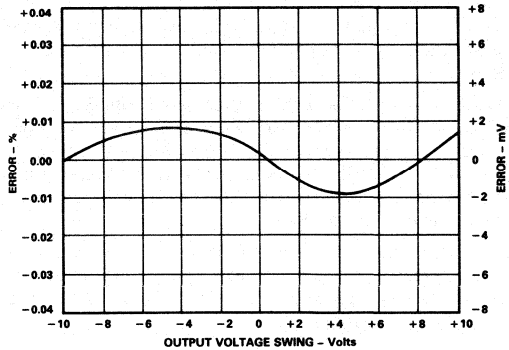


Figure 12. Gain Nonlinearity Error vs. Output

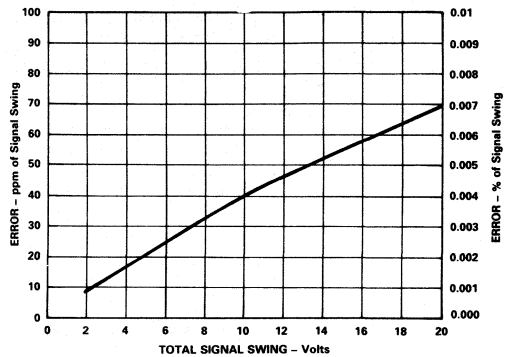


Figure 13. Gain Nonlinearity vs. Output Swing

Gain vs. Temperature: Figure 14 illustrates the AD210's gain vs. temperature performance. The gain versus temperature performance illustrated is for an AD210 configured as a unity gain amplifier.

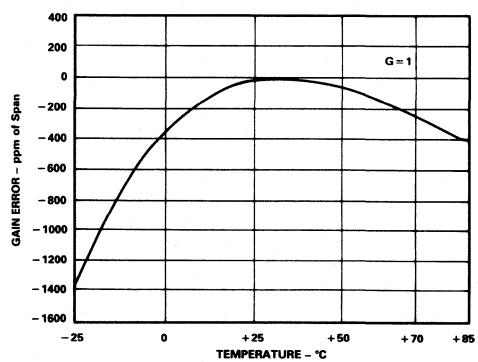


Figure 14. Gain vs. Temperature

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Isolated Power: The AD210 provides isolated power at the input and output ports. This power is useful for various signal conditioning tasks. Both ports are rated at a nominal ±15V at 5mA.

The load characteristics of the isolated power supplies are shown in Figure 15. For example, when measuring the load rejection of the input isolated supplies V_{ISS}, the load is placed between $+V_{ISS}$ and $-V_{ISS}$. The curves labeled V_{ISS} and V_{OSS} are the individual load rejection characteristics of the input and the output supplies, respectively.

There is also some effect on either isolated supply when loading the other supply. The curve labeled CROSSLOAD indicates the sensitivity of either the input or output supplies as a function of the load on the opposite supply.

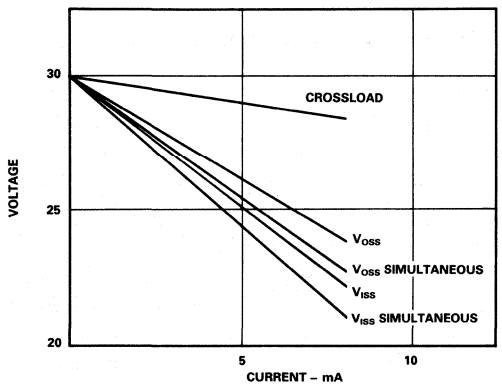


Figure 15. Isolated Power Supplies vs. Load

Lastly, the curves labeled V_{OSS} simultaneous and V_{ISS} simultaneous indicate the load characteristics of the isolated power supplies when an equal load is placed on both supplies.

The AD210 provides short circuit protection for its isolated power supplies. When either the input supplies or the output supplies are shorted to input common or output common, respectively, no damage will be incurred, even under continuous application of the short. However, the AD210 may be damaged if the input and output supplies are shorted simultaneously.

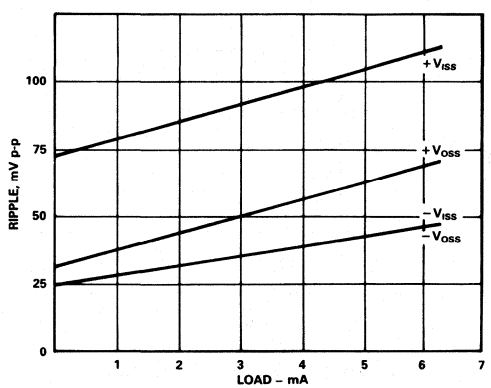


Figure 16a. Isolated Supply Ripple vs. Load (External 4.7μF Bypass)

Under any circumstances, care should be taken to ensure that the power supplies do not accidentally become shorted.

The isolated power supplies exhibit some ripple which varies as a function of load. Figure 16a shows this relationship. The AD210 has internal bypass capacitance to reduce the ripple to a point where performance is not affected, even under full load. Since the internal circuitry is more sensitive to noise on the negative supplies, these supplies have been filtered more heavily. Should a specific application require more bypassing on the isolated power supplies, there is no problem with adding external capacitors. Figure 16b depicts supply ripple as a function of external bypass capacitance under full load.

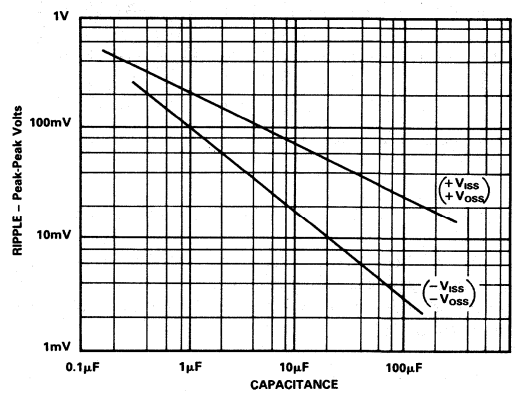


Figure 16b. Isolated Power Supply Ripple vs. Bypass Capacitance (Volts p-p, 1MHz Bandwidth, 5mA Load)

APPLICATIONS EXAMPLES

Noise Reduction in Data Acquisition Systems: Transformer coupled isolation amplifiers must have a carrier to pass both ac and dc signals through their signal transformers. Therefore, some carrier ripple is inevitably passed through to the isolator output. As the bandwidth of the isolator is increased more of the carrier signal will be present at the output. In most cases, the ripple at the AD210's output will be insigificant when compared to the measured signal. However, in some applications, particularly when a fast analog-to-digital converter is used following the isolator, it may be desirable to add filtering; otherwise ripple may cause inaccurate measurements. Figure 17 shows a circuit that will limit the isolator's bandwidth, thereby reducing the carrier ripple.

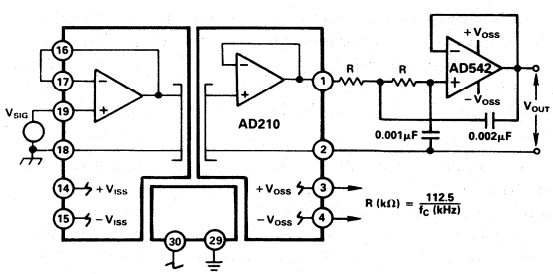


Figure 17. 2-Pole, Output Filter

Self-Powered Current Source

The output circuit shown in Figure 18 can be used to create a self-powered output current source using the AD210. The 2kΩ resistor converts the voltage output of the AD210 to an equivalent current $V_{OUT}/2k\Omega$. This resistor directly affects the output gain temperature coefficient, and must be of suitable stability for the application. The external low power op amp, powered by $+V_{OSS}$ and $-V_{OSS}$, maintains its summing junction at output common. All the current flowing through the 2kΩ resistor flows through the output Darlington pass devices. A Darlington configuration is used to minimize loss of output current to the base. The low leakage diode is used to protect the base-emitter junction against reverse bias voltages. Using $-V_{OSS}$ as a current return allows more than 10V of compliance. Offset and gain control may be done at the input of the AD210 or by varying the 2kΩ resistor and summing a small correction current directly into the summing node. A nominal range of 1-5mA is recommended since the current output cannot reach zero due to reverse bias and leakage currents. If the AD210 is powered from the input potential, this circuit provides a fully isolated, wide bandwidth current output. This configuration is limited to 5mA output current.

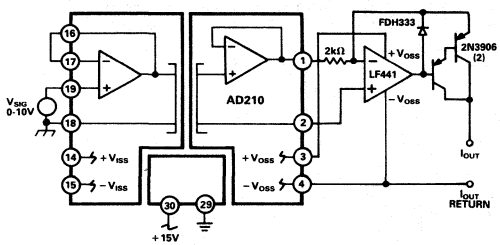


Figure 18. Self-Powered Isolated Current Source

Isolated V-to-I Converter

Illustrated in Figure 19, the AD210 is used to convert a 0 to +10V input signal to an isolated 4-20mA output current. The AD210 isolates the 0 to +10V input signal and provides a proportional voltage at the isolator's output. The output circuit converts the input voltage to a 4-20mA output current, which in turn is applied to the loop load R_{LOAD}.

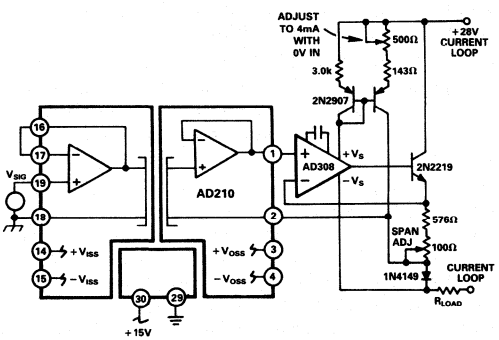


Figure 19. Isolated Voltage-to-Current Loop Converter

Isolated Thermocouple Amplifier

The AD210 application shown in Figure 20 provides amplification, isolation and cold-junction compensation for a standard J type thermocouple. The AD590 temperature sensor accurately monitors the input terminal (cold-junction). Ambient temperature changes from 0 to +40°C sensed by the AD590, are cancelled out at the cold junction. Total circuit gain equals 183; 100 and 1.83, from A1 and the AD210 respectively. Calibration is performed by replacing the thermocouple junction with plain thermocouple wire and a millivolt source set at 0.0000V (0°C) and adjusting R_O for E_{OUT} equal to 0.000V. Set the millivolt source to +0.02185V (400°C) and adjust R_G for V_{OUT} equal to +4.000V. This application circuit will produce a nonlinearized output of about +10mV/°C for a 0 to +400°C range.

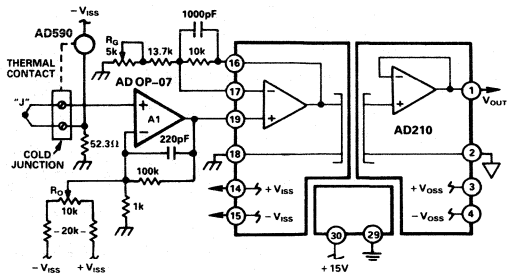


Figure 20. Isolated Thermocouple Amplifier

Precision Floating Programmable Reference

The AD210, when combined with a digital-to-analog converter, can be used to create a fully floating voltage output. Figure 21 shows one possible implementation.

The digital inputs of the AD7541 are TTL or CMOS compatible. Both the AD7541 and AD581 voltage reference are powered by the isolated power supply $+V_{ISS}$. I_{COM} should be tied to input digital common to provide a digital ground reference for the inputs.

The AD7541 is a current output DAC and, as such, requires an external output amplifier. The uncommitted input amplifier internal to the AD210 may be used for this purpose. For best results, its input offset voltage must be trimmed as shown.

The output voltage of the AD210 will go from 0V to −10V for digital inputs of 0 and full scale, respectively. However, since the output port is truly isolated, V_{OUT} and O_{COM} may be freely interchanged to get 0 to +10V.

This circuit provides a precision 0–10V programmable reference with a ±3500V common-mode range.

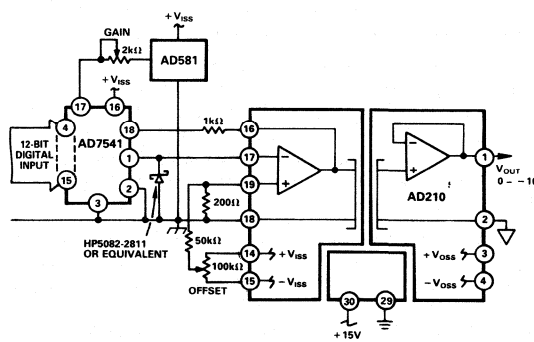


Figure 21. Precision Floating Programmable Reference

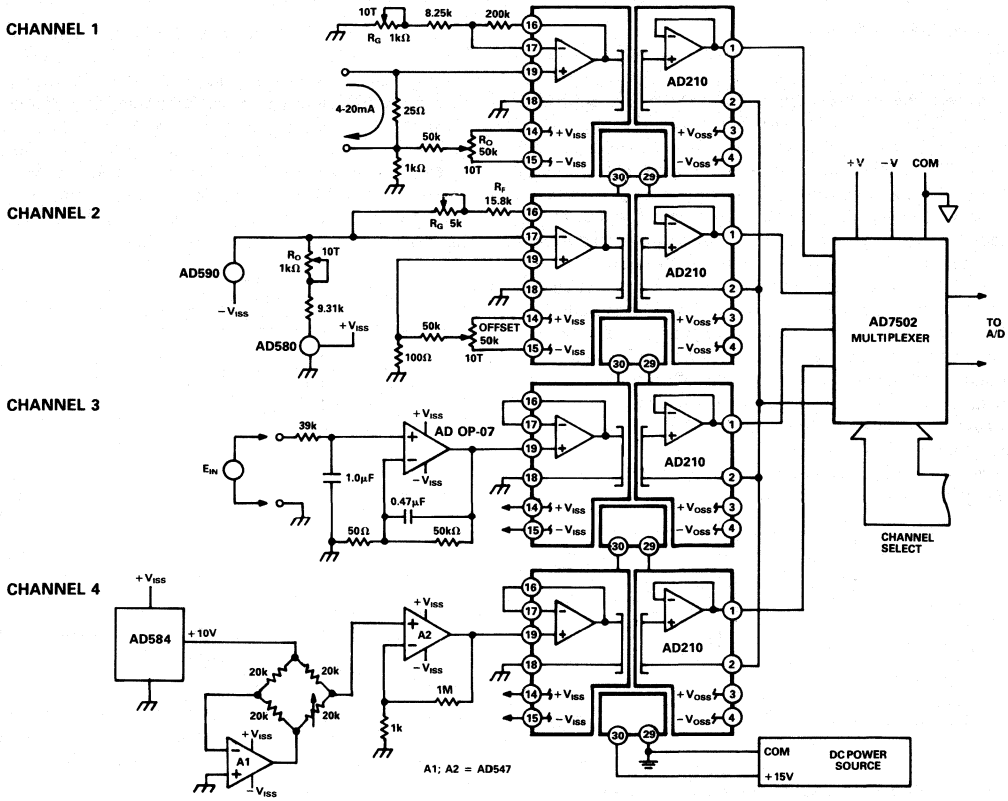


Figure 22. Multichannel Data Acquisition Front End

MULTICHANNEL DATA ACQUISITION FRONT-END

Illustrated in Figure 22 is a four-channel data acquisition front-end used to condition and isolate several common input signals found in various process applications. In this application, each AD210 will provide complete isolation from input to output as well as channel to channel. By using an isolator per channel, maximum protection and rejection of unwanted signals is obtained. The three-port design allows the AD210 to be configured as an input or output isolator. In this application the isolators are configured as input devices with the power port providing additional protection from possible power source faults.

Channel 1: The AD210 is used to convert a 4-20mA current loop input signal into a 0-10V input. The 25Ω shunt resistor converts the 4-20mA current into a +100 to +500mV signal. The signal is offset by −100mV via R_O to produce a 0 to +400mV input. This signal is amplified by a gain of 25 to produce the desired 0 to +10V output. With an open circuit, the AD210 will show −2.5V at the output.

Channel 2: In this channel, the AD210 is used to condition and isolate a current output temperature transducer, Model AD590. At +25°C, the AD590 produces a nominal current of 298.2μA. This level of current will change at a rate of 1μA/°C. At −17.8°C (0°F), The AD590 current will be reduced by 42.8μA to +255.4μA. The AD580 reference circuit provides an equal but opposite current, resulting in a zero net current flow, producing a 0V output from the AD210. At +100°C (+212°F), the AD590 current output will be 373.2μA minus the 255.4μA offsetting current from the AD580 circuit to yield a +117.8μA input current. This current is converted to a voltage via R_F and R_G to produce an output of +2.12V. Channel 2 will produce an output of +10mV/°F over a 0 to +212°F span.

Channel 3: Channel 3 is a low level input channel configured with a high gain amplifier used to condition millivolt signals. With the AD210's input set to unity and the input amplifier set for a gain of 1000, a ±10mV input will produce a ±10V at the AD210's output.

Channel 4: Channel 4 illustrates one possible configuration for conditioning a bridge circuit. The AD584 produces a +10V excitation voltage, while A1 inverts the voltage, producing negative excitation. A2 provides a gain of 1000V/V to amplify the low level bridge signal. Additional gain can be obtained by reconfiguration of the AD210's input amplifier. $\pm V_{ISS}$ provides the complete power for this circuit, eliminating the need for a separate isolated excitation source.

Each channel is individually addressed by the multiplexer's channel select. Additional filtering or signal conditioning should follow the multiplexer, prior to an analog-to-digital conversion stage.

ANALOG DEVICES

Economy, High Performance Self-Contained Isolation Amplifier

284J

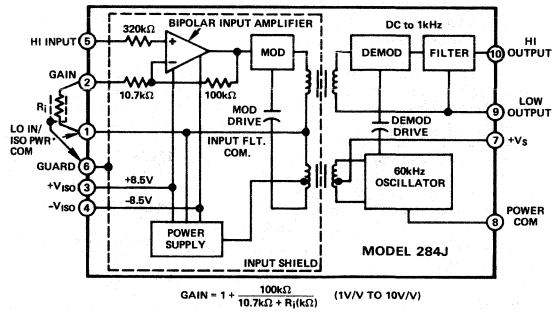
FEATURES

Low Nonlinearity: ±0.05% @ 10V pk-pk Output
High Gain Stability: ±0.0075%/°C, ±0.001%/1000 hours
Isolated Power Supply: ±8.5V dc @ ±5mA
High CMR: 110dB min with 5kΩ Imbalance
High CMV: ±5000V_{pk}, 10ms Pulse; ±2500V dc continuous
Small Size: 1.5" x 1.5" x 0.6"
Adjustable Gain: 1 to 10V/V; Single Resistor Adjust
Meets IEEE Std 472: Transient Protection (SWC)
Meets UL Std 544 Leakage: 2.0μA max @ 115V ac, 60Hz

APPLICATIONS

Biomedical and Patient Monitoring Instrumentation
Ground Loop Elimination in Industrial Control
Off-Ground Signal Measurements
4-20mA Isolated Current Loop Receiver

FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

Model 284J is a low cost isolation amplifier featuring isolated power, ±8.5V dc @ ±5mA loads, ±2500V dc off-ground isolation (CMV) and 110dB minimum CMR at 60Hz, 5kΩ source imbalance, in a compact 1.5" x 1.5" x 0.6" epoxy encapsulated package. This improved design achieves low nonlinearity of ±0.05% @ 10V pk-pk output, gain stability of ±0.0075%/°C and input offset drift of ±30μV/°C at G = 10V/V. Using modulation techniques with reliable transformer isolation, model 284J will interrupt ground loops, leakage paths and high voltage transients to ±5kV_{pk} (10ms pulse) providing dc to 1kHz (-3dB) response over an adjustable gain range of 1V/V to 10V/V. Model 284J's fully floating guarded input stage and floating isolated power for external input circuitry, offers versatility for both medical and industrial OEM applications.

WHERE TO USE MODEL 284J

Medical Applications: In all biomedical and patient monitoring equipment such as multi-lead ECG recorders and portable diagnostic designs, model 284J offers protection from lethal ground fault currents as well as 5kV defibrillator pulse inputs. Low level bioelectric signal recording is achieved with model 284J's low input noise (8μV p-p) and high CMR (110dB, min).

Industrial Applications: In computer interface systems, process signal isolators and high CMV instrumentation, model 284J offers complete galvanic isolation and protection against damage from transients and fault voltages. High level transducer interface is afforded with model 284J's 10V pk-pk input signal capability at a gain of 1V/V operation. In portable field designs, model 284J's single supply, low power drain of 85mW @ +12V operation offers long battery operation.

DESIGN FEATURES AND USER BENEFITS

Isolated Power: Dual ±8.5V dc @ ±5mA, completely isolated from the input power terminals (±2500V dc isolation), provides the capability to excite floating signal conditioners, front end buffer amplifiers and remote transducers such as thermistors or bridges.

Adjustable Gain: Model 284J's adjustable gain combined with its 10V pk-pk output signal dynamic range offers compatibility with a wide class of input signals. A single external resistor enables gain adjustment from 1V/V to 10V/V providing the flexibility of applying model 284J in both high level transducer interfacing as well as low level sensor measurements.

Floating, Guarded Front-End: The input stage of model 284J can directly accept floating differential signals, such as ECG biomedical signals, or it may be configured as a high performance instrumentation front-end to accept signals having CMV with respect to input power common.

High Reliability: Model 284J is a conservatively designed, compact module, capable of reliable operation in harsh environments. Model 284J has a calculated MTBF of over 400,000 hours and is designed to meet MIL-STD-202E environmental testing as well as the IEEE Standard for Transient Voltage Protection (472-1974: Surge Withstand Capability). As an additional assurance of reliability, every model 284J is factory tested for CMV and input ratings by application of 5kV pk, 10ms pulses, between input terminals as well as input/output terminals.

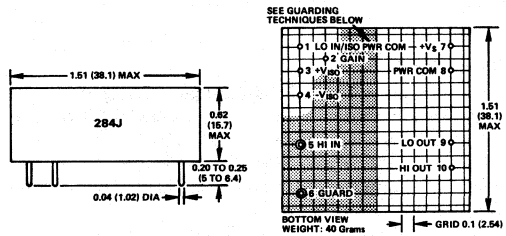
284J—SPECIFICATIONS (typical @ +25°C and V_S = ±15V unless otherwise noted)

MODEL	284J
GAIN (NON-INVERTING)	
Range (50kΩ Load)	1 to 10V/V
Formula	$\text{Gain} = [1 + \frac{100k\Omega}{10.7k\Omega + R_i(k\Omega)}]$
Deviation from Formula	±3%
vs. Time	±0.001%/1000 Hours
vs. Temperature (0 to +70°C)[1]	±0.0075%/°C
Nonlinearity, G = 1V/V to 10V/V[2]	±0.05%
INPUT VOLTAGE RATINGS	
Linear Differential Range, G = 1V/V	±5V min
Max Safe Differential Input	
Continuous	$240V_{rms}$
Pulse, 10ms duration, 1 pulse/10 sec	$\pm 6500V_{pk}$ max
Max CMV, Inputs to Outputs	
AC, 60Hz, 1 minute duration	$2500V_{rms}$
Pulse, 10ms duration, 1 pulse/10 sec	$\pm 2500V_{pk}$ max
With 510kΩ in series with Guard	$\pm 5000V_{pk}$ max
Continuous, ac or dc	$\pm 2500V_{pk}$ max
CMR, Inputs to Outputs, 60Hz, $R_S \leq 5k\Omega$	
Balanced Source Impedance	114dB
5kΩ Source Impedance Imbalance	110dB min
CMR, Inputs to Guard, 60Hz	
1kΩ Source Impedance Imbalance	78dB
Max Leakage Current, Inputs to Power Common @ 115V ac, 60Hz	2.0μA rms max
INPUT IMPEDANCE	
Differential	$10^8\Omega \| 70pF$
Overload	300kΩ
Common Mode	$5 \times 10^{10}\Omega \| 20pF$
INPUT DIFFERENCE CURRENT	
Initial, @ +25°C	±7nA max
vs. Temperature (0 to +70°C)	±0.1nA/°C
INPUT NOISE	
Voltage, G = 10V/V	
0.05Hz to 100Hz	8μV p-p
10Hz to 1kHz	10μV rms
Current	
0.05Hz to 100Hz	5pA p-p
FREQUENCY RESPONSE	
Small Signal, -3dB, G = 1V/V to 10V/V	1kHz
Slew Rate	25mV/μs
Full Power, 10V p-p Output	
Gain = 1V/V	700Hz
Gain = 10V/V	200Hz
Recovery Time, to ±100μV after Application of $\pm 6500V_{pk}$ Differential Input Pulse	200ms
OFFSET VOLTAGE REFERRED TO INPUT	
Initial, @ +25°C, Adjustable to Zero	±(5 + 20/G)mV
vs. Temperature (0 to +70°C)	±(15 + 150/G)μV/°C
vs. Supply Voltage	±1mV/%
RATED OUTPUT	
Voltage, 50kΩ Load	±5V min
Output Impedance	1kΩ
Output Ripple, 1MHz Bandwidth	5mV pk-pk
ISOLATED POWER OUTPUTS	
Voltage, ±5mA Load	±8.5V dc
Accuracy	±5%
Current	±5mA min
Regulation, No Load to Full Load	+0, -15%
Ripple, 100kHz Bandwidth	100mV p-p
POWER SUPPLY, SINGLE POLARITY[3]	
Voltage, Rated Performance	+15V dc
Voltage Operating	+(8 to 15.5)V dc
Current, Quiescent	+10mA
TEMPERATURE RANGE	
Rated Performance	0 to +70°C
Operating	-25°C to +85°C
Storage	-55°C to +85°C
CASE DIMENSIONS	1.5" x 1.5" x 0.62"

NOTES
[1]Gain temperature drift is specified as a percentage of output signal level.
[2]Gain nonlinearity is specified as a percentage of 10V pk-pk output span.
[3]Recommended power supply, ADI model 904, ±15V @ 50mA output.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

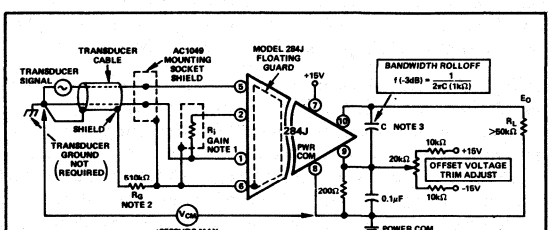


AC1049
SHIELDED MOUNTING SOCKET

INTERCONNECTION AND GUARDING TECHNIQUES

Model 284J can be applied directly to achieve rated performance as shown in Figure 1 below. To preserve the high CMR performance of model 284J, care must be taken to keep the capacitance balanced about the input terminals. A shield should be provided on the printed circuit board under model 284J as illustrated in the outline drawing above (screened area). The GUARD (Pin 6) should be connected to this shield. This guard-shield is provided with the mounting socket, model AC1049. A recommended guarding technique using model AC1049 is illustrated in Figure 1. To reduce effective cable capacitance, cable shield should be connected to the common mode signal source by connecting the shield as close as possible to the signal low.

Offset Voltage Trim Adjust: The trim adjust circuit shown in Figure 1 can be used to zero the output offset voltage over the gain range from 1 to 10V/V. The output terminals, HI OUT and LO OUT, can be floated with respect to PWR COM up to $\pm 50V_{pk}$ max, offering three-port isolation. A 0.1μF capacitor is required from LO OUT to PWR COM whenever the output terminals are floated with respect to PWR COM. LO OUT can be connected directly to PWR COM when output offset trimming is not required.



NOTE 1. GAIN RESISTOR, R_i, 1%, 50ppm/°C METAL FILM TYPE IS RECOMMENDED.
FOR GAIN = 1V/V, LEAVE TERMINAL 2 OPEN.
FOR GAIN = 10V/V, SHORT TERMINAL 2 TO TERMINAL 1

$$\text{GAIN} = 1 + \frac{100k\Omega}{10.7k\Omega + R_i(k\Omega)}$$

NOTE 2. GUARD RESISTOR, R_G, REQUIRED ONLY FOR CMV > $\pm 2500V_{PK}$ ($\pm 5kV_{PK}$ MAX).
R_G MAY BE MOUNTED ON AC1049 MOUNTING SOCKET USING STANDOFF PROVIDED.
(USE ¼ WATT, 5%, CARBON COMPOSITION TYPE; ALLEN BRADLEY RECOMMENDED).

NOTE 3. OUTPUT FILTER CAPACITOR, C, SELECT TO ROLLOFF NOISE AND OUTPUT RIPPLE: (e.g. SELECT C = 1.5μF FOR dc TO 100Hz BANDWIDTH).

Figure 1. Basic Isolator Interconnection

THEORY OF OPERATION

The remarkable performance of model 284J is derived from the carrier isolation technique which is used to transfer both signal and power between the amplifier's guarded input stage and the rest of the circuitry. The block diagram for model 284J is shown in Figure 2 below.

The 320kΩ input protection resistor limits the differential input current during periods of input amplifier saturation and also limits the differential fault current to approximately 35μA in case the preamplifier fails.

The bipolar input preamplifier operates single-ended (noninverting). Only a difference bias current flows with zero net bias current. A third wire return path for input bias current is not required. Gain can be set from 1V/V to 10V/V by changing the gain resistor, R_i. *To preserve high CMR, the gain resistor must be guarded.* Best performance is achieved by shorting terminal 2 to terminal 1 and operating model 284J at a gain of 10V/V.

For powering floating input circuitry such as buffer amplifiers, instrumentation amplifiers, calibration signals and transducers, dual isolated power is provided. High CMV isolation is achieved by the low-leakage transformer coupling between the input preamplifier, modulator section and the output circuitry. Only the 20pF leakage capacitance between the floating guarded input section and the rest of the circuitry keeps the CMR from being infinite.

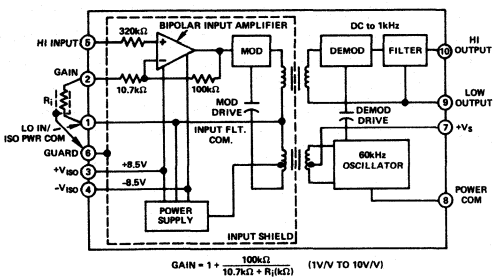


Figure 2. Block Diagram – Model 284J

INTERELECTRODE CAPACITANCE, TERMINAL RATINGS AND LEAKAGE CURRENTS LIMITS

Capacitance: Interelectrode terminal capacitance arising from stray coupling capacitance effects between the input terminals and the signal output terminals are each shunted by leakage resistance values exceeding 50kMΩ. Figure 3 illustrates the CMR ratings at 60Hz and 5kΩ source imbalance between signal input/output terminals, along with their respective capacitance.

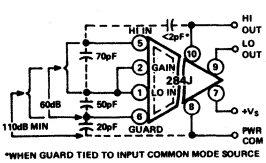


Figure 3. Model 284J Terminal Capacitance and CMR Ratings

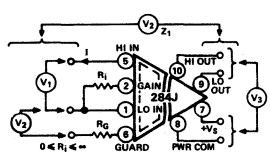


Figure 4. Model 284J Terminal Ratings

Terminal Ratings: CMV performance is given in both peak pulse and continuous ac or dc peak ratings. Pulse ratings are intended to support defibrillator and other transient voltages. Continuous peak ratings apply from dc up to the normal full power response frequencies. Figure 4 and Table 1 illustrate model 284J's ratings between terminals.

SYMBOL	RATING	REMARKS
V1 (pulse)	$\pm 6500V_{PK}$ (10ms)	Withstand Voltage, Defibrillator
V1 (cont.)	$\pm 240V_{RMS}$	Withstand Voltage, Steady State
V2 (pulse)	$\pm 2500V_{PK}$ (10ms) $R_G = 0$	Transient
V2 (pulse)	$\pm 5000V_{PK}$ (10ms) $R_G = 510k\Omega$	Isolation, Defibrillator
V2 (cont.)	$\pm 2500V_{PK}$	Isolation, Steady State
V3 (cont.)	$\pm 50V_{PK}$	Isolation, dc
Z1	50kMΩ‖20pF	Isolation Impedance
I	35μA rms	Input Fault Limit, DC to 60kHz

Table 1. Isolation Ratings Between Terminals

Leakage Current Limits: The low coupling capacitance between inputs and output yields a ground leakage current of less than 2.0μA rms at 115V ac, 60Hz (or 0.02μA/V ac). As shown in Figure 5, the transformer coupled modulator signal, through stray coupling, also creates an internally generated leakage current of about 5μA rms @ 60kHz. Line frequency leakage current levels are unaffected by the power on or off condition of model 284J.

For medical applications, model 284J is designed to improve on patient safety current limits proposed by F.D.A., U.L., A.A.M.I. and other regulatory agencies. (e.g. model 284J complies with leakage requirements for the Underwriters Laboratory STANDARD FOR SAFETY, MEDICAL AND DENTAL EQUIPMENT as established under UL544 for type A and B patient connected equipment – reference *Leakage Current*, paragraph 27.5).

In patient monitoring equipment, such as ECG recorders, model 284J will provide adequate isolation without exposing the patient to potentially lethal microshock hazards. Using passive components for input protection, this design limits input fault currents even under amplifier failure conditions.

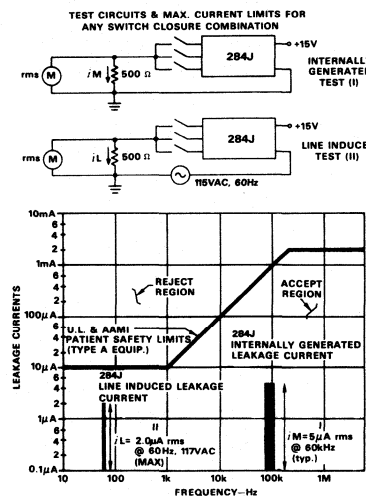


Figure 5. Model 284J Leakage Current Performance from Line Induced and Internally Generated (Modulator) Operating Conditions

5

PERFORMANCE CHARACTERISTICS

Common Mode Rejection: Input-to-Output CMR is dependent on source impedance imbalance, signal frequency and amplifier gain. CMR is rated at 115V ac, 60Hz and 5kΩ imbalance at a gain of 10V/V. Figure 6 illustrates CMR performance as a function of signal frequency. CMR approaches 146dB at dc with source imbalances as high as 5kΩ. As gain is decreased, CMR is reduced. At a gain of 1V/V, CMR is typically 6dB lower than at a gain of 10V/V.

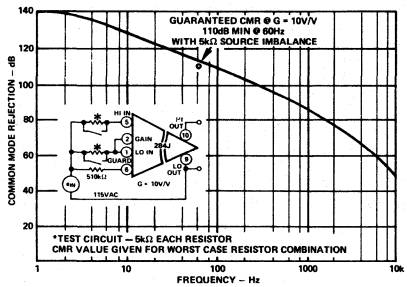


Figure 6. Common Mode Rejection vs. Frequency

Figure 7 illustrates the effect of source imbalance on CMR performance at 60Hz and Gain = 10V/V. CMR is typically 120dB at 60Hz and a balanced source. CMR is maintained greater than 80dB for source imbalances up to 100kΩ.

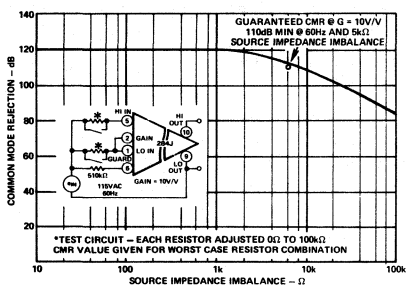


Figure 7. Common Mode Rejection vs. Source Impedance Imbalance

Input Voltage Noise: Voltage noise, referred to input, is dependent on gain and bandwidth as illustrated in Figure 8. RMS voltage noise is shown in a bandwidth from 0.05Hz to the frequency shown on the horizontal axis. The noise in a bandwidth from 0.05Hz to 100Hz is 8μV pk-pk at a gain of 10V/V. This value is derived by multiplying the rms value at f = 100Hz shown in Figure 8 (1.2μV rms) by 6.6.

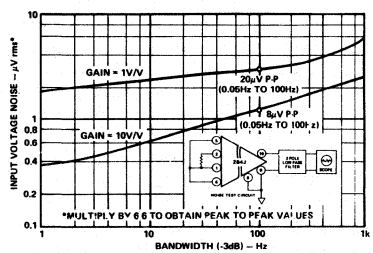


Figure 8. Input Voltage Noise vs. Bandwidth

For lowest noise performance, a low pass filter at the output should be used to selectively roll-off noise, output ripple and undesired signal frequencies beyond the bandwidth of interest (see note 3, Figure 1).

Input Offset Voltage Drift: Total input voltage drift is composed of two sources, input and output stage drifts and is gain dependent. The curve of Figure 9 illustrates the total input voltage drift over the gain range of 1 to 10V/V.

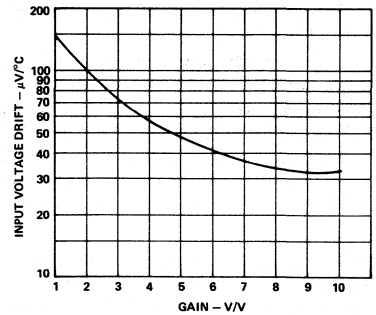
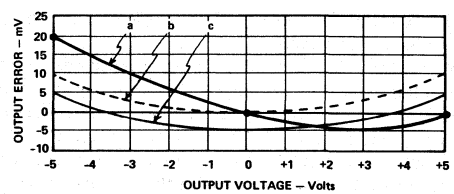


Figure 9. Input Offset Voltage Drift vs. Gain

Gain Nonlinearity: Linearity error is defined as the peak deviation of the output voltage from the best straight line and is specified as a % of peak-to-peak output voltage span; e.g. nonlinearity of model 284J operating at an output span of 10V pk-pk (±5V) is ±0.05% or ±5mV. In applying model 284J, highest accuracy is achieved by adjustment of gain and offset voltage to minimize the peak error over the operating output voltage span. A calibration technique illustrating how to minimize output error is shown below. In this example, model 284J is operating over an output span of +5V to -5V and a gain of 5V/V.



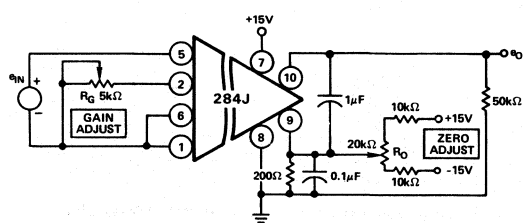


Figure 10. Gain and Offset Adjustment

GROUNDING PRACTICES

The more common sources of electrical noise arise from ground loops, electrostatic coupling and electromagnetic pickup. The guidelines listed below pertain to guarding low level, millivolt signals in hostile environments such as current shunt signals in "heavy industrial" plants.

Guidelines:

- Use twisted shielded cable to reduce inductive and capacitive pickup.
- Drive the transducer cable shield, S, with the common mode signal source, E_G, to reduce the effective cable capacitance as shown in Figure 11 below. This is accomplished by connecting the shield point S, as close as possible to the transducer signal low point B. This may not always be possible. In some cases the shield may be separated from signal low by a portion of the medium being measured (e.g. pressure transducer). This will cause a common mode signal, E_M, to be generated by the medium between the shield and the signal low. The 78dB CMR capability of model 284J between the input terminals (HI IN and LO IN) and GUARD, will work to suppress the common mode signal, E_M.
- To avoid ground loops and excessive hum, signal low, B, or the transducer cable shield, S, should never be grounded at more than one point.
- Dress unshielded leads short at the connection terminals and reduce the area formed by these leads to minimize inductive pickup.

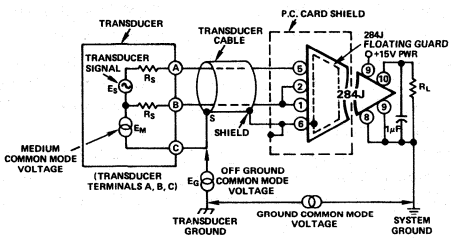


Figure 11. Transducer-Amplifier Interconnection

Isolated Power and Output Voltage Swing: Model 284J offers a floating power supply providing ±8.5V dc outputs with ±5mA output current rating. As shown in Figure 12, the minimum voltage output for $\pm V_{ISO}$, as well as the maximum load capability, is dependent on the input power supply, $+V_S$. Figure 12 also illustrates the typical output voltage range as both input supply, $+V_S$, and the isolated supply loads, $\pm I_L$, are varied. At ±5mA isolated load and V_S = +15V dc, model 284J can provide an output voltage swing of ±7.5V.

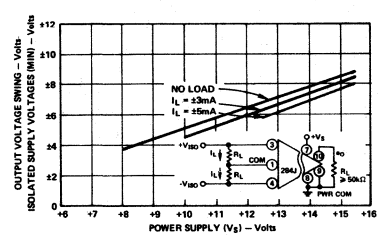


Figure 12. Isolated Power ($\pm V_{ISO}$) and Output Voltage Swing ($\pm E_O$) Versus Power Supply Input (V_S)

APPLICATIONS IN INDUSTRIAL MEASUREMENT AND CONTROL SYSTEMS

Remote Sensor Interface: In chemical, nuclear and metal processing industries, model 284J can be applied to measure and control off-ground millivolt signals in the presence of ±2500V dc CMV signals. In interface applications such as pH control systems of on-line process measurement systems such as pollution monitoring, model 284J offers complete galvanic isolation to eliminate troublesome ground loop problems. Isolated power outputs and adjustable gain add to the application flexibility of this model.

Figure 13 illustrates how model 284J can be combined with a low drift, 1μV/°C max, front-end amplifier, model AD517K, to interface low level transducer signals. Model 284J's isolated ±8.5V dc power and front-end guard eliminate ground loops and preserve high CMR (114dB @ 60Hz).

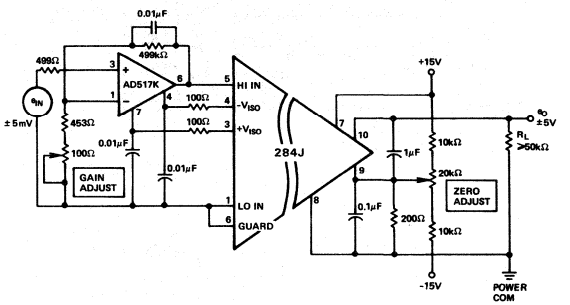


Figure 13. Input Signal Conditioning Using Isolated Power for Transducer Buffer Amplifier

Instrumentation Amplifier: Model 284J provides a floating guarded input stage capable of directly accepting isolated differential signals. The non-inverting, single-ended input stage offers simple two wire interconnection with floating input signals.

In applications where the isolated power is applied to transducers such as bridges which generate differential input signals with common mode voltages measured with respect to the isolated power common, model 284J can be connected as shown in Figure 14. To achieve high CMR with respect to the ISO PWR COM, the following trim procedure is recommended.

CMR Trim Procedure

1) Connect a 1V pk-pk oscillator between the +IN/-IN and IN COM terminals as shown in Figure 14.
2) Set the input frequency at 0.5Hz and adjust R1 for minimum e_O.
3) Set the input frequency at 60Hz and adjust R2 for minimum e_O.
4) Repeat steps 2 and 3 for best CMR performance.

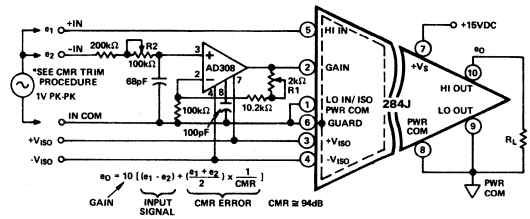


Figure 14. Application of 284J as Instrumentation Amplifier

APPLICATIONS IN BIOMEDICAL DESIGNS

Cardiac Monitoring: Heart signals can be masked by muscle noise, electrochemical noise, residual electrode voltages and 60Hz power line pickup. To achieve high performance in cardiac monitoring, model 284J's design provides high CMR in the dc to 100Hz bandwidth and substantial source impedance — to 5kΩ. An especially demanding ECG requirement is that of fetal heart monitoring as illustrated in Figure 15. The low input noise of model 284J and the dual CMR ratings are exploited in this application to extract the fetal ECG signals. The separation between the mother's and the fetal heartbeat is enhanced by the 78dB of CMR between the input electrodes and guard, while the 110dB of CMR from input to output ground screens out 60Hz pickup and other external interference.

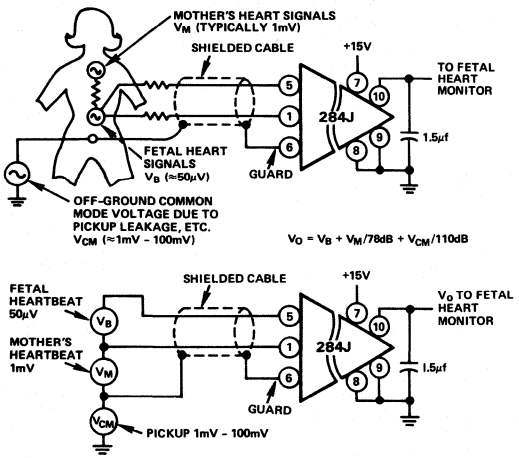


Figure 15. Fetal Heartbeat Monitoring

Single Lead ECG Recorder with Leads Off Indicator: In single lead applications model 284J offers simple two-wire hook-up to the ECG signal as illustrated in Figure 16. The floating signal can be connected directly to the HI IN and LO IN terminals using the GUARD tied to the patients' right leg for best CMR performance. Using the isolated power from model 284J an inexpensive calibration signal is easily provided. In ECG applications, model 284J provides a simple means to determine whenever a "Leads-Off" condition exists at the input. A "Leads-Off" condition ($R_S = \infty$) will cause the HI OUT terminal to be at a negative output saturation level; i.e. e_O = -8.5V to -9.5V @ V_S = +15V.

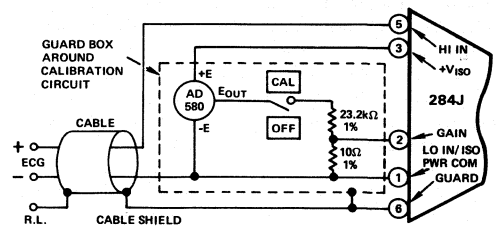


Figure 16. Single Lead ECG Recorder with 1mV Calibration Circuit and Leads Off Indicator

Multi-Lead ECG Recorder with Right Leg Drive: The small size, economy and isolated power makes model 284J an ideal isolation amplifier for application in clinical ECG recorders. Figure 17 illustrates how this new isolator can be applied in a high performance, portable multi-lead ECG recorder. In this application, model 284J's input is configured as an instrumentation amplifier with high CMR to the floating input common. The right leg drive offers improved CMR between input and isolated common by driving to zero any CMV existing between these points. The isolated power, $\pm V_{ISO}$, is used to drive the lead buffer amplifiers and the front-end, 1mV calibration signal.

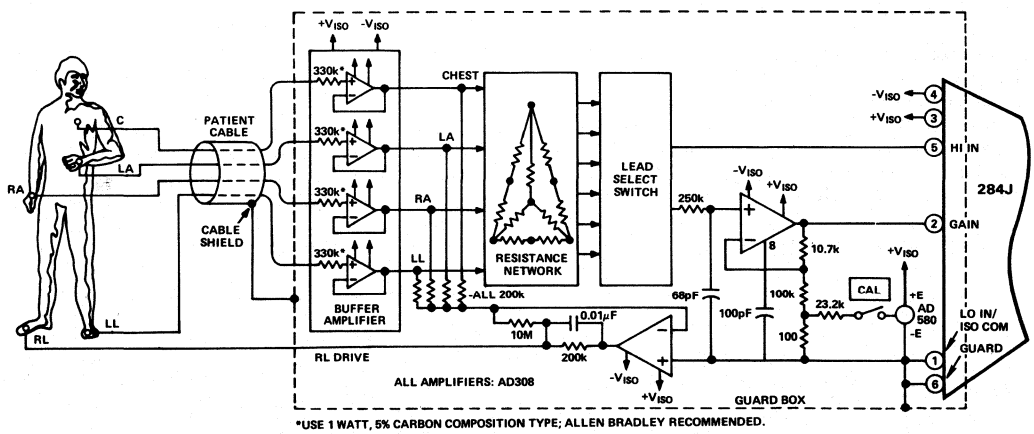


Figure 17. Multilead ECG Recorder Application Using 284J with Right Leg Drive Output

ANALOG DEVICES

High CMV, High Performance Synchronized Isolation Amplifiers

286J/281

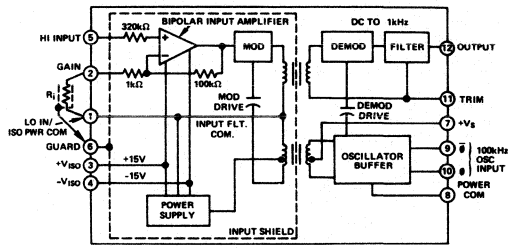
FEATURES

Low Cost
Single or Multi-Channel Capability Using External Oscillator
Isolated Power Supply: ±15V dc @ ±15mA
Low Nonlinearity: 0.05% @ 10V pk-pk Output
High Gain Stability: 0.001%/1000 Hours; 0.0075%/°C
Small Size: 1.5" x 1.5" x 0.62"
Low Input Offset Voltage Drift: 10μV/°C (Gain = 100V/V)
Wide Input/Output Dynamic Range: 20V pk-pk
High CMV Isolation: 2500V dc Continuous
Wide Gain Range: 1 to 100V/V

APPLICATIONS

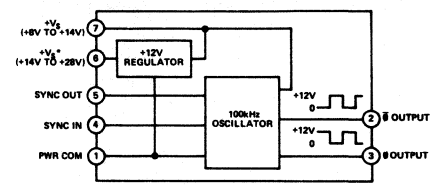
Ground Loop Elimination in Industrial and Process Control
High Voltage Protection in Data Acquisition Systems
Biomedical and Patient Monitoring Instrumentation
Off-Ground Signal Measurements

286J FUNCTIONAL BLOCK DIAGRAM



$$\text{GAIN} = 1 + \frac{100k\Omega}{1k\Omega + R_i\,(k\Omega)} \quad (1V/V \text{ TO } 100V/V)$$

281 FUNCTIONAL BLOCK DIAGRAM



*LEAVE TERMINAL 6 OPEN, WHEN POWER IS APPLIED TO TERMINAL 7

GENERAL DESCRIPTION

Model 286J is a low cost, compact, isolation amplifier that is optimized for single or multi-channel use in data acquisition systems for industrial and medical applications. A single external synchronizing oscillator can drive from 1 to 16 model 286J's, or a virtually limitless number of model 286's can be configured using multiple ganged oscillators. The oscillator drive circuit can be supplied by the user of specified in a compact, low cost, epoxy encapsulated module, model 281, which also includes a voltage regulator for operation over a wide single voltage range of +8V to +28V.

In addition to providing multi-channel operation, this new design features adjustable gain, 1 to 100V/V, dual isolated power, ±15V dc @ ±15mA, ±2500V dc off ground isolation (CMV) and 110dB minimum CMR at 60Hz, 5kΩ source imbalance, in a compact 1.5" x 1.5" x 0.6" epoxy encapsulated package. Model 286J achieves a low input noise of 8μV pk-pk (100Hz bandwidth, G = 100V/V), nonlinearity of ±0.05% @ 10V pk-pk output, and an input/output dynamic range of 20V pk-pk.

Using modulation techniques with reliable transformer isolation, model 286J will interrupt ground loops, leakage paths, and high voltage transients to ±5kV pk (10ms pulse), providing dc to 1kHz (-3dB) response.

WHERE TO USE MODEL 286J

Industrial Applications: In multi-channel data acquisition systems, computer interface systems, process signal isolators and high CMV instrumentation, model 286J offers complete galvanic isolation and protection against damage from transients and fault voltages. High level transducer interface capability is afforded with model 286J's 20V pk-pk input signal range at a gain of 1V/V operation. In portable multi-channel designs, model 286J's single supply, wide range operation (+8V to +16V) offers simple battery operation.

Medical Applications: In biomedical and patient monitoring equipment such as multi-channel VCG, ECG, and polygraph recorders, model 286J offers protection from lethal ground fault currents as well as 5kV defibrillator pulse inputs. Low level bioelectric signal recording is achieved with model 286J's low input noise (8μV pk-pk @ G = 100V/V) and high CMR (110dB, min @ 60Hz).

DESIGN FEATURES AND USER BENEFITS

High Reliability: Model 286J is a conservatively designed, compact module, capable of reliable operation in harsh environments. Model 286J has a calculated MTBF of 392,125 hours and is designed to meet MIL-STD-202E environmental testing as well as the IEEE Standard for Transient Voltage Protection (472-1974: Surge Withstand Capability). As an additional assurance of reliability, every model 286J is factory tested for CMV and input ratings by application of 5kV pk, 10ms pulses, between input terminals as well as input/output terminals.

Isolated Power Supply: Dual ±15V dc @ ±15mA, completely isolated from the input power terminals (±2500V dc isolation), provides the capability to excite floating signal conditioners, front end buffer amplifiers as well as remote transducers such as thermistors or bridges.

Adjustable Gain: A single external resistor enables gain adjustment from 1V/V to 100V/V providing the flexibility of applying model 286J in both high-level transducer interfacing as well as low-level sensor measurements.

5

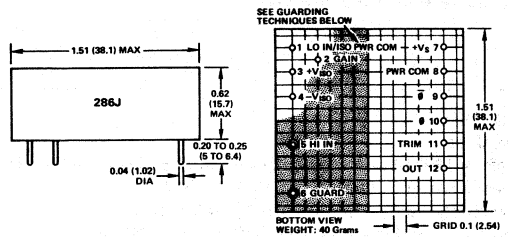
286J/281—SPECIFICATIONS

MODEL	286J*
GAIN (NONINVERTING)	
Range (50kΩ Load)	1 to 100V/V
Formula	Gain = 1+ [100kΩ/(1kΩ+R_i(kΩ))]
Deviation from Formula	±4%
vs. Temperature (0 to +70°C)[1]	±0.0075%/°C
vs. Time	±0.001%/1000 hours
Nonlinearity,[2] ±5V Output (G = 1 to 100V/V)	±0.05%
Nonlinearity,[2] ±10V Output (G = 1 to 100V/V)	±0.2%
INPUT VOLTAGE RATINGS	
Linear Differential Range, G = 1V/V	±10V min
Max Safe Differntial Input	
Continuous	240V rms
Pulse, 10ms Duration, 1 Pulse/10sec	±6500V pk max
Max CMV, Inputs to Outputs	
ac, 60Hz, 1 Minute Duration	2500V rms
Pulse, 10ms Duration, 1 Pulse/10sec	±2500V pk max
With 510kΩ in series with Guard	±5000V pk max
Continuous, ac or dc	±2500V pk max
CMR, Inputs to Outputs, 60Hz, $R_S \leq 5k\Omega$	
Balanced Source Impedance	114dB
5kΩ Source Impedance Imbalance	110dB min
CMR, Inputs to Guard, 60Hz	
1kΩ Source Impedance Imbalance	78dB
Max Leakage Current, Inputs to Power Common	
@ 115V ac 60Hz	2.5μA rms max
OFFSET VOLTAGE, REFERRED TO INPUT	
Initial, @ +25°C (Adjustable to zero)	±(5 + 45/G) mV
vs. Temperature (0 to +70°C)	
At Gain = 100V/V	±10μV/°C
At Other Gains (1 to 100V/V)	±(7 + 250/G)μV/°C
vs. Supply Voltage	±1mV/%
INPUT IMPEDANCE	
Differential	$10^8\Omega$‖150pF
Overload	300kΩ
Common Mode	5 x $10^{10}\Omega$‖20pF
INPUT DIFFERENCE CURRENT	
Initial, @ +25°C	±7nA max
vs. Temperature (0 to +70°C)	±0.1nA/°C
INPUT NOISE (Gain = 100V/V)	
Voltage	
0.05Hz to 100Hz	8μV pk-pk
10Hz to 1kHz	3.0μV rms
Current	
0.05Hz to 100Hz	5pA pk-pk
FREQUENCY RESPONSE (Gain: 1V/V to 100V/V)	
Small Signal Bandwidth, -3dB	1.0kHz
Slew Rate	25mV/μs
Full Power, 10V pk-pk Output	900Hz
Full Power, 20V pk-pk Output	400Hz
Recovery Time, to ±100μV	200ms
RATED OUTPUT	
Voltage, 50kΩ Load	±10V min
Output Impedance	1kΩ
Output Ripple, 1mHz Bandwidth	20mV pk-pk
OSCILLATOR DRIVE INPUT*	
Input Voltage	(8 to 16)V pk-pk
Input Frequency	100kHz ±5%, max
ISOLATED POWER SUPPLY	
Voltage	±15V dc
Accuracy	0, -6%
Current	±15mA min
Regulation, No Load to Full Load	+0, -10%
Ripple, 100kHz Bandwidth	200mV pk-pk
POWER SUPPLY, SINGLE POLARITY[3]	
Voltage, Rated Performance	+15V dc
Voltage, Operating	+(8V dc to 16V dc)
Current, Quiescent	+13mA
TEMPERATURE RANGE	
Rated Performance	0 to +70°C
Storage	-55°C to +85°C
CASE DIMENSIONS	1.5" x 1.5" x 0.62"

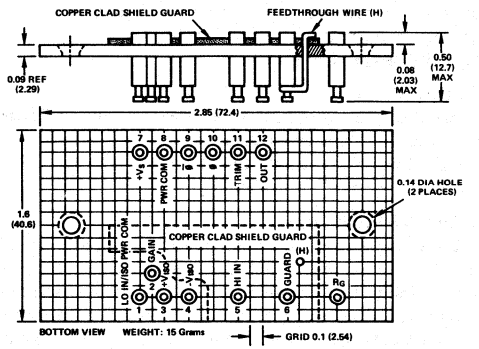
[1] Gain temperature drift is specified as a percentage of output signal level.
[2] Gain nonlinearity is specified as a percentage of output signal span.
[3] Recommended power supply, ADI model 904, ±15V @ ±50mA output.
*Specifications are for model 286J when driven by ADI model 281 oscillator circuit (see Figure 12).
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



SHIELDED MOUNTING SOCKET AC1054



GUARDING TECHNIQUES

To preserve the high CMR performance of model 286, care must be taken to keep the capacitance balanced about the input terminals. A shield should be provided on the printed circuit board under model 286 as illustrated in the outline drawing above (screened area). The GUARD (pin 6) must be connected to this shield. This shield is provided with the mounting socket, model AC1054 (solder feedthrough wire to the socket guard pin and copper foil surface.) A recommended guarding technique using model AC1054 is illustrated in Figure 1.

Best CMR performance will be achieved by using twisted, shielded cable to reduce inductive and capacitive pickup. To reduce effective cable capacitance, cable shield should be connected to the common mode signal source by connecting the shield as close as possible to signal low as shown in Figure 1.

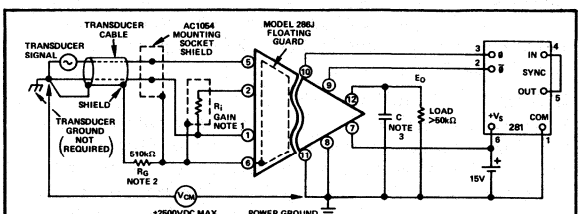


Figure 1. Basic Isolator Interconnection

THEORY OF OPERATION

The remarkable performance of model 286J is derived from the carrier isolation technique which is used to transfer both signal and power between the amplifier's guarded input stage and the rest of the circuitry. The block diagram for model 286J is shown in Figure 2 below.

The 320kΩ input protection resistor limits the differential input current during periods of input amplifier saturation and also limits the differential fault current to approximately 50μA in case the preamplifier fails.

The bipolar input preamplifier operates single-ended (non-inverting). Only a difference bias current flows with zero net bias current. A third wire return path for input bias current is not required. Gain can be set from 1V/V to 100V/V by changing the gain resistor, R_i. *To preserve high CMR, the gain resistor must be guarded.* Best performance is achieved by shorting terminal 2 to terminal 1 and operating model 286J at a gain of 100V/V.

For powering floating input circuitry such as buffer amplifiers, instrumentation amplifiers, calibration signals and transducers, dual isolated power is provided. High CMV isolation is achieved by the low-leakage transformer coupling between the input preamplifier, modulator section and the output circuitry.

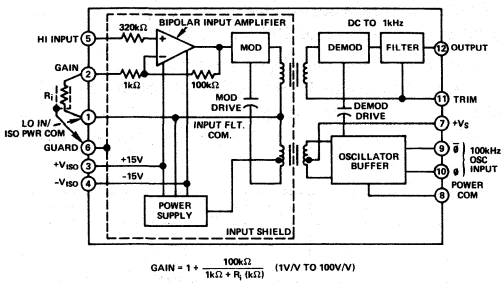


Figure 2. Block Diagram – Model 286J

OPTIONAL TRIM ADJUSTMENTS

Model 286J can be applied directly to achieve rated performance as shown in Figure 1, on previous page. Additional trim adjustment capability for bandwidth, output offset voltage and gain (for gains greater than 100V/V) is easily provided as shown in Figure 3 (below). The OUT and TRIM terminals can be floated with respect to PWR COM up to ±50V pk, max offering three-port isolation.

The TRIM terminal (pin 11) must be connected to the PWR COM terminal (pin 8) when not used to adjust the output offset voltage. A 0.1μF capacitor from pin 11 to PWR COM is recommended whenever the TRIM terminal is used.

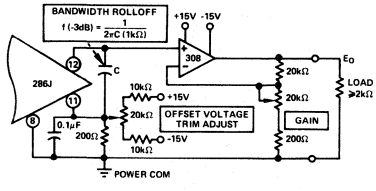


Figure 3. Optional Connections: Offset Voltage Trim Adjust, Bandwidth (-3dB) Rolloff and Gain Adjust (G>100V/V)

INTERELECTRODE CAPACITANCE, TERMINAL RATINGS AND LEAKAGE CURRENTS LIMITS

Capacitance: Interelectrode terminal capacitance arising from stray coupling capacitance effects between the input terminals and the signal output terminals are each shunted by leakage resistance values exceeding 50kMΩ. Figure 4 illustrates the CMR ratings at 60Hz and 5kΩ source imbalance between signal input/output terminals, along with their respective capacitance.

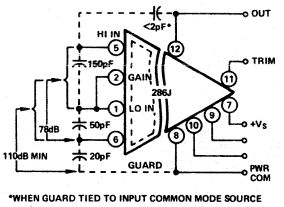


Figure 4. Model 286J Terminal Capacitance and CMR Ratings

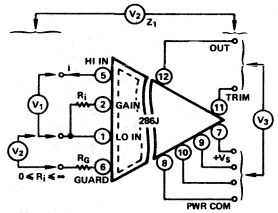


Figure 5. Model 286J Terminal Ratings

Terminal Ratings: CMV performance is given in both peak pulse and continuous ac or dc peak ratings. Pulse ratings are intended to support defibrillator and other transient voltages. Continuous peak ratings apply from dc up to the normal full power response frequencies. Figure 5 and Table 1 illustrate model 286J ratings between terminals.

SYMBOL	RATING	REMARKS
V1 (pulse)	±6500V_{PK} (10ms)	Withstand Voltage, Defibrillator
V1 (cont.)	±240V_{RMS}	Withstand Voltage, Steady State
V2 (pulse)	±2500V_{PK} (10ms) R_G = 0	Transient
V2 (pulse)	±5000V_{PK} (10ms) R_G = 510kΩ	Isolation, Defibrillator
V2 (cont.)	±2500V_{PK}	Isolation, Steady State
V3 (cont.)	±50V_{PK}	Isolation, dc
Z1	50kMΩ‖20pF	Isolation Impedance
I	50μA rms	Input Fault Limit, dc to 200kHz

Table 1. Isolation Ratings Between Terminals

Leakage Current Limits: The low coupling capacitance between inputs and output yields a ground leakage current of less than 2.5μA rms at 115V ac, 60Hz (or 0.02μA/V ac). As shown in Figure 6, the transformer coupled modulator signal, through stray coupling, also creates an internally generated leakage current of about 5μA rms @ 100kHz. Line frequency leakage current levels are unaffected by the power on or off condition of model 286J.

For medical applications, model 286J is designed to improve on patient safety current limits proposed by F.D.A., U.L., A.A.M.I. and other regulatory agencies (e.g., model 286J complies with leakage requirements for the Underwriters Laboratory STANDARD FOR SAFETY, MEDICAL AND DENTAL EQUIPMENT as established under UL544 for type A and B patient connected equipment – reference *Leakage Current*, paragraph 27.5).

In patient monitoring equipment, such as ECG recorders, model 286J will provide adequate isolation without exposing the patient to potentially lethal microshock hazards. Using passive components for input protection, this design limits input fault currents even under amplifier failure conditions.

5

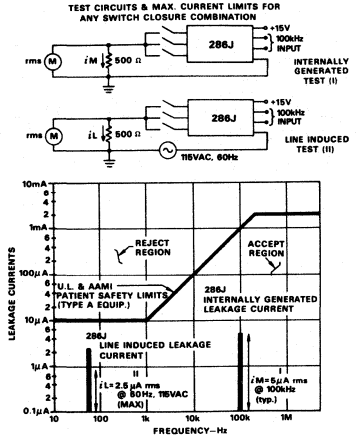


Figure 6. Model 286J Leakage Current Performance from Line Induced and Internally Generated (Modulator) Operating Conditions

PERFORMANCE CHARACTERISTICS

Common Mode Rejection: Input-to-Output CMR is dependent on source impedance imbalance, signal frequency and amplifier gain. CMR is rated at 115V ac, 60Hz and 5kΩ imbalance at a gain of 100V/V. Figure 7 illustrates CMR performance as a function of signal frequency. CMR approaches 156dB at dc with source imbalances as high as 5kΩ. As gain is decreased, CMR is reduced. At a gain of 1V/V CMR is typically 6dB lower than at gain of 100V/V.

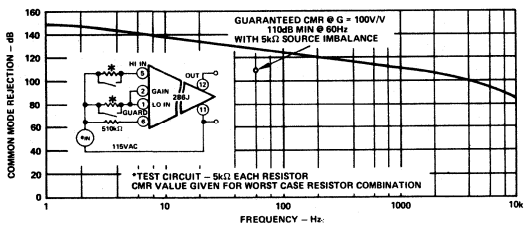


Figure 7. Common Mode Rejection vs. Frequency

Figure 8 illustrates the effect of source imbalance on CMR performance at 60Hz at gains of 1V/V, 10V/V, and 100V/V. CMR is typically 140dB at 60Hz and a balanced source. CMR is maintained greater than 80dB for source imbalances up to 100kΩ.

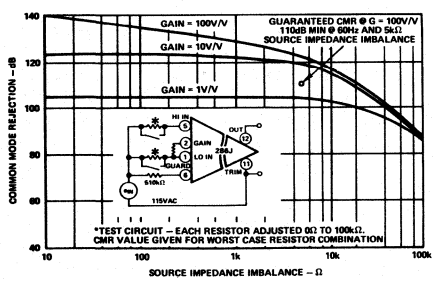


Figure 8. Common Mode Rejection vs. Source Impedance Imbalance

Gain Nonlinearity: Linearity error is defined as the deviation of the output voltage from the best straight line and is specified as a % of peak-to-peak output voltage span; e.g., nonlinearity of model 286J operating at an output span of 10V pk-pk (±5V) is ±0.05% or ±5mV. Figure 9 illustrates gain nonlinearity for any output span to 20V pk-pk (±10V).

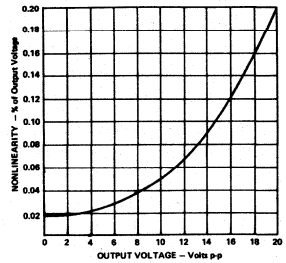


Figure 9. Gain Nonlinearity vs. Output Voltage

Input Voltage Noise: Voltage noise, referred to input, is dependent on gain and bandwidth as illustrated in Figure 10. RMS voltage noise is shown in a bandwidth from 0.05Hz to the frequency shown on the horizontal axis. The noise in a bandwidth from 0.05Hz to 100Hz is 8μV pk-pk at a gain of 100V/V. This value is derived by multiplying the rms value at f = 100Hz shown in Figure 10 (1.2μV rms) by 6.6.

For best noise performance in particular applications, a low pass filter at the output should be used to selectively roll-off noise and undesired signal frequencies beyond the bandwidth of interest (see note 3, Figure 1). Increasing gain will also reduce the input noise.

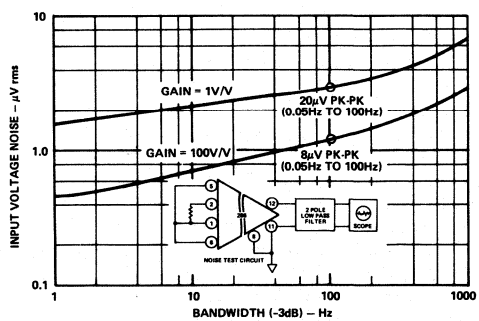


Figure 10. Input Voltage Noise vs. Bandwidth

Input Offset Voltage Drift: Total input drift is composed of two sources, input and output stage drifts and is gain dependent. The curve of Figure 11 illustrates total input drift over the gain range of 1 to 100V/V.

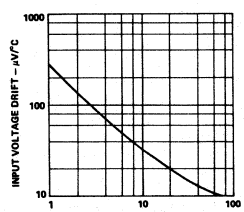


Figure 11. Input Offset Voltage Drift vs. Gain

REFERENCE EXCITATION OSCILLATOR

When applying model 286J, the user has the option of building a low cost 100kHz excitation oscillator, as shown in Figure 12, or purchasing a module from Analog Devices – model 281.

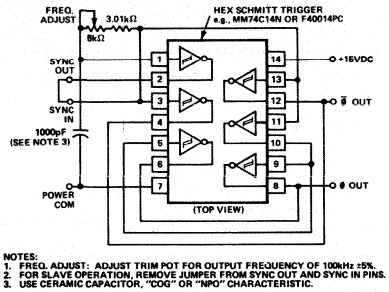


Figure 12. Model 281 100kHz Oscillator – Logic and Interconnection Diagram

The block diagram of model 281 is shown in Figure 13. An internal +12V dc regulator is provided to permit the user the option of operating over two, pin selectable, power input ranges; terminal 6 offers a range of +14V dc to +28V dc; terminal 7 offers an input range of +8V dc to +14V dc.

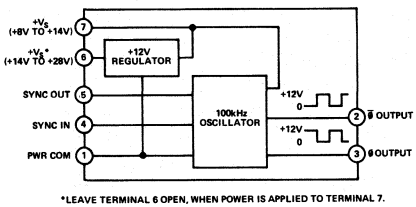


Figure 13. Model 281 Block Diagram

Model 281 oscillator is capable of driving up to 16 model 286J's as shown in Figure 14. An additional model 281 may be driven in a slave-mode, as shown in Figure 15, to expand the total system channels from 16 to 32. By adding additional model 281's in this manner, systems of over 1000 channels may be easily configured.

EXTERNAL OSCILLATOR INTERCONNECTION

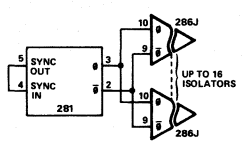


Figure 14. Model 281/286 Connection for Driving from 1 to 16 Isolators

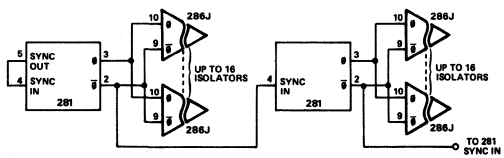


Figure 15. Model 281/286 Connection for Driving > 16 Isolators

SPECIFICATIONS

(typical @ +25° C and V_S = +15V dc unless otherwise noted)

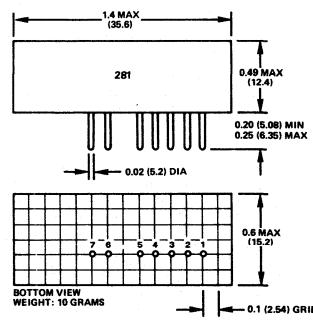
MODEL	281
OUTPUT	
Frequency	100kHz ±5%
Waveform	Squarewave
Voltage (ϕ and $\bar{\phi}$ terminals)	0 to +12V pk
Fan-Out[1,2]	16 max
POWER SUPPLY RANGE[3]	
High Input, Pin 6	+(14 to 28)V dc
Quiescent Current, N.L.	+5mA
F.L.	+16mA
Low Input, Pin 7	+(8 to 14)V dc
Quiescent Current, N.L.	+12mA
F.L.	+33mA
TEMPERATURE	
Rated Performance	0 to +70°C
Storage	-55°C to +85°C
MECHANICAL	
Case Size	1.4" x 0.6" x 0.49"
Weight	10 grams

[1] Model 286J oscillator drive input represents unity oscillator load.
[2] For applications requiring more than 16 286J's, additional 281's may be used in a master/slave mode. Refer to Figure 15.
[3] Full load consists of 16 model 286J's and 281 oscillator slave.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

MODEL 281



PIN TERMINAL IDENTIFICATION

1	POWER COMMON	5	SYNC OUTPUT
2	$\bar{\phi}$ OUTPUT	6	$+V_S$: HIGH RANGE +(14 to 28)V_{dc}
3	ϕ OUTPUT	7	$+V_S$: LOW RANGE +(8 to 14)V_{dc}
4	SYNC INPUT		

MATING SOCKET: CINCH #16 DIP OR EQUIVALENT

GUIDELINES ON EFFECTIVE SHIELDING & GROUNDING PRACTICES

- Use twisted shielded cable to reduce inductive and capacitive pickup.
- Drive the transducer cable shield, S, with the common mode signal source, E_G, to reduce the effective cable capacitance as shown in Figure 16. This is accomplished by connecting the shield point S, as close as possible to the transducer signal low point B. This may not always be possible. In some cases the shield may be separated from signal low by a portion of the medium being measured (e.g. pressure transducer). This will cause a common mode signal, E_M, to be generated by the medium between the shield and the signal low. The 78dB CMR capability of model 286J between the input terminals (HI IN and LO IN) and GUARD, will work to suppress the common mode signal, E_M.
- Dress unshielded leads short at the connection terminals and reduce the area formed by these leads to minimize inductive pickup.

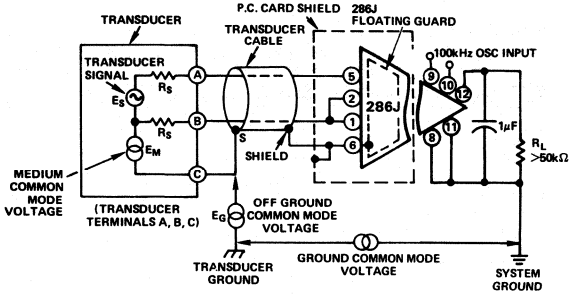
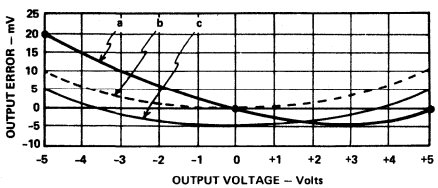


Figure 16. Transducer – Amplifier Interface

GAIN AND OFFSET TRIM PROCEDURE

In applying the isolation amplifier, highest accuracy is achieved by adjustment of gain and offset voltage to minimize the peak error encountered over the selected output voltage span. The following procedure illustrates a calibration technique which can be used to minimize output error. In this example, the output span is +5V to -5V and operation at Gain = 10V/V is desired.

1. Apply e_{IN} = 0 volts and adjust R_O for e_O = 0 volts.
2. Apply e_{IN} = +0.500V dc and adjust R_G for e_O = +5.000V dc.
3. Apply e_{IN} = –0.500V dc and measure the output error (see curve a).
4. Adjust R_G until the output error is one half that measured in step 3 (see curve b).
5. Apply +0.500V dc and adjust R_O until the output error is one half that measured in step 4 (see curve c).



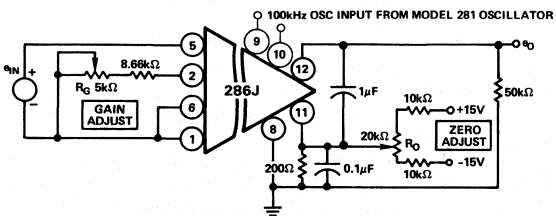


Figure 17. Gain and Offset Adjustment

APPLICATIONS IN INDUSTRIAL MEASUREMENT AND CONTROL SYSTEMS

Remote Sensor Interface: In chemical, nuclear and metal processing industries, model 286J can be applied to measure and control off-ground millivolt signals in the presence of ±2500V CMV signals. In interface applications such as pH control systems or on-line process measurement systems such as pollution monitoring, model 286J offers complete galvanic isolation to eliminate troublesome ground loop problems. Isolated power outputs and adjustable gain add to the application flexibility of this model.

Figure 18 illustrates how model 286J can be combined with a low drift, 1μV/°C max, front-end amplifier, model AD510K, to interface low level transducer signals. Model 286J's isolated ±15V dc power and front-end guard eliminate ground loops and preserve high CMR (110dB min @ 60Hz).

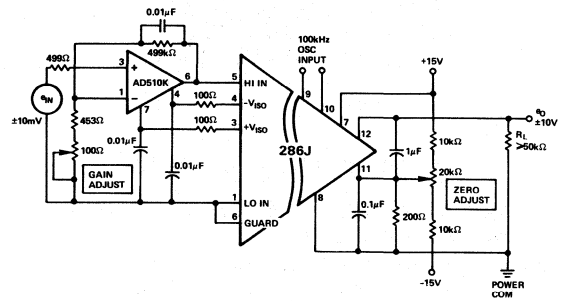


Figure 18. Input Signal Conditioning Using Isolated Power for Transducer Buffer Amplifier

Current Loop Receiver: Model 286J can be applied to measurement of analog quantities transmitted via 4-20mA current loops over substantial distances through harsh environments. Figure 19 shows an application of model 286J as a current loop receiver. A 25Ω resistor converts the 4–20mA current input from a remote loop to a 100–500mV differential voltage input, which the 286J amplifies, isolates, and translates to a 0 to +5V output level at local system ground.

Among the most-helpful characteristics of the 286J in this kind of measurement are the high common-mode rejection (110dB minimum at 60Hz with 5kΩ source unbalance) and the high common-mode rating (±2500 volts dc). The former means low noise pickup; the latter means excellent isolation and protection against large transients. The high common-mode rejection, permitting relatively low input voltage to be used (0.4V span, in this case), permits the use of a low current-metering resistance, which in turn results in low compliance-voltage loading on the current loop, and therefore permits insertion into existing loops without encountering overrange problems. The gain of 12.5 provides a substantial output span, and the floating output permits biasing to a 0 to 5V range.

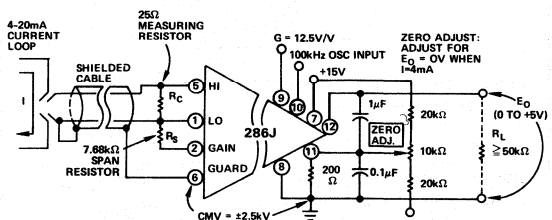


Figure 19. Isolated Analog Interface; 4 to 20mA is Converted to 0 to +5V at the Output, with Up to ±2500V of Isolation

ANALOG DEVICES

Precision, Wide Bandwidth, Synchronized Isolation Amplifier

289

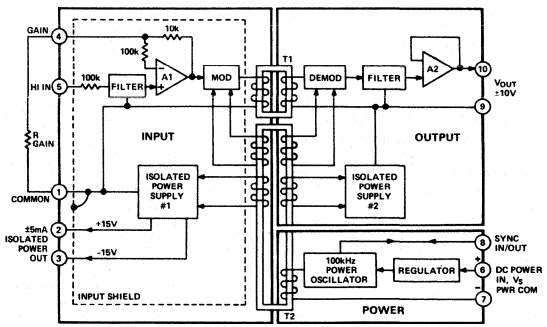
FEATURES

Low Nonlinearity: ±0.012% max (289L)
Frequency Response: (-3dB) dc to 20kHz
(Full Power) dc to 5kHz
Gain Adjustable 1 to 100V/V, Single Resistor
3-Port Isolation: ±2500V CMV Isolation Input/Output
Low Gain Drift: ±0.005%/°C max
Floating Power Output: ±15V @ ±5mA
120dB CMR at 60Hz: Fully Shielded Input Stage
Meets UL Std. 544 Leakage: 2μA rms max, @ 115V ac, 60Hz

APPLICATIONS

Multi-Channel Data Acquisition Systems
Current Shunt Measurements
Process Signal Isolator
High Voltage Instrumentation Amplifier
SCR Motor Control

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

Model 289 is a wideband, accurate, low cost isolation amplifier designed for instrumentation and industrial applications. Three accuracy selections are available offering guaranteed gain nonlinearity error at 10V p-p output: ±0.012% max (289L), ±0.025% max (289K), ±0.05% max (289J). All versions of the 289 provide a small signal frequency response from dc to 20kHz (-3dB) and a large signal response from dc to 5kHz (full power) at a gain of 1V/V. This new design offers true 3-port isolation, ±2500V dc between inputs and outputs (or power inputs), as well as 240V rms between power supply inputs and signal outputs. Using carrier modulation techniques with transformer isolation, model 289 interrupts ground loops and leakage paths and minimizes the effect of high voltage transients. It provides 120dB Common Mode Rejection between input and output common. The high CMV and CMR ratings of the model 289 facilitate accurate measurements in the presence of noisy electrical equipment such as motors and relays.

WHERE TO USE THE MODEL 289

The model 289 is designed to interface single and multichannel data acquisition systems with dc sensors such as thermocouples, strain gauges and other low level signals in harsh industrial environments. Providing high accuracy with complete galvanic isolation, and protection from line transients of fault voltages, model 289's performance is suitable for applications such as process controllers, current loop receivers, weighing systems, high CMV instrumentation and computer interface systems.

Use the model 289 when data must be acquired from floating transducers in computerized process control systems. The photograph above shows a typical multichannel application allowing potential differences or interrupting ground loops, among transducers, or between transducers and local ground.

DESIGN FEATURES AND USER BENEFITS

Isolated Power: The floating power supply section provides isolated ±15V outputs @ ±5mA. Isolated power is regulated to within ±5%. This feature permits model 289 to excite floating signal conditioners, front-end buffer amplifiers and remote transducers such as thermistors or bridges, eliminating the need for a separate isolated dc/dc converter.

Adjustable Gain: A single external resistor adjusts the model 289's gain from 1V/V to 100V/V for applications in high and low level transducer interfacing.

Synchronized: The model 289 provides a synchronization terminal for use in multichannel applications. Connecting the synchronization terminals of model 289s synchronizes their internal oscillators, thereby eliminating the problem of oscillator "beat frequency" interference that sometimes occurs when isolation amplifiers are closely mounted.

Internal Voltage Regulator: Improves power supply rejection and helps prevent carrier oscillator spikes from being broadcast via the isolator power terminal to the rest of the system.

Buffered Output: Prevents gain errors when an isolation amplifier is followed by a resistive load of low impedance. Model 289 can drive a 2kΩ load.

Three-Port Isolation: Provides true galvanic isolation between input, output and power supply ports. Eliminates need for power supply and output ports being returned through a common terminal.

Reliability: Model 289 is conservatively designed to be capable of reliable operation in harsh environments. Model 289 has a calculated MTBF of 271,835 hours. In addition, the model 289 meets UL Std. 544 leakage, 2μA rms @ 115V ac, 60Hz.

5

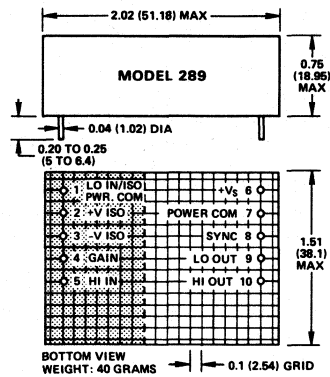
289—SPECIFICATIONS (typical @ +25°C and V_S = ±14.4V to +25V dc unless otherwise noted)

Model	289J	289K	289L
GAIN (NONINVERTING)			
Range		1 to 100V/V	
Formula		$G = 1 + \frac{10k\Omega}{R_G(k\Omega)}$	
Deviation from Formula		±1.5% max	
vs. Temperature (0 to +70°C)[1]		15ppm/°C typ (50ppm/°C max)	
Nonlinearity, (±5V Swing)[2,3]	±0.05% max	±0.025% max	±0.012% max
INPUT VOLTAGE RATINGS			
Linear Differential Range (G = 1V/V)		±10V min	
Max Safe Differential Input			
Continuous		120V rms	
1 Minute		240V rms	
Max CMV (Inputs to Outputs)			
Continuous ac or dc		±2500V peak max	
ac, 60Hz, 1 Minute Duration		2500V rms	
CMR, Inputs to Outputs 60Hz			
$R_S \leq 1k\Omega$, Balanced Source Impedance		120dB	
$R_S \leq 1k\Omega$, HI IN Lead Only		104dB min	
Max Leakage Current, Input to Output @			
115V rms, 60Hz ac		2μA rms max	
INPUT IMPEDANCE			
Differential		$33pF \| 10^8\Omega$	
Overload		$100k\Omega$	
Common Mode		$20pF \| 5 \times 10^{10}\Omega$	
INPUT DIFFERENCE CURRENT			
Initial @ +25°C		10nA (75nA max)	
vs. Temperature (0 to 70°C)		0.15nA/°C	
INPUT NOISE (GAIN = 100V/V)			
Voltage			
0.05Hz to 100Hz		8μV p-p	
10Hz to 1kHz		3μV rms	
Current			
0.05Hz to 100Hz		3pA rms	
FREQUENCY RESPONSE			
Small Signal -3dB			
G = 1V/V		20kHz	
G = 100V/V		5kHz	
Full Power, 10V p-p Output			
G = 1V/V		5kHz	
G = 100V/V		3.5kHz	
Full Power, 20V p-p Output			
G = 1V/V		2.3kHz	
G = 100V/V		2.3kHz	
Slew Rate		0.14V/μs	
Settling Time[4] ±0.05%, ±10V Step		400μs	
OFFSET VOLTAGE, REFERRED TO INPUT			
Initial, @ +25°C		$\pm\left(5 + \frac{20}{G}\right)$ mV max	
vs. Temperature (0 to +70°C)	$\pm\left(20 + \frac{200}{G}\right)\mu V/°C$ max	$\pm\left(15 + \frac{100}{G}\right)\mu V/°C$ max	$\pm\left(10 + \frac{50}{G}\right)\mu V/°C$ max
vs. Supply Voltage (+15V to +20V change)		$\pm\left(2 + \frac{10}{G}\right)\mu V/V$	
RATED OUTPUT			
Voltage, 2kΩ Load		±10V min	
Output Impedance		<1Ω(dc to 100Hz)	
Output Ripple, 0.1MHz Bandwidth			
No Signal IN		5mV p-p	
$+10V_{IN}$		50mV p-p	
ISOLATED POWER SUPPLY			
Voltage		±15V dc	
Accuracy		±10%	
Current		±5mA, min	
Regulation No Load to Full Load		±5%	
Ripple, 0.1MHz Bandwidth, No Load		25mV p-p	
Full Load		75mV p-p	
POWER SUPPLY, SINGLE POLARITY[5]			
Voltage, Rated Performance		+14.4V to +25V	
Voltage, Operating		+8.5V to +25V	
Current, Quiescent (@ V_S = +15V)		+25mA	
TEMPERATURE RANGE			
Rated Performance		0 to +70°C	
Operating		-15°C to +75°C	
Storage		-55°C to +85°C	
CASE DIMENSIONS		1.5" X 2.0" X 0.75"	

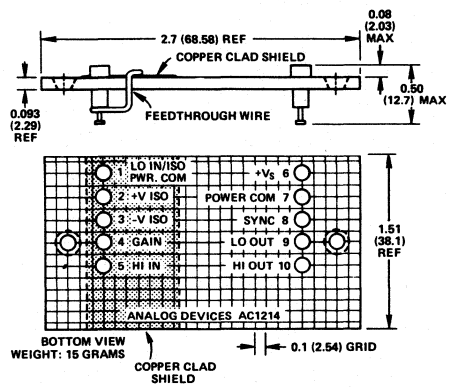
NOTES
[1] Gain temperature drift is specified as a percentage of output signal level.
[2] Gain nonlinearity is specified as a percentage of 10V pk-pk output span.
[3] When isolated power output is used, nonlinearity increases by ±0.002%/mA of current drawn.
[4] G = 1V/V; with 2-pole, 5kHz output filter (see Figure 13).
[5] Recommended power supply, ADI model 904, ±15V @ 50mA output.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



SHIELDED MATING SOCKET AC1214



INTERCONNECTIONS AND SHIELDING TECHNIQUE

To preserve the high CMR performance of model 289, care must be taken to keep the capacitance balanced about the input terminals. A shield should be provided on the printed circuit board under model 289 as illustrated in the outline drawing above (screened area). The LO IN/ISO PWR COM (pin 1) must be connected to this shield. This shield is provided with the mounting socket, model AC1214 (solder feedthrough wire to the socket pin 1 and copper foil surface). A recommended shielding technique using model AC1214 is illustrated in Figure 1.

Best CMR performance will be achieved by using twisted, shielded cable for the input signal to reduce inductive and capacitive pickup. To further reduce effective cable capacitance, the cable shield should be connected to the common mode signal source as close to signal low as possible (see Figure 1).

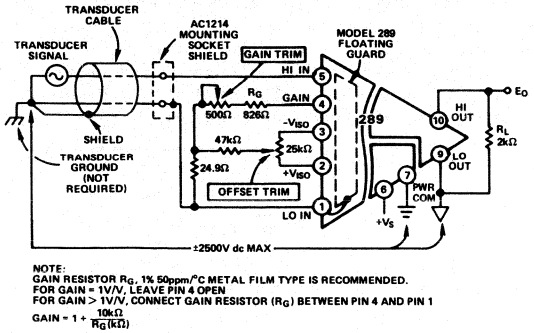


Figure 1. Basic Isolator Interconnection

THEORY OF OPERATION

The remarkable performance of the model 289 is derived from the carrier isolation technique used to transfer both signal and power between the amplifier's input stage and the rest of the circuitry. A block diagram is shown in Figure 2.

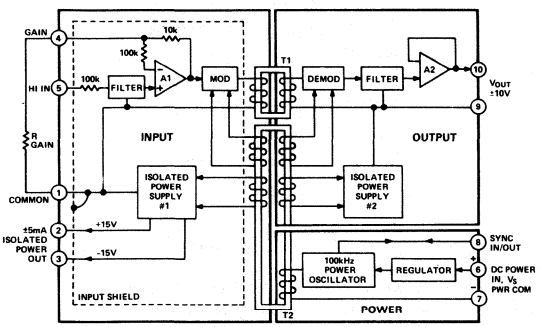


Figure 2. Model 289 Block Diagram

The input signal is filtered and appears at the input of the non-inverting amplifier, A1. This signal is amplified by A1, with its gain determined by the value of resistance connected externally between the gain terminal and the input common terminal. The output of A1 is modulated, carried across the isolation barrier by signal transformer T1, and demodulated. The demodulated voltage is filtered, amplified and buffered by amplifier A2, and applied to the output terminal. The voltage applied to the V_S terminal is set by the regulator to +12V which powers the 100kHz symmetrical square wave power oscillator. The oscillator drives the primary winding of transformer T2. The secondary windings of T2 energize both input and output power supplies, and drives both the modulator and demodulator.

INTERELECTRODE CAPACITANCE AND TERMINAL RATINGS

Capacitance: Interelectrode terminal capacitance, arising from stray coupling capacitance effects between the input terminals and the signal output terminals, are each shunted by leakage resistance values exceeding 50GΩ. Figure 3 illustrates model 289's capacitance, between terminals.

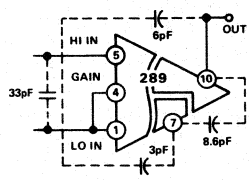


Figure 3. Model 289 Terminal Capacitance

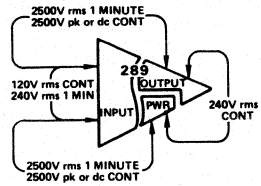


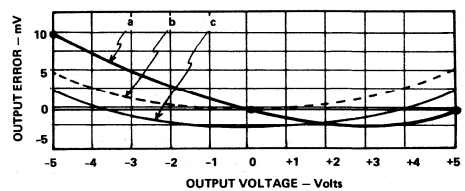
Figure 4. Model 289 Terminal Ratings

Terminal Ratings: CMV performance is given in both peak pulse and continuous ac, or dc peak ratings. Continuous peak ratings apply from dc up to the normal full power response frequencies. Figure 4 illustrates model 289 ratings between terminals.

GAIN AND OFFSET TRIM PROCEDURE

The following procedure illustrates a calibration technique which can be used to minimize output error. In this example, the output span is +5V to -5V and Gain = 10V/V.

1. Apply E_{IN} = 0 volts and adjust R_O for E_O = 0 volts.
2. Apply E_{IN} = +0.500V dc and adjust R_G for E_O = +5.000V dc.
3. Apply E_{IN} = -0.500V dc and measure the output error (see curve a).
4. Adjust R_G until the output error is one-half that measured in step 3 (see curve b).
5. Apply +0.500V dc and adjust R_O until the output error is one-half that measured in step 4 (see curve c).



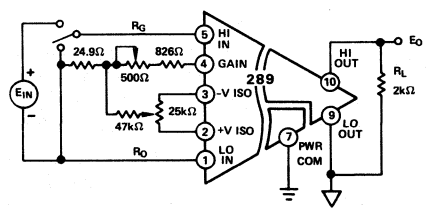


Figure 5a. Recommended Offset and Gain Adjustment for Gains > 1

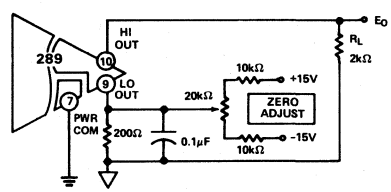


Figure 5b. Recommended Offset Adjustment for G = 1V/V

PERFORMANCE CHARACTERISTICS

Figure 6 shows the phase shift vs. frequency. The low phase shift and wide bandwidth of the model 289 make it suitable for use in SCR Motor Controller and other high frequency applications.

Figure 7 illustrates the effect of source impedance imbalance on CMR performance at 60Hz for gains of 1V/V, 10V/V, and 100V/V. CMR is typically 120dB at 60Hz and a balanced source impedance. CMR is >60dB for source impedance imbalances up to 100kΩ.

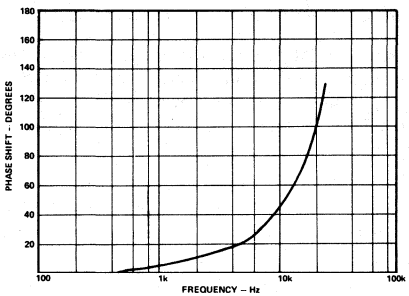


Figure 6. Typical 289 Phase vs. Frequency

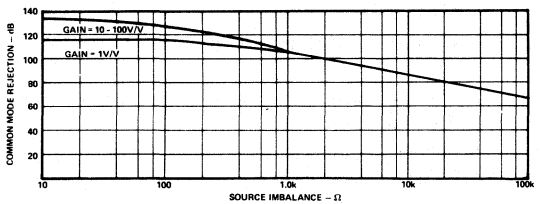


Figure 7. Typical 289 Common Mode Rejection vs. Source Impedance

Input Voltage Noise: Voltage noise, referred to input, is dependent on gain and bandwidth. Figure 8 shows rms voltage noise in a bandwidth from 0.05Hz to the frequency shown on the horizontal axis. The noise in a bandwidth from 0.05Hz to 100Hz is 8μV pk-pk at a gain of 100V/V. The peak-to-peak value is derived by multiplying the rms value at F = 100Hz (1.2μV rms) by 6.6.

For best noise performance in particular applications, a low pass filter at the output should be used to selectively roll-off noise and undesired signal frequencies beyond the bandwidth of interest. Increasing gain will also reduce the noise, referred to input.

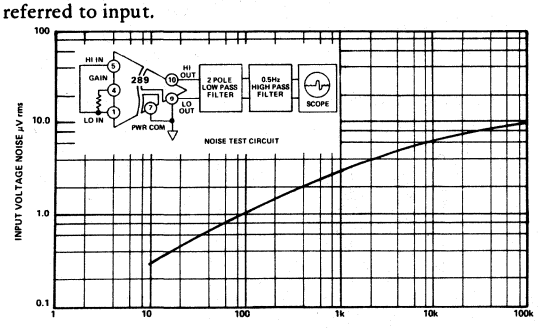


Figure 8. Typical Input Voltage Noise vs. Bandwidth

Gain Nonlinearity: Linearity error is defined as the deviation of the output voltage from the best straight line and is specified as a % peak-to-peak output voltage span; e.g., nonlinearity of model 289J operating at an output span of 10V pk-pk (±5V) is ±0.05% or ±5mV. Figure 9 illustrates gain nonlinearity for any output span to 20V pk-pk (±10V). Figure 10 shows the effect of gain vs. gain nonlinearity.

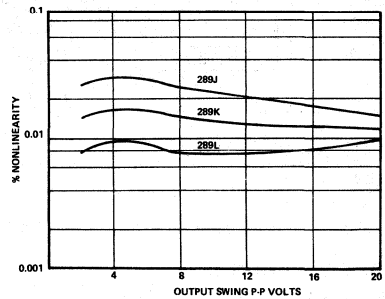


Figure 9. Typical Gain Nonlinearity vs. Output Swing

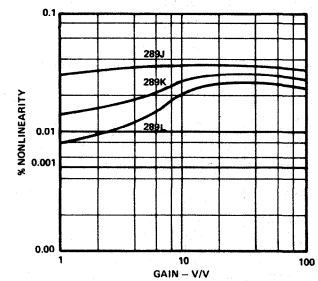


Figure 10. Typical Gain Nonlinearity vs. Gain

Common Mode Rejection: Input-to-output CMR is dependent on source impedance imbalance, signal frequency and amplifier gain. CMR is rated at 115V ac, 60Hz and 1kΩ balanced source at a gain of 100V/V. Figure 11 illustrates CMR performance as a function of signal frequency. CMR approaches 156dB at dc with source imbalance as high as 1kΩ. As gain is decreased, CMR is reduced. At a gain of 1V/V, CMR is typically 6dB lower than at a gain of 100V/V.

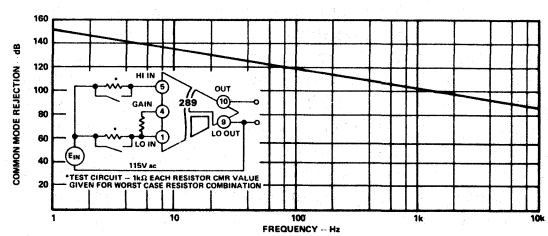


Figure 11. Typical Common Mode Rejection vs. Frequency at a Gain of 1V/V, CMR is typically 6dB Lower than at a Gain of 100V/V

MULTICHANNEL APPLICATIONS

Isolation amplifiers containing internal oscillators may exhibit a slowly varying offset voltage at the output when used in multichannel applications. This offset voltage is the result of adjacent internal oscillators beating together. For example, if two adjacent isolation amplifiers have oscillator frequencies of 100.0kHz and 100.1kHz respectively, a portion of the difference frequency may appear as a slowly varying output offset voltage error. Model 289 eliminates this problem by offering a synchronization terminal (pin 8). When this terminal is interconnected with other model 289 synchronization terminals, the units are synchronized. Alternately, one or more units may be synchronized to an external 100kHz ±2% square-wave generator by the connection of synchronization termial(s) to that generator. The generator output should be 2.5V—5.0V p-p with 1kΩ source impedance to each unit. Use an external oscillator when you need to sync to an external 100kHz source, such as a sub-multiple of a microprocessor clock. A differential line driver, such as SN75158, can be used to drive large clusters of model 289. When using the synchronization pin, keep leads as short as possible and do not use shielded wire. These precautions are necessary to avoid capacitance from the synchronization terminal to other points. It should be noted that units synchronized must share the same power common to ensure a return path.

APPLICATIONS IN INDUSTRIAL MEASUREMENT AND CONTROL SYSTEMS

Isolated DAS: In data acquisition systems where multiple transducers are powered by a single supply and the magnitude of that supply is low enough for a multiplexer to handle the voltages on all the transducers, it is economical to multiplex ahead of an isolator. The fast settling time of the model 289 makes this configuration practical where slower isolators would not be usable.

Figure 12 shows an application where the difference in voltage between any two terminals of any of the transducers does not exceed 30 volts. Though the input of the model 289 is protected against line voltage, its power terminals are not; neither is the multiplexer so protected. This circuit will not, therefore, withstand the differential application of line voltage.

Multiplexer addressing is binary, an enable providing selection of the circuit shown as a signal source. Optical isolation is provided for digital signals. When several of these circuits are used for several groups of transducers, the model 289's should be synchronized.

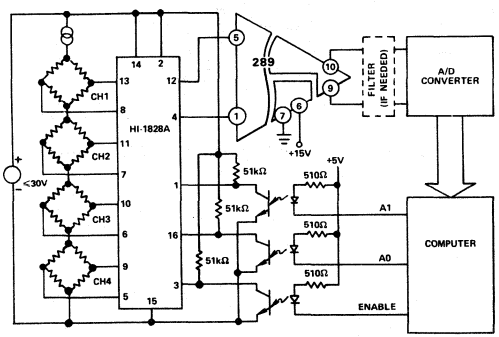


Figure 12. DAS with MUX Ahead of Isolator

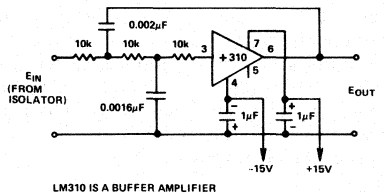


Figure 13. 2-Pole, 5kHz Active Filter

Noise Reduction in Data Acquisition Systems: Transformer coupled isolators must have a carrier to pass dc signals through their signal transformers. Inevitably some carrier frequency ripple passes through to the isolator output. As the bandwidth of an isolator becomes a larger fraction of its carrier frequency, this ripple becomes more difficult to control. Despite this difficulty, the model 289 produces very low ripple; therefore, additional filtration will usually be unnecessary. However, in some applications, particularly where a fast analog-to-digital converter is used following the isolator, it may be desirable to add filtration; otherwise, ripple may cause inaccurate conversions. The 2-pole low-pass shown in Figure 13 limits isolator bandwidth to 5kHz, which is the full power bandwidth of the model 289. Carrier ripple is much reduced. Another beneficial effect of an output filter is smoothing of discontinuous high frequency waveforms.

Motor Control and AC Load Control: Phase shift and bandwidth are important considerations for motor control and ac load control applications. The model 289 possesses sufficient bandwidth and acceptable phase shift for such tasks.

Figure 14 shows two model 289's sensing the armature voltage and current of a motor. Faithful replicas of the waveforms of these variables are applied to the motor control. A1 operates at unity gain from divided R1—R3 to deliver an output that is 1/100 of the armature voltage of the motor. A2 operates at a gain of 100V/V to deliver a voltage 100 times that developed across the current sensing shunt.

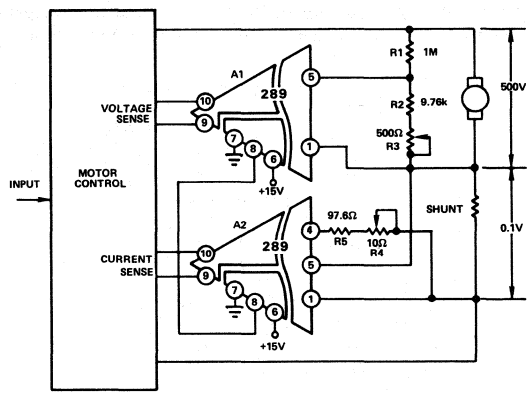


Figure 14. Isolating a Motor Controller

Figure 15 shows three model 289's sensing the voltages on the three phases of an ac load. The Y network shown divides the voltages of the three phases and creates a neutral for the input commons of the isolators. The output of each isolator is a faithful replica of the phase of the waveform it senses. The isolator outputs provide the feedback necessary for the trigger control to correctly fire the triacs. In other applications, the outputs of the isolators might have been fed to rms-to-dc converters.

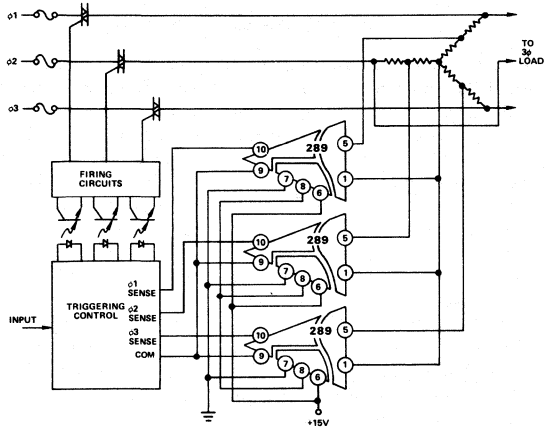


Figure 15. Isolating a 3-Phase Load Controller

Isolated DACs: Figure 16 shows a 12-bit DAC with ±5V isolated output. A buffered -5V reference voltage is provided to the DAC by A1a, A1b and associated circuitry. The digital input causes a proportion of DAC current to flow into OUT1 of the DAC. The remaining DAC current flows into OUT2. Current flowing into OUT1 causes positive voltage at the output of A1c. Current flowing into OUT2 causes a positive voltage at the output of A1d, which in turn causes a negative voltage at the output of A1c. Voltage appearing at the output of A1c is reproduced at the output of the model 289. R5 and R8 must be adjusted to produce less than 0.5mV at OUT1 and OUT2 of the DAC respectively. R15 may be used to adjust gain and R11 to adjust offset with the binary code 1000 0000 0000 to zero.

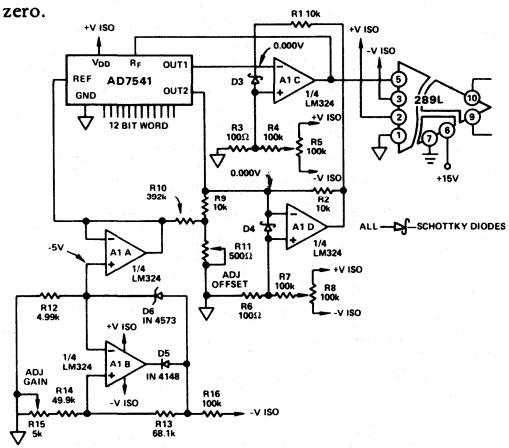


Figure 16. 12-Bit Isolated Voltage DAC

Figure 17 shows the model 289 providing an isolated 4-to-20mA output from a 12-bit DAC. A1a provides a -4V reference to the DAC. The digital input causes a portion of DAC current to flow into OUT1, causing a positive voltage at the output of A1d. A1b produces a voltage across R4 proportional to DAC current. A1c and associated circuitry sink a current which is one-fourth of the full scale current of the DAC, causing a positive voltage of 1 volt at the output of A1d. With the code 1111 1111 1111, +5 volts appears at the output of A1d. Operation is unipolar with a positive offset. The output voltage of A1d is reproduced at the output of the isolator, where the circuitry shown converts it into a 4-to-20mA current which may be applied to the load R_L.

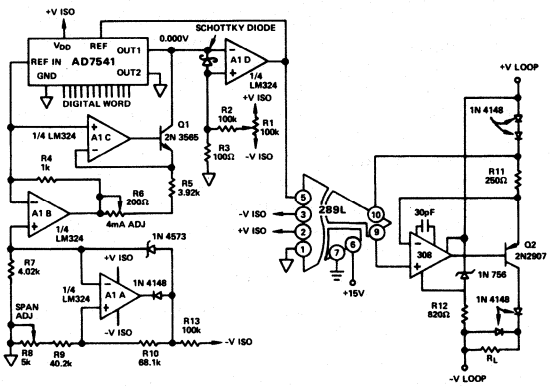


Figure 17. 12-Bit Isolated Process Current DAC

Temperature Measurement: Figure 18 shows the model 289 providing a ground-referred output in an application measuring the temperature of an object floating at a high common mode voltage. The AD590 temperature sensor sinks a current of -1μA/K. This current flows into the gain terminal of the model 289, developing +10mV/K across the internal feedback resistor. This voltage also appears at the output of the model 289.

The circuitry shown connected by a dotted line may be useful if an output of 10mV/°C is desired. A current of +273μA is sourced through the 8.66k resistor and the potentiometer cancelling the AD590 current at 0°C (273K), resulting in 0mV at the output at 0°C.

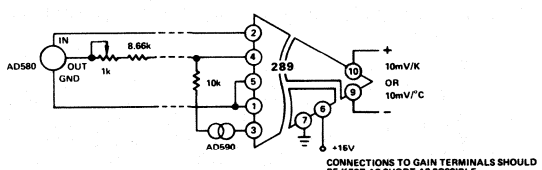


Figure 18. Isolated Temperature Measurement

ANALOG DEVICES

Low Cost, Single and Multichannel Isolation Amplifiers

290A/292A

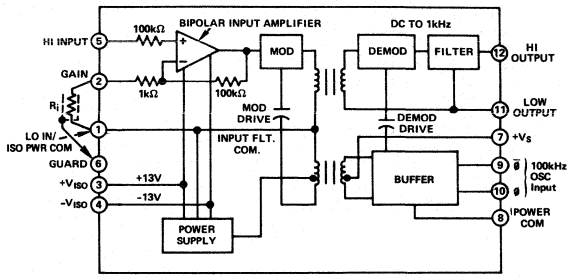
FEATURES

Low Cost
Multichannel Capability Using External Oscillator (292A)
Isolated Power Supply: ±13V dc @ ±5mA (290A) or ±15mA (292A)
Low Nonlinearity: 0.1% @ 10V pk-pk Output
High Gain Stability: 0.001%/1000 Hours; 0.01%/°C
Small Size: 1.5″ X 1.5″ X 0.62″
Low Input Offset Voltage Drift: 10μV/°C (Gain = 100V/V)
Wide Input/Output Dynamic Range: 20V pk-pk
High CMV Isolation: 1500V dc, Continuous
Wide Gain Range: 1 to 100V/V

APPLICATIONS

Ground Loop Elimination in Industrial and Process Control
High Voltage Protection in Data Acquisition Systems
Fetal Heart Biomedical and Monitoring Instrumentation
Off-Ground Signal Measurements

FUNCTIONAL BLOCK DIAGRAM



$$\text{GAIN} = 1 + \frac{100k\Omega}{1k\Omega + R_i\,(k\Omega)} \quad (1V/V \text{ TO } 100V/V)$$

GENERAL DESCRIPTION

Models 290A and 292A are low cost, compact, isolation amplifiers that are optimized for single and multichannel industrial applications, respectively. The model 290A has a self-contained oscillator and is intended for single channel applications. A single external synchronizing oscillator can drive up to 16 model 292As or, a virtually limitless number of model 292As can be configured using multiple oscillators. The user can supply the external oscillator circuit or specify model 281 oscillator module, which includes a voltage regulator for operation over a wide single supply voltage range of +8V to +28V.

Models 290A and 292A design features include: adjustable gain, from 1 to 100V/V, dual isolated power, ±13V dc, ±1500V dc off ground isolation, 100dB minimum CMR at 60Hz, 1kΩ source imbalance, in a compact 1.5″ X 1.5″ X 0.6″ module. Models 290A and 292A achieve low input noise of 1μV pk-pk (10Hz bandwidth, G = 100V/V), nonlinearity of ±0.1% @ 10V pk-pk output, and an input/output dynamic range of 20V pk-pk.

Using modulation techniques with reliable transformer isolation, models 290A and 292A will interrupt ground loops, leakage paths, and voltage transients, while providing dc to 2kHz (-3dB) response.

WHERE TO USE MODELS 290A AND 292A

Industrial Applications: In data acquisition systems, computer interface systems, process signal isolators and high CMV instrumentation, models 290A and 292A offer complete galvanic isolation and protection against damage from transients and fault voltages. High level transducer interface capability is afforded with 20V pk-pk input signal range at a gain of 1V/V operation. In portable single or multichannel designs, single power supply operation (+8V to +16V) enables battery operation.

DESIGN FEATURES AND USER BENEFITS

Isolated Power: Dual ±13V dc output, completely isolated from the input power terminals (±1500V dc isolation), provides the capability to excite floating signal conditioners, front end buffer amplifiers and remote transducers such as thermistors or bridges.

Adjustable Gain: Models 290A and 292A adjustable gain offers compatibility with a wide class of input signals. A single external resistor enables gain adjustment from 1V/V to 100V/V providing flexibility in both high level transducer interfacing as well as low level sensor measurement applications.

Floating, Guarded Front-End: The input stage of models 290A and 292A can directly accept floating differential signals or it may be configured as a high performance instrumentation front-end to accept signals having CMV with respect to input power common.

High Reliability: Models 290A and 292A are conservatively designed, compact modules, capable of reliable operation in harsh environments. They have a calculated MTBF of over 400,000 hours and are designed to meet IEEE Standard for Transient Voltage Protection (472-1974: Surge Withstand Capability).

5

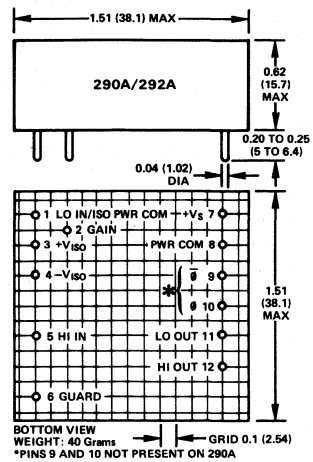
290A/292A—SPECIFICATIONS (typical @ +25°C; G = 100V/V and V_S = +15V dc, unless otherwise noted)

MODEL	290A	292A
GAIN (NONINVERTING)		
Range (50kΩ Load)	1 to 100V/V	
Formula	$\text{Gain} = \left[1 + \frac{100k\Omega}{1k\Omega + R_i\,(k\Omega)}\right]$	
Deviation from Formula	±3%	
vs. Time	±0.001%/1000 Hours	
vs. Temperature (-25°C to +85°C)[1]	±0.0075%/°C	
Nonlinearity, G = 1V/V to 100V/V[2]	±0.1% (±0.25%)[3]	
INPUT VOLTAGE RATINGS		
Linear Differential Range, G = 1V/V	±5V min (±10V min)[3]	
Max Safe Differential Input		
Continuous, 1 min	110V rms	
Max CMV, Inputs to Outputs		
ac, 60Hz, 1 Minute Duration	1500V rms max	
Continuous, ac	±1000V pk max	
Continuous, dc	±1500V pk max	
CMR, Inputs to Outputs, 60Hz, $R_S \leq 1k\Omega$		
Balanced Source Impedance	106dB	
1kΩ Hi In Lead Only	100dB min	
Max Leakage Current, Inputs to Power Common		
@ 115V ac, 60Hz	10μA rms max	
INPUT IMPEDANCE		
Differential	$10^8\,\Omega \| 70pF$	
Overload	100kΩ	
Common Mode	$5 \times 10^{10}\,\Omega \| 100pF$	
INPUT DIFFERENCE CURRENT		
Initial, @ +25°C	+3nA	
vs. Temperature (-25°C to +85°C)	±0.1nA/°C	
INPUT NOISE		
Voltage, G = 100V/V		
0.01Hz to 10Hz	1μV p-p	
10Hz to 1kHz	1.5μV rms	
Current		
0.05Hz to 100Hz	5pA p-p	
FREQUENCY RESPONSE		
Small Signal, -3dB, G = 1V/V	2.5kHz	
Slew Rate	50mV/μs	
Full Power, 10V p-p Output		
Gain - 1V/V thru 100V/V	2.0kHz(1.0kHz)[3]	3.0kHz(1.0kHz)[3]
OFFSET VOLTAGE REFERRED TO INPUT		
Initial, @ +25°C, Adjustable to Zero	±(5 + 50/G)mV	
vs. Temperature (-25°C to +85°C)	±(10 + 150/G)μV/°C	±(8 + 250/G)μV/°C
vs. Supply Voltage	±1mV/%	
RATED OUTPUT		
Voltage, 50k Load	±5V min (±10V min)[3]	
Output Impedance	1kΩ	
Output Ripple, 1MHz Bandwidth	10mV pk-pk	
OSCILLATOR DRIVE INPUT		
Input Voltage	N/A	8 to 16V pk-pk
Input Frequency	N/A	100kHz ±5%, max
ISOLATED POWER OUTPUTS		
Voltage Full Load	±13V dc	
Accuracy	±5%	
Current[4]	±5mA min	±15mA min
Regulation, No Load to Full Load	+0, -15%	
Ripple, 100kHz Bandwidth	200mV p-p	250mV p-p
POWER SUPPLY, SINGLE POLARITY		
Voltage, Rated Performance	+15V dc	
Voltage, Operating	+8V dc to +15.5V dc	
Current, Quiescent	+20mA	
TEMPERATURE RANGE		
Rated Performance	-25°C to +85°C	
Storage	-55°C to +85°C	
CASE DIMENSIONS	1.5" X 1.5" X 0.62"	

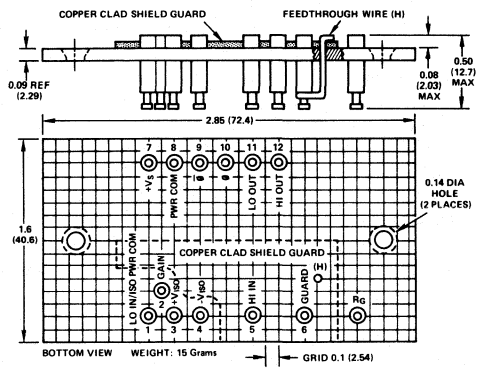
NOTES
[1] Gain temperature drift is specified as a percentage of output signal level.
[2] Gain nonlinearity is specified as a percentage of 10V pk-pk output span.
[3] These specs apply for a 20V pk-pk output span.
[4] Do not load V_{ISO} when operating at output spans greater than 10V pk-pk.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



SHIELDED MOUNTING SOCKET AC1054



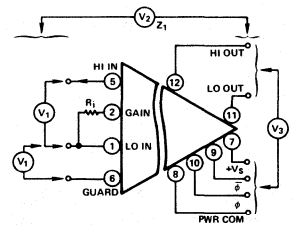


Figure 1. Model 290A and 292A Terminal Ratings

Symbol	Rating	Remarks
V_1	±110V rms (cont.)	Withstand Voltage, Steady State
V_2	±1000V pk (cont.)	Isolation, Steady State, ac
V_2	±1500V pk (cont.)	Isolation, Steady State, dc
V_2	±1500V rms (1 min)	Isolation, ac, 60Hz
V_3	±50V pk (cont.)	Isolation, dc
Z_1	$50G\Omega \| 20pF$	Isolation Impedance

Table I. Isolation Ratings Between Terminals

THEORY OF OPERATION

The remarkable performance of models 290A and 292A are derived from the carrier isolation technique which is used to transfer both signal and power between the amplifier's guarded input stage and the rest of the circuitry. The block diagram for both models is shown in Figure 2 below.

The bipolar input preamplifier operates single-ended (non-inverting). Only a difference bias current flows with zero net bias current. A third wire return path for input bias current is not required. Gain can be set from 1V/V to 100V/V by changing the gain resistor, R_i. *To preserve high CMR, the gain resistor must be guarded.* Best performance is achieved by shorting terminal 2 to terminal 1 and operating the isolator at a gain of 100V/V.

For powering floating input circuitry such as buffer amplifiers, instrumentation amplifiers, calibration signals and transducers, dual isolated power is provided. High CMV isolation is achieved by the low-leakage transformer coupling between the input preamplifier, modulator section and the output circuitry. Only the 10pF leakage capacitance between the floating input section and the rest of the circuitry keeps the CMR from being infinite.

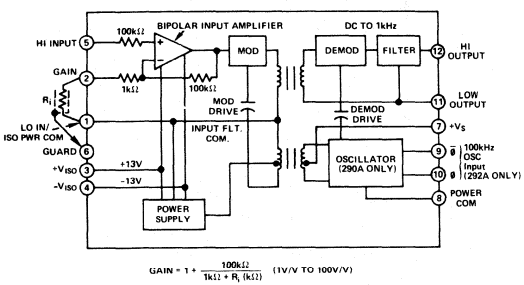


Figure 2. Block Diagram — Models 290A and 292A

GUIDELINES ON EFFECTIVE SHEILDING & GROUNDING PRACTICES

- Use twisted shielded cable to reduce inductive and capacitive pickup.
- Drive the transducer cable shield, S, with the common mode signal source, E_G, to reduce the effective cable capacitance as shown in Figure 3. This is accomplished by connecting the shield point S, as close as possible to the transducer signal low point B. This may not always be possible. In some cases the shield may be separated from signal low by a portion of the medium being measured (e.g. pressure transducer). This will cause a common mode signal, E_M, to be generated by the medium between the shield and the signal low. The 86dB CMR capability of both models between the input terminals (HI IN and LO IN) and GUARD, will work to suppress the common mode signal, E_M.
- Dress unshielded leads short at the connection terminals and reduce the area formed by these leads to minimize inductive pickup.

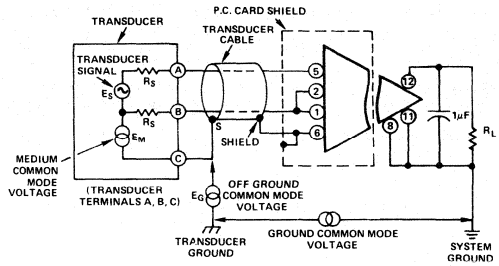
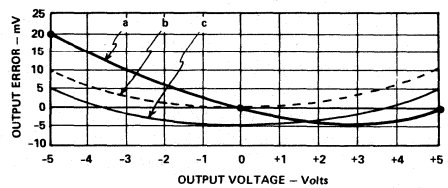


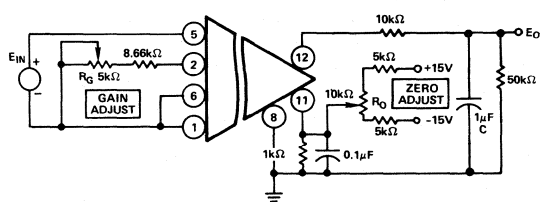
Figure 3. Transducer — Amplifier Interface

GAIN AND OFFSET TRIM PROCEDURE

In applying the isolation amplifier, highest accuracy is achieved by adjustment of gain and offset voltage to minimize the peak error encountered over the selected output voltage span. The following procedure illustrates a calibration technique which can be used to minimize output error. In this example, the output span is +5V to -5V and operation at Gain = 10V/V is desired.

1. Apply E_{IN} = 0 volts and adjust R_O for E_O = 0 volts.
2. Apply E_{IN} = +0.5V dc and adjust R_G for E_O = +5.0V dc.
3. Apply E_{IN} = -0.5V dc and measure the output error (see curve a).
4. Adjust R_G until the output error is one half that measured in step 3 (see curve b).
5. Apply +0.5V dc and adjust R_O until the output error is one half that measured in step 4 (see curve c).





GAIN RESISTOR, R_i, 1%, 50ppm/°C METAL FILM TYPE IS RECOMMENDED.
FOR GAIN = 1V/V, LEAVE TERMINAL 2 OPEN.
FOR GAIN = 100V/V, SHORT TERMINAL 2 TO TERMINAL 1

$$GAIN = 1 + \frac{100k\Omega}{1k\Omega + R_i(k\Omega)}$$

OUTPUT FILTER, 10kΩ RESISTOR AND CAPACITOR, C.
SELECT C TO ROLL-OFF NOISE AND OUTPUT RIPPLE:

$$f = (-3dB) = \frac{1}{2\pi C\,(11k\Omega)}$$

Figure 4. Gain and Offset Adjustment

SELECTING BANDWIDTH

In low frequency signal measurements, such as thermocouple temperature measurements, strain gage measurements and geophysical instrumentation, an external filter is used to select bandwidth and minimize output noise.

When used with a buffer amplifier as shown in Figure 5a below, a series resistor (R_S) is used to lower the effective value of the filter capacitor required to achieve very low frequency (under 200Hz) noise filtering.

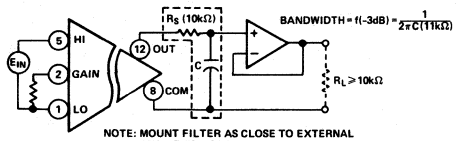


Figure 5a. Selecting Bandwidth with External Capacitor and Buffer

An active filter, as illustrated in Figure 5b will significantly improve 60Hz noise reduction at the output by providing a sharp roll-off characteristic. The 5Hz 3-pole active filter design illustrated in Figure 5b, will increase the 60Hz noise reduction by 50dB. Overall CMR performance of models 290 and 292 and the 5Hz active filter approaches 150dB @ 60Hz and 1kΩ imbalance.

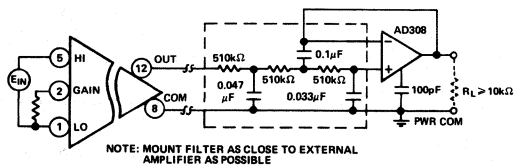


Figure 5b. Selecting Bandwidth with a 3-Pole 5Hz Active Filter

PERFORMANCE CHARACTERISTICS

Common Mode Rejection: Input-to-Output CMR is dependent on source impedance imbalance, signal frequency and amplifier gain. CMR is rated at 115V ac, 60Hz and 1kΩ imbalance at a gain of 100V/V. Figure 6 illustrates CMR performance as a function of signal frequency. CMR approaches 130dB at dc with source imbalances as high as 1kΩ. As gain is decreased, CMR is reduced. At a gain of 1V/V, CMR is typically 12dB lower than at a gain of 100V/V.

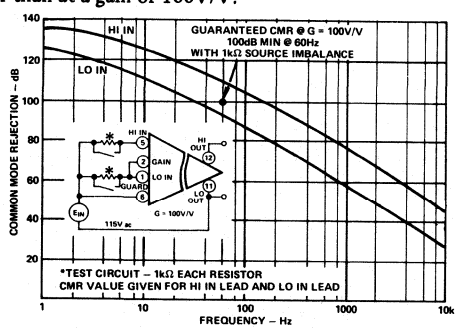


Figure 6. Typical Common Mode Rejection vs. Frequency

Figure 7 illustrates the effect of source imbalance on CMR performance at 60Hz and Gain = 100V/V. CMR is typically 110dB at 60Hz and a balanced source. CMR is maintained greater than 70dB for source imbalances up to 100kΩ.

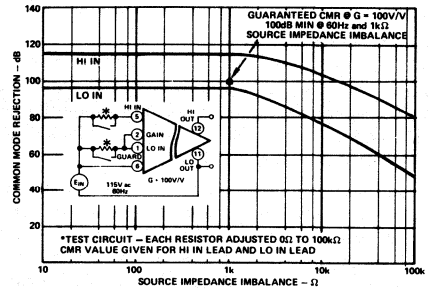


Figure 7. Typical Common Mode Rejection vs. Source Impedance Imbalance

Gain Nonlinearity: Linearity error is defined as the deviation of the output voltage from the best straight line and is specified as a % of peak-to-peak output voltage span; e.g., nonlinearity of models 290A and 292A operating at an output span of 10V pk-pk (±5V) is ±0.1% or ±10mV. Figure 8 illustrates gain nonlinearity for any output span to 20V pk-pk (±10V).

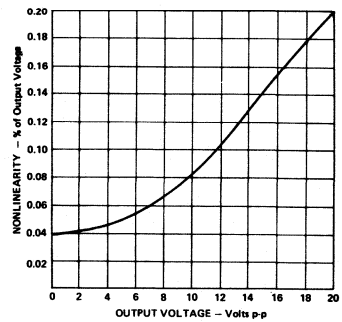


Figure 8. Typical Gain Nonlinearity vs. Output Voltage

Input Voltage Noise: Voltage noise, referred to input, is dependent on gain and bandwidth as illustrated in Figure 9. RMS voltage noise is shown in a bandwidth from 0.01Hz to the frequency shown on the horizontal axis. The noise in a bandwidth from 0.01Hz to 10Hz is 1μV pk-pk at a gain of 100V/V. This value is derived by multiplying the rms value at f = 10Hz shown in Figure 9 by 6.6.

For best noise performance in particular applications, a low pass filter at the output should be used to selectively roll-off noise and undesired signal frequencies beyond the bandwidth of interest. Increasing gain will also reduce the input noise.

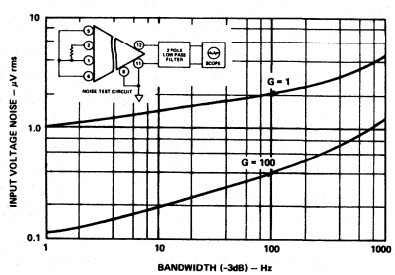


Figure 9. Typical Input Voltage Noise vs. Bandwidth

Input Offset Voltage Drift: Total input drift is composed of two sources, input and output stage drifts and is gain dependent. The curve of Figure 10 illustrates total input drift over the gain range of 1 to 100V/V.

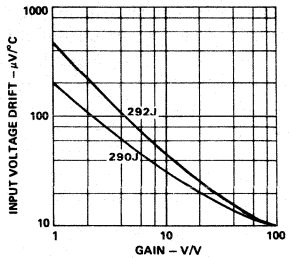


Figure 10. Typical Input Offset Voltage Drift vs. Gain

REFERENCE EXCITATION OSCILLATOR, MODEL 281

When applying model 292A, the user has the option of building a low cost 100kHz excitation oscillator, as shown in Figure 11, or purchasing a module from Analog Devices—model 281.

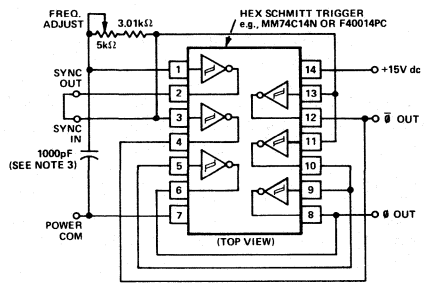


Figure 11. 100kHz Oscillator Interconnection Diagram

The block diagram of model 281 is shown in Figure 12. An internal +12V dc regulator is provided to permit the user the option of operating over two, pin selectable, power input ranges; terminal 6 offers a range of +14V dc to +28V dc; terminal 7 offers an input range of +8V dc to +14V dc.

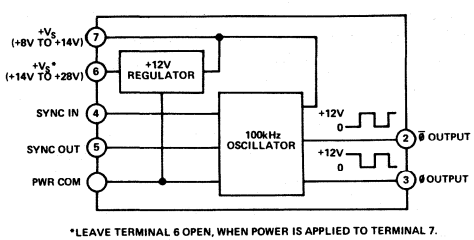


Figure 12. Model 281 Block Diagram

Model 281 oscillator is capable of driving up to 16 model 292As. As shown in Figure 13, an additional model 281 may be driven in a slave-mode to expand the total system channels from 16 to 32. By adding additional model 281's in this manner, systems of over 1000 channels may be easily configured.

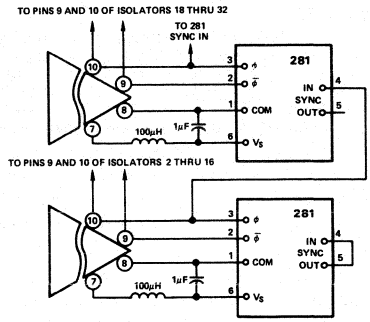


Figure 13. External Oscillator Interconnection

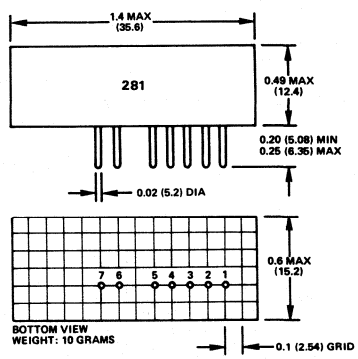
SPECIFICATIONS
(typical @ +25°C and V_S = +15V dc unless otherwise noted)

MODEL	281
OUTPUT	
Frequency	100kHz ±5%
Waveform	Squarewave
Voltage (ϕ and $\bar{\phi}$ terminals)	0 to +12V pk
Fan-Out[1,2]	16 max
POWER SUPPLY RANGE[3]	
High Input, Pin 6	+(14 to 28)V dc
Quiescent Current, N.L.	+5mA
F.L.	+16mA
Low Input, Pin 7	+(8 to 14)V dc
Quiescent Current, N.L.	+12mA
F.L.	+33mA
TEMPERATURE	
Rated Performance	0 to +70°C
Storage	-55°C to +85°C

[1] Model 292A oscillator drive input represents unity oscillator load.
[2] For applications requiring more than 16 292As, additional 281s may be used in a master/slave mode. Refer to Figure 13.
[3] Full load consists of 16 model 292As and 281 oscillator slave.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



PIN TERMINAL IDENTIFICATION

1	POWER COMMON	5	SYNC OUTPUT
2	$\bar{\phi}$ OUTPUT	6	$+V_S$: HIGH RANGE +(14 to 28)V dc
3	ϕ OUTPUT	7	$+V_S$: LOW RANGE +(8 to 14)V dc
4	SYNC INPUT		

MATING SOCKET:
CINCH #16 DIP OR EQUIVALENT

APPLICATIONS IN INDUSTRIAL MEASUREMENT AND CONTROL SYSTEMS

Remote Sensor Interface: In chemical, nuclear and metal processing industries, models 290A and 292A can be applied to measure and control off-ground millivolt signals in the presence ±1500V dc CMV signals. In interface applications such as pH control systems or on-line process measurement systems such as pollution monitoring, models 290A and 292A offer complete galvanic isolation to eliminate troublesome ground loop problems. Isolated power outputs and adjustable gain add to the application flexibility of these models.

Figure 14 illustrates how model 290A or 292A can be combined with a low drift, 1μV/°C front-end amplifier, model AD517L, to interface low level transducer signals. Both products provide isolated ±13V dc power and front-end guard in addition to eliminating ground loops and preserving high CMR (100dB @ 60Hz).

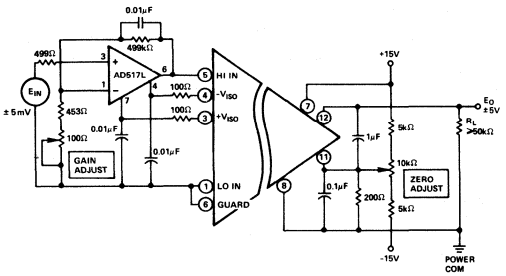


Figure 14. Input Signal Conditioning Using Isolated Power for Transducer Buffer Amplifier

Instrumentation Amplifier: Models 290A and 292A provide a floating guarded input stage capable of directly accepting isolated differential signals. The noninverting, single-ended input stage offers simple two wire interconnection with floating input signals.

In applications where the isolated power is applied to transducers such as bridges which generate differential input signals with common mode voltages measured with respect to the isolated power common, models 290A and 292A can be connected as shown in Figure 15. To achieve high CMR with respect to the ISO PWR COM, the following trim procedure is recommended.

CMR Trim Procedure

1) Connect a 1V pk-pk oscillator between the +IN/-IN and IN COM terminals as shown in Figure 15.
2) Set the input frequency at 0.5Hz and adjust R1 for minimum E_O.
3) Set the input frequency at 60Hz and adjust R2 for minimum E_O.
4) Repeat steps 2 and 3 for best CMR performance.

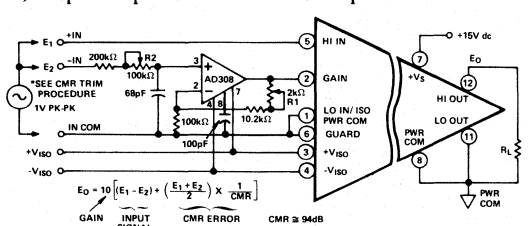


Figure 15. Application of 290A as Instrumentation Amplifier

Isolated Temperature Measurements: Industrial temperature measurements are often performed in harsh environments where line voltages or transients can sometimes be impressed on the temperature sensor. To provide protection for the delicate recording instrumentation, models 290A and 292A can be applied as shown in Figure 16. The Analog Devices' AC2626 probe is a temperature sensor whose output is a current directly proportional to absolute temperature. The isolation amplifier provides the isolated power (+13V dc) as well as the input/output isolation. Zero calibration is performed by placing the AC2626 probe in a zero temperature bath and adjusting R_O for E_O to 0 volts. Full scale output adjustment is performed by placing the AC2626 probe in boiling water (100°C) and adjusting R_S for 1.000V output.

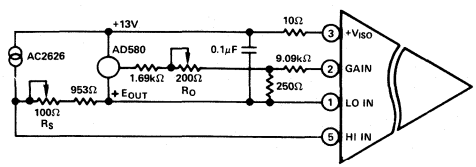


Figure 16. Isolated Temperature Measurements

Current Loop Receiver: Model 290A and 292A can be applied to measurement of analog quantities transmitted via 4-20mA current loops over substantial distances through harsh environments. Figure 17 shows an application of model 290A or 292A as a current loop receiver. A 25Ω resistor converts the 4-20mA current input from a remote loop to a 100–500mV differential voltage input, which the isolator amplifies, isolates, and translates to a 0 to +5V output level at local system ground.

Among the most-helpful characteristics of the isolator in this kind of measurement are the high common-mode rejection (100dB minimum at 60Hz with 1kΩ source unbalance) and the high common-mode rating (±1500 volts dc). The former means low noise pickup; the latter means excellent isolation and protection against large transients. The high common-mode rejection, permitting relatively low input voltage to be used (0.4V span, in this case), permits the use of a low current-metering resistance, which in turn results in low compliance-voltage loading on the current loop, and therefore permits insertion into existing loops without encountering overrange problems. The gain of 12.5 provides a substantial output span, and the floating output permits biasing to a 0 to 5V range.

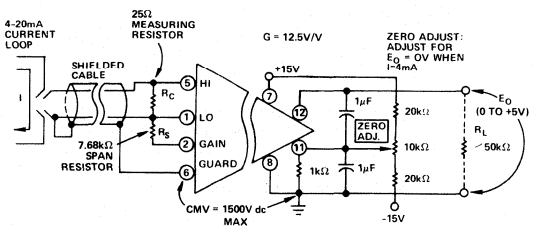


Figure 17. Isolated Analog Interface; 4 to 20mA is Converted to 0 to +5V at the Output, with Up to ±1500V of Isolation

Mixed-Signal Application Specific Integrated Circuits

Analog Devices offers a full spectrum of signal conditioning and conversion capabilities in mixed-signal application specific integrated circuits (ASICs). These chip-level systems can implement combined analog/digital designs with 10- to 14-bit accuracy and 12- to 20-bit resolution that formerly required board-level solutions. Combined with our general purpose DSPs from the ADSP-2100 and ADSP-21000 families, our ASICs can provide custom two-chip solutions to meet complex system requirements.

Analog Devices can incorporate most of the functions of its standard monolithic linear and converter parts in full-custom and semicustom ICs. Full-custom parts optimize performance and space requirements, while cell-based semicustom parts reduce development time and engineering expense. Development costs can be cut further by tailoring a predefined system-on-a-chip known as a Linear System Macro to your application.

Analog's experienced design engineers work with powerful computer-aided design tools to design and lay out your circuit. Design centers are currently in Massachusetts, Japan and Ireland.

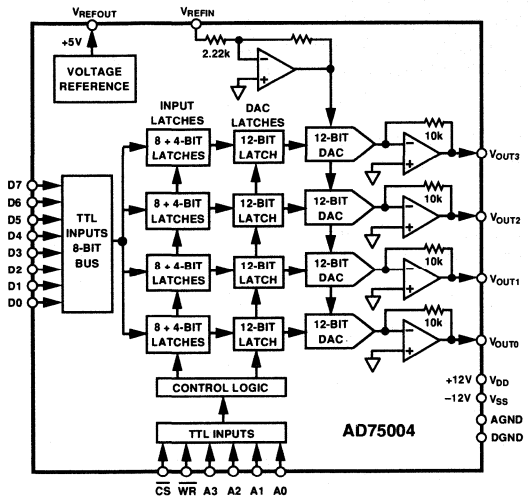
Multiple locations for fabrication, assembly and testing ensure a ready supply of production parts. Products are processed in our MIL-38510 certified facilities.

DESIGN EXAMPLES

Analog Devices has created a variety of customer-specific and function-specific ASICs for data acquisition and signal processing. Two examples of cell-based designs are the following application specific standard products (ASSPs).

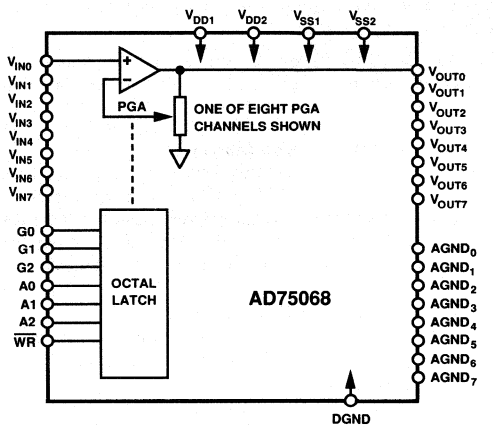
AD75004 Quad DAC

This circuit contains four separate 12-bit D/A converters with amplifiers for voltage output and an on-board reference. Double-buffering latches interface with an 8-bit parallel bus and permit updating of all four channels individually or simultaneously. Outputs swing ±5 V, drive ±5 mA, and settle within 4 μs.



AD75068 Octal Programmable Gain Amplifier

The AD75068 contains eight programmable gain amplifiers (PGAs). Each is complete, including switch/resistor network and gain programming latch, and requires no external components. Each channel may be independently programmed for gains from 1 to 128. A unique circuit design maintains constant 2 MHz bandwidth at all gains and offers very low phase shift; the PGAs also feature low input bias current (<4 pA).



Derivative Circuits

The circuits outlined above can be modified to suit a specific customer's application. For example, the AD75004 quad DAC could be expanded to 6 channels, each of which may have separate reference inputs. The AD75068 could be configured to include filtering. These modifications, when based on standard library cells, can provide the fastest, most cost effective semicustom solution.

Analog/Digital BiCMOS Processes

Analog Devices fabricates ASICs and USICs in four bipolar-CMOS processes, which are also used for volume production of standard ICs. All of these processes are optimized for analog and mixed-signal circuits and handle wide dynamic ranges. They combine bipolar and CMOS transistors with accurate resistors on one chip.

The bipolar transistors provide precision, low noise, low offset input stages and moderate-power output stages. The CMOS devices make low power logic; switches for analog multiplexers, data converters, and switched-capacitor filters; and high impedance input stages and current sources for linear circuitry. The thin-film resistors are very stable over time and temperature, and may be laser-trimmed for tight tolerance on relative matching and absolute values.

The BiMOS II Process

BiMOS II has the most comprehensive cell library of Analog's BiCMOS processes; highlights of the library are listed below. With supply voltages up to 24 V and its very low noise, it can handle signals with a dynamic range of over 20 bits.

BiMOS II features high quality NPN transistors that have very low noise, tight matching, and high Early voltage. These characteristics make possible high performance amplifiers and comparators with low offset input stages and excellent linearity, as well as stable bandgap references.

The 3-μ CMOS builds logic as well as analog switches and high impedance input stages and current sources. The exceptionally stable thin-film resistors are used in precision data converters, programmable-gain amplifiers, and other linear circuits.

BiMOS II uses two levels of metal interconnect as well as self-aligned polysilicon to reduce chip area and layout time. It is fabricated on epitaxial wafers that minimize crosstalk, leakage, and ESD susceptibility.

The BiMOS II process can operate with supplies up to 24 V; the cell library is designed to run on ±12 V supplies. Most BiMOS II cells are designed to accommodate ±5 V signals, although some cells can handle ±8 V or ±10 V swings.

BiMOS II Cell Library

The following table lists key examples of analog and converter cells in the BiMOS II library. Logic cells include gates, counters, registers, microsequencer, PLA, RAM and ROM. Interface cells include 8-bit and 16-bit parallel I/O ports as well as synchronous serial ports and UARTs.

Analog-to-Digital Converter

ADC1210	12-bit resolution, 15 μs conversion time, ±5 V input range, SAR type

Amplifiers

AMPBH10	Bipolar input op amp; gain > 120 dB, BW > 1.6 MHz, offset < 0.5 mV
AMPBH20	Bipolar input op amp; uncompensated, bandwidth > 2.75 MHz at gain ≥ 4
AMPBH30	Bipolar input instrument amplifier; CMRR ≥ 75 dB, nonlinearity < 20 ppm
AMPBH40	Bipolar input op amp; I_B < 1 nA, gain > 120 dB, offset < 0.5 mV
AMPMH10	MOS input op amp; I_B < 50 pA, gain > 120 dB, bandwidth > 1.6 MHz

Comparator

CMPBH10	Bipolar input comparator; clocked; prop delay < 130 ns at 1 mV overdrive

Digital-to-Analog Converters

DAC0810	8-bit res., settling time < 70 ns, 0–248 μA output, INL & DNL < 0.25 LSB
DAC1210	12-bit res., settling time < 100 ns, 0–1 mA output, INL & DNL < 1 LSB
DAC1220	12-bit res., settling time < 25 ns, 4-quad multiplying, INL & DNL < 1 LSB
DAC1410	14-bit resolution, settling time < 120 ns, 0–2 mA output, DNL < 1 LSB

Analog Multiplexers

MUX1B10D	2-channel mux; R_{ON} < 3 kΩ, turn-on time < 30 ns, charge injection ≈ 0.1 pC
MUX1B30	Analog switch; R_{ON} < 100 Ω, turn-on time < 30 ns, charge injection ≈ 1 pC

Voltage References

REF5V30	5 V reference; TC < 25 ppm/°C, I_{load} <4 mA, w/force and sense lines
REF10V10	10 V reference; TC < 25 ppm/°C, I_{load} <4 mA, w/force and sense lines

Sample-and-Hold Amplifier

SHATF10	For 12-bit use; acquisition time < 3 μs, slew rate ≈ 6 V/μs, droop ≈ 2.5 mV/ms

Temperature Sensor

TMP10	Outputs 10 mV/K (3.00 V at 27°C)

ANALOG DEVICES HIGH PERFORMANCE BiCMOS PROCESSES FOR ASICs

Process	Supply Voltage	Gate Length	f_T	Gate Capacity	Features
BiMOS II	24 V	3 μ	300 MHz	2,000	Large Cell Library
ABCMOS	12 V	2 μ	2 GHz	10,000	Highest Speed, Density
LC²MOS-2	12 V	2 μ	1 GHz	5,000	JFET, Buried Zener
LC²MOS-5	30 V	5 μ	1 GHz	1,000	JFET, Buried Zener

Other Processes

While BiMOS II is used for most cell-based USICs, Analog Devices fabricates USICs in three other processes which may be used in applications that require higher speed, lower noise, or higher supply voltage. ABCMOS (Advanced Analog BiCMOS) is our newest, fastest, and densest BiCMOS process. It features 2 GHz NPN devices and fine-geometry CMOS and runs on ±5 V supplies, with ±3 V signal swings. LC²MOS (Linear-Compatible CMOS) has two variants: one runs on ±5 V supplies, with ±3 V signal swings; the other runs on ±15 V, with ±10 V swings. LC²MOS also includes JFETs for very low input noise at high input impedance, and buried Zener diodes with better noise and drift than many bandgap references.

The table above compares our BiCMOS USIC processes and highlights the key features of each. Analog Devices will review your application and recommend the appropriate bipolar process for your needs.

COMPUTER-AIDED DESIGN TOOLS

Designing a high performance mixed-signal IC is inherently more difficult than designing a gate array. The variety of analog and digital functions requires a cell-based approach. However, the use of powerful tools gives high confidence of functionality at first silicon through thorough simulation and layout verification. Complete computer-generated documentation of all schematics and analog and logic simulation waveforms permits thorough evaluation of Analog's design by your design staff before signoff for final layout and fabrication.

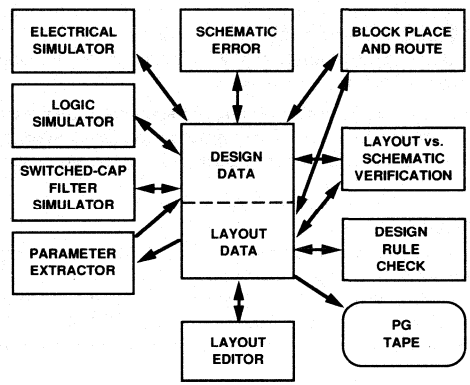
The overall work flow through the CAD environment follows. Key to meeting the special challenges of mixed analog/digital circuitry are the simulation and auto-layout tools, and the unification of design and layout information in a single database. Analog Devices has developed a suite of proprietary computer-aided design tools, called JANUS™, to address these issues and to implement turn-key designs.

The JANUS schematic editor offers numerous time-saving techniques and provides for specification of such data as wire widths, routing layers and routing priorities. It automatically generates a net list used by subsequent tools.

Analog uses several simulators, including electrical, logic and behavioral types. ADICE, a proprietary enhanced version of the SPICE electrical simulator, gives precision simulation of critical analog sections. It uses Newton-Raphson methods to iteratively solve nonlinear time-dependent simultaneous differential equations. It is efficient for circuits up to about 250 active devices and is used for the frequency domain or transient analysis of analog cells such as op amps, or sensitive digital cells such as dynamic RAM.

JANUS is a trademark of Analog Devices, Inc.

COMPUTER-AIDED DESIGN FLOW



Event-driven simulators handle larger circuits, with thousands of devices, and are typically used to simulate logic. The JANUS mixed-signal simulator combines an event-driven simulator with Newton-Raphson methods. It dynamically partitions the circuit to apply the faster event-driven techniques where possible, and the matrix methods where necessary. It also dynamically sizes the matrix and time steps to speed simulation further. The simulator can operate at the transistor level or use behavioral models, or both at the same time, allowing trade-offs between accuracy and speed.

For layout, the challenge is to increase automation while accommodating the layout sensitivity of analog circuitry. Device generators exist for the full range of active and passive devices available in the technology to automatically create a physical representation of the circuit schematic. This layout may be optimized through conventional interactive polygon-pushing.

The JANUS routing editor is driven by the connectivity of the schematics, but allows great freedom to manually control the routing of critical analog signal paths or power/ground lines while autorouting noncritical nets and spacing the layout to achieve automatic enforcement of layout rules. The JANUS routing editor uses up to three interconnect levels, and will automatically expand and compact placement as necessary to achieve 100% routing.

Finally, industry-standard layout verification tools assure conformance of the layout to both the schematic and design rules to give high confidence of functionality in first silicon. The CAD tool suite communicates via industry-standard stream formats to external databases and pattern generators.

TEST AND TRIM

Analog Devices has over 20 years of experience in testing complex circuits and manufactures commercial test systems for precision linear ICs. In each fabrication facility, a computer network integrates Analog Devices, H-P, Teradyne and LTX test equipment. The design, wafer probe and test areas share data on the network for statistical analysis and device modeling.

All Analog Devices ASICs are tested at the wafer level, and most are laser-wafer trimmed to achieve high accuracy. Untrimmed thin-film resistors match within 1% to 0.1%, depending on area. Trimmed resistors can match to better than 0.01%. Wafers may be laser drift trimmed with a hot-chuck probe to minimize the effects of temperature on accuracy.

After packaging, all parts are tested to assure that they meet guaranteed specifications. Environmental handlers can verify parts at multiple temperatures. Burn-in is performed as specified by the customer.

PACKAGING

Analog Devices ICs are available in most modern package types, including high pin-count and surface mount varieties. ASICs may be assembled in any of Analog Devices' standard packages, listed below. This list is constantly expanded and other packages may be used if they are suitable for high performance applications.

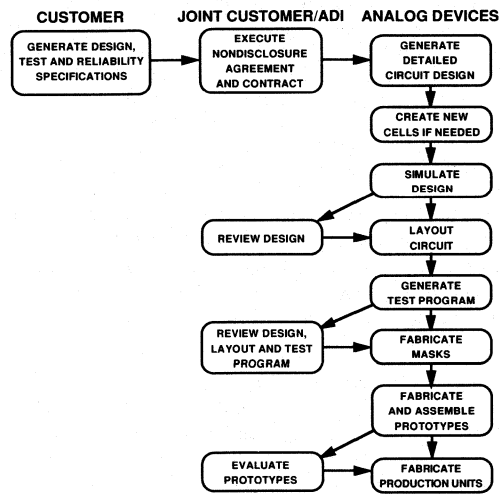
Available Packages

Pin Grid Array (PGA): 68 to 144 pins
Ceramic J Leaded Chip Carrier (CJLCC): 44 to 68 pins
Plastic Quad Flat Pack (PQFP): 44 to 132 pins
Plastic Leaded Chip Carrier (PLCC): 20 to 68 pins
Plastic Dual Inline Package (DIP): 14 to 64 pins
Side-Brazed DIP: 14 to 64 pins
Frit-Seal DIP (Cerdip): 14 to 40 pins
Small Outline (SO): 14 to 28 pins
Ceramic Quad Flat Pack (CQFP): 80 to 104 leads

PROGRAM RESPONSIBILITIES AND INTERFACES

The following figure shows the major phases in developing an ASIC and responsibilities during each phase. The overall development time depends on the complexity of the circuit and on how custom the design is.

Your Analog Devices sales engineer is your first interface for ASIC development. Your local sales office can provide further information on Analog Devices' custom/semicustom capabilities.



Power Supplies
Modular AC/DC Power Supplies

GENERAL DESCRIPTION

Analog Devices offers a broad line of modular ac/dc power supplies that provide both OEMs and designers a reliable, easy to use, low-cost solution to their power requirements. Models are available in PC mountable and chassis mountable designs with 5 volt to 15 volt (single, dual, triple) outputs and current ratings from 25 mA to 5 amps. Since these modular supplies are fully encapsulated, no trimming or external component selection is necessary; simply mount the unit, connect power and output leads, and you're on the air! Most Analog Devices' power supplies are available from stock in both large and small quantities with substantial discounts being applied to large quantity orders.

AC/DC POWER SUPPLY FEATURES

- Current Limit Short Circuit Protection
- PC Mounted and Chassis Mounted Versions
- Single (+5 V), Dual (±12 V, ±15 V), and Triple (±15 V/+5 V, ±15 V/+1 V to +15 V) Output Supplies
- Current Outputs:
  25 mA to 1000 mA for Dual and Triple Output Supplies
  250 mA to 5000 mA for Single Output Supplies
- Wide Input Voltage Range
- Low Output Ripple and Noise
- Excellent Line & Load Regulation Characteristics
- High Temperature Stability
- Free-Air Convection Cooling; No External Heat Sink Required

GENERAL SPECIFICATIONS

Power Requirements

Input Voltage Range:	105 V ac to 125 V ac
Frequency:	50 Hz to 250 Hz

Electrical Specifications

Temperature Coefficient:	0.02%/°C
Output Voltage Accuracy:	±2%, max See Specifications Table
Breakdown Voltage:	500 V rms, min
Isolation Resistance:	50 MΩ
Short Circuit Protection:	All ac/dc power supplies employ current limiting. They can withstand substantial overload including direct short. Prolonged operation should be avoided since excessive temperature rises will occur.

Environmental Requirements

Operating Temperature Range:	−25°C to +71°C
Storage Temperature Range:	−25°C to +85°C

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SPECIFICATIONS – Typical @ +25°C and 115 V ac 60 Hz unless otherwise noted*

	Type	Model	Output Voltage Volts	Output Current mA	Line Reg. max %	Load Reg. max %	Output Voltage Error max	Ripple & Noise mV rms max	Dimensions Inches
PC Board Mounted	Dual Output	904	±15	±50	0.02	0.02	±200 mV −0 mV	0.5	3.5×2.5×0.875
		902	±15	±100	0.02	0.02	+300 mV −0 mV	0.5	3.5×2.5×1.25
		902-2	±15	±100	0.02	0.02	+300 mV −0 mV	0.5	3.5×2.5×0.875
		920	±15	±200	0.02	0.02	+300 mV −0 mV	0.5	3.5×2.5×1.25
		925	±15	±350	0.02	0.02	±1%	0.5	3.5×2.5×1.62
		921	±12	±240	0.02	0.02	+300 mV −0 mV	0.5	3.5×2.5×1.25
	Single Output	905	5	1000	0.02	0.05	±1%	1	3.5×2.5×1.25
		922	5	2000	0.02	0.05	±1%	1	3.5×2.5×1.62
		928	5	3000	0.05	0.10	±2%	5 (typ)	3.5×2.5×1.25
	Triple Output	923	±15	±100	0.02	0.02	±1%	0.5	3.5×2.5×1.25
			+5	500	0.02	0.05	±1%	0.5	
		927	±15	±150	0.02	0.02	±2%	0.5 (typ)	3.5×2.5×1.62
			+5	1000	0.02	0.10	±2%	1.0 (typ)	
Chassis Mounted	Dual Output	970	±15	±200	0.05	0.05	±2%	1	4.4×2.7×1.45
		975	±15	±500	0.05	0.05	±2%	1	4.4×2.7×2.00
	Single Output	955	5	1000	0.05	0.15	±2%	2	4.4×2.7×1.45
		976	5	3000	0.05	0.10	±2%	5 (typ)	4.75×2.7×1.45
		977	5	5000	0.05	0.10	±2%	5 (typ)	4.75×2.7×1.45
	Triple Output	974	±15	±150	0.02	0.02	±2%	0.5 (typ)	4.75×2.7×1.45
			+5	1000	0.02	0.10	±2%	1.0 (typ)	

*Consult Analog Devices Power Supplies Catalog for additional information.
Specifications subject to change without notice.

Power Supplies
Modular DC/DC Converters

GENERAL DESCRIPTION

Analog Devices' line of compact dc/dc converters offers system designers a means of supplying a reliable, easy to use, low cost solution to a variety of floating (analog and digital) power applications. These devices provide high accuracy, short circuit protected, regulated outputs with very low output noise and ripple characteristics.

Fourteen models are offered in five power levels of 1 watt, 1.8 watts, 4.5 watts, 6 watts and 12 watts. Input voltage versions include 5 volt, 12 volt, 24 volt and 28 volt with output ranges as follows: +5 volt, ±12 volts and ±15 volts at ±60 mA to 1000 mA output current capability.

Most models are high efficiency (typically over 60% at full load) and feature complete 6-sided continuous shielding for EMI/RFI protection. A π-type input filter is contained, in some models, which virtually eliminates the effects of reflected input ripple current. Most Analog Devices' dc/dc converters are available from stock in both large and small quantities with substantial discounts being applied to large quantity orders.

DC/DC POWER SUPPLY FEATURES

- Inaudible (>20 kHz) Converter Switching Frequency
- Continuous, Six-Sided EMI/RFI Shielding Except on 1 Watt and 1.8 Watt Models
- Output Short Circuit Protection (Either Output to Common)
- Automatic Restart After Short Condition Removed
- Automatic Starting with Reverse Current Injected into Outputs
- Low Output Ripple and Noise
- High Temperature Stability
- Free Air Convection Cooling

  No external heat sink or specification derating is required over the operating temperature range.

GENERAL SPECIFICATIONS FOR 1 W AND 1.8 W MODELS

Line Regulation – Full Range: ±0.3% (±1% max, 949)
Load Regulation – No Load to Full Load: ±0.4% (±0.5% max, 949)
Output Noise and Ripple: 20 mV p–p, with 15 μF tantalum capacitor across each output (2 mV rms max, 949)
Breakdown Voltage: 300 V dc min (500 V dc min, 949)
Input Filter Type: π
Operating Temperature Range: −25°C to +71°C
Storage Temperature Range: −40°C to +125°C (+100°C, 949)
Fusing: If input fusing is desired, we recommend the use of a slow blow type fuse that is rated at 150%–200% of the dc/dc converter's full load input current.

GENERAL SPECIFICATIONS FOR 4.5 W, 6 W AND 12 W MODELS

Line Regulation – Full Range: ±0.07% max (±0.02% max, 951, 960 Series) (±0.1% max, 943)
Load Regulation – No Load to Full Load: ±0.07% max (±0.02% max, 951, 960 Series) (±0.1% max, 943)
Output Noise and Ripple: 1 mV rms max
Breakdown Voltage: 500 V dc min
Input Filter Type: π
Operating Temperature Range: −25°C to +71°C
Storage Temperature Range: −40°C to +125°C
Fusing: If input fusing is desired, we recommend the use of a slow blow type fuse that is rated at 150%–200% of the dc/dc converter's full load input current.

SPECIFICATIONS – Typical @ +25°C at nominal input voltage unless otherwise noted*

Model	Output Voltage Volts	Output Current mA	Input Voltage Volts	Input[1] Voltage Range Volts	Input Current Full Load	Output Voltage Error max	Temperature Coefficient /°C max	Efficiency Full Load min	Dimensions Inches
943	5	1000	5	4.75/5.25	1.52A	±1%	±0.02%	62%	2.0×2.0×0.38
958	5	100	5	4.5/5.5	200 mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
941	±12	±150	5	4.75/5.25	1.17A	±1%	±0.01%	58%	2.0×2.0×0.38
960	±12	±40	5	4.5/5.5	384 mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
962	±15	±33	5	4.5/5.5	396 mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
964	±15	±33	12	10.8/13.2	165 mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
965	±15	±190	5	4.65/5.5	1.7 A	±1%	±0.005% (typ)	62% (typ)	2.0×2.0×0.38
966	±15	±190	12	11.2/13.2	710 mA	±1%	±0.005% (typ)	62% (typ)	2.0×2.0×0.38
967	±15	±190	24	22.3/26.4	350 mA	±1%	±0.005% (typ)	62% (typ)	2.0×2.0×0.38
949	±15	±60**	5	4.65/5.5	0.6 A	±2%	±0.03%	58%	2.0×1.0×0.375
940	±15	±150	5	4.75/5.25	1.35 A	±1%	±0.01%	62%	2.0×2.0×0.38
953	±15	±150	12	11/13	0.6 A	±0.5%	±0.01%	62%	2.0×2.0×0.38
945	±15	±150	28	23/31	250 mA	±0.5%	±0.01%	61%	2.0×2.0×0.38

NOTES
[1]Models 940 and 941 will deliver up to 120 mA output current (and Model 943 will deliver up to 600 mA) over an input voltage range of 4.65 V dc and 5.5 V dc.
*Consult Analog Devices Power Supplies Catalog for additional information.
**Single-ended or unbalanced operation is permissible such that total output current load does not exceed a total of 120 mA.
Specifications subject to change without notice.

Package Information
Contents

ADI Letter Designator	PMI Letter Designator	Package Description	MIL-STD-1835 Applicable Configuration	Page
Side Brazed DIP (Ceramic)				
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D-16	QB*	16-Lead	CDIP2-T16	8-4
D-18	XB*	18-Lead	CDIP2-T18	8-5
Bottom Brazed DIP (Ceramic)				
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Leadless Chip Carrier (Ceramic)				
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N-16	P	16-Lead		8-17
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Q-16	Q	16-Lead	GDIP1-T16	8-21
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R-8		8-Lead		8-23
	SO-8	8-Lead		8-24
	SO-14	14-Lead		8-25
R-16A	SO-16	16-Lead (Narrow Body)		8-26
R-16	SOL-16	16-Lead (Wide Body)		8-27
R-20	SOL-20	20-Lead (Wide Body)		8-28
Single In-Line Package (SIP)				
Y-10		10-Lead		8-29
Leaded Chip Carrier				
Z-8A		8-Lead		8-30

*Special Order Only

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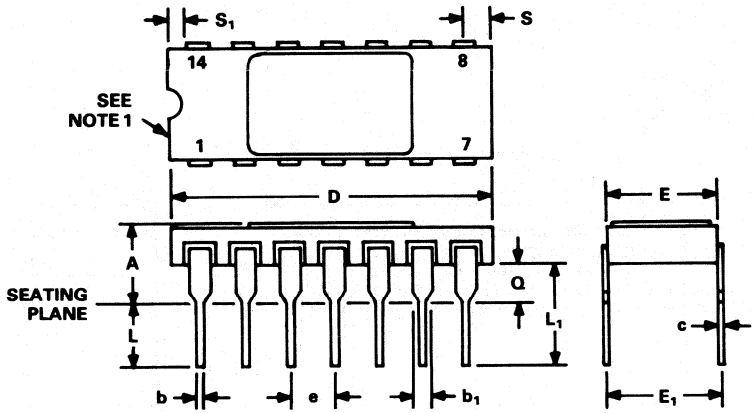
D-14

14-Lead Side Brazed Ceramic DIP
(YB Suffix)



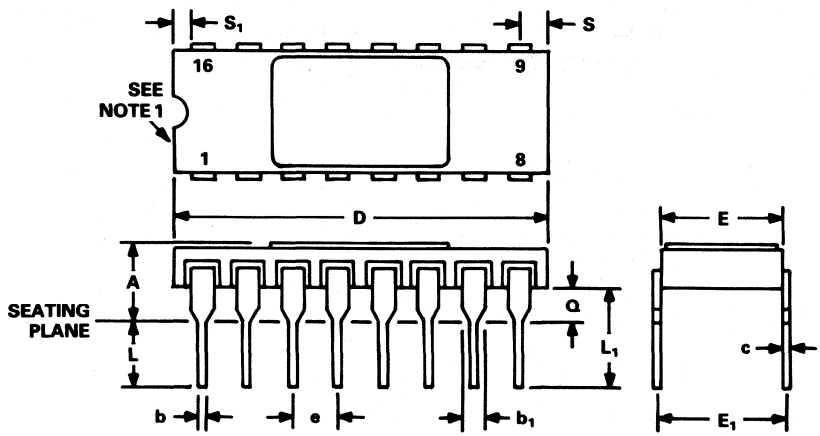
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2, 6
c	0.008	0.015	0.20	0.38	6
D		0.785		19.94	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	
e	0.100 BSC		2.54 BSC		7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08 mm) measured at the center of the flat, when hot solder DIP lead finish is applied.
7. Twelve spaces.

8

D-16

16-Lead Side Brazed Ceramic DIP
(QB Suffix)



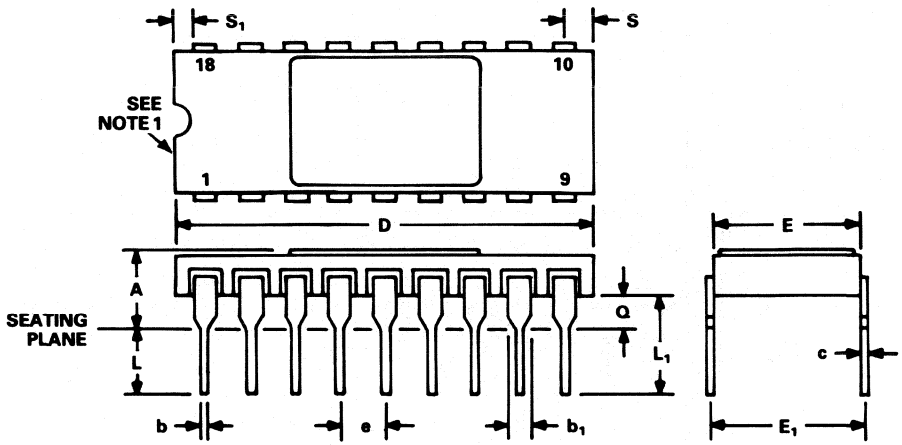
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2, 6
c	0.008	0.015	0.20	0.38	6
D		0.840		21.34	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	
e	0.100 BSC		2.54 BSC		7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.080		2.03	5
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023″ (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003″ (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Fourteen spaces.

D-18

18-Lead Side Brazed Ceramic DIP
(XB Suffix)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2, 6
c	0.008	0.015	0.20	0.38	6
D		0.960		24.38	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	
e	0.100 BSC		2.54 BSC		7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5

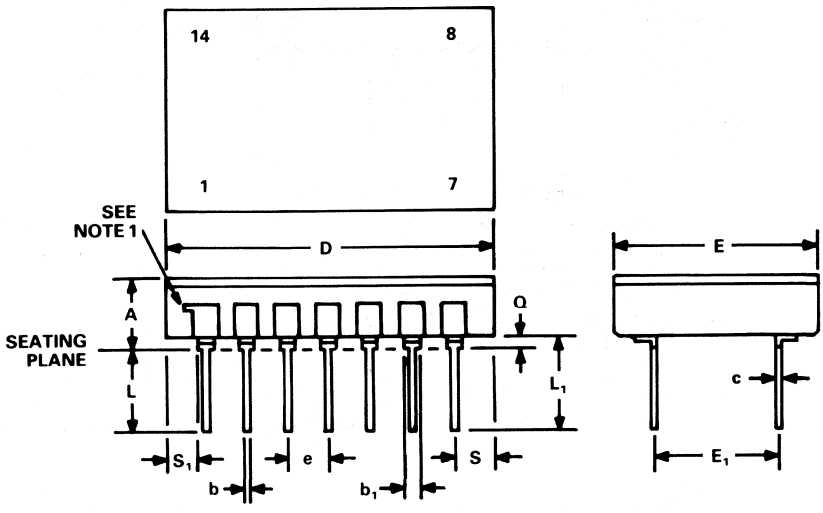
NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023″ (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003″ (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Sixteen spaces.

8

DH-14B

14-Lead Bottom Brazed Ceramic (Large Capacity)



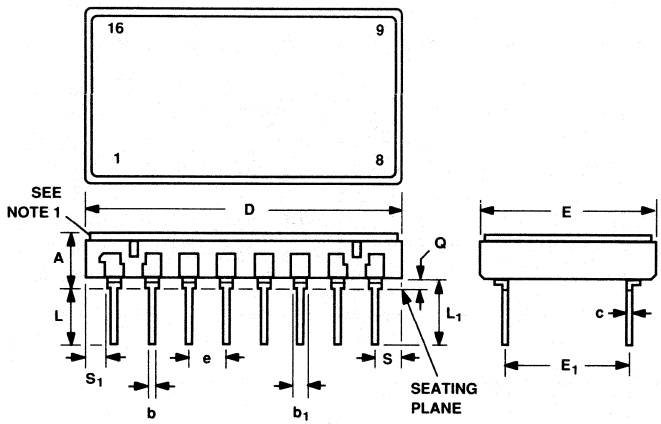
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.156	0.220	3.96	5.59	
b	0.014	0.023	0.36	0.58	
b_1	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	
D	0.835	0.875	21.21	22.23	
E	0.480	0.510	12.19	12.95	
E_1	0.295	0.305	7.49	7.75	6
e	0.100 BSC		2.54 BSC		4, 7
L	0.145		3.68		
L_1	0.180		4.57		
Q	0.015	0.035	0.38	0.89	3
S		0.137		3.48	5
S_1	0.060		1.52		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The basic pin spacing is 0.100" (2.54 mm) between centerlines.
5. Applies to all four corners.
6. E_1 shall be measured at the centerline of the leads.
7. Twelve spaces.

DH-16C

16-Lead Bottom Brazed Ceramic DIP
(Large Cavity)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.016	0.020	0.41	0.51	
b_1	0.030	0.070	0.76	1.78	2
c	0.009	0.012	0.23	0.31	
D		0.900		22.86	
E	0.480	0.500	12.19	12.70	
E_1	0.290	0.310	7.37	7.87	6
e	0.100 BSC		2.54 BSC		4, 7
L	0.145		3.68		
L_1	0.180		4.57		
Q	0.015	0.035	0.38	0.89	3
S		0.098		2.49	5
S_1	0.005		0.13		5

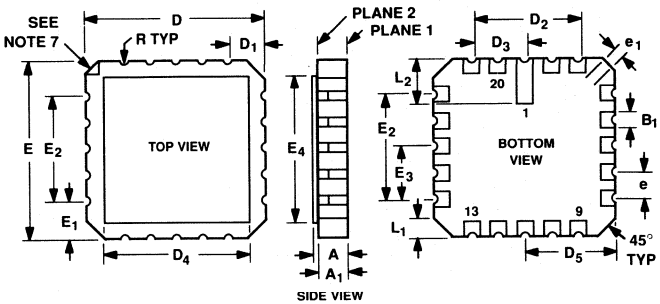
NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023″ (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The basic pin spacing is 0.100″ (2.54 mm) between centerlines.
5. Applies to all four corners.
6. E1 shall be measured at the center line of all the leads, at standoff.
7. Fourteen spaces.

8

E-20A

20-Terminal Leadless Chip Carrier
(RC Suffix)



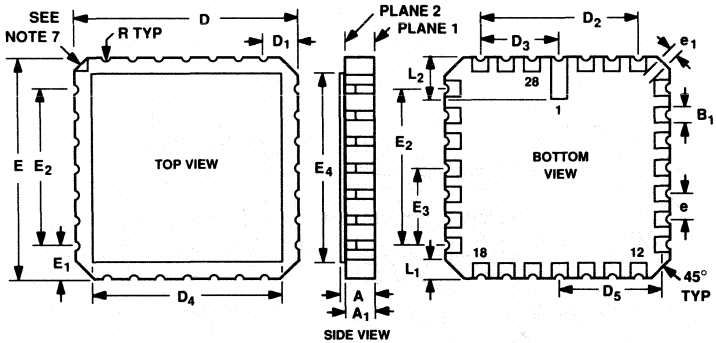
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.064	0.100	1.63	2.54	5
A_1	0.054	0.088	1.37	2.24	
B_1	0.022	0.028	0.56	0.71	2
D	0.342	0.358	8.69	9.09	
D_1	0.075 REF		1.91 REF		
D_2	0.200 REF		5.08 REF		
D_3	0.100 REF		2.54 REF		
D_4		0.358		9.09	3
D_5	0.150 BSC		3.81 BSC		
E	0.342	0.358	8.69	9.09	
E_1	0.075 REF		1.91 REF		
E_2	0.200 REF		5.08 REF		
E_3	0.100 REF		2.54 REF		
E_4		0.358		9.09	3
e	0.050 BSC		1.27 BSC		
e_1	0.015		0.38		1
L_1	0.045	0.055	1.14	1.40	
L_2	0.075	0.095	1.90	2.41	4
R	0.007	0.011	0.18	0.28	

NOTES

1. A minimum clearance of 0.015″ (0.381 mm) is maintained between corner terminals.
2. Electrical connection is required on Plane 1. Metalization is optional on Plane 2. However, if Plane 2 is metalized, it must be electrically connected.
3. A minimum clearance of 0.020″ (0.508 mm) is maintained between overall dimensions $D_4 \times E_4$ and all other features including metalization, chamfers and edges.
4. Nonelectrical feature for No. 1 terminal identification, optical orientation or handling purposes shall be within the shaded area shown on Plane 2.
5. Dimension A controls the overall package thickness.
6. Length of pad metalization may increase only toward package periphery.
7. When space is available, the index corner may be metalized on either or both Planes 1 and 2. The package edge at the index corner shall not be metalized.

E-28A

28-Terminal Leadless Chip Carrier
(TC Suffix)

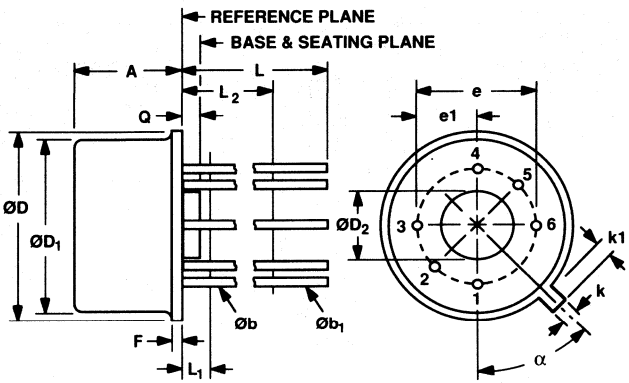


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.064	0.100	1.63	2.54	5
A_1	0.054	0.088	1.37	2.24	
B_1	0.022	0.028	0.56	0.71	2
D	0.442	0.458	11.23	11.63	
D_1	0.075 REF		1.91 REF		
D_2	0.300 REF		7.62 REF		
D_3	0.150 REF		3.81 REF		
D_4		0.458		11.63	3
D_5	0.200 BSC		5.08 BSC		
E	0.442	0.458	11.23	11.63	
E_1	0.075 REF		1.91 REF		
E_2	0.300 REF		7.62 REF		
E_3	0.150 REF		3.81 REF		
E_4		0.458		11.63	3
e	0.050		1.27		
e_1	0.015		0.38		1
L_1	0.045	0.055	1.14	1.40	
L_2	0.075	0.095	1.90	2.41	4
R	0.007	0.011	0.18	0.28	

NOTES

1. A minimum clearance of 0.015" (0.381 mm) is maintained between corner terminals.
2. Electrical connection is required on Plane 1. Metalization is optional on Plane 2. However, if Plane 2 is metalized, it must be electrically connected.
3. A minimum clearance of 0.020" (0.508 mm) is maintained between overall dimensions $D_4 \times E_4$ and all other features including metalization, chamfers and edges.
4. Nonelectrical feature for No. 1 terminal identification, optical orientation or handling purposes shall be within the shaded area shown on Plane 2.
5. Dimension A controls the overall package thickness.
6. Length of pad metalization may increase only toward package periphery.
7. When space is available, the index corner may be metalized on either or both Planes 1 and 2. The package edge at the index corner shall not be metalized.

6-Lead TO-78 Metal Can
(H Suffix)



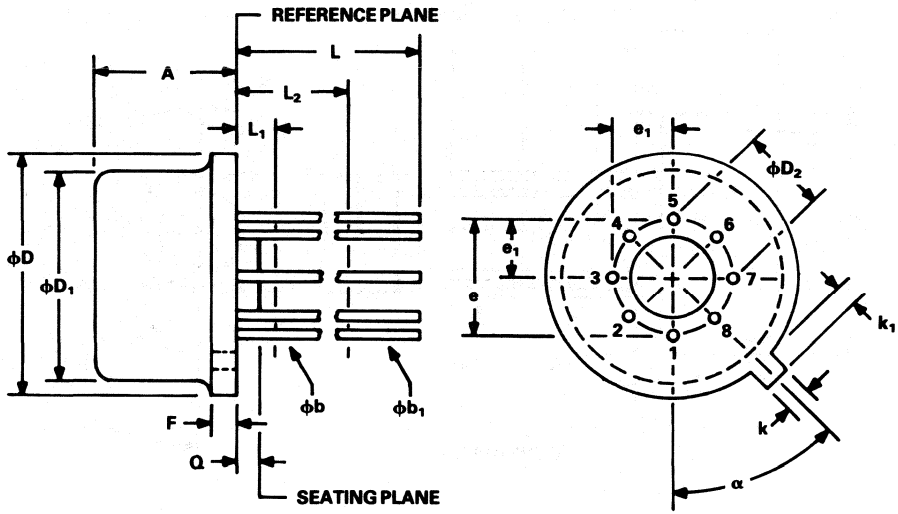
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	
ϕb	0.016	0.019	0.41	0.48	1
ϕb_1	0.016	0.021	0.41	0.53	1
ϕD	0.335	0.370	8.51	9.40	
ϕD_1	0.305	0.335	7.75	8.51	
ϕD_2	0.110	0.160	2.79	4.06	
e	0.200 BSC		5.08 BSC		3
e_1	0.100 BSC		2.54 BSC		3
F		0.040		1.02	
k	0.027	0.034	0.69	0.86	
k_1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L_1		0.050		1.27	1
L_2	0.250		6.35		1
Q	0.010	0.045	0.25	1.14	
α	45° BSC		45° BSC		3

NOTES

1. (All leads) ϕb applies between L_1 and L_2. ϕb_1 applies between L_2 and 0.500″ (12.70 mm) from the reference plane. Diameter is uncontrolled in L_1 and beyond 0.500″ (12.70 mm) from the reference plane.
2. Measured from the maximum diameter of the product.
3. Leads having a maximum diameter 0.019″ (0.48 mm) measured in gaging plane 0.054″ (1.37 mm) + 0.001″ (0.03 mm) – 0.000″ (0.00 mm) below the base plane of the product is within 0.007″ (0.18 mm) of their true position relative to a maximum width tab.

H-08A

8-Lead Metal Can (TO-99)
(J Suffix)



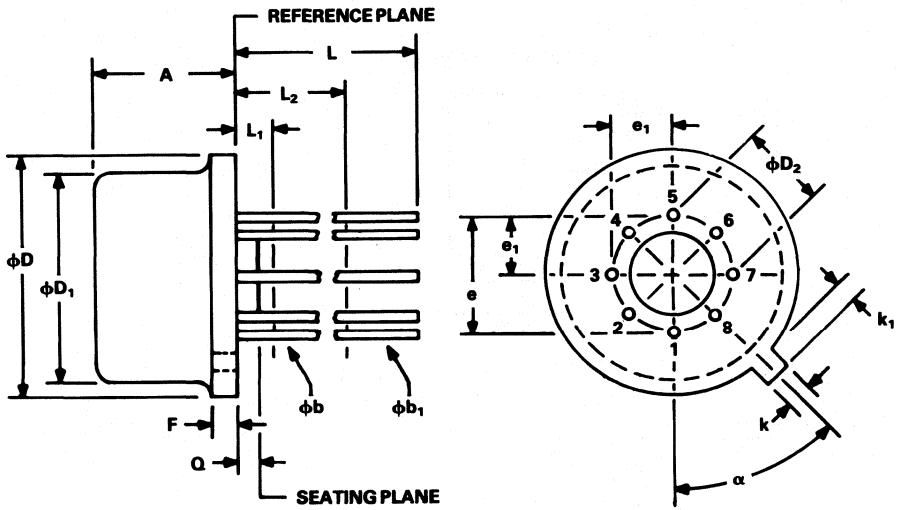
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.165	0.185	4.19	4.70	
ϕb	0.016	0.019	0.41	0.48	1,4
ϕb_1	0.016	0.021	0.41	0.53	1,4
ϕD	0.335	0.370	8.51	9.40	
ϕD_1	0.305	0.335	7.75	8.51	
ϕD_2	0.110	0.160	2.79	4.06	
e	0.200 BSC		5.08 BSC		3
e_1	0.100 BSC		2.54 BSC		3
F		0.040		1.02	
k	0.027	0.034	0.69	0.86	
k_1	0.027	0.045	0.69	1.14	
L	0.500	0.750	12.70	19.05	
L_1		0.050		1.27	
L_2	0.250		6.35		
Q	0.010	0.045	0.25	1.14	
α	45° BSC		45° BSC		3

NOTES

1. (All leads) ϕb applies between L_1 and L_2. ϕb_1 applies between L_2 and 0.500" (12.70mm) from the reference plane. Diameter is uncontrolled in L_1 and beyond 0.500" (12.70mm) from the reference plane.
2. Measured from the maximum diameter of the product.
3. Leads having a maximum diameter 0.019" (0.48mm) measued in gauging plane 0.054" (1.37mm) + 0.001" (0.03mm) – 0.000" (0.00mm) below the base plane of the product are within 0.007" (0.18mm) of their true position relative to the maximum width tab.
4. All leads – increase maximum limit 0.003" (0.08mm) when hot solder dip finish is applied.

H-08B

8-Lead Metal Can (TO-99 Style)



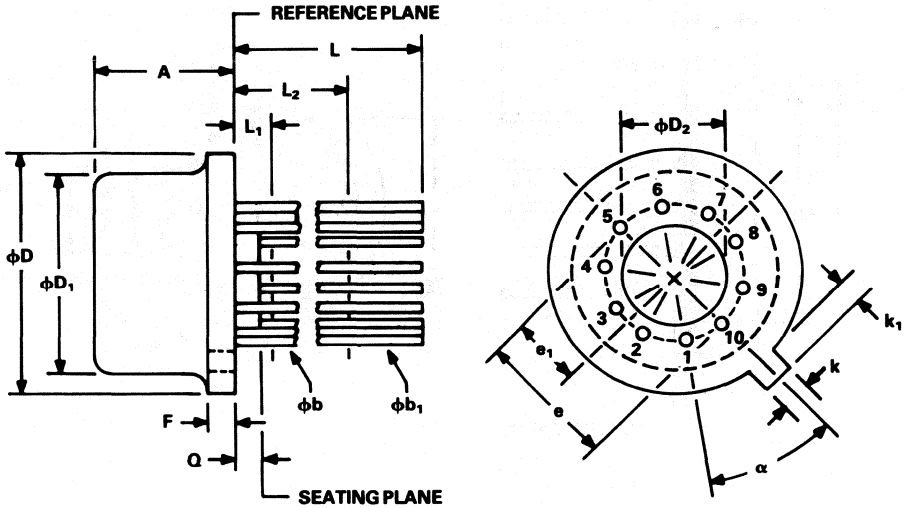
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.165	0.185	4.19	4.70	
ϕb	0.016	0.019	0.41	0.48	1, 4
ϕb_1	0.016	0.021	0.41	0.53	1, 4
ϕD	0.335	0.370	8.51	9.40	
ϕD_1	0.305	0.335	7.75	8.51	
ϕD_2	0.110	0.160	2.79	4.06	
e	0.230 BSC		5.84 BSC		3
e_1	0.115 BSC		2.92 BSC		3
F		0.040		1.02	
k	0.027	0.034	0.69	0.86	
k_1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L_1		0.050		1.27	1
L_2	0.250		6.35		1
Q	0.010	0.045	0.25	1.14	
α	45° BSC		45° BSC		3

NOTES

1. (All leads) ϕb applies between L_1 and L_2. ϕb_1 applies between L_2 and 0.500" (12.70mm) from the reference plane. Diameter is uncontrolled in L_1 and beyond 0.500" (12.70mm) from the reference plane.
2. Measured from the maximum diameter of the product.
3. Leads having a maximum diameter 0.019" (0.48mm) measued in gauging plane 0.054" (1.37mm) + 0.001" (0.03mm) – 0.000" (0.00mm) below the base plane of the product are within 0.007" (0.18mm) of their true position relative to the maximum width tab.
4. All leads – increase maximum limit 0.003" (0.08mm) when hot solder dip finish is applied.

H-10A

10-Lead Metal Can (TO-100)
(K Suffix)



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.165	0.185	4.19	4.70	
ϕb	0.016	0.019	0.41	0.48	1,4
ϕb_1	0.016	0.021	0.41	0.53	1,4
ϕD	0.335	0.370	8.51	9.40	
ϕD_1	0.305	0.335	7.75	8.51	
ϕD_2	0.110	0.160	2.79	4.06	
e	0.230 BSC		5.84 BSC		3
e_1	0.115 BSC		2.92 BSC		3
F		0.040		1.02	
k	0.027	0.034	0.69	0.86	
k_1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L_1		0.050		1.27	1
L_2	0.250		6.35		1
Q	0.010	0.045	0.25	1.14	
α	36° BSC		36° BSC		3

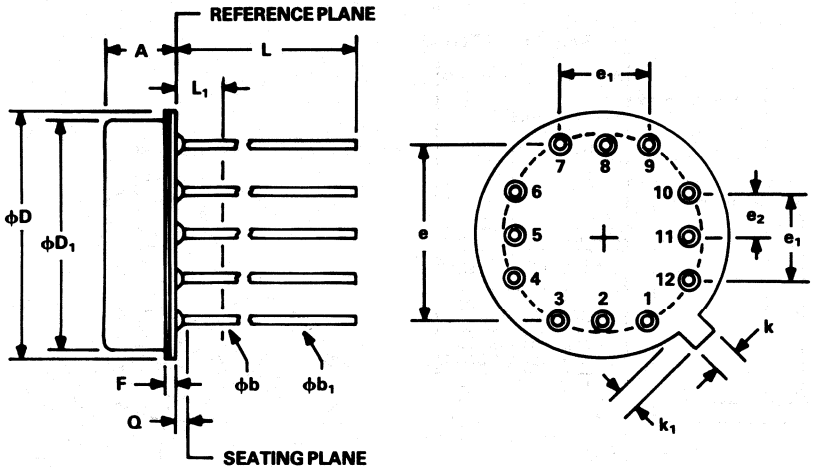
NOTES

1. (Three Leads) ϕb_2 applies between L_1 and L_2. ϕb applies between L_2 and 0.5" (12.70mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.5" (12.70mm) from seating plane.
2. Leads having maximum diameter 0.019" (0.48mm) measured in gauging plane 0.054" (1.4mm) + 0.001" (0.03mm) – 0.000" (0.00mm) below the seating plane of the device are within 0.007" (0.18mm) of their true positions relative to a maximum-width tab.
3. Measured from maximum diameter of the actual device.
4. All leads – increase maximum limit by 0.003" (0.08mm) when hot solder dip finish is applied.

8

H-12A

12-Lead Metal Can (TO-8 Style)



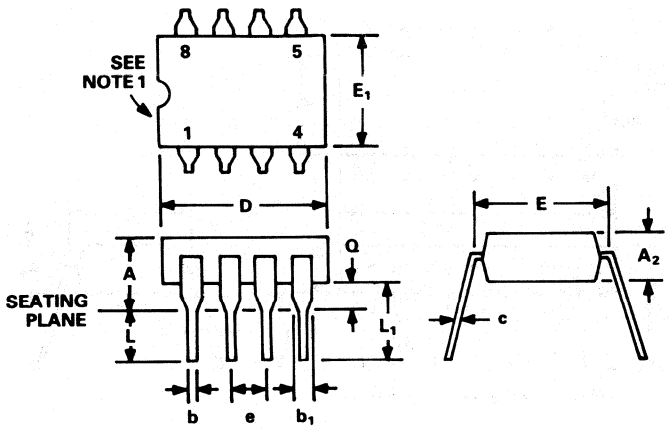
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.148	0.181	3.76	4.60	
ϕb	0.016	0.019	0.41	0.48	1
ϕb_1	0.016	0.021	0.41	0.53	1
ϕD	0.592	0.615	15.04	15.62	
ϕD_1	0.545	0.555	13.84	14.10	
e	0.400 BSC		10.16 BSC		3
e_1	0.200 BSC		5.08 BSC		3
e_2	0.100 BSC		2.54 BSC		3
F		0.040		1.02	
k	0.026	0.036	0.66	0.91	
k_1	0.026	0.037	0.66	0.94	2
L	0.375		9.53		1
L_1		0.050		1.27	1
Q	0.000	0.045	0.000	1.14	

NOTES

1. (All leads) ϕb applies between L and L_1. ϕb_1 applies between L_1 and 0.375″ (9.50 mm) from the reference plane. Diameter is uncontrolled in L_1 and beyond 0.375″ (9.50 mm) from the reference plane.
2. Measured from the maximum diameter of the product.
3. Leads having a maximum diameter 0.019″ (0.48 mm) measured in gaging plane 0.054″ (1.37 mm) + 0.001″ (0.03 mm) – 0.000″ (0.00 mm) below the base plane of the product is within 0.007″ (0.18 mm) of their true position relative to a maximum width tab.

N-8

8-Lead Plastic DIP
(P Suffix)

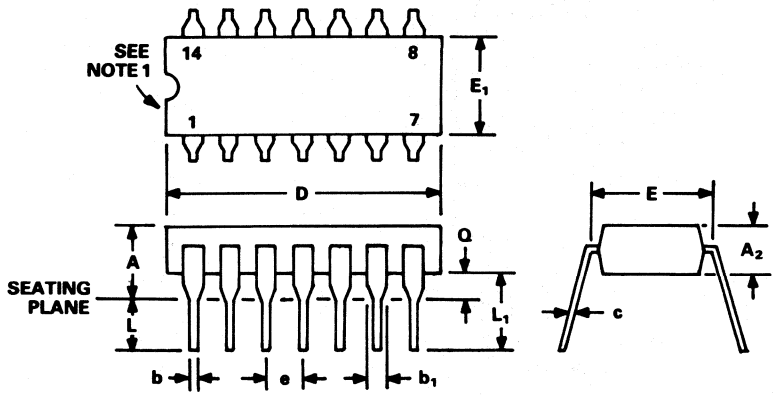


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	0.348	0.430	8.84	10.92	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.115	0.160	2.93	4.06	
L_1	0.130		3.30		
Q	0.015	0.060	0.38	1.52	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. This dimension does not include mold flash or protrusions.

N-14

14-Lead Plastic DIP
(P Suffix)



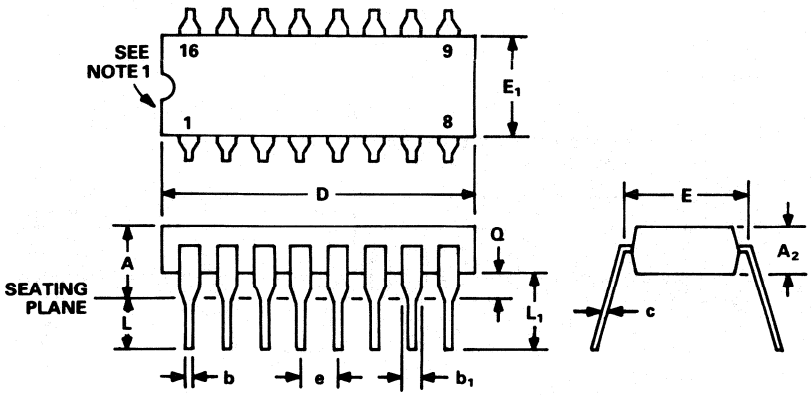
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	0.725	0.795	18.42	20.19	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.115	0.160	2.93	4.06	
L_1	0.130		3.30		
Q	0.015	0.060	0.38	1.52	

NOTES

1. **Index area; a notch or a lead one identification mark is located adjacent to lead one.**
2. **This dimension does not include mold flash or protrusions.**

N-16

16-Lead Plastic DIP
(P Suffix)



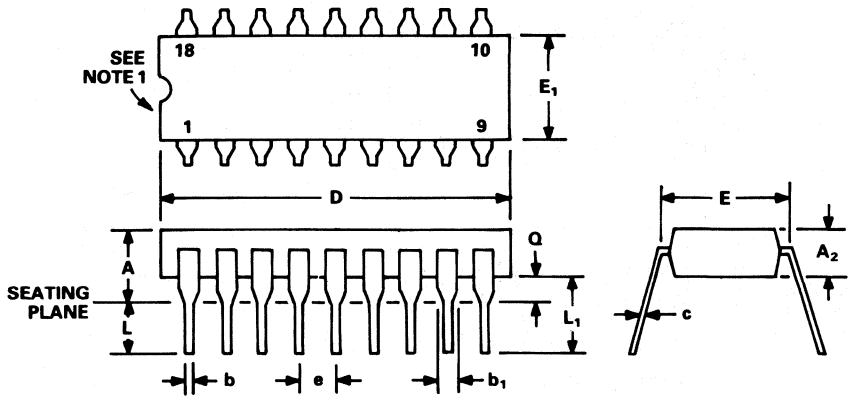
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	0.745	0.840	18.93	21.33	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.115	0.160	2.93	4.06	
L_1	0.130		3.30		
Q	0.015	0.060	0.38	1.52	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. This dimension does not include mold flash or protrusions.

8

N-18

18-Lead Plastic DIP
(P Suffix)



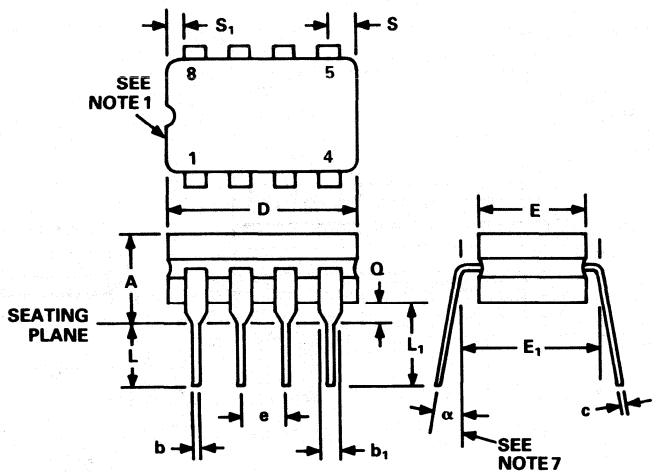
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	0.845	0.925	21.47	23.49	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.115	0.160	2.93	4.06	
L_1	0.130		3.30		
Q	0.015	0.060	0.38	1.52	

NOTES

1. **Index area; a notch or a lead one identification mark is located adjacent to lead one.**
2. **This dimension does not include mold flash or protrusions.**

Q-8

8-Lead Cerdip
(Z Suffix)

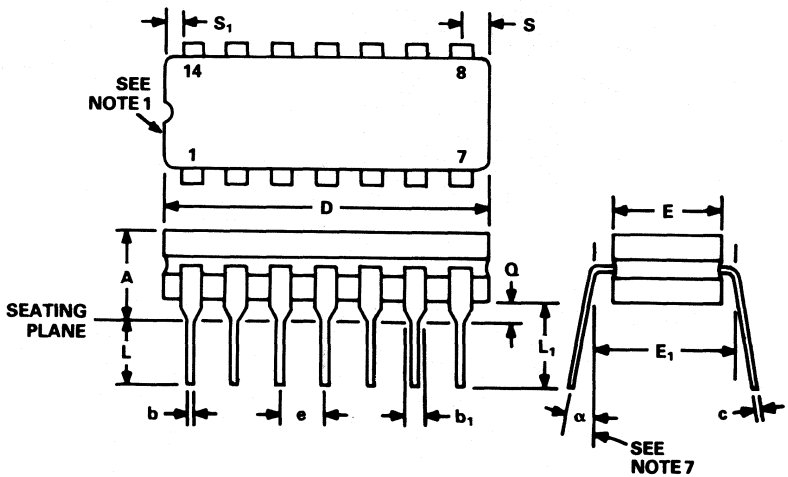


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2, 7
c	0.008	0.015	0.20	0.38	7
D		0.405		10.29	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.100 BSC		2.54 BSC		8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.055		1.4	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Leads center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003" (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Six spaces.

Q-14

14-Lead Cerdip
(Y Suffix)



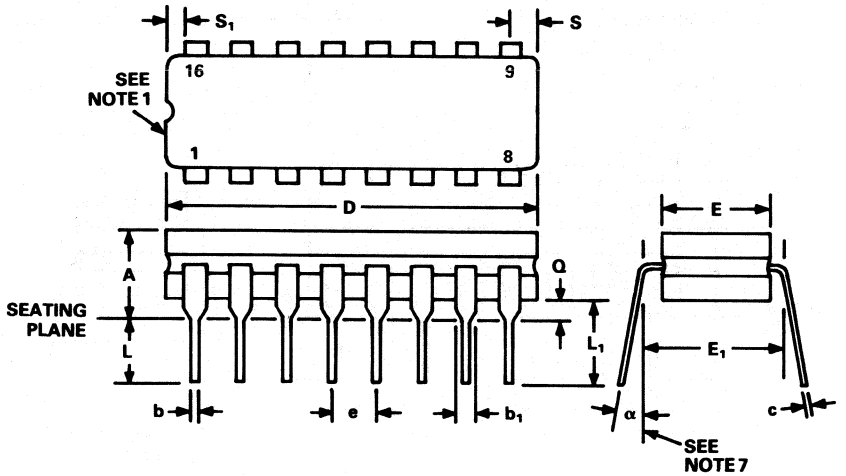
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2, 7
c	0.008	0.015	0.20	0.38	7
D		0.785		19.94	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.100 BSC		2.54 BSC		8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003" (0.08 mm) measured at the center of the flat when hot solder dip lead finish is applied.
8. Twelve spaces.

Q-16

16-Lead Cerdip
(Q Suffix)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2, 7
c	0.008	0.015	0.20	0.38	7
D		0.840		21.34	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.100 BSC		2.54 BSC		8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.080		2.03	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

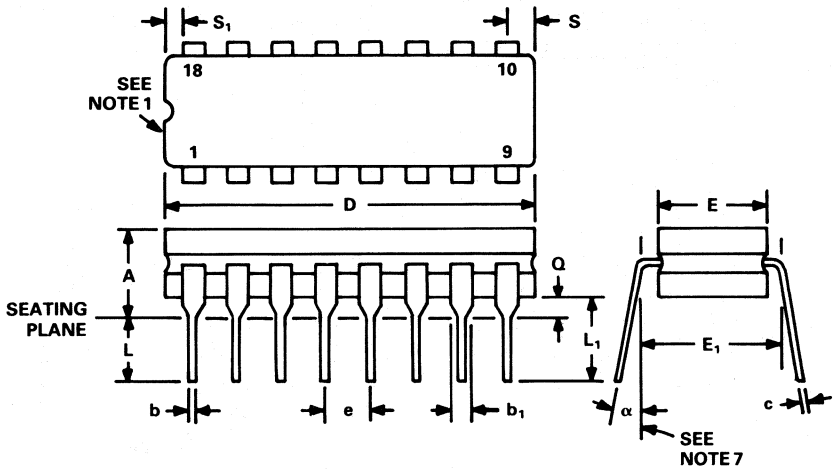
NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003" (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Fourteen spaces.

8

Q-18

18-Lead Cerdip
(X Suffix)



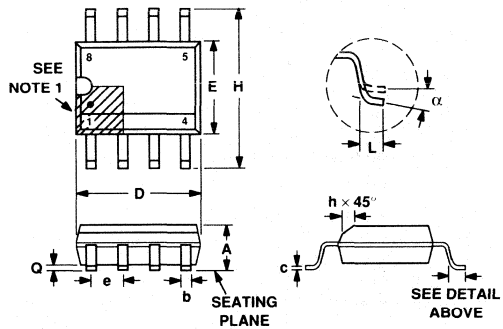
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2, 7
c	0.008	0.015	0.20	0.38	7
D		0.960		24.38	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.100 BSC		2.54 BSC		8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003" (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Sixteen spaces.

R-8

8-Lead Narrow-Body (SO)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.094	0.102	2.39	2.59	2
b	0.0138	0.0192	0.35	0.49	
c	0.0075	0.0098	0.19	0.25	
D	0.1890	0.1968	4.80	5.00	
E	0.1497	0.1574	3.80	4.00	
H	0.2284	0.2440	5.80	6.20	
e	0.0500 BSC		1.27 BSC		
h	0.0099	0.0196	0.25	0.50	
L	0.0160	0.0500	0.41	1.27	
Q	0.0040	0.0098	0.10	0.25	
α	0°	8°	0°	8°	

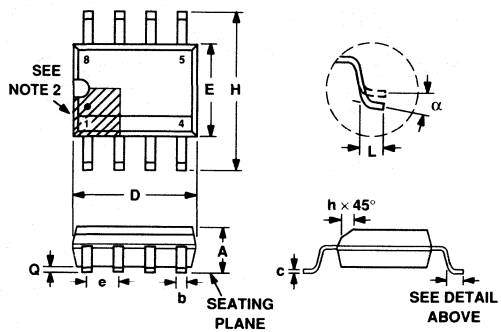
NOTES

1. **Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.**
2. **The R-8 and SO-8 packages differ only in this dimension.**

8

SO-8

8-Lead Narrow-Body SO
(S-Suffix)



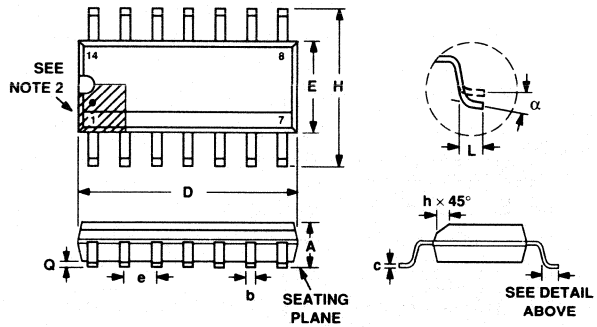
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	3
b	0.0138	0.0192	0.35	0.49	
c	0.0075	0.0098	0.19	0.25	
D	0.1890	0.1968	4.80	5.00	
E	0.1497	0.1574	3.80	4.00	
H	0.2284	0.2440	5.80	6.20	
e	0.0500 BSC		1.27 BSC		
h	0.0099	0.0196	0.25	0.50	
L	0.0160	0.0500	0.41	1.27	
Q	0.0040	0.0098	0.10	0.25	
α	0°	8°	0°	8°	

NOTES

1. **Package dimensions conform to JEDEC specification MS-012-AA (Issue A, June 1985).**
2. **Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.**
3. **The SO-8 and R-8 packages differ only in this dimension.**

SO-14

14-Lead Narrow-Body SO
(S-Suffix)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	
b	0.0138	0.0192	0.35	0.49	
c	0.0075	0.0098	0.19	0.25	
D	0.3367	0.3444	8.55	8.75	
E	0.1497	0.1574	3.80	4.00	
H	0.2284	0.2440	5.80	6.20	
e	0.0500 BSC		1.27 BSC		
h	0.0099	0.0196	0.25	0.50	
L	0.0160	0.0500	0.41	1.27	
Q	0.0040	0.0098	0.10	0.25	
α	0°	8°	0°	8°	

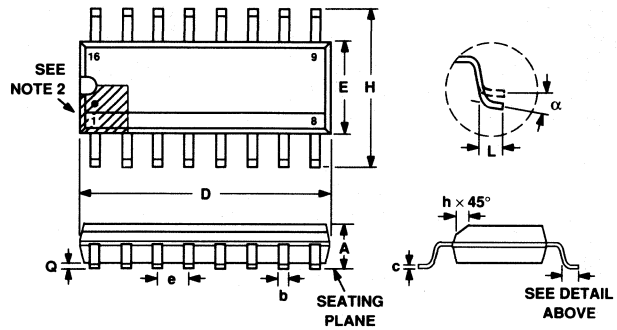
NOTES

1. Package dimensions conform to JEDEC specification MS-012-AB (Issue A, June 1985).
2. Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.

8

R-16A
SO-16

16-Lead Narrow Body SO
(S Suffix)



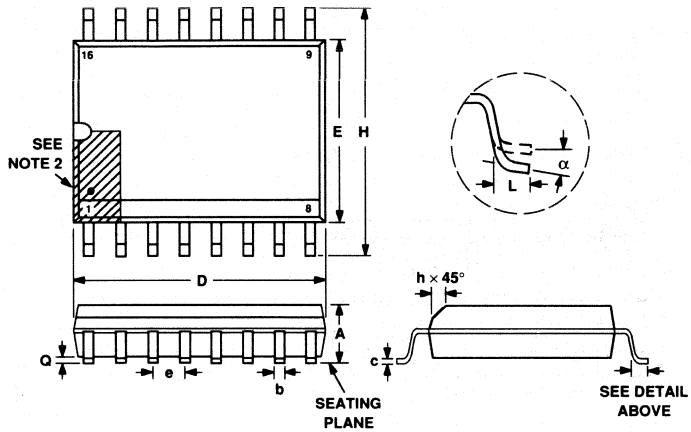
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	
b	0.0138	0.0192	0.35	0.49	
c	0.0075	0.0099	0.19	0.25	
D	0.3859	0.3937	9.80	10.00	
E	0.1497	0.1574	3.80	4.00	
H	0.2284	0.2440	5.80	6.20	
e	0.0500 BSC		1.27 BSC		
h	0.0099	0.0196	0.25	0.50	
L	0.0160	0.0500	0.41	1.27	
Q	0.0040	0.0098	0.10	0.25	
α	0°	8°	0°	8°	

NOTES

1. **Package dimensions conform to JEDEC specification MS-012-AC (Issue A, June 1985).**
2. **Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.**

R-16
SOL-16

16-Lead Wide Body SO
(S Suffix)



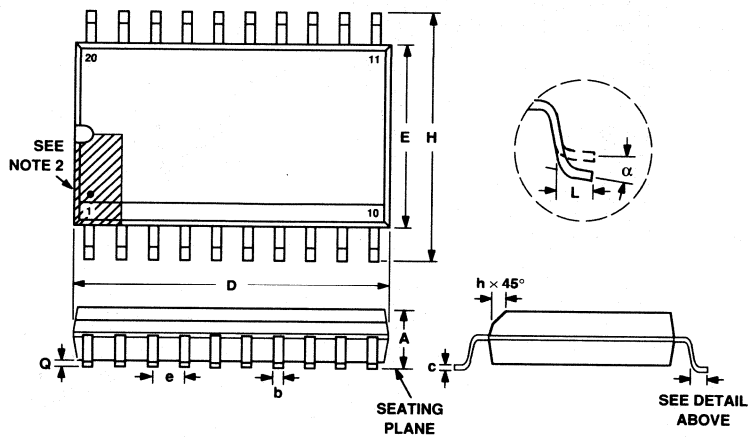
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	
b	0.0138	0.0192	0.35	0.49	
c	0.0091	0.0125	0.23	0.32	
D	0.3977	0.4133	10.10	10.50	
E	0.2914	0.2992	7.40	7.60	
H	0.3937	0.4193	10.00	10.65	
e	0.0500 BSC		1.27 BSC		
h	0.0098	0.0291	0.25	0.74	
L	0.0157	0.0500	0.40	1.27	
Q	0.0040	0.0118	0.10	0.30	
α	0°	8°	0°	8°	

NOTES

1. Package dimensions conform to JEDEC specification MS-013-AA (Issue A, June 1985).
2. Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.

8

R-20
SOL-20
20-Lead Wide-Body SO
(S Suffix)

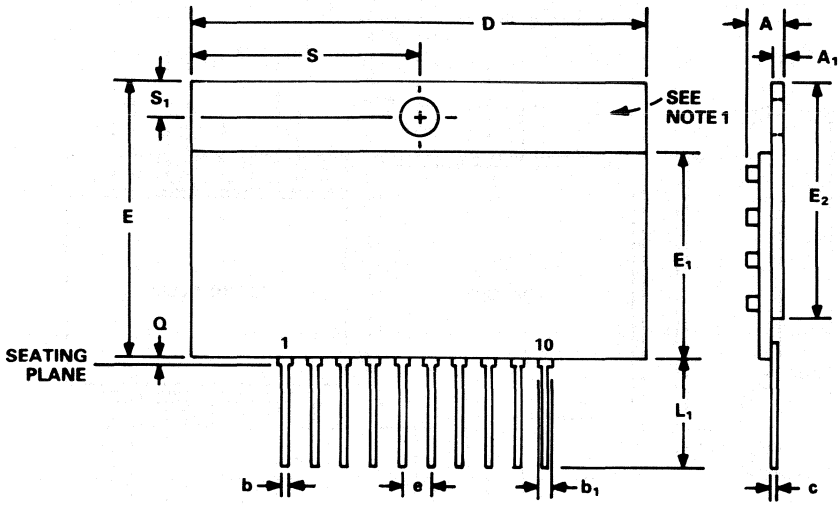


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	
b	0.0138	0.0192	0.35	0.49	
c	0.0091	0.0125	0.23	0.32	
D	0.4961	0.5118	12.60	13.00	
E	0.2914	0.2992	7.40	7.60	
H	0.3937	0.4193	10.00	10.65	
e	0.0500 BSC		1.27 BSC		
h	0.0098	0.0291	0.25	0.74	
L	0.0157	0.0500	0.40	1.27	
Q	0.0040	0.0118	0.10	0.30	
α	0°	8°	0°	8°	

NOTES

1. **Package dimensions conform to JEDEC specification MS-013-AC (Issue A, June 1985).**
2. **Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.**

Y-10
10-Lead Single In-Line Package (SIP)



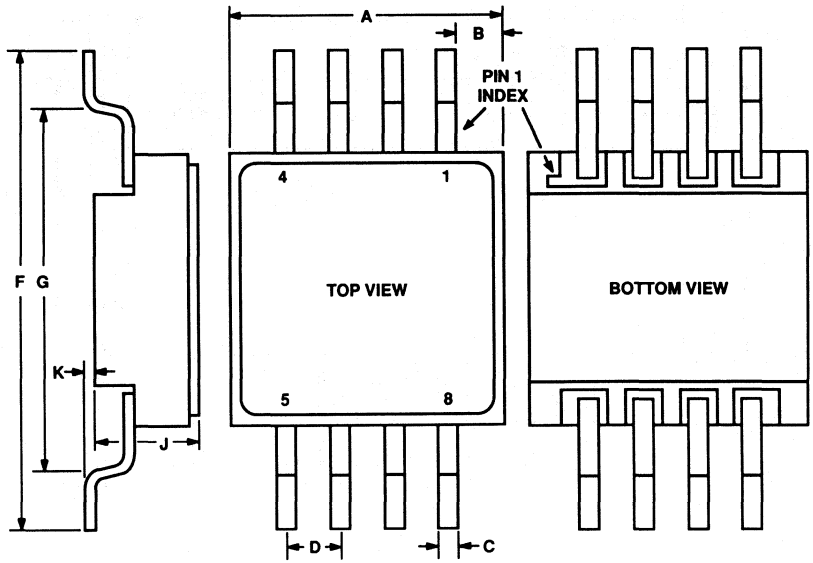
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.123	0.150	3.12	3.81
A_1	0.038	0.042	0.97	1.07
b	0.016	0.020	0.41	0.51
b_1	0.040	0.070	1.02	1.78
c	0.009	0.012	0.23	0.31
D	1.566	1.586	39.78	40.28
E	0.990	1.050	25.15	26.67
E_1	0.750 REF		19.05 REF	
E_2	0.810 REF		20.57 REF	
e	0.100 BSC		2.54 BSC	
L_1	0.150	0.350	3.81	8.89
Q	0.060	0.080	1.52	2.03
S	0.780 REF		19.51 REF	
S_1	0.115 REF		2.92 REF	

NOTE
1. Metal tab is electrically insulated from circuitry.

8

Z-8

8-Lead Leaded Chip Carrier (Gull Wing)



	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.250	0.260	6.35	6.61
B	0.028	0.049	0.711	1.25
C	0.015	0.019	0.38	0.48
D	0.045	0.055	1.14	1.40
F	0.433	0.457	10.90	11.60
G	0.323	0.347	8.20	8.81
J	0.083	0.103	23.37	23.87
K	0.015		0.381	

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Substitution Guide for Product Families No Longer Available 9–5
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Ordering Guide

INTRODUCTION

This Ordering Guide should make it easy to order Analog Devices products, whether you're buying one IC op amp, a multi-option subsystem, or 1000 each of 15 different items. It will help you:

1. Find the correct part number for the options you want.
2. Get a price quotation and place an order with us.
3. Know our warranty for components and subsystems.

For answers to further questions, call the nearest sales office (listed at the back of the book) or our main office in Norwood, Mass. U.S.A. (617-329-4700).

MODEL NUMBERING

In this reference manual many of the data sheets for products having a number of standard options contain an Ordering Guide. Use it to specify the correct part number for the exact combination of options you want. Two model numbering schemes are used by Analog Devices. The first model numbering scheme is used for designating standard Analog Devices monolithic and hybrid products. The second scheme is used by our Precision Monolithics Division (formerly PMI) as designators for its product line.

Figure 1 shows the form of model number used for our proprietary standard monolithic ICs and many of our hybrids. It consists of an "AD" (Analog Devices) prefix, a 3-to-5-digit number,* an alphabetic performance/temperature-range designator and a package designator. One or two additional letters may immediately follow the digits ("A" for second-generation redesigned ICs, "DI" for dielectrically isolated CMOS switches, e.g., AD536AJH, AD7512DIKD).

Figure 2 shows a different numbering scheme used by our Precision Monolithics Division. This numbering scheme starts with a prefix which designates the device type and model number. It is then followed by a suffix consisting of alphabetic designators (as applicable) to indicate additional functional designations or options and packaging options.

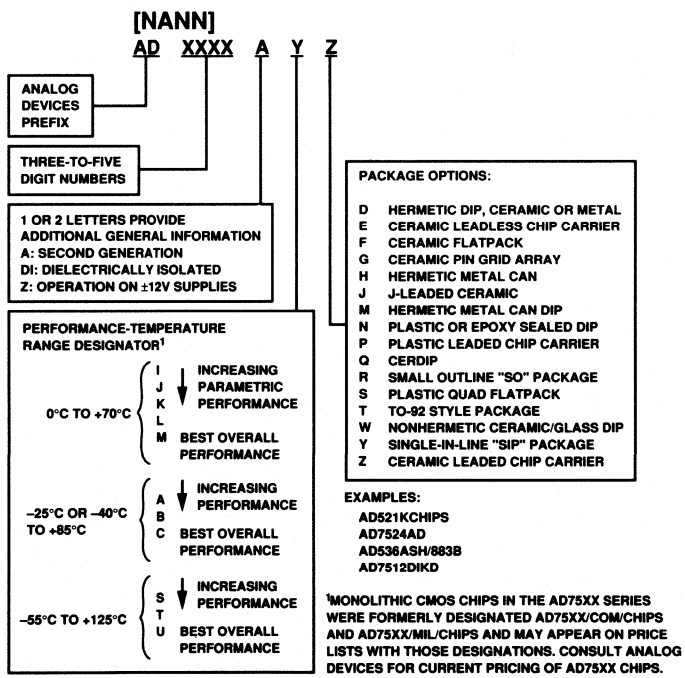

Figure 1. Model-Number Designations for Standard Analog Devices Monolithic and Hybrid IC Products. S, T and U Grades have the Added Suffix, /883B for Devices that Qualify to the Latest Revision of MIL-STD-883, Level B.

***For some models, the combination [digit][letter] [two or three digits] is used instead of ADXXXX, e.g., 2S80.**

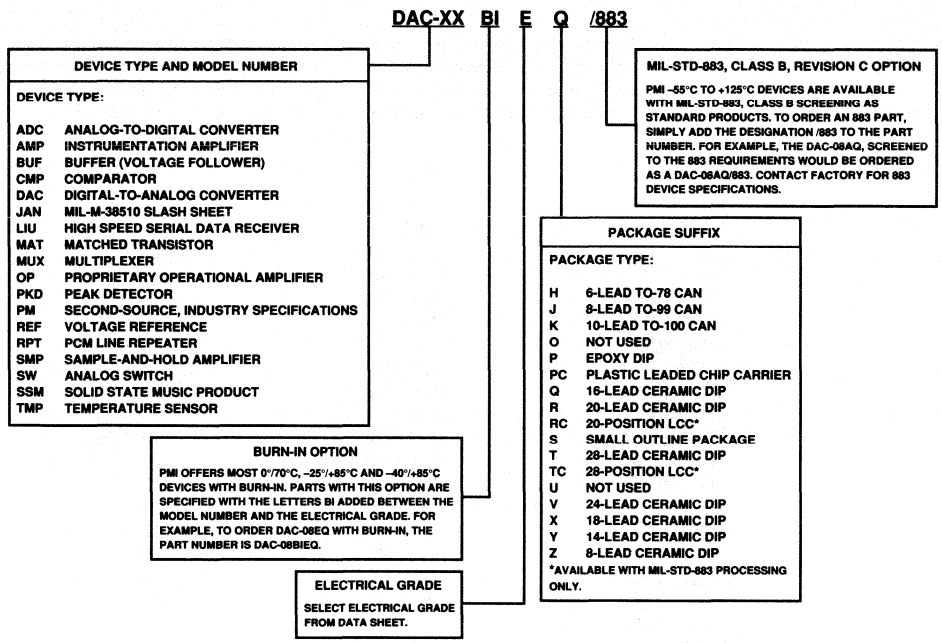

Figure 2. Precision Monolithics Division's Product Designations

ORDERING FROM ANALOG DEVICES

When placing an order, please provide specific information regarding model type, number, option designations, quantity, ship-to and bill-to address. Prices quoted are list; they do not include applicable taxes, customs, or shipping charges. All shipments are F.O.B. factory. Please specify if air shipment is required.

Place your orders with our local sales office or representative, or directly with our customer service group located in the Norwood facility. Orders and requests for quotations may be telephoned, sent via fax or telex, or mailed. Orders will be acknowledged when received; billing and delivery information is included.

Payments for new accounts, where open-account credit has not yet been established, will be C.O.D. or prepaid. Analog Devices' minimum order value is two hundred fifty dollars ($250.00).

When prepaid, orders should include $2.50 additional for packaging and postage (and a 5% sales tax on the price of the goods if you are ordering for delivery to a destination in Massachusetts).

You may also order Analog Devices parts through distributors. For information on distributors, please see pages 9–12 and 9–13 at the back of this volume.

WARRANTY AND REPAIR CHARGE POLICIES

All Analog Devices, Inc., products are warranted against defects in workmanship and materials under normal use and service for one year from the date of their shipment by Analog Devices, Inc., except that components obtained from others are warranted only to the extent of the original manufacturers' warranties, if any, except for component test systems, which have a 180-day warranty, and μMAC and MACSYM systems, which have a 90-day warranty. This warranty does not extend to any products which have been subjected to misuse, neglect, accident, or improper installation or application, or which have been repaired or altered by others. Analog Devices' sole liability and the Purchaser's sole remedy under this warranty is limited to repairing or replacing defective products. (The repair or replacement of defective products does not extend the warranty period. This warranty does not apply to components which are normally consumed in operation or which have a normal life inherently shorter than one year.) Analog Devices, Inc., shall not be liable for consequential damages under any circumstances.

THE FOREGOING WARRANTY AND REMEDY ARE IN LIEU OF ALL OTHER REMEDIES AND ALL OTHER WARRANTIES, WRITTEN OR ORAL, STATUTORY, EXPRESS, OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

Product Families Not Included in the Reference Manual (But Still Available)

The information published in this Reference Manual is intended to assist the user in choosing components for the design of *new* equipment, using the most cost-effective products available from Analog Devices. The popular product types listed below may have been designed into your circuits in the past, but they are no longer likely to be the most economic choice for your new designs. Nevertheless, we recognize that it is often a wise choice to refrain from redesigning proven equipment, and we are continuing to make these products available for use in existing designs. Data sheets on these products are available upon request.

Model	Model	Model	Model
AD101	ADC-912	DAC1138	SW-01/02
AD201	ADC1130	DAC1146	SW-7510/7511
AD301	ADC1131	DAC-1408A	2B24
AD301AL	ADC1143	DAC1508A	2B34
AD363R	AD DAC-08	DAC-8212	2B52
AD364R	AD DAC71	DAS1153	2B53
AD503	AD DAC72	DAS1157	2B56
AD504	ADEB770	HDS-1240E	2B57
AD506	ADSP-1008A	HDS-1250	2B58
AD507SH/883B	ADSP-1009A	HOS-050/050A/050C	2B59
AD510	ADSP-1010A	HOS-060	4B Series
AD515	ADSP-1010B	HTC-0300A	40
AD518	ADSP-1012A	HTS-0010	171
AD533	ADSP-1016A	HTS-0025	233
AD535	ADSP-1024A	JM38510/11301/11302	277
AD545	ADSP-1080A	MUX-88	285
AD567	ADSP-1081A	OP-08	290
AD611	ADSP-1101	OP-43	292
AD651	ADSP-1110A	OP-44	310
AD689	ADSP-1401	OP-65	426
AD757	ADSP-1402	OP-111	429
AD1175	ADSP-1410	OP-147	434
AD1322	ADSP-3128A	OP-150	436
AD1403	ADSP-3201	OP-166	442
AD2004	ADSP-3202	PM-119	451
AD2006	ADSP-3210	PM-219	453
AD2020	ADSP-3211	PM-148/248	460
AD5200 Series	ADSP-3212	PM-155	741A
AD5210 Series	ADSP-3220	PM-156	751
AD7110	ADSP-3221	PM-157	756
AD7240	ADSP-3222	PM-355	947
AD7520	CAV-1210	PM-356	950
AD7521	CMP-08	PM-562	968
AD7522	CMP-404	PM-725	
AD7523	DAC-01	PM-741	
AD7525	DAC-02/03	PM-0820	
AD7530	DAC-05/06	PM-7541	
AD7531	DAC-12QS	PM-7574	
AD7541	DAC-20	SHA-1144	
AD7546	DAC71/72	SMP-81	
AD7576	DAC-86	SSM-2044	
AD7772	DAC-88	SSM-2045	
AD9502	DAC-89	SSM-2047	
AD9611	DAC-210	SSM-2100	
AD9686	DAC-888	SSM-2132	
ADC-908	DAC1136	SSM-2300	

Substitution Guide for Product Families No Longer Available

The products listed in the left-hand column are no longer available from Analog Devices. In many cases, comparable functions and performance may be obtained with newer models, but—as a rule—they are not directly interchangeable. The closest recommended Analog Devices equivalent, physically and electrically, is listed in the right-hand column. If no equivalent is listed, or for further information, contact your local sales office.

Model	Closest Recommended Equivalent	Model	Closest Recommended Equivalent	Model	Closest Recommended Equivalent
AD108/208/308	AD705	AD2008	None	ADC-14I/17I	AD1170
AD108A/208A/308A	AD705	AD2009	None	ADC1100	AD1170
AD111/211/311	AD790	AD2016	None	ADC1102	AD7870
AD246	AD204/AD208	AD2022	None	ADC1103	AD7572A
AD295	AD210	AD2023	None	ADC1105	AD7550/AD7552
AD293	AD210	AD2024	None	ADC1109	AD7572A
AD294	AD210	AD2025	None	ADC1111	AD574A
AD345	AD1321/1324	AD2027	None	ADC1121	AD7880
AD351	AD790	AD2028	None	ADC1123	AD7880
AD362	AD1362	AD2033	None	ADC1133	AD574A
AD367	None	AD2036	None	ADC-QU	AD574A/AD674A
AD368	None	AD2037	None	AD DAC100	AD561
AD369	None	AD2038	None	ADG200	None
AD370/371	AD767	AD2040	None	ADG201	ADG201A
AD376	AD1376	AD2050	None	ADLH0032G/CG	AD843
AD381	AD744	AD2051	None	ADLH0033G/CG	AD9620/AD9630
AD382	AD744/AD845	AD2060	None	ADM501	None
AD386	AD1154	AD2061	None	ADP501	None
AD392	AD664	AD2070	None	ADREF01	REF-01
AD501	AD711	AD2071	None	ADREF02	REF-02
AD502	AD711	AD3554	None	ADSHC-85	AD585
AD505	AD509	AD3860	AD567	ADSHM-5	HTC-0300A
AD506SH/883B	AD42626	AD5010/6020	AD9000	AMP-01BX	AMP-01AX
AD508	AD517	AD5240	AD ADC85	AMP-01BX/883C	AMP-01AX/883C
AD511	AD711	AD6012	AD565A	AMP-05BX	AMP-05AX
AD512	AD711	AD7115	AD7111	AMP-05BX/883C	AMP-05Z/883C
AD513	AD711	AD7513	ADG201A	API1620/1718	Consult ADI
AD514	AD711	AD7516	AD7510DI	BDM 1615/16/17	None
AD516	AD711	AD7519	None	BUF-03BJ/883C	BUF-03AJ/883C
AD520	AD524	AD7527	AD7548	CAV-0920/1020	AD9020/9060
AD523	AD549	AD7544	AD7548	CAV-1202	AD9007
AD528	AD711/744	AD7550	None	CAV-1205	AD9007
AD530	AD533	AD7552	None	CMP-01Z	CMP-01J
AD531	AD532	AD7555	AD1175K	CMP-05BJ	CMP-05CJ
AD540	AD544	AD7560	None	CMP-05BZ	CMP-05CZ
AD559	AD557/AD558	AD7570	AD7579/AD7580	CMP-05GJ	CMP-05CJ
AD565	AD565A	AD7571	AD7579/AD7580	CMP-404BY	CMP-404AY
AD566	AD566A	AD7583	AD7880+MUX	CMP-404BY/883C	CMP-404AY/883C
AD612	AD524	AD9011	AD9002	DAC-02ACX1	DAC-02CCX1
AD614	AD524	AD9521	AD640	DAC-05AX1	DAC-02CCX1
AD801	AD711	AD9615	AD9611/AD9617	DAC-05EX1	DAC-02CCX1
AD1145	AD7846	AD9685	AD96685	DAC-10BX	DAC-10FX
AD1147/48	AD669	AD9687	AD96686	DAC-10CX	DAC-10GX
AD1332	None	AD9688	AD9002/AD9028	DAC-10DF	AD568
AD1408	AD558	AD ADC-816	AD7820/AD7821	DAC-10H	None
AD1508	AD558	ADC-8S	AD673	DAC-10Z	None
AD1678	AD678	ADC-10Z	AD574A	DAC-12QZ	AD667
AD1679	AD679	ADC-12QL	AD7578	DAC-12M	AD7845
AD1779	AD779	ADC-12QM	AD574A/AD674A	DAC-14QM	DAC1136
AD2003	AD2021	ADC-12QZ	AD574A/AD674A	DAC-16QM	DAC1136

Model	Closest Recommended Equivalent	Model	Closest Recommended Equivalent	Model	Closest Recommended Equivalent
DAC-100AAQ7	DAC-100ACQ7	HOS-100AH/SH	None	OP-12CZ	OP-12AZ
DAC-100AAQ8	DAC-100ACQ8	HOS-200	AD9620/30	OP-12GZ	OP-12FZ
DAC-100ABQ7	DAC-100ACQ7	HTC-0300	HTC-0300A	OP-14DZ	OP-14CZ
DAC-100ABQ8	DAC-100ACQ8	HTC-0500	HTC-0300A	OP-14GRBC	OP-14GBC
DAC-100BBQ5/883C	DAC-100ACQ5/883C	IPA-1751	IPA-1764	OP-14J/883C	OP-14AJ/883C
DAC-100BCQ7	DAC-100BBQ7	IRDC1730-33	AD2S80A/82A	OP-15BJ	OP-15AJ
DAC-100DDQ7	DAC-100CCQ7	MAH-0801	AD9005	OP-15BZ	OP-15AZ
DAC-312BR	DAC-312ER	MAH-1001	AD9005	OP-16BJ	OP-16AJ
DAC-888AX	DAC-888EX	MAS-0801	AD9005	OP-17BZ/883C	OP-17AZ/883C
DAC-888BX	DAC-888EX	MAS-1001	AD9005	OP-17CJ	OP-17AJ
DAC1009	AD767	MAS-1202	AD9005	OP-17FJ	OP-17EJ
DAC1106	AD568	MAT-01/883C	MAT-01AH/883C	OP-17FZ	OP-17EZ
DAC1108	AD568	MAT-02BH	MAT-02AH	OP-20CJ	OP-20BJ
DAC1112	DAC12QS	MAT-02BH/883C	MAT-02AH/883C	OP-21GRBC	OP-21GBC
DAC1118	AD767	MATV-0811	AD9012/48	OP-215BJ	OP-215AJ
DAC1122	AD7541A	MATV-0816	AD9012/48	OP-215BJ/883C	OP-215AJ/883C
DAC1125	AD7533	MATV-0820	AD9012/48	OP-215BZ	OP-215AZ
DAC1132	AD667	MCI-1794	AD2S80A/82A	OP-215CZ/883C	OP-215BZ/883
DAC-1408-6P	DAC-1408-8P	MDA Family	AD9712B/13B	OP-21BJ	OP-21AJ
DAC-1408-7P	DAC-1408-8P	MDH Family	AD9712B/13B	OP-21BZ	OP-21AZ
DAC-1408-7Q	DAC-1408-8Q	MDMS Family	AD9712B/13B	OP-21EJ	OP-21AJ
DAC-1408-GQ	DAC-1408-8Q	MDS Family	AD9712B/13B	OP-220BJ	OP-220AJ
DAC1420	None	MDSL Family	AD9712B/13B	OP-22AJ	OP-22AJ/883C
DAC1422	None	MOD-1005/20	AD9020/60	OP-22EJ	OP-22AJ/883C
DAC1423	None	MUX-08AQ	MUX-08BQ	OP-32BZ	OP-32AZ
DAC1508A-8Q	DAC-1408-8Q	MUX-24AQ	MUX-24EQ	OP-32BZ/883C	OP-32AZ/883C
DAS1128	AD1341	MUX-24BQ	MUX-24FQ	OP-32FZ	OP-32EZ
DAS1150	None	MUX-16AT	MUX-16ET	OP-50BY	OP-50AY
DAS1151	None	MUX-16BT	MUX-16FT	OP-50BY/883C	OP-50AY/883C
DAS1155	None	OP-01HJ	OP-01J	OSC-1754	OSC-1758
DAS1156	None	OP-01HZ	OP-01HP	PKD-01BY	PKD-01AY
DRC1605/06	Consult ADI	OP-02BJ	OP-02AJ	PKD-01BY/883C	PKD-01AY/883C
DRC1705/1706	Consult ADI	OP-02BJ/883C	OP-02AJ/883C	PM-111Y	PM-111J
DRC1765/66	AD2S65/66	OP-02EJ	OP-07DJ	PM-11Y/883C	PM-111J/883C
DSC1605/06	Consult ADI	OP-02EP	OP-177GP	PM-139AY	PM-139AY/883C
DSC1705/1706	Consult ADI	OP-02EZ	OP-177GZ	PM-156AZ	PM-156AZ/883C
DSC1765/66	AD2S65/66	OP-02J	OP-02AJ	PM-157J	PM-175J/883C
DTM1716/17	AD2S65/66	OP-02/883C	OP-02AZ/883C	PM-157J/883C	PM-157AJ/883C
HAS-0802	HAS1202A	OP-04DY	OP-04CY	PM-208AJ	PM-108AJ/883C
HAS-1002	HAS1202A	OP-04GBC	OP-04NBC	PM-208AZ	PM-108AZ
HAS-1202	HAS1202A	OP-04Y/883C	OP-04AY/883C	PM-308AZ	PM-1008GZ
HDD-1015	AD9712A	OP-05Z	OP-05AZ	PM-308J	PM-1008G
HDD-1409	None	OP-05/883C	OP-05AZ/883C	PM-4136RC	OP-11ARC/883C
HDG-0805	AD9701	OP-06BJ/883C	OP-06AJ/883C	PM-562AV	PM-562HV
HDH-0802	AD9713B	OP-06EZ	OP-06GZ	PM-562BV	PM-562HV
HDH-1003	AD9713B	OP-06FZ	OP-06GZ	PM-562FV	PM-562HV
HDH-1205	AD9713B	OP-08AJ	PM-1008AJ	PM-562GV	PM-562HV
HDL-3805	ADV453/ADV478	OP-08AJ/883C	PM-1008AJ/883C	PM-741J	OP-02AJ
HDL-3806	ADV453/ADV478	OP-08AZ/883C	PM-1008AZ/883C	RAC1763	None
HDM-1210	AD668/AD9713B	OP-08CZ/883C	PM-1008AZ/883C	RDC1602/03	RDC1702/03
HDS-0810E	AD9712B	OP-08EJ	PM-1008EJ	RDC1700	Consult ADI
HDS-0820	AD9713B	OP-08EZ	PM-1008EZ	RDC1702	Consult ADI
HDS-1015E	AD9712B	OP-09ARC/883C	OP-11ARC/883C	RDC1704	Consult ADI
HDS-1025	AD9713B	OP-09FY	OP-09EY	RDC1711	None
		OP-12BZ	OP-12AZ	RDC1721	AD2S46

Model	Closest Recommended Equivalent
RDC1725	Consult ADI
RDC1726	Consult ADI
RDC1728	Consult ADI
RDC1767	Consult ADI
RDC1768	Consult ADI
RSCT1621	AD2S80A/82A
RTI-1200	RTI-711 Series
RTI-1201	RTI-711 Series
RTI-1202	RTI-711 Series
RTM Series	Consult ADI
SAC1763	None
SBCD1752/53/56/57	None
SCDX1623	None
SCM1677	None
SDC1602/3/4	Consult ADI
SDC1700	Consult ADI
SDC1702	Consult ADI
SDC1703	Consult ADI
SDC1704	Consult ADI
SDC1711	None
SDC1721	AD2S46
SDC1725	Consult ADI
SDC1726	Consult ADI
SDC1728	Consult ADI
SDC1767	Consult ADI
SDC1768	Consult ADI
SERDEX	μMAC-5000
SHA-1A	AD585
SHA-2A	AD781
SHA-3	AD585
SHA-4	AD585
SHA-5	None
SHA-6	AD1154
SHA1114	AD585
SHA-1134	None
SMP-10BY	SMP-10AY
SMP-10BY/883C	SMP-10AY/883C
SPA-1695	None
SSCT1621	AD2S80A/82A
SSCT1622/23	None
STM Series	Consult ADI
SW-01BQ	SW-01FQ
SW-7510AQ	SW-7510EQ
SW-7510BQ	SW-7510FQ
SW-7511AQ	SW-1577BQ
THC-Family	HTC-0300A
THS-Family	HTC-0300A
TSL1612	Consult ADI
1S10/20	AD2S80A/82A
1S14/24/44/64/74	AD2S83
1S60/61	AD2S80A/82A

Model	Closest Recommended Equivalent
2B35	None
2S20	AD2S80A/82A
5S70/5S72	AD2S75
9S70/71/72	None
9S75/76/79	None
41	AD515A
42	AD549
43	AD549
44	AD845
45	AD744
46	AD844
47	AD845
48	AD845
50	AD844
51	AD844
52	AD707
102	AD845
106	AD711
107	AD711
108	AD845
110	AD845
118	AD711
120	AD844
141	40
142	AD845
143	AD845
146	AD382
148	AD549
149	AD844
153	AD517
161	None
163	None
165	None
170	None
180	AD OP-07
183	AD707
184	AD707
220	233
230	233
231	233
232	233
234	233
235	233
260	AD707
261	OP-177
272	None
273	None
274J	284J
275	AD210
276	None
279	286J

Model	Closest Recommended Equivalent
280	281
282J	292A
283J	292A
287	None
288	AD210
301	310 (Module)
302	310 (Module)
311	AD549
350	None
424	AD534
427	None
428	AD538
432	None
433	434
435	AD734
440	442
450	AD652
452	None
454	AD537
456	AD537
458	460
602J10	AD524
602J100	AD524
602K100	AD524
603	AD524
605	AD524
606	AD625
610	AD625
752	759
901	904
903	905
906	905
907	921
908	921
909	921
915	904
926	927
931	None
932	None
933	None
935	None
942	None
944	None
946	None
948	947
951	None
952	970
956	None
959	960
971	921
972	974
973	975

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DATA CONVERTER REFERENCE MANUAL—1992: Volumes 1 and 2. Data sheets and selection guides on A/D and D/A Converters, V/F and F/V Converters, Synchro/Resolver-to-Digital Converters, Sample/Track-Hold Amplifiers, Switches and Multiplexers, Voltage References, Data-Acquisition Subsystems, Analog I/O Ports, Communications Products, Bus Interface and I/O Products, Application-Specific ICs, Digital Panel Meters, Power Supplies. (Available FREE)

AUDIO/VIDEO REFERENCE MANUAL—1992. Data sheets and selection guides on Operational Amplifiers, Audio A/D and D/A Converters, Video A/D and D/A Converters, Special Function Audio Products, Special Function Video Products, and Digital Signal Processing Products, plus 42 Application Notes.

MILITARY PRODUCTS DATABOOK—1990 (in two volumes). Information and data on products available with processing in accordance with MIL-STD-883.

Volume 2: PMI Division products—including Class S
Volume 1: All other Analog Devices products

DATA-ACQUISITION AND CONTROL CATALOG—1990. Tutorial and Configuration Guide, with Product Reference and Index. Bus-Compatible I/O Boards for: IBM PS/2,* IBM PC/XT/ AT,* STD Bus, VMEbus, MULTIBUS.† Distributed I/O Subsystems—fixed-function front ends, programmable units, and distributed control systems. Modular Signal Conditioners—analog and digitizing. Analog Signal-Conditioning Panels—isolated and nonisolated. Digital Subsystems—16- and 24/32-channel. Software—DOS drivers and applications packages.

POWER SUPPLIES‡–Linear Supplies•DC-DC Converters. 12-page Short-Form Catalog listing AC/DC Power Supplies, Modular DC/DC Converters, Power-Supply Test Procedures, Transients, Thermal Derating, Mechanical Outlines of Packages and Sockets.

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1992 Short Form Designers' Guide. A 142-page summary of Analog Devices products, including data converters, amplifiers, transducers, audio/video components, voltage references, switches and multiplexers, data-acquisition subsystems—and components for analog and digital signal processing, audio/video, disk drives, automotive electronics, ATE, and communications. It features new-product descriptions, specifications, and block diagrams—and provides selection guides, selection trees, and characteristics tables, plus a comprehensive index to all products.

Analog CMOS Switches and Multiplexers. A 16-page short form guide to high-speed CMOS switches, CMOS switches with dielectric isolation and CMOS multiplexers. Also included are reliability data and information on single-supply operation.

Applications Guide for Isolation Amplifiers and Signal Conditioners. A 20-page guide to specifications and applications of galvanically isolated amplifiers and signal conditioners for industrial, instrumentation and medical applications.

CMOS DAC Application Guide 3rd Edition by Phil Burton (1989—64 pages). Introduction to CMOS DACs, Inside CMOS DACs, Basic Application Circuits in Current-Steering Mode, Single-Supply Operation Using Voltage-Switching Mode, The Logic Interface, Applications.

Digital Signal Processing—a 20-page brochure outlining the Analog Devices approach to DSP, mixed-signal processing and signal computing. Includes philosophies, fixed- and floating-point architectures, products, benchmarks, applications, tools (hardware, software, and third-party), support—and migration paths to the future.

ESD Prevention Manual—Protecting ICs from electrostatic discharges. Thirty pages of information that will assist the reader in implementing an appropriate and effective program to ensure protection against electrostatic discharge (ESD) failures.

High-Speed Data Conversion. A 24-page short-form guide to video and other high-speed A/D and D/A converters and accessories, in forms ranging from monolithic ICs to card-level products.

High-Speed Op Amp Selection Guide. A 4-page quick-reference chart outlining specs and characteristics of high-speed op amps, further subdivided into precision, low-noise, FET-input, transimpedance, general-purpose and buffer classifications. Includes a worldwide sales directory.

Instrumentation Amplifier Application Guide, by Charles Kitchin and Lew Counts. Its 44 pages include basic instrumentation-amplifier ("in-amp") theory, design considerations, applications, specifications, and products—plus a brief bibliography and two indexes (by topic and by device model number).

Multiple Digital-to-Analog Converter Integrated Circuits Selection Guide. A 32-page guide for the designer who wants to save space and cost in applications calling for from two to eight or more DACs and resolutions from 6 to 18 bits. Devices include triple 6-, 8-, and 10-bit video DACs, dual 18-bit audio DACs, 8-bit octuples, and 12- and 14-bit quads.

Resolver-to-Digital Converter Selection Chart. A 40-page collection of accuracy and speed data for use in the design of systems combining Analog Devices monolithic integrated-circuit RDCs with a variety of resolvers. Topics include single- and multi-speed resolvers, speed-accuracy charts, resolver charts for nine different manufacturers, and definitions of terms.

RMS-to-DC Conversion Application Guide 2nd Edition by C. Kitchin and L. Counts (1986—61 pages). RMS-DC Conversion: Theory, Basic Design Considerations; RMS Application Circuits; Testing Critical Parameters; Input Buffer Amplifier Requirements; Programs for Computing Errors, Ripple and Settling Time.

Sampling Analog-to-Digital Converter Integrated Circuits—1992 Short-Form Selection Guide. Its 28 pages cover 35 different models with resolutions from 8 to 16 bits, and 12-bit resolution up to 20 MSPS. Besides block diagrams and key specs of each product, the booklet includes a detailed discussion of selection issues and a selection table sorted by resolution and speed.

Signal Computing. A 16-page brochure describing the present and future of product designs that require synchronous, real-time execution of complex mathematical signal-processing algorithms. In it, chipsets (e.g., a DSP teamed with appropriate analog ports) provide the hardware platform; and prepackaged third-party software, written by experts in a variety of fields (but modified to meet the needs of individual designs) provides the problem-solving configuration. So (for example) the same processor can be used as a PC-based sound coprocessor, or an embedded audio processor in digital TVs, or a host processor in digital cellular telephones. Some illustrations are provided, using Analog Devices products.

*Surface Mount IC.** A 28-page guide to ICs in SO and PLCC packages. Products include op amps, rms-to-dc converters, DACs, ADCs, VFCs, sample-holds and CMOS switches.

DIGITAL SIGNAL PROCESSING MANUALS

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ADSP-2101/ADSP-2102 USER'S MANUAL—Architecture. [Fixed-point processor] Introduction; Computational Units; Data Moves, Program Control; Timer; Serial Ports; System Interface; Memory Interface; Instruction Set Overview; Appendixes; Index. 190 pages.

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ADSP-2111 USER'S MANUAL—Architecture. [Fixed-point processor] Introduction; Computational Units; Data Moves; Program Control; Timer; Host Interface Port; Serial Ports; System Interface; Memory Interface; Instruction Set Overview; Appendixes; Index. 218 pages.

ADSP-21020 USER'S MANUAL. [Floating-point processor] Introduction; Computational Units; Program Sequencing; Data Addressing; Timer; Memory Interface; Instruction Summary; Assembly Programmer's Tutorial; Hardware System Configuration; Appendixes; Index. 394 pages.

TECHNICAL REFERENCE BOOKS

Can be purchased from Analog Devices, Inc., at the prices shown. If more than one book is ordered, deduct a discount of $1.00 from the price of each book. Price of the entire set of 10 books is $177.00—a bargain for your department's library (in effect, the Amplifier Applications and High-Speed books come free). VISA and MasterCard are welcome; phone (617) 461-3392 or fax (617) 821-4273. Or send your check for the indicated amount to Analog Devices, Inc., P.O. Box 9106, Norwood, MA 02062-9106.

NEW—*AMPLIFIER APPLICATIONS GUIDE*, by the Applications Engineering Staff of Analog Devices and edited by Walt Kester, published by Analog Devices (1992). 648 pages of timely and practical information on amplifiers—including operational, audio, instrumentation, video, and log amps. Topics include: Introduction; Precision transducer interfaces; High-impedance, low current; Single-supply, low-power; Audio; Filtering, Driving ADCs; Video and other high-speed applications; Nonlinear circuit applications; Unusual applications; Subtleties; Hardware techniques; Simulation; and a complete Index. $20.00

ANALOG-DIGITAL CONVERSION HANDBOOK: Third Edition, by the Engineering Staff of Analog Devices, edited by Daniel H. Sheingold. Englewood Cliffs, NJ: Prentice Hall (1986). A comprehensive guide to A/D and D/A converters and their applications. This third edition of our classic is in hardcover and has more than 700 pages, an Index, a Bibliography, and much new material, including: video-speed, synchro-resolver, V/F, high-resolution, and logarithmic converters, ICs for DSP, and a "Guide for the Troubled." Seven of its 22 chapters are totally new. $32.95

DIGITAL SIGNAL-PROCESSING APPLICATIONS USING THE ADSP-2100 FAMILY, by the Applications Staff of Analog Devices, DSP Division; edited by Amy Mar (628 pages). Englewood Cliffs NJ: Prentice Hall (1990). Bridge the gap between DSP algorithms and their real-world implementation on state-of-the-art signal processors. Each chapter tackles a specific application topic, briefly describing the algorithm and discussing its implementation on the ADSP-2100 family of DSP chips. Comprehensive source-code listings are complete with comments and accompanied by explanatory text. Programs are listed on a pair of supplementary diskettes—furnished with the book. Application areas include fixed- and floating-point arithmetic, function approximation, digital filters, one- and two-dimensional FFTs, image processing, graphics, LP speech coding, PCM, ADPCM, high-speed modem algorithms, DTMF coding, sonar beamforming. Additional topics include memory interface, multiprocessing, and host interface. The book can serve as a companion to *Digital Signal Processing in VLSI*. **Now in paperback**; its price includes a diskette.

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DIGITAL SIGNAL PROCESSING IN VLSI, by Richard J. Higgins. Englewood Cliffs NJ: Prentice Hall (1990). An introductory 614-page guide for the engineer and scientist who needs to understand and use DSP algorithms and special-purpose DSP hardware ICs—and the software tools developed to carry them out efficiently. Real-World Signal Processing; Sampled Signals and Systems; The DFT and the FFT Algorithm; Digital Filters; The Bridge to VLSI; Real DSP Hardware; Software Development for the DSP System; DSP Applications; plus Bibliography and Index. $38.00

DIGITAL SIGNAL PROCESSING LABORATORY Using the ADSP-2101 Microcomputer, by Vinay K. Ingle and John G. Proakis (Northeastern University). Englewood Cliffs NJ: Prentice Hall (1991). Contents: Introduction to the ADSP-2100/2101 family; ADSP-2101 instruction set overview; Overview of development tools; Getting started with the ADSP-2101; Laboratory experiments using the ADSP-2101; FIR filter implementation; IIR filter implementation; Fast Fourier transform implementation; Applications in communications; Adaptive filters and their applications; References; Index. $24.00

HIGH-SPEED DESIGN SEMINAR, published by Analog Devices (1990). A 496-page guide to the practical application of high-speed semiconductor devices in processing of analog signals. Topics include: data conversion, digital video applications, high-speed sample-holds and operational amplifiers, nonlinear signal processors (including log amps), comparators and pin electronics, time-delay generators, phase-locked loops, direct digital synthesis, computer graphics and RAMDACs, and high-speed techniques. $20.00

MIXED-SIGNAL DESIGN SEMINAR, published by Analog Devices (1991). Contents: Introduction to mixed-signal processing of real-world signals and signal conditioning; Linear and nonlinear analog signal processing; Fundamentals of sampled-data systems; ADCs for DSP applications; DACs for DSP applications; Sigma-delta ADCs and DACs; Digital signal-processing techniques; DSP hardware; Interfacing ADCs and DACs to digital signal processors; Mixed-signal processing applications; Mixed-signal circuit techniques; Index. $22.00

NONLINEAR CIRCUITS HANDBOOK: Designing with Analog Function Modules and ICs, by the Engineering Staff of Analog Devices, edited by Daniel H. Sheingold. Norwood MA: Analog Devices, Inc. (1974). A 540-page guide to multiplying and dividing, squaring and rooting, rms-to-dc conversion, and multifunction devices. Principles, circuitry, performance, specifications, testing, and application of these devices–contains 325 illustrations. $5.95

SYNCHRO & RESOLVER CONVERSION, edited by Geoff Boyes. Norwood, MA; Analog Devices, Inc. (1980). Principles and practice of interfacing synchros, resolvers, and Inductosyns* to digital and analog circuitry. $11.50

TRANSDUCER INTERFACING HANDBOOK: A Guide to Analog Signal Conditioning, edited by Daniel H. Sheingold. Norwood MA: Analog Devices, Inc. (1980). A book for the electronic engineer who must interface transducers for temperature, pressure, force, level, or flow to electronics, these 260 pages tell how transducers work—as circuit elements—and how to connect them to electronic circuits for effective processing of their signals. $14.50

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AD364	C II
AD365	A 4–9
AD380	A 2–31
AD389	C II
AD390	C I
AD394	C I
AD395	C I
AD396	C I
AD503	D
AD504	D
AD506	D
AD507	A 2–37
AD509	A 2–41
AD510	D
AD515	D
AD515A	A 2–45
AD517	A 2–51
AD518	D
AD521	A 4–17
AD522	A 4–23
AD524	A 4–27
AD526	A 4–39
AD532	SL 2–9
AD533	D
AD534	SL 2–15
AD535	D
AD536A	SL 4–7
AD537	C II
AD538	SL 2–23
AD539	AV, SL 2–27
AD542	A 2–57
AD544	A 2–57
AD545	D
AD545A	A 2–65
AD546	A 2–69
AD547	A 2–57
AD548	A 2–81
AD549	A 2–89
AD557	C I
AD558	C I
AD561	C I
AD562	C I
AD563	C I
AD565A	C I
AD566A	C I
AD567	D
AD568	C I
AD569	C I
AD570	C II
AD571	C II
AD572	C II
AD573	C II
AD574A	C II
AD575	C II
AD578	C II
AD579	C II
AD580	C II
AD581	C II
AD582	C II

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Model	Page†
AD583	C II
AD584	C II
AD585	C II
AD586	C II
AD587	C II
AD588	C II
AD589	C II
AD590	SL 9–7
AD592	SL 9–17
AD594/595	SL 10–9
AD596/597	SL 10–17
AD598	SL 10–23
*AD600	AV, SL 3–7
*AD602	AV, SL 3–7
*AD606	SL 3–25
AD611	D
*AD620	A 4–51
*AD621	A 4–67
AD624	A 4–71
AD625	A 4–83
*AD626	A 4–95
AD630	SL 2–35
AD632	SL 2–43
*AD633	AV, SL 2–47
AD636	SL 4–15
AD637	SL 4–23
AD639	SL 7–5
AD640	SL 3–31
AD642	A 2–101
AD644	A 2–107
AD645	A 2–113
AD647	A 2–121
AD648	A 2–127
AD650	C II
AD651	D
AD652	C II
AD654	C II
*AD660	D
AD664	C I
AD667	C I
AD668	C I
*AD669	C I
AD670	C II
AD671	C II
AD673	C II
AD674A	C II
*AD674B	C II
*AD675	C II
*AD676	C II
*AD677	D
AD678	C II
AD679	C II

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*AD680	C II
*AD682	C II
AD684	C II
*AD688	C II
AD689	D
AD693	SL 10–39
AD694	SL 10–51
AD704	A 2–137
AD705	A 2–145
AD706	A 2–153
AD707	A 2–161
AD708	A 2–169
AD711	AV, A 2–177
AD712	AV, A 2–189
AD713	AV, A 2–201
*AD720	AV, SL 7–9
*AD730	SL 7–13
*AD734	AV, SL 2–55
AD736	SL 4–31
AD737	SL, 4–39
AD741	A 2–213
AD743	A 2–217
AD744	A 2–229
*AD745	A 2–241
AD746	A 2–253
*AD766	C I
AD767	C I
AD770	C II
*AD773	AV, C II
*AD774B	C II
*AD776	C II
AD779	C II
*AD781	C II
*AD783	C II
AD790	A 3–5
*AD795	A 2–261
*AD796	A 2–267
*AD797	A 2–271
*AD800	SL 7–19
*AD802	SL 7–19
*AD805	SL 7–23
*AD810	A 2–277
*AD811	AV, A 2–281
*AD817	A 2–295
*AD820	A 2–299
*AD822	A 2–299
AD827	AV, A 2–301
AD829	AV, A 2–309
*AD830	A 2–321
AD834	AV, SL 2–67
AD840	AV, A 2–327
AD841	AV, A 2–335

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Model	Page†
AD842	AV, A 2–343
AD843	AV, A 2–351
AD844	AV, A 2–363
AD845	AV, A 2–375
AD846	AV, A 2–383
AD847	AV, A 2–395
AD848	AV, A 2–407
AD849	AV, A 2–407
*AD880	SL 5–5
AD890	SL 5–7
AD891	SL 5–9
AD891A	SL 5–11
AD892	SL 5–13
*AD896	SL 5–15
*AD897	SL 5–27
*AD899	SL 5–29
AD1139	C I
AD1154	C II
AD1170	C II
AD1175	D
AD1315	SL 6–7
*AD1317	SL 6–15
*AD1320	SL 6–27
AD1321	SL 6–33
AD1322	D
*AD1324	SL 6–45
AD1334	C II
*AD1341	C II
AD1362	C II
AD1376	C II
AD1377	C II
*AD1378	C II
AD1380	C II
*AD1382	C II
*AD1385	C II
AD1403/1403A	C II
*AD1671	C II
*AD1674	C II
*AD1849	D
*AD1851	AV, C I
AD1856	AV, C I
AD1860	AV, C I
*AD1861	AV, C I
*AD1862	AV, C I
*AD1864	AV, C I
*AD1865	AV, C I
*AD1866	AV, C I
*AD1868	AV, C I
*AD1876	AV, C II
*AD1878	AV, C II
*AD1879	AV, C II
*AD1885	AV

Model	Page†
AD2004	D
AD2006	D
AD2010	C I
AD2020	D
AD2021	C I
AD2026	C I
AD2700	C II
AD2701	C II
AD2702	C II
AD2710	C II
AD2712	C II
AD5200 Series	D
AD5210 Series	D
AD5539	AV, A 2–415
*AD7001	C I
*AD7002	C I
*AD7005	C I
*AD7008	C I
AD7110	D
AD7111	AV, C I
AD7118	AV, C I
AD7224	C I
AD7225	C I
AD7226	C I
AD7228	C I
*AD7228A	C I
*AD7233	C I
AD7237	C I
AD7240	D
*AD7242	C I
*AD7243	C I
*AD7244	C I
AD7245	C I
*AD7245A	C I
AD7247	C I
AD7248	C I
*AD7248A	C I
*AD7306	C I
AD7341	C I
AD7371	C I
AD7501	C II
AD7502	C II
AD7503	C II
AD7506	C II
AD7507	C II
AD7510DI	C II
AD7511DI	C II
AD7512DI	C II
AD7520	D
AD7521	D
AD7522	D
AD7523	D

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Model	Page†
AD7524	C I
AD7525	D
AD7528	C I
AD7530	D
AD7531	D
AD7533	C I
AD7534	C I
AD7535	C I
AD7536	C I
AD7537	C I
AD7538	C I
AD7541	D
AD7541A	C I
AD7542	C I
AD7543	C I
AD7545	C I
AD7545A	C I
AD7546	D
AD7547	C I
AD7548	C I
AD7549	C I
*AD7564	C I
*AD7568	C I
AD7569	C II
AD7572	C II
*AD7572A	C II
AD7574	C II
AD7575	C II
AD7576	D
AD7578	C II
AD7579	C II
AD7580	C II
AD7581	C II
AD7582	C II
*AD7586	C II
AD7590DI	C II
AD7591DI	C II
AD7592DI	C II
AD7628	C I
AD7669	C II
AD7672	C II
*AD7701	C II
*AD7703	C II
*AD7710	C II
*AD7711	C II
*AD7712	C II
*AD7713	C II
AD7716 (AD79024)	C II
AD7769	C II
AD7772	D
*AD7773	C II
*AD7774	C II
*AD7775	C II
*AD7776	C II
*AD7777	C II
*AD7778	C II
AD7820	C II
AD7821	C II
AD7824	C II
AD7828	C II
*AD7837	C I
AD7840	C I
AD7845	C I
AD7846	C I
*AD7847	C I
AD7848	C I
*AD7868	C II
*AD7869	C II
AD7870	C II
AD7871	C II
AD7872	C II
*AD7874	C II
*AD7875	C II
*AD7876	C II
AD7878	C II
*AD7880	C II
*AD7884	C II
*AD7885	C II
*AD7886	C II
*AD7890	C II
*AD7891	C II
*AD7892	C II
*AD7893	C II
AD9000	C II
AD9002	C II
AD9003	C II
*AD9003A	D
*AD9005A	C II
AD9006	C II
*AD9007	D
AD9012	C II
*AD9014	C II
AD9016	C II
*AD9020	AV, C II
AD9028	C II
*AD9032	C II
*AD9034	C II
AD9038	C II
*AD9040	C II
AD9048	AV, C II
*AD9058	C II
*AD9060	AV, C II
*AD9100	C II
*AD9101	D

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Model	Page†
AD9300	AV, C II
AD9500	SL 6–57
AD9501	SL 6–67
AD9502	D
*AD9505	A 6–79
AD9610	A 2–431
AD9611	D
AD9617	A 2–439
AD9618	A 2–447
*AD9620	A 2–455
AD9630	A 2–461
AD9686	D
AD9696	A 3–13
AD9698	A 3–13
AD9701	C I
AD9712	C I
*AD9712B	D
AD9713	C I
*AD9713B	D
*AD9720	C I
*AD9721	C I
AD9768	C I
AD9901	C I
*AD9950	C I
*AD22001	SL 11–5
*AD22002	SL 11–5
*AD22030	SL 11–6
*AD22050	SL 11–6
*AD22055	SL 11–7
*AD22100	SL 11–7
*AD22150	SL 11–8
*AD22180	SL 11–8
*AD22181	SL 11–9
AD75004	C I
*AD75019	C II
*AD75062	A 4–107
*AD75068	A 4–107
*AD75069	C I
*AD75089	C I
*AD75090	C I
*AD79024 (AD7716)	C II
AD96685	A 3–21
AD96687	A 3–21
AD ADC71	C II
AD ADC72	C II
AD ADC80	C II
AD ADC84	C II
AD ADC85	C II
*ADC-170	C II
ADC-908	D
ADC-910	C II
ADC-912	D

Model	Page†
*ADC-912A	C II
ADC1130/1131	D
ADC1140	C II
ADC1143	D
AD DAC-08	D
AD DAC71	D
AD DAC72	D
AD DAC80	C I
AD DAC85	C I
AD DAC87	C I
*ADDS-21XX-SOFTWARE	D
*ADDS-21XX-EZ	D
*ADDS-2100A-ICE	AV, D
*ADDS-21XX-ICE	D
*ADDS-21XXX-SOFTWARE	D
*ADDS-21XXX-EZ	D
ADEB770	D
ADG201A	C II
ADG201HS	C II
ADG202A	C II
ADG211A	C II
ADG212A	C II
ADG221	C II
ADG222	C II
*ADG408	C II
*ADG409	C II
*ADG411	C II
*ADG412	C II
*ADG441	C II
*ADG442	C II
*ADG444	C II
*ADG445	C II
ADG506A	C II
ADG507A	C II
ADG508A	C II
ADG509A	C II
ADG526A	C II
ADG527A	C II
ADG528A	C II
ADG529A	C II
AD OP-07	A 2–467
AD OP-27	A 2–473
AD OP-37	A 2–481
ADSP-1008A	D
ADSP-1009A	D
ADSP-1010A	D
ADSP-1010B	D
ADSP-1012A	D
ADSP-1016A	D
ADSP-1024A	D
ADSP-1080A	D
ADSP-1081A	D

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Model	Page†
ADSP-1101	D
ADSP-1110A	D
ADSP-1401	D
ADSP-1402	D
ADSP-1410	D
ADSP-2100	AV, D
ADSP-2100A	AV, C I, SL 12–2
ADSP-2101	AV, C I, SL 12–2
ADSP-2102	AV, C I, SL 12–2
*ADSP-2105	C I, SL 12–2
*ADSP-2106	C I, SL 12–2
*ADSP-2111	AV, C I, SL-12–2
*ADSP-2112	C I, SL 12–2
*ADSP-21msp50	C I, SL 12–2
*ADSP-21msp51	C I, SL 12–2
ADSP-3128A	D
ADSP-3201	D
ADSP-3202	D
ADSP-3210	D
ADSP-3211	D
ADSP-3212	D
ADSP-3220	D
ADSP-3221	D
ADSP-3222	D
*ADSP-21010	D, SL 12–2
*ADSP-21020	AV, C I, SL 12–2
*ADV101	C I
ADV453	AV, C I
ADV471	AV, C I
*ADV473	C I
*ADV475	C I
ADV476	AV, C I
*ADV477	C I
ADV478	AV, C I
*ADV7120	AV, C I
*ADV7121	AV, C I
*ADV7122	AV, C I
*ADV7141	AV, C I
*ADV7146	AV, C I
*ADV7148	AV, C I
*ADV7150	C I
*ADV7151	C I
*ADV7152	C I
ADVFC32	C II
*ADXL02	SL 11–9
*ADXL50	SL 7–27, SL 11–10
AMP-01	A 4–115
AMP-02	A 4–137
AMP-03	A 4–149
*AMP-04	A 4–159
AMP-05	A 4–165
ASICs	A 6–1, SL 13–1
BUF-03	A 2–489

Model	Page†
CAV-1210	D
CMP-01	A 3–27
C/MP-02	A 3–35
CMP-04	A 3–43
CMP-05	A 3–51
CMP-08	D
CMP-404	D
DAC-QS	D
DAC-QZ	D
DAC-01	D
DAC-02/03	D
DAC-05	D
DAC-06	D
DAC-08	C I
DAC-10	C I
DAC-12QS	D
*DAC-16	C I
DAC-20	D
DAC71/72 (see AD DAC71/72)	
DAC80 (see AD DAC80)	
DAC85 (see AD DAC85)	
DAC-86	D
DAC87 (see AD DAC87)	
DAC-88	D
DAC-89	D
DAC-100	C I
DAC-210	D
DAC-312	C I
DAC-888	D
DAC1136	D
DAC1138	D
DAC1146	D
DAC-1408A	D
DAC-1508A	D
DAC-8012	C I
DAC-8043	C I
DAC-8143	C I
DAC-8212	D
DAC-8221	C I
DAC-8222	C I
DAC-8228	C I
DAC-8229	C I
DAC-8248	C I
DAC-8408	AV, C I
DAC-8412	C I
*DAC-8413	C I
*DAC-8420	D
DAC-8426	C I
DAC-8800	AV, C I
DAC-8840	AV, C I
*DAC-8841	AV, C I
DAS1152	C II
DAS1153	D

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Model	Page†
DAS1157	D
DAS1158	C II
DAS1159	C II
DRC1745	C I
DRC1746	C I
HDS-1240E	D
HDS-1250	D
HOS-050A	D
HOS-060	D
HTC-0300A	D
HTS-0010	D
HTS-0025	D
*IPA1764	C I
JM38510/11301/11302	D
LIU-01	C I
MAT-01	SL 8–5
MAT-02	SL 8–11
MAT-03	SL 8–23
MAT-04	AV, SL 8–33
MUX-08	C II
MUX-16	C II
MUX-24	C I
MUX-28	C II
MUX-88	D
OP-01	A 2–497
OP-02	A 2–503
OP-04	A 2–511
OP-05	A 2–519
OP-06	A 2–529
OP-07	A 2–537
OP-08	D
OP-09	A 2–547
OP-10	A 2–555
OP-11	A 2–547
OP-12	A 2–567
OP-14	A 2–511
OP-15	A 2–571
OP-16	A 2–571
OP-17	A 2–571
OP-20	A 2–585
OP-21	A 2–591
OP-22	A 2–597
OP-27	A 2–609
OP-32	A 2–621
OP-37	A 2–633
OP-41	A 2–645
OP-42	A 2–657
OP-43	D
OP-44	D
OP-50	A 2–671
OP-61	AV, A 2–683
OP-64	AV, A 2–701

Model	Page†
OP-65	D
OP-77	A 2–715
OP-80	A 2–727
OP-90	A 2–739
OP-97	A 2–751
OP-111	D
*OP-113	A 2–761
OP-147	D
OP-150	D
*OP-160	A 2–765
OP-166	D
*OP-176	A 2–789
OP-177	A 2–791
OP-200	A 2–803
OP-207	A 2–813
*OP-213	A 2–761
OP-215	A 2–819
OP-220	A 2–827
OP-221	A 2–835
OP-227	A 2–843
OP-249	AV, A 2–855
OP-260	AV, A 2–873
OP-270	A 2–893
OP-271	AV, A 2–909
*OP-275	AV, A 2–919
*OP-282	A 2–927
*OP-285	A 2–939
OP-290	A 2–943
*OP-295	A 2–953
*OP-297	A 2–959
OP-400	A 2–975
*OP-413	A 2–761
OP-420	A 2–987
OP-421	A 2–993
*OP-467	A 2–999
OP-470	A 2–1005
OP-471	AV, A 2–1021
*OP-482	A 2–927
OP-490	A 2–1037
*OP-495	A 2–953
*OP-497	A 2–1049
*OSC1758	C I
PKD-01	AV, SL 7–33
PM-0828	D
PM-108	A 2–1061
PM-111/211	A 3–59
PM-119/219	D
PM-139	A 3–65
PM-148/248	D
PM-155	D
PM-155A	A 2–1065
PM-156	D

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PM-156A	A 2–1065
PM-157	D
PM-157A	A 2–1065
PM-211	A 3–59
PM-239	A 3–65
PM-248	D
PM-355	D
PM-356	D
PM-562	D
PM-725	D
PM-741	D
PM-747	D
PM-1008	D
PM-1012	A 2–1065
PM-2108	A 2–1061
*PM-6012	C I
PM-7224	C I
PM-7226	C I
PM-7226A	C I
PM-7524	C I
PM-7528	C I
PM-7533	C I
PM-7541	D
PM-7541A	C I
PM-7542	C I
PM-7543	C I
PM-7545	C I
PM-7548	C I
PM-7574	D
PM-7628	C I
PM-7645	C I
REF-01	C II
REF-02	C II
REF-03	C II
REF-05	C II
REF-08	C II
REF-10	C II
REF-43	C II
RPT-82	C I
RPT-83	C I
RPT-85	C I
RPT-86	C I
RPT-87	C I
SDC1740/RDC1740	C I
SDC1741/RDC1741	C I
SDC1742/RDC1742	C I
SHA-1144	D
SMP-04	C II
SMP-08	C II
SMP-10	C II
SMP-11	C II
*SMP-18	C II

Model	Page†
SMP-81	D
SSM-2013	AV
SSM-2014	AV
SSM-2015	AV
SSM-2016	AV, A 4–185
SSM-2017	AV, A 4–193
SSM-2018	AV
SSM-2024	AV
SSM-2100	D
SSM-2110	AV
SSM-2120	AV
SSM-2122	AV
SSM-2125	AV
SSM-2126	AV
SSM-2131	AV
SSM-2132	D
SSM-2134	AV
SSM-2139	AV
SSM-2141	AV, A 4–201
SSM-2142	AV, A 4–207
*SSM-2143	AV, A 4–213
SSM-2210	AV
SSM-2220	AV
SSM-2300	D
SSM-2402	AV, C II
*SSM-2404	AV, C II
SSM-2412	AV, C II
SW-01	D
SW-02	D
SW-06	C II
SW-201	C II
SW-202	C II
SW-7510	D
SW-7511	D
*TMP-01	SL 9–25
1B21	SL 10–63
1B22	SL 10–67
1B31	SL 10–71
1B32	SL 10–79
1B41	SL 10–87
1B51	SL 10–91
*1S74	C I
2B20	SL 10–95
2B22	SL 10–99
2B23	SL 10–103
2B24	D
2B30	SL 10–107
2B31	SL 10–107
2B34	D
2B50	SL 10–113
2B52	D
2B53	D

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Model	Page†
2B54/2B55	SL 10–117
2B56	D
2B57	D
2B58	D
2B59	D
2S50	C I
2S54	C I
2S56	C I
2S58	C I
2S80A	C I
2S81A	C I
2S82A	C I
3B Series	SL 10–3
4B Series	D
5B Series	SL 10-3
6B Series	SL 10–3
*7B Series	SL 10–123
40	D
171	D
233	D
277	D
281	A 5–69
284J	A 5–63
285	D
286J	A 5–69
289	A 5–75
290	D
290A	A 5–81
292	D
292A	A 5–81
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†A = *Amplifier Reference Manual*; AV = *Audio/Video Reference Manual*; C I = *Data Converter Reference Manual, Volume I*; C II = *Data Converter Reference Manual, Volume II*; D = *Data Sheet*; ; SL = *Special Linear Reference Manual.*

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